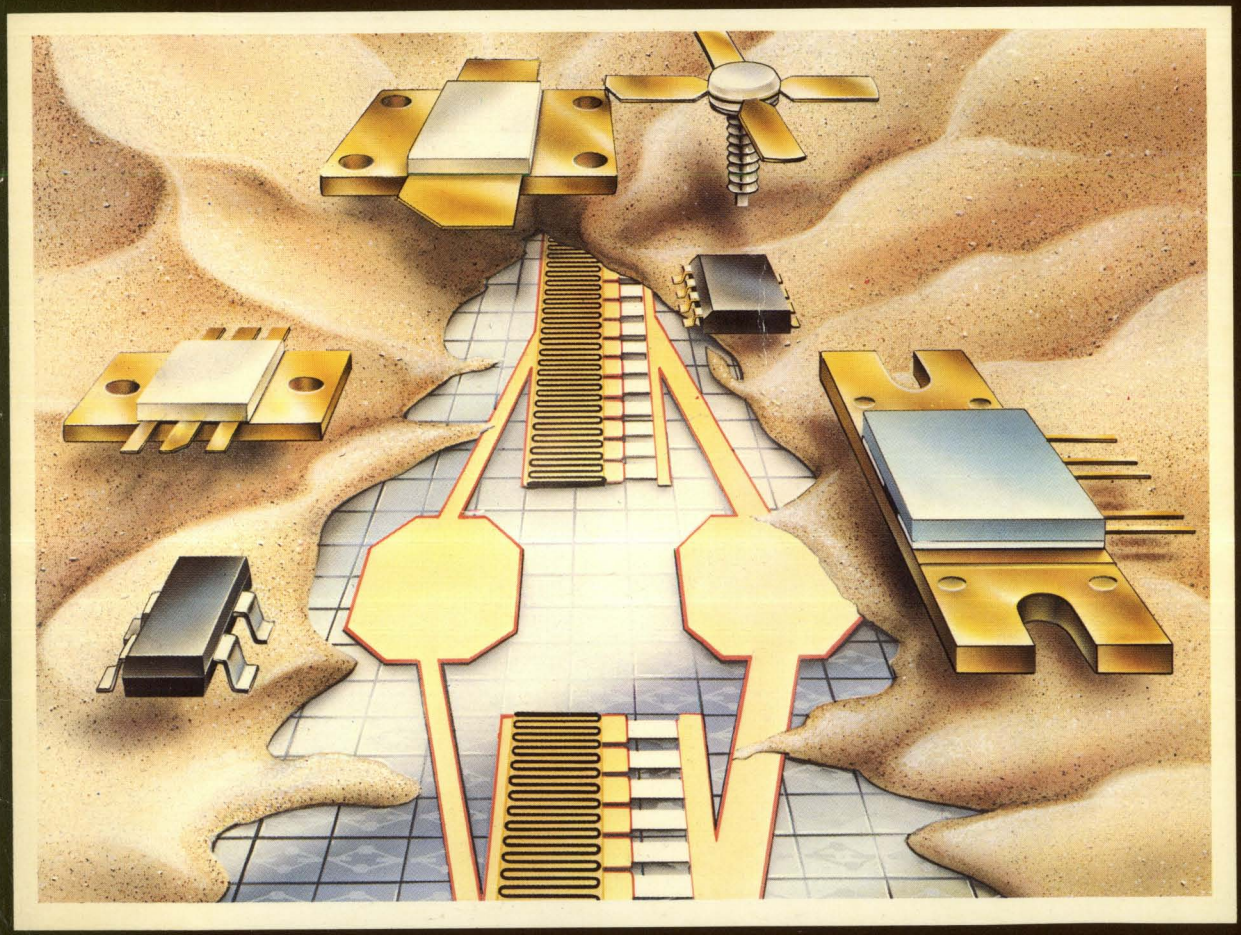
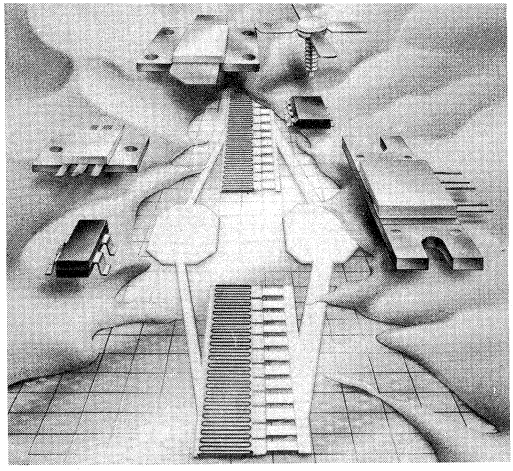
DL 110
REV 2

MOTOROLA



RF DEVICE DATA



Index and Cross-Reference 1

Selector Guide 2

Transistors 3

Amplifiers 4

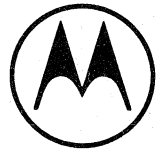
Tuning, Hot Carrier and PIN Diodes 5

Technical Information 6

Transistor Design

Application Notes

Reliability and Quality Assurance



MOTOROLA
RF DATA MANUAL

Prepared by
Technical Information Center

The Fourth Edition of the RF Data Manual has been updated to incorporate the latest changes since the last printing. There are several hundred devices along with a selection of application notes, article reprints and engineering bulletins which cover RF Power and Small-Signal Transistors, RF Amplifiers, and Tuning Diodes.

Motorola's RF family now includes Dual-Gate GaAs FETs for low-cost operation to 1 GHz; state-of-the-art, 800 MHz Discretes and Hybrids for Cellular Base Station and Mobile Radio Designs; unique RF TMOS Power FETs with high-gain and improved high-order IMD characteristics; and Fine-line, Bipolar Small-Signal Transistors for enhanced gain and NF performance.

The information in this book has been carefully checked; no responsibility, however, is assumed for inaccuracies. Furthermore, this information does not convey to the purchaser of microelectronic devices any license under the patent rights of the manufacturer.

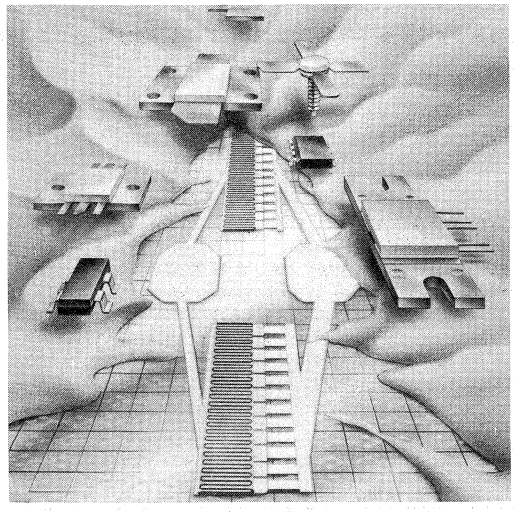
Fourth Edition
First Printing
©MOTOROLA INC., 1986
Previous Printing ©1983
"All Rights Reserved"

Printed in U.S.A.

Designer's, Epicap and TMOS are trademarks of Motorola Inc.

Annular Semiconductors patented by Motorola Inc.

Motorola reserves the right to make changes without further notice to any products herein to improve reliability, function or design. Motorola does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights nor the rights of others. Motorola and Ⓜ are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Employment Opportunity/ Affirmative Action Employer.



Index and Cross-Reference

1

Alphanumeric Cross Reference

Considerable judgment is necessary in creating a cross-reference for RF devices. The only real proof of a replacement is through direct substitution in a particular circuit or system. Guidelines used to compare low power parts were dc voltage ratings, cutoff frequency, current rating, junction capacitance and noise figure. For high power parts the parameters used were dc voltage ratings, output power, gain, frequency of operation and output capacitance.

A direct replacement will always be in a package that is the same as or for all practical purposes equivalent to the package of the original device. Similar replacement are generally but not always in packages that are identical or can be readily substituted; for example a .280" stud package in place of a .380" stud package or a 100 mil ceramic package in place of a 80 mil ceramic package.

A similar replacement may also be somewhat different in electrical specifications such as lower gain or higher noise figure. However, it is Motorola's closest device to the original and is considered sufficiently similar to warrant further investigation by the device user.

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
2N1491		MRF586	3-649
2N2631		2N3553	3-8
2N2857	2N2857		3-2
2N2876		2N3375	—
2N2947		MRF485	3-544
2N3118		MRF531	3-588
2N3119		MRF531	3-588
2N3296		2N5641	3-64
2N3309A		2N3553	3-8
2N3375	2N3375		—
2N3478		2N5179	3-54
2N3553	2N3553		3-8
2N3600	2N5179		3-54
2N3632	2N3632		—
2N3733		2N3632	—
2N3818		2N3632	—
2N3839	2N3839		—
2N3866	2N3866		3-10
2N3866A	2N3866A		3-10
2N3880		2N5032	3-36
2N3924	2N3924		3-14
2N3925		2N5589	—
2N3926	2N3926		—
2N3927	2N3927		—
2N3948	2N3948		3-17
2N3950	2N3950		—
2N3959	2N3959		3-19
2N3960	2N3960		3-19
2N3961		2N5641	3-64
2N4012	2N4012		—
2N4040		2N5636	—
2N4041		2N5635	—
2N4072	2N4072		—
2N4073	2N4073		—
2N4127		2N5642	3-67
2N4128		2N5642	3-67
2N4130		MRF464	3-520
2N4416	2N4416		—
2N4427	2N4427		3-23
2N4428	2N4428		3-25

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
2N4440	2N4440		—
2N4932	2N3927		—
2N4933	2N5071		—
2N4957	2N4957		3-27
2N4958	2N4958		3-27
2N4959	2N4959		3-27
2N5016	2N5016		—
2N5031	2N5031		3-36
2N5032	2N5032		3-36
2N5053	2N6305		3-120
2N5054	2N6304		3-120
2N5070	2N5070		—
2N5071	2N5071		—
2N5090	2N5090		—
2N5102		2N5071	—
2N5108	2N5108		3-40
2N5109	2N5109		3-44
2N5160	2N5160		3-50
2N5179	2N5179		3-54
2N5180		2N5179	3-54
2N5262		MRF531	3-588
2N5421	2N4427		3-23
2N5422	MRF607		3-663
2N5423	2N3926		—
2N5424	2N3927		—
2N5583	2N5583		3-60
2N5589	2N5589		—
2N5590	2N5590		—
2N5591	2N5591		—
2N5635		MRF5174	3-915
2N5636		MRF331	3-422
2N5637		MRF323	3-402
2N5641	2N5641		3-64
2N5642	2N5642		3-67
2N5643	2N5643		3-70
2N5644	2N5644		—
2N5645	2N5645		—
2N5646		MRF653	3-694
2N5687	MRF230		—
2N5688		2N5847	—

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
2N5689		2N5847	—
2N5690		2N5848	—
2N5691		2N5849	—
2N5697	MRF515		3-567
2N5698		2N5644	—
2N5699		2N5945	3-90
2N5710	2N4073		—
2N5711		2N5641	3-64
2N5712		2N5642	3-67
2N5713		2N5643	3-70
2N5773		MRF5174	3-915
2N5774		MRF331	3-422
2N5775		MRF5177A	3-924
2N5829		2N4957	3-27
2N5834	2N3553		3-8
2N5835	2N5835		3-73
2N5836	2N5836		3-73
2N5837	2N5837		3-73
2N5841	2N5841		—
2N5842	2N5842		—
2N5846		MRF231	—
2N5847		2N6081	3-104
2N5848	2N5848		—
2N5849	2N5849		3-79
2N5862	2N5862		—
2N5913	MRF607		3-663
2N5914		2N5944	3-90
2N5915		2N5946	3-90
2N5916		MRF5174	3-915
2N5917		MRF5174	3-915
2N5918		MRF321	3-398
2N5919A		MRF323	3-402
2N5941	MRF466		3-524
2N5942		MRF464	3-520
2N5943	2N5943		3-83
2N5944	2N5944		3-90
2N5945	2N5945		3-90
2N5946	2N5946		3-90
2N5947	2N5947		3-97
2N5992		MRF232	3-337
2N5993		MRF234	3-345
2N5994		MRF315	3-386
2N5995		MRF212	—
2N5996		2N5591	—
2N6080	2N6080		3-101
2N6081	2N6081	MRF221	3-104
2N6082	2N6082		3-107
2N6083	2N6083		3-110
2N6084	2N6084	MRF224	3-113
2N6093		MRF464	3-520
2N6094	2N6094		—
2N6095	2N6095		—
2N6096	2N6096		—
2N6097	2N6097		—
2N6104		MRF5177A	3-924
2N6105		MRF5177A	3-924
2N6136	2N6136		—
2N6166	2N6166		3-116
2N6197	2N5641		3-64
2N6198	2N5642		3-67

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
2N6199	2N5643		3-70
2N6200		2N5643	3-70
2N6201		2N6166	3-116
2N6202		2N5635	—
2N6203		MRF331	3-422
2N6204		MRF323	3-402
2N6205	MRF5177A		3-924
2N6206		MRF891	3-772
2N6207		MRF892	3-776
2N6255	2N6255		—
2N6256	2N6256		—
2N6304	2N6304		3-120
2N6305	2N6305		3-120
2N6366		MRF231	—
2N6367		MRF433	3-493
2N6368	MRF460		3-515
2N6370	MRF410		3-457
2N6439	2N6439		3-125
2N6455	MRF449A		3-499
2N6456	MRF450A		3-502
2N6457	MRF492A		3-552
2N6458	MRF406		3-453
2N6459	MRF450		3-502
2N6460	MRF492		3-552
2N6603	2N6603		3-129
2N6604	2N6604		3-133
2SA711	2N3959		3-19
2SA800	MM4049		3-173
2SA1161	MPS536		3-192
2SA1223		MRF536	3-173
2SA1228	MM4049		3-173
2SA1230		MRF536	3-173
2SA1245	MMBR4957		3-189
2SC319	2N4427		3-23
2SC320	MRF607		3-663
2SC567	MRF502		3-559
2SC568	MRF501		3-559
2SC571	2N3924		3-14
2SC572	2N3926		—
2SC573	2N3927		—
2SC585	2N3632		—
2SC597	2N3553		3-8
2SC598		2N4440	—
2SC600	2N3632		—
2SC628	MRF225		—
2SC635	2N3375		—
2SC636	2N3632		—
2SC637	2N3926		—
2SC638	2N3927		—
2SC651	2N4428		3-25
2SC652		2N4428	3-25
2SC730	2N4427		3-23
2SC821		2N4427	3-23
2SC822	2N4427		3-23
2SC823		2N5109	3-44
2SC824		2N5943	3-83
2SC831	2N5016		—
2SC852		2N5943	3-83
2SC890		MRF515	3-567
2SC891	2N5645		—

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
2SC892		MRF653	3-694
2SC988		MRF914	3-804
2SC988A	MRF914		3-804
2SC990		2N5637	—
2SC994		2N4427	3-23
2SC998		MRF237	3-349
2SC1043	MRF587		3-649
2SC1044	2N6304		3-120
2SC1081		MRF654	3-698
2SC1090-1		2N6604	3-133
2SC1119		MRF901	3-788
2SC1239		MRF475	3-528
2SC1251		MRF587	3-649
2SC1252		MRF586	3-649
2SC1253		MRF586	3-649
2SC1254	2N6304		3-120
2SC1256	2N6255		—
2SC1257		2N6081	3-104
2SC1258	2N6081		3-104
2SC1259		2N6083	3-110
2SC1260	2N2857		3-2
2SC1268		MRF572	3-627
2SC1275	2N2857		3-2
2SC1297		2N5643	3-70
2SC1298		MRF315A	3-386
2SC1306		MRF485	3-544
2SC1307	MRF485		3-544
2SC1329	2N5849		3-79
2SC1336		MRF572	3-627
2SC1365	MRF586		3-649
2SC1366	MRF586		3-649
2SC1424	MRF914		3-804
2SC1426		MRF965	3-147
2SC1560		MRF572	3-627
2SC1589		MRF260	3-362
2SC1590		MRF262	3-370
2SC1591		MRF262	3-370
2SC1592		MRF587	3-649
2SC1593		MRF587	3-649
2SC1594		MRF587	3-649
2SC1600		MRF586	3-649
2SC1603		MRF752	3-710
2SC1604		MRF750	3-706
2SC1605A		MRF2628	3-907
2SC1606		2N6080	3-101
2SC1656		MRF903	—
2SC1678	MRF476		3-532
2SC1689		MRF315A	3-386
2SC1729		MRF2628	3-907
2SC1763		MRF464	3-520
2SC1764	MRF464		3-520
2SC1804		MRF321	3-398
2SC1805		MRF323	3-402
2SC1807		BFY90	3-161
2SC1808		MRF652	3-690
2SC1945	MRF479		3-540
2SC1946		MRF222	—
2SC1946A		MRF1946A	3-862
2SC1947	MRF237		3-349
2SC1949		MRF962	3-147

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
2SC1955	MRF237		3-349
2SC1966		2N5945	3-90
2SC1967		2N5946	3-90
2SC1968A		MRF641	3-674
2SC1969	MRF475		3-528
2SC1970		MRF553	3-606
2SC1971	MRF260		3-362
2SC1972	MRF262		3-370
2SC1988	MRF914		3-804
2SC2025		MRF965	3-147
2SC2026	MPS911		3-211
2SC2040	MRF587		3-649
2SC2065		MRF587	3-649
2SC2075	MRF476		3-532
2SC2081	2N5944		3-90
2SC2082		2N5946	3-90
2SC2083		MRF654	3-698
2SC2098	MRF475		3-528
2SC2099	MRF406		3-453
2SC2100	MRF412		3-461
2SC2101		2N6081	3-104
2SC2102	MRF2628		3-907
2SC2103A	MRF1946A		3-862
2SC2104		MRF652	3-690
2SC2105		MRF653	3-694
2SC2106		MRF654	3-698
2SC2131	MRF629		—
2SC2132		MRF646	3-682
2SC2148		2N6604	3-133
2SC2149		MRF572	3-627
2SC2174	MRF572		3-627
2SC2178		MRF221	3-104
2SC2181	MRF224		3-113
2SC2207	MRF475		3-528
2SC2217		MRF572	3-627
2SC2218		MRF572	3-627
2SC2222		2N5946	3-90
2SC2280		2N5944	3-90
2SC2281		2N5946	3-90
2SC2282	MRF2628		3-907
2SC2290	MRF454		3-507
2SC2329		MRF607	3-663
2SC2350	MRF911		3-801
2SC2351	MMBR571		3-198
2SC2367		MRF572	3-627
2SC2369	MRF2369		3-902
2SC2395	MRF433		3-493
2SC2420	MRF1946		3-862
2SC2494K		MRF750	3-706
2SC2494M		MRF750	3-706
2SC2495K		MRF752	3-710
2SC2495M		MRF752	3-710
2SC2496A		MRF646	3-682
2SC2498	MPS911		3-211
2SC2499	MPS901		3-207
2SC2508	MRF1946		3-862
2SC2509	MRF479		3-540
2SC2510	MRF422		3-469
2SC2570	MPS571		3-198
2SC2586	MRF629		—

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
2SC2627		2N6080	3-101
2SC2628		MRF2628	3-907
2SC2629		MRF1946A	3-862
2SC2630		MRF247	3-355
2SC2642		MRF641	3-674
2SC2643		MRF644	3-678
2SC2652		MRF448	3-495
2SC2694	MRF247		3-355
2SC2753	MPS571		3-198
2SC2759	MMBR911		3-211
2SC2782	MRF247		3-355
2SC2783	MRF646		3-682
2SC2876		MRF571	3-627
2SC2879	MRF421		3-465
2SC2886		MRF331	3-422
2SC2887	MRF331		3-422
2SC2888		MRF314A	3-382
2SC2889		MRF315A	3-386
2SC2890		MRF316	3-390
2SC2891	MRF317		3-394
2SC2892	MRF5174		3-915
2SC2893	MRF321		3-398
2SC2894		MRF323	3-402
2SC2895	MRF325		3-406
2SC2896	MRF309		3-378
2SC2897	MRF327		3-414
2SC2905		MRF646	3-682
2SC2906AK		MRF754	3-714
2SC2906AM		MRF754	3-714
2SC2915	MRF648		3-686
2SC2917	MRF247		3-355
2SC2931		MRF557	3-615
2SC2932		MRF840	3-734
2SC2933		MRF842	3-744
2SC2946A		MRF646	3-682
2SC2952		MRF586	3-649
2SC2953		MRF587	3-649
2SC2954	BFQ19		3-138
2SC3011		MMBR901	3-183
2SC3019	MRF559		3-620
2SC3020		MRF652	3-690
2SC3021		MRF653	3-694
2SC3022		MRF644	3-678
2SC3099	MMBR901		3-183
2SC3101	MRF630		3-670
2SC3102		MRF648	3-686
2SC3103		MRF752	3-710
2SC3104		MRF754	3-714
2SC3105		MRF844	3-754
2SC3120		MMBR911	3-211
2SC3133	MRF479		3-540
2SC3139		MRF890	3-760
2SC3147		MRF247	3-355
2SC3268	MXR571		3-198
2SC3282	MRF842		3-744
2SC3283	MRF844		3-754
2SC3301		MXR571	3-198
2SC3302	MRF571		3-627
2SC3355		MPS571	3-198
2SC3356		MMBR571	3-198

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
2SC3358		MRF572	3-627
2SC3429	MMBR571		3-198
2SC3445		MMBR571	3-198
2SC3582		MPS571	3-198
2SC3583		MMBR571	3-198
2SC3584		MRF571	3-627
2SC3604		MRF572	3-627
8BSE10	MRF892		3-776
8BSE30	MRF894		3-780
8MOB1	MRF838A		3-724
8MOB2		MRF839	3-728
8MOB5		MRF841	3-738
8MOB5E	MRF839F		3-728
8MOB10		MRF840	3-734
8MOB15	MRF842		3-744
8MOB15E	MRF873		3-764
8MOB25	MRF844		3-754
8MOB30		MRF844	3-754
8MOB45	MRF846		3-757
9BSE2	MRF890		3-768
9BSE10		MRF892	3-776
9BSE35		MRF894	3-780
9BSE55		MRF898	3-784
0104-100		MRF392	3-442
0105-50		MRF390	3-438
0105-100		MRF392	3-442
0204-50	MRF390		3-438
0204-125	MRF392		3-442
0510-10		MRF892	3-776
0510-25		MRF894	3-780
0912-7		MRF1008MC	3-830
0912-25		MRF1035MC	3-838
0912-45		MRF1090MC	3-842
0912-125A		MRF1150MC	3-850
0912-125B		MRF1150MC	3-850
2001	MRF2001		3-866
2003	MRF2003		3-874
2005	MRF2005		3-882
2010	MRF2010		3-890
2010M	MRF2010M		3-894
2015M	MRF2016M		3-898
2023-1.5		MRF2001M	3-870
2023-1.5T		MRF2001M	3-870
2023-3		MRF2003M	3-878
2023-3T		MRF2003M	3-878
2023-6		MRF2005M	3-886
2023-6T		MRF2005M	3-886
2023-12		MRF2010M	3-894
2023-16		MRF2016M	3-898
2301		MRF2003	3-874
2304		MRF2005	3-882
2307		MRF2010	3-890
35821B		2N6603	3-129
35821E		2N6603	3-129
35822B		2N6603	3-129
35822E		2N6603	3-129
35824A		MRF904	3-794
35825B		2N6603	3-129
35825E		2N6603	3-129
40006		MRF464	3-520

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
40080		MRF476	3-532
40081		MRF476	3-532
40082		MRF475	3-528
40240	MRF501		3-559
40279	2N3375		—
40280	2N4427		3-23
40281	2N3926		—
40282	2N3927		—
40290	2N3553		3-8
40291	2N3632		—
40292	2N3632		—
40340	2N5071		—
40341	2N3950		—
40446		MRF475	3-528
40578	2N3866		3-10
40581		MRF475	3-528
40582		MRF475	3-528
40608	2N5943		3-83
40637A		2N4072	—
40665		2N3375	—
40666		2N3632	—
40893	2N5946		3-90
40894		2N5179	3-54
40895		2N5179	3-54
40896		2N5179	3-54
40897		2N5179	3-54
40915	2N5031		3-36
40934	MRF616		—
40936	2N5070		—
40940	MRF5175		3-918
40941		MRF313	3-380
40953	MRF207		—
40954	MRF212		—
40955	MRF1946A		3-862
40964	MRF515		3-567
40965	MRF515		3-567
40967	2N5944		3-90
40968	2N5946		3-90
40970	MRF644		3-678
40971	MRF646		3-682
40972	MRF607		3-663
40973	2N6081		3-104
40974	2N6082		3-107
40975	2N3553		3-8
40976	2N3553		3-8
40977	2N5642		3-67
41009	MRF616		—
41009A	2N5944		3-90
41010	2N5946		3-90
41024	2N5108		3-40
41025	MRF321		3-398
41026	MRF323		3-402
41027	MRF321		3-398
41028	MRF323		3-402
41038	MRF905		3-799
80091	MRF511		3-561
80099	MRF525		3-584
80167	MRF511		3-561
80231	MRF511		3-561
A3-12		2N5847	—

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
A3-28		2N5641	3-64
A15-12	MRF406		3-453
A25-28	MRF314A		3-382
A80-12		MRF492	3-552
A80-12G		MRF492	3-552
A210	MRF517		3-571
A234	MRF581		3-639
A400	MRF904		3-794
A401	MRF914		3-804
A402		MRF904	3-794
A403		MRF914	3-804
A406		MRF965	3-147
A440		MM4049	3-173
A485		BFX89	3-161
A486		BFW92A	3-156
A490	BFX89		3-161
A500		2N6603	3-129
A501	2N6603		3-129
A510		2N6604	3-133
A511	2N6604		3-133
A516		MRF581	3-639
A522		MRF521	3-576
A523		MRF521	3-576
A561	MRF962		3-147
A573	MRF572		3-627
A574		MRF572	3-627
AP15-12	MRF261		3-366
AP30-12	MRF477		3-536
AP30-12L	MRF477		3-536
AT004		MRF904	3-794
AT0017	MRF904		3-794
AT0017A	MRF904		3-794
AT25		MRF901	3-788
AT25A		MRF901	3-788
AT25B		MRF901	3-788
AT0045	MRF904		3-794
AT50	BFR90		3-139
AT51	BFR90		3-139
AT52	BFR90		3-139
AT1425		BFR90	3-139
AT1825	2N6604		3-133
AT1845	2N6603		3-129
AT1845A	2N6603		3-129
AT2625		2N6603	3-129
AT2645		2N6603	3-129
AT2645A		2N6603	3-129
AT2715	MRF962		3-147
B1-12		MRF553	3-606
B2-8Z		2N6080	3-101
B3-12	2N6080		3-101
B3-28	2N5641		3-64
B5-8Z		2N6081	3-104
B8-12	MRF212		—
B12-12	2N6081		3-104
B12-28	2N5642		3-67
B15-12	2N6081		3-104
B25-12	2N6082		3-107
B25-28	2N5643		3-70
B30-12	2N6083		3-110
B40-12A	2N6084		3-113

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
B40-28		2N5643	3-70
B45-12	2N6084		3-113
B70-28		2N6166	3-116
BAL0105-50		MRF390	3-438
BAL0105-100		MRF392	3-442
BAM20	MRF314		3-382
BAM40	MRF315		3-386
BAM40SR	MRF315		3-386
BAM80		2N6166	3-116
BAM80SR		2N6166	3-116
BAM100SR		MRF317	3-394
BAM120		MRF317	3-394
BAM120SR		MRF317	3-394
BF7-35	MRF134		3-221
BF14-35	MRF136		3-229
BF25-35		MRF137	3-239
BF50-35	MRF172		3-311
BF100-35		MRF174	3-319
BF679		MRF536	3-173
BFG90A		MRF901	3-788
BFG91A	MRF2369		3-902
BFG96	MRF961		3-147
BFP10		MRF914	3-804
BFP91A	MRF573		—
BFP96		MRF581	3-639
BFQ17	BFQ17		3-137
BFQ19	BFQ19		3-138
BFQ22		MRF904	3-794
BFQ23		MRF536	3-173
BFQ34		MRF587	3-649
BFQ34T	MRF580		3-639
BFQ42	MRF607		3-663
BFQ43	MRF237		3-349
BFQ51		MRF536	3-173
BFQ63	MRF914		3-804
BFQ66		MRF572	3-627
BFQ85	MRF571		3-627
BFR36	MRF517		3-571
BFR38	2N4959		3-27
BFR49	2N6603		3-129
BFR53		MMBR920	3-184
BFR63	MRF511		3-561
BFR64	MRF511		3-561
BFR65	MRF511		3-561
BFR90	BFR90		3-139
BFR90A	BFR90		3-139
BFR91	BFR91		3-142
BFR91A		MRF571	3-627
BFR92	BFR92		3-145
BFR92A	BFR92A		3-145
BFR93	BFR93		3-146
BFR93A	BFR93A		3-146
BFR94	MRF587		3-649
BFR95	MRF517		3-571
BFR96	BFR96	BFRC96	3-147
BFR96S	MRF580A		3-639
BFR99	2N4957		3-27
BFS17	BFS17		3-155
BFS17S	BFS17S		—
BFS22A		2N3924	3-14

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
BFT24	MRF931		3-807
BFT50	MRF904		3-794
BFT95		MRF536	3-173
BFT96		MRF536	3-173
BFW16A	MRF517		3-571
BFW17A	MRF517		3-571
BFW46	2N3924		3-14
BFW47	2N3553		3-8
BFW92A	BFW92A		3-156
BFW93		MRF911	3-801
BFW94	MRF559		3-620
BFX89	BFX89		3-161
BFY90	BFY90		3-161
BGD102	MHW5185		4-71
BGY40A	MHW709-1		4-14
BGY40B	MHW709-2		4-14
BGY40C	MHW709-3		4-14
BGY41A	MHW710-1		4-18
BGY41B	MHW710-2		4-18
BGY41C	MHW710-3		4-18
BGY50		MHW1121	—
BGY51		MHW1122	—
BGY52		MHW3171	4-51
BGY53		MHW3172	4-51
BGY54	MHW3171		4-51
BGY55	MHW3172		4-51
BGY56		MHW3222	4-55
BGY57	MHW3222		4-55
BGY58A	MHW3342		4-57
BGY61	MHW1134		4-45
BGY65	MHW1184		4-45
BGY67	MHW1224		4-45
BGY67A	MHW1244		4-45
BGY70		MHW5122	—
BGY71	MHW5122		—
BGY78	MHW5342		—
BGY84	MHW5171		—
BGY84A	MHW5181		—
BGY85	MHW5172		—
BGY85A	MHW5182		—
BGY91	MHW806-1		4-34
BGY92	MHW820-1		4-40
BLU20/12	MRF644		3-678
BLU45/12	MRF646		3-682
BLU52	MRF390		3-438
BLU53		MRF392	3-442
BLU60/12	MRF648		3-686
BLU98	MRF581		3-639
BLU99	MRF841		3-738
BLV10		MRF212	—
BLV11	MRF221		3-104
BLV15/12		MRF221	3-104
BLV20		2N5641	3-64
BLV21	MRF314		3-382
BLV30		MRF5175	3-918
BLV31		MRF323	3-402
BLV45/12		MRF416	—
BLV75/12	MRF247		3-355
BLV80/28	MRF316		3-390
BLV90	MRF838A		3-724

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
BLV91	MRF870A		3-728
BLV92	MRF841		3-738
BLV93	MRF840		3-734
BLV94	MRF843		3-748
BLV95		MRF844	3-754
BLV96		MRF846	3-757
BLV97	MRF894		3-780
BLW29	2N2628		—
BLW31	MRF1946A		3-862
BLW32		MRF890	3-768
BLW33		MRF321	3-398
BLW34		MRF321	3-398
BLW50F	MRF464		3-520
BLW60		2N6084	3-113
BLW60C		2N6084	3-113
BLW64	MRF208		—
BLW75	MRF226		3-327
BLW76	MRF464		3-520
BLW77		MRF422	3-469
BLW78		MRF464	3-520
BLW79	2N5944		3-90
BLW80	MRF652		3-690
BLW81	2N5946		3-90
BLW82		MRF644	3-678
BLW83	MRF426		3-473
BLW84	MRF314		3-382
BLW85		MRF224	3-113
BLW85SP		MRF224	3-113
BLW86	MRF315		3-386
BLW87	MRF222		—
BLW89	MRF5174		3-915
BLW90	MRF5175		3-918
BLW91	MRF321		3-398
BLW95	MRF429		3-485
BLW96		MRF448	3-495
BLW97		MRF422	3-469
BLW98		MRF323	3-402
BLW99	MRF421		3-465
BLX13		MRF426A	3-473
BLX13C	MRF426A		3-473
BLX14		MRF464A	3-520
BLX39	MRF315A		3-386
BLX65		MRF629	—
BLX66		2N5944	3-90
BLX67		2N5946	3-90
BLX68		2N5946	3-90
BLX69A		MRF654	3-698
BLX91		MRF313	3-380
BLX91A		MRF313	3-380
BLX92		MRF5174	3-915
BLX92A		MRF5174	3-915
BLX93		MRF331	3-422
BLX93A		MRF331	3-422
BLX94A		MRF5177A	3-924
BLX94C		MRF323	3-402
BLX95		MRF5177A	3-924
BLX96		MRF890	3-768
BLX97		MRF321	3-398
BLX98		MRF323	3-402
BLY53A		2N5946	3-90

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
BLY57	2N3926		—
BLY58	2N3927		—
BLY59	2N3375		—
BLY60	2N3632		—
BLY87A		MRF212	—
BLY87C	MRF2628		3-907
BLY88A		2N6081	3-104
BLY88C	2N6081		3-104
BLY89A		2N6082	3-107
BLY89C	2N6082		3-107
BLY91A		2N5641	3-64
BLY91C		2N5641	3-64
BLY92A		2N5642	3-67
BLY92C	2N5642		3-67
BLY93A		MRF314A	3-382
BLY93C	MRF314A		3-382
BLY94		MRF315A	3-386
BM30-12	MRF216		—
BM45-12		MRF243	—
BM70-12	MRF247		3-355
BM80-12	MRF247		3-355
BM100-28	MRF317		3-394
BP8-12		MRF262	3-370
BP15-12	MRF262		3-370
BP30-12	MRF264		3-374
BP30-12L		MRF264	3-374
C2M50-28		MRF326	3-410
C2M50-28R		MRF326	3-410
C2M60-28	2N6439		3-125
C2M60-28R	2N6439		3-125
C2M70-28R	MRF327		3-414
C2M100-28	MRF329		3-418
C2M100-28A	MRF329		3-418
C1/2-12	MRF626		—
C1-12	MRF616		—
C1-28		MRF313	3-380
C2-8Z	MRF752		3-710
C3-12	2N5645		—
C3-28	MRF5174		3-915
C5-8Z		MRF754	3-714
C5-12	MRF652		3-690
C12-28		MRF331	3-422
C25-28		MRF323	3-402
C40-28	MRF5177A		3-924
CA100		MHW1171	—
CA200		MHW1172	—
CA401B		MHW1182	—
CA416		MHW1184	4-45
CA418	MHW1184		4-45
CA601B/U		MHW1342	—
CA636	MHW1342		—
CA801	MHW590		4-2
CA804		MHW590	4-2
CA860	MHW592		4-8
CA870	MHW590		4-2
CA2100	MHW3171		4-51
CA2101	MHW3171		4-51
CA2200	MHW3172		4-51
CA2201	MHW3172		4-51
CA2300		MHW3222	4-55

INDEX CROSS-REFERENCE (Continued)

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
CA2301	MHW3222		4-55
CA2418	MHW1184		4-45
CA2422	MHW1224		4-45
CA2600	MHW3342		4-57
CA2601BU		MHW1343	4-49
CA2603	MHW1344		4-49
CA2700	MHW1392		—
CA2800		MHW5172	—
CA2800H		MHW5172	—
CA2810	MHW5342		—
CA2810H		MHW5342	—
CA2812		MHW593	4-11
CA2812H		MHW593	4-11
CA2813		MHW591	4-5
CA2818		MHW3182	4-53
CA2818H		MHW3182	4-53
CA2820		MHW590	4-2
CA2820H		MHW590	4-2
CA2830		MHW592	4-8
CA2830H	MHW592		4-8
CA2832		MHW592	4-8
CA2832H		MHW592	4-8
CA2840	MHW3222		—
CA2840H		MHW3222	4-55
CA2842	MHW3222		4-55
CA2842H		MHW3222	4-55
CA2850	MHW1182		—
CA2850R	MHW1172R		4-47
CA2870	MHW5342		—
CA2870H		MHW5342	—
CA2875	MHW1182		—
CA2875R	MHW1172R		4-47
CA2876	MHW5222		—
CA2876R	MHW5222R		—
CA3100	MHW3171		4-51
CA3101	MHW3171		4-51
CA3200	MHW3172		4-51
CA3201	MHW3172		4-51
CA4101	MHW5171		—
CA4201	MHW5172		—
CA4411	MHW1134		4-45
CA4412	MHW1134		4-45
CA4418	MHW1184		4-45
CA4422	MHW1224		4-45
CA4424	MHW1244		4-45
CA4600	MHW5342		—
CA5101	MHW5181		—
CA5170	MHW5171		—
CA5180		MHW5142	—
CA5201	MHW5182		—
CA5270	MHW5172		—
CA5280	MHW5142		—
CA5300		MHW5222	—
CA5301	MHW5222		—
CA5600	MHW5342		—
CA6101	MHW6181		4-90
CA6201	MHW6182		4-90
CD1752		MRF317	3-394
CD1802	MRF226		3-327
CD1979		MRF5177A	3-924

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
CD2035	MRF5175		3-918
CD2087		MRF5175	3-918
CD2088	MRF321		3-398
CD2089	MRF323		3-402
CD2505	MRF5175		3-918
CD2514		2N6081	3-104
CD2545		MRF450	3-502
CD2810		MRF321	3-398
CD2811		MRF321	3-398
CD2812		MRF321	3-398
CD2813		MRF321	3-398
CD3025	2N5946		3-90
CD3400		MRF315	3-386
CD3401		MRF316	3-390
CD3403		MRF317	3-394
CD3463	MRF421		3-465
CD4024	MRF224		3-113
CD5916	MRF5174		3-915
CD5918	MRF321		3-398
CD5919A	MRF323		3-402
CD5944	2N5944		3-90
CD5945	2N5945		3-90
CD5946	2N5946		3-90
CD6105		MRF5177A	3-924
CD6105A		MRF5177A	3-924
CD7012	MRF454		3-507
CF4-28	MRF161		3-279
CG125	2N6603		3-129
CG125A		2N6603	3-129
CG125B		MRF572	3-627
CG125C		MRF572	3-627
CG125D	2N6604		3-133
CG125L		2N6604	3-133
CG127	MRF572		3-627
CG127A		MRF572	3-627
CG127B		MRF572	3-627
CHE0		MRF616	—
CM10-12A		MRF641	3-674
CM10-28		MRF331	3-422
CM20-12A	MRF641		3-674
CM25-28	MRF325		3-406
CM25-28A		MRF325	3-406
CM30-12A	MRF644		3-678
CM45-12A	MRF646		3-682
CM45-28		MRF326	3-410
CM60-12A	MRF648		3-686
CM80-28	MRF327		3-414
CM80-28R	MRF327		3-414
CME50-12		MRF648	3-686
CP5-12	MRF660		3-702
CTC14		MRF464A	3-520
CTC15		MRF428	3-481
CTC1175M	MRF1150M		3-846
CTC1350M	MRF1325M		3-858
CTC2001A	MRF2001		3-866
CTC2003A	MRF2003		3-874
CTC2005A	MRF2005		3-882
CTC2010	MRF2010		3-890
CZ8110	MWA110		4-104
CZ8120	MWA120		4-104

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
CZ8130	MWA130		4-104
CZ8210	MWA210		4-112
CZ8220	MWA220		4-112
CZ8230	MWA230		4-112
CZ8310	MWA310		4-120
CZ8320	MWA320		4-120
CZ8330	MWA330		4-120
CZ8401		MWA110	4-104
CZ8402		MWA120	4-104
CZ8403		MWA230	4-112
CZ8404		MWA230	4-112
CZ8461		MWA110	4-104
CZ8462		MWA120	4-104
CZ8463		MWA230	4-112
CZ8464		MWA230	4-112
D1/2-12		MRF838A	3-724
D1-12E		MRF838A	3-724
D1-28		MRF313	3-380
D2-12E		MRF839	3-728
D3-28		MRF5174	3-915
D10-28	MRF321		3-398
D10P		MRF1015MC	3-834
D20-28	MRF323		3-402
DM10P		MRF1015MB	3-834
DM30-12BA	MRF844		3-754
DM30P		MRF1035MB	3-838
DM50P		MRF1090MB	3-842
DMB5-12		MRF841F	3-738
DMB5-12BA		MRF841F	3-738
DMB10-12	MRF840		3-734
DMB10-12BA	MRF840		3-734
DMB10-25	MRF892		3-776
DMB15-12		MRF842	3-744
DMB20-12	MRF842		3-744
DMB20-12BA	MRF842		3-744
DMB30-12	MRF844		3-754
DMB30-25	MRF894		3-780
DMB45-12	MRF846		3-757
DMB45-12BA	MRF846		3-757
DME2		MRF1002MA	3-822
DME6L		MRF1008MC	3-830
DME7		MRF1008MC	3-830
DME10		MRF1015MA	3-834
DME25		MRF1035MC	3-838
DME30L		MRF1035MC	3-838
DME50		MRF1090MC	3-842
DME75		MRF1090MB	3-842
DME120L		MRF1150MC	3-850
DME150	MRF1150M		3-846
DME250		MRF1250M	3-854
DME375		MRF1325M	3-858
DME375A		MRF1325M	3-858
DMEG70		MRF1090MC	3-842
DMEG250		MRF1250M	3-854
DV1006	MRF137		3-239
DV1007	MRF171		3-303
DV1008	MRF172		3-311
DV1010	MRF174		3-319
DV2805S	MRF134		3-221
DV2810S	MRF136		3-229

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
DV2820S	MRF136		3-229
DV2840S	MRF171		3-303
DV2880U	MRF172		3-311
DV28120U	MRF174		3-319
ESM269	MRF914		3-604
FF124		MHW4524F	4-59
GM-104-1A		MRF313	3-380
GM-104-4		MRF5174	3-915
GM-104-20		MRF323	3-402
GM-104-100		MRF329	3-418
GPA501		MWA210	4-112
GPA502		MWA220	4-112
GPA503		MWA230	4-112
GPA510	MWA210		4-112
GPA511	MWA220		4-112
GPA512	MWA230		4-112
GPA1001		MWA310	4-120
GPA1002		MWA320	4-120
GPA1003		MWA330	4-120
GPA1004		MWA320	4-120
GPA1005		MWA320	4-120
GPA1006	MWA330		4-120
GPA1007		MWA330	4-120
GPD110	MWA110		4-104
GPD120	MWA120		4-104
GPD130	MWA130		4-104
GPD310	MWA310		4-120
GPD320	MWA320		4-120
GPD330	MWA330		4-120
GPD401		MWA110	4-104
GPD402		MWA120	4-104
GPD403		MWA230	4-112
GPD404		MWA230	4-112
GPD461		MWA110	4-104
GPD462		MWA120	4-104
GPD463		MWA230	4-112
GPD464		MWA230	4-112
H50-28	MRF464		3-520
H100-28		MRF422	3-469
H100-50		MRF428	3-481
H175-50		MRF428	3-481
HMIL-100-28	MRF422		3-469
HMIL-150-50	MRF429		3-485
HXTR2102	2N6604		3-133
HXTR6104	2N6603		3-129
HXTR6105		2N6603	3-129
IMD604HA		MRF2001	3-866
IMD604HB		MRF2003	3-874
IMD604HC		MRF2005	3-882
IMD2001	MRF2001		3-866
IMD2003	MRF2003		3-874
IMD2005	MRF2005		3-882
IMD2010	MRF2010		3-890
J01006	MRF317		3-394
J02000		MRF5177A	3-924
J02005		MRF5177A	3-924
J02007A	2N6439		3-125
J02009	MRF325		3-406
J02014	MRF326		3-410
J02015A	MRF327		3-414

INDEX CROSS-REFERENCE (Continued)

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
J02016		MRF327	3-414
J03012		MRF641	3-674
J03015	MRF641		3-674
J03020	MRF644		3-678
J03025	MRF644		3-678
J03028		MRF644	3-678
J03030		MRF646	3-682
J03035		MRF646	3-682
J03037		MRF646	3-682
J03040	MRF646		3-682
J03045	MRF646		3-682
J03050		MRF648	3-686
J03055	MRF648		3-686
J03060	MRF648		3-686
J03401	MRF840		3-734
J03402	MRF842		3-744
J03403		MRF844	3-754
J03404	MRF844		3-754
J03405		MRF846	3-757
J03406	MRF846		3-757
J03502		MRF894	3-780
J04028		MRF216	—
J04030		MRF216	—
J04036		MRF216	—
J04040	MRF216		—
J04045		MRF216	—
J04070	MRF4070		3-911
J04075	MRF247		3-355
J04080		MRF245	—
LMIL1	MRF890		3-768
LNA1001		MWA310	4-120
LT1001A	MRF586		3-649
LT2001	MRF587		3-639
LT3005		MRF587	3-649
LT3014		MRF587	3-649
LT3046		MRF586	3-649
LT3047		MRF904	3-794
LT3072	MRF904		3-794
LT3203	MRF580		3-639
LT3204	MRF581		3-639
LT3700	2N6603		3-129
LT3703		MRF901	3-788
LT3704	MRF901		3-788
LT3746	MRF905		3-799
LT3772	MRF904		3-794
LT4400	MRF962		3-147
LT4403	BFR96		3-147
LT4404	MRF961		3-147
LT4446	MRF965		3-147
LT4485		MRF962	3-147
LT4700	MRF572		3-627
LT4703	BFR91		3-142
LT4704	MRF571		3-627
LT4746		MRF905	3-799
LT4772	MRF914		3-804
LT4785	MRF573		3-617
M57704H		MHW710-2	4-18
M57704L		MHW710-1	4-18
M57704M		MHW710-1	4-18
MC5381	MHW3181		4-53

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
MC5382	MHW3182		4-53
MC5383	MHW3342		4-57
MC5384	MHW5181		—
MC5385	MHW5182		—
MC5386	MHW5342		—
MC5387	MHW6181		4-90
MC5388	MHW6182		4-90
MC5389	MHW6342		4-96
MC5813	MHW1134		4-45
MC5814		MHW5222	—
MC5815	MHW5222		—
MC5816		MHW6222	4-92
MC5817	MHW6222		4-92
MC5818	MHW1184		4-45
MC5819	MHW6181		4-90
MC5820	MHW6182		4-90
MC5821	MHW6342F		4-96
MC5822	MHW1224		4-45
MC5824	MHW1244		4-45
MD4957	MD4957		3-165
MHW580	MHW1342		—
MHW590	MHW590		4-2
MHW591	MHW591		4-5
MHW592	MHW592		4-8
MHW593	MHW593		4-11
MHW594	MHW1171		—
MHW595	MHW1172		—
MHW709-001	MHW709-001		4-14
MHW709-002	MHW709-002		4-14
MHW709-003	MHW709-003		4-14
MHW710-001	MHW710-001		4-18
MHW710-002	MHW710-002		4-18
MHW710-003	MHW710-003		4-18
MHW720-001	MHW720-001		4-22
MHW720-002	MHW720-002		4-22
MHW720A1	MHW720A1		4-26
MHW720A2	MHW720A2		4-26
MHW725-1	MHW725-1		—
MHW725-2	MHW725-2		—
MHW725-3	MHW725-3		—
MHW802-001	MHW802-001		4-30
MHW802-002	MHW802-002		4-30
MHW806-001	MHW806-001		4-34
MHW806-002	MHW806-002		4-34
MHW806-003	MHW806-003		4-34
MHW806-004	MHW806-004		4-34
MHW806A1	MHW806A1		4-37
MHW806A2	MHW806A2		4-37
MHW806A3	MHW806A3		4-37
MHW806A4	MHW806A4		4-37
MHW806A5	MHW806A5		4-37
MHW806A6	MHW806A6		4-37
MHW806A7	MHW806A7		4-37
MHW806A8	MHW806A8		4-37
MHW812-1	MHW812-1		TBA
MHW812-2	MHW812-2		TBA
MHW812-3	MHW812-3		TBA
MHW820-001	MHW820-001		4-40
MHW820-002	MHW820-002		4-40
MHW820-003	MHW820-003		4-40

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
MHW1121	MHW1121		—
MHW1122	MHW1122		—
MHW1134	MHW1134		4-45
MHW1171	MHW1171		—
MHW1171R	MHW1171R		4-47
MHW1172	MHW1172		—
MHW1172R	MHW1172R		4-47
MHW1182	MHW1182		—
MHW1184	MHW1184		4-45
MHW1221	MHW1221		—
MHW1222	MHW1222		—
MHW1224	MHW1224		4-45
MHW1244	MHW1244		4-45
MHW1341	MHW1341		—
MHW1342	MHW1342		—
MHW1343	MHW1343		4-49
MHW1344	MHW1344		4-49
MHW2172	MHW2172		—
MHW3171	MHW3171		4-51
MHW3172	MHW3172		4-51
MHW3181	MHW3181		4-53
MHW3182	MHW3182		4-53
MHW3222	MHW3222		4-55
MHW3242	MHW3242		—
MHW3272A	MHW3272A		—
MHW3342	MHW3342		4-57
MWH3382A	MHW3382A		—
MHW4171	MHW4171		—
MHW4172	MHW4172		—
MHW4341	MHW4341		—
MHW4342	MHW4342		—
MHW4524F	MHW4524F		4-59
MHW5122	MHW5122		—
MHW5122A	MHW5122A		4-61
MHW5141A	MHW5141A		4-63
MHW5142	MHW5142		—
MHW5142A	MHW5142A		4-63
MHW5162A	MHW5162A		4-65
MHW5171	MHW5171		—
MHW5171A	MHW5171A		4-67
MHW5172	MHW5172		—
MHW5172A	MHW5172A		4-67
MHW5181	MHW5181		—
MHW5181A	MHW5181A		4-69
MHW5182	MHW5182		—
MHW5182A	MHW5182A		4-69
MHW5185	MHW5185		4-71
MHW5222	MHW5222		—
MHW5222A	MHW5222A		4-74
MHW5272A	MHW5272A		4-76
MHW5332A	MHW5332A		4-78
MHW5341	MHW5341		—
MHW5342	MHW5342		—
MHW5342A	MHW5342A		4-80
MHW5342A	MHW5342A		4-80
MHW5382	MHW5382		—
MHW5382A	MHW5382A		4-82
MHW6122	MHW6122		4-84
MHW6141	MHW6141		4-86
MHW6142	MHW6142		4-86

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
MHW6171	MHW6171		4-88
MHW6172	MHW6172		4-88
MHW6181	MHW6181		4-90
MHW6182	MHW6182		4-90
MHW6185	MHW6185		4-71
MHW6222	MHW6222		4-92
MHW6272	MHW6272		4-94
MHW6342	MHW6342		4-96
MHW6342F	MHW6342		4-96
MKB12040WS		MRF1035MC	3-838
MKB12100WS		MRF1090MC	3-842
MKB12140W	MRF1090MC		3-842
MM439		2N4959	3-27
MM1500		MRF905	3-799
MM1500A		MRF905	3-799
MM1501		MRF905	3-799
MM1501A		MRF905	3-799
MM1510	2N5851		—
MM1511	2N5852		—
MM1549	2N5635		3-915
MM1550	2N5636		3-422
MM1551	2N5637		3-402
MM1557	2N5641		3-64
MM1558	2N5642		3-67
MM1559	2N5643		3-70
MM1561	2N6166		3-116
MM1601	2N5589		—
MM1602	2N5590		—
MM1603	2N5591		—
MM1605	2N5841		—
MM1606	2N5842		—
MM1607	2N5842		—
MM1608	2N5846		—
MM1612	2N6255		—
MM1618	2N5847		3-104
MM1620	2N5849		3-79
MM1622	2N5849		3-79
MM1632	2N5941		3-524
MM1633	2N5942		3-520
MM1646	2N5849		3-79
MM1660	2N5644		—
MM1661	2N5645		—
MM1662	2N5646		3-694
MM1665	2N6136		—
MM1666	2N6082		3-107
MM1667	2N6083		3-110
MM1668	2N6084		3-113
MM1669	2N6084		3-113
MM1680	2N6080		3-101
MM1681	2N6081		3-104
MM1713	2N4072		—
MM1943	2N4072		—
MM1945	2N4072		—
MM4018	MM4018		3-169
MM4019	MM4019		3-171
MM4020	2N6094		—
MM4021	2N6095		—
MM4022	2N6096		—
MM4023	2N6097		—
MM4049	MM4049		3-173

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
MMC4049	MMC4049		3-173
MM4500	2N5583		3-60
MM5177		MRF5177A	3-924
MM8000	MM8000		3-178
MM8001	MM8001		3-178
MM8002	2N5943		3-83
MM8003	MRF511		3-561
MM8004		MRF475	3-528
MM8006	2N5031		3-36
MM8007	2N5032		3-36
MM8008		MRF905	3-799
MM8009		MRF905	3-180
MM8010		MRF905	3-799
MM8011		MRF905	3-799
MM8012	2N5947		3-97
MM8020	2N5836		—
MM8021	2N5837		—
MM8023		2N5943	3-83
MMBR536	MMBR536		3-192
MMBR571	MMBR571		3-198
MMBR901	MMBR901		3-183
MMBR911	MMBR911		3-211
MMBR920	MMBR920		3-184
MMBR930	MMBR930		3-185
MMBR931	MMBR931		3-186
MMBR941	MMBR941		3-809
MMBR941L	MMBR941L		3-809
MMBR951	MMBR951		3-811
MMBR951L	MMBR951L		3-811
MMBR2060	MMBR2060		3-187
MMBR2857	MMBR2857		3-188
MMBR4957	MMBR4957		3-189
MMBR5031	MMBR5031		3-190
MMBR5179	MMBR5179		3-191
MO1011B150Y		MRF1150MC	3-850
MO1011B250Y		MRF1250M	3-854
MPN3404	MPN3404		—
MPS536	MPS536		3-192
MPS571	MPS571		3-198
MPS901	MPS901		3-207
MPS911	MPS911		3-211
MPS1983	MPS901		3-207
MPS3866	MPS3866		3-220
MR1011B150Y		MRF1150MC	3-850
MR1011B300Y		MRF1250M	3-854
MRA1720-2		MRF2003M	3-878
MRA1720-5		MRF2005M	3-886
MRA1720-9		MRF2010M	3-894
MRA1720-20		MRF2016M	3-898
MRAL1720-2	MRF2003M		3-878
MRAL1720-5	MRF2005M		3-886
MRAL1720-9	MRF2010M		3-894
MRAL1720-20		MRF2016M	3-898
MRAL2023-1.5	MRF2001M		3-870
MRAL2023-1.5H		MRF2001M	3-870
MRAL2023-3	MRF2003M		3-878
MRAL2023-3H		MRF2003M	3-878
MRAL2023-6		MRF2010M	3-894
MRAL2023-6H		MRF2010M	3-894
MRAL2023-12		MRF2016M	3-898

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
MRAL2023-12H		MRF2016M	3-898
MRAL2023-18H		MRF2016M	3-898
MRB12175YR		MRF1150MC	3-850
MRB12350YR		MRF1325M	3-858
MRF134	MRF134		3-221
MRF136	MRF136		3-229
MRF136Y	MRF136Y		3-229
MRF137	MRF137		3-239
MRF138	MRF138		3-247
MRF140	MRF140		3-252
MRF148	MRF148		3-257
MRF150	MRF150		3-262
MRF153	MRF153		3-267
MRF154	MRF154		3-273
MRF161	MRF161		3-279
MRF162	MRF162		3-287
MRF163	MRF163		3-295
MRF171	MRF171		3-303
MRF172	MRF172		3-311
MRF174	MRF174		3-319
MRF201	2N6255		—
MRF203		MRF245	—
MRF207	MRF207		—
MRF208	MRF208		—
MRF212	MRF212		—
MRF216	MRF216		—
MRF220	MRF220		—
MRF221	MRF221		3-104
MRF222		MRF1946	3-862
MRF223		MRF1946	3-862
MRF224	MRF224		3-113
MRF225		MRF227	3-329
MRF226	MRF226		3-327
MRF227	MRF227		3-329
MRF229	MRF229		3-333
MRF230		2N4427	3-23
MRF231		2N6080	3-101
MRF232	MRF232		3-337
MRF233	MRF233		3-341
MRF234	MRF234		3-345
MRF237	MRF237		3-349
MRF238	MRF238		—
MRF239	MRF239		—
MRF240	MRF240		3-351
MRF240A	MRF240A		3-351
MRF243		MRF247	3-355
MRF245	MRF245		—
MRF247	MRF247		3-355
MRF248	MRF248		3-358
MRF260	MRF260		3-362
MRF261	MRF261		3-366
MRF262	MRF262		3-370
MRF264	MRF264		3-374
MRF305	MRF325		3-406
MRF306	2N6439		—
MRF309	MRF309		3-378
MRF313	MRF313		3-380
MRF313A		MRF313	3-380
MRF314	MRF314		3-382
MRF314A	MRF314A		3-382

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
MRF315	MRF315		3-386
MRF315A	MRF315A		3-386
MRF316	MRF316		3-390
MRF317	MRF317		3-394
MRF321	MRF321		3-398
MRF323	MRF323		3-402
MRF325	MRF325		3-406
MRF326	MRF326		3-410
MRF327	MRF327		3-414
MRF329	MRF329		3-418
MRF331	MRF331		3-422
MRF338	MRF338		3-426
MRF340	MRF340		3-430
MRF344	MRF344		3-434
MRF390	MRF390		3-438
MRF392	MRF392		3-442
MRF393	MRF393		3-446
MRF401	MRF401		3-450
MRF402		2N4427	3-23
MRF406	MRF406		3-454
MRF410	MRF410		3-457
MRF410A	MRF410A		3-457
MRF412	MRF412		3-461
MRF412A		MRF454A	3-507
MRF415	2N6366		—
MRF416	2N6367		—
MRF417	2N6368		3-515
MRF418	MRF460		3-515
MRF419	2N6370		3-457
MRF420	MRF454		3-507
MRF421	MRF421		3-465
MRF421MP	MRF421MP		3-465
MRF422	MRF422		3-469
MRF422MP	MRF422MP		3-469
MRF426	MRF426		3-473
MRF426A	MRF426A		3-473
MRF427	MRF427		3-477
MRF427A	MRF427A		3-477
MRF428	MRF428		3-481
MRF429	MRF429		3-485
MRF429MP	MRF429MP		3-485
MRF430	MRF430		3-498
MRF432	MRF432		—
MRF433	MRF433		3-493
MRF435	MRF422		3-469
MRF437	MRF437		—
MRF437A	MRF437A		—
MRF448	MRF448		3-495
MRF449	MRF449		3-499
MRF449A	MRF449A		3-499
MRF450	MRF450		3-502
MRF450A	MRF450A		3-502
MRF451	MRF453		3-505
MRF452	MRF453		3-505
MRF453	MRF453		3-505
MRF453A	MRF453A		3-505
MRF454	MRF454		3-507
MRF454A	MRF454A		3-507
MRF455	MRF455		3-509
MRF455A	MRF455A		3-509

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
MRF458	MRF458		3-511
MRF458A	MRF458A		3-511
MRF460	MRF460		3-515
MRF464	MRF464		3-520
MRF464A	MRF464A		3-520
MRF466	MRF466		3-524
MRF475	MRF475		3-528
MRF476	MRF476		3-532
MRF477	MRF477		3-536
MRF479	MRF479		3-540
MRF485	MRF485		3-544
MRF486	MRF486		3-548
MRF492	MRF492		3-552
MRF492A	MRF492A		3-552
MRF497	MRF497		3-555
MRF501	MRF501		3-559
MRF502	MRF502		3-559
MRF504		MRF511	3-561
MRF511	MRF511		3-561
MRF515	MRF515		3-567
MRF517	MRF517		3-571
MRF519		MRF517	3-571
MRF521	MRF521	MRFC521	3-576
MRF522	MRF522		3-576
MRF524	MRF524		3-576
MRF525	MRF525		3-584
MRF526	MRF526		—
MRF531	MRF531		3-588
MRF532	MRF532		—
MRF534	MRF534		3-173
MRF536	MRF536		3-173
MRF542	MRF542		3-590
MRF543	MRF543		3-592
MRF544	MRF544		3-594
MRF545	MRF545		3-598
MRF546	MRF546		3-602
MRF547	MRF547		3-604
MRF548	MRF548		3-590
MRF549	MRF549		3-592
MRF553	MRF553		3-606
MRF555	MRF555		3-611
MRF557	MRF557		3-615
MRF559	MRF559		3-620
MRF571	MRF571		3-627
MRF572	MRF572		3-627
MRF573	MRF573		—
MRF580	MRF580		3-639
MRF580A	MRF580A		3-639
MRF581	MRF581		3-639
MRF581A	MRF581A		3-639
MRF586	MRF586		3-649
MRF587	MRF587		3-649
MRF601	2N6256		—
MRF602	2N6136		—
MRF604	MRF604		3-660
MRF605	2N6439		3-125
MRF606		MRF237	3-349
MRF607	MRF607		3-663
MRF616	MRF616		—
MRF618	MRF641		3-674

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
MRF619	MRF644		3-678
MRF620	MRF644		3-678
MRF621	MRF646		3-682
MRF626	MRF626		—
MRF627	MRF627		3-666
MRF628		MRF559	3-620
MRF629	MRF629		—
MRF630	MRF630		3-670
MRF641	MRF641		3-674
MRF644	MRF644		3-678
MRF646	MRF646		3-682
MRF648	MRF648		3-686
MRF652	MRF652		3-690
MRF653	MRF653		3-694
MRF654	MRF654		3-698
MRF660	MRF660		3-702
MRF750	MRF750		3-706
MRF752	MRF752		3-710
MRF754	MRF754		3-714
MRF837	MRF837		3-718
MRF838	MRF838		3-724
MRF838A	MRF838A		3-724
MRF839	MRF839		3-728
MRF839F	MRF839F		3-728
MRF840	MRF840		3-734
MRF841	MRF841		3-738
MRF841F	MRF841F		3-738
MRF842	MRF842		3-744
MRF843	MRF843		3-748
MRF843F	MRF843F		3-748
MRF844	MRF844		3-754
MRF846	MRF846		3-757
MRF848	MRF848		3-761
MRF870		MRF839	3-728
MRF870A	MRF839		3-728
MRF873	MRF873		3-764
MRF890	MRF890		3-768
MRF891	MRF891		3-772
MRF892	MRF892		3-776
MRF894	MRF894		3-780
MRF898	MRF898		3-784
MRF901	MRF901		3-788
MRF902	2N6603		3-129
MRF904	MRF904		3-794
MRF905	MRF905		3-799
MRF911	MRF911		3-801
MRF912	2N6604		3-133
MRF914	MRF914		3-804
MRF931	MRF931		3-807
MRF941	MRF941	MRFC941	3-809
MRF942	MRF942		3-809
MRF951	MRF951	MRFC951	3-811
MRF952	MRF952		3-811
MRF961	MRF961		3-147
MRF962	MRF962		3-147
MRF965	MRF965		3-147
MRF966	MRF966		3-813
MRF1000MA	MRF1000MA		3-818
MRF1000MB	MRF1000MB		3-818
MRF1000MC	MRF1000MC		3-818

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
MRF1002MA	MRF1002MA		3-822
MRF1002MB	MRF1002MB		3-822
MRF1002MC	MRF1002MC		3-822
MRF1004MA	MRF1004MA		3-826
MRF1004MB	MRF1004MB		3-826
MRF1004MC	MRF1004MC		3-826
MRF1008MA	MRF1008MA		3-830
MRF1008MB	MRF1008MB		3-830
MRF1008MC	MRF1008MC		3-830
MRF1015MA	MRF1015MA		3-834
MRF1015MB	MRF1015MB		3-834
MRF1015MC	MRF1015MC		3-834
MRF1035MA	MRF1035MA		3-838
MRF1035MB	MRF1035MB		3-838
MRF1035MC	MRF1035MC		3-838
MRF1090MA	MRF1090MA		3-842
MRF1090MB	MRF1090MB		3-842
MRF1090MC	MRF1090MC		3-842
MRF1150M	MRF1150M		3-846
MRF1150MA	MRF1150MA		3-850
MRF1150MB	MRF1150MB		3-850
MRF1150MC	MRF1150MC		3-850
MRF1250M	MRF1250M		3-854
MRF1325M	MRF1325M		3-858
MRF1946	MRF1946		3-862
MRF1946A	MRF1946A		3-862
MRF2001	MRF2001		3-866
MRF2001B	MRF2001B		3-866
MRF2001M	MRF2001M		3-870
MRF2003	MRF2003		3-874
MRF2003B	MRF2003B		3-874
MRF2003M	MRF2003M		3-878
MRF2005	MRF2005		3-882
MRF2005B	MRF2005B		3-882
MRF2005M	MRF2005M		3-886
MRF2010	MRF2010		3-890
MRF2010B	MRF2010B		3-890
MRF2010M	MRF2010M		3-894
MRF2016M	MRF2016M		3-898
MRF2369	MRF2369		3-902
MRF2628	MRF2628		3-907
MRF4070	MRF4070		3-911
MRF5174	MRF5174		3-915
MRF5175	MRF5175		3-918
MRF5176	MRF5176		3-921
MRF5177A	MRF5177A		3-924
MRF5178		2N6439	3-125
MRF5211,L	MRF5211,L		3-576
MRF5711,L	MRF5711,L		3-927
MRF5812	MRF5812		3-931
MRF8003		MRF476	3-532
MRF8004		MRF475	3-528
MRF8372	MRF8372		3-936
MRF9011,L	MRF9011,L		3-940
MRF9331,L	MRF9331,L		3-944
MRF9411	MRF9411		3-809
MRF9411L	MRF9411L		3-809
MRF9511	MRF9511		3-811
MRF9511L	MRF9511L		3-811
MAS0204	MWA0204		4-98

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
MSC1000M	MRF1000MA/B		3-807
MSC1002M	MRF1002MA/B		3-822
MSC1004M	MRF1004MA/B		3-826
MSC1015M	MRF1015MA/B		3-834
MSC1035M	MRF1035MA/B		3-838
MSC1075M	MRF1090MA/B		3-842
MSC1090M	MRF1090MA/B		3-842
MSC1150M	MRF1150MA/B		3-850
MSC1175M	MRF1150MA/B		3-850
MSC1250M	MRF1250M		3-854
MSC1325M	MRF1325M		3-858
MSC2001	MRF2001		3-866
MSC2003	MRF2003		3-874
MSC2005	MRF2005		3-882
MSC2010	MRF2010		3-890
MSC2302		MRF2003	3-874
MSC2304		MRF2005	3-882
MSC2307		MRF2010	3-890
MSC82001	MRF2001		3-866
MSC82003	MRF2003		3-874
MSC82005	MRF2005		3-882
MSC82005M	MRF2005M		3-886
MSC82010	MRF2010		3-890
MSC82012M	MRF2010M		3-894
MSC82020M	MRF2016M		3-898
MSC82201	MRF2001		3-866
MSC82203	MRF2003		3-874
MSC82304M	MRF2005M		3-886
MSC82310M	MRF2010M		3-894
MSC82313M	MRF2016M		4-898
MWA0204	MWA0204		4-98
MWA0211	MWA0211,L		4-98
MWA0270	MWA0270		4-98
MWA110	MWA110		4-104
MWA110H	MWA110H		4-104
MWA120	MWA120		4-104
MWA120H	MWA120H		4-104
MWA130	MWA130		4-104
MWA130H	MWA130H		4-104
MWA210	MWA210		4-112
MWA210H	MWA210H		4-112
MWA220	MWA220		4-112
MWA220H	MWA220H		4-112
MWA230	MWA230		4-112
MWA230H	MWA230H		4-112
MWA310	MWA310		4-120
MWA310H	MWA310H		4-120
MWA320	MWA320		4-120
MWA320H	MWA320H		4-120
MWA330	MWA330		4-120
MWA330H	MWA330H		4-120
MWA5121	MWA5121		4-128
MWA5157	MWA5157		4-132
MX7.5	MHW709		—
MX12	MHW710		—
MX15		MHW710	—
MX20	MHW720A		—
MXR100	MXR100		—
MXR571	MXR571		3-198
MXR911	MXR911		3-211

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
MXR3866	MXR3866		3-948
MXR5160	MXR5160		3-949
MXR5583	MXR5583		3-950
MXR5943	MXR5943		3-951
NE02107	MRF572		3-627
NE02108		MRF573	—
NE02132	MPS571		3-198
NE02133	MMBR571		3-198
NE02135	MRF573		—
NE02137	MRF2369		3-902
NE020214-12		MRF607	3-663
NE020320-12		2N5944	3-90
NE020320-28		MRF331	3-422
NE020620-07		2N5946	3-90
NE021020-12		2N5946	3-90
NE021020-28	MRF331		3-422
NE022025-12		2N6081	3-104
NE022025-28		MRF314A	3-382
NE022526-12		2N6082	3-107
NE024027-28		MRF315A	3-386
NE028029-12	MRF247		3-355
NE028029-28		MRF316	3-390
NE050214-12	MRF629		—
NE050320-12	2N5944		3-90
NE050490-07		MRF752	3-710
NE050491-07		MRF752	3-710
NE050690-07		MRF754	3-714
NE050691-07		MRF754	3-714
NE051020-28	MRF321		3-398
NE051025-12		2N5946	3-90
NE051525-12		MRF654	3-698
NE052025-28		MRF323	3-402
NE080420-12		MRF839	3-728
NE21935		MRF573	—
NE21937		MRF571	3-627
NE22120		MRF587	3-649
NE24615		MRF586	3-649
NE24620		MRF587	3-649
NE32702		2N6604	3-133
NE32707	2N6604		3-133
NE41603		MRF962	3-147
NE41607		MRF962	3-147
NE41610	MRF965		3-147
NE41612		MRF965	3-147
NE41615		MRF965	3-147
NE41620		MRF587	3-649
NE41635		MRF962	3-147
NE57510		MRF586	3-649
NE57520		MRF587	3-649
NE57803		MRF572	3-627
NE57807	MRF572		3-627
NE57808		MRF573	—
NE57835	MRF573		—
NE59312	MM4049		3-173
NE59335		MRF536	3-173
NE59503		MRF581	3-649
NE64310		MRF586	3-649
NE64320		MRF587	3-649
NE68132		MPS571	3-198
NE68133		MMBR571	3-193

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
NE68135		MRF573	—
NE68137		MRF571	3-627
NE73412	MRF914		3-804
NE73432	MPS911		3-211
NE73433	MMBR911		3-211
NE73435		2N6604	3-133
NE73437	MRF911		3-801
NE74014		MRF586	3-649
NE74020		MRF587	3-649
NE74113	MRF586		3-649
NE74114		MRF586	3-649
NE77320		MRF587	3-649
NE85632		MPS571	3-198
NE85633		MMBR571	3-198
NE85637		MRF571	3-627
NE88912	MM4049		3-173
NE88933	MMBR536		3-192
NEL080120-24		MRF890	3-768
NEM020C29-28	MRF317		3-394
NEM050C29-28	MRF327		3-414
NEM054029-12	MRF646		3-682
NEM054029-28	MRF325		3-406
NEM056029-12	MRF648		3-686
NEM056029-28	MRF309		3-378
NEM080481E-12	MRF839F		3-728
NEM081081B-12	MRF840		3-734
NEM081081E-12	MRF873		3-764
NEM082081B-12	MRF842		3-744
NEM084081B-12	MRF844		3-754
NEM085081B-12	MRF846		3-757
NEM092081B-28	MRF892		3-776
NEM094081B-28	MRF894		3-780
NEM2010B-20		MRF2016M	3-898
NEM2305B-20		MRF2010M	3-894
PEE0015U		MRF323	3-402
PEE0020U		MRF323	3-402
PEE0035U		MRF5177A	3-924
PH0105-100	MRF393		3-446
PH0401H	MRF5174		3-915
PH0403H	MRF5175		3-918
PH0406H		MRF5175	3-918
PH0412H	MRF321		3-398
PH0425H		MRF5177A	3-924
PH0450D	2N6439		3-125
PH0450H	2N6439		3-125
PH0501H	MRF5174		3-915
PH0503H		MRF5175	3-918
PH0506H	MRF331		3-422
PH0512H	MRF331		3-422
PH0525H	MRF325		3-406
PH0550H		2N6439	3-125
PH1100C		MRF1150MC	3-850
PH1100H		MRF1150MC	3-850
PH1110C		MRF1015MC	3-834
PH1150C		MRF1090MC	3-842
PH1175		MRF1150MC	3-850
PH2001C	MRF2001M		3-870
PH2003C	MRF2003M		3-878
PH2005C	MRF2005M		3-886
PH2010C	MRF2010M		3-894

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
PH2020C		MRF2016M	3-898
PH2301H		MRF2001	3-866
PH2303H		MRF2005	3-882
PH2306H		MRF2010	3-890
PH8193		MRF905	3-799
PHA3317-1	MHW3171		4-51
PHA3317-2	MHW3172		4-51
PHA3318-1	MHW3181		4-53
PHA3318-2	MHW3182		4-53
PHA3334-2	MHW3342		4-57
PHA4517-1	MHW5171		—
PHA4517-2	MHW5172		—
PHA4518-1	MHW5181		—
PHA4518-2	MHW5182		—
PHA4534	MHW5342		—
PHA5018-1	MHW6181		4-90
PHA5018-2	MHW6182		4-90
PHA5034	MHW6342F		4-96
PKB20010U		MRF2010	3-890
PKB23001U		MRF2001	3-866
PKB23003U		MRF2003	3-874
PKB23005U		MRF2005	3-882
PME04030U	MRF325		3-406
PT3501	2N4427		3-23
PT3502	2N5635		3-915
PT3503	2N5589		—
PT3535	2N4427		3-23
PT3536		MRF553	3-606
PT3537		2N5944	3-90
PT3570	2N5947		3-97
PT3571	2N5943		3-83
PT3571A	2N5943		3-83
PT3690		2N5641	3-64
PT4537		2N5944	3-90
PT4544		MRF226	3-327
PT4555		MRF234	3-345
PT4556		MRF450	3-502
PT4570	2N5947		3-97
PT4572A	2N5947		3-97
PT4574	MRF511		3-561
PT4578	MRF517		3-571
PT4579	2N5943		3-83
PT5695		MRF233	3-341
PT5701	MRF402		3-23
PT5740		2N5590	—
PT5741	MRF449A		3-499
PT5788		MRF464A	3-520
PT6665A		MRF464	3-520
PT8549		2N5589	—
PT8551		2N3553	3-8
PT8554A	MRF492A		3-552
PT8717		MRF231	3-101
PT8740		MRF225	3-329
PT8769		MRF233	3-341
PT8809	2N5944		3-90
PT8809S	MRF616		—
PT8810	2N5945		3-90
PT8811	2N5946		3-90
PT8825		2N6136	—
PT8828A	MRF226		3-327

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
PT8837	2N6081		3-104
PT8838		2N6084	3-113
PT8850		2N5847	3-104
PT8850A	2N5847		3-104
PT8851	MRF221		—
PT8851A	MRF233		3-341
PT8852	MRF222		3-862
PT8852A	2N6082		3-107
PT8853	MRF224		3-113
PT8853A	2N6084		3-113
PT8854		MRF492	3-552
PT8854A		MRF492A	3-552
PT8860	2N4427		3-23
PT8861	MRF220		—
PT8861A	2N5589		—
PT8862	MRF222		3-862
PT8862A	MRF233		3-341
PT8863	MRF222		3-862
PT8863A	MRF234		3-345
PT8864	MRF223		3-862
PT8864A	2N6083		3-110
PT8865		MRF492	3-552
PT8865A		MRF492A	3-552
PT8866	MRF237		3-552
PT8870	MRF220		—
PT8870A	2N6081		3-104
PT8871	MRF616		—
PT8871A	2N5944		3-90
PT8873	MRF221		3-104
PT8873A	2N6081		3-104
PT8873F	MRF221		3-104
PT8874	MRF224		3-113
PT8874A	2N6084		3-113
PT8874F		MRF224	3-113
PT8877	MRF237		3-349
PT8880	MRF517		3-571
PT8881	MRF616		—
PT8881A		2N5944	3-90
PT8889		MRF526	—
PT9073B	MRF321		3-398
PT9700	MRF5174		3-915
PT9701		MRF5175	3-918
PT9701B	MRF5175		3-918
PT9702		MRF323	3-402
PT9702B	MRF323		3-402
PT9703	MRF331		3-422
PT9704		MRF5177A	3-924
PT9704A		MRF5177A	3-924
PT9704B		MRF5177A	3-924
PT9730		2N5641	3-64
PT9731	MRF314A		3-382
PT9732		2N5641	3-64
PT9733	MRF315A		3-386
PT9734		MRF314A	3-382
PT9776		MRF492	3-552
PT9776A		MRF492A	3-552
PT9780	MRF464		3-520
PT9780A		MRF464A	3-520
PT9782		MRF317	3-394
PT9782A		MRF317	3-394

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
PT9783		MRF466	3-524
PT9783A		MRF466	3-524
PT9784		MRF492	3-552
PT9784A		MRF492A	3-552
PT9785	MRF421		3-465
PT9787	MRF410		3-457
PT9787A	MRF410A		3-457
PT9788		MRF401	3-450
PT9788A	MRF401		3-450
PT9790	MRF428		3-481
PT9795	MRF222		3-862
PT9795A	MRF233		3-341
PT9796	MRF223		3-862
PT9796A	2N6083		3-110
PT9797	MRF450		3-502
PT9797A	MRF450A		3-502
PT9847		MRF421	3-465
PTE081	MRF890		3-786
R47M10	MHW709		—
R47M13	MHW710		—
R47M15	MHW710		—
RF14	MRF455A		3-509
RF15	MRF455		3-509
RF16		MRF455A	3-509
RF23	MRF224		3-113
RF25		MRF453	3-505
RF35	MRF453A		3-505
RF45	MRF453		3-505
RF46		MRF222	3-862
RF47	2N5847		3-104
RF48		2N6082	3-107
RF49		2N6084	3-113
RF85	MRF454		3-507
RF105	MRF421		3-465
RF110	MRF421		3-465
RF221	MRF221		3-104
RF260	MRF260		3-362
RF264	MRF264		3-374
RF1003	MRF221		3-104
RF1004	MRF223		3-862
RF2081	MRF216		—
RF2092		MRF460	3-515
RF2123	MRF238		—
RF2125		MRF450	3-502
RF2127	MRF245		—
RF2135	MRF223		3-862
RF2142	2N6367		3-493
RF2143		MRF454	3-507
RF2144	MRF224		3-113
RF2146	MRF476		3-532
RF2147	MRF475		3-528
S-AU3		MHW720-1	4-22
S-AU4		MHW720-1	4-22
S-AU6H		MHW710-3	4-18
S-AU6L		MHW710-1	4-18
S-AU6M		MHW710-2	4-18
S-AU7		MHW820-1	4-40
S-AU11		MHW806A3	4-37
S-AU12		MHW806-1	4-34
S10-12	MRF433		3-493

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
S10-28	MRF410		3-457
S15-12	MRF433		3-493
S15-28	MRF410		3-457
S15-50		MRF427	3-477
S25-12	MRF449		3-499
S25-50	MRF427		3-477
S30-28	MRF426		3-473
S50-12		MRF450	3-502
S50-28	MRF464		3-520
S80-12	MRF454		3-507
S100-12	MRF421		3-465
S100-28		MRF422	3-469
S100-50		MRF428	3-481
S175-28		MRF422	3-469
S175-50		MRF428	3-481
S200-50	MRF448		3-495
S250-50		MRF448	3-495
SD1005	2N5947		3-97
SD1006	2N5943		3-83
SD1007-1	MRF511		3-561
SD1012	2N5590		—
SD1012-3	MRF220		—
SD1013	2N5642		3-67
SD1013-3		2N5642	3-67
SD1014-1	MRF221		3-104
SD1014-6	MRF221		3-104
SD1015	MRF314A		3-382
SD1018-4	MRF224		3-113
SD1018-6	MRF224		3-113
SD1018-15	MRF224		3-113
SD1019		MRF317	3-394
SD1019	2N6166		3-116
SD1020		2N4427	3-23
SD1020-6		MRF313	3-380
SD1020-7	MRF313		3-380
SD1021	MRF212		—
SD1022	MRF1946A		3-862
SD1074	MRF453		3-505
SD1076	MRF454		3-507
SD1077		MRF475	3-528
SD1078	MRF464		3-520
SD1080	MRF207		—
SD1080-2	MRF628		3-620
SD1080-4	MRF604		3-660
SD1080-6	MRF627		3-666
SD1080-7	MRF626		—
SD1087	MRF641		3-674
SD1088	MRF644		3-678
SD1089	MRF646		3-682
SD1095		MRF840	3-734
SD1096		MRF842	3-744
SD1098		MRF844	3-754
SD1099		MRF846	3-757
SD1115-4	MRF607		3-663
SD1124	MRF245		—
SD1127	MRF237		3-349
SD1131	MRF629		—
SD1132-4		MRF750	3-706
SD1132-5	MRF838		3-724
SD1133	MRF212		—

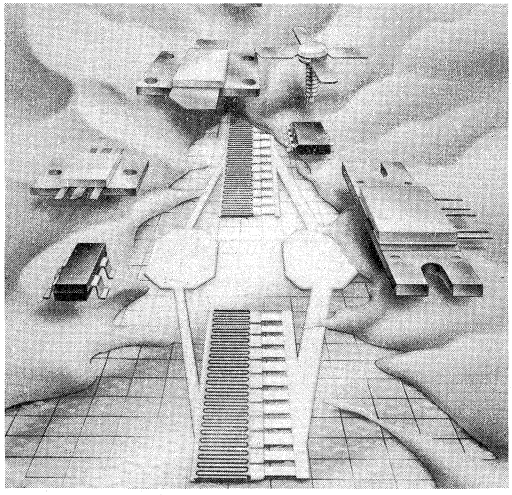
Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
SD1133-1		MRF212	—
SD1134	2N5944		3-90
SD1134-1		MRF227	3-339
SD1135	MRF652		3-690
SD1136	2N5946		3-90
SD1143	MRF212		—
SD1143-1	MRF221		3-104
SD1147	MRF5175		3-918
SD1148	MRF321		3-398
SD1149	MRF323		3-402
SD1166	MRF403		—
SD1167	2N5847		3-104
SD1168	2N5848		—
SD1169	2N5849		3-79
SD1174	2N6255		—
SD1177		2N5589	—
SD1200	2N3866		3-10
SD1212-4		MRF476	3-532
SD1212-7	MRF475		3-528
SD1214-4		MRF475	3-528
SD1214-6	MRF479		3-540
SD1216	2N5591		—
SD1218	MRF209		—
SD1220-1		2N5641	3-64
SD1222-5		2N5642	3-67
SD1222-6	2N5642		3-67
SD1224-2	MRF315		3-386
SD1224-4		MRF466	3-524
SD1224-10		MRF426	3-473
SD1229	2N6083		3-110
SD1229-1	MRF222		3-862
SD1232	MRF517		3-571
SD1242-5		2N5641	3-64
SD1244-6		2N5642	3-67
SD1245		MRF321	3-398
SD1256		2N5589	—
SD1262	MRF226		3-327
SD1272		MRF1946A	3-862
SD1273	MRF240		3-351
SD1274	MRF1946A		3-862
SD1274-1	MRF1946		3-862
SD1275	MRF240		3-351
SD1278		MRF240	3-351
SD1285	MRF406		3-453
SD1288	MRF453A		3-505
SD1289	MRF453		3-505
SD1290		2N6084	3-113
SD1295	MRF421		3-465
SD1299	MRF326		3-410
SD1300	BFY90		3-161
SD1301	BYF90		3-161
SD1303	2N6304		3-120
SD1308	MRF905		3-799
SD1309	2N2857		3-2
SD1315	MRF511		3-561
SD1316	MRF586		3-649
SD1317	MRF587		3-649
SD1330		MRF572	3-627
SD1331		MRF571	3-627
SD1333	BFR96		3-147

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
SD1334	MRF580		3-639
SD1347-7	MRF402		3-23
SD1375	2N4957		3-27
SD1377		MRF1000MA/B	3-818
SD1400-2	MRF892		3-776
SD1400-3		MRF892	3-776
SD1401	MRF894		3-780
SD1403	MRF428		3-481
SD1404	MRF427		3-477
SD1405	MRF492		3-552
SD1407		MRF435	3-469
SD1407-8		MRF435	3-469
SD1410		MRF841	3-738
SD1410-3		MRF840	3-734
SD1411		MRF842	3-744
SD1411-1	MRF842		3-744
SD1412		MRF842	3-744
SD1412-3	MRF842		3-744
SD1414		MRF846	3-757
SD1415	MRF216		—
SD1416	MRF247		3-355
SD1418		MRF842	3-744
SD1421	MRF844		3-754
SD1422	MRF644		3-678
SD1424	MRF449A		3-499
SD1425		MRF475	3-528
SD1427	MRF243		3-355
SD1428	MRF216		—
SD1429		MRF641	3-674
SD1429-3	MRF641		3-674
SD1433	MRF653		3-694
SD1434	MRF646		3-682
SD1438		MRF316	3-390
SD1438-2		MRF317	3-394
SD1444	MRF629		—
SD1446		MRF492	3-552
SD1449	MRF421		3-465
SD1450	MRF422		3-469
SD1451		MRF453	3-505
SD1451-1	MRF453		3-505
SD1452	MRF458		3-511
SD1461		MRF313	3-380
SD1462		MRF313	3-380
SD1464		MRF325	3-406
SD1465		MRF5177A	3-924
SD1466		MRF326	3-410
SD1467	MRF326		3-410
SD1468		MRF327	3-414
SD1469		MRF328	—
SD1480		MRF317	3-394
SD1482		MRF752	3-710
SD1484-10	MRF604		3-660
SD1485-3		MRF894	3-780
SD1487	MRF421		3-465
SD1488		MRF646	3-682
SD1496		MRF898	3-784
SD1496-3		MRF898	3-784
SD1499	MRF338		3-426
SD1499-1	MRF648		3-686
SD1510		MRF1035MA/B	3-838

INDEX CROSS-REFERENCE (Continued)

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
SD1511		MRF1035MA/B	3-838
SD1512		MRF1090MA/B	3-842
SD1513		MRF1090MA/B	3-842
SD1514		MRF1150MA/B	3-850
SD1520	MRF1000MA		3-818
SD1522	MRF1000MA		3-818
SD1522-2		MRF1002MA	3-822
SD1522-4	MRF1002MA		3-822
SD1524		MRF1004MA	3-826
SD1526		MRF1008MA	3-830
SD1528		MRF1035MA	3-838
SD1530	MRF1035MA		3-838
SD1532		MRF1090MA	3-842
SD1534	MRF1090MA		3-842
SD1536		MRF1090MA	3-842
SD1538	MRF1150MA		3-850
SD1540	MRF1325M		3-858
SD1544		MRF2001M	3-870
SD1545		MRF2003M	3-878
SD1574	MRF260		3-362
SD1575	MRF262		3-370
SD1577	MRF264		3-374
TAN15		MRF1015MC	3-834
TAN75		MRF1090MC	3-842
TAN150H		MRF1150MC	3-850
TAN250A		MRF1250M	3-854
TC0204-125	MRF392		3-442
TCC0105-100		MRF392	3-442
TH20		MRF430	3-489
TH416	MRF422		3-469
TH417		MRF422	3-469
TH430	MRF448		3-495
TH476		MRF5174	3-915
TH478		MRF321	3-398
TH480		MRF321	3-398
TH513	MRF428		3-481
TH518		MRF426A	3-473
TH519		2N6439	3-125
TH525	MRF323		3-402
TH526	MRF5177A		3-924
TH532		MRF325	3-406
TH550		MRF331	3-422
TH552	MRF321		3-398
TH553	MRF323		3-402
TH562		MRF448	3-495
TH569	MRF437		—
TH571	MRF426		3-473
TH1002	MRF2003		3-874
TH1005	MRF2005		3-882
TH1010	MRF2010		3-890
TH2001	MRF2001		3-866
TH2003	MRF2003		3-874
TH2005	MRF2005		3-882
THA13	MRF426A		3-473
THA15	MRF429		3-485
THA93	MRF314A		3-382
THB13		MRF426A	3-473
THB94	MRF315		3-386
THY94	MRF315A		3-386
TP312		BFR96	3-147

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
TP390	BFW92A		3-156
TP393	BFR91		3-142
TP394	MRF580		3-639
TP491	BFR91		3-142
TPM4040		MRF390	3-438
TPM4100		MRF392	3-442
TPM4130		MRF392	3-442
TPR10		MRF1015MB	3-834
TPR50		MRF1090MB	3-842
TPR150		MRF1150MB	3-850
TRF559	MRF559		3-620
TRW2001	MRF2001		3-866
TRW2003	MRF2003		3-874
TRW2005	MRF2005		3-882
TRW2010	MRF2010		3-890
TRW2015	MRF2016M		3-898
TSP150		MRF1150MC	3-850
TSP350		MRF1325M	3-858
TZ9401		MWA110	4-104
TZ9402		MWA120	4-104
TZ9403		MWA230	4-112
TZ9404		MWA230	4-112
UMIL1		MRF313	3-380
UMIL3		MRF5174	3-915
UMIL5		MRF331	3-422
UMIL5FT		MRF161	3-279
UMIL10	MRF321		3-398
UMIL20FT		MRF163	3-295
UMIL25	MRF325		3-406
UMIL-60	2N6439		3-125
UMIL-70	MRF327		3-414
UMIL-100		MRF329	3-418
UMIL-100A		MRF329	3-418
UMOB-45	MRF646		3-682
UMOB-55	MRF648		3-686
VAM-40		2N5643	3-70
VAM-80		2N6166	3-116
VAM-120		MRF317	3-394
VMIL-50		MRF464	3-520
VMIL-100	MRF317		3-394
VMIL20FT	MRF137		3-239
VMIL40FT	MRF171		3-303
VMIL60FT		MRF172	3-311
VMIL80FT		MRF172	3-311
VMIL120FT		MRF174	3-319
VMOB-70	MRF247		3-355
V996		2N6603	3-129



Selector Guide 2

Table of Contents

Page #

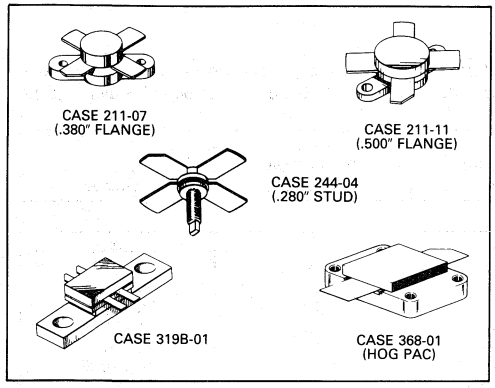
RF Power TMOS FETs
- 1.5–150 MHz HF/SSB FETs ... 2-3
- 2–200 MHz VHF AM/FM FETs ... 2-3
- 2–400 MHz UHF AM/FM FETs ... 2-3

RF Power Bipolar Transistors
- HF
  - 1.5–30 MHz, HF/SSB ... 2-4
  - 14–30 MHz, CB/Amateur ... 2-4
  - 27–50 MHz, Low-Band FM ... 2-5
- VHF
  - 30–200 MHz, VHF AM/FM ... 2-5
  - 66–88 MHz, Midband FM ... 2-5
  - 136–174 MHz, High-Band/VHF FM ... 2-6
  - 225 MHz, Amateur FM ... 2-6
- UHF
  - 100–400 MHz, AM/FM ... 2-7
  - 100–500 MHz, AM/FM ... 2-7
  - 407–512 MHz, UHF FM ... 2-7
- 800 MHz
  - 806–960 MHz, FM ... 2-8
- Microwave
  - L-Band Pulsed Power ... 2-9
  - 1.7–2.3 GHz Broadband CW ... 2-10
  - 2 GHz Narrowband CW ... 2-10

RF Small-Signal Transistors
- Selection by Package ... 2-11
  - Plastic SOE Case ... 2-11
  - Ceramic SOE Case ... 2-12
  - Metal Cans ... 2-13
- Low-Noise Transistors ... 2-14
- CATV, MATV, and Class A Linear Transistors ... 2-15
- High-Speed Switches ... 2-16
- UHF and Microwave Oscillators ... 2-16
- High Reliability (MIL) Transistors ... 2-16
- Complementary Devices ... 2-16

Tuning and Switching Diodes
- Tuning Diodes, Abrupt Junction ... 2-17
  - General-Purpose, Glass ... 2-17
  - General-Purpose, Plastic ... 2-18
- High Capacitance ... 2-19
- Dual Diodes ... 2-19
- Tuning Diodes Hyper-Abrupt Junction ... 2-20
- Hot-Carrier (Schottky) Diodes ... 2-21
- PIN Switching Diodes ... 2-21

Hybrid Amplifiers
- Land Mobile Hybrid Power Amplifiers
  - 407–512 MHz, UHF FM ... 2-22
  - 806–960 MHz, UHF FM ... 2-22
- CATV Distribution Hybrid Amplifiers
  - Forward Amplifiers to 40 Channels — 330 MHz ... 2-23
  - Forward Amplifiers to 60 Channels — 450 MHz ... 2-23
  - Forward Amplifiers to 77 Channels — 550 MHz ... 2-24
  - Reverse Amplifiers ... 2-24
  - 450/550 MHz Power Doubling ... 2-24
  - 450 MHz Feed Forward ... 2-24
- General Purpose Wideband Amplifiers
  - 50 Ω–100 Ω ... 2-25
  - 50 Ω TO-39 ... 2-25
  - 50 Ω–75 Ω ... 2-25
  - 50 Ω Monolithic Microwave Integrated Circuits ... 2-25



Power Transistors

RF Power TMOS FETs

Motorola RF Power MOSFETs, (trademark TMOS), are constructed using a planar process to enhance manufacturing repeatability. **They are N-channel field effect transistors** with an oxide insulated gate which controls vertical current flow.

Compared with bipolar transistors, RF Power FETs exhibit higher gain, higher input impedance, enhanced thermal stability and lower noise. The FETs listed in this section are specified for operation in RF Power Amplifiers and are grouped by frequency range of operation and type of application. Arrangement within each group is by order of first voltage then increasing output power.

1.5–150 MHz HF/SSB FETs

For military and commercial HF/SSB fixed, mobile, and marine transmitters. Data shown is for an operating frequency of 30 MHz.

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	G_{ps} Typical Gain dB	Typical IMD		Package
				d_3 dB	d_{11} dB	
V_{DD} = 28 Volts						
MRF138	30	0.6	17	−30	−60	211-07
MRF140	150	4.7	15	−30	−60	211-11
V_{DD} = 50 Volts						
MRF148	30	0.5	18	−35	−60	211-07
MRF150	150	2.9	17	−32	−60	211-11
MRF153	300	6	17	−25	—	368-01
MRF154	600	12	17	−25	—	368-01

2–200 MHz VHF AM/FM FETs

For VHF military and commercial aircraft radio transmitters. Data shown is for an operating frequency of 150 MHz.

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	G_{ps} Minimum Gain dB	η Minimum Efficiency %	Package
V_{DD} = 28 Volts					
MRF134	5	0.4	11	50	211-07
MRF136	15	0.75	13	50	211-07
MRF136Y	30	1.9	12	50	319B-01
MRF137	30	1.9	12	50	211-07
MRF171	45	2.8	12	50	211-07
MRF172	80	8	10	50	211-11
MRF174	125	15.8	9	50	211-11

2–400 MHz UHF AM/FM FETs

For VHF/UHF military and commercial aircraft radio transmitters. Data shown is for an operating frequency of 400 MHz.

V_{DD} = 28 Volts

MRF161	5	0.4	11	45	244-04
MRF162	15	1.2	11	45	244-04
MRF163	25	2.5	10	45	244-04

Bipolar Power RF Transistors

1.5–30 MHz, HF/SSB TRANSISTORS

Designed for broadband operation, these devices feature specified Intermodulation Distortion at rated power output. Applications include mobile, marine, fixed station, and amateur HF/SSB equipment, operating from 12.5, 13.6, 28 or 50 volt supplies. Data shown is for an operating frequency of 30 MHz.

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	G_{PE} Power Gain dB Min	Package
V_{CC} = 12.5 or 13.6 Volts				
MRF476	3 PEP/CW	0.1	15	TO-220
MRF475	12 PEP/CW	1.2	10	TO-220
MRF433	12.5 PEP/CW	0.125	20	211-07
MRF479	15 PEP/CW	1.5	10	TO-220CE
MRF406	20 PEP/CW	1.25	12	211-07
MRF460	40 PEP/CW	2.5	12	211-11
MRF477	40 PEP/CW	1.25	15	TO-220CE
MRF412	70 PEP/CW	3.5	13	211-11
MRF421	100 PEP/CW	10	10	211-11
V_{CC} = 28 Volts				
MRF410	10 PEP/CW	0.5	13	211-07
MRF410A	10 PEP/CW	0.5	13	145A-09
MRF485	15 PEP/CW	1.5	10	TO-220
MRF401	25 PEP/CW	1.25	13	145A-09
MRF426	25 PEP/CW	0.16	22	211-07
MRF426A	25 PEP/CW	0.16	22	145A-09
MRF466	40 PEP/CW	1.25	15	211-09
MRF486	40 PEP/CW	1.25	15	TO-220CE
MRF464	80 PEP/CW	2.53	15	211-11
MRF464A	80 PEP/CW	2.53	15	145A-10
MRF422	150 PEP/CW	15	10	211-11
MRF435	150 PEP/CW	15	10	211-11
V_{CC} = 50 Volts				
MRF427	25 PEP/CW	0.4	18	211-11
MRF427A	25 PEP/CW	0.4	18	145A-10
MRF437	25 PEP/CW	0.4	18	211-11
MRF437A	25 PEP/CW	0.4	18	145A-10
MRF428	150 PEP/CW	7.5	13	211-11
MRF429	150 PEP/CW	7.5	13	211-11
MRF448	250 PEP/CW	15.7	12	211-11
MRF430	600 PEP/CW	60	10	368-01

14–30 MHz, CB/AMATEUR TRANSISTORS

These HF transistors are designed for economical, high-volume use in CW, AM and SSB applications. Gains shown are for operating frequencies of 30 MHz.

V_{CC} = 12.5 or 13.6 Volts

MRF476	3	0.1	15	TO-220
MRF475	4	0.4	10	TO-220
MRF449/MRF449A	30	1.9	12	211-07/145A-09
MRF450	50	4	11	211-09
MRF450A	50	4	11	145A-09
MRF453/MRF453A	60	3	13	211-11/145A-10
MRF455	60	3	13	211-07
MRF455A	60	3	13	145A-09
MRF454	80	5	12	211-11
MRF454A	80	5	12	145A-10
MRF458/MRF458A	80	5	12	211-11/145A-10

27–50 MHz, LOW-BAND FM TRANSISTORS

For use in the FM "Low-Band," for Mobile communications. Gains shown are for operating frequencies of 50 MHz.

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	G_{PE} Power Gain dB Min	Package
V_{CC} = 12.5 or 13.6 Volts				
MRF402	1	0.1	10	TO-39
MRF475	4	0.4	10	TO-220
MRF497	40	4	10	TO-220CE
MRF492	70	5.6	11	211-11

VHF Transistors

30–200 MHz VHF AM/FM TRANSISTORS

Designed for Military Radio and Commercial Aircraft VHF bands, these 28-volt devices include the all-gold metallized MRF314/15/16/17 high-reliability series. Gains shown are for various frequencies of operation in the VHF band. Consult data sheets for specific detail.

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	G_{PE} Power Gain dB Min	Package
V_{CC} = 28 Volts				
2N3553	2.5	0.25	10	TO-39
2N5641	7	1	8.4	144B-05
MRF340	8	0.4	13	TO-220CE
2N5642	20	3	8.2	145A-09
MRF342	24	1.9	11	TO-220CE
MRF314	30	3	10	211-07
MRF314A	30	3	10	145A-09
2N5643	40	6.9	7.6	145A-09
MRF315	45	5.7	9	211-07
MRF315A	45	5.7	9	145A-09
MRF344	60	15	6	TO-220CE
MRF316 (1)	80	8	10	316-01
MRF317 (1)	100	12.5	9	316-01

66–88 MHz, MIDBAND FM TRANSISTORS

Power output chains up to 25 watts output are obtainable in the international VHF FM "Mid-Band" for which these transistors are optimized. Gains shown are for operating frequencies of 90 MHz.

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	G_{PE} Power Gain dB Min	Package
V_{CC} = 12.5 Volts				
MRF229	1.5	0.15	10	TO-39CE
MRF232	7.5	0.95	9	145A-09
MRF233	15	1.5	10	145A-09
MRF234	25	2.8	9.5	145A-09

(1) Internal Impedance Matched

136–174 MHz, HIGH-BAND/VHF FM TRANSISTORS

The "workhorse" VHF FM High-Band is served by Motorola with the broadest range of devices and package combinations in the industry. All gains shown are for operating frequencies of 175 MHz.

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	G_{PE} Power Gain dB Min	Package
V_{CC} = 12.5 Volts				
2N4427	1	0.1	10	TO-39
MRF604	1	0.1	10	TO-46
MRF553	1.5	0.11	11.5	317D-01
MRF607	1.75	0.12	11.5	TO-39
2N5589	3	0.44	8.2	144B-05
2N6255	3	0.5	7.8	TO-39
2N6080	4	0.25	12	145A-09
MRF220	4	0.25	12	211-07
MRF237	4	0.25	12	TO-39CE
MRF260	5	0.5	10	TO-220CE
2N5590	10	3	5.2	145A-09
MRF212	10	1.25	9	145A-09
MRF261	10	3	5.2	TO-220CE
2N6081	15	3.5	6.3	145A-09
MRF221	15	3.5	6.3	211-07
MRF262	15	3.5	6.3	TO-220CE
MRF2628	15	0.95	12	244-04
2N5591	25	9	4.4	145A-09
2N6082	25	6	6.2	145A-09
2N6083	30	8.1	5.7	145A-09
MRF238	30	3.7	9	145A-09
MRF239	30	3	10	145A-09
MRF264	30	9.1	5.2	TO-220CE
MRF1946	30	3	10	211-07
MRF1946A	30	3	10	145A-09
2N6084	40	14.3	4.5	145A-09
MRF224	40	14.3	4.5	211-07
MRF240	40	5	9	145A-09
MRF4070 (1)	70	20	5	316-01
MRF247 (1)	75	15	7	316-01
MRF248 (1)	80	8	10	316-01

225 MHz, AMATEUR FM TRANSISTORS

Specifically designed and characterized for the 225 MHz band, these devices eliminate the guesswork required when adapting 175 MHz characterized devices to this application. Gains shown are for operating frequencies of 225 MHz.

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	G_{PE} Power Gain dB Min	Package
V_{CC} = 12.5 Volts				
MRF207	1	0.15	8.2	TO-39
MRF225	1.5	0.18	9	TO-39
MRF227	3	0.13	13.5	TO-39CE
MRF208	10	0.1	10	145A-09
MRF226	13	1.6	9	145A-09

(1) Internal Impedance Matched

UHF Transistors

100–400 MHz, AM/FM TRANSISTORS

Stringent requirements of the UHF Military band are met by MRF325, 326, 327, 329, 331 and 2N6439 types, with all-gold metal systems, specified ruggedness and programmed wirebond construction, to assure consistent input impedances for internally matched parts. Hi-Rel versions of these transistors are available upon request. Gains shown are for operating frequencies of 400 MHz.

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	G_{PE} Power Gain dB Min	Package
V_{CC} = 28 Volts				
MRF525	0.02	0.001	13	TO-39CE
2N3866	1	0.1	10	TO-39
2N5160 (1)	1	0.16	8	TO-39
MRF5174	2	0.125	12	244-04
MRF331	10	1.6	8	244-04
MRF325 (2)	30	4.3	8.5	316-01
MRF5177A	30	7.5	6	145A-09
MRF326 (2)	40	8	9	316-01
MRF309 (2)	50	10	7	316-01
2N6439 (2)	60	10	7.8	316-01
MRF390 (3)	60	6.8	7.5	744-02
MRF327 (2)	80	14.9	7.3	316-01
MRF329 (2)	100	20	7	333-03
MRF392 (3)	125	19.8	8	744A-01

100–500 MHz, AM/FM TRANSISTORS

Similar to the 100–400 MHz transistors, these devices have bandwidth capabilities allowing their use to 500 MHz. All have nitride passivated die, gold metal systems, specified ruggedness and controlled wireband construction to meet the stringent requirements of military space applications. Hi-Rel versions are available upon request. Gains shown are at a frequency of 400 MHz unless otherwise noted.

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	G_{PE} Power Gain dB Min	Package
V_{CC} = 28 V				
MRF313	1	0.03	15	305A-01
MRF321	10	0.62	12	244-04
MRF323	20	2	10	244-04
MRF338 (2) (4)	80	15	7.3	333-03
MRF393 (3) (5)	125	19.8	8	744A-01

407–512 MHz, UHF FM TRANSISTORS

Higher power output devices in this UHF power transistor series feature internally input-matched construction, are designed for broadband operation, and have guaranteed ruggedness under output mismatch and RF overdrive conditions. Devices are specified for handheld, mobile and base station operation. Gains shown are for an operating frequency of 470 MHz.

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	G_{PE} Power Gain dB Min	Package
V_{CC} = 7.5 Volts				
MRF750	0.5	0.05	10	305A-01
MRF752	2.5	0.4	8	249-05
MRF754	8	2	6	249-05

(1) PNP
(2) Internal Impedance Matched.
(3) Internal Impedance Matched Push-Pull Transistors.
(4) Gain specified at 470 MHz
(5) Gain specified at 500 MHz.

UHF TRANSISTORS (continued)

407–512 MHz, UHF FM TRANSISTORS (continued)

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	G_{PE} Power Gain dB Min	Package
V_{CC} = 12.5 Volts				
MRF627	0.5	0.05	10	305A-01
MRF581 (1)	0.6	0.023	14	317-01
MRF515	0.75	0.12	8	TO-39
2N5644	1	0.2	7	145A-09
MRF555	1.5	0.15	10	317D-01
2N5944	2	0.25	9	244-04
MRF629	2	0.32	8	TO-39CE
MRF630	3	0.33	9.5	TO-39CE
2N5945	4	0.64	8	244-04
MRF652 (2)	5	0.5	10	244-04
MRF660	7	2	5.4	TO-220CE
2N5946	10	2.5	6	244-04
MRF653 (2)	10	2	7	244-04
MRF641 (4)	15	2.5	7.8	316-01
MRF654 (4)	15	2.5	7.8	244-04
MRF644 (4)	25	5.9	6.2	316-01
MRF646 (4)	40	13.3	4.8	316-01
MRF648 (4)	60	22	4.4	316-01

800 MHz Transistors

806–960 MHz, FM TRANSISTORS

Designed specifically for the 800 MHz mobile radio band, types MRF840 through 846 offer superior gain and ruggedness, using the unique CS-12 package, which minimizes common-element impedance, and thus maximizes gain and stability. Devices are listed for mobile and base station applications. Gains shown are for an operating frequency of 870 MHz, unless otherwise noted.

V_{CC} = 12.5 Volts				
MRF559	0.5	0.08	8	317-01
MRF581 (1)	0.6	0.06	10	317-01
MRF837	0.75	0.11	8	317-01
MRF8372	0.75	0.11	8	751-02
MRF838	1	0.22	6.5	305A-01
MRF838A	1	0.22	6.5	305-01
MRF557	1.5	0.23	8	317D-01
MRF839	3	0.46	8	305A-01
MRF839A	3	0.46	8	305-01
MRF839F	3	0.46	8	319-04
MRF841 (3)	5	0.7	8.5	244-04CB
MRF841F	5	0.7	8.5	319-04CB
MRF840 (3)	10	2.5	6	319-04CB
MRF843 (3)	15	3	7	244-04CB
MRF843F	15	3	7	319-04
MRF873	15	3	7	319-04
MRF842 (3)	20	5	6	319-04CB
MRF844 (3)	30	9	5.2	319-04CB
MRF846 (3)	40	15	4.3	319-04CB
MRF848 (3)	60	20	4.7	333A-01CB
V_{CC} = 24 Volts				
MRF890 (4)	2	0.25	9	305-01
MRF891 (4)	5	0.63	9	319-04
MRF892 (3) (4)	14	2	8.5	319-04CB
MRF894 (3) (4)	30	6	7	319-04CB
MRF898 (3) (4)	60	12	7	333A-01

(1) Typical gain. Part specified as small-signal transistor at 500 MHz.
(2) Gain at 512 MHz.
(3) Internal impedance matched.
(4) Gain specified at 900 MHz.

Microwave Transistors

L-BAND PULSED POWER

These products are designed to operate in short pulse width, 10 μs, low duty cycle, 1%, power amplifiers operating in the 960 to 1215 MHz band. All devices have internal impedance matching. The prime application is avionics equipment for distance measuring (DME), area navigation (TACAN) and interrogation (IFF). All devices offered with hermetic option.

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	G_{PE} Power Gain dB Min	Package
V_{CC} = 18 Volts				
MRF1000MA (1)	0.2	0.02	10	332-04
MRF1000MB (1)	0.2	0.02	10	332A-02
MRF1000MC (1)	0.2	0.02	10	361A-01

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	G_{PB} Power Gain dB Min	Package
V_{CC} = 35 Volts				
MRF1002MA	2	0.2	10	332-04
MRF1002MB	2	0.2	10	332A-02
MRF1002MC	2	0.2	10	361A-01
MRF1004MA	4	0.4	10	332-04
MRF1004MB	4	0.4	10	332A-02
MRF1004MC	4	0.4	10	361A-01
MRF1008MA	8	0.8	10	332-04
MRF1008MB	8	0.8	10	332A-02
MRF1008MC	8	0.8	10	361A-01
V_{CC} = 50 Volts				
MRF1015MA	15	1.5	10	332-04
MRF1015MB	15	1.5	10	332A-02
MRF1015MC	15	1.5	10	361A-01
MRF1035MA	35	3.5	10	332-04
MRF1035MB	35	3.5	10	332A-02
MRF1035MC	35	3.5	10	361A-01
MRF1090MA	90	9	10	332-04
MRF1090MB	90	9	10	332A-02
MRF1090MC	90	9	10	361A-01
MRF1150M	150	25	7.8	336-03
MRF1150MA	150	25	7.8	332-04
MRF1150MB	150	25	7.8	332A-02
MRF1150MC	150	25	7.8	361A-01
MRF1250M	250	63	6	336-03
MRF1325M	325	81	6	336-03

(1) Class A, Common Emitter

2

1.7–2.3 GHz BROADBAND CW

The MRF2000M Series of transistors have internal input impedance matching networks which facilitate broadband circuit designs in the 1.7 to 2.3 GHz telecommunications band. The devices are designed for Class B and C common base amplifier applications.

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	G_{PB} Power Gain dB Min	Package
V_{CC} = 24 Volts				
MRF2001M	1	0.14	8.5	337-02
MRF2003M	3	0.48	8	337-02
MRF2005M	5	0.89	7.5	337-02
MRF2010M	10	2	7	337-02
MRF2016M	16	3.6	6.5	337-02

2 GHz NARROWBAND CW

The MRF2000 Series of NPN Silicon microwave power transistors are designed for common base service in amplifier or oscillator applications in the 1 to 2.3 GHz frequency range.

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	G_{PB} Power Gain dB Min	Package
V_{CC} = 28 Volts				
MRF2001	1	0.13	9	328A-01
MRF2001B	1	0.13	9	328-02
MRF2003	3	0.5	7.8	328A-01
MRF2003B	3	0.5	7.8	328-02
MRF2005	5	0.8	8	328A-01
MRF2005B	5	0.8	8	328-02
MRF2010	10	2.5	6	328A-01
MRF2010B	10	2.5	6	328-02

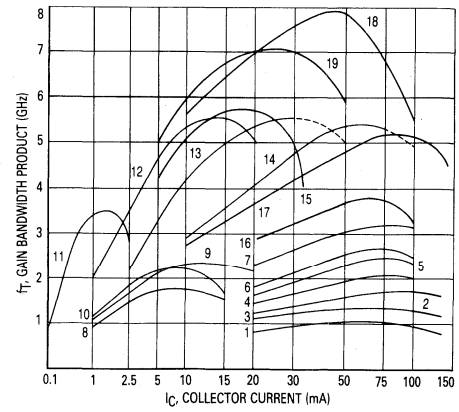
RF Small-Signal Transistors

Selection by Package

In small-signal RF applications, the package style is often determined by the end application or circuit construction technique. To aid the circuit designer in device selection, the Motorola broad range of RF small-signal amplifier transistors is organized by package. Devices for specific applications such as oscillators or switches are grouped in the appropriate succeeding tables. **These devices are NPN polarity unless otherwise designated.**

RF Small Signal Transistor Gain Characteristics

Curve numbers apply to transistors listed in the subsequent tables.



PLASTIC SOE CASE

Device	Gain-Bandwidth f_T @ I_C GHz Typ mA	Curve No. Page 2-10	Noise Figure NF @ f dB Typ MHz	Gain @ dB Typ f MHz	Maximum Ratings $V_{(BR)CEO}$ Volts	I_C mA	P_T mW	Package
Case 317-01 — MACRO-X								
MRF521 (1)	4.2 50	—	2.8 1000	11 1000	10	70	750	
MRF536 (1)	6 20	19	4.5 1000	10 1000	10	30	300	
MRF559	3 100	16	— —	13 512	18	150	2000	
MRF571	8 50	18	1.5 1000	12 1000	10	70	1000	
MRF581	5 75	17	2 500	15.5 500	18	200	2500	
MRF581A	5 75	17	1.8 500	15.5 500	15	200	2500	
MRF901	4.5 15	12	2 1000	12 1000	15	30	375	
MRF911	5 30	13	2.5 1000	12.5 1000	12	40	400	
MRF931	3 1	11	3.8 500	16 500	5	5	50	
MRF961	4.5 50	14	2 500	15 500	15	100	500	
MRF2369	6 40	18	1.5 1000	12 1000	15	70	750	
Case 317A-01 — MACRO-T								
BFR90	5 14	12	2.4 500	18 500	15	30	180	
BFR91	5 30	13	1.9 500	16 500	12	35	180	
BFR96	4.5 50	14	2 500	14.5 500	15	100	500	
BFW92A	4.5 10	15	2.7 500	16 500	15	35	180	
MRF580	5 75	17	2 500	14 500	18	200	2500	
MRF580A	5 75	17	1.8 500	14 500	15	200	2500	
Case 317D-01								
MRF542 (2)	— —	2	— —	5.5 250	70	400	3000	
MRF543 (1) (2)	— —	2	— —	5.5 250	70	400	3000	
MRF553	— —	—	— —	13 175	16	500	3000	
MRF555	— —	—	— —	12.5 470	16	400	3000	
MRF557	— —	—	— —	9 870	16	400	3000	
Case 318-02 — SOT-23								
BFR93	3 30	—	2.5 30	— —	12	35	350	
MMBR536 (1)	5.5 20	19	4.5 500	14 500	10	30	350	
MMBR571	8 50	18	2 500	16.5 500	10	80	350	
MMBR901	4 15	12	1.9 1000	13 1000	15	30	350	
MMBR911	6 30	13	2 500	17 500	12	40	350	
MMBR920	4.5 14	—	2.4 500	15 500	15	35	350	
MMBR930	5.5 30	—	1.9 500	11 500	12	35	350	

(1) PNP (2) Common Base Configuration.

(continued)

PLASTIC SOE CASE

Device	Gain-Bandwidth f_T GHz Typ	@ I_C mA	Curve No. Page 2-10	Noise Figure NF dB Typ	@ f MHz	Gain dB Typ	@ f MHz	Maximum Ratings $V_{(BR)CEO}$ Volts	I_C mA	P_T mW	Package
Case 318-02 (continued)											
MMBR931	3.5	1	11	4.3	1000	10	1000	5	5	350	
MMBR4957 (1)	2	2	10	3	450	17	450	30	30	350	
MMBR5031	2	5	—	1.9	450	17	450	10	20	350	
MMBR5179	1.5	5	8	4	450	11	450	12	50	350	
Case 318A-02 — SOT-143											
MRF5211 (1)	4.2	50	—	2.8	1000	11	1000	10	70	580	
MRF5711	7.5	50	18	1.6	1000	13.5	1000	10	70	580	
MRF9011	3.8	15	12	2.3	1000	10.2	1000	15	30	300	
MRF9331	5	1	—	2.5	1000	12.5	1000	8	1	50	
Case 345-01, SOT-89											
BFQ17	1.2	150	2	—	—	—	—	25	300	1000	
MXR100	4	50	—	—	—	—	—	18	200	1000	
MXR571	7	50	18	2.1	500	15	500	10	80	1000	
MXR911	7	30	13	2	500	16	500	12	40	1000	
MXR3866	0.8	50	1	—	—	12	400	30	400	1000	
MXR5583 (1)	1.5	100	5	—	—	—	—	30	500	1000	
MXR5943	1.4	50	4	3.4	200	11.4	200	30	400	1000	
Case 751-02 — SO-8											
MRF5812	5	75	17	1.8	500	16	500	15	200	1500	
MRF8372	—	—	17	—	—	10	870	16	200	1500	
Case 29-02, TO-226AA											
MPS536 (1)	5	20	19	4.5	500	14	500	10	30	625	
MPS571	6	50	18	2	500	14	500	10	80	625	
MPS901	4.5	15	12	2.5	900	12	900	15	30	625	
MPS911	7	30	13	1.7	500	16.5	500	12	40	625	
MPS3866	0.8	50	1	—	—	10	400	30	400	625	
CERAMIC SOE CASE											
Case 144D-06											
2N5947	1.5	75	3	3.8	200	11	250	30	400	5000	
MRF511	2.1	80	7	7.3	200	11	250	25	250	5000	
Case 244A-01											
MRF546 (2)	—	—	—	—	—	6	250	70	600	9000	
MRF547 (2)(1)	—	—	—	—	—	5.5	250	70	600	9000	
MRF548 (2)	—	—	2	—	—	5.5	250	70	400	5000	
MRF549 (2)(1)	—	—	2	—	—	5.5	250	70	400	5000	
MRF587	5.5	90	17	3	500	13	500	17	200	5000	

(1) PNP (2) Common Base Configuration.

CERAMIC SOE CASE (continued)

Device	Gain-Bandwidth f_T @ I_C GHz Typ mA	Curve No. Page 2-10	Noise Figure NF @ f dB Max MHz	Gain @ dB Min f MHz	Maximum Ratings $V_{(BR)CEO}$ Volts	I_C mA	P_T mW	Package
Case 303-01								
2N6603	5.5 15	12	2.5 1000	10 1000	15	30	400	
2N6604	5.5 30	13	3 1000	9 1000	15	50	500	
MRF522 (1)	4.2 50	—	3.5 1000	10 1000	10	50	620	
MRF572	8 50	18	2 1000	10 1000	10	70	750	
MRF962	4.5 50	14	2 (2) 500	16.5 (2) 500	15	100	750	
Case 358-01								
MRF573	8 50	18	2 1000	10 1000	10	70	750	
TO-72 METAL CAN								
2N2857	1.6 8	8	4.5 450	12.5 450	15	40	200	
2N4957 (1)	1.6 2	10	3 450	17 450	30	30	200	
2N4958 (1)	1.5 2	10	3.3 450	16 450	30	30	200	
2N4959 (1)	1.5 2	10	3.8 450	15 450	30	30	200	
2N5031	1.6 5	8	2.5 450	14 450	10	20	200	
2N5032	1.5 5	8	3 450	14 450	10	20	200	
2N5179	1.4 10	8	4.5 200	15 200	12	50	200	
2N6304	1.8 10	9	4.5 450	15 450	15	50	200	
2N6305	1.8 10	9	5.5 450	12 450	15	50	200	
BFX89	1.6 25	9	6.5 500	19 200	15	50	200	
BFY90	1.7 25	9	5 500	21 (2) 200	15	50	200	
MM4049 (1)	5 20	19	3 (2) 500	11.5 500	10	30	200	
MRF501	1 5	8	4.5 (2) 200	15 (2) 200	15	50	200	
MRF502	1.2 5	8	4 (2) 200	17 (2) 200	15	50	200	
MRF524 (1)	4.2 50	—	2.5 500	9 500	10	50	200	
MRF904	4 15	12	1.5 (2) 450	16 (2) 450	15	30	200	
MRF914	4.5 20	13	2 (2) 500	15 (2) 500	12	40	200	
TO-39 METAL CAN								
2N5109	1.5 50	4	3 (2) 200	11 216	20	400	2500	
2N5583 (1)	1.5 100	5	— —	— —	30	500	5000	
2N5943	1.5 50	4	3.4 (2) 200	11.4 (2) 200	30	400	3500	
MM8000	0.8 50	1	2.7 (2) 200	11.4 (2) 200	30	400	3500	
MM8001	1 50	4	2.7 (2) 200	11.4 (2) 200	30	400	3500	
MRF517	2.7 60	7	7.5 300	10 (2) 300	20	150	2500	
MRF525 (TO-39CE)	3 50	7	4 400	13 400	20	150	2500	
MRF544	1.4 50	2	— —	16.5 (2) 250	70	400	3500	
MRF545 (1)	1.2 50	2	— —	15.5 (2) 250	70	400	3500	
MRF586	4.5 90	17	4 500	9 500	17	200	2500	

(1) PNP (2) Typical

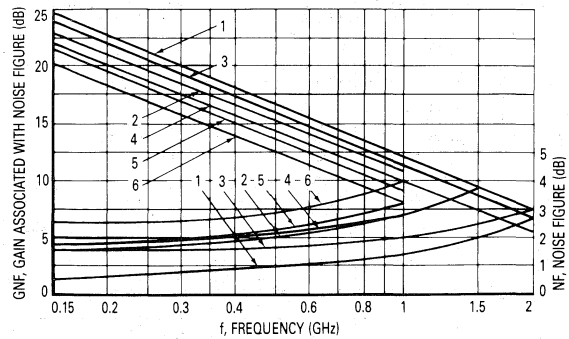
Low-Noise Transistors

The Small-Signal devices listed are designed for low noise and high gain amplifier mixer, and multiplier applications. Each transistor type is available in various packages. **Polarity is NPN unless otherwise noted.**

Package	Name	Case Number	Curve Number					
			1	2	3	4	5	6(1)
	MACRO-T	317A-01	—	MRF580	—	BFR91	BFR96	—
	MACRO-X	317-01	MRF571	MRF581	MRF901	MRF911	MRF961	MRF536
	—	303-01	MRF572	—	2N6603	2N6604	MRF962	—
	MICRO-X	358-01	MRF573	—	—	—	—	—
	TO-72	20-03	—	—	MRF904	MRF914	—	MM4049
	TO-46	26-03	—	—	—	—	MRF965	—
	TO-92	29-02	MPS571	—	MPS901	MPS911	—	MPS536
	SOT-23	318-02/03	MMBR571	—	MMBR901	MMBR911	—	MMBR536
	SOT-89	345-01	MXR571	MXR100	—	MXR911	—	—
	SOT-143	318A-02	MRF5711	—	MRF9011	—	—	—
	SO-8	751-02	—	MRF5812	—	—	—	—

(1) PNP

Gain and Noise Figure versus Frequency



CATV, MATV, and Class A Linear Transistors

For Class A linear CATV/MATV applications. Listed according to increasing gain-bandwidth (f_T).

Device	Nominal Test Conditions V_{CE}/I_C Volts/mA	f_T MHz Typ	Noise Figure	Distortion Specifications				Package
			Typ/Freq. dB/MHz	2nd Order IMD	3rd Order IMD	12 Ch. Cross-Mod.	Output Level dBmV	
MRF501	6/5	1000	4.5/200					TO-72
MRF502	6/5	1200	4/200					TO-72
BFQ17	15/150	1200						SOT-89
2N5179	6/10	1400	3.2/200					TO-72
MXR5943	15/50	1400	3.4/200	−50		−42	+50	SOT-89
MXR5583 (1)	10/100	1500						SOT-89
MMBR5179	6/5	1500	4/450					SOT-23
2N5109	15/50	1500	3/200					TO-39
2N5943	15/50	1500	3.4/200	−50		−4	+50	TO-39
2N5947	20/75	1500	3.8/200		−55	−60	+50	TO-117
BFX89	5/25	1600	2.5/500					TO-72
BFY90	5/25	1700	2.5/500					TO-72
2N6305	5/10	1800	4/450					TO-72
2N6304	5/10	1800	3.2/450					TO-72
MMBR4957 (1)	10/2	2000	3/450					SOT-23
MMBR5031	6/5	2000	1.9/450					SOT-23
MRF511	20/80	2100	7.3/200	−50	−65	−57	+50	TO-117
MRF517	15/60	2700	6.5/300	−60	−72	−57	+45	TO-39
MMBR920	10/14	4500	2.4/500					SOT-23
BFW92A	10/10	4500	2.7/500					317A-01
MRF586	15/90	4500	3/500	−50	−72		+50	TO-39
BFR96	10/50	4500	2/500					317A-01
MRF961	10/50	4500	2/500					317-01
MRF962	10/50	4500	2/500					303-01
MRF965	10/50	4500	2/500					TO-46
BFR90	10/14	5000	2.4/500					317A-01
BFR91	5/30	5000	1.9/500					317A-01
MRF581	10/75	5000	2/500		−65		+50	317-01
MRF581A	10/75	5000	1.8/500		−65		+50	317-01
MRF5812	10/75	5000	1.8/500		−65		+50	751-02
MRF587	15/90	5500	3/500	−52	−72		+50	TO-117

(1) PNP

High-Speed Switches

The transistors listed below are for use as high-frequency current-mode switches. They are also suitable for RF amplifier and oscillator applications. The devices are listed in ascending order of collector current. These devices are NPN polarity unless otherwise designated.

Device	Test Conditions I_C/V_{CE} mA/Volts	f_T MHz Min	$r_b' C_C$ ps Max	Package
2N3959	10/10	1300	25	TO-18
2N3960	10/10	1600	40	TO-18
2N5835	10/6	2500	5 (2)	TO-72
MM4049 (1)	20/5	4000	15	TO-72
MRF914	20/10	4500 (2)	—	TO-72
2N5583 (1)	50/10	1000	8 (2)	TO-39
2N5836	50/6	2000	6 (2)	TO-46
2N5943	50/15	1200	5.5 (2)	TO-39
2N5837	100/3	1700	6 (2)	TO-46

2

UHF and Microwave Oscillators

The transistors listed below are for UHF and microwave oscillator applications as initial signal sources or as output stages of limited range transmitters. Devices are listed in order of increasing output power.

Device	Test Conditions f MHz	Test Conditions V_{CC} Volts	P_{out} mW Min	f_T MHz Typ	Package
2N5179	500	10	20	1400	TO-72
2N2857	500	10	30	1600	TO-72
MM8009	1680	20	200	1400	TO-39
2N5108	1680	20	300	1400	TO-39
MRF905	1680	20	500 (2)	2200	TO-46
2N3866	400	15	1000	800	TO-39
MPS3866	400	15	1000	800	TO-226AA
MXR3866	400	15	1000	800	SOT-89

(1) PNP (2) Typical

High Reliability (MIL) Transistors

The listed devices are active per QPL-19500 (Qualified Products List). For detailed specification, see indicated page #.

Device	Page #	JAN	JTX	JTXV	JANS
2N2857	210	X	X	X	X
2N3553	201	X	X	X	
2N3866	203	X	X	X	
2N3866A	203	X	X	X	
2N3959	213			X	
2N3960	213	X	X	X	
2N4957	210	X	X	X	
2N5109	210	X	X	X	
2N6603	210	X	X	X	
2N6604	210	X	X	X	

Complementary Devices

The transistor complements listed are suitable for most applications requiring NPN and PNP devices of similar RF characteristics. Special matching of complementary transistors is available upon request. See indicated pages for specifications.

NPN	Page #	PNP	Page #
2N2857	210	2N4958	210
2N3866	203	2N5160	203
2N5943	210	2N5583	210
MRF904	210	MM4049	210
MRF571	208	MRF521	208

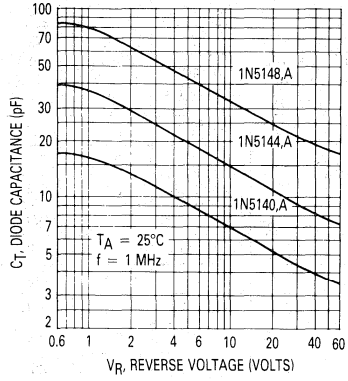
Tuning and Switching Diodes

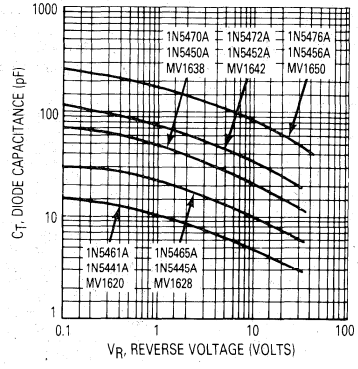
Tuning Diodes
Abrupt Junction

Voltage variable capacitance diodes for electronic tuning and control of RF circuits through UHF frequencies. Utilized for television tuning and AFC circuits.

TYPICAL CHARACTERISTICS

Diode Capacitance versus Reverse Voltage





2

General-Purpose

Glass



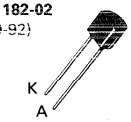
CASE 51-02
DO-204AA
(DO-7)

	• High Q • Capacitance TOL 10% — No Suffix 5% — Suffix A			• Premium 30 V • Very High Q • Guaranteed High CR • Capacitance TOL 10% – A, 5% – B, 2% – C			• High Q • Controlled CR • Capacitance TOL 10% – A, 5% – B, 2% – C			• General-Purpose		
	Maximum Working Voltage											
	60 Volts			30 Volts						20 Volts		
	Cap Ratio C4/C60 Min	**Q @ 4 V 50 MHz Min**	**Device Type**	**Cap Ratio C2/C30 Min**	**Q @ 4 V 50 MHz Min**	**Device Type**	**Cap Ratio C2/C30 Min**	**Q @ 4 V 50 MHz Min**	**Device Type**	**Cap Ratio C2/C20 Min**	**Q @ 4 V 50 MHz Min**	**Device Type**
C_T Nominal Capacitance pF ±10% @ V_R = 4 V f = 1 MHz												
6.8	2.7	350	1N5139,A	2.7	600	1N5461A	2.5	450	1N5441A	2	300	MV1620
8.2				2.8	600	1N5462A	2.5	450	1N5442A	2	300	MV1622
10	2.8	300	1N5140,A	2.8	550	1N5463A	2.6	400	1N5443A	2	300	MV1624
12	2.8	300	1N5141,A	2.8	550	1N5464A	2.6	400	1N5444A	2	300	MV1626
15	2.8	250	1N5142,A	2.8	550	1N5465A	2.6	450	1N5445A	2	250	MV1628
18	2.8	250	1N5143,A	2.9	500	1N5466A	2.6	350	1N5446A	2	250	MV1630
20				2.9	500	1N5467A	2.6	350	1N5447A	2	250	MV1632
22	3.2	200	1N5144,A	2.9	500	1N5468A	2.6	350	1N5448A	2	250	MV1634
27	3.2	200	1N5145,A	2.9	500	1N5469A	2.6	350	1N5449A	2	200	MV1636
33	3.2	200	1N5146,A	2.9	500	1N5470A	2.6	350	1N5450A	2	200	MV1638
39	3.2	200	1N5147,A	2.9	450	1N5471A	2.6	300	1N5451A	2	200	MV1640
47	3.2	200	1N5148,A	2.9	400	1N5472A	2.6	250	1N5452A	2	200	MV1642
56				2.9	300	1N5473A	2.6	200	1N5453A	2	150	MV1644
68				2.9	250	1N5474A	2.7	175	1N5454A	2	150	MV1646
82				2.9	225	1N5475A	2.7	175	1N5455A	2	150	MV1648
100				2.9	200	1N5476A	2.7	175	1N5456A	2	150	MV1650

General-Purpose

Plastic

CASE 182-02
(TO-92)



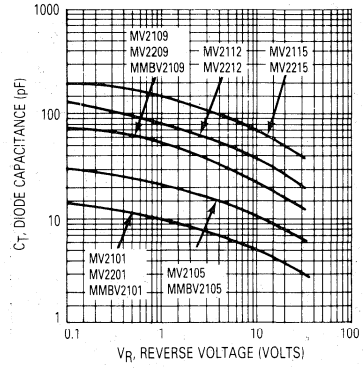
CASE 318-02
(TO-236AA)



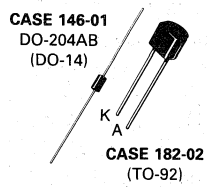
		• Low-Cost • High Volume			• Lower Cost • General Purpose			• Low-Cost • High Volume		
		Maximum Working Voltage								
		30 Volts			25 Volts			30 Volts		
		CASE 182-02 2-Lead TO-92						CASE 318-02 TO-236AA		
		Cap Ratio C2/C30 Min	Q @ 4 V 50 MHz Min	Device Type	Cap Ratio C1/C10 Min	Q @ 4 V 50 MHz Min	Device Type C_T ±20%	Cap Ratio C2/C30 Min	Q @ 4 V 50 MHz Typ	Device Type
C_T Nominal Capacitance pF ±10% @ V_R = 4 V f = 1 MHz	6.8	2.5	450	MV2101	1.9	300	MV2201	2.5	400	MMBV2101
	8.2	2.5	450	MV2102				2.5	350	MMBV2102
	10	2.5	400	MV2103	2	200	MV2203	2.5	350	MMBV2103
	12	2.5	400	MV2104				2.5	350	MMBV2104
	15	2.5	400	MV2105	2	200	MV2205	2.5	350	MMBV2105
	18	2.5	350	MV2106				2.5	300	MMBV2106
	22	2.5	350	MV2107	2	150	MV2207	2.5	300	MMBV2107
	27	2.5	300	MV2108				2.5	250	MMBV2108
	33	2.5	200	MV2109	2	150	MV2209	2.5	200	MMBV2109
	39	2.5	150	MV2110						
	47	2.5	150	MV2111	2	100	MV2211			
	56	2.6	150	MV2112						
	68	2.6	150	MV2113	2	100	MV2213			
	82	2.6	100	MV2114						
	100	2.6	100	MV2115	2	50	MV2215			

TYPICAL CHARACTERISTICS

Diode Capacitance versus Reverse Voltage



High Capacitance



CASE 146-01
DO-204AB
(DO-14)

CASE 182-02
(TO-92)

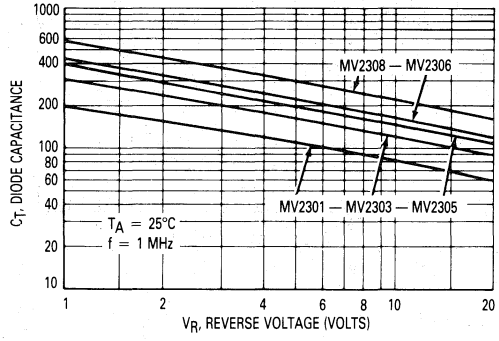
C_T Nominal Capacitance pF ±10% @ V_R = 4 V f = 1 MHz	MAXIMUM WORKING VOLTAGE 20 Volts							
	Case 182-02 (TO-92)			**CASE 146-01,** DO-204AB (DO-14)			
	Cap Ratio C2/C20 Min	**Q @ 4 V 20 MHz Min**	**Device Type**	**Cap Ratio C2/C20 Min**	**Q @ 4 V 20 MHz Min**	**Device Type**	**C_T**
120	2.3	250	MV2301	2	250	MV1652	120
150	2.3	250	MV2302	2	250	MV1654	150
180	2.3	200	MV2303	2	200	MV1656	180
200	2.3	200	MV2304	2	200	MV1658	200
220	2.3	150	MV2305	2	150	MV1660	220
250	2.3	150	MV2306	1.8*	150	MV1662**	250
270	2.3	100	MV2307	1.8*	100	MV1664**	270
330	2.3	100	MV2308	1.8*	100	MV1666**	330

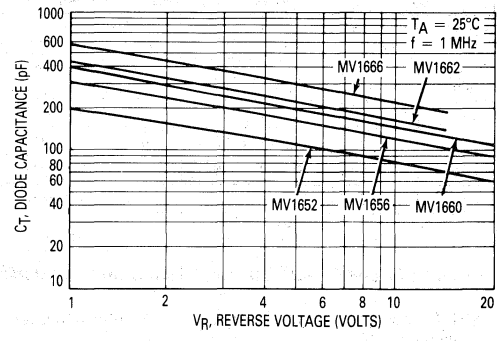
*C2/C15 **Maximum Working Voltage 15 V

2

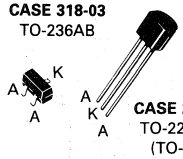
TYPICAL CHARACTERISTICS

Diode Capacitance versus Reverse Voltage





Dual Diodes



CASE 318-03
TO-236AB

CASE 29-02
TO-226AA
(TO-92)

- High Q
- Guaranteed Capacitance Range
- Monolithic Dual

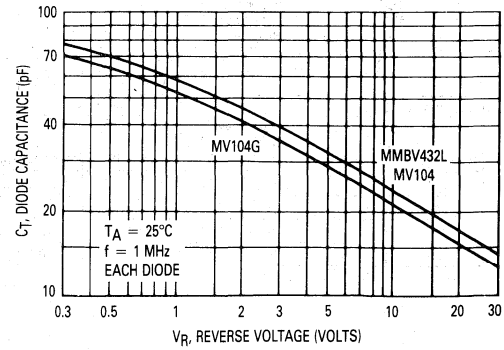
Maximum Working Voltage
32 Volts

C_T Capacitance pF @ V_R			Cap Ratio C3/C30 Min	Q @ 3 V 50 MHz Min	Device Type
Min	**Max**	**Volts**			
34	39	3	2.5	100	MV104G(1)
37	42	3	2.5	100	MV104(1)
43	48.1	2	1.5*	100	MMBV432L(2)

(1) Case 29 (2) Case 318 *C2/C8

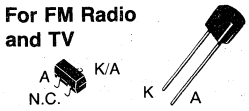
TYPICAL CHARACTERISTICS

Diode Capacitance versus Reverse Voltage



Tuning Diodes Hyper-Abrupt Junction

For FM Radio and TV



CASE 318-02 (TO-236AA) **CASE 182-02** (TO-92)

- High Q
- Guaranteed Capacitance Range

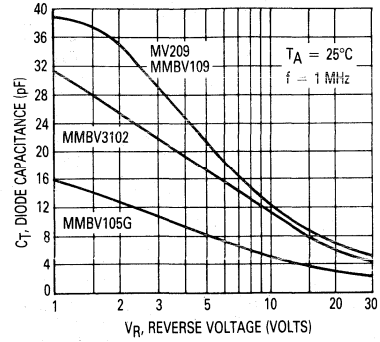
Maximum Working Voltage: 30 Volts

C_T Capacitance pF @ V_R Volts			Cap Ratio C3/C25 Min	Q @ 3 V 50 MHz Typ	Device Type
Min	Max				
1.8	2.8	25	4	350	MMBV105G*
20	25	3	4.5	300	MMBV3102*
26	32	3	5	250	MMBV109*
26	32	3	5	250	MV209**

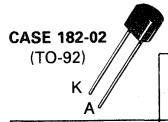
*Case 318 **Case 182

TYPICAL CHARACTERISTICS

Diode Capacitance versus Reverse Voltage



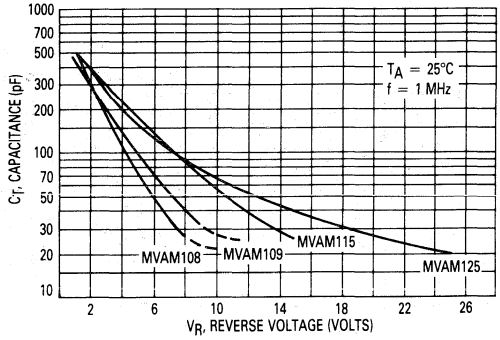
For AM Radio



CASE 182-02 (TO-92)

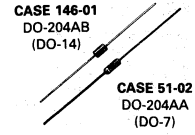
- High Capacitance Ratio
- Guaranteed Diode Capacitance
- Close Matching

C_T		Q @ 1 Vdc, 1 MHz = 150 (Min)			
V_R=1 V, f=1 MHz pF		$V_{BR(R)}$ Min	Cap Ratio Min	@ V_R Volts	Device Type
Min	Max				
440	560	12	15	1/8	MVAM108
400	520	15	12	1/9	MVAM109
440	560	18	15	1/15	MVAM115
440	560	28	15	1/25	MVAM125



For High Capacitance and High Reliability Applications

100% Screening to High Rel electrical and environmental specifications, H suffix.



CASE 146-01 DO-204AB (DO-14)

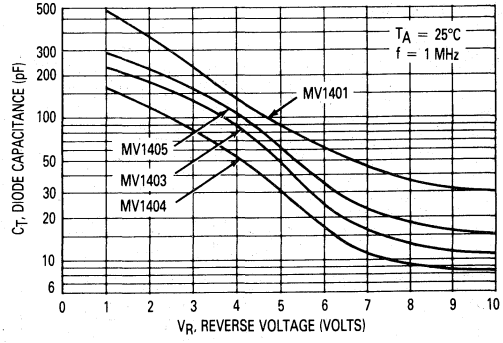
CASE 51-02 DO-204AA (DO-7)

- Hyper-Abrupt
- High Tuning Ratio
- High Rel — Suffix H

Maximum Working Voltage: 12 Volts

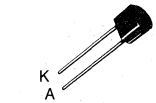
C_T, Nominal Capacitance pF @ V_R Volts Nom ± 20%		Cap Ratio C2/C10 Min	Q @ 2 V 1 MHz Min	Device Type	
				Case 51	Case 146
120	2	10	200	MV1404,H	
175	2	10	200	MV1403,H	
250	2	10	200	MV1405,H	
550*	1	14(1)	200		MV1401,H

*±15% (1)Cap Ratio @ C1/C10 V



Hot-Carrier (Schottky) Diodes

Hot-Carrier diodes are ideal for VHF and UHF mixer and detector applications as well as many higher frequency applications. They provide stable electrical characteristics by eliminating the point-contact diode presently used in many applications.



CASE 182-02



CASE 318-02

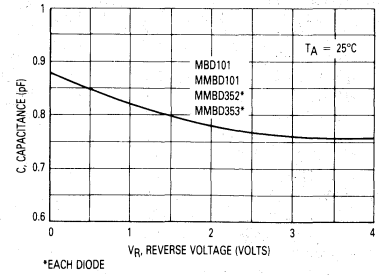
CASE 318-02

STYLE 8:	STYLE 11:	STYLE 19:
PIN 1. ANODE	PIN 1. ANODE	PIN 1. CATHODE
2. N.C.	2. CATHODE	2. ANODE
3. CATHODE	3. CATHODE/ ANODE	3. CATHODE/ ANODE

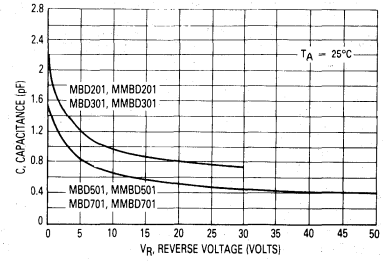
$V_{(BR)R}$ I_R = 10 μA Volts Min	C_T f = 1 MHz pF Max	@ Volts V_R	V_F I_F = 10 mA Volts Max	I_R nA Max	@ Volts V_R	Device Type
CASE 182, STYLE 1						
4	1	0	0.6	250	3	MBD101
20	1.5	15	0.6	200	15	MBD201
30	1.5	15	0.6	200	25	MBD301
50	1	20	1.2	200	25	MBD501
70	1	20	1.2	200	35	MBD701
CASE 318, STYLE 8						
4	1	0	0.6	250	3	MMBD101
20	1.5	15	0.6	200	15	MMBD201
30	1.5	15	0.6	200	25	MMBD301
50	1	20	1.2	200	25	MMBD501
70	1	20	1.2	200	35	MMBD701
DUAL DIODES, CASE 318, STYLE 11*, STYLE 19**						
4	1	0	0.6	250	3	MMBD352*
4	1	0	0.6	250	3	MMBD353**

TYPICAL CHARACTERISTICS

Capacitance versus Reverse Voltage



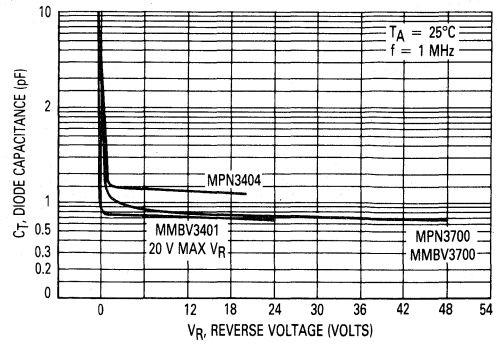
*EACH DIODE



PIN Switching Diodes

. . . designed for VHF band switching and general-purpose switching.

$V_{(BR)R}$ I_R = 10 μAdc Volts Min	R_S I_F = 10 mAdc f = 100 MHz Ohms Max	C_T V_R = 20 V f = 1 MHz pF Max	Device Type
CASE 182, STYLE 1			
20	0.85	2	MPN3404
200	1	1	MPN3700
CASE 318, STYLE 8			
35	0.7	1	MMBV3401
200	1	1	MMBV3700



Hybrid Amplifiers

Land Mobile Hybrid Power Amplifiers

The advantages of small size, reproducibility and overall lower cost become more pronounced with increasing frequency of operation. These modules offer a wide range in power levels and gain, with guaranteed performance specifications for bandwidth, stability and ruggedness.

407–512 MHz, UHF FM MODULES

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	f Frequency MHz	G_P Power Gain dB Min	V_{CC} Supply Voltage Volts	Package
MHW709-1	7.5	0.1	400–440	18.8	12.5	700-03
MHW709-2	7.5	0.1	440–470	18.8	12.5	700-03
MHW709-3	7.5	0.1	470–512	18.8	12.5	700-03
MHW710-1	13	0.15	400–440	19.4	12.5	700-03
MHW710-2	13	0.15	440–470	19.4	12.5	700-03
MHW710-3	13	0.15	470–512	19.4	12.5	700-03
MHW720-1	20	0.15	400–440	21	12.5	700-03
MHW720-2	20	0.15	440–470	21	12.5	700-03
MHW720A1 (1)	20	0.15	400–440	21	12.5	700-03
MHW720A2 (1)	20	0.15	440–470	21	12.5	700-03
MHW725-1 (1)*	25	0.15	400–440	22.2	12.5	301D-01
MHW725-2 (1)*	25	0.15	440–470	22.2	12.5	301D-01
MHW725-3 (1)*	25	0.15	470–512	22.2	12.5	301D-01

806–960 MHz, UHF FM MODULES

MHW802-1	2.2	0.02	825–845	20.4	9.5	784-01
MHW802-2	2.2	0.02	890–915	20.4	9.5	784-01
MHW806-1	6	0.25	820–850	13.8	12.5	297B-01
MHW806-2	6	0.25	806–870	13.8	12.5	297B-01
MHW806-3	6	0.35	890–915	12.3	12.5	297B-01
MHW806-4	6	0.35	870–960	12.3	12.5	297B-01
MHW806A1 (1)*	6	0.03	820–850	23	12.5	301H-01
MHW806A2 (1)*	6	0.03	806–870	23	12.5	301H-01
MHW806A3 (1)*	6	0.03	890–915	23	12.5	301H-01
MHW806A4 (1)*	6	0.03	870–960	23	12.5	301H-01
MHW806A5 (1)*	6	0.10	820–850	17.8	12.5	301H-01
MHW806A6 (1)*	6	0.10	806–870	17.8	12.5	301H-01
MHW806A7 (1)*	6	0.10	890–915	17.8	12.5	301H-01
MHW806A8 (1)*	6	0.10	870–960	17.8	12.5	301H-01
MHW812A1 (1)*	15	0.25	806–870	17.8	12.5	301D-01
MHW812A2 (1)*	15	0.25	806–890	17.8	12.5	301D-01
MHW812A3 (1)*	15	0.25	870–960	17.8	12.5	301D-01
MHW820-1	20	0.25	806–870	19	12.5	301G-01
MHW820-2	20	0.25	806–890	19	12.5	301G-01
MHW820-3	18	0.35	870–950	17.1	12.5	301G-01

(1) Designed for Wide Range P_{out} Level Control
*To be introduced

CATV Distribution Hybrid Amplifiers

Motorola Hybrids are manufactured using fourth generation technology which has set new standards for CATV system performance and reliability. These hybrids have been optimized to provide premium performance in all CATV systems up to 77 channels.

HYBRIDS UP TO 40 CHANNELS AND 330 MHz (Case 714-03)

Device	Hybrid Gain (Nominal) dB	Channel Loading Capacity	Maximum Distortion Specifications						Noise Figure @ 330 MHz dB	
			Output Level dBmV	2nd Order Test (1) dB	Composite Triple Beat dB		Cross Modulation dB			
					35 CH	40 CH	35 CH	40 CH	Max	Typ
MHW1121	12	40	+50	−68	−51	—	−51	—	7	6
MHW1122	12	40	+50	−70	−56	—	−56	—	8	6.5
MHW3171	17	40	+50	−68	−56	−54	−55	−54	6	5.5
MHW3172	17	40	+50	−70	−59	−57	−58	−57	7	6
MHW3181	18	40	+50	−68	−54	−52	−55	−54	6	5.2
MHW3182	18	40	+50	−68	−57	−55	−58	−57	7	6
MHW3222	22	40	+50	−65	−57	−55	−55	−54	6.5	5
MHW3272A	27	40	+46	−74	—	−64	—	−63	6	5.5
MHW3342	34	40	+50	−68	−57	−55	−57	−55	5.5	4.5
MHW3382A	38	40	+46	−70	—	−61	—	−59	5.5	4.5

HYBRIDS UP TO 60 CHANNELS AND 450 MHz (Case 714-03)

Device	Hybrid Gain (Nominal) dB	Channel Loading Capacity	Maximum Distortion Specifications						Noise Figure @ 450 MHz dB	
			Output Level dBmV	2nd Order Test (2) dB	Composite Triple Beat dB		Cross Modulation dB			
					53 CH	60 CH	53 CH	60 CH	Max	Typ
MHW5122	12	60	+46	−70	−61	−58	−62	−61	9	8
MHW5141A	14	60	+46	−72	−61	−58	−61	−59	7	—
MHW5142	14	60	+46	−70	−62	−59	−62	−61	8	7
MHW5142A	14	60	+46	−74	−63	−61	−63	−62	8	—
MHW5171	17	60	+46	−70	−58	−55	−58	−57	6.5	5.5
MHW5171A	17	60	+46	−72	−61	−58	−60	−59	6.5	—
MHW5172	17	60	+46	−70	−61	−58	−61	−60	7	6
MHW5172A	17	60	+46	−74	−63	−61	−63	−62	7	—
MHW5181	18	60	+46	−72	−58	−55	−59	−58	6.5	5.5
MHW5181A	18	60	+46	−72	−61	−58	−59	−58	6	—
MHW5182	18	60	+46	−72	−62	−59	−62	−61	7	6
MHW5182A	18	60	+46	−74	−63	−61	−62	−61	7	—
MHW5222	22	60	+46	−68	−57	—	−54	—	7	6
MHW5222A	22	60	+46	−72	−62	−60	−60	−59	6.5	—
MHW5272A	27	60	+46	−72	−62	−60	−61	−60	6.5	—
MHW5342	34	60	+46	−70	−61	−58	−61	−59	6	5
MHW5342A	34	60	+46	−72	−61	−59	−61	−59	5.5	—
MHW5382	38	60	+46	−68	−60	−57	−60	−58	6	5
MHW5382A	38	60	+46	−70	−60	−58	−60	−58	5.5	—

(1) Channels (2 and 13) @ R
(2) Channels (2 and M13) @ M22

HYBRIDS UP TO 77 CHANNELS AND 550 MHz (Case 714-03)

Device	Hybrid Gain (Nominal) dB	Channel Loading Capacity	Maximum Distortion Specifications				Noise Figure @ 550 MHz dB
			Output Level dBmV	2nd Order Test (1) dB	Composite Triple Beat dB	Cross Modulation dB	
					77 CH	77 CH	Typ
MHW6141	14	77	+44	−70	−56	−59	7.5
MHW6142	14	77	+44	−72	−59	−62	8.5
MHW6171	17	77	+44	−68	−56	−59	6
MHW6172	17	77	+44	−70	−59	−62	6.5
MHW6181	18	77	+44	−70	−56	−59	7
MHW6182	18	77	+44	−72	−59	−62	8
MHW6222	22	77	+44	−64	−57	−57	7
MHW6342	34	77	+44	−68	−57	−59	6.5

REVERSE AMPLIFIER HYBRIDS (Case 714-03)

Device	Hybrid Gain (Nominal) dB	Channel Loading Capacity	Maximum Distortion Specifications						Noise Figure @ 175 MHz dB	
			Output Level dBmV	2nd Order Test dB (4)	Composite Triple Beat dB		Cross Modulation dB			
					22 CH	26 CH	12 CH	22 CH	Max	Typ
MHW1134	13	22	+50	−72	−73	−71 (2)	−70	−65	7	—
MHW1184	18	22	+50	−72	−72	−70 (2)	−68	−64	5.5	—
MHW1224	22	22	+50	−72	−71	−68 (2)	−67	−62	5	—
MHW1244	24	22	+50	−70	−70	−68 (2)	−66	−61	5	—

450/550 MHz POWER DOUBLING HYBRIDS (Case 714-03)

Device	Hybrid Gain (Nominal) dB	Channel Loading Capacity	Maximum Distortion Specifications						Noise Figure @ 450/550 MHz dB	
			Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB		Cross Modulation dB			
					60 CH	77 CH	60 CH	77 CH	Max	Typ
MHW5185	18	60	+46	−74 (3)	−65	—	−66	—	7	—
MHW6185	18	77	+46	−67 (1)	—	−60	—	−60	8	—

450 MHz FEEDFORWARD HYBRIDS (Case 714-03)

Device	Hybrid Gain (Nominal) dB	Channel Loading Capacity	Maximum Distortion Specifications				Noise Figure @ 450 MHz dB	
			Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB	Cross Modulation dB		
					60 CH	60 CH	Max	Typ
MHW4524F	24	60	+46	−84 (3)	−80	−75	8.5	8

(1) Channels (2 and M30) @ M39
(2) Typical
(3) Channels (2 and M13) @ M22
(4) Channels (2 and A) @ 7

General-Purpose Wideband Hybrid Amplifiers

50 Ω–100 Ω WIDEBAND AMPLIFIERS (Case 714-03)

The general purpose hybrid amplifiers listed are for broadband system applications requiring superior gain and current stability with temperature. The 50 to 100 ohm input and output impedances help simplify designs.

Device	Frequency Range MHz	Gain dB Min/Typ	Supply Voltage Vdc	Output Level 1 dB Compresson mW/f (MHz)	Noise Figure @ 250 MHz dB
MHW591	1–250	34.5/36.5	13.6	700/100	5
MHW593	10–400	33/34.5	13.6	600/200	5
MHW590	10–400	31.5/34	24	800/200	5
MHW592	1–250	33.5/35	24	900/100	5

50 Ω TO-39 (Case 31A-01)

The MWA Series features excellent gain versus frequency flatness, temperature stability and are cascadable for high gain lineups. Construction techniques include thin film gold metal circuitry and hermetic TO-39 package. MWA devices processed similarly to MIL-S-883, Method 5004.4, Class B, are available to special order.

Device	Frequency Range MHz	Gain dB Min/Typ	Supply Voltage Vdc	Output Level 1 dB Compresson dBm	Noise Figure @ 250 MHz dB
MWA110	0.1–400	13/14	2.9	−2.5	4
MWA120	0.1–400	13/14	5	+8.2	5.5
MWA130	0.1–400	13/14	5.5	+18	7
MWA210	0.1–600	9/10	1.75	+1.5	6
MWA220	0.1–600	9/10	3.2	+10.5	6.5
MWA230	0.1–600	9/10	4.4	+18.5	7.5
MWA310	0.1–1000	7/8	1.6	+3.5	6.5
MWA320	0.1–1000	7/8	2.9	+11.5	6.7
MWA330	0.1–1000	—/6.2	4	+15.2	9

50 Ω–75 Ω WIDEBAND AMPLIFIERS (Case 790-01)

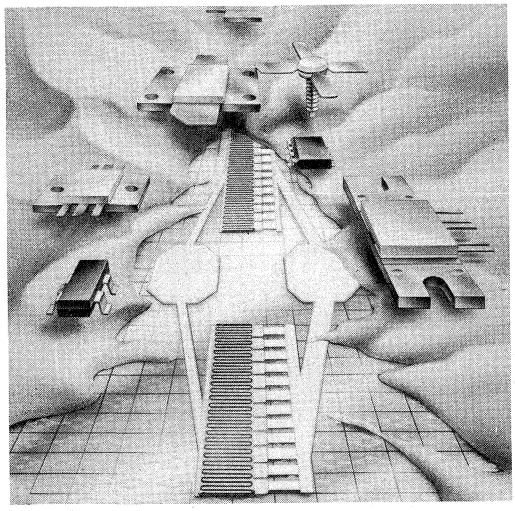
The Case 790-01 amplifiers feature high gain with low noise, low input and output VSWR and excellent gain flatness to 1 GHz. Three amplifier stages are constructed using SOT-23 packaged devices mounted on thick film circuit substrates.

Device	Frequency Range MHz	Gain dB Min/Typ	Supply Voltage Vdc	Output Level 1 dB Compresson dBm	Noise Figure @ 250 MHz dB
MWA5157	30–890	22/24	10–14	+6	5
MWA5121	30–890	25/27	18–22	+6	4

50 Ω Monolithic Microwave Integrated Circuits

These monolithic amplifiers are fully cascadable and usable to frequencies over 3 GHz. External blocking capacitors are required along with an external bias resistor. Hermetic versions are available to special order in Case 303-01.

Device	Frequency Range MHz	Gain dB Typ @ 1 GHz	Supply Voltage Vdc	Output Level 1 dB Compresson dBm Typ	Noise Figure @ 1500 MHz db
(Case 317-01)					
MWA0204	30-4000	11	7-15	7	6
(Case 318A-02)					
MWA0211	30-4000	11	7-15	7	6



Transistors 3

2N2857

The RF Line

NPN SILICON
RF SMALL-SIGNAL
TRANSISTORS

NPN SILICON RF SMALL-SIGNAL TRANSISTORS

. . . designed primarily for use in high-gain, low-noise amplifier, oscillator, and mixer applications. Can also be used in UHF converter applications.

- High Current-Gain—Bandwidth Product — f_T = 1.6 GHz (Typ) @ I_C = 8.0 mAdc
- Low Collector-Base Time Constant — $r_b'C_c$ = 15 ps (Max) @ I_E = 2.0 mAdc
- Characterized with Scattering Parameters
- Ideal for Micro-Power Applications

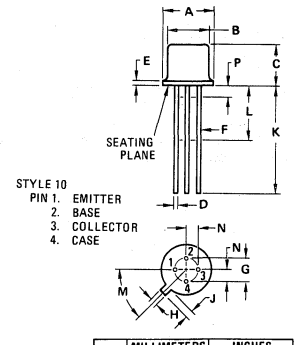


3

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CB}	30	Vdc
Emitter-Base Voltage	V_{EB}	2.5	Vdc
Collector Current — Continuous	I_C	40	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	200 1.14	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 1.72	mW mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

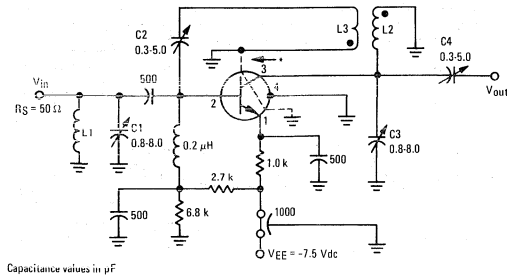
CASE 20-03
TO-72

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage** (I_C = 3.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	15	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 1.0 μAdc, I_E = 0)	$V_{(BR)CBO}$	30	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	$V_{(BR)EBO}$	2.5	–	–	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	0.01	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 3.0 mAdc, V_{CE} = 1.0 Vdc)	h_{FE}	30	–	150	–
DYNAMIC CHARACTERISTICS					
Current-Gain–Bandwidth Product ① (I_C = 5.0 mAdc, V_{CE} = 6.0 Vdc, f = 100 MHz)	f_T	1000	–	1900	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 to 1.0 MHz)	C_{cb}	–	0.7	1.0	pF
Small-Signal Current Gain (I_C = 2.0 mAdc, V_{CE} = 6.0 Vdc, f = 1.0 kHz)	h_{fe}	50	–	220	–
Collector-Base Time Constant (I_E = 2.0 mAdc, V_{CB} = 6.0 Vdc, f = 31.9 MHz)	$r_b'C_c$	4.0	–	15	ps
Noise Figure (Figure 1)	NF				dB
(I_E = 0.1 mAdc, V_{CE} = 1.0 Vdc, R_S = 50 ohms, f = 450 MHz) ②		–	5.8	–	
(I_C = 1.5 mAdc, V_{CE} = 6.0 Vdc, R_S = 50 ohms, f = 450 MHz)		–	4.1	4.5	
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (Figure 1)	G_{pe}				dB
(I_E = 0.1 mAdc, V_{CE} = 1.0 Vdc, f = 450 MHz) ②		–	11	–	
(I_C = 1.5 mAdc, V_{CE} = 6.0 Vdc, f = 450 MHz)		12.5	–	19	
Power Output (Figure 2) (I_E = 12 mAdc, V_{CB} = 10 Vdc, f = 500 MHz)	P_{out}	30	–	–	mW

*Indicates JEDEC Registered Data.
**Motorola guarantees this data in addition to JEDEC Registered Data.
① f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.
② Micro-Power Specifications.

FIGURE 1 – TEST CIRCUIT FOR NOISE FIGURE AND POWER GAIN



L1, L2 – Silver-plated brass rod, 1-1/2" long and 1/4" dia. Install at least 1/2" from nearest vertical chassis surface.

L3 – 1/2 turn #16 AWG wire, located 1/4" from and parallel to L2.

* – External interlead shield to isolate collector lead from emitter and base leads.

Neutralization Procedure:

(A) Connect 450-MHz signal generator (with R_S = 50 ohms) to input terminals of amplifier.

(B) Connect 50-ohm RF voltmeter across output terminals of amplifier.

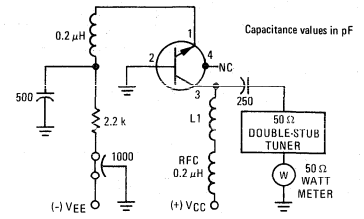
(C) Apply V_{EE}, and with signal generator adjusted for 5 mV output from amplifier, tune C1, C3, and C4 for maximum output.

(D) Interchange connections to signal generator and RF voltmeter.

(E) With sufficient signal applied to output terminals of amplifier, adjust C2 for minimum indication at input.

(F) Repeat steps (A), (B), and (C) to determine if retuning is necessary.

FIGURE 2 – TEST CIRCUIT FOR OSCILLATOR POWER OUTPUT



L1 – 3 turns #16 AWG wire, 3/8" O.D. 1-1/4" long.

FIGURE 3 – NOISE FIGURE *versus* FREQUENCY

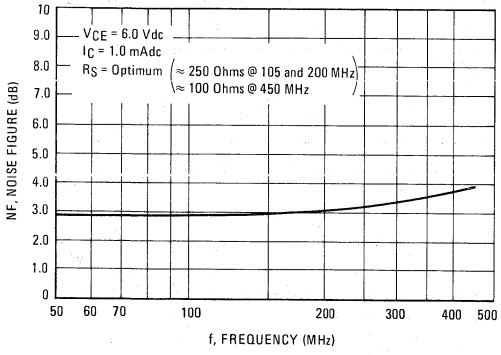


FIGURE 4 – NOISE FIGURE *versus* SOURCE RESISTANCE AND COLLECTOR CURRENT

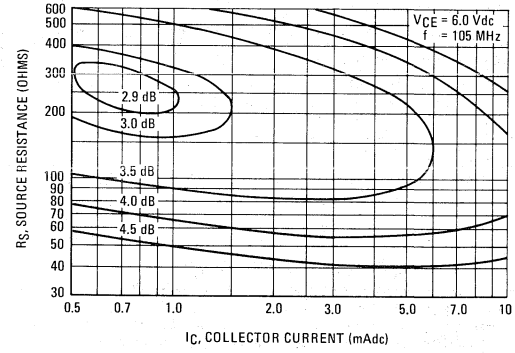


FIGURE 5 – NOISE FIGURE *versus* SOURCE RESISTANCE AND COLLECTOR CURRENT

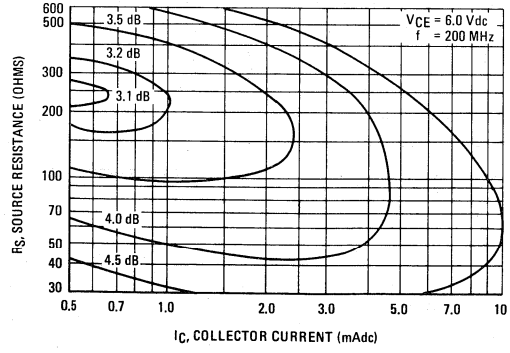


FIGURE 6 – CURRENT-GAIN–BANDWIDTH PRODUCT

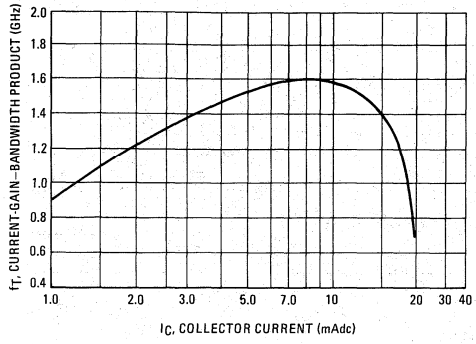


FIGURE 7 – NOISE FIGURE AND POWER GAIN versus COLLECTOR CURRENT

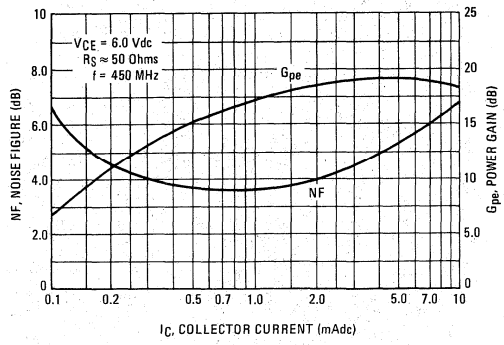


FIGURE 8 – INPUT ADMITTANCE versus FREQUENCY

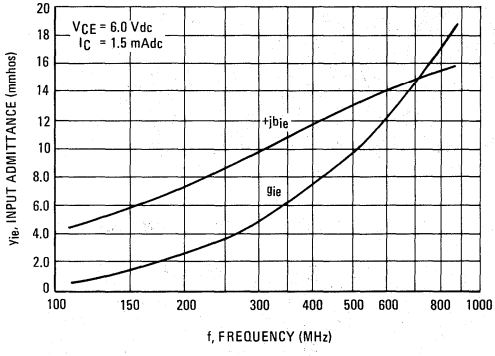


FIGURE 9 – OUTPUT ADMITTANCE versus FREQUENCY

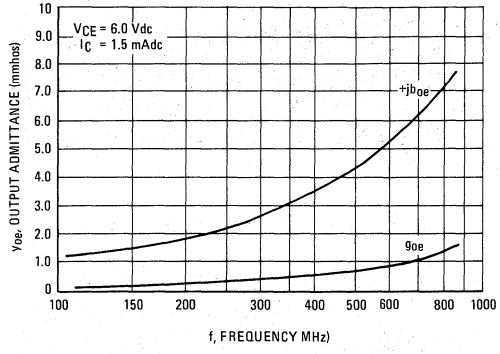


FIGURE 10 – FORWARD TRANSFER ADMITTANCE versus FREQUENCY

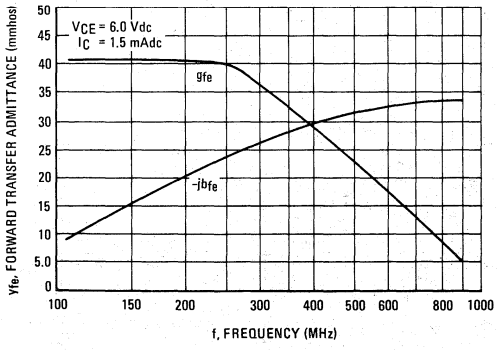
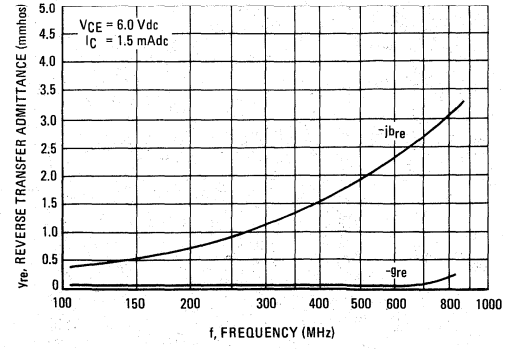


FIGURE 11 –REVERSE TRANSFER ADMITTANCE versus FREQUENCY



3

FIGURE 12 – S_{11}, INPUT REFLECTION COEFFICIENT

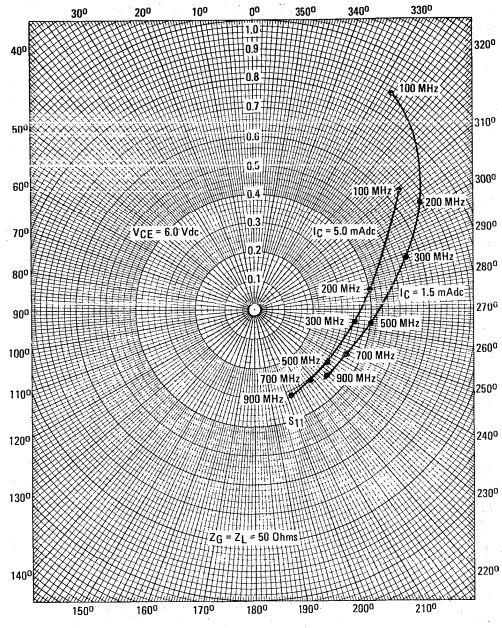


FIGURE 13 – S_{22}, OUTPUT REFLECTION COEFFICIENT

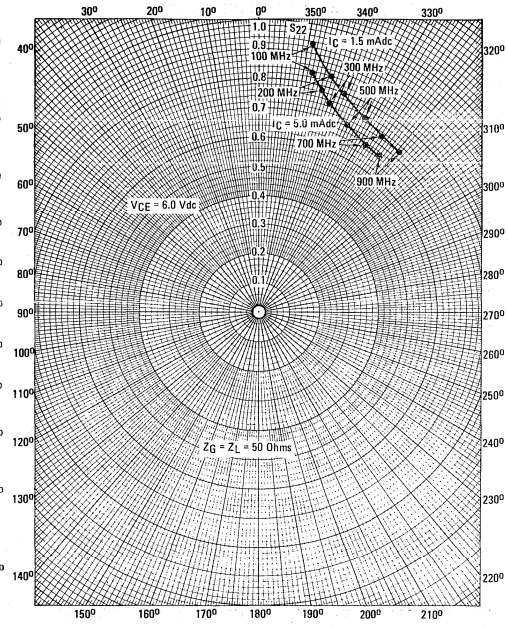


FIGURE 14 – S_{12}, REVERSE TRANSMISSION COEFFICIENT

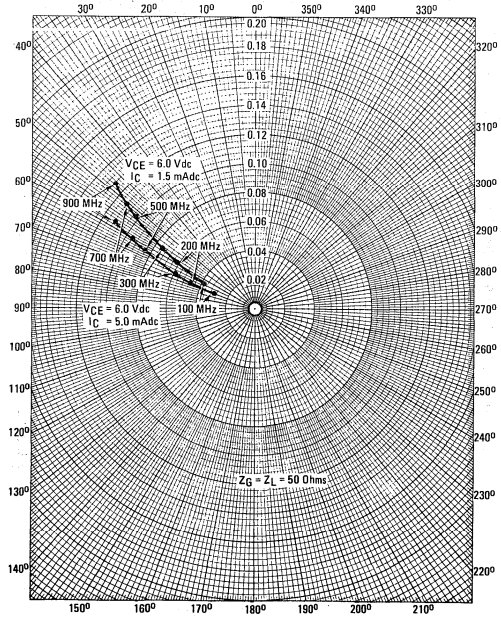


FIGURE 15 – S_{21}, FORWARD TRANSMISSION COEFFICIENT

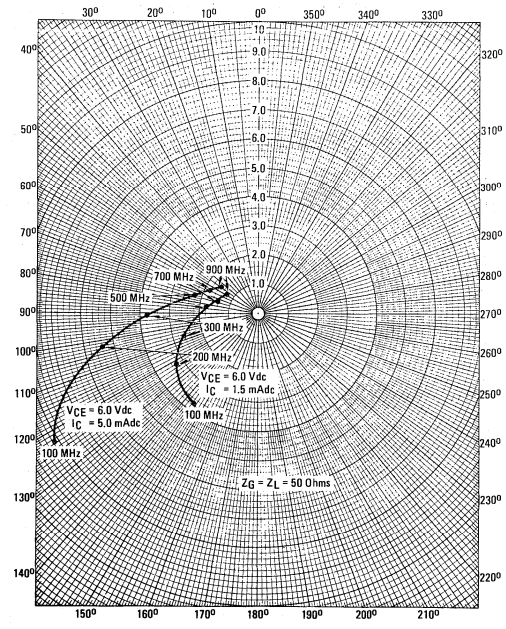
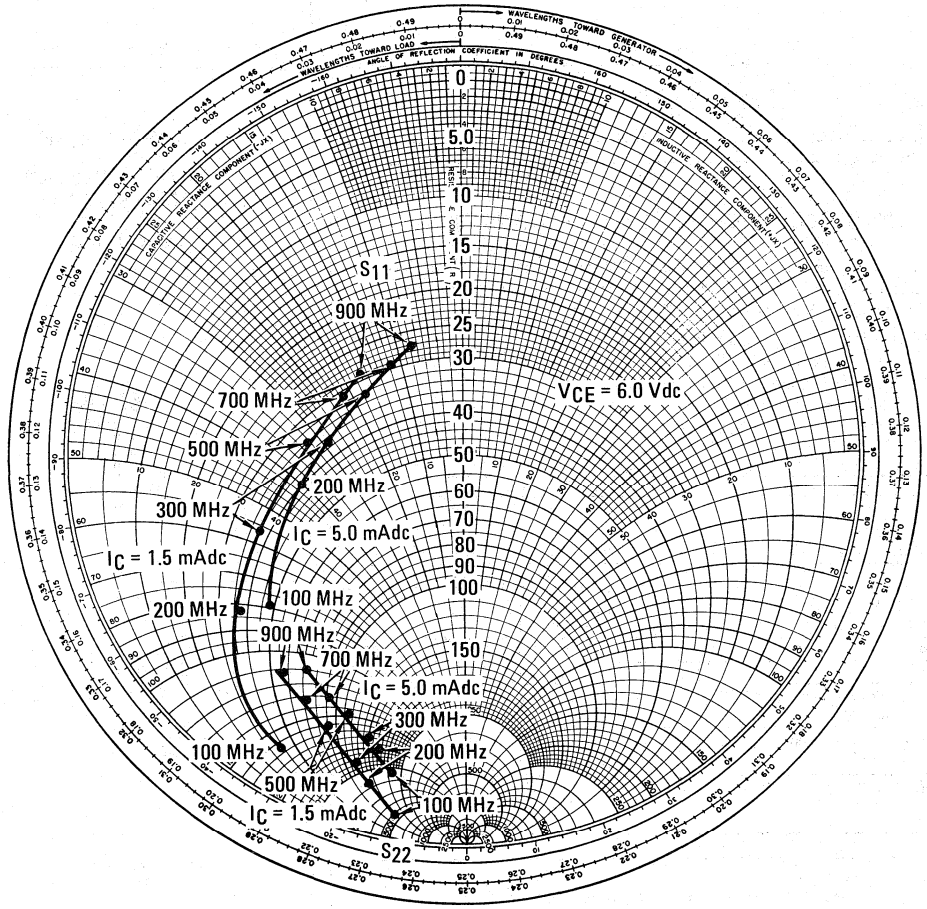


FIGURE 16 – S_{11}, INPUT REFLECTION COEFFICIENT AND S_{22}, OUTPUT REFLECTION COEFFICIENT



2N3553

The RF Line

2.5 W – 175 MHz

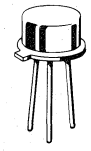
HIGH FREQUENCY TRANSISTOR

NPN SILICON

NPN SILICON HIGH-FREQUENCY TRANSISTOR

. . . designed for amplifier and oscillator applications in military and industrial equipment. Suitable for use as output, driver or pre-driver stages in VHF equipment.

- Specified 175 MHz, 28 Vdc Characteristics –
  Output Power = 2.5 Watts
  Minimum Gain = 10 dB
  Efficiency = 50%



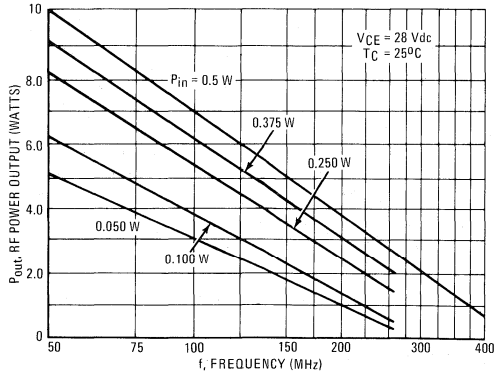
3

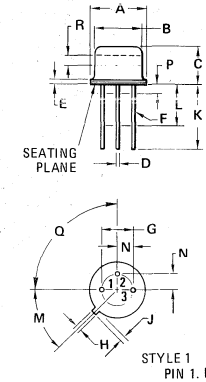
***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	65	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	1.0	Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	7.0 40	Watts $mW/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	^oC

*Indicates JEDEC Registered Data.

FIGURE 1 – OUTPUT POWER versus FREQUENCY





STYLE 1
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO-39

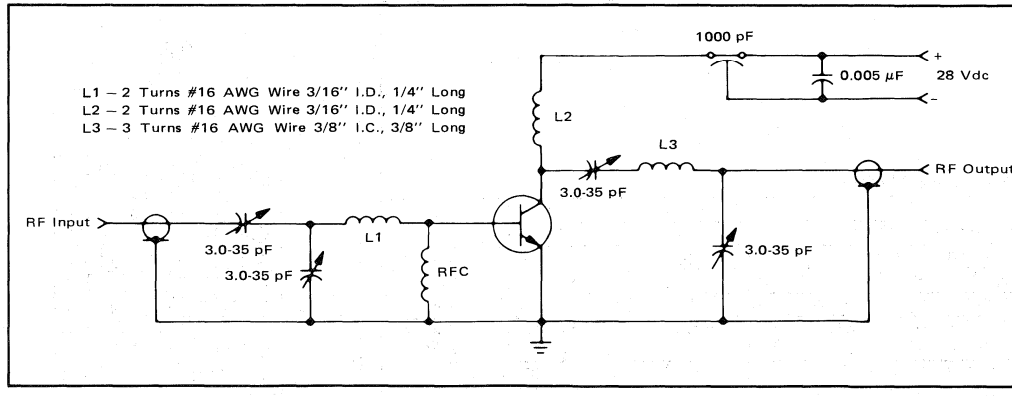
***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{(BR)CEO(sus)}$	40	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	–	–	0.1	mAdc
Collector Cutoff Current (V_{CE} = 30 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 200°C) (V_{CE} = 65 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	– –	– –	5.0 1.0	mAdc
Emitter Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	–	0.1	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	–	–	–
Collector-Emitter Saturation Voltage (I_C = 250 mAdc, I_B = 50 mAdc)	$V_{CE(sat)}$	–	–	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain–Bandwidth Product (I_C = 100 mAdc, V_{CE} = 28 Vdc, f = 100 MHz)	f_T	–	500	–	MHz
Output Capacitance (V_{CB} = 30 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	–	8.0	10	pF
FUNCTIONAL TESTS					
Power Input (V_{CE} = 28 Vdc, P_{out} = 2.5 Watts, f = 175 MHz)	P_{in}	–	–	0.25	Watt
Common-Emitter Amplifier Power Gain (V_{CE} = 28 Vdc, P_{out} = 2.5 Watts, f = 175 MHz)	G_{pe}	10	–	–	dB
Collector Efficiency (V_{CE} = 28 Vdc, P_{out} = 2.5 Watts, f = 175 MHz)	η	50	–	–	%

*Indicates JEDEC Registered Data

(1) Pulsed thru a 25 mH inductor.

FIGURE 2 – 175 MHz TEST CIRCUIT SCHEMATIC



2N3866
2N3866A

The RF Line

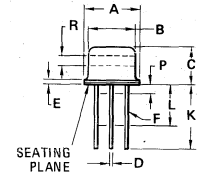
1.0 W — 400 MHz
HIGH FREQUENCY TRANSISTOR
NPN SILICON

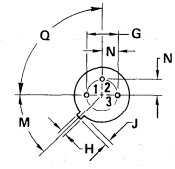
NPN SILICON HIGH FREQUENCY TRANSISTOR

. . . designed for amplifier and oscillator applications in military and industrial equipment. Suitable for use as output, driver or pre-driver stages in VHF and UHF equipment.

- Specified 400 MHz, 28 Vdc Characteristics —
  Output Power = 1.0 Watt
  Minimum Gain = 10 dB
  Efficiency = 45%
- Large Signal Series Equivalent Impedances
- S-Parameter Characterization







DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	—	0.500	—
L	6.35	—	0.250	—
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
Q	90° NOM		90° NOM	
R	2.54	—	0.100	—

All JEDEC dimensions and notes apply.

STYLE 1
PIN 1. EMITTER
2. BASE
3. COLLECTOR

CASE 79-02
TO-39

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	55	Vdc
Emitter-Base Voltage	V_{EBO}	3.5	Vdc
Collector Current — Continuous	I_C	0.4	Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate Above 25^oC	P_D	5.0 28.6	Watts $mW/^oC$
Storage Temperature Range	T_{stg}	-65 to +200	^oC

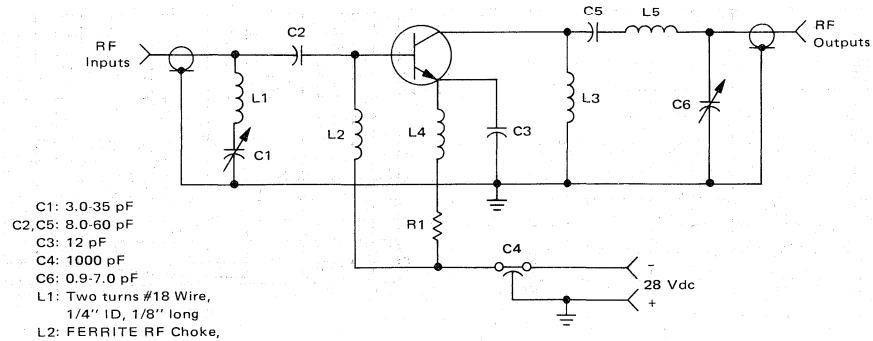
*Indicates JEDEC Registered Data

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted).

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 5.0 mAdc, I_B = 0)		$V_{CEO(sus)}$	30	—	Vdc
Collector-Base Sustaining Voltage (I_C = 5.0 mAdc, R_{BE} = 10 Ω)		$V_{CER(sus)}$	55	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		$V_{(BR)EBO}$	3.5	—	Vdc
Collector Cutoff Current (V_{CE} = 28 Vdc, I_B = 0)		I_{CEO}	—	0.02	mAdc
Emitter Cutoff Current (V_{BE} = 3.5 Vdc, I_C = 0)		I_{EBO}	—	0.1	mAdc
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 30 Vdc, V_{BE} = −1.5 Vdc (Rev.), T_C = 200°C)			—	5.0	
(V_{CE} = 55 Vdc, V_{BE} = −1.5 Vdc (Rev.)			—	0.1	
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			—
(I_C = 360 mAdc, V_{CE} = 5.0 Vdc)	Both		5.0	—	
(I_C = 50 mAdc, V_{CE} = 5.0 Vdc)	2N3866		10	200	
	2N3866A		25	200	
Collector-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 20 mAdc)		$V_{CE(sat)}$	—	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product		f_T			MHz
(I_C = 50 mAdc, V_{CE} = 15 Vdc, f = 200 MHz)	2N3866		500	—	
	2N3866A		800	—	
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	—	3.0	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 1.0 W, f = 400 MHz)		G_{PE}	10	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 1.0 W, f = 400 MHz)		η	45	—	%

*Indicates JEDEC Registered Data.

FIGURE 1 – 400 MHz TEST CIRCUIT SCHEMATIC



C1: 3.0-35 pF
C2,C5: 8.0-60 pF
C3: 12 pF
C4: 1000 pF
C6: 0.9-7.0 pF
L1: Two turns #18 Wire, 1/4" ID, 1/8" long
L2: FERRITE RF Choke, One Turn, z = 450 Ohms
L3,L4: RF Choke, 0.1 μH
L5: 2-3/4 Turns, #18 Wire, 1/4" ID, 3/16" long
R1: 5.6 Ohms

FIGURE 2 – POWER OUTPUT versus FREQUENCY (Class C)

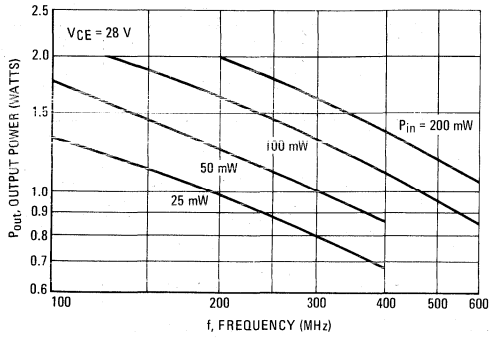


FIGURE 3 – CURRENT-GAIN – BANDWIDTH PRODUCT

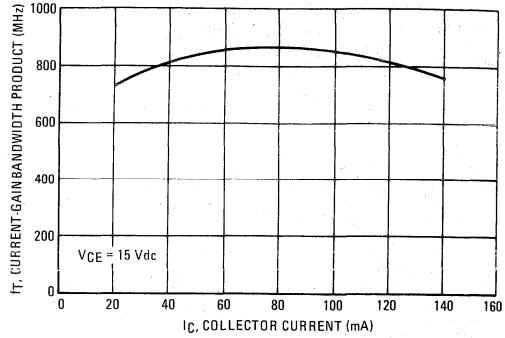


FIGURE 4 – COLLECTOR-BASE TIME CONSTANT

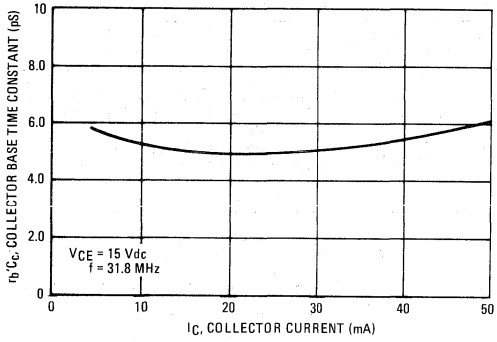


FIGURE 5 – OUTPUT CAPACITANCE

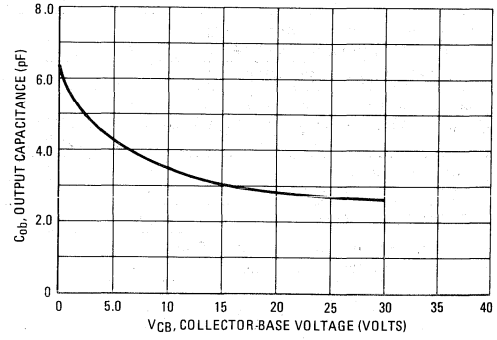


FIGURE 6 – OUTPUT POWER versus INPUT POWER (CLASS C)

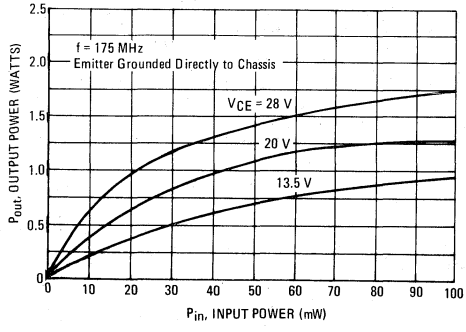


FIGURE 7 – SMALL-SIGNAL CURRENT GAIN

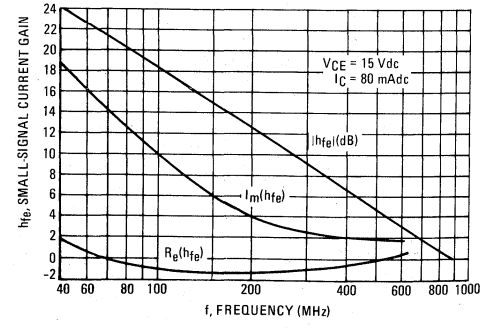


FIGURE 8 – LARGE-SIGNAL SERIES EQUIVALENT IMPEDANCES

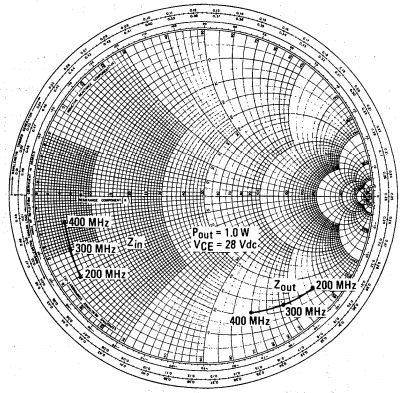


FIGURE 9 – S_{11} AND S_{22} versus FREQUENCY

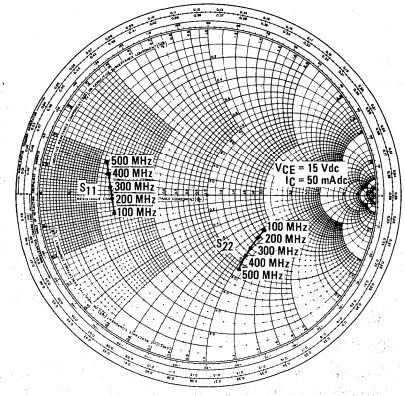


FIGURE 10 – S_{21} versus FREQUENCY

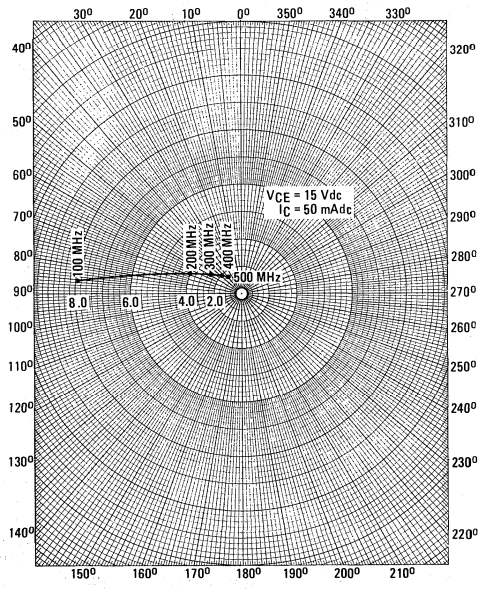
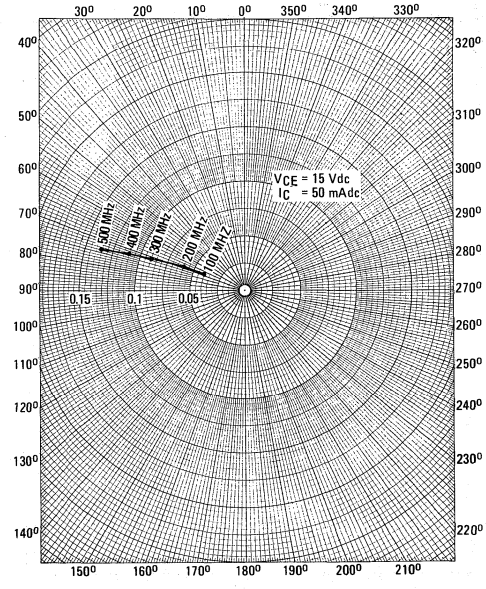


FIGURE 11 – S_{12} versus FREQUENCY



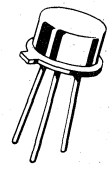
2N3924

NPN SILICON RF POWER TRANSISTORS

. . . optimized Annular* transistor for large-signal power-amplifier and driver applications to 300 MHz.

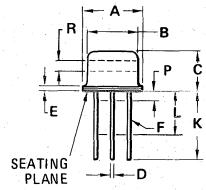
- Designed for 13.6-volt Operation
- Wide choice of min Power Outputs @ 175 MHz
  4 watts — 2N3924
- Multiple-Emitter Construction for Excellent High-Frequency Performance
- Guaranteed Safe Operating Area
  $V_{(BR)CEO(sus)}$ Measured at I_C = 200 mAdc

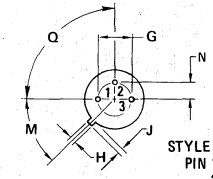
NPN SILICON RF POWER TRANSISTORS



2N3924
(TO-39)

Case 79





STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO-205AD

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

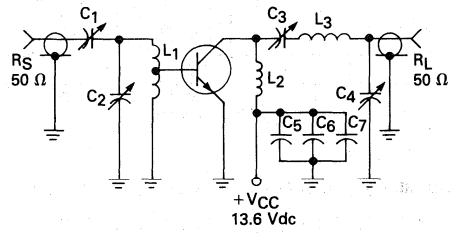
Rating	Symbol	2N3924	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CB}	36	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	0.5	Adc
Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	7.0 40	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Figure 2) (I_C = 200 mAdc)		$V_{(BR)CEO(sus)}$*	18	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 0.25 mAdc, I_E = 0)		$V_{(BR)CBO}$	36	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)		$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0) (V_{CB} = 15 Vdc, I_E = 0, T_A = 150°C)		I_{CBO}	— —	— —	0.1 5.0	mAdc
DYNAMIC CHARACTERISTICS						
Current-Gain — Bandwidth Product (I_C = 100 mAdc, V_{CE} = 13.6 Vdc, f = 100 MHz		f_T	—	350	—	MHz
Output Capacitance (V_{CB} = 13.6 Vdc, I_E = 0, f = 100 kHz		C_{ob}	—	12.5	20	pF
FUNCTIONAL TESTS						
Power Input	Test Circuit Figure 1	P_{in}	—	—	1.0	Watt
Common-Emitter Amplifier Power Gain	V_{CE} = 13.6 Vdc, R_S = 50 ohms, R_L = 50 ohms, f = 175 MHz	G_{pe}	6.0	7.3	—	dB
Collector Efficiency	P_{out} = 4.0 Watts	η	70	—	—	%

3

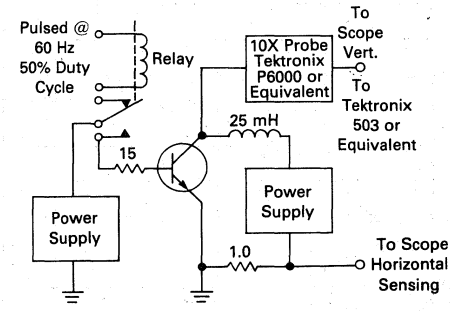
FIGURE 1 — 175 MHz TEST CIRCUIT



C_1, C_2, C_4 ..... 5–50 pF (Air variable)
C_3 .....7–100 pF (Air variable)
C_5 .....470 pF (Disc ceramic)
C_6 .....0.01 μF (Disc ceramic)
C_7 .....0.001 μF (Disc ceramic)

L_1 — 1½ turns #14 AWG tinned wire; ⅜" ID Air wound; winding length 3/16"; base tapped 1 turn from ground
L_2 — RFC
L_3 — 2 turns #14 AWG tinned wire; ¼" ID Air wound; winding length 3/16"

FIGURE 2 — PULSE TEST CIRCUIT



CLASS C DESIGN DATA FOR V_{CE} = 13.6 Vdc, T_C = 25°C

(Emitter Grounded Directly to the Chassis — No Tuned-Emitter Techniques Used)

FIGURE 3 — POWER OUTPUT versus FREQUENCY

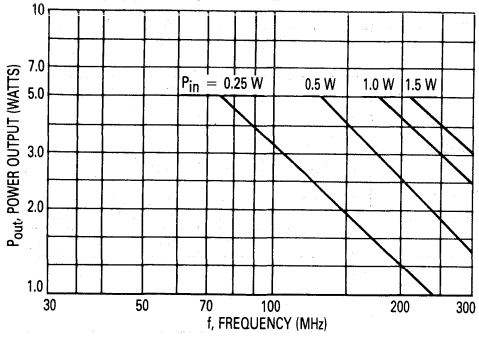


FIGURE 4 — POWER OUTPUT versus POWER INPUT

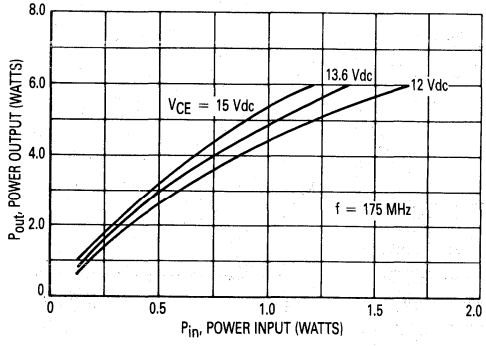


FIGURE 5 — PARALLEL EQUIVALENT INPUT RESISTANCE

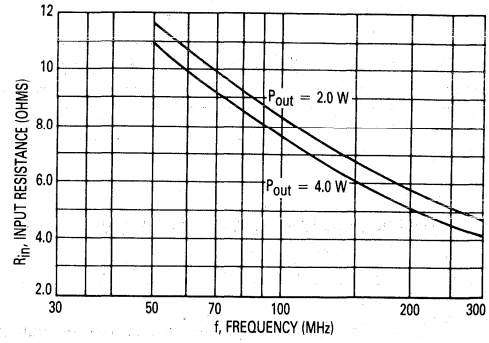


FIGURE 6 — PARALLEL EQUIVALENT INPUT CAPACITANCE

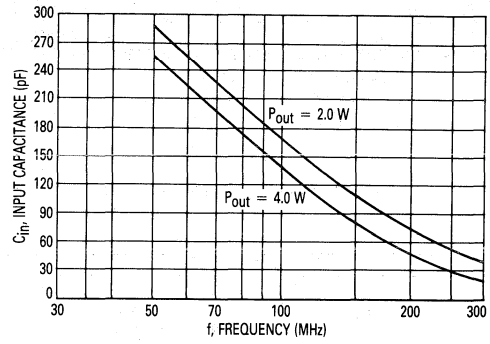
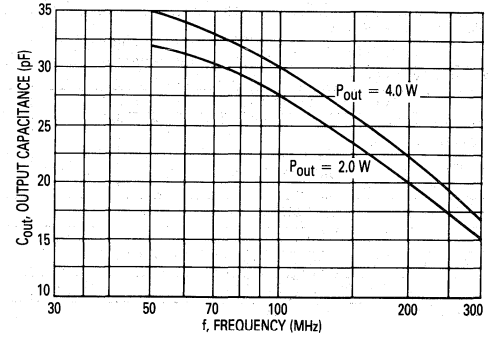


FIGURE 7 — PARALLEL EQUIVALENT OUTPUT CAPACITANCE



2N3948

The RF Line

1.0 W — 400 MHz

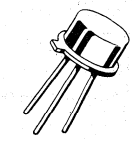
HIGH FREQUENCY TRANSISTOR

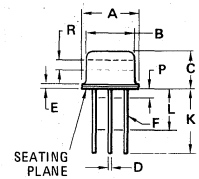
NPN SILICON

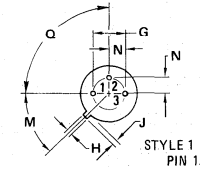
NPN SILICON HIGH-FREQUENCY TRANSISTOR

. . . designed for amplifier applications in industrial and commercial equipment. Suitable for use as output, driver or pre-driver stages in UHF equipment.

- Specified 400 MHz, 13.6 Vdc Characteristics —
  Output Power = 1.0 Watt
  Minimum Gain = 6.0 dB
  Efficiency = 45%







STYLE 1
PIN 1. EMITTER
2. BASE
3. COLLECTOR

***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CB}	36	Vdc
Emitter-Base Voltage	V_{EB}	3.5	Vdc
Collector Current — Continuous	I_C	400	mAdc
Total Device Dissipation @ $T_A = 25^oC$ Derate above 25^oC	P_D	1.0 5.71	Watt mW/^oC
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	35	$^oC/W$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	175	$^oC/W$

*Indicates JEDEC Registered Data

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	—	0.500	—
L	6.35	—	0.250	—
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
Q	90° NOM		90° NOM	
R	2.54	—	0.100	—

All JEDEC dimensions and notes apply.

CASE 79-02
TO-39

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{CEO(sus)}$	20	–	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	36	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	–	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0) (V_{CB} = 15 Vdc, I_E = 0, T_A = 150°C)	I_{CBO}	– –	0.1 100	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	15	–	–
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product (I_E = 50 mAdc, V_{CE} = 15 Vdc, f = 200 MHz)	f_T	700	–	MHz
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	4.5	pF
FUNCTIONAL TEST				
Power Gain	(V_{CC} = 13.6 Vdc, f = 400 MHz, P_{in} = 0.25 W)	G_{pe}	6.0	–	dB
Output Power		P_{out}	1.0	–	Watt
Collector Efficiency		η	45	–	%

*Indicates JEDEC Registered Data

FIGURE 1 – 400 MHz RF AMPLIFIER TEST CIRCUIT

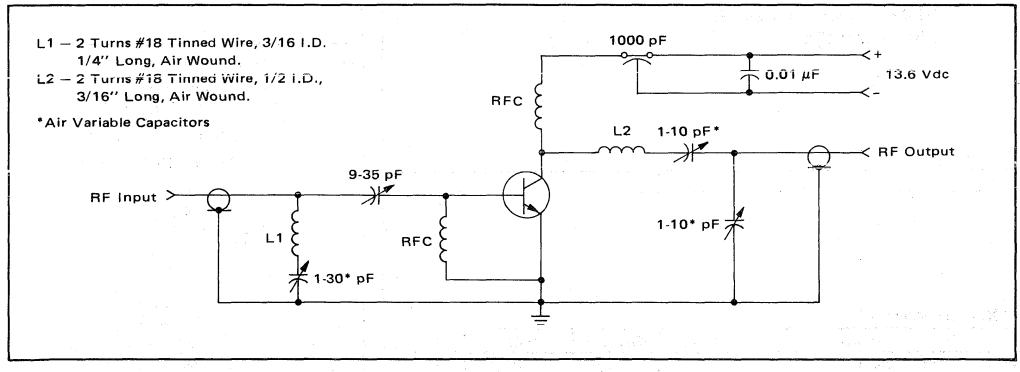


FIGURE 2 – OUTPUT POWER versus FREQUENCY

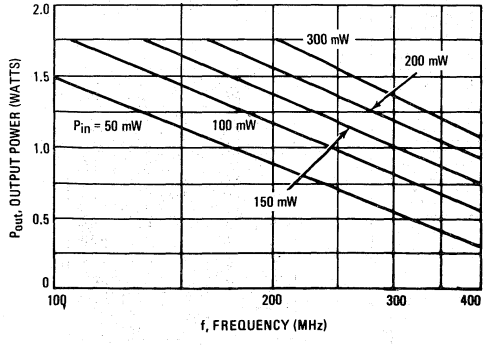
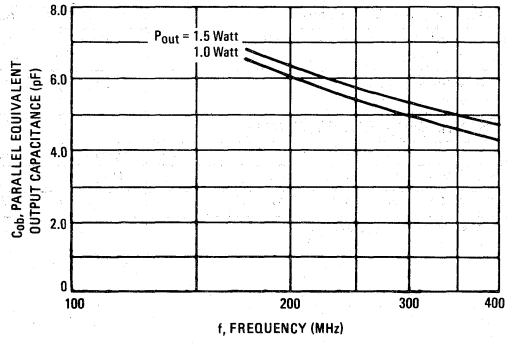


FIGURE 3 – PARALLEL EQUIVALENT OUTPUT CAPACITANCE



2N3959
2N3960

The RF Line

NPN SILICON HIGH-FREQUENCY TRANSISTORS

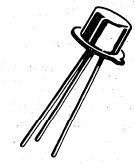
. . . designed for high-speed current-mode logic switching applications.

- High Current-Gain—Bandwidth Product — f_T = 1800 MHz (Typ) @ I_C = 10 mAdc
- Low Input and Output Capacitance — C_{ib} and C_{ob} = 2.5 pF (Max)
- Excellent Current-Mode Performance — t_r = 1.7 ns (Typ) @ I_C = 30 mAdc
- Low Collector-Base Time Constant — $r_b'C_c$ = 25 ps (Max) @ I_C = 10 mAdc — 2N3959

1.8 GHz — 10 mAdc

HIGH FREQUENCY TRANSISTORS

NPN SILICON



Current-Mode logic operation, because of the absence of storage time, offers improved high-speed performance for digital applications. In addition, the low impedance drive circuit offers improved delay, rise, and fall times.

The basic characteristics of importance in current-mode logic applications are Current-Gain—Bandwidth Product (f_T), Input and Output Capacitance (C_{ib} and C_{ob}), and Base Spreading Resistance (r'_b).

The 2N3959 and 2N3960 offer a combination of extremely high f_T values, low capacitances, and low base spreading resistance which results in exceptionally high speed in current-mode logic circuits.

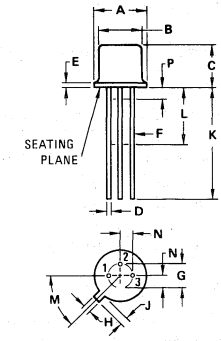
*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	12	Vdc
Collector-Base Voltage	V_{CB}	20	Vdc
Emitter-Base Voltage	V_{EB}	4.5	Vdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	400 2.3	mW mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	750 4.3	mW mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	0.436	°C/mW
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.233	°C/mW

*Indicates JEDEC Registered Data.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.406	0.533	0.016	0.021
E	–	0.762	–	0.030
F	0.406	0.483	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.914	1.17	0.036	0.046
J	0.711	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

All JEDEC notes and dimensions apply.

CASE 22-03
(TO-18)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Fig. No.	Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**							
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)		–	$V_{(BR)CEO}$	12	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)		–	$V_{(BR)CBO}$	20	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)		–	$V_{(BR)EBO}$	4.5	–	–	Vdc
Collector Reverse Current		–	I_{CEX}				μAdc
(V_{CE} = 10 Vdc, V_{EB} = 2.0 Vdc)				–	–	0.005	
(V_{CE} = 10 Vdc, V_{EB} = 2.0 Vdc, T_A = 150°C)				–	–	5.0	
Base Cutoff Current (V_{CE} = 10 Vdc, V_{EB} = 2.0 Vdc)		–	I_{BL}	–	–	0.005	μAdc
Collector Forward Current (V_{CE} = 5.0 Vdc, V_{BE} = 0.4 Vdc)		–	I_{CEX}	–	–	1.0	μAdc
***ON CHARACTERISTICS**							
DC Current Gain		1	h_{FE}				–
(I_C = 1.0 mAdc, V_{CE} = 1.0 Vdc)				25	–	–	
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)				40	–	400	
(I_C = 30 mAdc, V_{CE} = 1.0 Vdc)				25	–	–	
Collector-Emitter Saturation Voltage		–	$V_{CE(sat)}$				Vdc
(I_C = 1.0 mAdc, I_B = 0.1 mAdc)				–	–	0.2	
(I_C = 30 mAdc, I_B = 3.0 mAdc)				–	–	0.3	
Base-Emitter "on" Voltage		–	$V_{BE(on)}$				Vdc
(I_C = 1.0 mAdc, V_{CE} = 1.0 Vdc)				–	–	0.8	
(I_C = 30 mAdc, V_{CE} = 1.0 Vdc)				–	–	1.0	
***DYNAMIC CHARACTERISTICS**							
Current-Gain—Bandwidth Product		2	f_T				MHz
(I_C = 5.0 mAdc, V_{CE} = 4.0 Vdc, f = 100 MHz)	2N3959			1000	–	–	
	2N3960			1300	–	–	
(I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	2N3959			1300	–	–	
	2N3960			1600	–	–	
(I_C = 30 mAdc, V_{CE} = 4.0 Vdc, f = 100 MHz)	2N3959			1000	–	–	
	2N3960			1200	–	–	
Output Capacitance (V_{CB} = 4.0 Vdc, I_E = 0, f = 1.0 MHz)		4	C_{ob}	–	2.0	2.5	pF
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 100 MHz)		4	C_{ib}	–	1.5	2.5	pF
Collector-Base Time Constant		3	$r_b'C_c$				ps
(I_C = 5.0 mAdc, V_{CE} = 4.0 Vdc)	2N3959			–	–	30	
	2N3960			–	–	50	
(I_C = 10 mAdc, V_{CE} = 10 Vdc)	2N3959			–	–	25	
	2N3960			–	–	40	
(I_C = 30 mAdc, V_{CE} = 4.0 Vdc)	2N3959			–	–	30	
	2N3960			–	–	50	
SWITCHING CHARACTERISTICS (Figure 7)							
Turn-On Delay Time		–	$t_{d(on)}$				ns
(I_C = 10 mAdc, V_{out} = 1.0 Vdc)				–	2.4	–	
(I_C = 30 mAdc, V_{out} = 1.0 Vdc)				–	2.0	–	
Rise Time		–	t_r				ns
(I_C = 10 mAdc, V_{out} = 1.0 Vdc)	Both Devices			–	3.0	–	
(I_C = 30 mAdc, V_{out} = 1.0 Vdc)	2N3959			–	2.2	–	
	2N3960			–	1.7	–	
Turn-Off Delay Time		–	$t_{d(off)}$				ns
(I_C = 10 mAdc, V_{out} = 1.0 Vdc)				–	1.6	–	
(I_C = 30 mAdc, V_{out} = 1.0 Vdc)				–	1.6	–	
Fall Time		–	t_f				ns
(I_C = 10 mAdc, V_{out} = 1.0 Vdc)	Both Devices			–	3.3	–	
(I_C = 30 mAdc, V_{out} = 1.0 Vdc)	2N3959			–	2.3	–	
	2N3960			–	1.9	–	

*Indicates JEDEC Registered Data.

FIGURE 1 – TYPICAL DC CURRENT GAIN

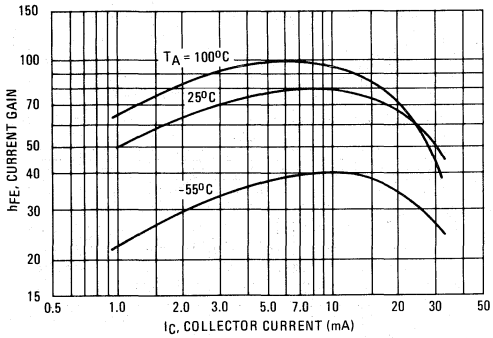


FIGURE 2 – TYPICAL CURRENT-GAIN – BANDWIDTH PRODUCT

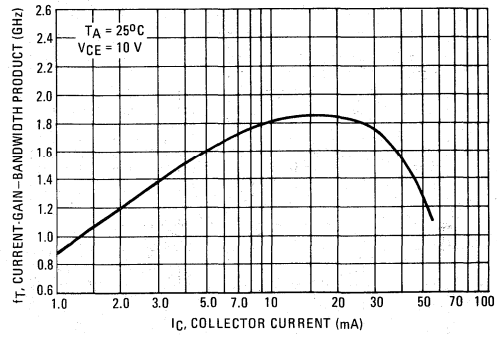


FIGURE 3 – TYPICAL COLLECTOR-BASE TIME CONSTANT

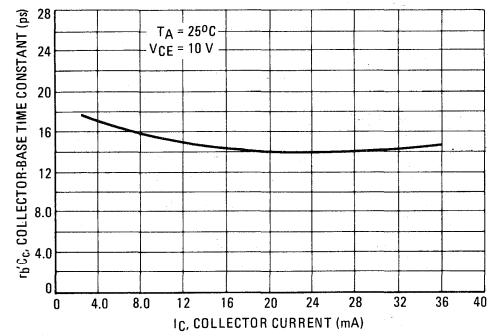
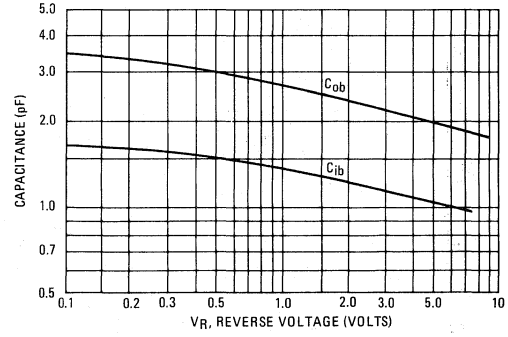


FIGURE 4 – TYPICAL JUNCTION CAPACITANCE



3

TURN-ON AND TURN-OFF TIMES

FIGURE 5 – V_{out} = 1.0 Vdc

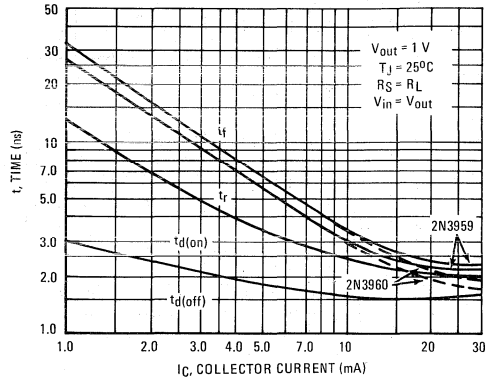


FIGURE 6 – V_{out} = 2.0 Vdc

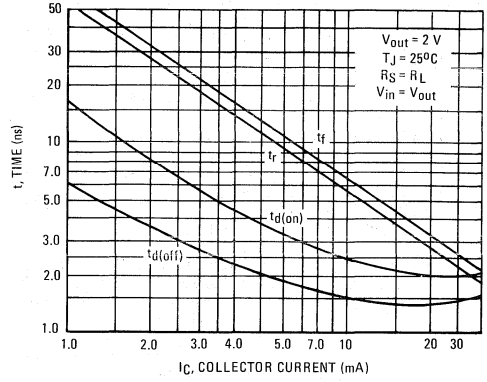
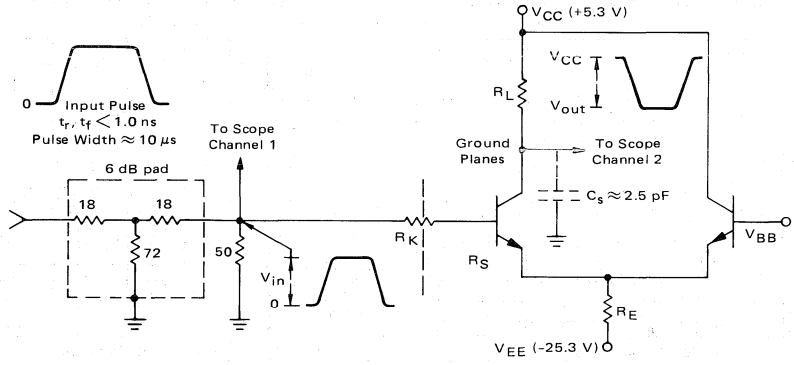


FIGURE 7 – SWITCHING TIMES TEST CIRCUIT



This test set up is designed to simulate a cascade of identical stages. ∴The source resistance (R_S) equals the load resistance (R_L). Values used in the test are shown in the table.

For $V_{in} = V_{out}$ = 1 V, V_{BB} = +0.5 V, R_L & R_K values appropriately reduced.

$V_{in} = V_{out}$ = 2 volts, V_{BB} = +1.0V			
I_C (mA)	R_E (kΩ)	R_L (Ω)	R_K (Ω)
1.0	24.0	2.0 k	2.0 k
3.0	8.2	680	680
10	2.4	200	180
30	0.8	68	36

2N4427

The RF Line

NPN SILICON HIGH FREQUENCY TRANSISTOR

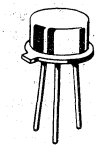
. . . designed for amplifier, frequency multiplier, or oscillator applications in military and industrial equipment. Suitable for use as output driver or pre-driver stages in VHF and UHF equipment.

- Specified 175 MHz, 12 Vdc Characteristics –
  Output Power = 1.0 Watt
  Minimum Gain = 10 dB
  Efficiency = 50%

1 W – 175 MHz

HIGH FREQUENCY TRANSISTOR

NPN SILICON



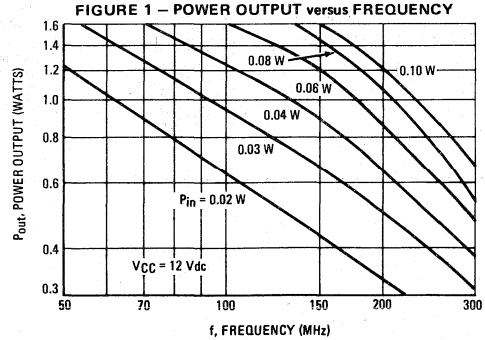
3

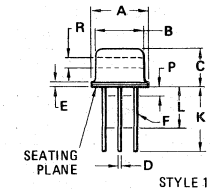
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Collector-Emitter Voltage	V_{CEO}	20	Vdc
*Collector-Base Voltage	V_{CB}	40	Vdc
*Emitter-Base Voltage	V_{EB}	2.0	Vdc
*Collector Current – Continuous	I_C	400	mAdc
*Base Current – Continuous	I_B	400	mAdc
Total Device Dissipation @ $T_A = 25^oC$ Derate above 25^oC	P_D	1.0 5.71	Watt $mW/^oC$
*Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	3.5 20	Watts $mW/^oC$
*Storage Temperature Range	T_{stg}	-65 to + 200	^oC

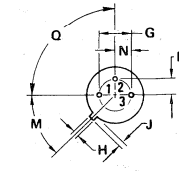
*Indicates JEDEC Registered Data

FIGURE 1 – POWER OUTPUT versus FREQUENCY





STYLE 1
PIN 1. EMITTER
2. BASE
3. COLLECTOR



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

CASE 79-02
TO-39

All JEDEC dimensions and notes apply.

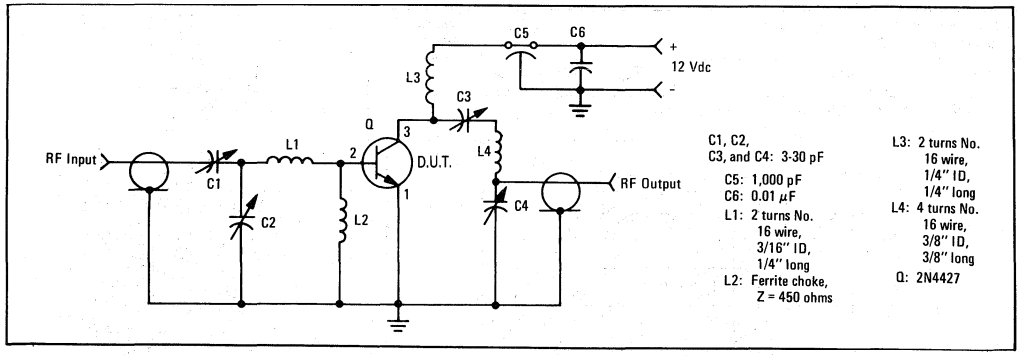
Available in TO-46 Package as MRF604

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
*Collector-Emitter Sustaining Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{CEO(sus)}$	20	–	Vdc
*Collector-Emitter Sustaining Voltage (I_C = 5.0 mAdc, R_{BE} = 10 ohms)	$V_{CER(sus)}$	40	–	Vdc
*Collector Cutoff Current (V_{CE} = 12 Vdc, I_B = 0)	I_{CEO}	–	0.02	mAdc
*Collector Cutoff Current (V_{CE} = 40 Vdc, V_{BE} = -1.5 Vdc) (V_{CE} = 12 Vdc, V_{BE} = -1.5 Vdc, T_C = +150°C)	I_{CEV}	– –	0.1 5.0	mAdc
*Emitter Cutoff Current (V_{EB} = 2.0 Vdc, I_C = 0)	I_{EBO}	–	0.1	mAdc
ON CHARACTERISTICS				
*DC Current Gain (I_C = 100 mAdc, V_{CE} = 5.0 Vdc) (I_C = 360 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10 5.0	200 –	–
*Collector-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 20 mAdc)	$V_{CE(sat)}$	–	0.5	Vdc
DYNAMIC CHARACTERISTICS				
*Current-Gain – Bandwidth Product (I_C = 50 mAdc, V_{CE} = 15 Vdc, f = 200 MHz)	f_T	500	–	MHz
*Output Capacitance (V_{CB} = 12 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	4.0	pF
FUNCTIONAL TEST				
*Power Input (Figure 2) (P_{out} = 1.0 W, V_{CC} = 12 Vdc, f = 175 MHz)	P_{in}	–	100	mW
Common-Emitter Amplifier Power Gain (P_{in} = 100 mW, V_{CC} = 12 Vdc, f = 175 MHz)	G_{pe}	10	–	dB
*Collector Efficiency (Figure 2) (P_{out} = 1.0 W, V_{CC} = 12 Vdc, f = 175 MHz)	η	50	–	%

*Indicates JEDEC Registered Data

FIGURE 2 – 175 MHz RF AMPLIFIER CIRCUIT FOR POWER-OUTPUT TEST



2N4428

The RF Line

NPN SILICON RF POWER TRANSISTOR

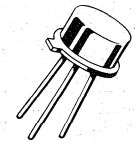
. . . designed primarily for use in large signal VHF and UHF amplifier output stages in military and industrial communications applications.

- Specified 28 Volt, 500 MHz Characteristics –
  Output Power = 750 mW
  Typical Gain = 10 dB
  Efficiency = 35%

0.75 W – 500 MHz

RF POWER TRANSISTOR

NPN SILICON

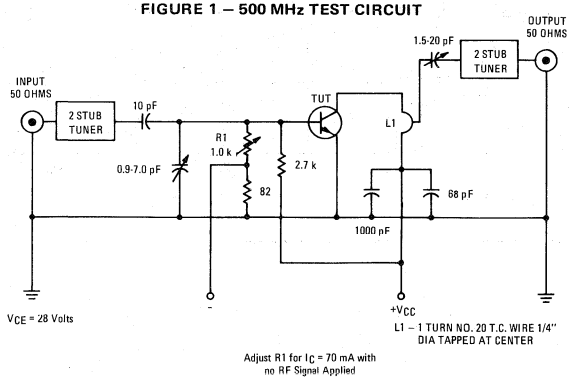


***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	35	Vdc
Collector-Base Voltage	V_{CB}	55	Vdc
Emitter-Base Voltage	V_{EB}	3.5	Vdc
Collector Current – Continuous	I_C	425	mAdc
Base Current – Continuous	I_B	150	mAdc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	3.5 20	Watts $mW/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	^oC

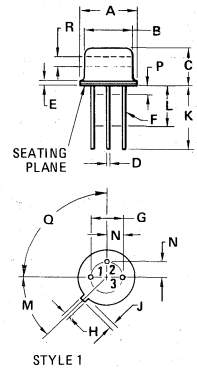
*Indicates JEDEC Registered Data.

FIGURE 1 – 500 MHz TEST CIRCUIT



L1 – 1 TURN NO. 20 T.C. WIRE 1/4" DIA TAPPED AT CENTER

Adjust R1 for I_C = 70 mA with no RF Signal Applied



STYLE 1
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO-39

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO(sus)}$	35	–	–	Vdc
Collector-Emitter Sustaining Voltage (I_C = 20 mAdc, R_{BE} = 10 ohms)	$V_{(BR)CER(sus)}$	55	–	–	Vdc
Collector Cutoff Current (V_{CE} = 55 Vdc, $V_{BE(on)}$ = -1.5 Vdc)	I_{CEX}	–	–	1.0	mAdc
Emitter Cutoff Current (V_{EB} = 3.5 Vdc, I_C = 0)	I_{EBO}	–	–	0.1	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 50 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	20	–	200	–
(I_C = 400 mAdc, V_{CE} = 5.0 Vdc)		5.0	–	–	
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 50 mAdc, V_{CE} = 20 Vdc, f = 200 MHz)	f_T	700	1000	–	MHz
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	1.2	3.5	pF
FUNCTIONAL TEST					
Power Input (Figure 1) (P_{out} = 750 mW, V_{CE} = 28 Vdc, R_S = 50 Ohms, f = 500 MHz)	P_{in}	–	–	75	mW
Collector Efficiency (Figure 1) (P_{out} = 750 mW, V_{CE} = 28 Vdc, R_S = 50 Ohms, f = 500 MHz)	η	35	–	–	%

*Indicates JEDEC Registered Data.

FIGURE 2 – CURRENT-GAIN–BANDWIDTH PRODUCT

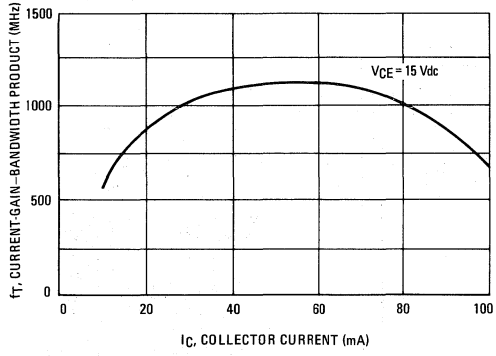
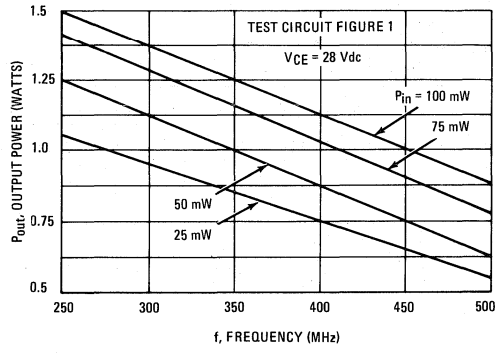


FIGURE 3 – OUTPUT POWER versus FREQUENCY



2N4957
2N4958
2N4959

The RF Line

PNP SILICON HIGH FREQUENCY TRANSISTORS

. . . designed for high-gain, low-noise amplifier, oscillator and mixer applications.

- Low Noise Figure @ 450 MHz –
  NF = 3.0 dB (Max) – 2N4957
  = 3.3 dB (Max) – 2N4958
  = 3.8 dB (Max) – 2N4959
- High Power Gain @ 450 MHz –
  G_{pe} = 17 dB (Min) – 2N4957
  = 16 dB (Min) – 2N4958
  = 15 dB (Min) – 2N4959
- High Current-Gain–Bandwidth Product –
  f_T = 1.2 GHz (Min) @ I_E = 2.0 mAdc – 2N4957
  = 1.0 GHz (Min) @ I_E = 2.0 mAdc – 2N4958, 2N4959

1.2 GHz @ 2.0 mAdc – 2N4957
1.0 GHz @ 2.0 mAdc – 2N4958, 2N4959

HIGH FREQUENCY TRANSISTORS

PNP SILICON

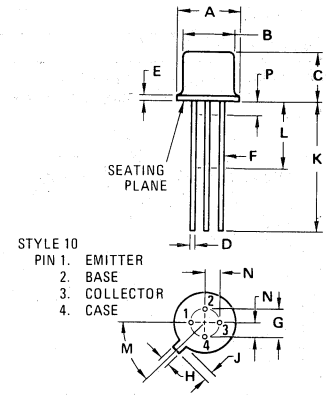


3

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	30	Vdc
Emitter-Base Voltage	V_{EBO}	3.0	Vdc
Collector Current – Continuous	I_C	30	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	200 1.14	mW mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

CASE 20-03
TO-72

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)		$V_{(BR)CEO}$	30	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)		$V_{(BR)CBO}$	30	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		$V_{(BR)EBO}$	3.0	–	–	Vdc
Collector Cutoff Current		I_{CBO}				μAdc
(V_{CB} = 10 Vdc, I_E = 0)			–	–	0.1	
(V_{CB} = 10 Vdc, I_E = 0, T_A = 150°C)			–	–	100	
ON CHARACTERISTICS						
DC Current Gain (I_C = 2.0 mAdc, V_{CE} = 10 Vdc)		h_{FE}	20	40	150	–
DYNAMIC CHARACTERISTICS						
Current-Gain–Bandwidth Product (1)		f_T				MHz
(I_E = 2.0 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	2N4957		1200	1600	2500	
	2N4958, 2N4959		1000	1500	2500	
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{cb}	–	0.4	0.8	pF
Small-Signal Current Gain (I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	20	–	200	–
Collector-Base Time Constant (I_E = 2.0 mAdc, V_{CB} = 10 Vdc, f = 63.6 MHz)		$r_b'C_c$	1.0	–	8.0	ps
Noise Figure		NF				dB
(I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 450 MHz)	2N4957		–	2.3	2.5	
	2N4958		–	2.6	3.0	
	2N4959		–	2.9	3.3	
			–	3.2	3.8	
FUNCTIONAL TESTS						
Common-Emitter Amplifier Power Gain		G_{pe}				dB
(V_{CE} = 10 Vdc, I_C = 2.0 mAdc, f = 450 MHz)	2N4957		17	–	25	
	2N4958		16	–	25	
	2N4959		15	–	25	

*Indicates JEDEC Registered Data.

(1) f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

FIGURE 1 – NOISE FIGURE AND POWER GAIN TEST CIRCUIT

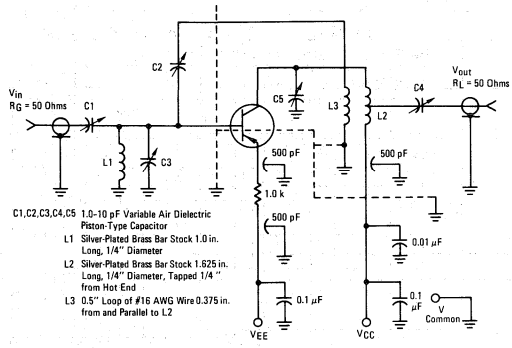


FIGURE 2 – UNILATERALIZED POWER GAIN versus FREQUENCY

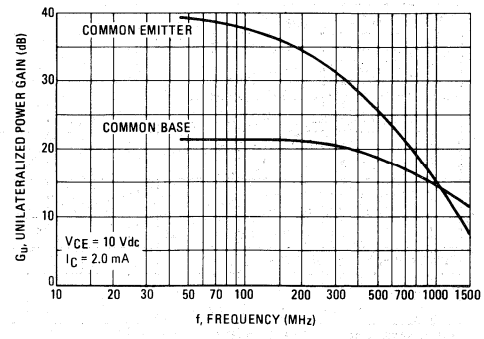


FIGURE 3 – NOISE FIGURE versus FREQUENCY

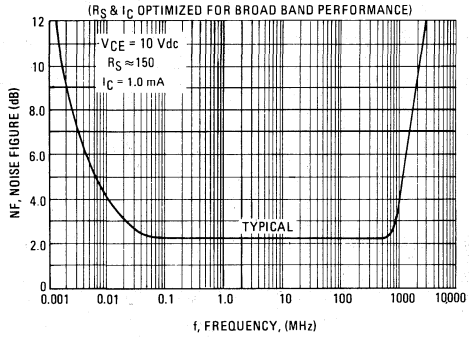


FIGURE 4 – NOISE FIGURE AND POWER GAIN versus COLLECTOR CURRENT

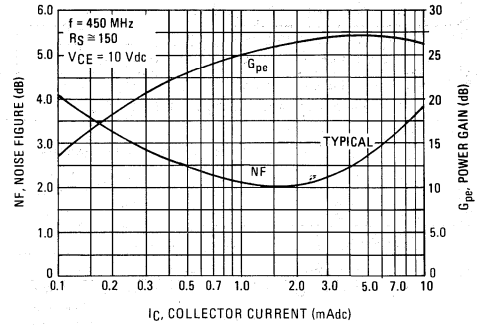


FIGURE 5 – CONTOURS OF NOISE FIGURE versus SOURCE RESISTANCE AND COLLECTOR CURRENT

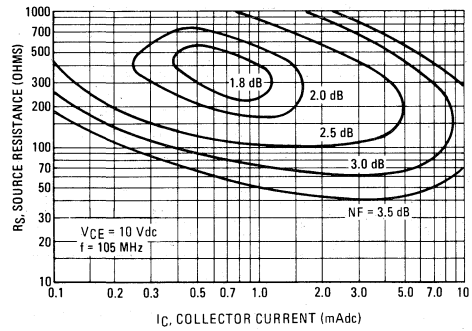
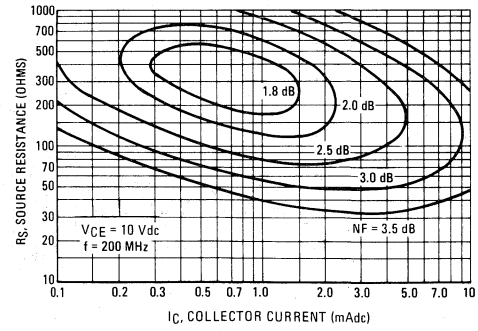


FIGURE 6 – CONTOURS OF NOISE FIGURE versus SOURCE RESISTANCE AND COLLECTOR CURRENT



COMMON EMITTER CIRCUIT DESIGN DATA

(V_{CE} = 10 Vdc, I_C = 2.0 mAdc)

FIGURE 7 – TRANSDUCER GAIN versus FREQUENCY

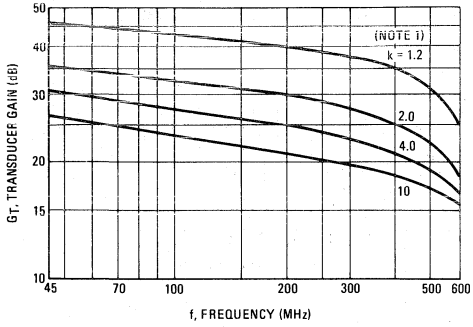


FIGURE 8 – LINVILL STABILITY FACTOR versus FREQUENCY

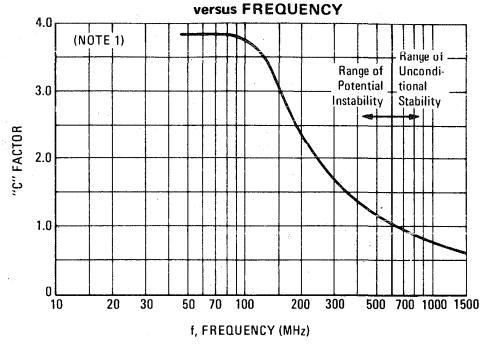


FIGURE 9 – LOAD ADMITTANCE versus FREQUENCY (REAL)

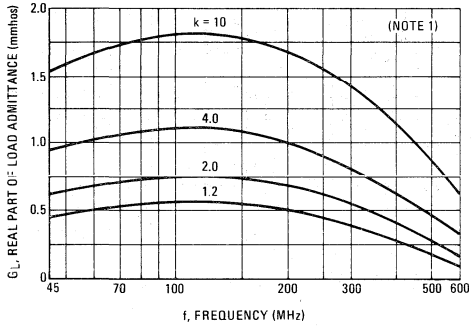


FIGURE 10 – LOAD ADMITTANCE versus FREQUENCY (IMAGINARY)

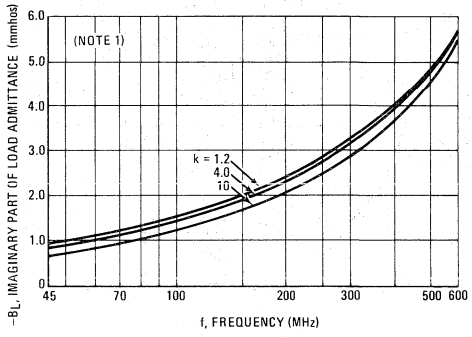


FIGURE 11 – SOURCE ADMITTANCE versus FREQUENCY (REAL)

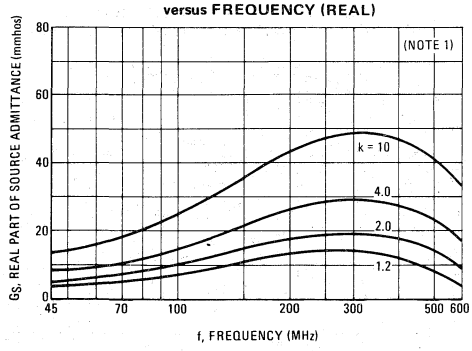
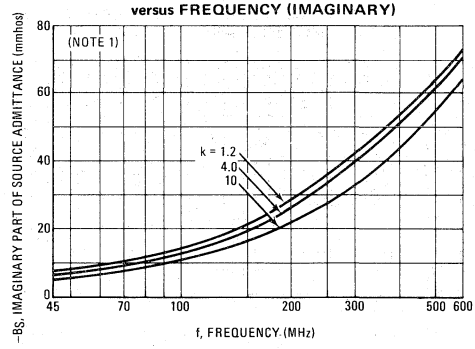


FIGURE 12 – SOURCE ADMITTANCE versus FREQUENCY (IMAGINARY)



NOTE 1

Figures 7 through 18 are included to assist the circuit designer in determining the stability of his particular circuit. Two stability criteria are given in these figures.

The Linvill "C" factor* is a measure of transistor stability when the input and output are terminated in the worst-case (open circuit) condition. When "C" is less than 1.0, the circuit is unconditionally stable. When "C" is greater than 1.0, the circuit is potentially unstable.

The Stern "K" factor† has been defined to determine the stability of a practical amplifier terminated in finite load and source admittances. If "K" is greater than 1.0, the circuit will be stable. If less than 1.0, the circuit will be unstable. For further details, see Application Note AN-215A.

* "Transistors and Active Circuits," Linvill and Gibbons, McGraw-Hill, 1961.

† "Stability and Power Gain of Tuned Transistor Amplifiers," Arthur P. Stern, Proc. I.R.E., March 1967.

COMMON BASE CIRCUIT DESIGN DATA

(V_{CB} = 10 Vdc, I_C = 2.0 mAdc)

FIGURE 13 – TRANSDUCER GAIN versus FREQUENCY

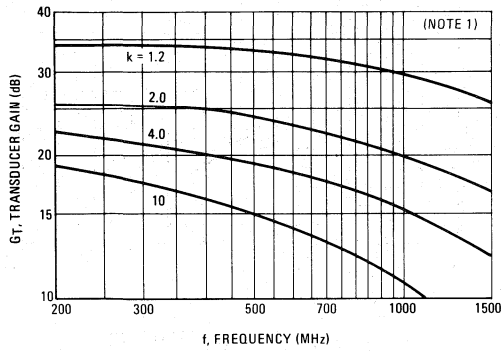


FIGURE 14 – LINVILL STABILITY FACTOR versus FREQUENCY

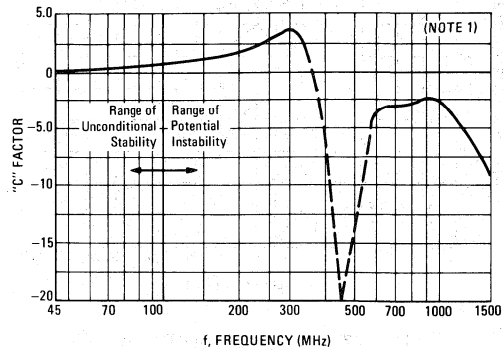


FIGURE 15 – LOAD ADMITTANCE versus FREQUENCY (REAL)

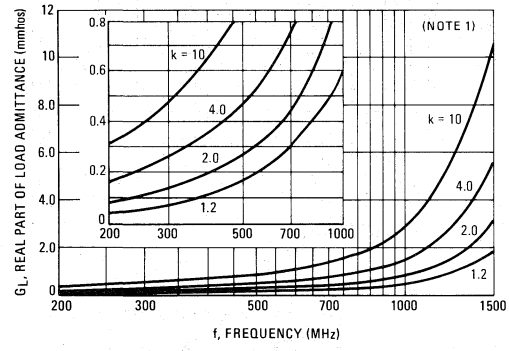


FIGURE 16 – LOAD ADMITTANCE versus FREQUENCY (IMAGINARY)

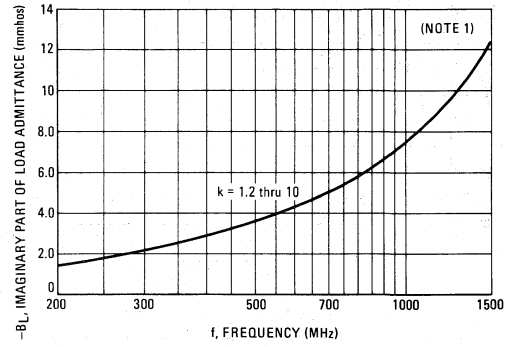


FIGURE 17 – SOURCE ADMITTANCE versus FREQUENCY (REAL)

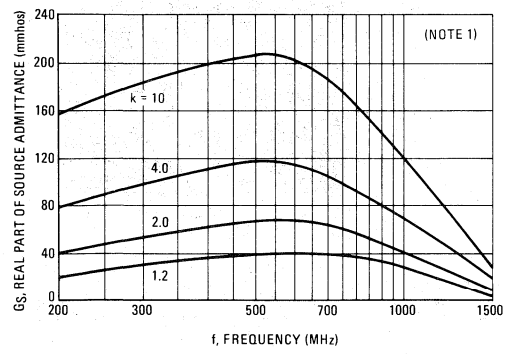
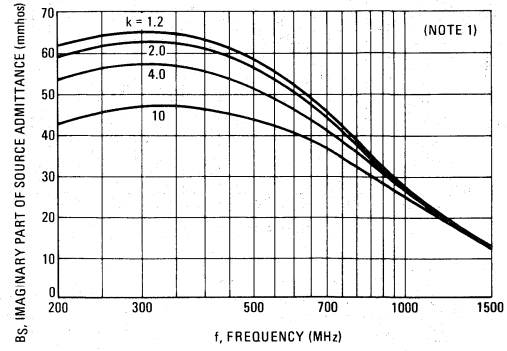


FIGURE 18 – SOURCE ADMITTANCE versus FREQUENCY (IMAGINARY)



3

FIGURE 19 – SMALL-SIGNAL CURRENT GAIN versus FREQUENCY

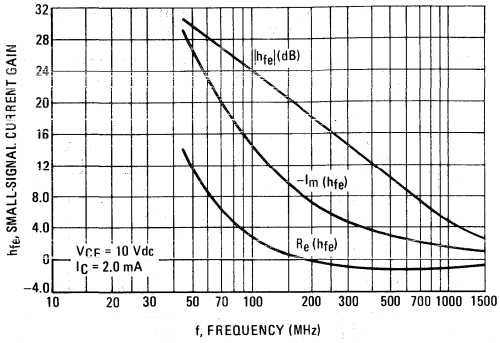


FIGURE 20 – POLAR h_{fe}

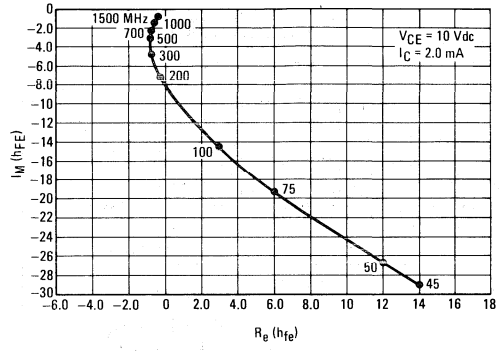


FIGURE 21 – f_T versus COLLECTOR CURRENT

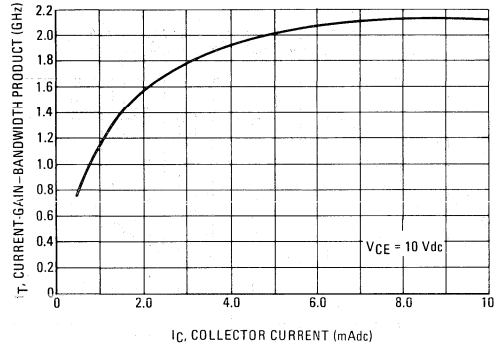


FIGURE 22 – DC CURRENT GAIN

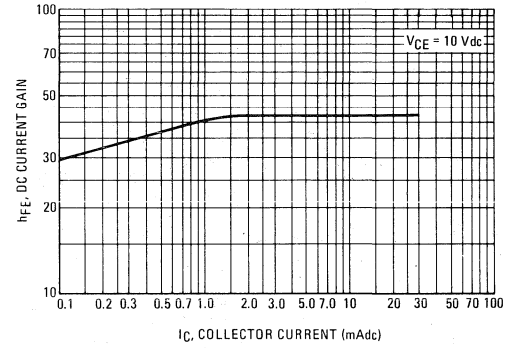


FIGURE 23 – CAPACITANCE

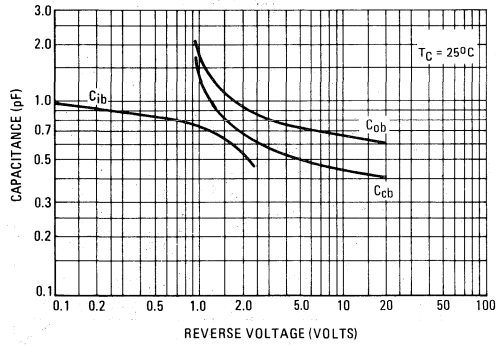
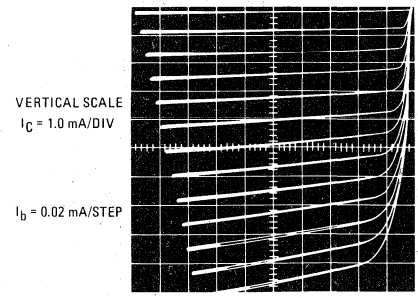
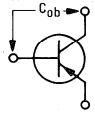
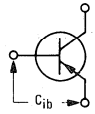


FIGURE 24 – COLLECTOR CHARACTERISTICS

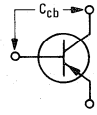




Apply reverse bias between collector and base and measure capacitance between these terminals. Emitter is open.



Apply reverse bias between emitter and base and measure capacitance between these terminals. Collector is open.



Apply reverse bias between collector and base and measure capacitance between these terminals. Emitter is guarded.

Y PARAMETERS versus CURRENT

(f = 450 MHz)

COMMON BASE

V_{CB} = 10 Vdc ——— V_{CB} = 15 Vdc — — —

FIGURE 25 – INPUT ADMITTANCE

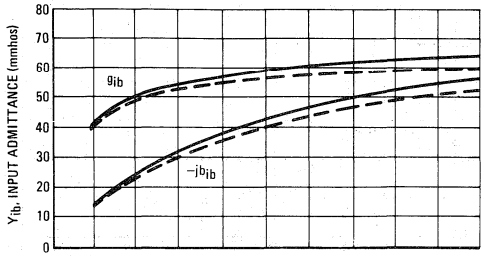


FIGURE 27 – FORWARD TRANSFER ADMITTANCE

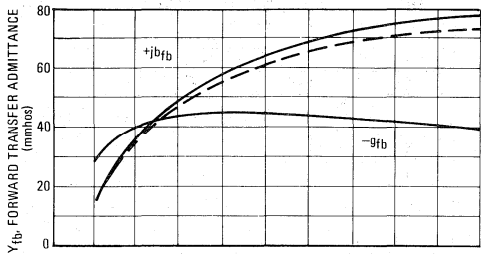


FIGURE 29 – OUTPUT ADMITTANCE

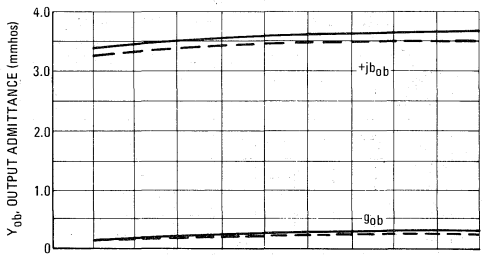
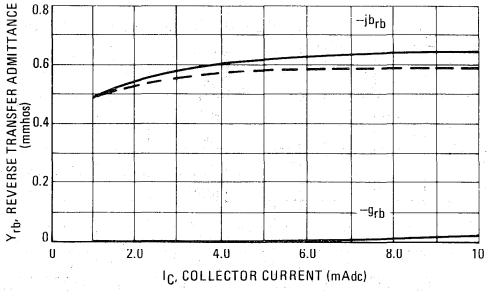


FIGURE 31 – REVERSE TRANSFER ADMITTANCE



COMMON EMITTER

V_{CE} = 10 Vdc ——— V_{CE} = 15 Vdc — — —

FIGURE 26 – INPUT ADMITTANCE

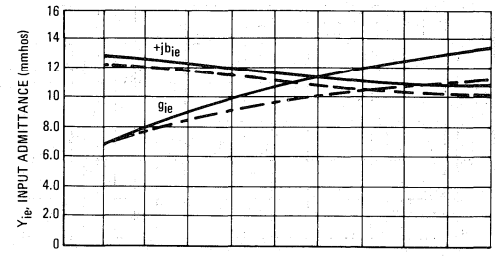


FIGURE 28 – FORWARD TRANSFER ADMITTANCE

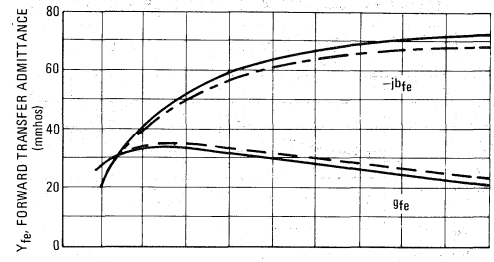


FIGURE 30 – OUTPUT ADMITTANCE

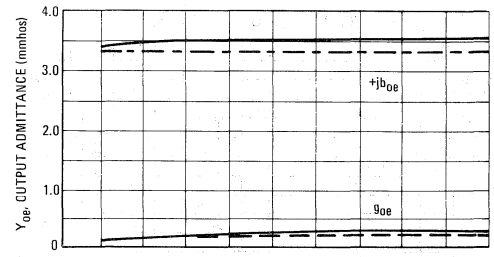
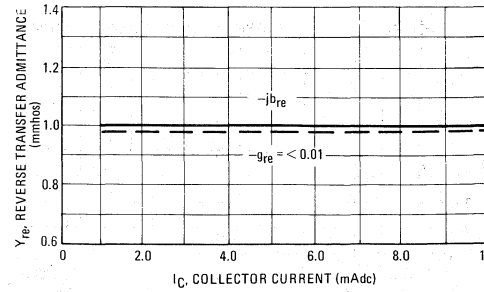


FIGURE 32 – REVERSE TRANSFER ADMITTANCE



3

COMMON BASE y PARAMETER VARIATIONS

(V_{CB} = 10 Vdc, I_C = 2.0 mAdc)

y PARAMETERS versus FREQUENCY

FIGURE 33 – y_{ib} INPUT ADMITTANCE

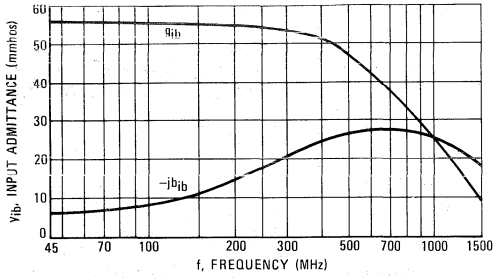


FIGURE 35 – y_{fb} FORWARD TRANSFER ADMITTANCE

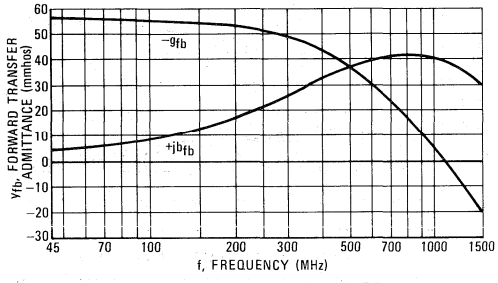


FIGURE 37 – y_{ob} OUTPUT ADMITTANCE

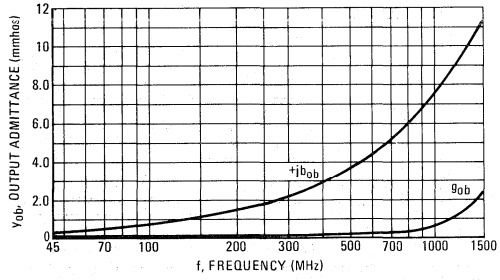
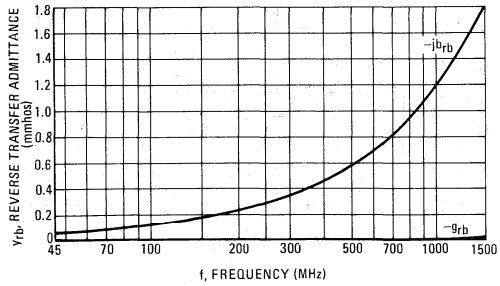


FIGURE 39 – y_{rb} REVERSE TRANSFER ADMITTANCE



POLAR y PARAMETERS versus FREQUENCY

FIGURE 34 – y_{ib} INPUT ADMITTANCE

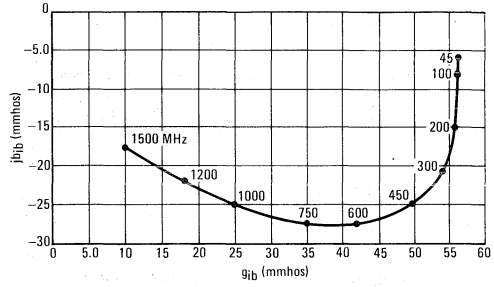


FIGURE 36 – y_{fb} FORWARD TRANSFER ADMITTANCE

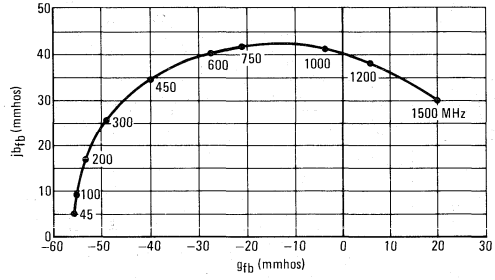


FIGURE 38 – y_{ob} OUTPUT ADMITTANCE

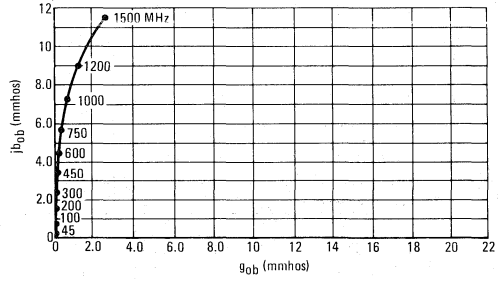
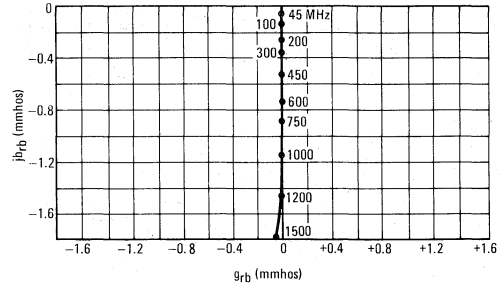


FIGURE 40 – y_{rb} REVERSE TRANSFER ADMITTANCE



COMMON EMITTER y PARAMETER VARIATIONS

(V_{CE} = 10 Vdc, I_C = 2.0 mAdc)

y PARAMETERS versus FREQUENCY

FIGURE 41 – y_{ie} INPUT ADMITTANCE

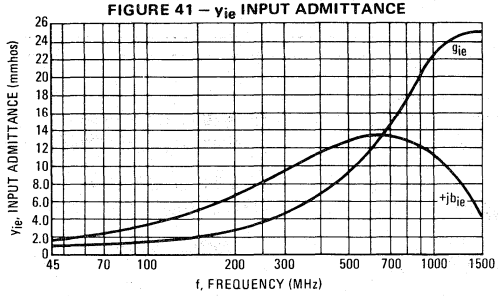


FIGURE 43 – y_{fe} FORWARD TRANSFER ADMITTANCE

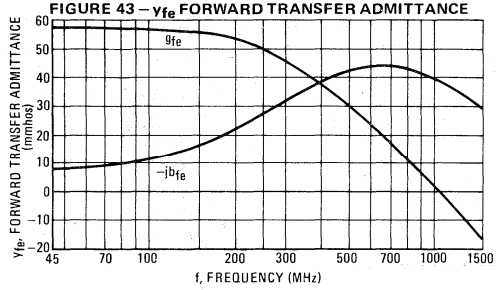


FIGURE 45 – y_{oe} OUTPUT ADMITTANCE

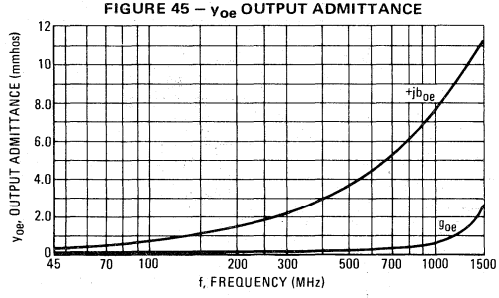
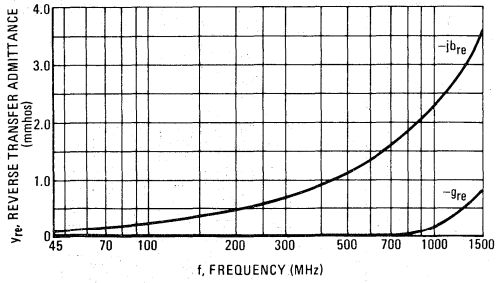


FIGURE 47 – y_{re} REVERSE TRANSFER ADMITTANCE



POLAR y PARAMETERS versus FREQUENCY

FIGURE 42 – y_{ie} INPUT ADMITTANCE

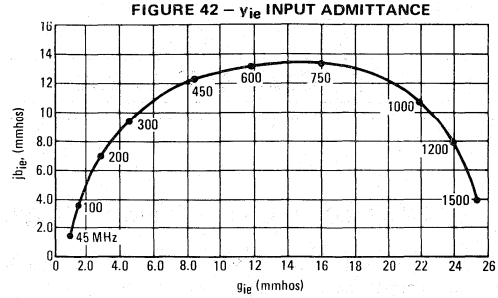


FIGURE 44 – y_{fe} FORWARD TRANSFER ADMITTANCE

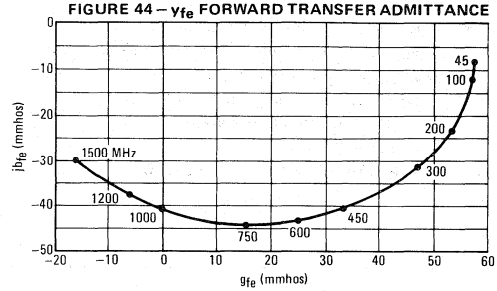


FIGURE 46 – y_{oe} OUTPUT ADMITTANCE

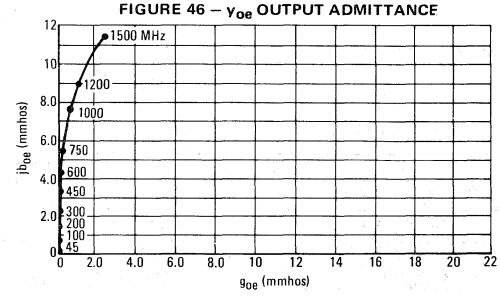
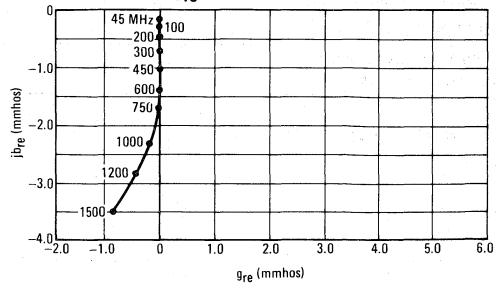


FIGURE 48 – y_{re} REVERSE TRANSFER ADMITTANCE



3

2N5031
2N5032

The RF Line

2.5 dB @ 450 MHz – 2N5031
3.0 dB @ 450 MHz – 2N5032

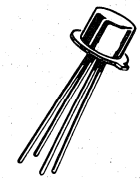
HIGH FREQUENCY TRANSISTORS

NPN SILICON

NPN SILICON HIGH-FREQUENCY TRANSISTORS

. . . designed primarily for use in high-gain, low-noise, small-signal amplifiers.

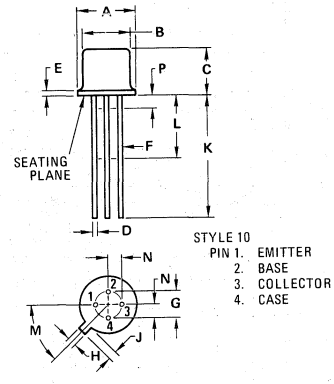
- High Current-Gain – Bandwidth Product –
  f_T = 1000 MHz (Min) @ I_C = 5.0 mAdc
- Low Noise Figure @ f = 450 MHz –
  NF = 2.5 dB (Max) – 2N5031
  = 3.0 dB (Max) – 2N5032
- High Power Gain –
  G_{pe} = 14 dB (Min) @ f = 450 MHz



*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	10	Vdc
Collector-Base Voltage	V_{CBO}	15	Vdc
Emitter-Base Voltage	V_{EBO}	3.0	Vdc
Collector Current – Continuous	I_C	20	mAdc
Total Device Dissipation @ T_A = 25°C	P_D	200	mW
Derate above 25°C		1.14	mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.



STYLE 10
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. CASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

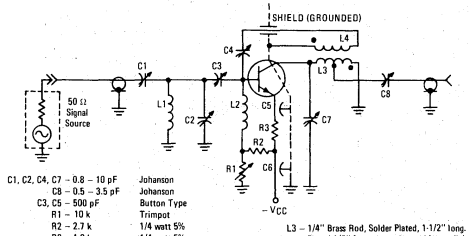
CASE 20-03
TO-72

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
*Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	10	–	–	Vdc
*Collector-Base Breakdown Voltage (I_C = 0.01 mAdc, I_E = 0)	$V_{(BR)CBO}$	15	–	–	Vdc
*Emitter-Base Breakdown Voltage (I_E = 0.01 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.0	–	–	Vdc
*Collector Cutoff Current (V_{CB} = 6.0 Vdc, I_E = 0)	I_{CBO}	–	1.0	10	nAdc
ON CHARACTERISTICS					
*DC Current Gain (I_C = 1.0 mAdc, V_{CE} = 6.0 Vdc)	h_{FE}	25	–	300	–
DYNAMIC CHARACTERISTICS					
*Current-Gain–Bandwidth Product (I_C = 5.0 mAdc, V_{CE} = 6.0 Vdc, f = 100 MHz)	f_T	1000	–	3500	MHz
*Output Capacitance (V_{CE} = 6.0 Vdc, I_E = 0, f = 0.1 MHz)	C_{cb}	–	1.3	1.5	pF
Collector-Base Time Constant (I_C = 6.0 mAdc, V_{CE} = 6.0 Vdc, f = 31.8 MHz)	$r_b'C_c$	–	5.0	–	ps
*Noise Figure (Figure 1) (I_C = 1.0 mAdc, V_{CE} = 6.0 Vdc, f = 450 MHz) 2N5031 2N5032	NF	– –	– –	2.5 3.0	dB
FUNCTIONAL TEST					
*Common-Emitter Amplifier Power Gain (Figure 1) (V_{CE} = 6.0 Vdc, I_C = 1.0 mAdc, f = 450 MHz)	G_{pe}	14	17	25	dB

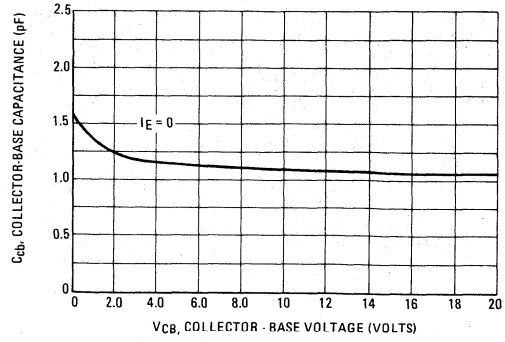
*Indicates JEDEC Registered Data.
(1) Tuned for Minimum Noise.

FIGURE 1 – POWER GAIN AND NOISE FIGURE TEST CIRCUIT



C1, C2, C4, C7 – 0.8 – 10 pF Johanson
C8 – 0.5 – 3.5 pF Johanson
C3, C5 – 500 pF Button Type
R1 – 10 k Trimpot
R2 – 2.7 k 1/4 watt 5%
R3 – 1.0 k 1/4 watt 5%
L1 – 1/4" Brass Rod, Solder Plated, 1-1/8" long. Placed 5/8" from the socket and in parallel with the shield, which bisects the socket. The ungrounded side is soldered directly to the ungrounded side of C2.
L2 – 0.22 μH
L3 – 1/4" Brass Rod, Solder Plated, 1-1/2" long. Placed 1/2" from the socket and in parallel with shield, which bisects the socket. The ungrounded side is soldered directly to the ungrounded side of C7. Output tap is 15/16" from ground.
L4 – 1/2 Turn #16, 5/16" above L3 and 5/8" long, (over L3).

FIGURE 2 – COLLECTOR-BASE CAPACITANCE versus VOLTAGE



3

FIGURE 3 – CURRENT-GAIN–BANDWIDTH PRODUCT

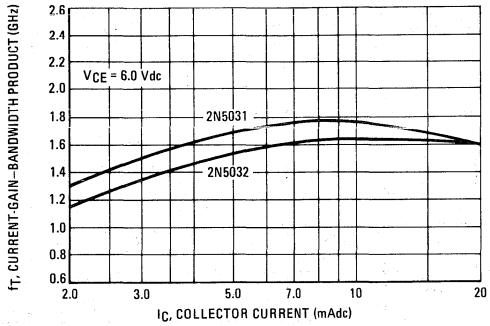


FIGURE 4 – S_{11} AND S_{22}

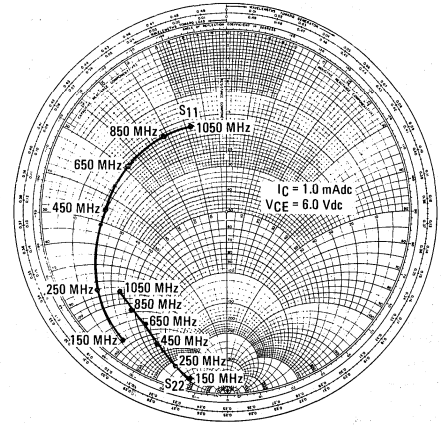


FIGURE 5 – S_{12}

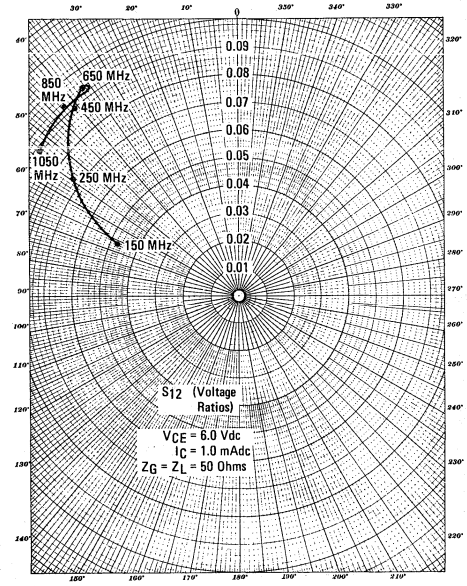


FIGURE 6 – S_{21}

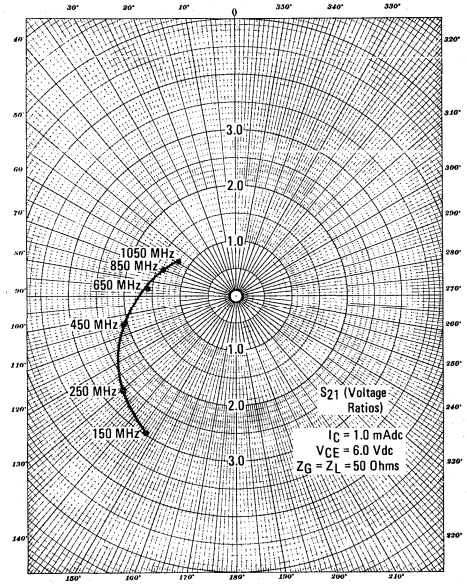


FIGURE 7 – NOISE FIGURE versus FREQUENCY

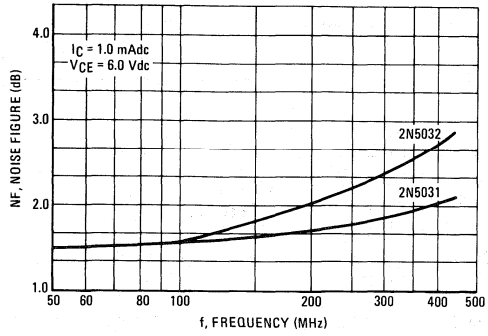


FIGURE 8 – POWER GAIN versus FREQUENCY

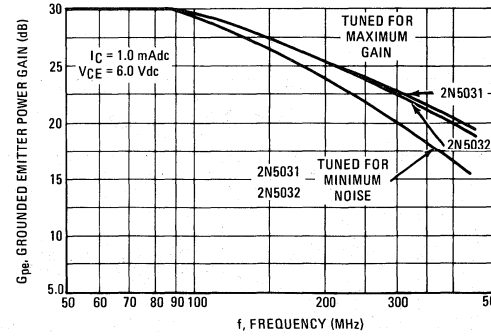


FIGURE 9 – INPUT ADMITTANCE versus FREQUENCY

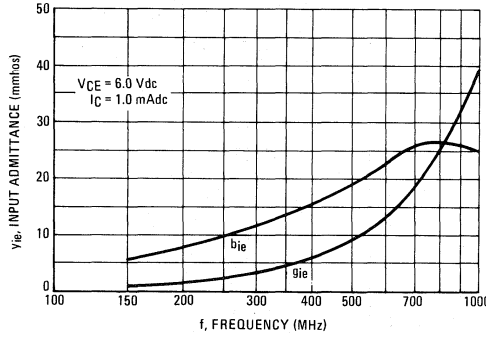


FIGURE 10 – OUTPUT ADMITTANCE versus FREQUENCY

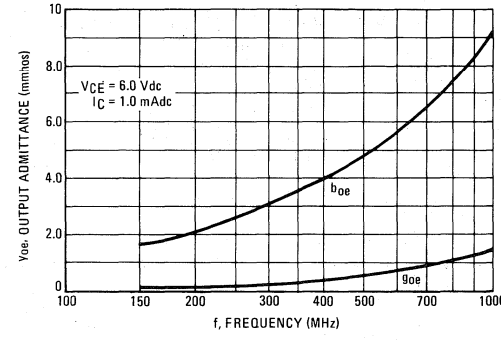


FIGURE 11 – FORWARD TRANSFER ADMITTANCE versus FREQUENCY

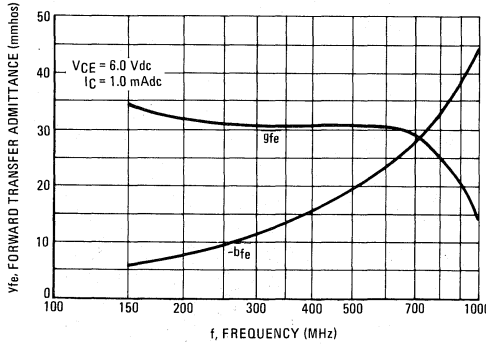
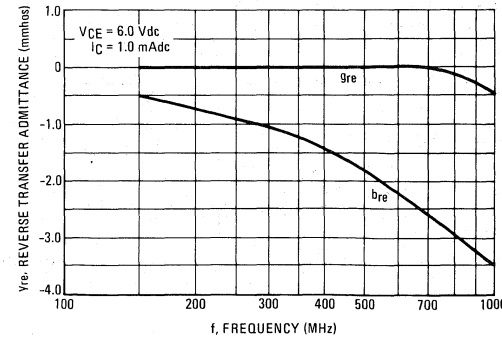


FIGURE 12 – REVERSE TRANSFER ADMITTANCE versus FREQUENCY



3

2N5108

The RF Line

1.0 W - 1 GHz

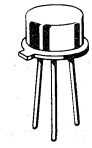
HIGH FREQUENCY TRANSISTOR

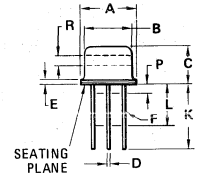
NPN SILICON

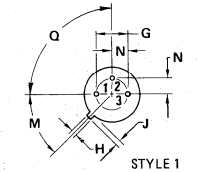
NPN SILICON HIGH-FREQUENCY TRANSISTOR

. . . designed for amplifier, frequency multiplier, or oscillator applications in military and industrial equipment. Suitable for use as output, driver, or pre-driver stages in UHF equipment and as a fundamental frequency oscillator at 1.68 GHz.

- Specified 1 GHz, 28 Vdc Characteristics —
  Output Power = 1.0 Watt
  Minimum Gain = 5.0 dB
  Efficiency = 35%
- Typical 1.68 GHz, 28 Vdc Characteristics —
  Output Power = 0.3 Watt
  Efficiency = 15%







STYLE 1
PIN 1. EMITTER
2. BASE
3. COLLECTOR

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
*Collector-Emitter Voltage (R_{BE} = 10 Ohms)	V_{CER}	55	Vdc
*Collector-Base Voltage	V_{CB}	55	Vdc
*Emitter-Base Voltage	V_{EB}	3.0	Vdc
*Collector Current — Continuous	I_C	0.4	Adc
*Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	3.5 0.02	Watts $W/^oC$
*Storage Temperature Range	T_{stg}	-65 to +200	^oC

*Indicates JEDEC Registered Data.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

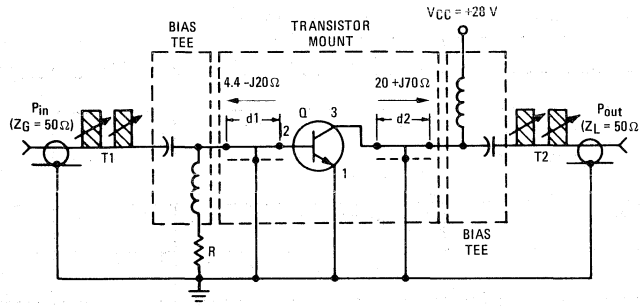
CASE 79-02
TO-39

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
*Collector-Emitter Sustaining Voltage (I_C = 5.0 mAdc, R_{BE} = 10 ohms)	$V_{CER(sus)}$	55	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	55	–	–	Vdc
*Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.0	–	–	Vdc
*Collector Cutoff Current (V_{CE} = 15 Vdc, I_B = 0)	I_{CEO}	–	–	20	μAdc
*Collector Cutoff Current (V_{CE} = 50 Vdc, V_{BE} = 0) (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 150°C)	I_{CES}	– –	– –	1.0 10	μAdc mAdc
ON CHARACTERISTICS					
Collector-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)	$V_{CE(sat)}$	–	–	0.5	Vdc
DYNAMIC CHARACTERISTICS					
*Current-Gain—Bandwidth Product (I_C = 50 mAdc, V_{CE} = 15 Vdc, f = 200 MHz)	f_T	1200	–	–	MHz
*Output Capacitance (V_{CB} = 30 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	1.3	3.0	pF
FUNCTIONAL TEST					
*Common-Emitter Amplifier Power Gain (Figure 1) (P_{out} = 1.0 W, V_{CC} = 28 Vdc, I_C = 102 mAdc, f = 1.0 GHz)	G_{PE}	5.0	–	–	dB
Power Output (Figure 1) (P_{in} = 316 mW, V_{CE} = 28 Vdc, f = 1.0 GHz)	P_{out}	1.0	–	–	Watt
*Collector Efficiency (P_{in} = 316 mW, V_{CE} = 28 Vdc, f = 1.0 GHz)	η	35	–	–	%
Power Output (Oscillator) (Figure 2) (V_{CE} = 20 Vdc, V_{EB} = 1.5 Vdc, f = 1.68 GHz) (Minimum Efficiency = 15%)	P_{out}	–	0.3	–	Watt

*Indicates JEDEC Registered Data.

FIGURE 1 – 1 GHz RF AMPLIFIER OUTPUT POWER TEST CIRCUIT

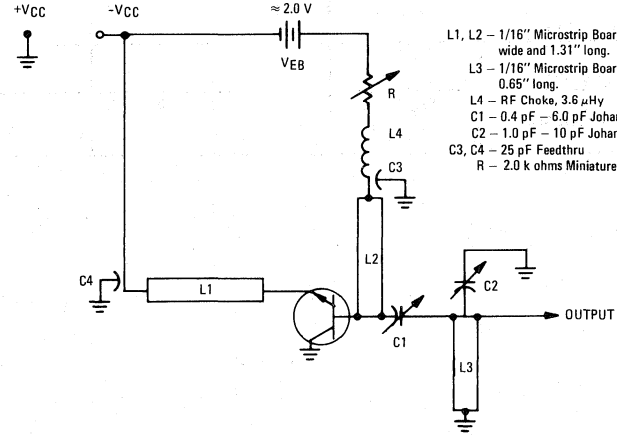


d1: 1" Input line, center conductor width = 0.280"
d2: 1" Output line, center conductor width = 0.125"
Q: 2N5108
R: 3.9 ohms
T1, T2: Microlab Double Stub Tuner, or Equivalent
Bias Tee: Microlab 08N, or Equivalent
Transistor Mount: 1/32" Microstrip board

Note: Impedance measurements are made at transistor socket pins.

3

FIGURE 2 – 1.68 GHz RF OSCILLATOR OUTPUT POWER TEST CIRCUIT



L1, L2 – 1/16" Microstrip Board. Lines are 0.16" wide and 1.31" long.
L3 – 1/16" Microstrip Board. 0.16" wide and 0.65" long.
L4 – RF Choke, 3.6 μHy
C1 – 0.4 pF – 6.0 pF Johanson 4640
C2 – 1.0 pF – 10 pF Johanson 4355
C3, C4 – 25 pF Feedthru
R – 2.0 k ohms Miniature Trim pot

FIGURE 3 – OUTPUT POWER versus INPUT POWER

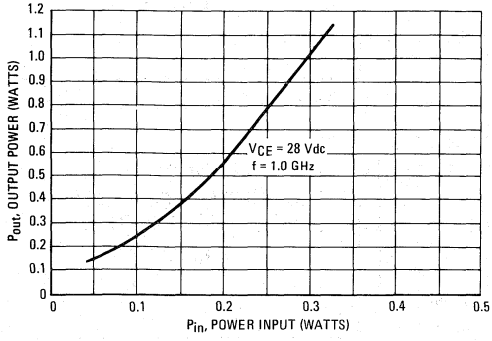


FIGURE 4 – OUTPUT POWER versus FREQUENCY

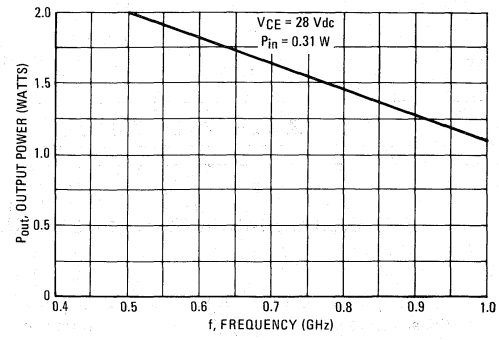


FIGURE 5 – OUTPUT POWER versus COLLECTOR-EMITTER VOLTAGE

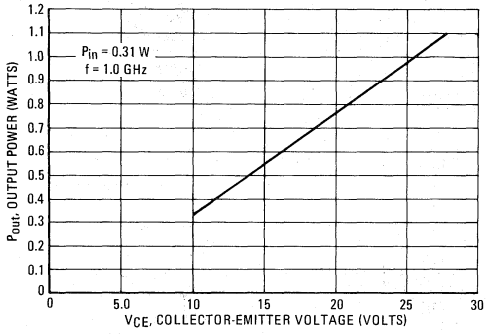


FIGURE 6 – OSCILLATOR OUTPUT POWER versus COLLECTOR CURRENT

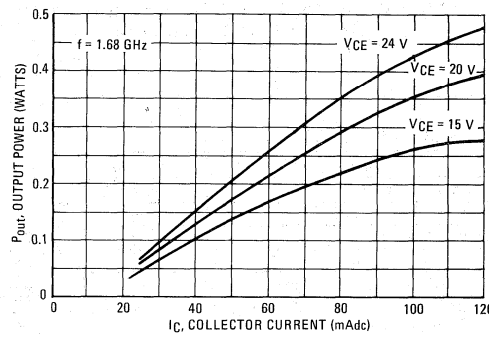


FIGURE 7 CURRENT-GAIN–BANDWIDTH PRODUCT versus CURRENT

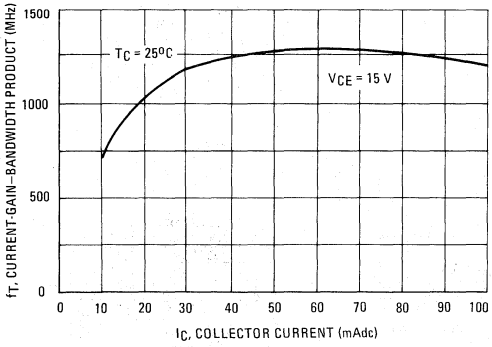
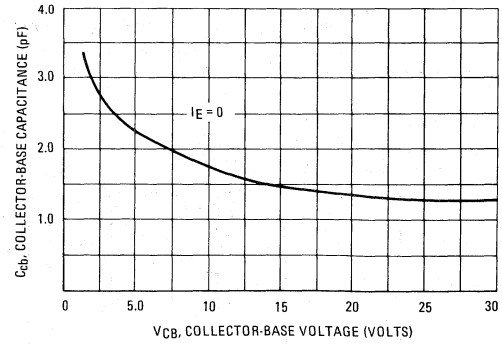


FIGURE 8 COLLECTOR BASE CAPACITANCE versus VOLTAGE



3

2N5109

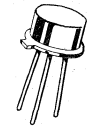
The RF Line

NPN SILICON HIGH-FREQUENCY TRANSISTOR

. . . designed specifically for broadband applications requiring good linearity. Useable as a high frequency current mode switch to 200 mA.

- Low Noise Figure – @ f = 200 MHz
  NF = 3.0 dB (Typ)
- High Current-Gain – Bandwidth Product –
  f_T = 1200 MHz (Min) @ I_C = 50 mAdc

1.2 GHz @ 50 mAdc
HIGH FREQUENCY TRANSISTOR
NPN SILICON



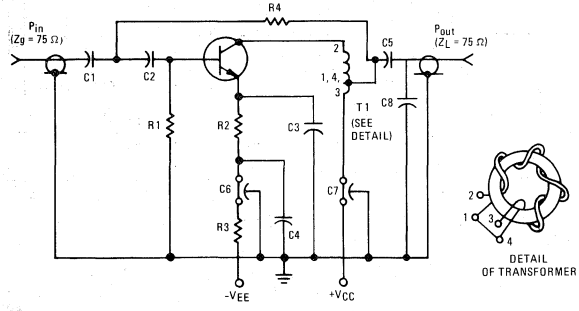
3

*MAXIMUM RATINGS

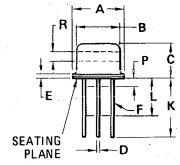
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CBO}	40	Vdc
Emitter-Base Voltage	V_{EBO}	3.0	Vdc
Base Current – Continuous	I_B	400	mAdc
Collector Current – Continuous	I_C	400	mAdc
Total Device Dissipation @ T_C = 75°C (1) Derate above 25°C	P_D	2.5 20	Watt mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

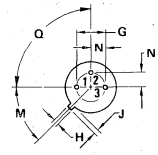
(1) Total Device Dissipation at T_A = 25°C is 1.0 Watt.
* Indicates JEDEC Registered Data.

FIGURE 1 – RF AMPLIFIER FOR VOLTAGE GAIN TEST CIRCUIT



C1, C2, C3, C5 0.002 μF
C4 0.03 μF
C6, C7 1500 pF
C8 18 pF
R1 4.7 k, 1/4 W
R2 6.8 Ω, 1/2 W
R3 330 Ω, 1 W
R4 200 Ω, 1/4 W
T1 4 Turns #30 Wire
Bifilar wound on "Indiana General" Core #CF-102-Q1, or equivalent





STYLE 1
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

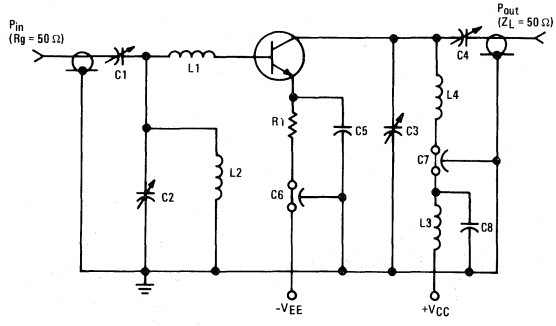
CASE 79-02
TO-39

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**					
Collector-Emitter Sustaining Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{CEO(sus)}$	20	–	–	Vdc
Collector-Emitter Sustaining Voltage (1) (I_C = 5.0 mAdc, R_{BE} = 10 Ω)	$V_{CER(sus)}$	40	–	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, I_B = 0)	I_{CEO}	–	–	20	μAdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = -1.5 V, T_C = 150°C) (V_{CE} = 35 Vdc, V_{BE} = -1.5 V)	I_{CEX}	– –	– –	5.0 5.0	mAdc mAdc
Emitter Cutoff Current (V_{BE} = 3.0 Vdc, I_C = 0)	I_{EBO}	–	–	100	μAdc
***ON CHARACTERISTICS**					
DC Current Gain (I_C = 360 mAdc, V_{CE} = 5.0 Vdc) (I_C = 50 mAdc, V_{CE} = 15 Vdc)	h_{FE}	 5.0 40	 – –	 – 120	 – –
DYNAMIC CHARACTERISTICS					
*Current-Gain – Bandwidth Product (I_C = 50 mAdc, V_{CE} = 15 Vdc, f = 200 MHz)	f_T	1200	–	–	MHz
*Collector-Base Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	–	1.8	3.5	pF
Noise Figure (I_C = 10 mAdc, V_{CE} = 15 Vdc, f = 200 MHz) (Figure 2)	NF	–	3.0	–	dB
FUNCTIONAL TEST					
*Common-Emitter Amplifier Voltage Gain (Figure 1) (I_C = 50 mAdc, V_{CC} = 15 Vdc, f = 50 to 216 MHz)	G_{ve}	11	–	–	dB
*Power Input (Figure 2) (I_C = 50 mAdc, V_{CC} = 15 Vdc, R_S = 50 ohms, P_{out} = 1.26 mW, f = 200 MHz)	P_{in}	–	–	0.1	mW

*Indicates JEDEC Registered Data.
(1) Pulsed thru a 25 mH Inductor; 50% Duty Cycle

FIGURE 2 – 200 MHz TEST CIRCUIT



C1, C2, C3 1.0 – 30 pF
C4 1.0 – 20 pF
C5 10,000 pF
C6, C7 1,000 pF
C8 0.01 μF

L1 4-1/2 turns, No. 22 wire, 3/16" I.D.
L4 3-1/2 turns, No. 22 wire, 3/16" I.D.
L2, L3 0.82 μH RFC
R1 240 OHMS, 2 WATTS

FIGURE 3 – CURRENT-GAIN – BANDWIDTH PRODUCT

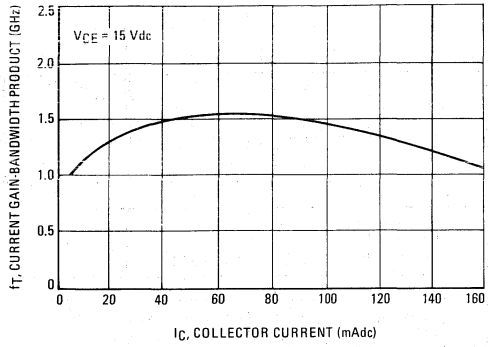


FIGURE 4 – COLLECTOR-BASE TIME CONSTANT

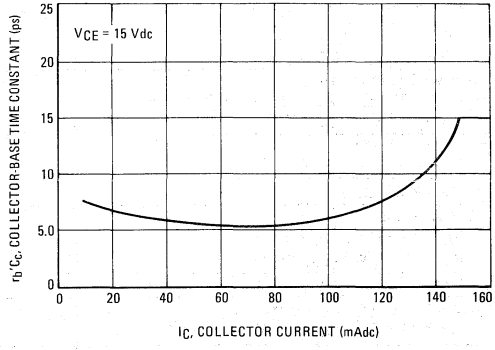


FIGURE 5 – SATURATION VOLTAGES

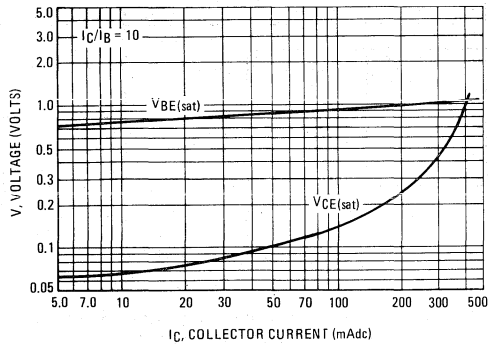


FIGURE 6 – CAPACITANCES versus REVERSE VOLTAGE

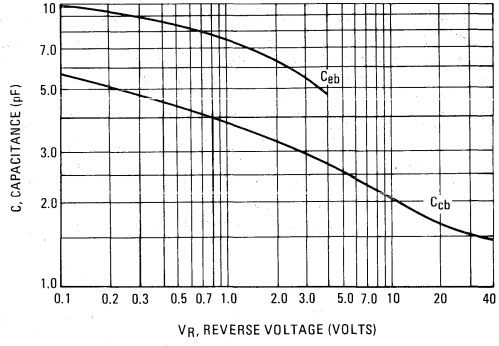


FIGURE 7 – INPUT ADMITTANCE versus FREQUENCY

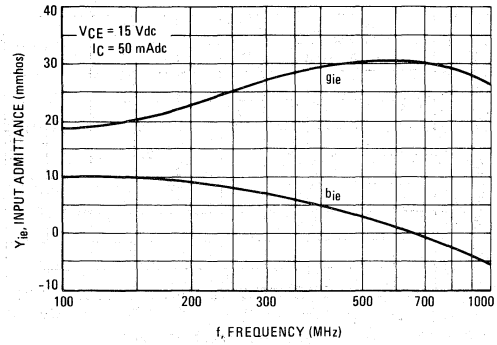


FIGURE 8 – INPUT ADMITTANCE versus COLLECTOR CURRENT

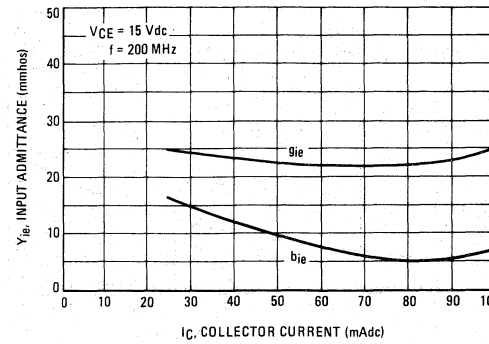


FIGURE 9 – REVERSE TRANSFER ADMITTANCE versus FREQUENCY

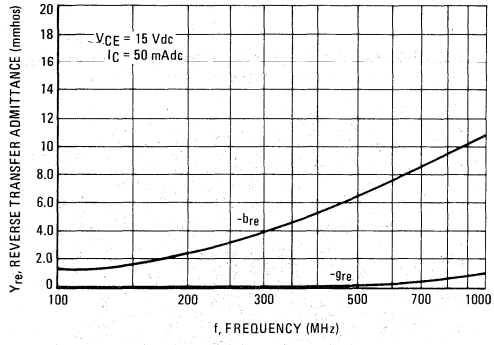


FIGURE 10 – REVERSE TRANSFER ADMITTANCE versus COLLECTOR CURRENT

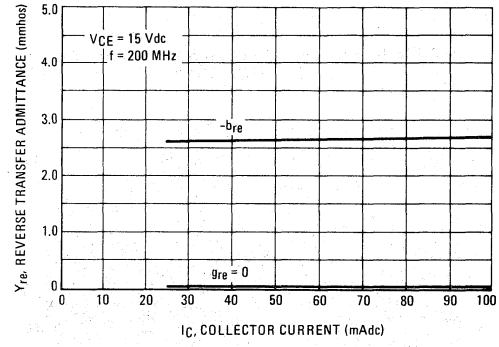


FIGURE 11 – FORWARD TRANSFER ADMITTANCE versus FREQUENCY

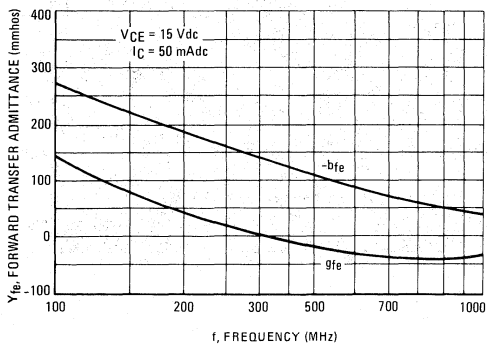


FIGURE 12 – FORWARD TRANSFER ADMITTANCE versus COLLECTOR CURRENT

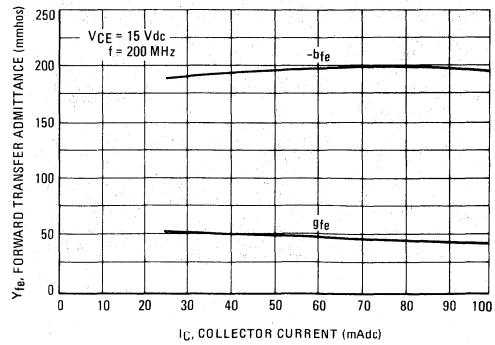


FIGURE 13 – OUTPUT ADMITTANCE versus FREQUENCY

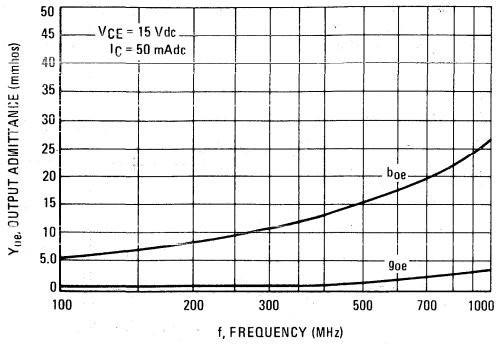


FIGURE 14 – OUTPUT ADMITTANCE versus COLLECTOR CURRENT

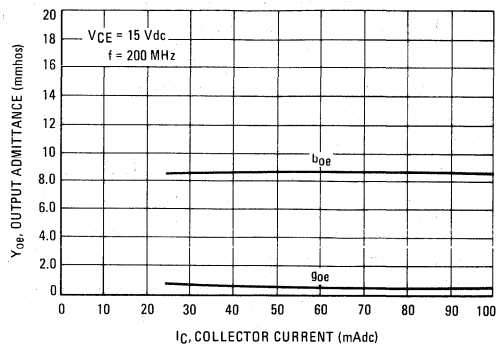


FIGURE 15 – INPUT REFLECTION COEFFICIENT versus FREQUENCY

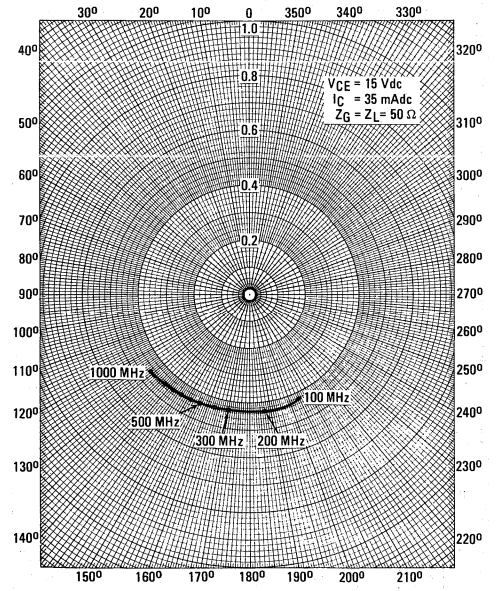


FIGURE 16 – OUTPUT REFLECTION COEFFICIENT versus FREQUENCY

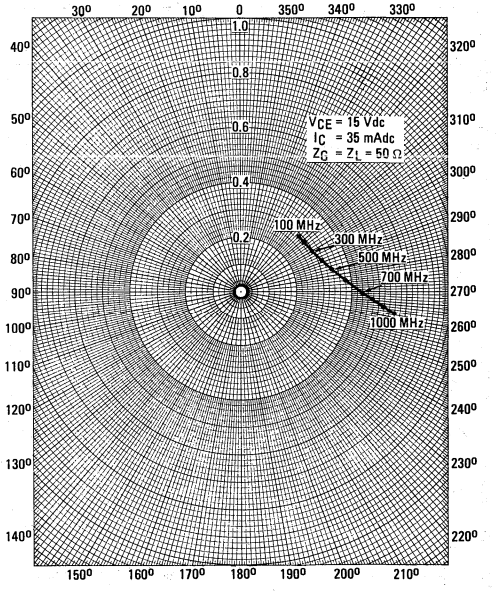


FIGURE 17 – REVERSE TRANSMISSION COEFFICIENT versus FREQUENCY

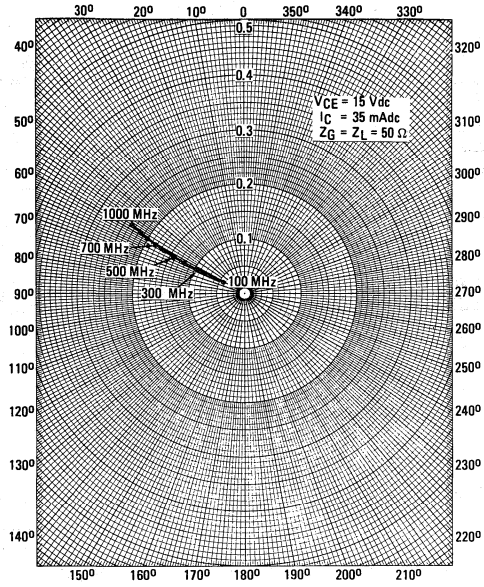


FIGURE 18 – FORWARD TRANSMISSION COEFFICIENT versus FREQUENCY

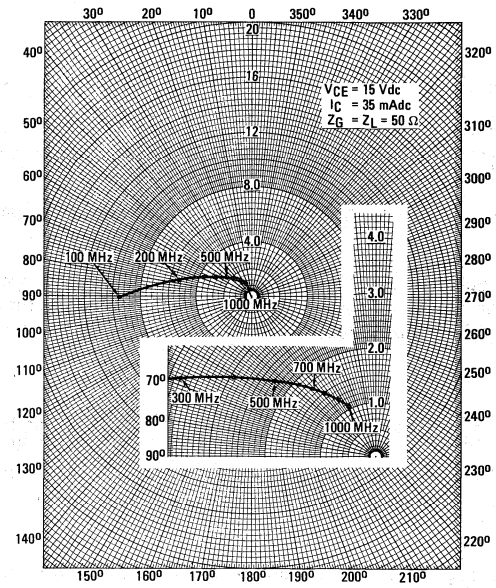
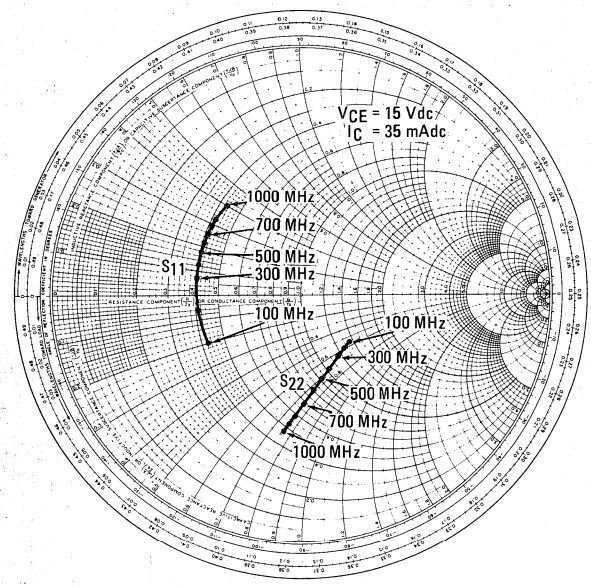


FIGURE 19 – INPUT REFLECTION COEFFICIENT AND OUTPUT REFLECTION COEFFICIENT versus FREQUENCY



2N5160

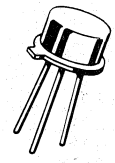
The RF Line

PNP SILICON RF POWER TRANSISTORS

. . . designed for amplifier, frequency multiplier or oscillator applications in military and industrial equipment. Suitable for use as Class A, B, or C output driver, or pre-driver stages in VHF and UHF.

- High Power Gain – G_{PE} = 8.0 dB (Min) @ f = 400 MHz, 14.5 dB (Typ) @ 175 MHz – No Emitter Tuning
- Power Output – P_{out} = 1.0 Watt (Min) @ f = 400 MHz = 1.5 Watt (Typ) @ f = 175 MHz
- Resists Burnout When Load is Shorted or Opened
- Designed for Use in Complementary Circuits with 2N3866

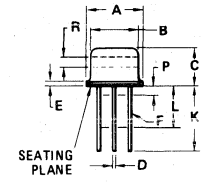
PNP SILICON
AMPLIFIER
TRANSISTOR

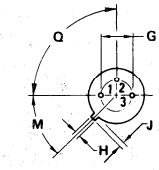


3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	0.4	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	5.0 28.6	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C





STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO-39

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{(BR)CEO(sus)}$	40	-	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO(sus)}$	4.0	-	-	Vdc
Collector Cutoff Current (V_{CE} = 28 Vdc, I_B = 0)	I_{CEO}	-	-	20	μAdc
Collector Cutoff Current (V_{CE} = 60 Vdc, V_{BE} = 0)	I_{CES}	-	-	0.1	mAdc
Collector Cutoff Current (V_{CB} = 28 Vdc, I_E = 0)	I_{CBO}	-	-	1.0	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 50 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	-	-	-
DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwidth Product (I_C = 50 mAdc, V_{CE} = 15 Vdc, f = 200 MHz)	f_T	500	900	-	MHz
Collector-Base Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 0.1 to 1.0 MHz)	C_{cb}	-	2.5	4.0	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CE} = 28 Vdc, P_{in} = 0.16 Watt, f = 400 MHz) (V_{CE} = 28 Vdc, P_{in} = 50 mW, f = 175 MHz)	G_{PE}	8.0 -	8.8 14.5	- -	dB
Power Output (V_{CE} = 28 Vdc, P_{in} = 0.16 Watt, f = 400 MHz) (V_{CE} = 28 Vdc, P_{in} = 50 mW, f = 175 MHz)	P_{out}	1.0 -	1.2 1.4	- -	Watt
Collector Efficiency (V_{CE} = 28 Vdc, P_{in} = 0.16 Watt, f = 400 MHz)	η	45	55	-	%

FIGURE 1 – 400-MHz TEST CIRCUIT

C_1 – 10 pF
C_2, C_3, C_4, C_5 – 1.0 – 10 pF variable
C_6 – 2400 pF feed through
C_7 – 0.004 μF
C_8 – 0.01 μF
L_1 – 30 nH, 1 turn, No. 20 AWG
L_2 – 75 nH, 3 turns, No. 20 AWG
L_3 – 0.33 μH, R.F.C.

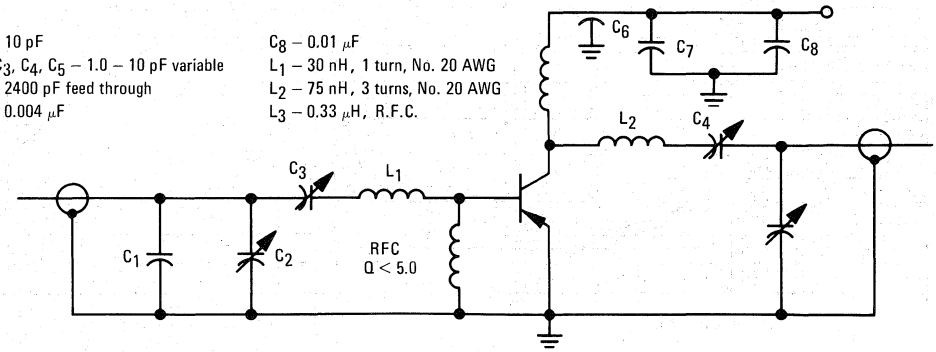


FIGURE 2 – POWER OUTPUT versus FREQUENCY

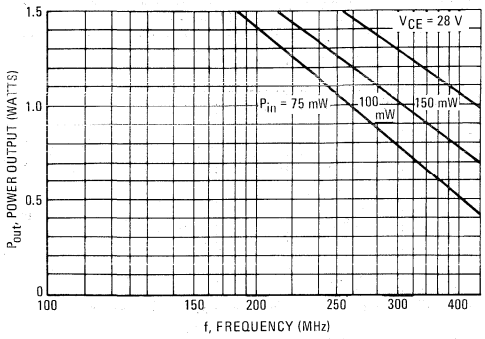


FIGURE 3 – POWER OUTPUT versus POWER INPUT

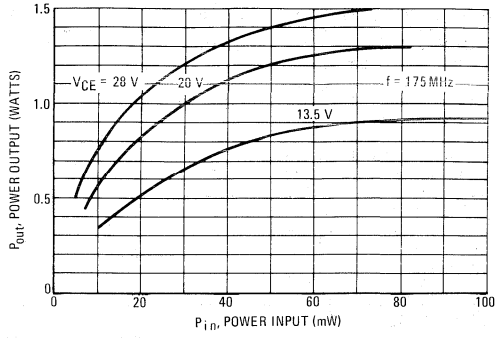


FIGURE 4 – PARALLEL INPUT IMPEDANCE versus FREQUENCY

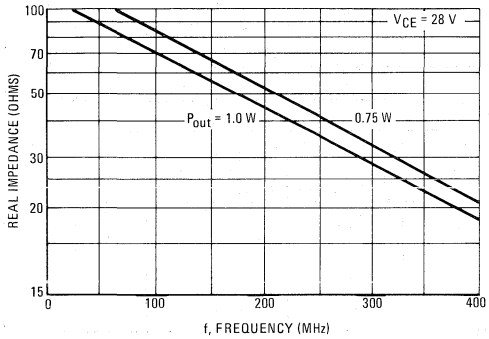


FIGURE 5 – PARALLEL INPUT IMPEDANCE versus FREQUENCY

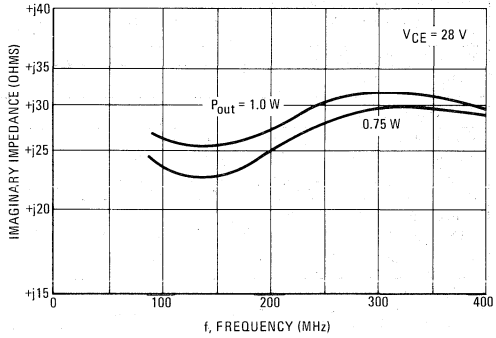


FIGURE 6 – PARALLEL OUTPUT CAPACITANCE versus FREQUENCY

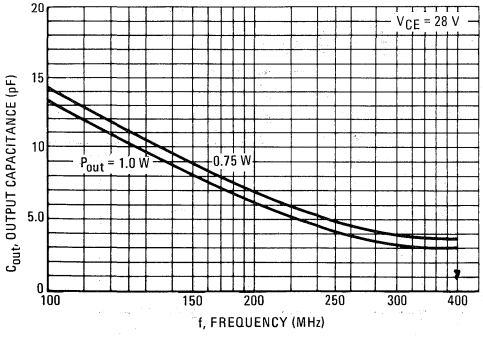


FIGURE 7 – CURRENT-GAIN–BANDWIDTH PRODUCT versus COLLECTOR CURRENT

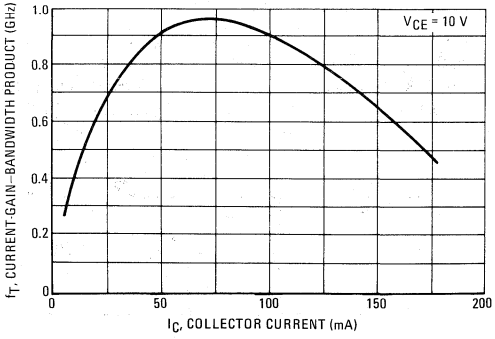


FIGURE 8 – 2N5160 300-MHz COMPLEMENTARY POWER OUTPUT CIRCUIT

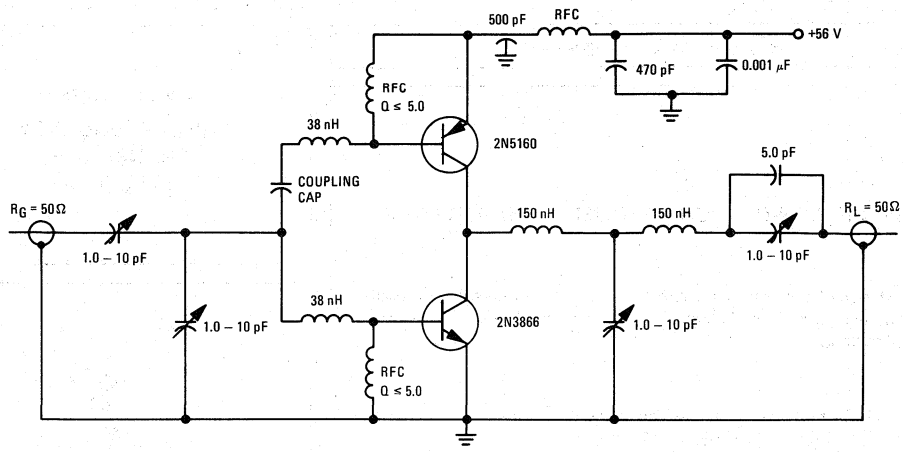
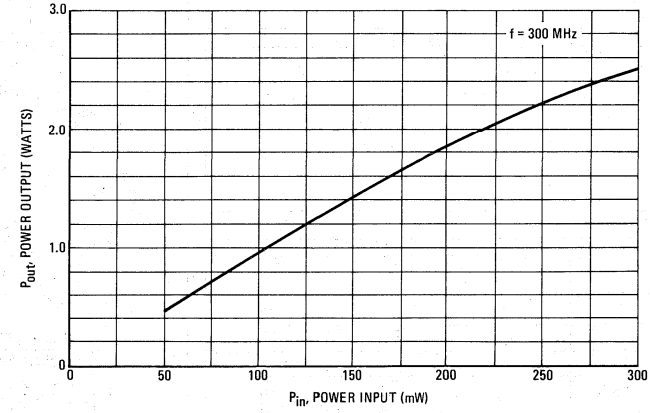


FIGURE 9 – COMPLEMENTARY CIRCUIT – POWER OUTPUT versus POWER INPUT



2N5179

The RF Line

4.5 dB @ 200 MHz

HIGH FREQUENCY TRANSISTOR

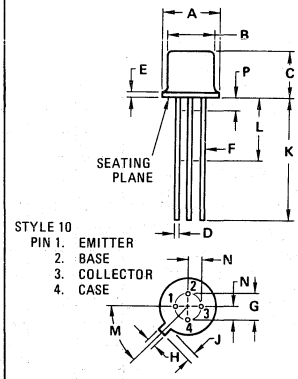
NPN SILICON

NPN SILICON RF HIGH FREQUENCY TRANSISTOR

. . . designed primarily for use in high-gain, low-noise amplifier, oscillator, and mixer applications. Can also be used in UHF converter applications.

- High Current-Gain – Bandwidth Product – f_T = 1.4 GHz (Typ) @ I_C = 10 mAdc
- Low Collector-Base Time Constant – $r_b'C_c$ = 14 ps (Max) @ I_E = 2.0 mAdc
- Characterized with Scattering Parameters
- Low Noise Figure – NF = 4.5 dB (Max) @ f = 200 MHz





DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

CASE 20-03
TO-72

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage Applicable 1.0 to 20 mAdc	V_{CEO}	12	Vdc
Collector-Base Voltage	V_{CB}	20	Vdc
Emitter-Base Voltage	V_{EB}	2.5	Vdc
Collector Current	I_C	50	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	200 1.14	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 1.71	mW mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.

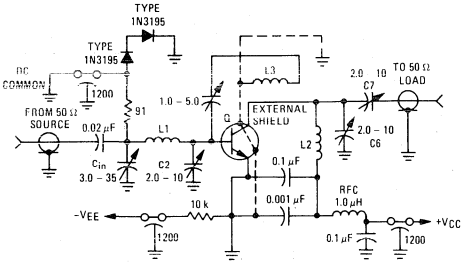
*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I_C = 3.0 mAdc, I_B = 0)	$V_{CEO(sus)}$	12	–	Vdc
Collector-Base Breakdown Voltage (I_C = 0.001 mAdc, I_E = 0)	$V_{(BR)CBO}$	20	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.01 mAdc, I_C = 0)	$V_{(BR)EBO}$	2.5	–	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0) (V_{CB} = 15 Vdc, I_E = 0, T_A = 150°C)	I_{CBO}	– –	0.02 1.0	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 3.0 mAdc, V_{CE} = 1.0 Vdc)	h_{FE}	25	250	–
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{CE(sat)}$	–	0.4	Vdc
Base-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{BE(sat)}$	–	1.0	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product ① (I_C = 5.0 mAdc, V_{CE} = 6.0 Vdc, f = 100 MHz)	f_T	900	2000	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 to 1.0 MHz)	C_{cb}	–	1.0	pF
Small-Signal Current Gain (I_C = 2.0 mAdc, V_{CE} = 6.0 Vdc, f = 1.0 kHz)	h_{fe}	25	300	–
Collector-Base Time Constant (I_E = 2.0 mAdc, V_{CB} = 6.0 Vdc, f = 31.9 MHz)	$r_b' C_c$	3.0	14	ps
Noise Figure (See Figure 1) (I_C = 1.5 mAdc, V_{CE} = 6.0 Vdc, R_S = 50 ohms, f = 200 MHz)	NF	–	4.5	dB
FUNCTIONAL TEST				
Common-Emitter Amplifier Power Gain (See Figure 1) (V_{CE} = 6.0 Vdc, I_C = 5.0 mAdc, f = 200 MHz)	G_{pe}	15	–	dB
Power Output (See Figure 2) (V_{CB} = 10 Vdc, I_E = 12 mAdc, f≥500 MHz)	P_{out}	20	–	mW

*Indicates JEDEC Registered Values.

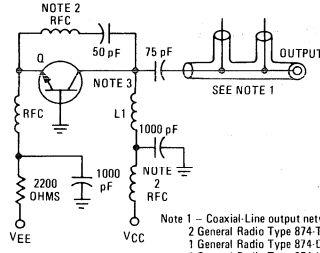
① f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

FIGURE 1 – 200 MHz AMPLIFIER POWER GAIN AND NOISE FIGURE CIRCUIT



L1 1-3/4 Turns, #18 AWG, 0.5" L, 0.5" Diameter
L2 2 Turns, #16 AWG, 0.5" L, 0.5" Diameter
L3 2 Turns, #13 AWG, 0.25" L, 0.5" Diameter (Position 1/4" from L2)

FIGURE 2 – 500 MHz OSCILLATOR CIRCUIT



Note 1 – Coaxial-Line output network consisting of:
2 General Radio Type 874-TEE or equivalent
1 General Radio Type 874-D20 Adjustable Stub or equivalent
1 General Radio Type 874-LA Adjustable Line or equivalent
1 General Radio Type 874-WN3 Short-circuit termination or equivalent
Note 2 – RFC = 0.2 μH Ohmite #2-460 or equivalent
Note 3 – Lead Number 4 (case) floating
L1 – 2 turns #16 AWG wire, 3/8 inch OD, 1-1/4 inch long
Q = 2N5179

FIGURE 3 – NOISE FIGURE versus FREQUENCY

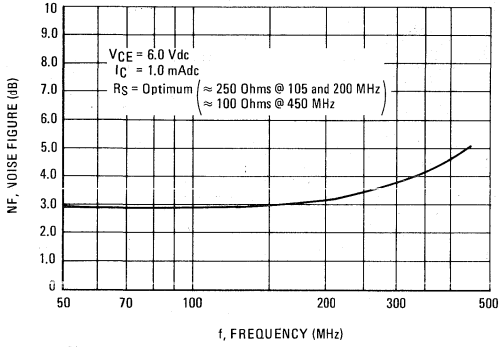


FIGURE 4 – NOISE FIGURE versus SOURCE RESISTANCE and COLLECTOR CURRENT

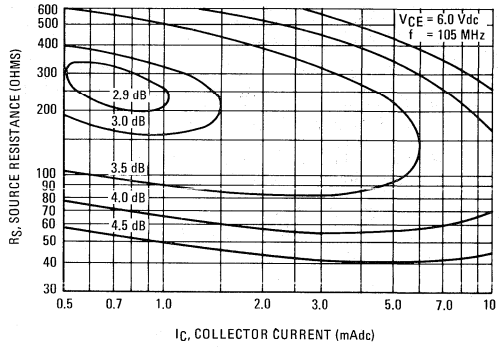


FIGURE 5 – NOISE FIGURE versus SOURCE RESISTANCE and COLLECTOR CURRENT

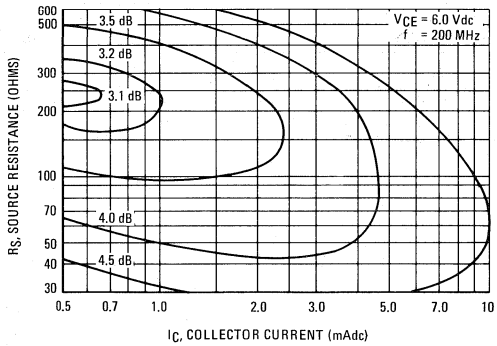


FIGURE 6 – CURRENT-GAIN-BANDWIDTH PRODUCT

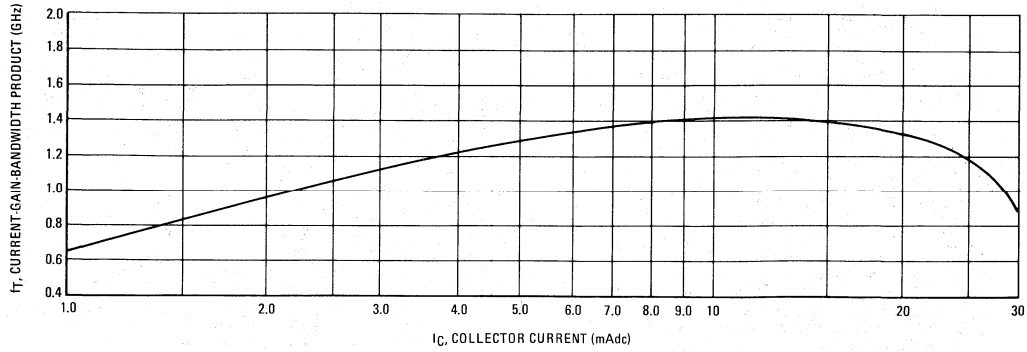


FIGURE 7 – INPUT ADMITTANCE versus FREQUENCY

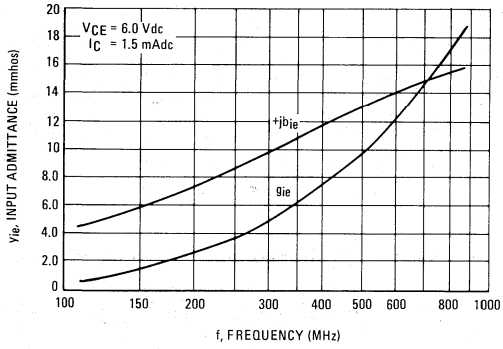


FIGURE 8 – OUTPUT ADMITTANCE versus FREQUENCY

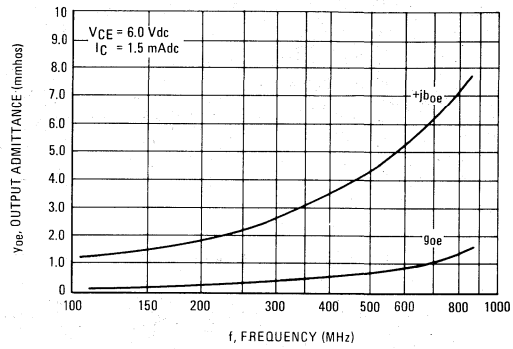


FIGURE 9 – FORWARD TRANSFER ADMITTANCE versus FREQUENCY

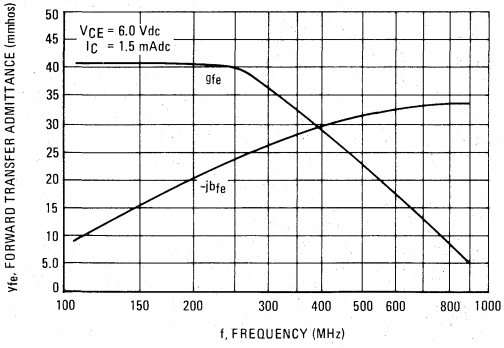


FIGURE 10 – REVERSE TRANSFER ADMITTANCE versus FREQUENCY

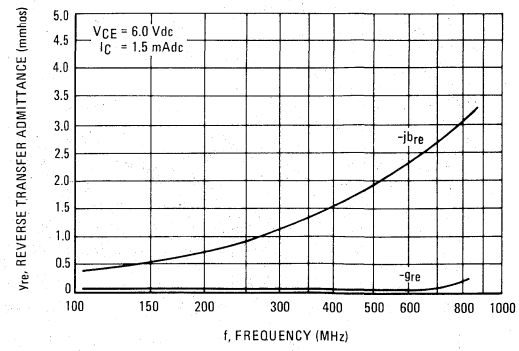


FIGURE 11– S_{11}, INPUT REFLECTION COEFFICIENT

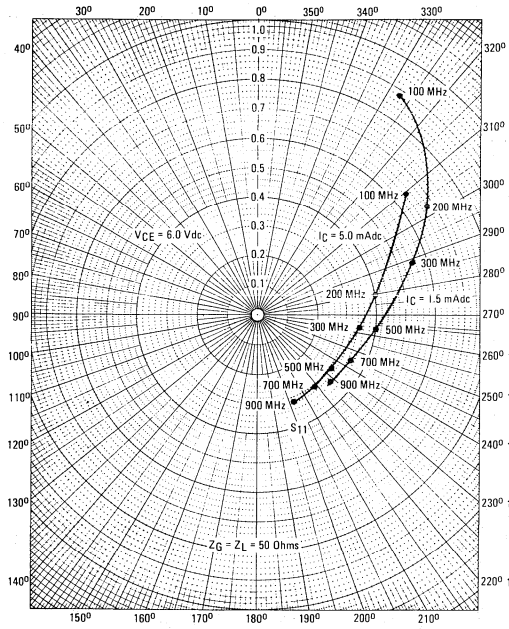


FIGURE 12 – S_{22}, OUTPUT REFLECTION COEFFICIENT

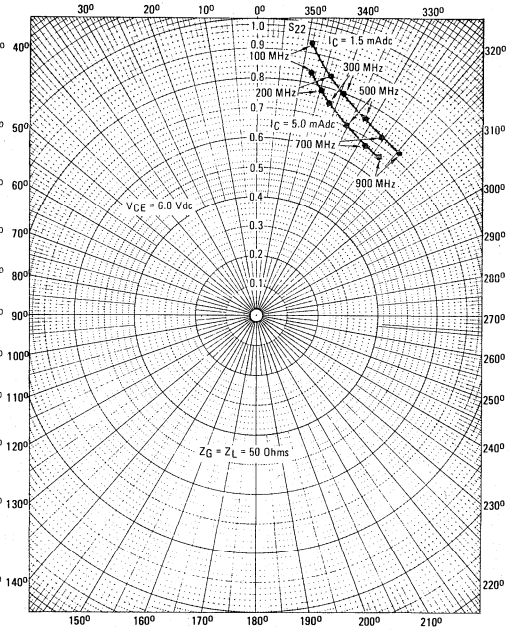


FIGURE 13 – S_{12}, REVERSE TRANSMISSION COEFFICIENT

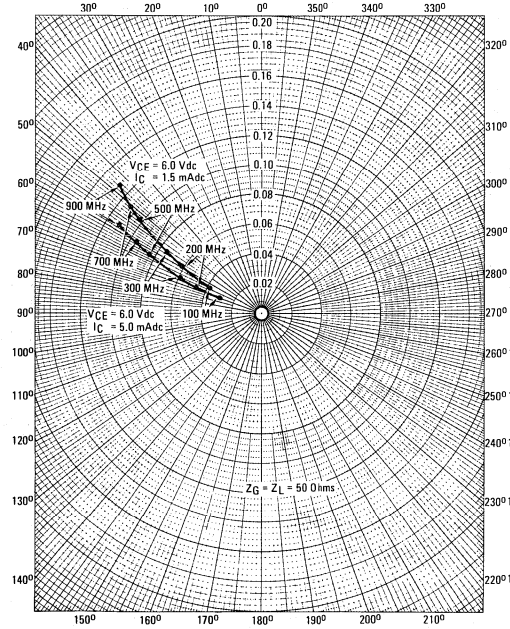


FIGURE 14 – S_{21}, FORWARD TRANSMISSION COEFFICIENT

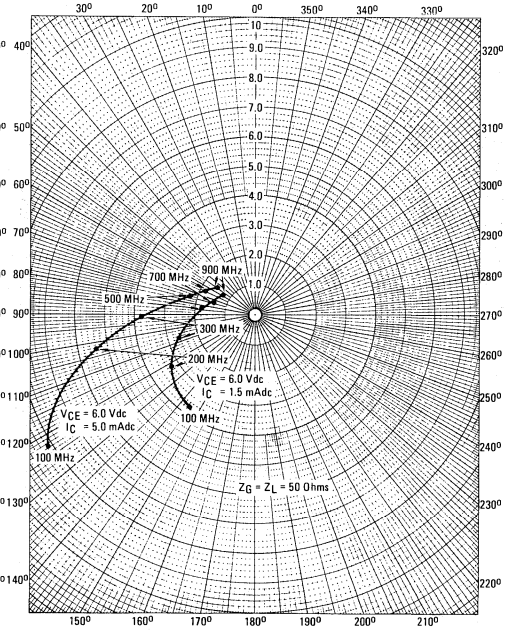
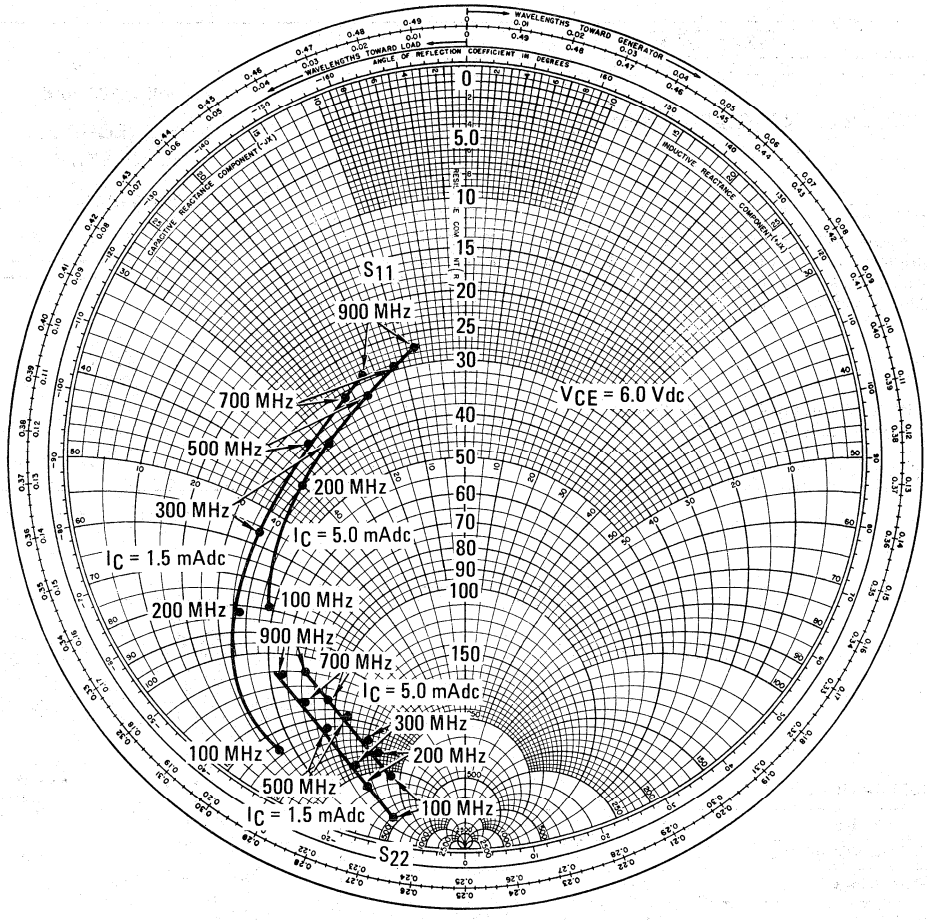


FIGURE 15 – S_{11}, INPUT REFLECTION COEFFICIENT AND S_{22}, OUTPUT REFLECTION COEFFICIENT



2N5583

The RF Line

PNP SILICON HIGH-FREQUENCY TRANSISTOR

. . . designed for applications in high frequency amplifiers and non-saturated switching circuits. High gain-bandwidth product characteristic provides excellent performance in a variety of small signal and linear amplifier applications.

- High Current-Gain—Bandwidth Product — f_T = 1300 (Min) @ I_C = 100 mAdc
- Low Collector-Base Time Constant — $r_b'C_C$ = 8.0 ps (Typ) @ I_C = 50 mAdc

1.3 GHz @ 100 mAdc

HIGH-FREQUENCY TRANSISTOR

PNP SILICON

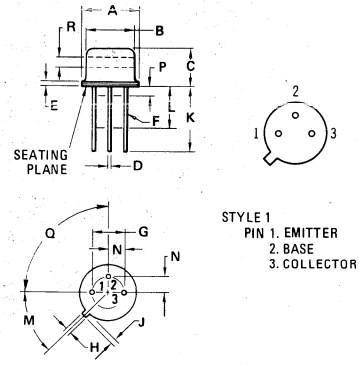


3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Collector-Emitter Voltage	V_{CEO}	30	Vdc
*Collector-Base Voltage	V_{CB}	30	Vdc
*Emitter-Base Voltage	V_{EB}	3.0	Vdc
*Collector Current — Continuous	I_C	500	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 5.71	Watt mW/°C
*Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	5.0 28.6	Watts mW/°C
*Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO-39

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Figure No.	Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**						
Collector-Emitter Breakdown Voltage (Note 1) (I_C = 10 mAdc, I_B = 0)	–	$V_{(BR)CEO}$	30	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	–	$V_{(BR)CBO}$	30	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	–	$V_{(BR)EBO}$	3.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)	4	I_{CBO}	–	–	50	nAdc
Emitter Cutoff Current (V_{EB} = 2.0 Vdc, I_C = 0)	–	I_{EBO}	–	–	0.5	μAdc
***ON CHARACTERISTICS**						
DC Current Gain (Note 1)	1	h_{FE}				–
(I_C = 40 mAdc, V_{CE} = 2.0 Vdc)			20	40	–	
(I_C = 100 mAdc, V_{CE} = 2.0 Vdc)			25	40	100	
(I_C = 300 mAdc, V_{CE} = 5.0 Vdc)			15	22	–	
Collector-Emitter Saturation Voltage (Note 1) (I_C = 100 mAdc, I_B = 10 mAdc)	2,3	$V_{CE(sat)}$	–	0.6	0.8	Vdc
Base-Emitter On Voltage (Note 1) (I_C = 100 mAdc, V_{CE} = 2.0 Vdc)	3	$V_{BE(on)}$	–	0.84	1.8	Vdc
SMALL-SIGNAL CHARACTERISTICS						
*Current-Gain—Bandwidth Product	7	f_T				MHz
(I_C = 40 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)			1000	1300	–	
(I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)			1300	1500	–	
*Collector-Base Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 100 kHz)	5	C_{cb}	–	2.5	5.0	pF
*Emitter-Base Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 100 kHz)	5	C_{eb}	–	18	35	pF
Collector-Base Time Constant (I_C = 50 mAdc, V_{CB} = 10 Vdc, f = 63.6 MHz)	8	$r_b'C_c$	–	8.0	–	ps
SWITCHING CHARACTERISTICS						
Delay Time	9,10	t_d	–	1.0	–	ns
Rise Time	9,10	t_r	–	2.1	–	ns
Fall Time	9,10	t_f	–	1.8	–	ns

(V_{CC} = 31.4 Vdc, I_C = 150 mAdc, R_C = 160 Ohms, R_E = 26.6 Ohms)

*Indicates JEDEC Registered Data.
Note 1: Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2.0%.

FIGURE 1 – DC CURRENT GAIN

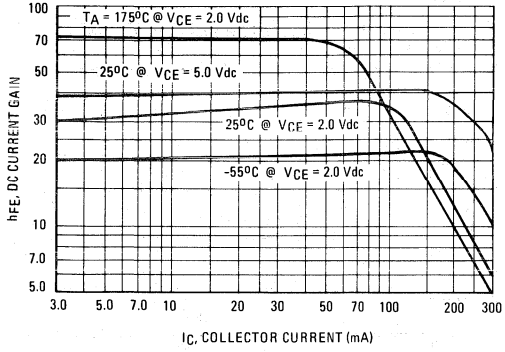


FIGURE 2 – COLLECTOR SATURATION REGION

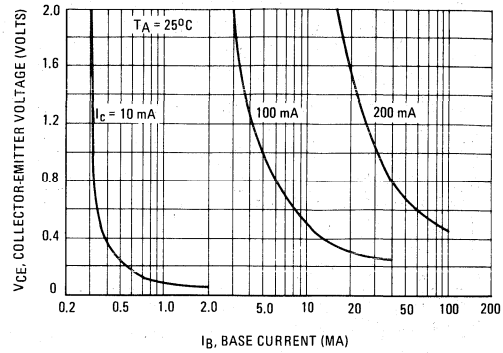


FIGURE 3 – "ON" VOLTAGES

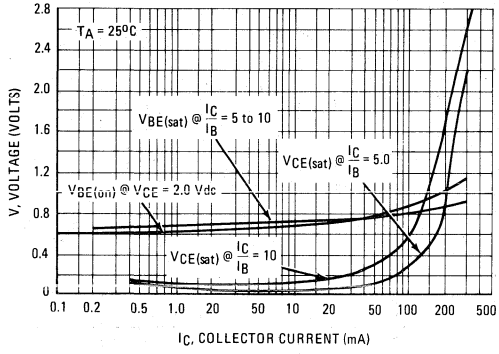


FIGURE 4 – COLLECTOR CURRENT versus BASE VOLTAGE

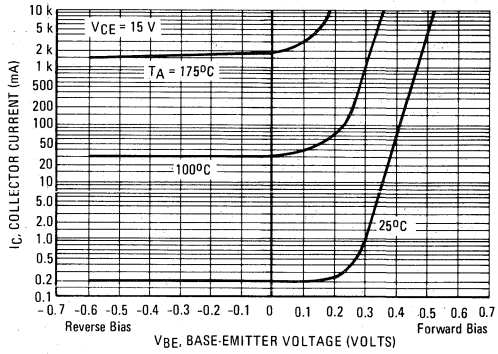


FIGURE 5 – CAPACITANCES

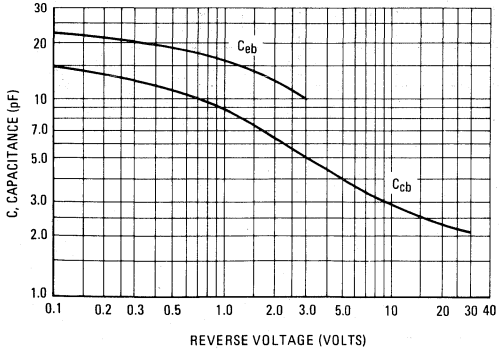


FIGURE 6 – TEMPERATURE COEFFICIENTS

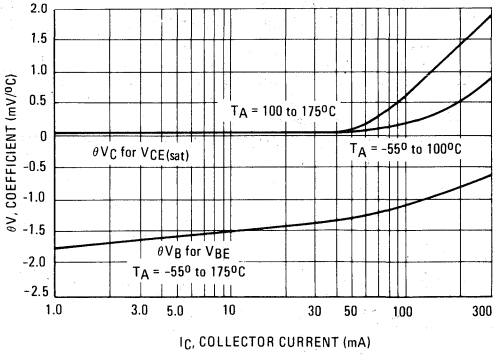


FIGURE 7 – CURRENT-GAIN–BANDWIDTH PRODUCT

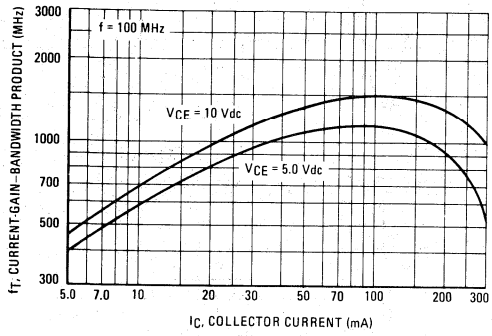


FIGURE 8 – COLLECTOR-BASE TIME CONSTANT

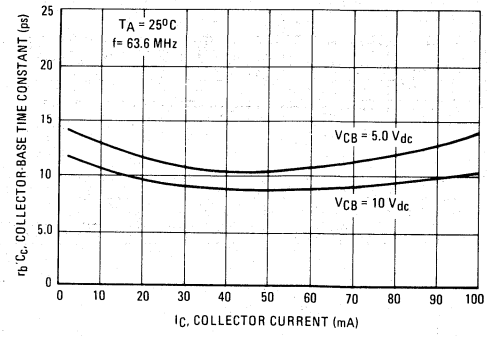


FIGURE 9 – SWITCHING TIMES

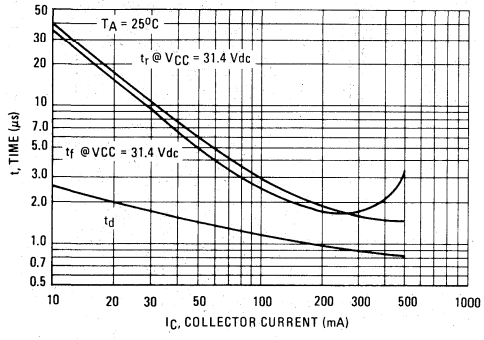
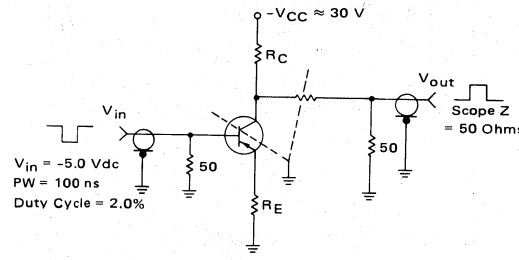


FIGURE 10 – SWITCHING TIMES TEST CIRCUIT



IC mA	RC Ohms	RE Ohms	VCC Volts
50	526	80	34.4
150	160	26.6	31.4
300	78	13.3	30.6
500	46.5	8.0	30.3

2N5641

The RF Line

7.0 W – 175 MHz

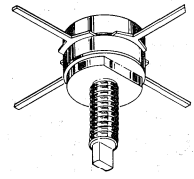
RF POWER
TRANSISTOR

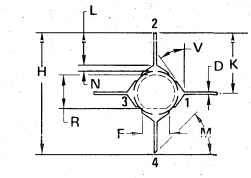
NPN SILICON

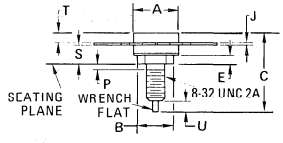
NPN SILICON RF POWER TRANSISTOR

. . . designed primarily for wideband large-signal amplifier stages in the 125-175 MHz frequency range.

- Specified 28 Volt, 175 MHz Characteristics –
  Output Power = 7.0 Watts
  Minimum Gain = 8.4 dB
  Efficiency = 60%
- Characterized from 125 to 175 MHz
- Includes Series Equivalent Impedances







STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

NOTE:
1. DIM "N" IS FROM DIA "A" TO ANGLE "V"

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	17.63	19.46	0.694	0.766
D	0.64	0.89	0.025	0.035
E	1.78	2.03	0.070	0.080
F	5.59	5.84	0.220	0.230
H	26.16	27.69	1.030	1.090
J	0.10	0.15	0.004	0.006
K	13.08	13.84	0.515	0.545
L	7.11	7.37	0.280	0.290
M	40°	50°	40°	50°
N	1.27	1.52	0.050	0.060
P		1.27		0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.16	2.41	0.085	0.095
U	2.54	3.30	0.100	0.130
V	10°	20°	10°	20°

CASE 144B-03

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	35	Vdc
Collector-Base Voltage	V_{CB}	65	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current – Continuous	I_C	1.0	Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	15 86	Watts mW/^oC
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	^oC

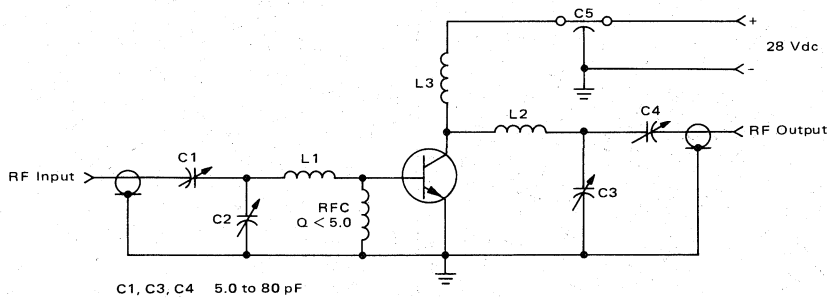
*Indicates JEDEC Registered Data.

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (Note 1) (I_C = 200 mAdc, I_B = 0)	$V_{(BR)CEO}$	35	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 200 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	65	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0	–	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 30 Vdc, I_E = 0, f = 0.1 to 1.0 MHz)	C_{ob}	–	8.5	15	pF
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (Figure 1) (P_{out} = 7.0 Watts, V_{CE} = 28 Vdc, f = 175 MHz)	G_{PE}	8.4	12.5	–	dB
Collector Efficiency (Figure 1) (P_{out} = 7.0 Watts, V_{CE} = 28 Vdc, f = 175 MHz)	η	60	–	–	%

Note 1: Pulsed through 25 mH inductor.
*Indicates JEDEC Registered Data.

FIGURE 1 – 175 MHz TEST CIRCUIT SCHEMATIC



C1, C3, C4	5.0 to 80 pF
C2	9.0 - 180 pF
C5	0.1 μF
L1	1-1/4 Straight #14 AWG
L2	3 Turns #16 AWG, 14" I.D.
L3	0.22 μH

FIGURE 2 – OUTPUT POWER versus FREQUENCY

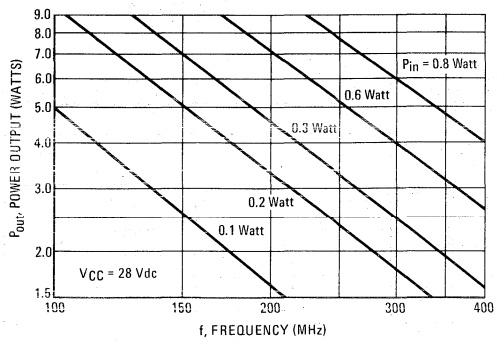


FIGURE 3 – OUTPUT POWER versus FREQUENCY

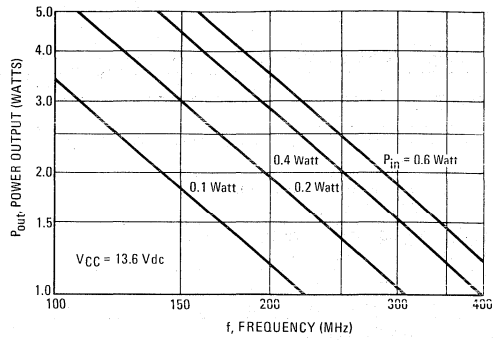
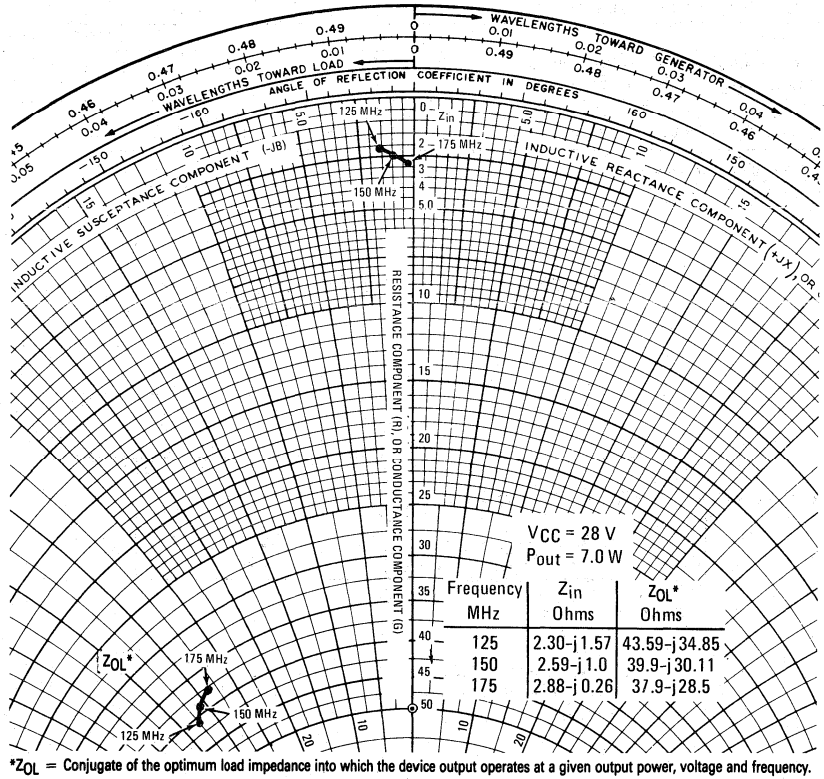


FIGURE 4 – SERIES EQUIVALENT IMPEDANCE



Frequency MHz	Z_{in} Ohms	Z_{OL}* Ohms
125	2.30-j1.57	43.59-j34.85
150	2.59-j1.0	39.9-j30.11
175	2.88-j0.26	37.9-j28.5

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

2N5642

The RF Line

20 W – 175 MHz

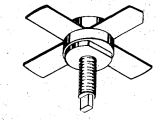
RF POWER TRANSISTOR

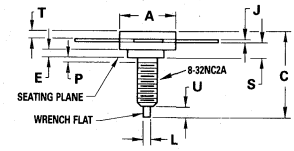
NPN SILICON

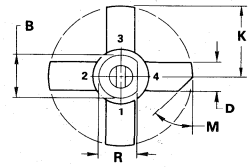
NPN SILICON RF POWER TRANSISTOR

. . . designed primarily for wideband large-signal amplifier stages in the 125-175 MHz frequency range.

- Specified 28 Volt, 175 MHz Characteristics –
  Output Power = 20 Watts
  Minimum Gain = 8.2 dB
  Efficiency = 60%
- Characterized from 125 to 175 MHz
- Includes Series Equivalent Impedances







STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	17.02	20.07	0.670	0.790
D	5.46	5.97	0.215	0.235
E	1.78	→	0.070	—
J	0.08	0.18	0.003	0.007
K	12.45	—	0.490	—
L	1.40	1.78	0.055	0.070
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.11	2.54	0.083	0.100
U	2.49	3.35	0.098	0.132

CASE 145A-09

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	35	Vdc
Collector-Base Voltage	V_{CB}	65	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current — Continuous	I_C	3.0	Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	30 171	Watts $mW/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	^oC

*Indicates JEDEC Registered Data.

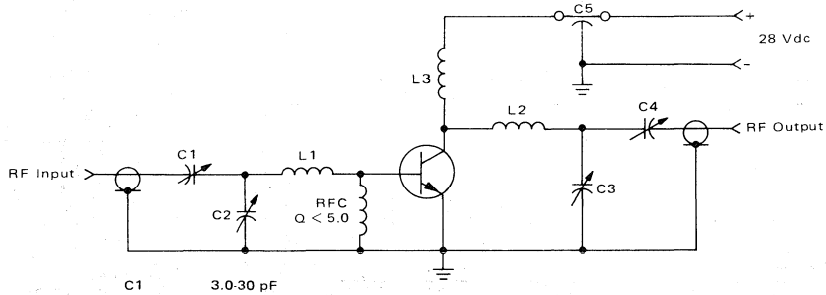
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (Note 1) (I_C = 200 mAdc, I_B = 0)	$V_{(BR)CEO}$	35	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 200 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	65	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 200 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0	–	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 30 Vdc, I_E = 0, f = 0.1 to 1.0 MHz)	C_{ob}	–	22	35	pF
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (Figure 1) (P_{out} = 20 Watts, V_{CE} = 28 Vdc, f = 175 MHz)	G_{PE}	8.2	10.2	–	dB
Collector Efficiency (Figure 1) (P_{out} = 20 Watts, V_{CE} = 28 Vdc, f = 175 MHz)	η	60	–	–	%

Note 1: Pulsed through 25 mH inductor.
*Indicates JEDEC Registered Data.

3

FIGURE 1 – 175 MHz TEST CIRCUIT SCHEMATIC



C1	3.0-30 pF
C2, C3, C4	9.0-180 pF
C5	0.1 μF
L1	1" Straight #14 AWG
L2	1 Turn #16 AWG, 1/4" I.D.
L3	0.22 μH

FIGURE 2 – OUTPUT POWER versus FREQUENCY

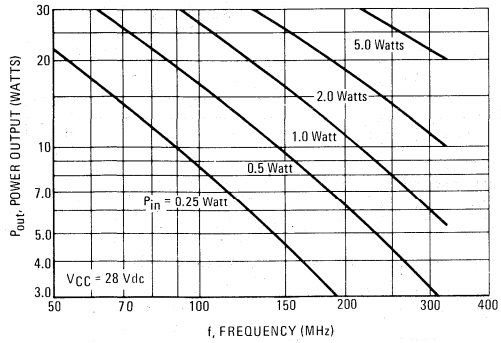


FIGURE 3 – OUTPUT POWER versus FREQUENCY

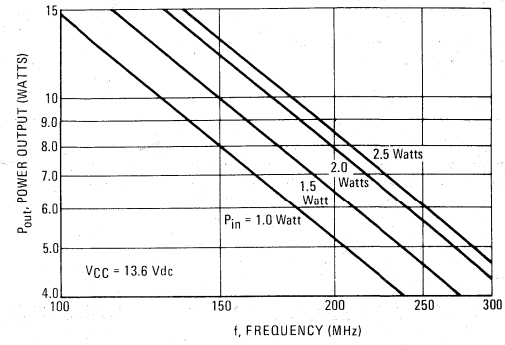
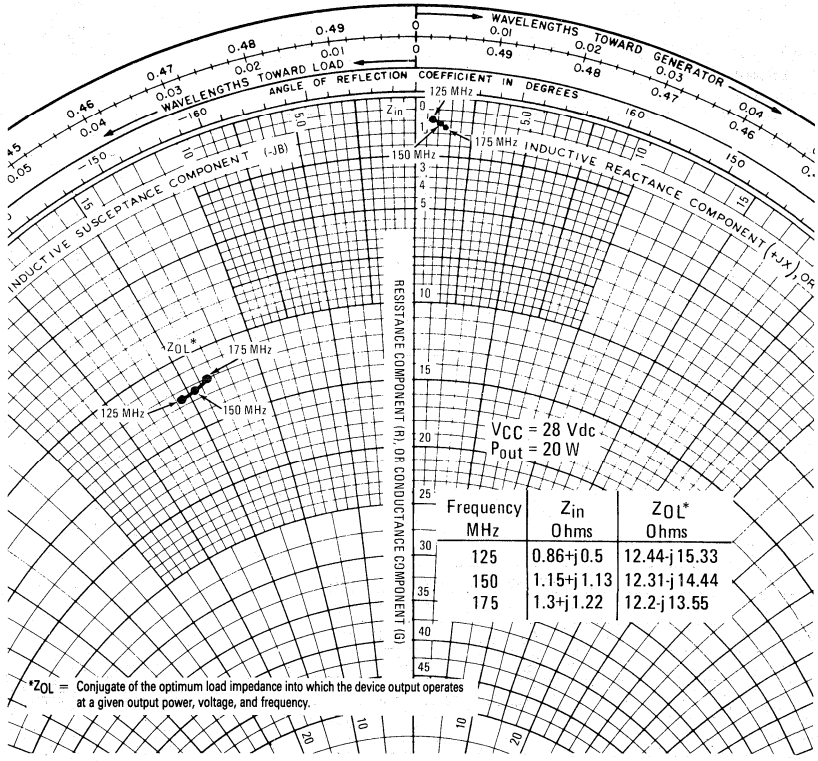


FIGURE 4 – SERIES EQUIVALENT IMPEDANCE



Frequency MHz	Z_{in} Ohms	Z_{OL}^* Ohms
125	0.86+j0.5	12.44-j15.33
150	1.15+j1.13	12.31-j14.44
175	1.3+j1.22	12.2-j13.55

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

2N5643

The RF Line

40 W – 175 MHz

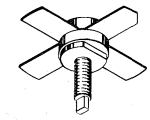
RF POWER
TRANSISTOR

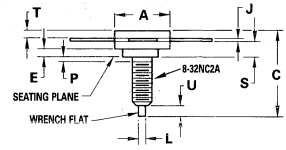
NPN SILICON

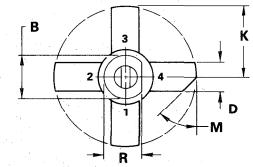
NPN SILICON RF POWER TRANSISTOR

. . . designed primarily for wideband large-signal amplifier stages in the 125-175 MHz frequency range.

- Specified 28 Volt, 175 MHz Characteristics –
  Output Power = 40 Watts
  Minimum Gain = 7.6 dB
  Efficiency = 60%
- Characterized from 125 to 175 MHz
- Includes Series Equivalent Impedances







STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	17.02	20.07	0.670	0.790
D	5.46	5.97	0.215	0.235
E	1.78	—	0.070	—
J	0.08	0.18	0.003	0.007
K	12.45	—	0.490	—
L	1.40	1.78	0.055	0.070
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.11	2.54	0.083	0.100
U	2.49	3.35	0.098	0.132

CASE 145A-09

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	35	Vdc
Collector-Base Voltage	V_{CB}	65	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current – Continuous	I_C	5.0	Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	60 342	Watts $mW/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	^oC

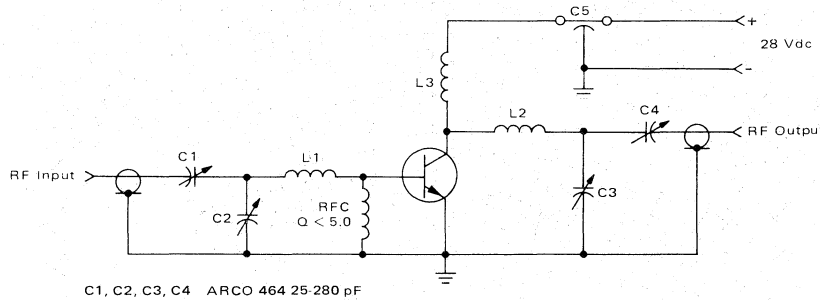
*Indicates JEDEC Registered Data.

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (Note 1) (I_C = 200 mAdc, I_B = 0)	$V_{(BR)CEO}$	35	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 200 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	65	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0	–	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 30 Vdc, I_E = 0, f = 0.1 to 1.0 MHz)	C_{ob}	–	45	65	pF
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (Figure 1) (P_{out} = 40 Watts, V_{CE} = 28 Vdc, f = 175 MHz)	G_{PE}	7.6	8.1	–	dB
Collector Efficiency (Figure 1) (P_{out} = 40 Watts, V_{CE} = 28 Vdc, f = 175 MHz)	η	60	–	–	%

Note 1: Pulsed through 25 mH inductor.
*Indicates JEDEC Registered Data.

FIGURE 1 – 175 MHz TEST CIRCUIT SCHEMATIC



C1, C2, C3, C4	ARCO 464 25-280 pF
C5	0.1 μF
L1	1" Straight #14 AWG
L2	1 Turn #16 AWG, 1/4" I.D.
L3	0.22 μH

3

FIGURE 2 – OUTPUT POWER versus FREQUENCY

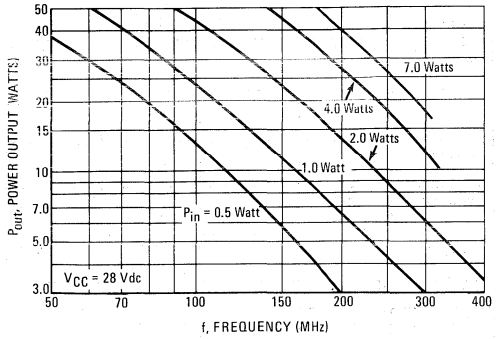


FIGURE 3 – OUTPUT POWER versus FREQUENCY

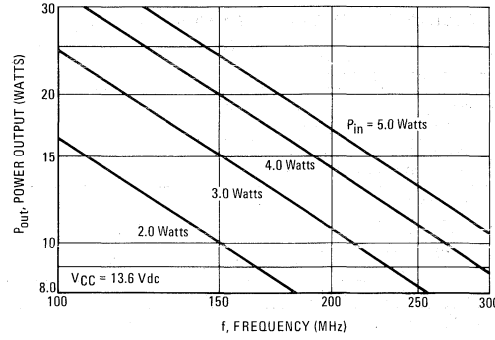
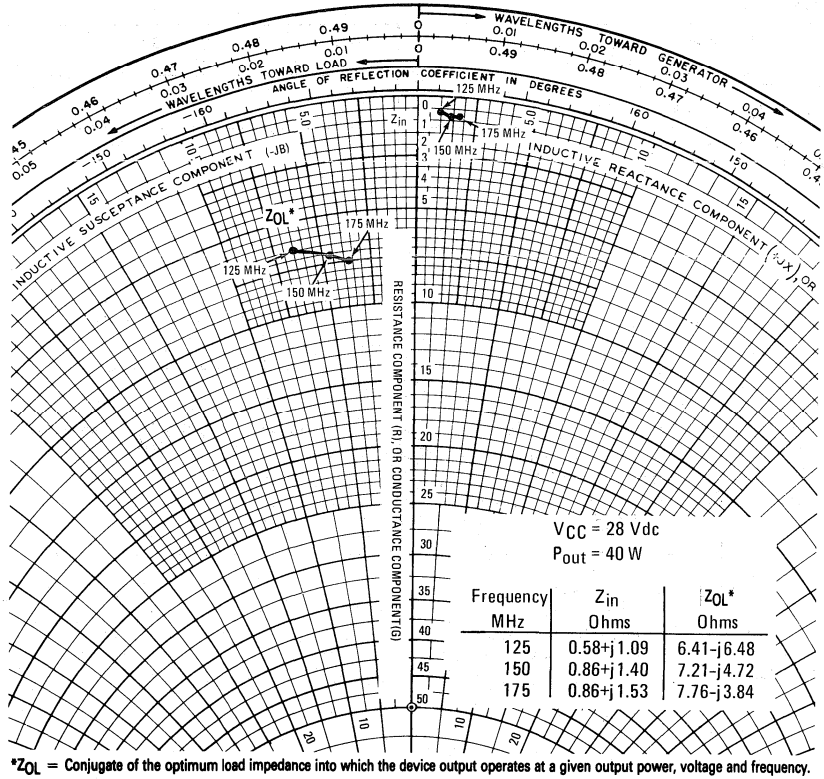


FIGURE 4 – SERIES EQUIVALENT IMPEDANCE



Frequency MHz	Z_{in} Ohms	Z_{OL}* Ohms
125	0.58+j1.09	6.41-j6.48
150	0.86+j1.40	7.21-j4.72
175	0.86+j1.53	7.76-j3.84

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

2N5835
2N5836
2N5837

The RF Line

NPN SILICON HIGH-FREQUENCY TRANSISTORS

. . . designed primarily for use in fact current-mode switching circuits in military and industrial equipment. Suitable for use in general high-frequency amplifier applications to 1.5 GHz.

- 2N5835 – 10 mAdc, 6.0 Vdc Characteristics
  f_T = 2.5 GHz (Min)
  $r_b'C_c$ = 5.0 ps (Typ)
  t_r = 250 ps (Typ)
- 2N5836 – 50 mAdc, 6.0 Vdc Characteristics –
  f_T = 2.0 GHz (Min)
  $r_b'C_c$ = 6.0 ps (Typ)
  t_r = 320 ps (Typ)
- 2N5837 – 100 mAdc, 3.0 Vdc Characteristics –
  f_T = 1.7 GHz (Min)
  $r_b'C_c$ = 6.0 ps (Typ)
  t_r = 650 ps (Typ)

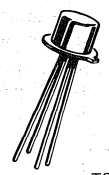
2.5 GHz @ 10 mAdc – 2N5835
2.0 GHz @ 50 mAdc – 2N5836
1.7 GHz @ 100 mAdc – 2N5837

HIGH FREQUENCY TRANSISTORS

NPN SILICON



TO-46
2N5836
2N5837



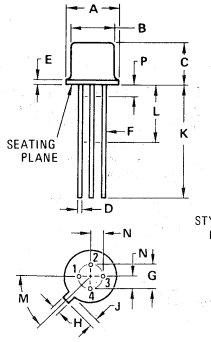
TO-72
2N5835

3

*MAXIMUM RATINGS

Rating	Symbol	2N5835	2N5836	2N5837	Unit
Collector-Emitter Voltage	V_{CEO}	10	10	5.0	Vdc
Collector-Base Voltage	V_{CBO}	15	15	10	Vdc
Emitter-Base Voltage	V_{EBO}	3.5	3.5	3.5	Vdc
Collector Current – Continuous	I_C	15	200	300	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	200 1.14	– –	– –	mW mW/°C
Total Device Dissipation @ T_C = 100°C **Derate above 100°C**	P_D	– –	**.75** **7.5**	**.75** **7.5**	Watts mW/°C
Storage Junction Temperature Range	T_{stg}	← -65 to +200 →			°C

*Indicates JEDEC Registered Data.

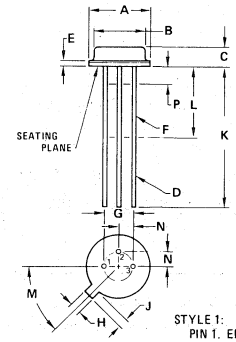


STYLE 10
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. CASE

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

CASE 20-03
TO-72



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	1.65	2.16	0.065	0.085
D	0.406	0.533	0.016	0.021
E	–	1.02	–	0.040
F	0.305	0.483	0.012	0.019
G	2.54 BSC		0.100 BSC	
H	0.914	1.17	0.036	0.046
J	0.711	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

All JEDEC dimensions and notes apply

CASE 26-03
TO-46

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

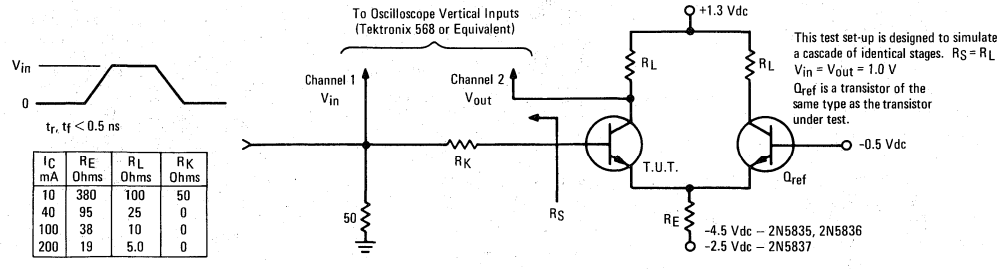
Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Base Breakdown Voltage		$V_{(BR)CBO}$				Vdc
(I_C = 10 μAdc, I_E = 0)	2N5835		15	–	–	
(I_C = 100 μAdc, I_E = 0)	2N5836		15	–	–	
	2N5837		10	–	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		$V_{(BR)EBO}$	3.5	–	–	Vdc
Collector Cutoff Current		I_{CBO}				μAdc
(V_{CB} = 7.5 Vdc, I_E = 0)	2N5835		–	–	0.01	
(V_{CB} = 10 Vdc, I_E = 0)	2N5836		–	–	10	
(V_{CB} = 5.0 Vdc, I_E = 0)	2N5837		–	–	10	
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)		I_{EBO}	–	–	100	μAdc
ON CHARACTERISTICS						
DC Current Gain		h_{FE}				–
(I_C = 10 mAdc, V_{CE} = 6.0 Vdc)	2N5835		25	–	–	
(I_C = 50 mAdc, V_{CE} = 6.0 Vdc)	2N5836		25	–	–	
(I_C = 100 mAdc, V_{CE} = 3.0 Vdc)	2N5837		25	–	–	
Base-Emitter On Voltage		$V_{BE(on)}$				Vdc
(I_C = 10 mAdc, V_{CE} = 6.0 Vdc)	2N5835		–	–	0.9	
(I_C = 50 mAdc, V_{CE} = 6.0 Vdc)	2N5836		–	–	0.9	
(I_C = 100 mAdc, V_{CE} = 3.0 Vdc)	2N5837		–	–	0.9	
DYNAMIC CHARACTERISTICS						
Current-Gain—Bandwidth Product ①		f_T				GHz
(I_C = 10 mAdc, V_{CE} = 6.0 Vdc, f = 200 MHz)	2N5835		2.5	–	–	
(I_C = 50 mAdc, V_{CE} = 6.0 Vdc, f = 200 MHz)	2N5836		2.0	–	–	
(I_C = 100 mAdc, V_{CE} = 3.0 Vdc, f = 200 MHz)	2N5837		1.7	–	–	
Collector-Base Capacitance		C_{cb}				pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 to 1.0 MHz)	2N5835		–	–	0.8	
	2N5836		–	–	3.5	
(V_{CB} = 5.0 Vdc, I_E = 0, f = 0.1 to 1.0 MHz)	2N5837		–	–	5.0	
Collector-Base Time Constant ②		$r_b'C_c$				ps
(I_C = 10 mAdc, V_{CE} = 6.0 Vdc, f = 63.6 MHz)	2N5835		–	5.0	–	
(I_C = 50 mAdc, V_{CE} = 6.0 Vdc, f = 63.6 MHz)	2N5836		–	6.0	–	
(I_C = 100 mAdc, V_{CE} = 3.0 Vdc, f = 63.6 MHz)	2N5837		–	6.0	–	
SWITCHING CHARACTERISTICS ②						
Rise Time (See Figure 1)	(I_C = 10 mAdc) 2N5835	t_r	–	250	–	ps
	(I_C = 40 mAdc) 2N5836		–	320	–	
	(I_C = 100 mAdc) 2N5837		–	650	–	

*Indicates JEDEC Registered Data

① f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

② Typical values shown in addition to JEDEC Registered Data.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT



I_C mA	R_E Ohms	R_L Ohms	R_K Ohms
10	380	100	50
40	95	25	0
100	38	10	0
200	19	5.0	0

FIGURE 2 – SWITCHING TIME

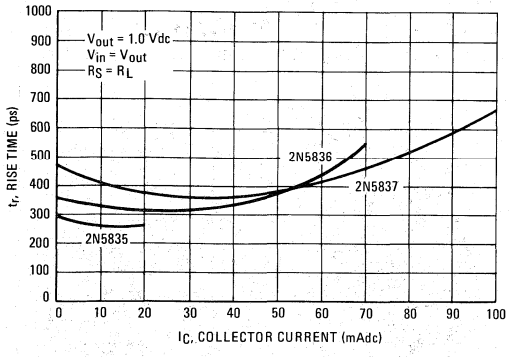


FIGURE 3 – CURRENT-GAIN–BANDWIDTH PRODUCT

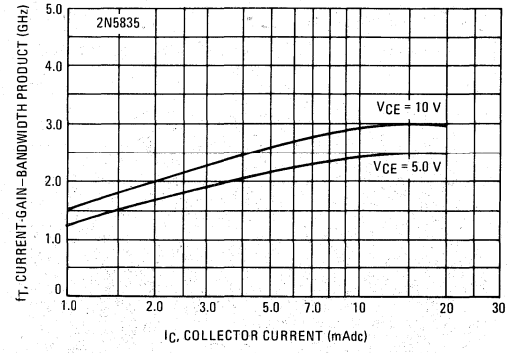


FIGURE 4 – CURRENT-GAIN–BANDWIDTH PRODUCT

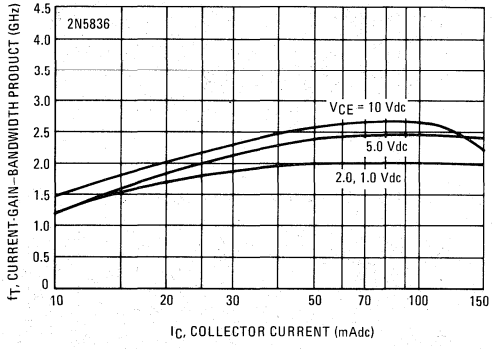


FIGURE 5 – CURRENT-GAIN–BANDWIDTH PRODUCT

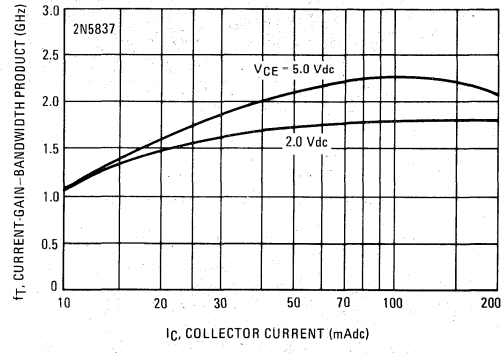


FIGURE 6 – COLLECTOR-BASE TIME CONSTANT

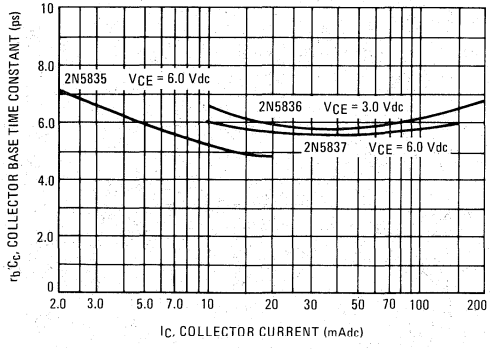
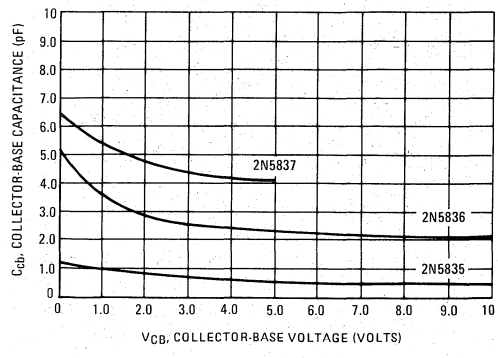


FIGURE 7 – COLLECTOR-BASE CAPACITANCE



3

2N5835 SCATTERING PARAMETERS
(I_C = 5.0 mAdc, V_{CE} = 6.0 Vdc, Z_G = Z_L = 50 Ohms)

FIGURE 8 – S_{11}, INPUT REFLECTION COEFFICIENT

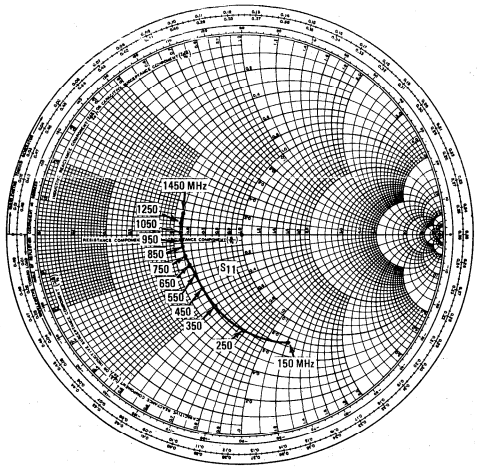


FIGURE 9 – S_{22}, OUTPUT REFLECTION COEFFICIENT

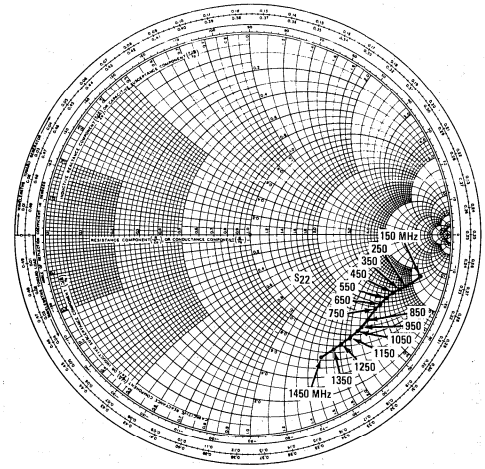


FIGURE 10 – S_{12}, REVERSE TRANSMISSION COEFFICIENT

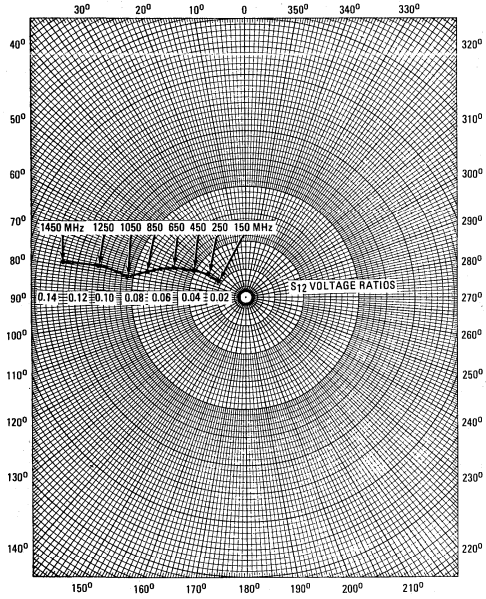
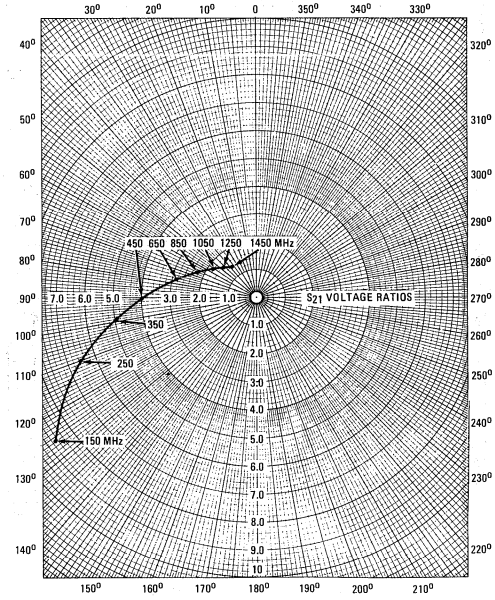


FIGURE 11 – S_{21}, FORWARD TRANSMISSION COEFFICIENT



2N5836 SCATTERING PARAMETERS

(I_C = 100 mAdc, V_{CE} = 10 Vdc, Z_G = Z_L = 50 Ohms)

FIGURE 12 – S_{11}, INPUT REFLECTION COEFFICIENT

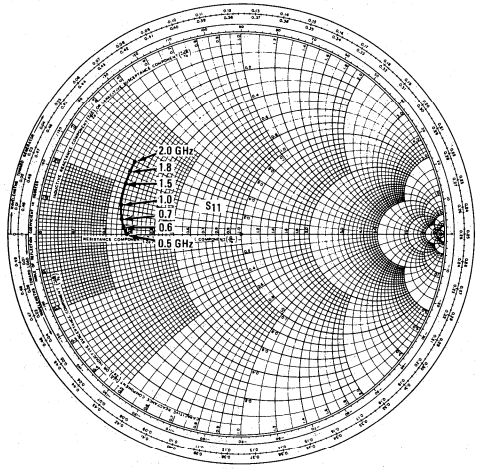


FIGURE 13 – S_{22}, OUTPUT REFLECTION COEFFICIENT

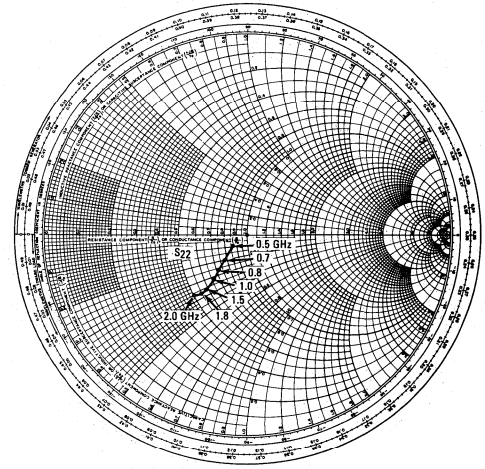


FIGURE 14 – S_{12}, REVERSE TRANSMISSION COEFFICIENT

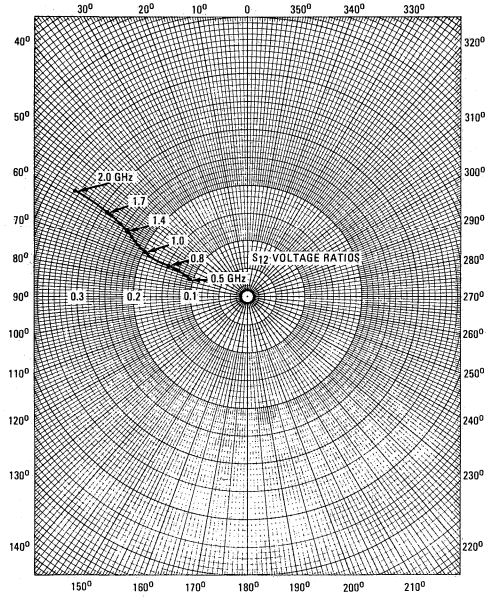
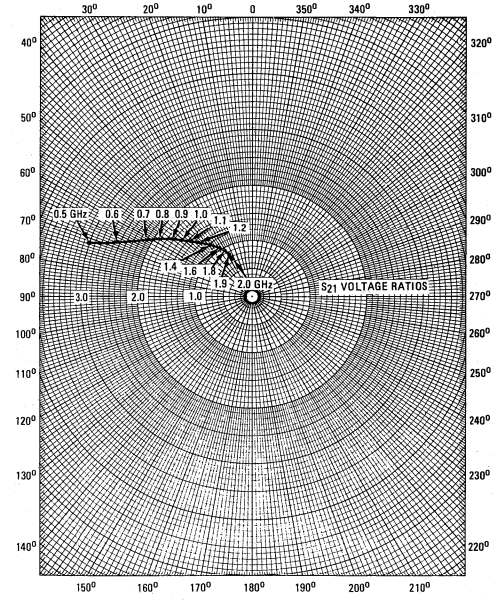


FIGURE 15 – S_{21}, FORWARD TRANSMISSION COEFFICIENT



3

2N5837 SCATTERING PARAMETERS

(I_C = 100 mAdc, V_{CE} = 3.0 Vdc, Z_G = Z_L = 50 Ohms)

FIGURE 16 – S_{11}, INPUT REFLECTION COEFFICIENT

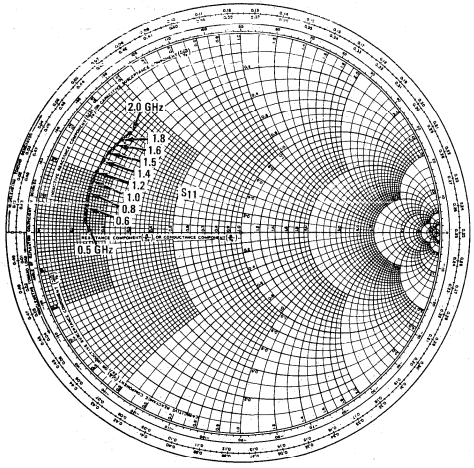


FIGURE 17 – S_{22}, OUTPUT REFLECTION COEFFICIENT

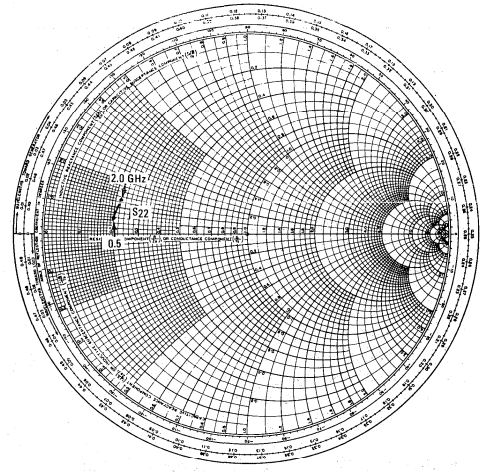


FIGURE 18 – S_{12}, REVERSE TRANSMISSION COEFFICIENT

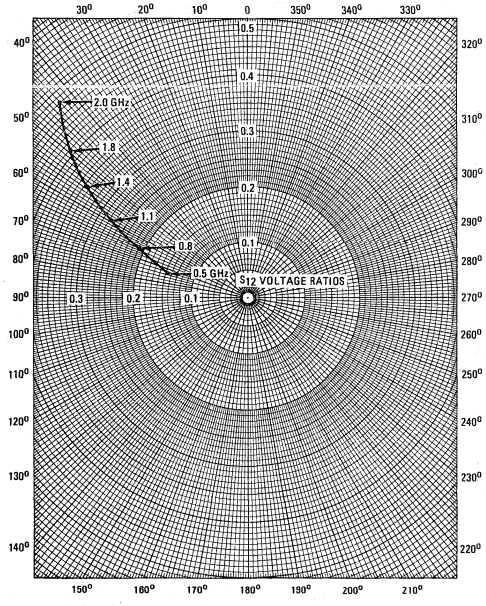
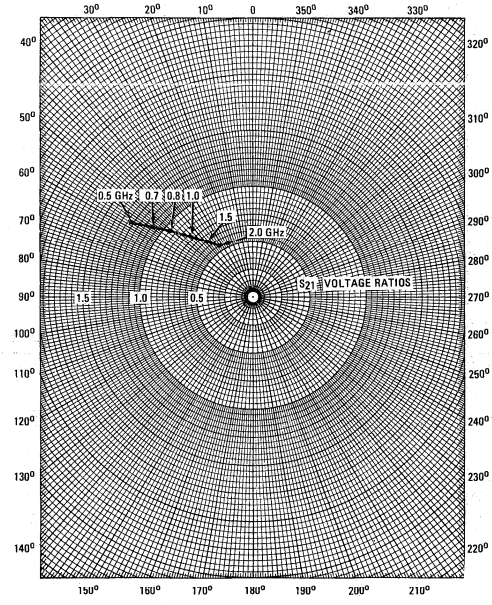


FIGURE 19 – S_{21}, FORWARD TRANSMISSION COEFFICIENT



2N5849

The RF Line

NPN SILICON RF POWER TRANSISTOR

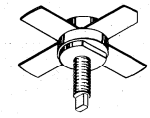
. . . designed primarily for use in large-signal amplifier output stages, the 2N5849 is intended for use in industrial communications equipment operating at frequencies to 80 MHz.

- Specified 12.5 Volt, 50 MHz Characteristics –
  Output Power = 40 Watts
  Minimum Gain = 7.5 dB
  Efficiency = 50%

40 W–50 MHz

RF POWER TRANSISTOR

NPN SILICON



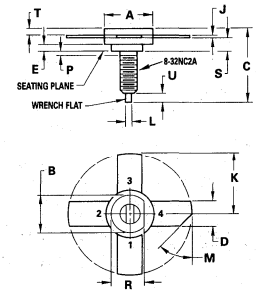
3

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	24	Vdc
Collector-Base Voltage	V_{CB}	48	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current — Continuous	I_C	7.0	Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	100 571	Watts mW/^oC
Storage Temperature Range	T_{stg}	–65 to +200	^oC

*Indicates JEDEC Registered Data.

This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF amplifier.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	17.02	20.07	0.670	0.790
D	5.46	5.97	0.215	0.235
E	1.78	—	0.070	—
J	0.08	0.18	0.003	0.007
K	12.45	—	0.490	—
L	1.40	1.78	0.055	0.070
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.11	2.54	0.083	0.100
U	2.49	3.35	0.098	0.132

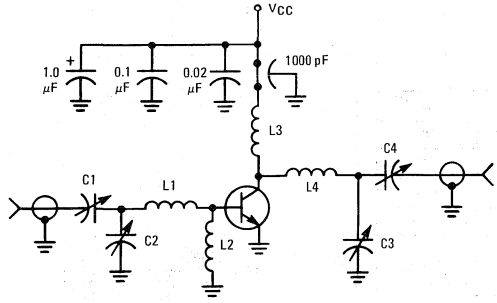
CASE 145A-09

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 200 mAdc, I_B = 0)	$V_{(BR)CEO}$	24	–	–	Vdc
Collector-Emitter Breakdown Voltage(1) (I_C = 100 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	48	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_A = +125°C)	I_{CES}	–	–	10	mAdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.4 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	3.0	–	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 0.1 to 1.0 MHz)	C_{ob}	–	180	230	pF
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (P_{out} = 40 W, V_{CC} = 12.5 Vdc, f = 50 MHz)	G_{PE}	7.5	–	–	dB
Collector Efficiency (P_{out} = 40 W, V_{CC} = 12.5 Vdc, f = 50 MHz)	η	50	–	–	%

*Indicates JEDEC Registered Data.
(1)Pulsed thru a 25 mH Inductor.

FIGURE 1 – 50 MHz POWER GAIN TEST CIRCUIT



C1 25-280 pF, Arco 464 or Equivalent
C2 80-480 pF, Arco 466 or Equivalent
C3 0-75 pF, Hammarlund MAPC 75 or Equivalent
C4 0-50 pF, Hammarlund MAPC 50 or Equivalent
L1 1 Turn #14 AWG 5/16" I.D.
L2 2-1/2 Turns #22 AWG on 3/8" Ferrite Bead
L3 18 Turns #18 AWG 3/8" I.D. 2 Layers, 9 Turns Each
L4 4 Turns #14 AWG 7/16" I.D. 7/16" Long

FIGURE 2 – POWER OUTPUT versus POWER INPUT

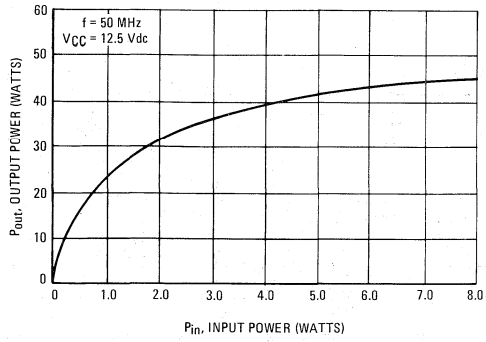


FIGURE 3 – POWER OUTPUT versus FREQUENCY

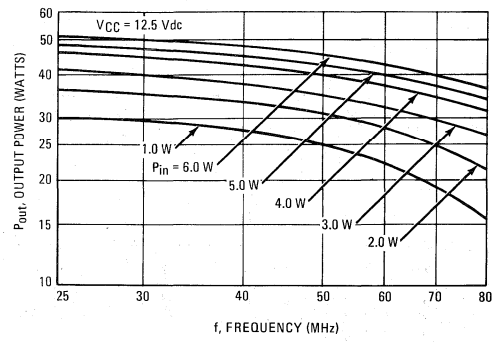


FIGURE 4 – PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

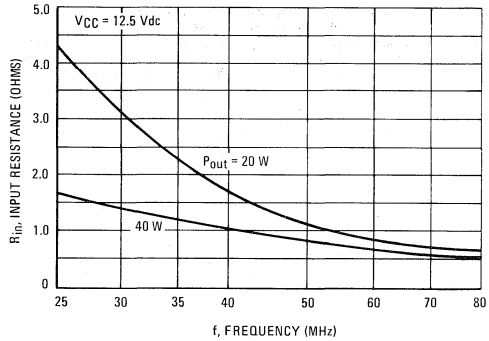


FIGURE 5 – PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

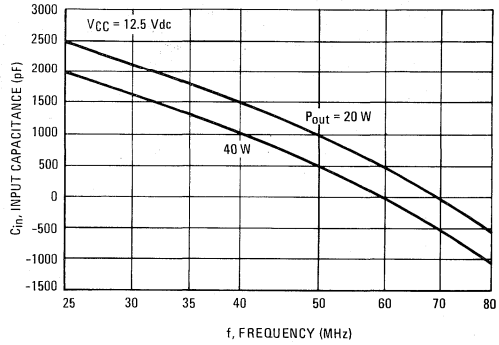


FIGURE 6 – PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY

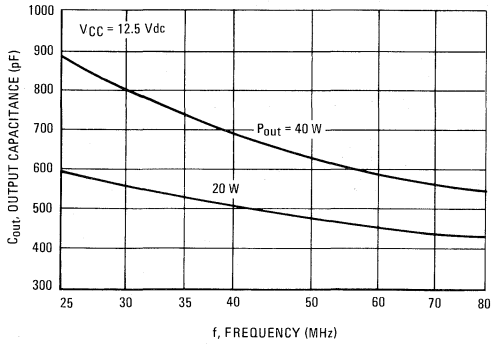
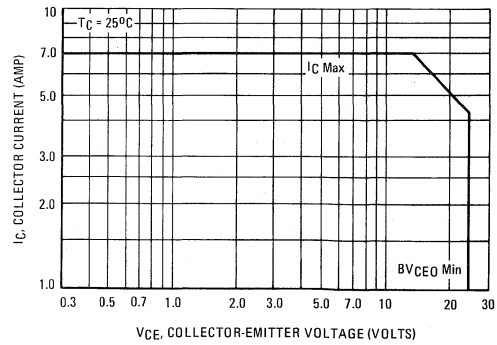
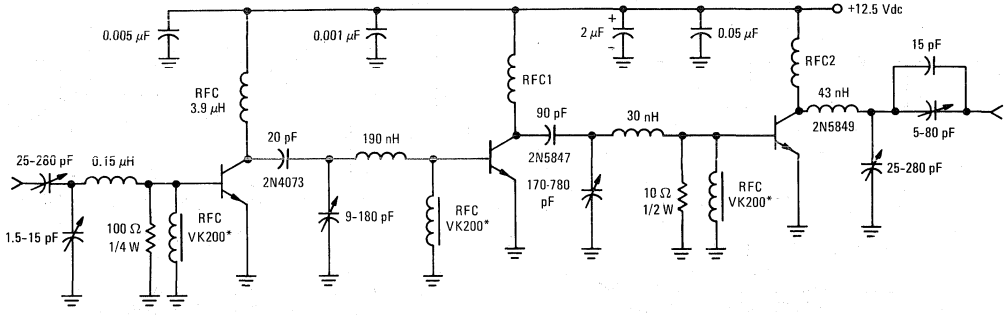


FIGURE 7 – DC SAFE OPERATING AREA



3

40 WATT, 50 MHz TRANSMITTER SCHEMATIC



P_O = 40 W
P_{in} = 20 mW
Overall Gain = 33 dB
Overall Efficiency = 59.2%

*Ferroxcube Part Number
RFC1 – 20 Turns #18 AWG, 3/16" I.D., 2 Layers, 10 Turns Each, Close Wound.
RFC2 – 18 Turns, #18 AWG, 3/16" I.D., 2 Layers, 9 Turns Each, Close Wound.

2N5943

The RF Line

NPN SILICON HIGH-FREQUENCY TRANSISTOR

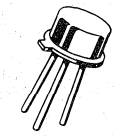
. . . designed specifically for broadband applications requiring low cross-modulation distortion and low-noise figure. Characterized for use in CATV applications.

- Low Noise Figure – @ f = 200 MHz
  NF (Narrowband) = 3.4 dB (Typ)
  NF (Broadband) = 6.8 dB (Typ)
- High Current-Gain – Bandwidth Product –
  f_T = 1200 MHz (Min) @ I_C = 50 mAdc
- Completely Characterized with s and y-Parameters

1.2 GHz – 50 mAdc

NPN SILICON HIGH-FREQUENCY TRANSISTOR

NPN SILICON

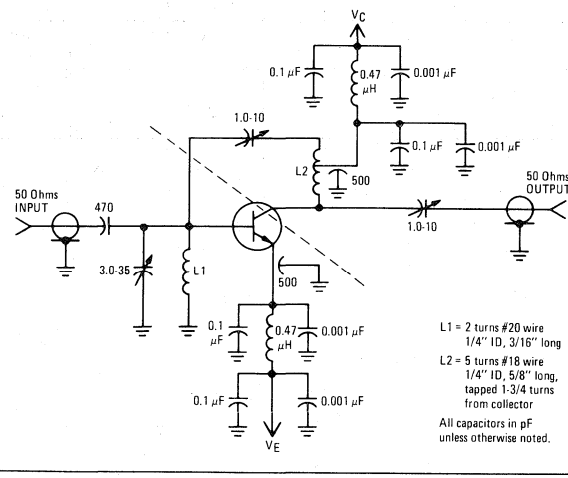


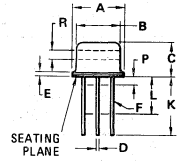
***MAXIMUM RATINGS**

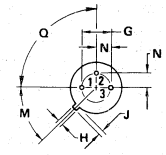
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	40	Vdc
Emitter-Base Voltage	V_{EBO}	3.5	Vdc
Collector Current – Continuous	I_C	400	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 5.7	Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	3.5 0.02	Watts W/°C*
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.

FIGURE 1 – NARROW-BAND TEST CIRCUIT







STYLE 1
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO-39

3

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	$V_{(BR)CBO}$	40	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	–	–	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0)	I_{CEO}	–	–	50	μAdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	10	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 50 mAdc, V_{CE} = 15 Vdc)	h_{FE}	25	–	300	–
Collector-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)	$V_{CE(sat)}$	–	0.15	0.2	Vdc
Base-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)	$V_{BE(sat)}$	–	0.88	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (Figure 2)	f_T				MHz
(I_C = 25 mAdc, V_{CE} = 15 Vdc, f = 200 MHz)		1000	1350	–	
(I_C = 50 mAdc, V_{CE} = 15 Vdc, f = 200 MHz)		1200	1550	2400	
(I_C = 100 mAdc, V_{CE} = 15 Vdc, f = 200 MHz)		1000	1425	–	
Collector-Base Capacitance (Figure 5) (V_{CB} = 30 Vdc, I_E = 0, f = 100 kHz)	C_{cb}	1.0	1.6	2.5	pF
Emitter-Base Capacitance (Figure 5) (V_{EB} = 0.5 Vdc, I_C = 0, f = 100 kHz)	C_{eb}	–	8.4	15	pF
Small-Signal Current Gain (I_C = 50 mAdc, V_{CE} = 15 Vdc, f = 1.0 kHz)	h_{fe}	25	–	350	–
Collector-Base Time Constant (I_E = 50 mAdc, V_{CB} = 15 Vdc, f = 31.8 MHz)	$r_b'C_c$	2.0	5.5	20	ps
Noise Figure	NF				dB
(I_C = 30 mAdc, V_{CE} = 15 Vdc, f = 200 MHz) (Figure 1)		–	3.4	–	
(I_C = 35 mAdc, V_{CE} = 15 Vdc, f = 200 MHz) (Figures 6, 11, 14) (1)		–	6.8	8.0	
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain	G_{pe}				dB
(I_C = 10 mAdc, V_{CE} = 15 Vdc, f = 200 MHz) (Figure 1)		–	11.4	–	
(I_C = 50 mAdc, V_{CE} = 15 Vdc, f = 250 MHz) (Figure 6)		7.0	7.6	–	
Intermodulation Distortion (Figure 7) (I_C = 50 mAdc, V_{CE} = 15 Vdc, V_{out} = +50 dBmV)	IM	–	–	-50	dB
Cross Modulation Distortion (Figure 8)	XM				dB
(I_C = 50 mAdc, V_{CE} = 15 Vdc, V_{out} = +40 dBmV)		–	-67	–	
(I_C = 50 mAdc, V_{CE} = 15 Vdc, V_{out} = +50 dBmV)		–	-45	-42	

*Indicates JEDEC Registered Data.

(1) Includes noise figure of post-amplifier and matching pad.

FIGURE 2 – CURRENT-GAIN – BANDWIDTH PRODUCT

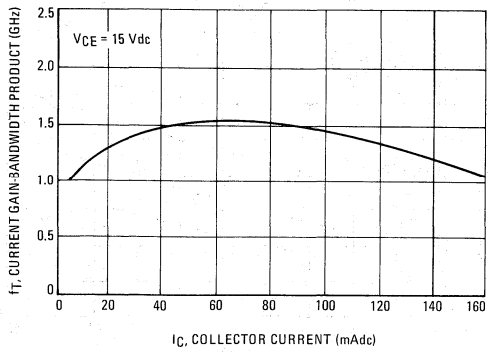


FIGURE 3 – COLLECTOR-BASE TIME CONSTANT

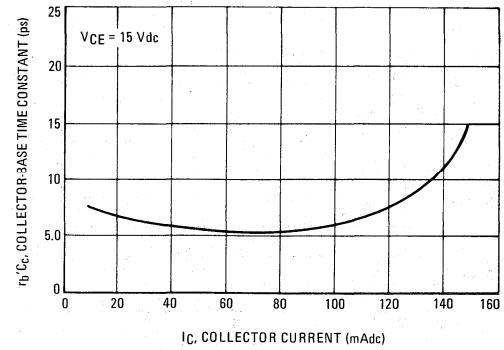


FIGURE 4 – SATURATION VOLTAGES

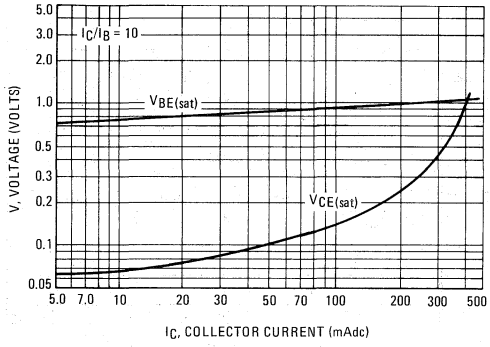


FIGURE 5 – CAPACITANCES versus REVERSE VOLTAGE

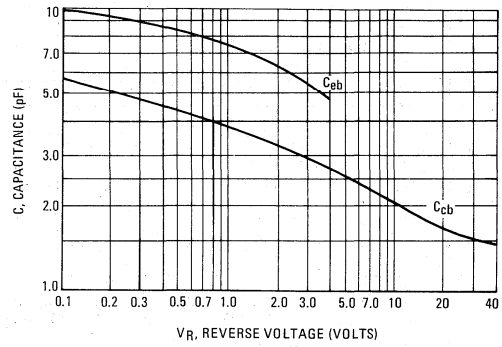
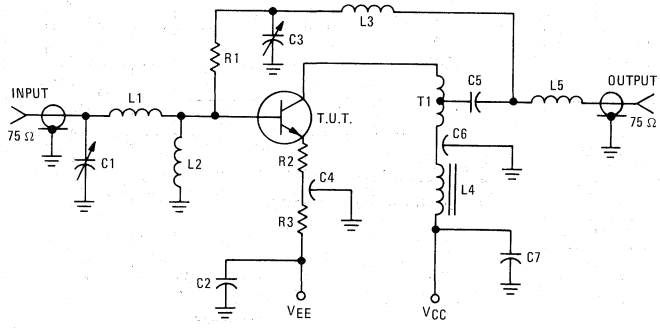


FIGURE 6 – BROADBAND TEST CIRCUIT



C1	1.0-10 pF	JOHANSON 2951 OR EQUIVALENT
C2, C7	0.01 μF	
C3	0.5-6.0 pF	JOHANSON 4642 OR EQUIVALENT
C4, C6	1500 pF	
C5	470 pF	
L1	2 TURNS AWG #26, 5/32" I.D.	
L2	1 μH MOLDED CHOKE	
L3	5 TURNS AWG #26, 3/32" I.D.	
L4	FERRITE CHOKE, 3 TURNS #30 ON STACKPOLE 57-0156 BEAD	
L5	2 TURNS AWG #26, 3/32" I.D.	
T1	AWG #30 TRIFILAR WOUND 1-9-9 ON STACKPOLE 57-0985, #11 TOROID	
R1	270 OHMS	
R2	18 OHMS	
R3	150 OHMS	

GARLOCK TEFLON SOCKET

3

FIGURE 7 – CROSS-MODULATION DISTORTION versus COLLECTOR CURRENT

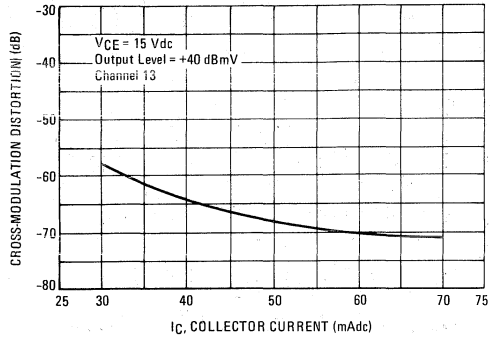


FIGURE 8 – CROSS-MODULATION DISTORTION versus OUTPUT LEVEL

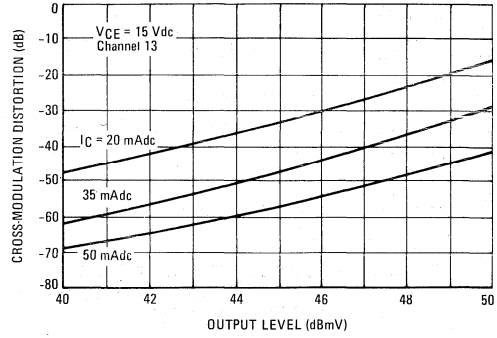


FIGURE 9 – NARROWBAND NOISE FIGURE versus COLLECTOR CURRENT

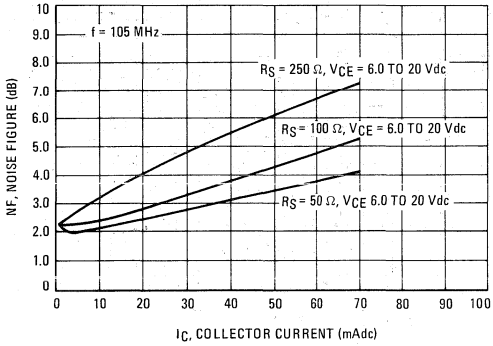


FIGURE 10 – NARROWBAND NOISE FIGURE versus COLLECTOR CURRENT

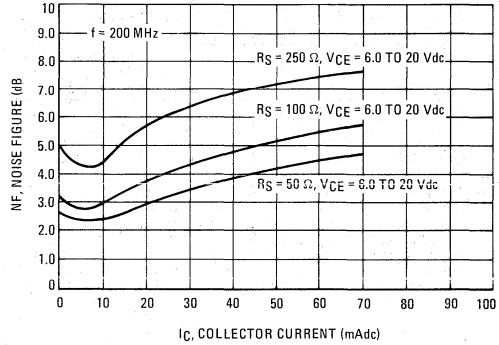


FIGURE 11 – BROADBAND NOISE FIGURE versus COLLECTOR CURRENT

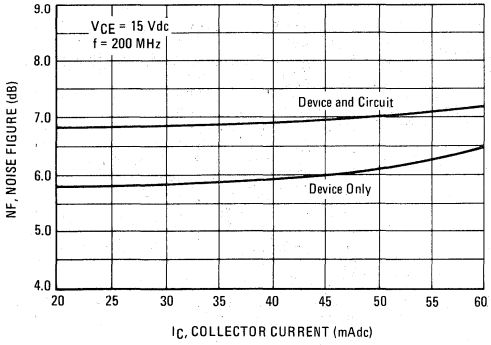


FIGURE 12 – NARROWBAND NOISE FIGURE versus FREQUENCY

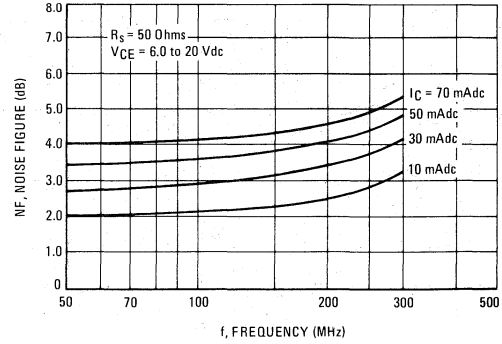


FIGURE 13 – INPUT ADMITTANCE versus FREQUENCY

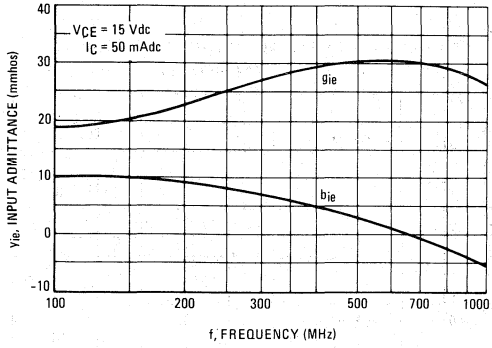


FIGURE 14 – INPUT ADMITTANCE versus COLLECTOR CURRENT

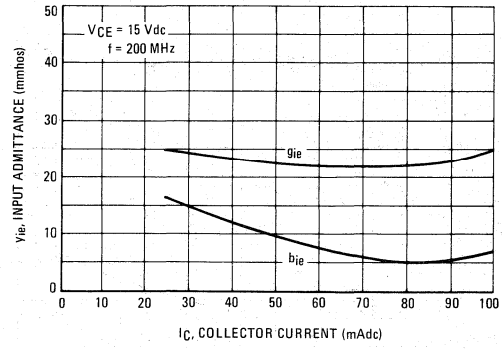


FIGURE 15 – REVERSE TRANSFER ADMITTANCE versus FREQUENCY

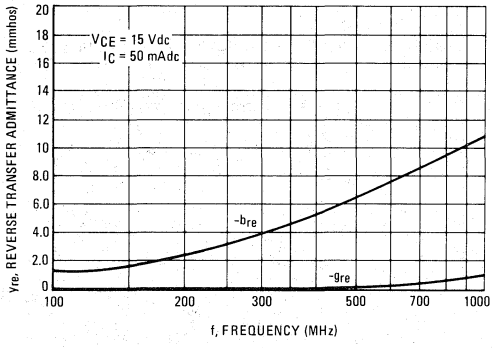


FIGURE 16 – REVERSE TRANSFER ADMITTANCE versus COLLECTOR CURRENT

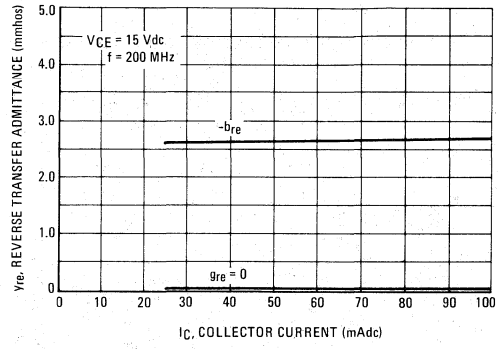


FIGURE 17 – FORWARD TRANSFER ADMITTANCE versus FREQUENCY

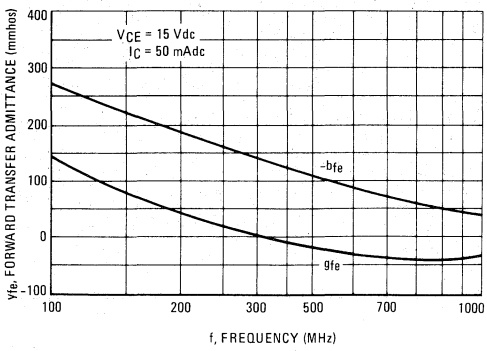


FIGURE 18 – FORWARD TRANSFER ADMITTANCE versus COLLECTOR CURRENT

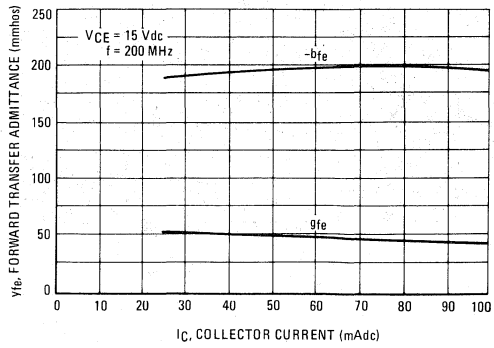


FIGURE 19 – OUTPUT ADMITTANCE versus FREQUENCY

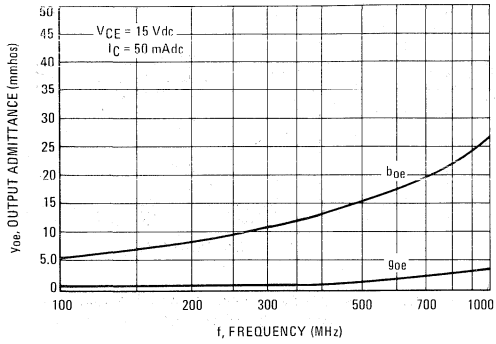


FIGURE 20 – OUTPUT ADMITTANCE versus COLLECTOR CURRENT

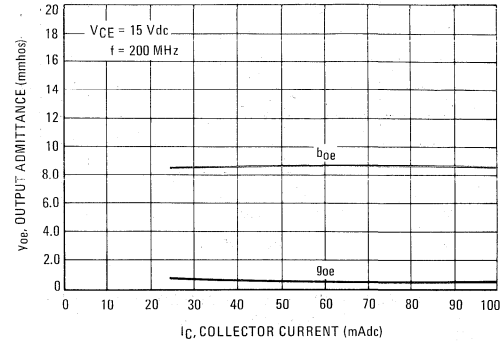


FIGURE 21 – INPUT REFLECTION COEFFICIENT versus FREQUENCY

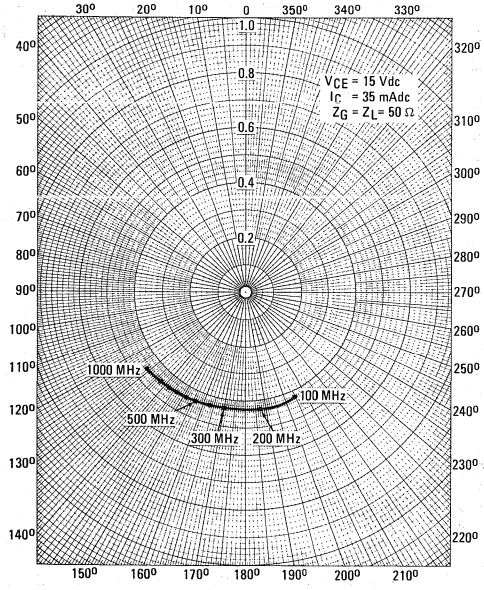


FIGURE 22 – OUTPUT REFLECTION COEFFICIENT versus FREQUENCY

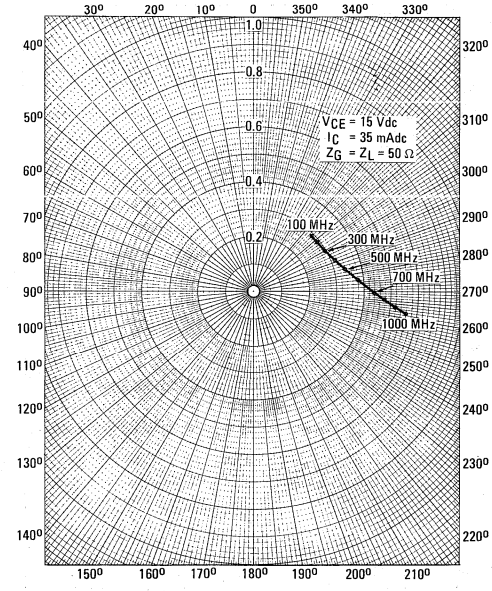


FIGURE 23 – REVERSE TRANSMISSION COEFFICIENT versus FREQUENCY

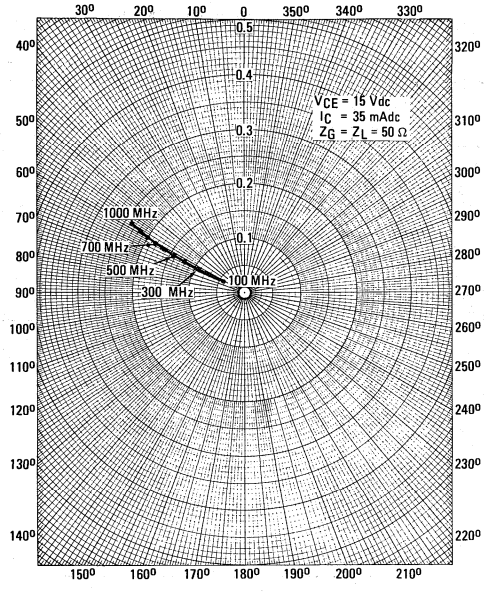


FIGURE 24 – FORWARD TRANSMISSION COEFFICIENT versus FREQUENCY

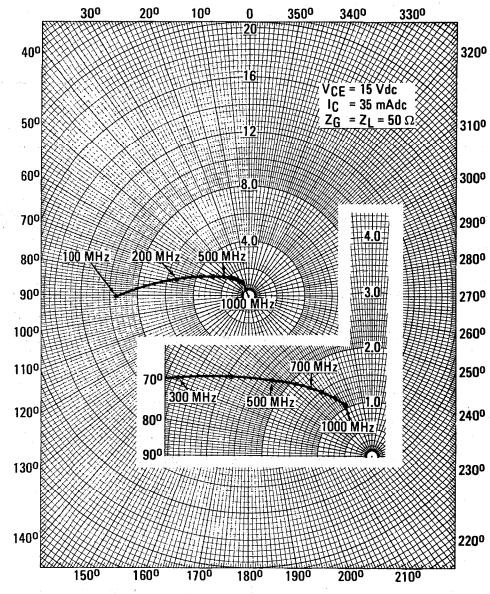
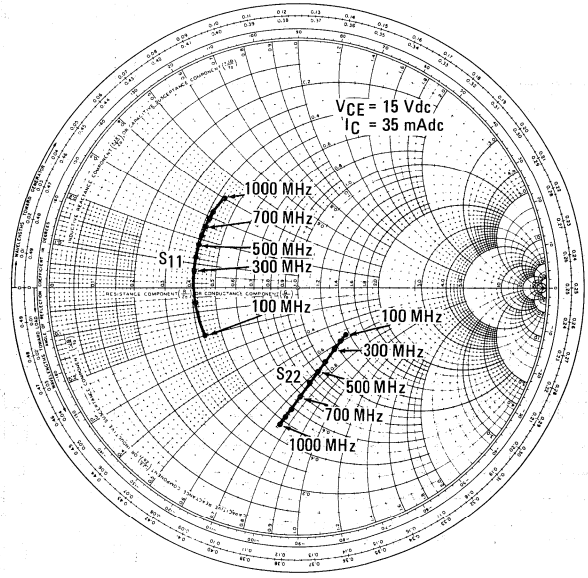


FIGURE 25 – INPUT REFLECTION COEFFICIENT AND OUTPUT REFLECTION COEFFICIENT versus FREQUENCY



3

2N5944
2N5945
2N5946

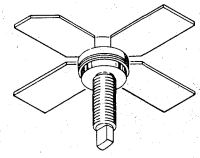
The RF Line

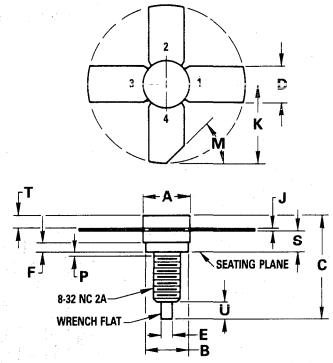
2.0, 4.0, 10 W - 470 MHz
RF POWER
TRANSISTORS
NPN SILICON

NPN SILICON RF POWER TRANSISTORS

. . . designed for 7.0 to 15 Volts, UHF large signal amplifier applications required in industrial and commercial FM equipment operating in the 400 to 960 MHz range.

- Specified 12.5 Volt, 470 MHz Characteristics —
  Power Output = 2.0 W — 2N5944
  4.0 W — 2N5945
  10 W — 2N5946
  Minimum Gain = 9.0 dB — 2N5944
  8.0 dB — 2N5945
  6.0 dB — 2N5946
  Efficiency = 60% Minimum
- Characterized with series equivalent large-signal impedance parameters





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.06	7.26	0.278	0.286
B	6.20	6.50	0.244	0.256
C	14.99	16.51	0.590	0.650
D	5.46	5.96	0.215	0.235
E	1.40	1.65	0.055	0.065
F	1.52	—	0.060	—
J	0.08	0.17	0.003	0.007
K	11.05	—	0.435	—
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
S	3.00	3.25	0.118	0.128
T	1.40	1.77	0.055	0.070
U	2.92	3.68	0.115	0.145

CASE 244-04

STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

MAXIMUM RATINGS

Rating	Symbol	2N5944	2N5945	2N5946	Unit
*Collector-Emitter Voltage	V_{CEO}	← 16 →			Vdc
*Collector-Base Voltage	V_{CBO}	← 36 →			Vdc
*Emitter-Base Voltage	V_{EBO}	← 4.0 →			Vdc
*Collector Current — Continuous	I_C	0.4	0.8	2.0	Adc
*Total Device Dissipation @ $T_C = 25^oC$(1) Derate above 25^oC	P_D	5.0 28.5	15 85.5	37.5 214	Watts mW/^oC
*Storage Temperature Range	T_{stg}	← −65 to +200 →			^oC
Stud Torque(2)	—	← 6.5 →			in-lbs.

*Indicates JEDEC Registered Data
(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.
(2) For repeated assembly use 5 in-lbs.

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage		$V_{(BR)CEO}$				Vdc
(I_C = 50 mAdc, I_B = 0)	2N5944		16	–	–	
(I_C = 100 mAdc, I_B = 0)	2N5945		16	–	–	
(I_C = 200 mAdc, I_B = 0)	2N5946		16	–	–	
Collector-Emitter Breakdown Voltage		$V_{(BR)CES}$				Vdc
(I_C = 50 mAdc, V_{BE} = 0)	2N5944		36	–	–	
(I_C = 100 mAdc, V_{BE} = 0)	2N5945		36	–	–	
(I_C = 200 mAdc, V_{BE} = 0)	2N5946		36	–	–	
Emitter-Base Breakdown Voltage		$V_{(BR)EBO}$				Vdc
(I_E = 1.0 mAdc, I_C = 0)	2N5944		4.0	–	–	
(I_E = 2.0 mAdc, I_C = 0)	2N5945		4.0	–	–	
(I_E = 4.0 mAdc, I_C = 0)	2N5946		4.0	–	–	
Collector Cutoff Current		I_{CES}				mAdc
(V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 55°C)	2N5944		–	0.2	10	
	2N5945,2N5946		–	0.5	20	
Collector Cutoff Current		I_{CBO}				mAdc
(V_{CB} = 15 Vdc, I_E = 0)	2N5944,2N5945		–	–	1.0	
	2N5946		–	–	2.0	
ON CHARACTERISTICS						
DC Current Gain		h_{FE}				–
(I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	2N5944		20	80	–	
(I_C = 200 mAdc, V_{CE} = 5.0 Vdc)	2N5945		20	80	–	
(I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	2N5946		20	80	–	
DYNAMIC CHARACTERISTICS						
Output Capacitance		C_{ob}				pF
(V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	2N5944		–	11	15	
	2N5945		–	18	25	
	2N5946		–	38	45	
FUNCTIONAL TEST (Figures 20 and 21).						
Common-Emitter Amplifier Power Gain		G_{PE}				dB
(V_{CC} = 12.5 Vdc, P_{out} = 2.0 W, I_C(max) = 267 mAdc, f = 470 MHz)	2N5944		9.0	10	–	
(V_{CC} = 12.5 Vdc, P_{out} = 4.0 W, I_C(max) = 533 mAdc, f = 470 MHz)	2N5945		8.0	9.0	–	
(V_{CC} = 12.5 Vdc, P_{out} = 10 W, I_C(max) = 1.33 Adc, f = 470 MHz)	2N5946		6.0	7.0	–	
Collector Efficiency		η				%
(V_{CC} = 12.5 Vdc, P_{out} = 2.0 W, I_C(max) = 240 mAdc, f = 470 MHz)	2N5944		60	–	–	
(V_{CC} = 12.5 Vdc, P_{out} = 4.0 W, I_C(max) = 500 mAdc, f = 470 MHz)	2N5945		60	–	–	
(V_{CC} = 12.5 Vdc, P_{out} = 10 W, I_C(max) = 1.3 Adc, f = 470 MHz)	2N5946		60	–	–	

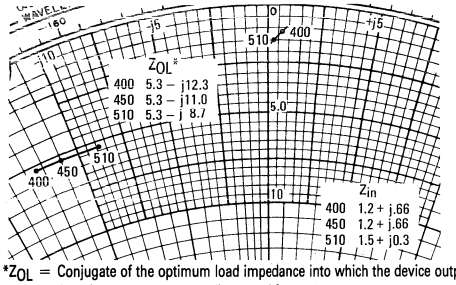
*Indicates JEDEC Registered Data

These devices are available in various packages, such as a studless stripline package, TO-39, and also in chip form on beryllium oxide carriers for hybrid assemblies.

For further information, contact your nearest Motorola representative or the factory representative.

2N5944
TYPICAL PERFORMANCE DATA

FIGURE 1 – SERIES EQUIVALENT IMPEDANCE



*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.
V_{CC} = 12.5 Vdc, P_{out} = 2.0 W

FIGURE 2 – OUTPUT POWER versus SUPPLY VOLTAGE

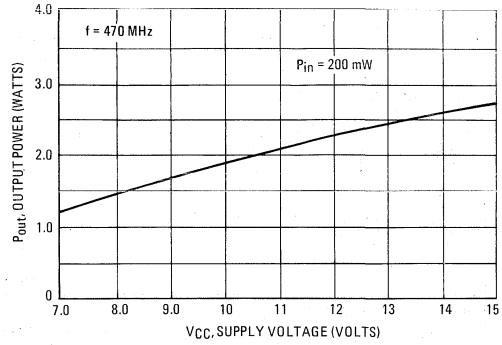


FIGURE 3 – OUTPUT POWER versus INPUT POWER

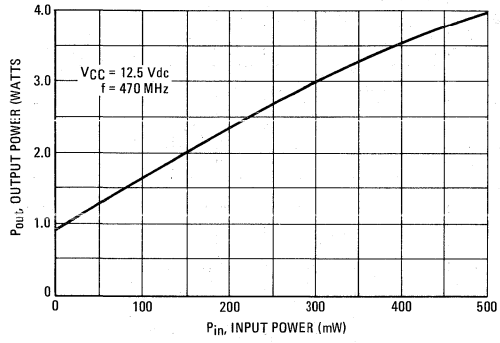


FIGURE 4 – OUTPUT POWER versus FREQUENCY

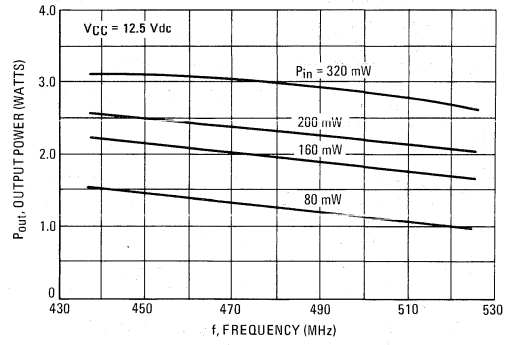


FIGURE 5 – OUTPUT POWER versus INPUT POWER

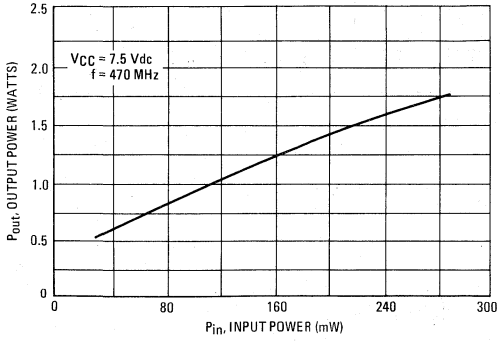
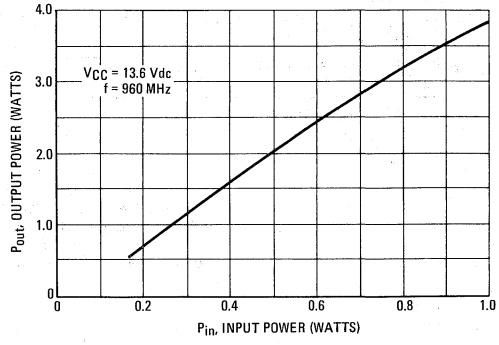
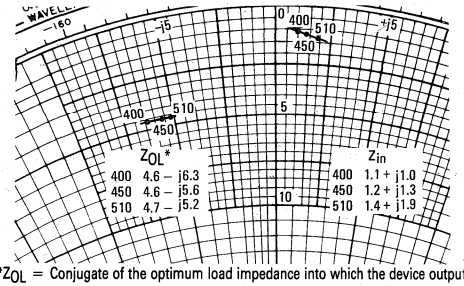


FIGURE 6 – OUTPUT POWER versus INPUT POWER



2N5945
TYPICAL PERFORMANCE DATA

FIGURE 7 – SERIES EQUIVALENT IMPEDANCE



*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

V_{CC} = 12.5 Vdc, P_{out} = 4.0 W

FIGURE 8 – OUTPUT POWER versus SUPPLY VOLTAGE

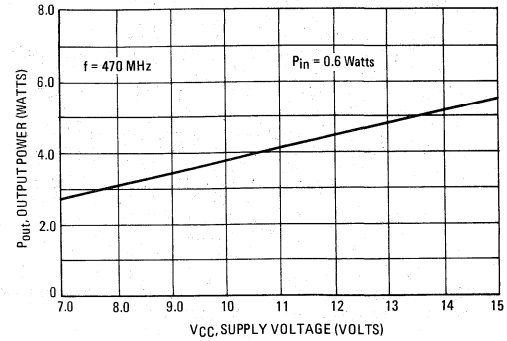


FIGURE 9 – OUTPUT POWER versus INPUT POWER

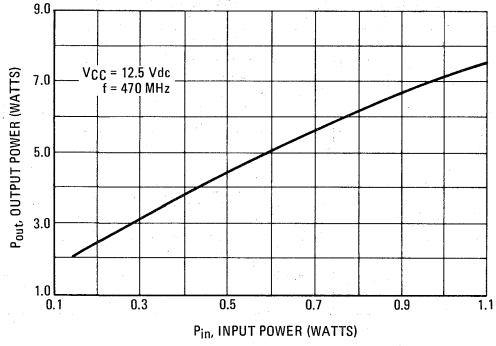


FIGURE 10 – OUTPUT POWER versus FREQUENCY

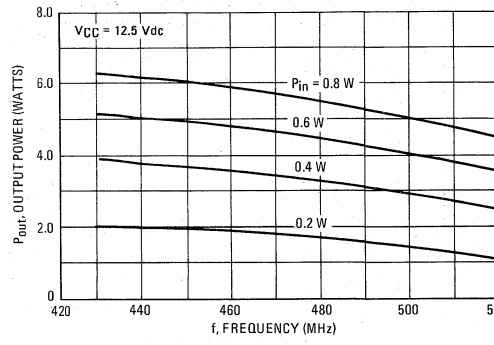


FIGURE 11 – OUTPUT POWER versus INPUT POWER

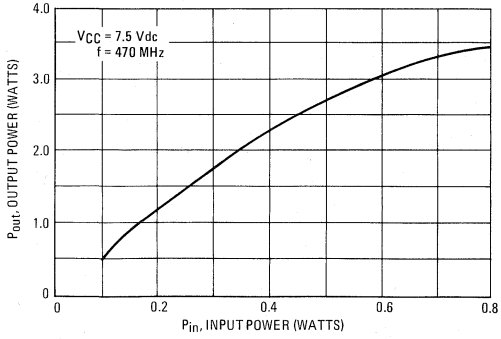
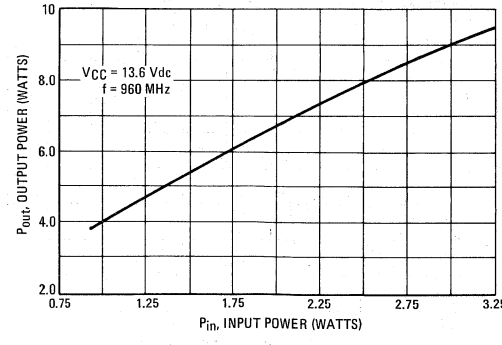
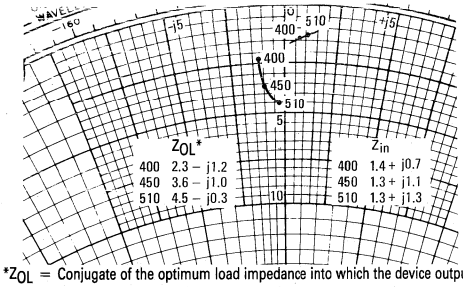


FIGURE 12 – OUTPUT POWER versus INPUT POWER



2N5946
TYPICAL PERFORMANCE DATA

FIGURE 13 – SERIES EQUIVALENT IMPEDANCE



*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.
V_{CC} = 12.5 Vdc, P_{out} = 12 W

FIGURE 14 – OUTPUT POWER versus SUPPLY VOLTAGE

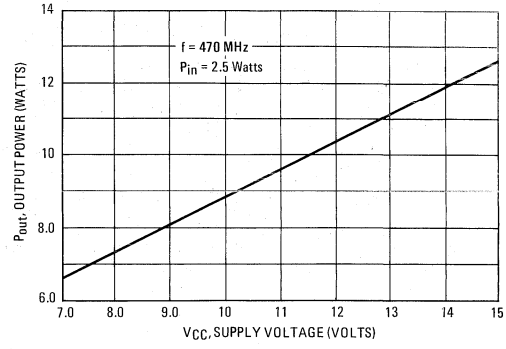


FIGURE 15 – OUTPUT POWER versus INPUT POWER

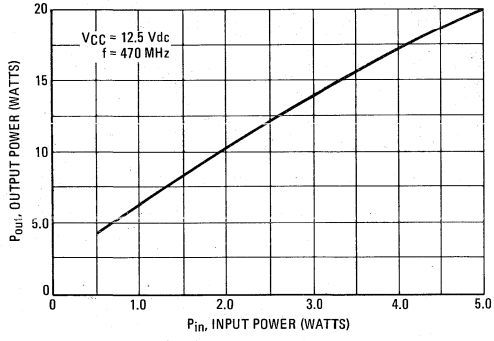


FIGURE 16 – OUTPUT POWER versus FREQUENCY

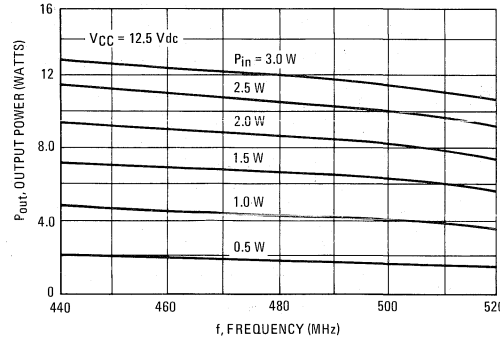
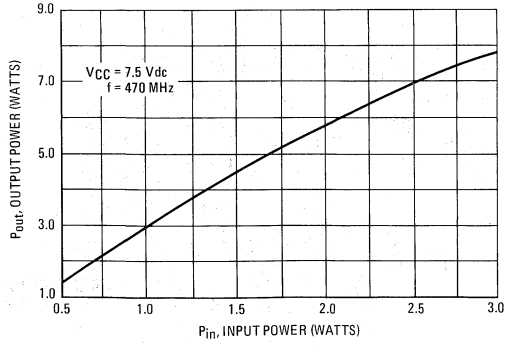
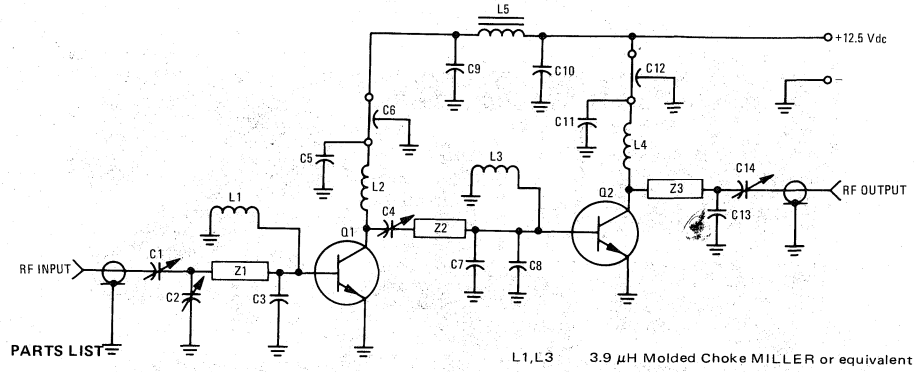


FIGURE 17 – OUTPUT POWER versus INPUT POWER



10-WATT BROADBAND UHF AMPLIFIER

FIGURE 18



PARTS LIST

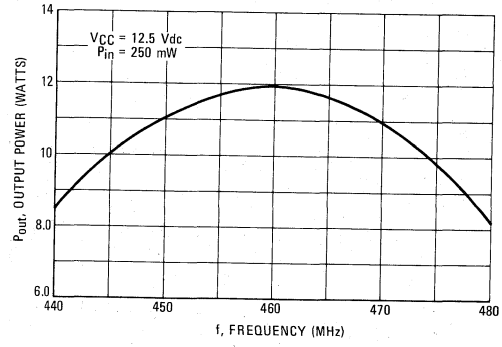
C1,C2,C4,C13,C14	0.9-7.0 pF ARCO 400 or equivalent
C3,C7,C8	25 pF UNELCO or equivalent
C5,C11	0.1 μF Ceramic 35 V
C6,C12	680 pF ALLEN BRADLEY Feedthru
C9,C10	1.0 μF, 35 V Tantalum
L1,L3	3.9 μH Molded Choke MILLER or equivalent
L2,L4	5 Turns #18 AWG Enameled 0.2" I.D.
L5	FERROXCUBE Ferrite Choke VK200 20/4B
Z1,Z2,Z3	Microstrip Lines (See Template Below)
Q1	2N5944
Q2	2N5946

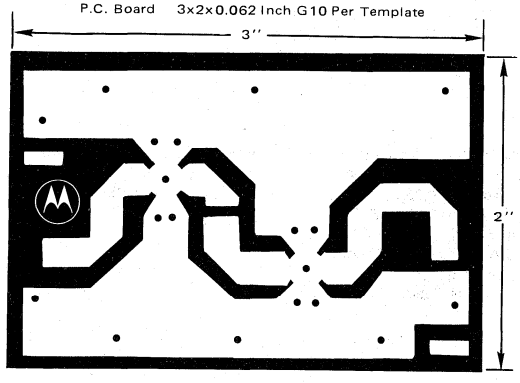
10 W AMPLIFIER PERFORMANCE

V_{CC} = 12.5 Vdc

Frequency MHz	P_{in} mW	P_{out} W	I_C Amp
440	250	8.5	1.5
450	250	11	1.6
460	250	12	1.6
470	250	10.9	1.5
480	250	8.2	1.2

FIGURE 19 – OUTPUT POWER versus FREQUENCY





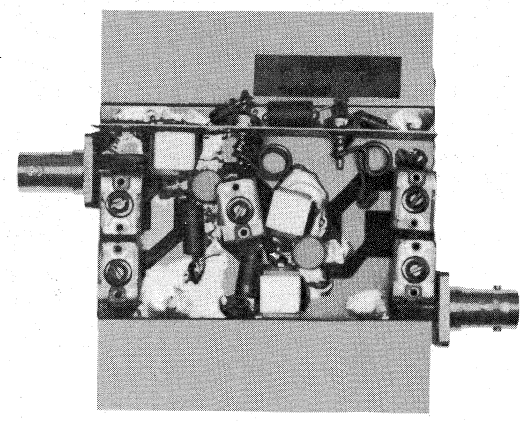
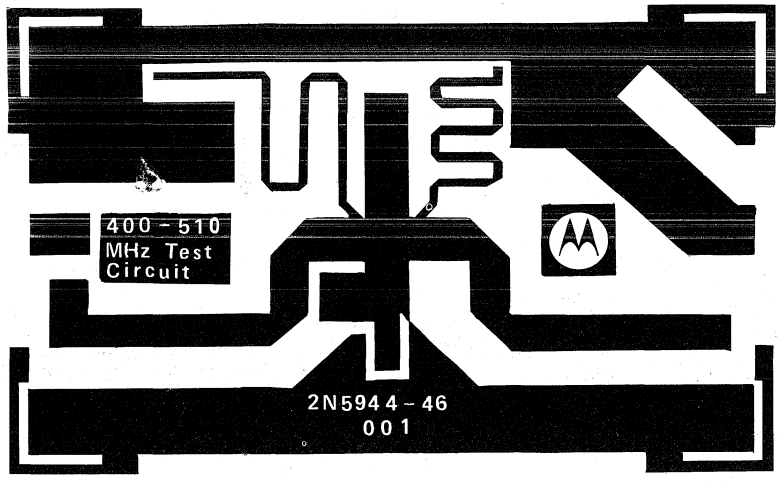


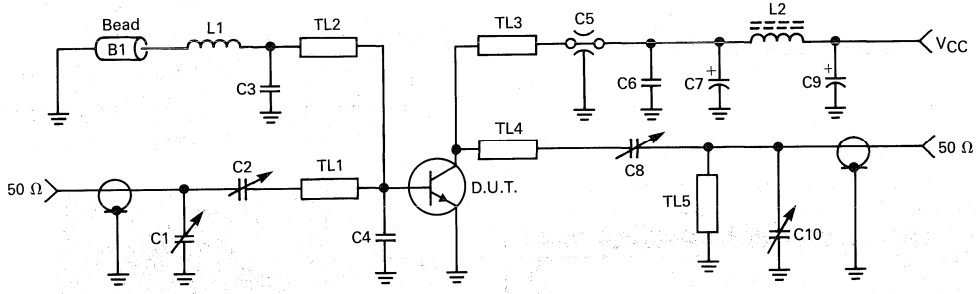
FIGURE 20 — 470 MHz TEST CIRCUIT



NOTE: The Printed Circuit Board shown is 75% of the original.

3

FIGURE 21 — 470 MHz TEST CIRCUIT SCHEMATIC



C1, C2, C8, C10 — Johanson Trimmer, JMC #5501
C3 — 100 pF Unelco 350 Vdc J101
C4 — 15 pF Unelco
C5 — 680 pF Allen Bradley Feed-Thru
C6 — 0.1 μF Monolithic
C7 — 1 μF Tantalum Sprague ±10% 35 Vdc
C9 — 5 μF Electrolytic 5–25 Vdc

TL1 — Micro Strip 0.26″ x 2.9″
TL2 — Micro Strip 0.055″ x 3.9″
TL3 — Micro Strip 0.055″ x 2.9″
TL4 — Micro Strip 0.26″ x 2.9″
TL5 — Micro Strip 0.50″ x 1.2″
L1 — #18 AWG Wire 0.750″ Long
L2 — VK200 20/4B
B1 — Ferroxcube Bead, 56-590-65-3B

Board — 0.062″ Glass Teflon
2 oz. Cu CLAD
ϵ_r = 2.55

2N5947

The RF Line

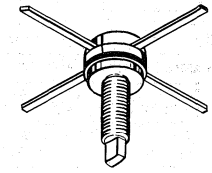
NPN SILICON HIGH FREQUENCY TRANSISTOR

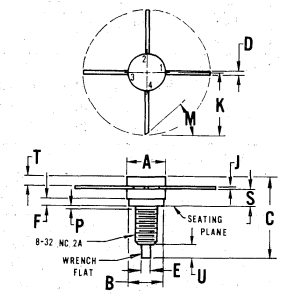
. . . designed specifically for broadband applications requiring low cross-modulation distortion and low noise figure. Characterized for use in CATV applications. The 2N5947 was formerly the MM8012.

- Low Cross Modulation Distortion –
  XM = -57 dB (Max) @ +50 dBmV Output
- Low Noise Figure – @ f = 200 MHz
  NF (Narrowband) = 3.8 dB (Typ)
  NF (Broadband) = 8.5 dB (Max)
- High Broadband Power Gain –
  G_{pe} = 10 dB (Min) @ f = 250 MHz

HIGH FREQUENCY TRANSISTOR

NPN SILICON





STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.06	7.26	0.278	0.286
B	6.20	6.50	0.244	0.256
C	15.24	16.51	0.600	0.650
D	0.66	0.86	0.026	0.034
E	1.40	1.65	0.055	0.065
F	1.52	–	0.060	–
J	0.10	0.15	0.004	0.006
K	11.17	–	0.440	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
S	2.74	3.35	0.108	0.132
T	1.40	1.78	0.055	0.070
U	2.92	3.68	0.115	0.145

CASE 244A-01

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	3.5	Vdc
Collector Current – Continuous	I_C	400	mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	5.0 28.6	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.

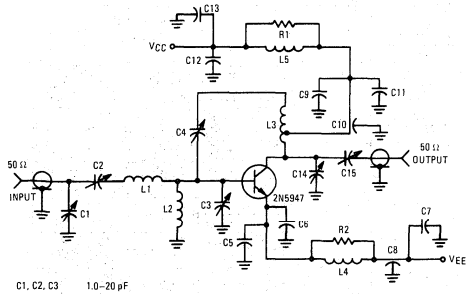
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	$V_{(BR)CBO}$	40	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	–	–	Vdc
Collector Cutoff Current (V_{CE} = 28 Vdc, I_B = 0)	I_{CEO}	–	–	100	μAdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)	I_{CBO}	–	–	10	μAdc
Emitter Cutoff Current (V_{BE} = 3.5 Vdc, I_C = 0)	I_{EBO}	–	–	100	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 75 mAdc, V_{CE} = 20 Vdc)	h_{FE}	25	–	250	–
Collector-Emitter Saturation Voltage (I_C = 200 mAdc, I_B = 20 mAdc)	$V_{CE(sat)}$	–	0.2	0.35	Vdc
Base-Emitter Saturation Voltage (I_C = 200 mAdc, I_B = 20 mAdc)	$V_{BE(sat)}$	–	1.0	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (Figure 3) (I_C = 75 mAdc, V_{CE} = 20 Vdc, f = 200 MHz)	f_T	1100	1500	–	MHz
Collector-Base Capacitance (Figure 4) (V_{CB} = 30 Vdc, I_E = 0, f = 100 kHz)	C_{cb}	–	1.5	4.0	pF
Emitter-Base Capacitance (Figure 4) (V_{EB} = 0.5 Vdc, I_C = 0, f = 100 kHz)	C_{eb}	–	8.2	12	pF
Small-Signal Current Gain (I_C = 75 mAdc, V_{CE} = 20 Vdc, f = 1.0 kHz)	h_{fe}	25	–	300	–
Collector-Base Time Constant (I_E = 75 mAdc, V_{CB} = 20 Vdc, f = 31.8 MHz)	$r_b C_c$	2.0	–	20	ps
Noise Figure	NF				dB
(I_C = 50 mAdc, V_{CE} = 20 Vdc, f = 200 MHz) (Figure 1)		–	3.8	–	
(I_C = 50 mAdc, V_{CE} = 20 Vdc, f = 200 MHz) (1) (Figure 2, 9)		–	7.2	8.5	
(I_C = 75 mAdc, V_{CE} = 20 Vdc, f = 200 MHz) (1) (Figure 2, 9)		–	7.8	–	
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (Figure 2) (I_C = 75 mAdc, V_{CE} = 20 Vdc, f = 250 MHz)	G_{pe}	10	11	–	dB
Intermodulation Distortion (Figure 2, 10) (I_C = 75 mAdc, V_{CE} = 20 Vdc, V_{out} = +50 dBmv)	IM	–	-55	-50	dB
Cross Modulation Distortion (Figure 2, 11) (I_C = 75 mAdc, V_{CE} = 20 Vdc, V_{out} = +50 dBmV)	XM	–	-60	-57	dB

*Indicates JEDEC Registered Data.

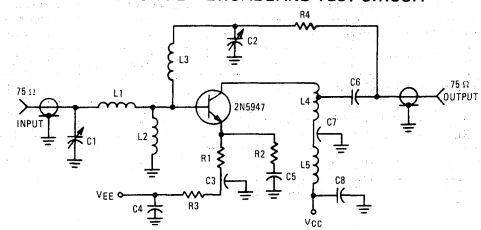
(1) Includes noise figure of post-amplifier and matching pad.

FIGURE 1 – NARROWBAND TEST CIRCUIT



C1, C2, C3	1.0–20 pF	L2	1-1/2 Turns AWG #18, 1/4" I.D., 3/16" Long
C4, C14, C15	1.0–10 pF	L3	9-3/4 Turns AWG #18, 3/16" I.D., 1" Long Tapped 1-3/4 Turns from Collector End
C5, C8, C9	470 pF		
C6, C10, C11	0.001 μF		
C7, C13	0.01 μF		
C12	0.1 μF		
L1	3 Turns AWG #18, 1/4" I.D., 5/16" Long	L4, L5	0.47 μH Molded Choke
		R1, R2	10 Ohms

FIGURE 2 – BROADBAND TEST CIRCUIT



C1, C2	0.5–6.0 pF	L4	#30 AWG Trifilar Wound 1:9:9 Stackpole 57-0985, #11 Toroid
C3, C7	1500 pF Underwood		
C4, C5, C8	0.01 μF		
C6	470 pF	L5	Ferrite Choke, 3 Turns #30 on Stackpole 57-0156 Bead
L1	3 Turns #20 AWG, 5/32" I.D.		
L2	0.84 μH, Ohmite Z235	R1	20 Ohms
L3	5 Turns #26 AWG, 5/32" I.D.	R2	68 Ohms
		R3	150 Ohms
		R4	360 Ohms

FIGURE 3 – CURRENT-GAIN–BANDWIDTH PRODUCT

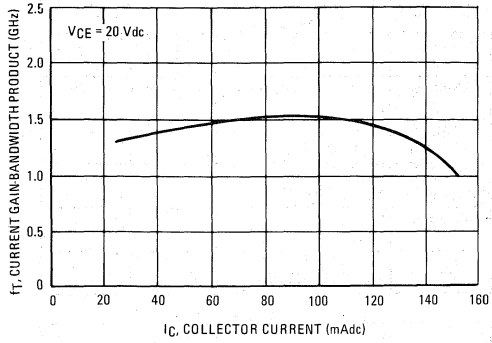


FIGURE 4 – CAPACITANCES

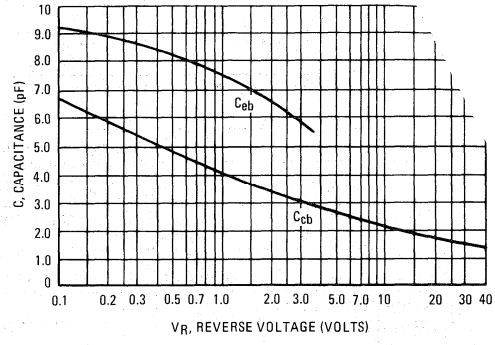


FIGURE 5 – COLLECTOR-EMITTER SATURATION VOLTAGE

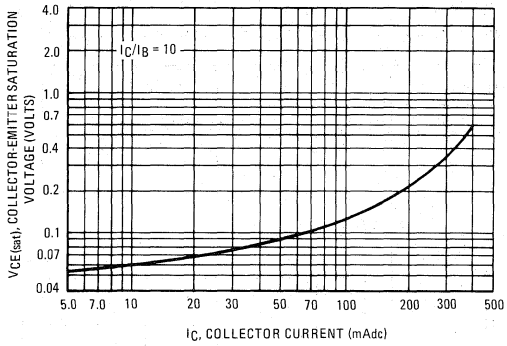


FIGURE 6 – BASE-EMITTER SATURATION VOLTAGE

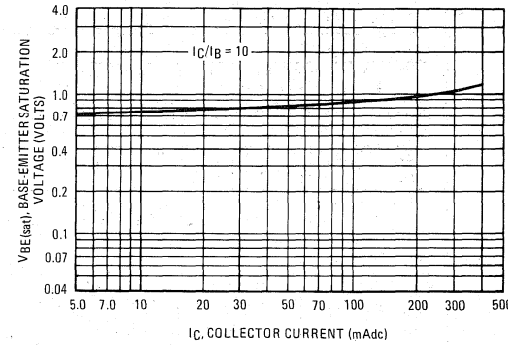


FIGURE 7 – NARROWBAND NOISE FIGURE versus CURRENT

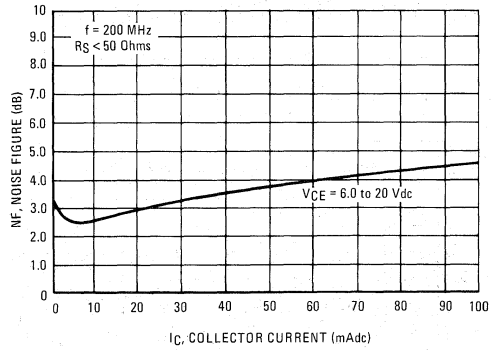


FIGURE 8 – BROADBAND NOISE FIGURE versus CURRENT

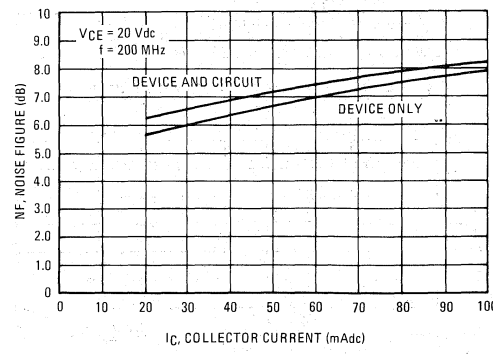
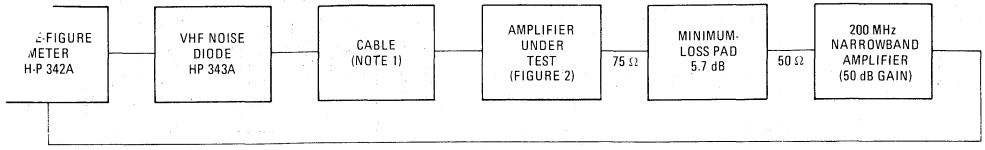


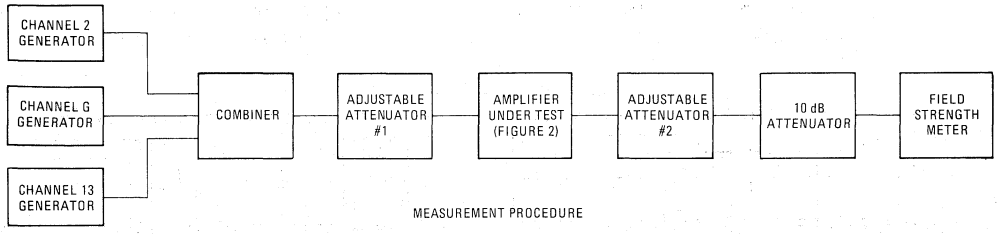
FIGURE 9 – NOISE FIGURE TEST SETUP



NOTE 1. RG-59 CABLE WITH ORIGINAL CENTER CONDUCTOR REPLACED WITH #30 WIRE. OVERALL LENGTH, INCLUDING BNC CONNECTORS, IS A QUARTER-WAVELENGTH AT 200 MHz (APPROX. 11 INCHES). USED TO MATCH IMPEDANCE OF NOISE DIODE TO AMPLIFIER UNDER TEST.

THE NOISE FIGURE OF THE POST-AMPLIFIERS AND MINIMUM LOSS PAD IS 8.4 dB.

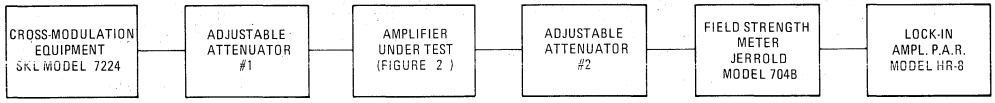
FIGURE 10 – INTERMODULATION DISTORTION TEST SETUP



MEASUREMENT PROCEDURE

1. ADJUST CHANNEL 2 GENERATOR FOR RATED OUTPUT FROM TEST AMPLIFIER (CHANNELS G & 13 OFF).
2. REPEAT FOR CHANNEL G (2 & 13 OFF) AND CHANNEL 13 (2 & G OFF). NOTE FOR REFERENCE THE FIELD STRENGTH METER READING FOR CHANNEL 13 (2 & G OFF).
3. TURN CHANNEL 13 OFF AND DRIVE THE TEST AMPLIFIER WITH CHANNELS 2 & G. MEASURE THE LEVEL OF INTERMODULATION DISTORTION AT CHANNEL 13 RELATIVE TO THE REFERENCE LEVEL IN STEP 2.

FIGURE 11 – CROSS MODULATION DISTORTION TEST SETUP



MEASUREMENT PROCEDURE

1. ADJUST THE CROSSMODULATION EQUIPMENT FOR +50 dBmV OUTPUT FROM EACH CHANNEL.
2. ADJUST ATTENUATOR #1 FOR THE DESIRED OUTPUT LEVEL FROM THE TEST AMPLIFIER. ADJUST ATTENUATOR #2 TO MAINTAIN THE FIELD STRENGTH METER INPUT AT +10 dBmV.
3. WITH THE FIELD STRENGTH METER SELECT CHANNEL 13. USING THE WAVE ANALYZER MEASURE THE LEVEL OF THE MODULATION ON CHANNEL 13 DUE TO CROSS-MODULATION OF CHANNELS 2-12.

FIGURE 12 – CROSS MODULATION DISTORTION versus OUTPUT LEVEL

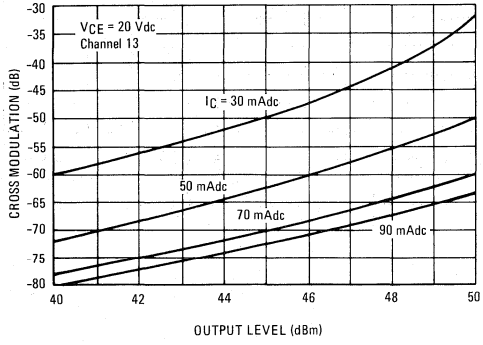
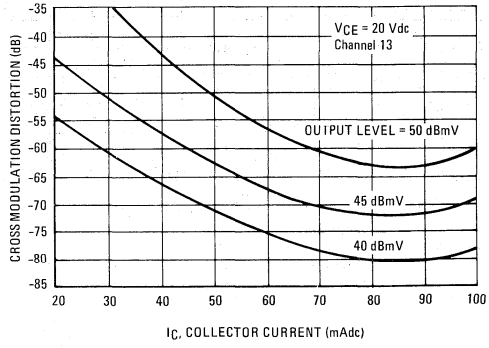


FIGURE 13 – CROSS MODULATION DISTORTION versus CURRENT



2N6080

The RF Line

4.0 W – 175 MHz

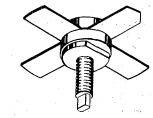
RF POWER TRANSISTOR

NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed for 12.5 Volt VHF large-signal power amplifier applications required in military and industrial equipment operating to 300 MHz.

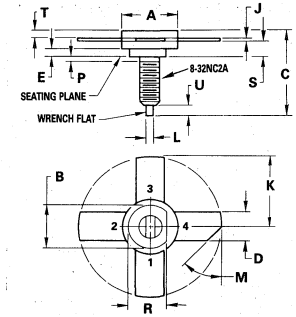
- Specified 12.5 Volt, 175 MHz Characteristics –
  Output Power = 4.0 W
  Minimum Gain = 12 dB
  Efficiency = 50%
- Characterized with Series Equivalent Large-Signal Impedance Parameters



***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current – Continuous	I_C	1.0	Adc
Total Device Dissipation @ $T_C = 25^oC$ (2) Derate above 25^oC	P_D	12 68.5	Watts $mW/^oC$
Storage Temperature Range	T_{stg}	-65 to +200	^oC
Stud Torque (1)	–	6.5	in. lb.

*Indicates JEDEC Registered Data.
(1) For repeated assembly use 5 in lb.
(2) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	17.02	20.07	0.670	0.790
D	5.46	5.97	0.215	0.235
E	1.78	—	0.070	—
J	0.08	0.18	0.003	0.007
K	12.45	—	0.490	—
L	1.40	1.78	0.055	0.070
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.11	2.54	0.083	0.100
U	2.49	3.35	0.098	0.132

CASE 145A-09

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = +55°C)	I_{CES}	–	–	5.0	mAdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	0.25	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 0.25 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0	–	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	15	20	pF
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (P_{out} = 4.0 W, V_{CC} = 12.5 Vdc, f = 175 MHz)	G_{PE}	12	–	–	dB
Collector Efficiency (P_{out} = 4.0 W, V_{CC} = 12.5 Vdc, f - 175 MHz)	η	50	–	–	%

*Indicates JEDEC Registered Data.

FIGURE 1 – 175 MHz TEST CIRCUIT

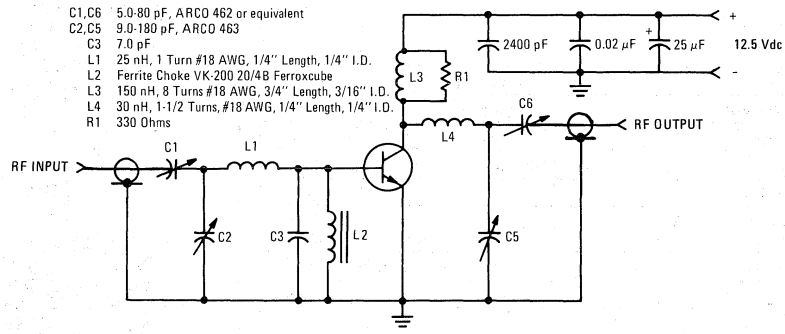


FIGURE 2 – OUTPUT POWER versus INPUT POWER

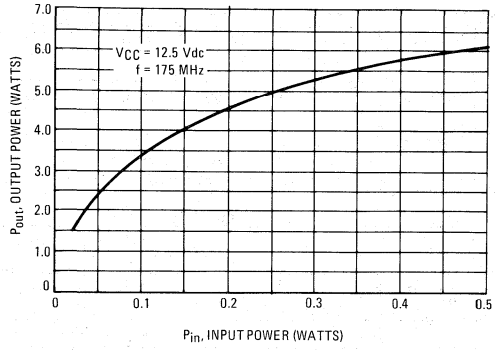


FIGURE 3 – OUTPUT POWER versus FREQUENCY

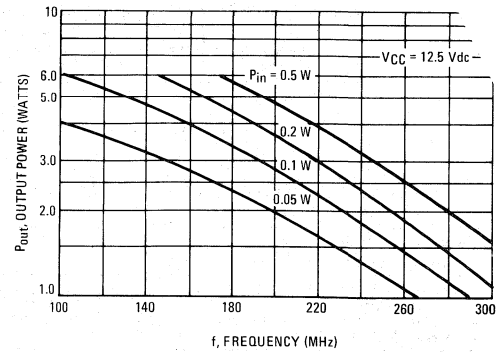


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

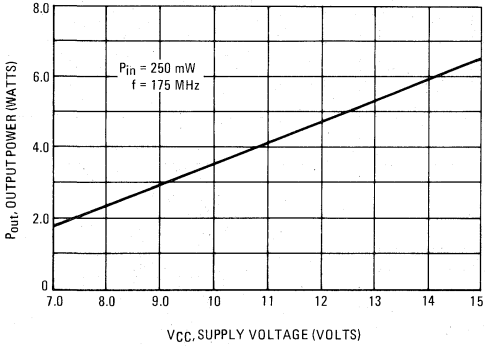
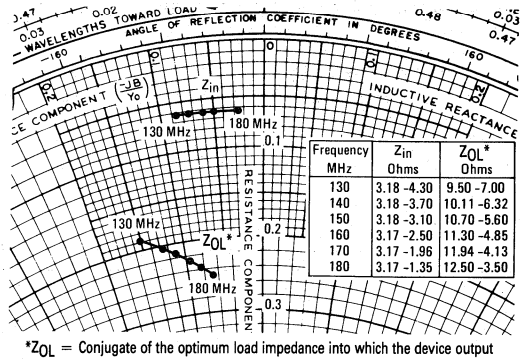


FIGURE 5 – SERIES EQUIVALENT IMPEDANCE



Frequency MHz	Z_{in} Ohms	Z_{OL}* Ohms
130	3.18 -4.30	9.50 -7.00
140	3.18 -3.70	10.11 -6.32
150	3.18 -3.10	10.70 -5.60
160	3.17 -2.50	11.30 -4.85
170	3.17 -1.96	11.94 -4.13
180	3.17 -1.35	12.50 -3.50

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

2N6081
MRF221

The RF Line

15 W – 175 MHz

RF POWER TRANSISTORS

NPN SILICON

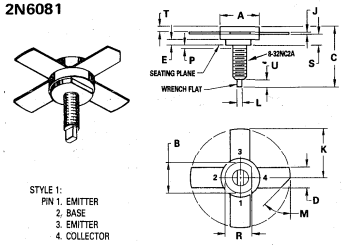
NPN SILICON RF POWER TRANSISTORS

. . . designed for 12.5 Volt VHF large-signal power amplifier applications required in commercial and industrial equipment operating to 300 MHz.

- Specified 12.5 Volt, 175 MHz Characteristics –
  Output Power = 15 W
  Minimum Gain = 6.3 dB
  Efficiency = 60%
- Characterized with Series Equivalent Large-Signal Impedance Parameters

3

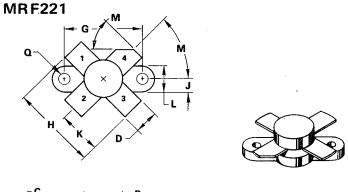
2N6081



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	17.02	20.07	0.670	0.790
D	5.46	5.97	0.215	0.235
E	1.78	—	0.070	—
J	0.08	0.18	0.003	0.007
K	12.45	—	0.490	—
L	1.40	1.78	0.055	0.070
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.11	2.54	0.083	0.100
U	2.49	3.35	0.098	0.132

CASE 145A-09

MRF221



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.39	25.15	0.960	0.990
B	9.40	9.91	0.370	0.390
C	5.82	7.14	0.229	0.281
D	5.46	5.97	0.215	0.235
E	2.16	2.67	0.085	0.105
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	20.07	20.57	0.790	0.810
K	10.03	10.29	0.395	0.405
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.81	4.57	0.150	0.180
Q	2.87	3.30	0.113	0.130

CASE 211-07

***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current – Continuous	I_C	2.5	Adc
Total Device Dissipation @ $T_C = 25^oC$ (1) Derate above 25^oC	P_D	31 177	Watts $mW/^oC$
Storage Temperature Range	T_{stg}	-65 to +200	^oC
Stud Torque (2)	–	6.5	in. lb.

*Indicates JEDEC Registered Data for 2N6081.

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

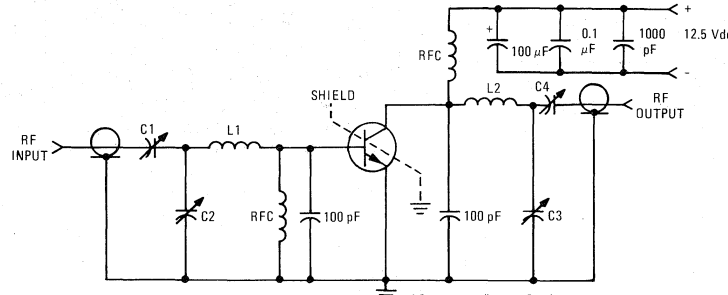
(2) For repeated assembly use 5 in. lb.

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	–	–	
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	–	–	Vc
Emitter-Base Breakdown Voltage (I_E = 2.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = +55°C)	I_{CES}	–	–	8.0	mAdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	0.5	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0	–	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	70	85	pF
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (P_{out} = 15 W, V_{CC} = 12.5 Vdc, f = 175 MHz)	G_{PE}	6.3	–	–	dB
Collector Efficiency (P_{out} = 15 W, V_{CC} = 12.5 Vdc, f = 175 MHz)	η	60	–	–	%

*Indicates JEDEC Registered Data for 2N6081.

FIGURE 1 – 175 MHz TEST CIRCUIT



C1,2,3,4 5.0-80 pF ARCO 462
L1 Straight Wire, #14 AWG, 1-3/8" Long
L2 1 Turn, #14 AWG, 3/8" ID, Length Plus Leads = 1"
RFC VK200-20/4B, FERROXCUBE.

URE 2 – OUTPUT POWER versus INPUT POWER

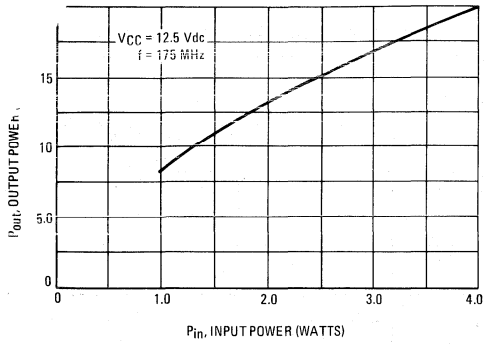


FIGURE 3 – OUTPUT POWER versus FREQUENCY

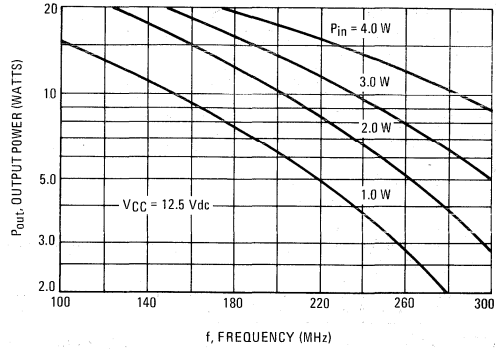


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

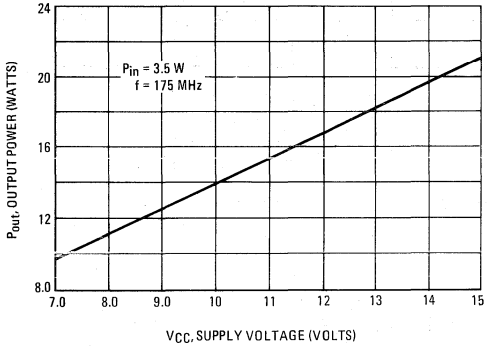
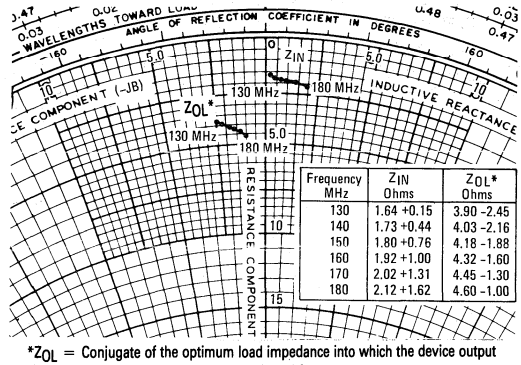


FIGURE 5 – SERIES EQUIVALENT IMPEDANCE



Frequency MHz	ZIN Ohms	ZOL* Ohms
130	1.64 +0.15	3.90 -2.45
140	1.73 +0.44	4.03 -2.16
150	1.80 +0.76	4.18 -1.88
160	1.92 +1.00	4.32 -1.60
170	2.02 +1.31	4.45 -1.30
180	2.12 +1.62	4.60 -1.00

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

2N6082

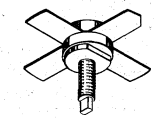
The RF Line

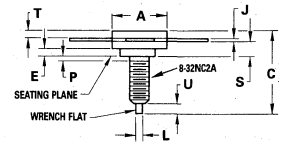
25 W – 175 MHz
RF POWER TRANSISTOR
NPN SILICON

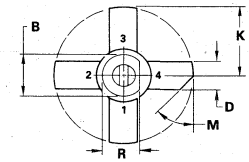
NPN SILICON RF POWER TRANSISTORS

. . . designed for 12.5 Volt VHF large-signal amplifier applications required in commercial and industrial equipment operating to 300 MHz.

- Specified 12.5 Volt, 175 MHz Characteristics –
  Output Power = 25 W
  Minimum Gain = 6.2 dB
  Efficiency = 65%







STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	5.0	Adc
Total Device Dissipation @ T_C = 25°C(2) Derate above 25°C	P_D	65 .37	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Stud Torque(1)	—	6.5	in.lb.

*Indicates JEDEC Registered Data for 2N6082.
(1)For Repeated Assembly Use 5 in. lb.
(2)These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	17.02	20.07	0.670	0.790
D	5.46	5.97	0.215	0.235
E	1.78	—	0.070	—
J	0.08	0.18	0.003	0.007
K	12.45	—	0.490	—
L	1.40	1.78	0.055	0.070
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.11	2.54	0.083	0.100
U	2.49	3.35	0.098	0.132

CASE 145A-09

3

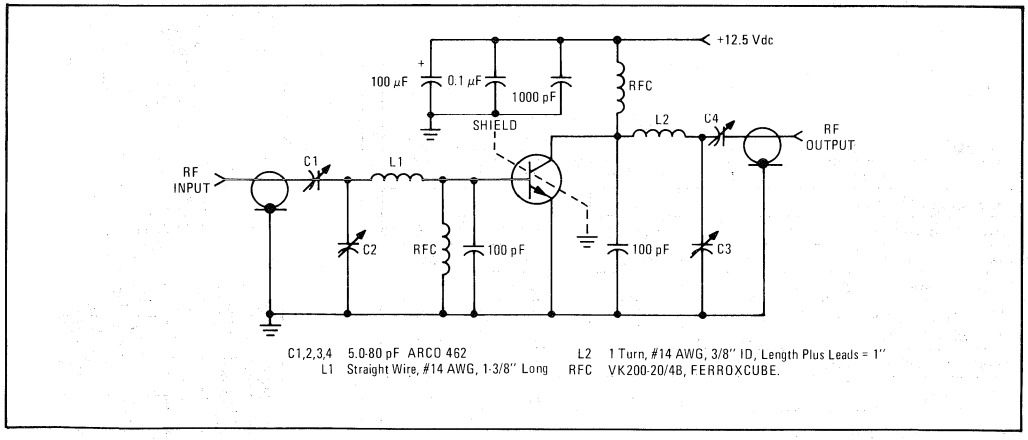
CAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
RACTERISTICS					
r-Emitter Breakdown Voltage = 100 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	–	–	Vdc
ctor-Emitter Breakdown Voltage (I_C = 15 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	–	–	Vdc
mitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = +55°C	I_{CES}	–	–	10	mAdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0	–	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	110	130	pF
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (P_{out} = 25 W, V_{CC} = 12.5 Vdc, f = 175 MHz)	G_{PE}	6.2	–	–	dB
Collector Efficiency (P_{out} = 25 W, V_{CC} = 12.5 Vdc, f = 175 MHz)	η	65	–	–	%

*Indicates JEDEC Registered Data for 2N6082.

3

FIGURE 1 – 175 MHz TEST CIRCUIT



C1,2,3,4 5.0-80 pF ARCO 462
L1 Straight Wire, #14 AWG, 1-3/8" Long
L2 1 Turn, #14 AWG, 3/8" ID, Length Plus Leads = 1"
RFC VK200-20/4B, FERROXCUBE.

FIGURE 2 – OUTPUT POWER versus INPUT POWER

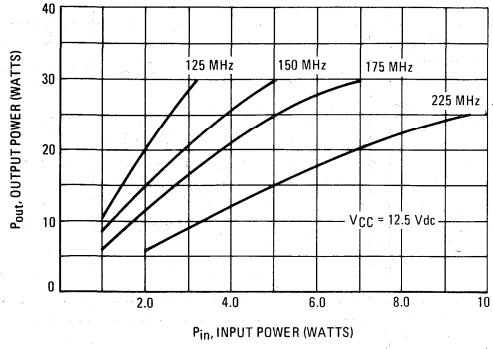


FIGURE 3 – OUTPUT POWER versus SUPPLY V

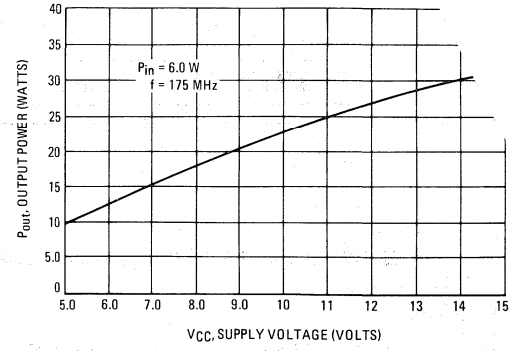
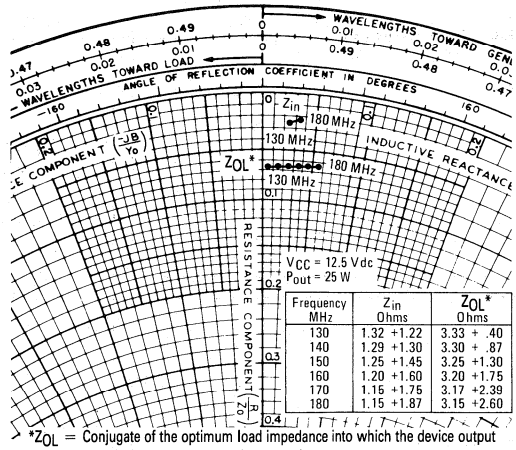


FIGURE 4 – SERIES EQUIVALENT IMPEDANCE



Frequency MHz	Zin Ohms	ZOL* Ohms
130	1.32 +1.22	3.33 + .40
140	1.29 +1.30	3.30 + .87
150	1.25 +1.45	3.25 +1.30
160	1.20 +1.60	3.20 +1.75
170	1.15 +1.75	3.17 +2.39
180	1.15 +1.87	3.15 +2.60

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

2N6083

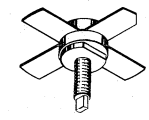
The RF Line

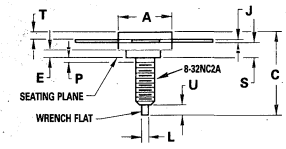
30 W – 175 MHz
RF POWER TRANSISTOR
NPN SILICON

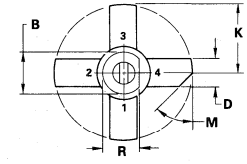
NPN SILICON RF POWER TRANSISTORS

. . . designed for 12.5 Volt VHF large-signal amplifier applications required in commercial and industrial equipment operating to 300 MHz.

- Specified 12.5 Volt, 175 MHz Characteristics –
  Output Power = 30 W
  Minimum Gain = 5.7 dB
  Efficiency = 65%







STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	5.0	Adc
Total Device Dissipation @ T_C = 25°C(2) Derate above 25°C	P_D	65 .37	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +200	°C
Stud Torque(1)	—	6.5	in.lb.

*Indicates JEDEC Registered Data for 2N6083.
(1) For Repeated Assembly Use 5 in. lb.
(2) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	17.02	20.07	0.670	0.790
D	5.46	5.97	0.215	0.235
E	1.78	—	0.070	—
J	0.08	0.18	0.003	0.007
K	12.45	—	0.490	—
L	1.40	1.78	0.055	0.070
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.11	2.54	0.083	0.100
U	2.49	3.35	0.098	0.132

CASE 145A-09

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 15 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = +55°C)	I_{CES}	–	–	10	mAdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0	–	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	110	130	pF
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (P_{out} = 30 W, V_{CC} = 12.5 Vdc, f = 175 MHz)	G_{PE}	5.7	–	–	dB
Collector Efficiency (P_{out} = 30 W, V_{CC} = 12.5 Vdc, f = 175 MHz)	η	65	–	–	%

*Indicates JEDEC Registered Data for 2N6083.

FIGURE 1 – 175 MHz TEST CIRCUIT

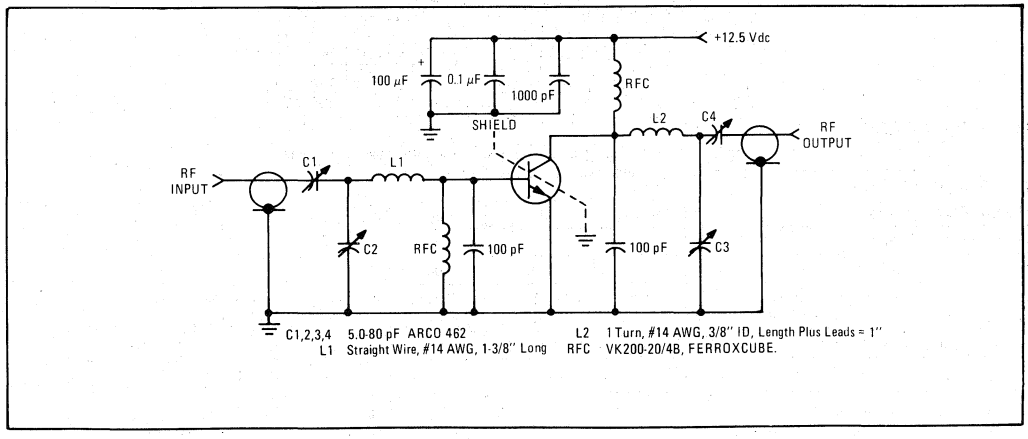


FIGURE 2 – OUTPUT POWER versus INPUT POWER

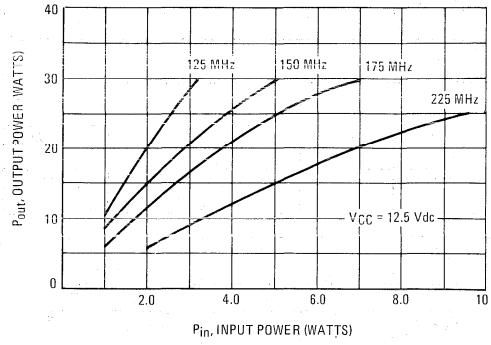


FIGURE 3 – OUTPUT POWER versus SUPPLY VOLTAGE

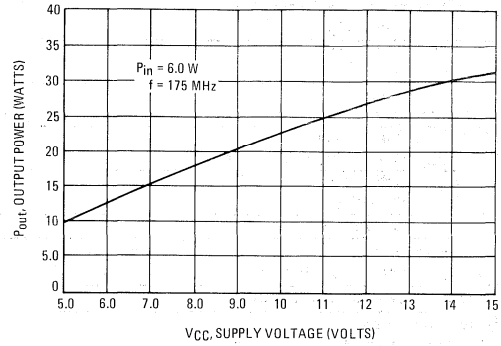
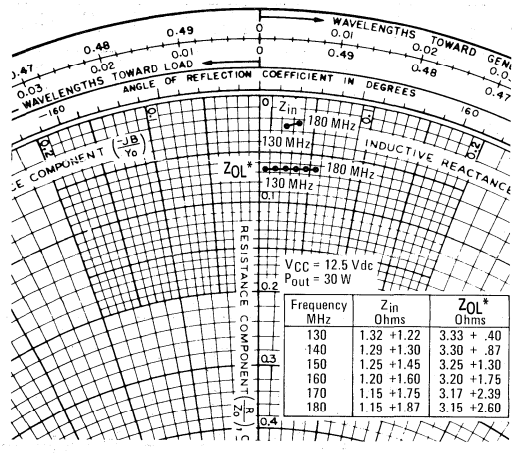


FIGURE 4 – SERIES EQUIVALENT IMPEDANCE



Frequency MHz	Z_{in} Ohms	Z_{OL}^* Ohms
130	1.32 +1.22	3.33 + .40
140	1.29 +1.30	3.30 + .87
150	1.25 +1.45	3.25 +1.30
160	1.20 +1.60	3.20 +1.75
170	1.15 +1.75	3.17 +2.39
180	1.15 +1.87	3.15 +2.60

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

2N6084
MRF224

The RF Line

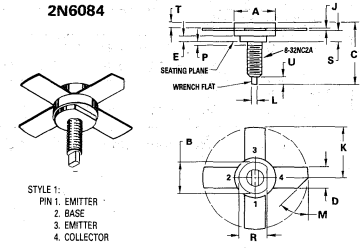
NPN SILICON RF POWER TRANSISTORS

. . . designed for 12.5 Volt VHF large-signal amplifier applications required in commercial and industrial equipment operating to 300 MHz.

- Specified 12.5 Volt, 175 MHz Characteristics —
  Output Power = 40 W
  Minimum Gain = 4.5 dB
  Efficiency = 70%

40 W — 175 MHz
RF POWER
TRANSISTORS
NPN SILICON

2N6084



STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	17.02	20.07	0.670	0.790
D	5.46	5.97	0.215	0.235
E	1.78	—	0.070	—
J	0.08	0.18	0.003	0.007
K	12.45	—	0.490	—
L	1.40	1.78	0.055	0.070
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.11	2.54	0.083	0.100
U	2.49	3.35	0.098	0.132

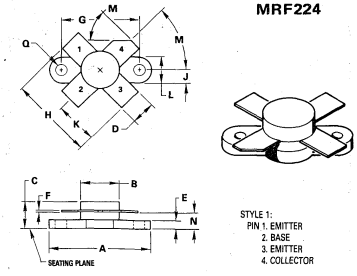
CASE 145A-09

***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	7.0	Adc
Total Device Dissipation @ T_C = 25°C(2) Derate above 25°C	P_D	80 .46	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +200	°C
Stud Torque(1)	—	6.5	in.lb.

*Indicates JEDEC Registered Data for 2N6084.
(1)For Repeated Assembly Use 5 in. lb.
(2)These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

MRF224



STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	9.40	9.91	0.370	0.390
C	5.82	7.14	0.229	0.281
D	5.46	5.97	0.215	0.235
E	2.16	2.67	0.085	0.105
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	20.07	20.57	0.790	0.810
K	10.03	10.29	0.395	0.405
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.81	4.57	0.150	0.180
Q	2.87	3.30	0.113	0.130

CASE 211-07

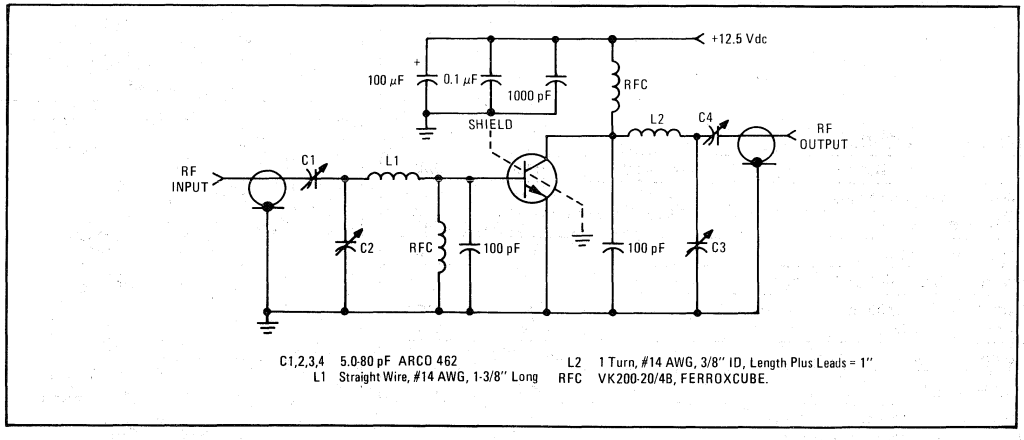
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = +55°C)	I_{CES}	–	–	10	mAdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	2.5	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0	–	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	170	200	pF
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (P_{out} = 40 W, V_{CC} = 12.5 Vdc, f = 175 MHz)	G_{PE}	4.5	–	–	dB
Collector Efficiency (P_{out} = 40 W, V_{CC} = 12.5 Vdc, f = 175 MHz)	η	70	–	–	%

*Indicates JEDEC Registered Data for 2N6084.

3

FIGURE 1 – 175 MHz TEST CIRCUIT



C1,2,3,4 5.0-80 pF ARCO 462
L1 Straight Wire, #14 AWG, 1-3/8" Long
L2 1 Turn, #14 AWG, 3/8" ID, Length Plus Leads = 1"
RFC VK200-20/4B, FERROXCUBE.

FIGURE 2 – OUTPUT POWER versus INPUT POWER

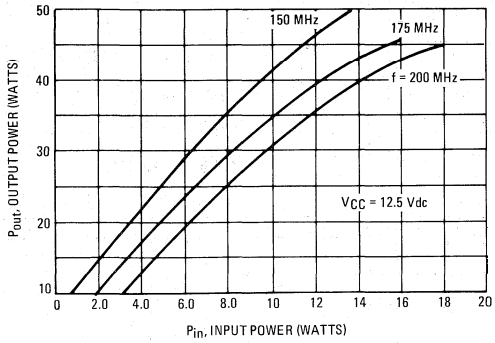


FIGURE 3 – OUTPUT POWER versus SUPPLY VOLTAGE

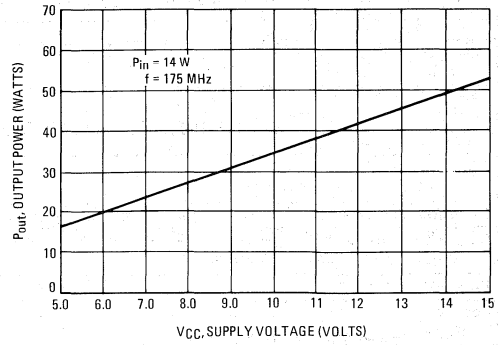
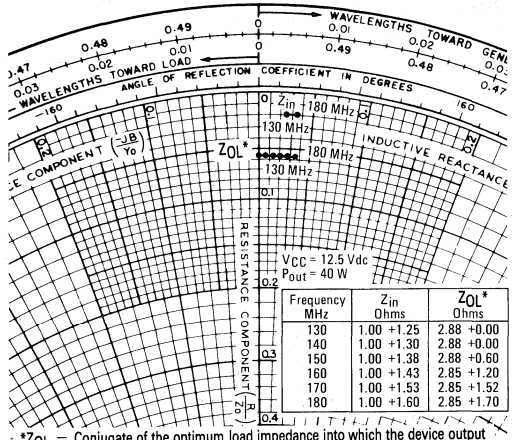


FIGURE 4 – SERIES EQUIVALENT IMPEDANCE



Frequency MHz	Z_{in} Ohms	Z_{OL}^* Ohms
130	1.00 +1.25	2.88 +0.00
140	1.00 +1.30	2.88 +0.00
150	1.00 +1.38	2.88 +0.60
160	1.00 +1.43	2.85 +1.20
170	1.00 +1.53	2.85 +1.52
180	1.00 +1.60	2.85 +1.70

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

2N6166

The RF Line

100 WATTS – 150 MHz

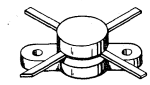
RF POWER
TRANSISTOR

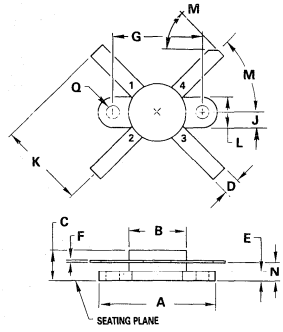
NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed for VHF power amplifier applications in military and industrial equipment. Particularly suited for use in Class AB, B, or C amplifier applications to 200 MHz

- Specified 28-Volt, 150-MHz Characteristics –
  Output Power = 100 Watts
  Minimum Gain = 6.0 dB
  Efficiency = 60%
- Specified 13.5-Volt, 150 MHz Characteristics –
  Output Power = 30 Watts
  Minimum Gain = 4.5 dB
- Parallel Impedance Characterization





STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

NOTE:
1. 211-06 OBS, NEW STD 211-10 FOR REFERENCE, SEE ISSUE "F".

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	11.81	12.95	0.465	0.510
C	5.82	6.98	0.229	0.275
D	2.16	3.94	0.085	0.155
E	2.13	2.79	0.084	0.110
F	0.08	0.18	0.003	0.007
G	18.29	18.54	0.720	0.730
K	17.78	—	0.700	—
L	6.22	6.48	0.245	0.255
M	45° NOM		45° NOM	
N	3.66	4.52	0.144	0.178
Q	2.92	3.30	0.115	0.130

CASE 211-10

3

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	35	Vdc
Collector-Base Voltage	V_{CBO}	65	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current – Continuous	I_C	9.0	Adc
Total Device Dissipation @ $T_C = 25^oC$ (1) Derate above 25^oC	P_D	117 0.667	Watts $W/^oC$
Storage Temperature Range	Tstg	−65 to +150	^oC

THERMAL CHARACTERISTICS

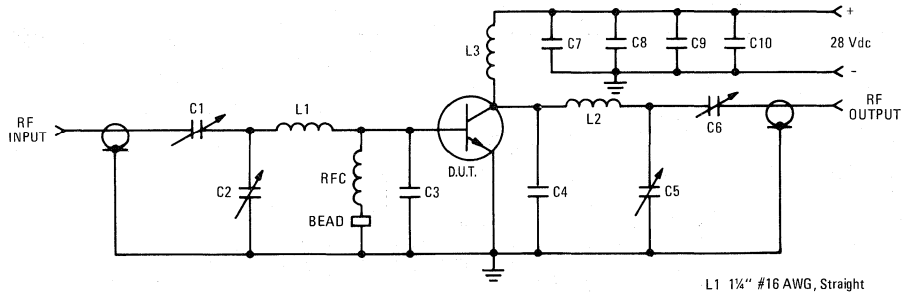
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.5	$^oC/W$

(1) This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF amplifier.

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

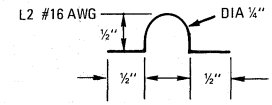
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 200 mAdc, I_B = 0)	$V_{(BR)CEO}$	35	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 200 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	65	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0, T_C = 55°C)	I_{CES}	–	5.0	mAdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	3.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0	–	–
DYNAMIC CHARACTERISTICS				
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	130	pF
FUNCTIONAL TEST				
Common-Emitter Amplifier Power Gain (P_{out} = 100 W, V_{CC} = 28 Vdc, I_C (Max) = 5.95 Adc, f = 150 MHz)	G_{PE}	6.0	–	dB
Common-Emitter Amplifier Power Gain (P_{out} = 30 W, V_{CC} = 13.5 V, f = 150 MHz)	G_{PE}	4.5	–	dB
Collector Efficiency (P_{out} = 100 W, V_{CC} = 28 Vdc, I_C (Max) = 5.95 Adc, f = 150 MHz)	η	60	–	%

FIGURE 1 – 150 MHz TEST CIRCUIT

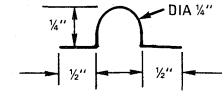


C1, C6 2.7-30 pF, Arco 461 or Equivalent
C2, C5 9.0-180 pF, Arco 463 or Equivalent
C3 100 pF Underwood
C4 25 pF Underwood
C7 0.01 μF Ceramic Disc
C8 0.1 μF Ceramic Disc
C9 2400 pF Button
C10 5.0 μF/50 V
RFC 0.15 μH J. W. Miller
BEAD: FERROXCUBE 56-590-65-3B

L1 1¼" #16 AWG, Straight



L3 1/8" Wide Copper Strap



OUTPUT POWER versus FREQUENCY

FIGURE 2 – V_{CC} = 28 Vdc

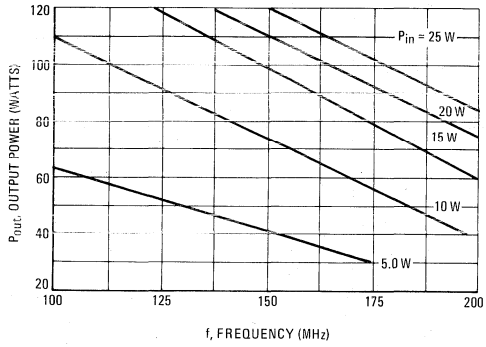


FIGURE 3 – V_{CC} = 13.5 Vdc

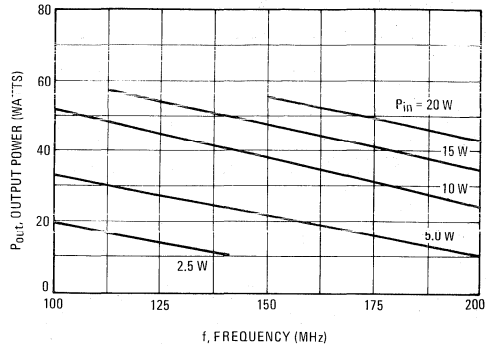


FIGURE 4 – OUTPUT POWER versus INPUT POWER

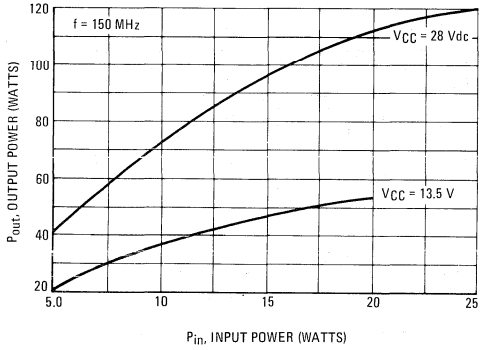


FIGURE 5 – OUTPUT POWER versus SUPPLY VOLTAGE

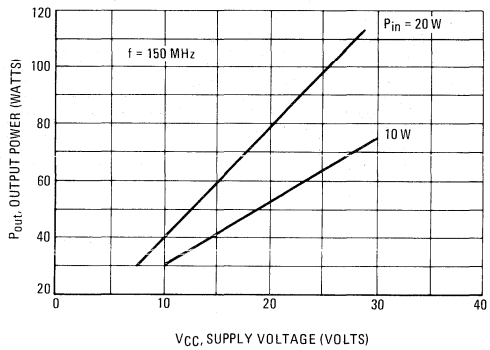


FIGURE 6 – PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

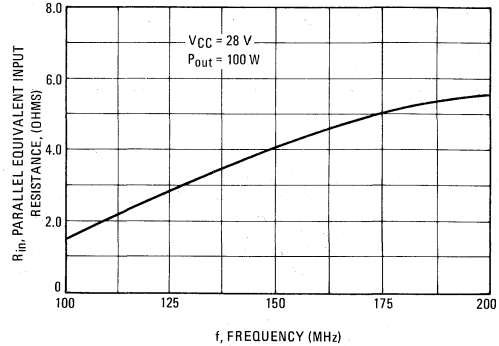


FIGURE 7 – PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

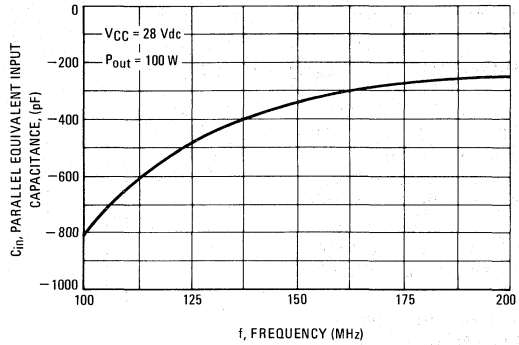
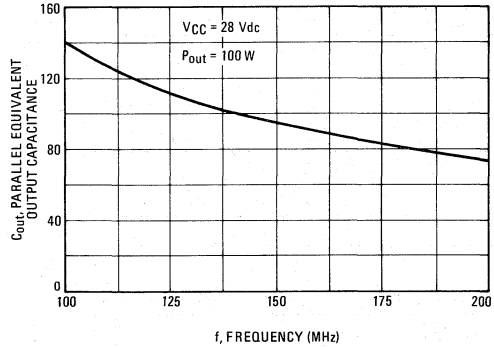


FIGURE 8 – PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY



3

2N6304
2N6305

The RF Line

NPN SILICON HIGH-FREQUENCY TRANSISTORS

. . . designed for use as low-noise, high-gain, general-purpose amplifiers.

- High Current-Gain – Bandwidth Product –
  f_T = 1.4 GHz (Min) @ I_C = 10 mAdc – 2N6304
  = 1.2 GHz (Min) @ I_C = 10 mAdc – 2N6305
- Low Noise Figure –
  NF = 4.5 dB (Max) @ f = 450 MHz – 2N6304
  = 5.5 dB (Max) @ f = 450 MHz – 2N6305
- High Power Gain –
  G_{pe} = 15 dB (Min) @ f = 450 MHz – 2N6304
  = 12 dB (Min) @ f = 450 MHz – 2N6305

1.4 GHz @ 10 mAdc – 2N6304
1.2 GHz @ 10 mAdc – 2N6305

HIGH FREQUENCY TRANSISTORS

NPN SILICON



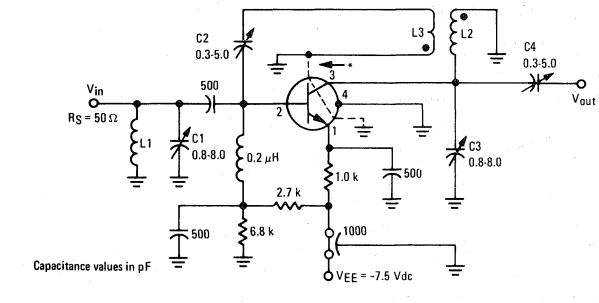
3

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage 1.0 to 20 mAdc	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CBO}	30	Vdc
Emitter-Base Voltage	V_{EBO}	3.0	Vdc
Collector Current Continuous	I_C	50	mAdc
Total Continuous Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	200 1.14	mW mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.

FIGURE 1 – TEST CIRCUIT FOR NOISE FIGURE AND POWER GAIN



L1, L2 – Silver-plated brass rod, 1-1/2" long and 1/4" dia. Install at least 1/2" from nearest vertical chassis surface.

L3 – 1/2 turn #16 AWG wire, located 1/4" from and parallel to L2.

* – External interlead shield to isolate collector lead from emitter and base leads.

Neutralization Procedure:

(A) Connect 450-MHz signal generator (with R_S = 50 ohms) to input terminals of amplifier.

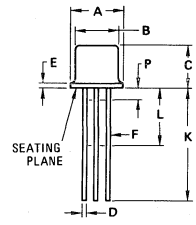
(B) Connect 50-ohm RF voltmeter across output terminals of amplifier.

(C) Apply V_{EE}, and with signal generator adjusted for 5 mV output from amplifier, tune C1, C3, and C4 for maximum output.

(D) Interchange connections to signal generator and RF voltmeter.

(E) With sufficient signal applied to output terminals of amplifier, adjust C2 for minimum indication at input.

(F) Repeat steps (A), (B), and (C) to determine if retuning is necessary.



STYLE 10
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. CASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

CASE 20-03
TO-72

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)		$V_{(BR)CEO}$	15	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)		$V_{(BR)CBO}$	30	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)		$V_{(BR)EBO}$	3.5	–	–	Vdc
Collector Cutoff Current (V_{CB} = 5.0 Vdc, I_E = 0)		I_{CBO}	–	–	10	nAdc
ON CHARACTERISTICS						
DC Current Gain (I_C = 2.0 mAdc, V_{CE} = 5.0 Vdc)		h_{FE}	25	–	250	–
DYNAMIC CHARACTERISTICS						
Current-Gain–Bandwidth Product (I_C = 10 mAdc, V_{CE} - 5.0 Vdc, f - 100 MHz)	2N6304 2N6305	f_T	1400 1200	– –	– –	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{cb}	–	0.8	1.0	pF
Small-Signal Current Gain (I_C = 2.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)		h_{fe}	25	–	250	–
Collector-Base Time Constant (I_E = 2.0 mAdc, V_{CB} = 5.0 Vdc, f = 31.8 MHz)	2N6304 2N6305	$r_b'C_c$	2.0 2.0	–	12 15	ps
Noise Figure (I_C = 2.0 mAdc, V_{CE} = 5.0 Vdc, R_S = 50 ohms, f = 450 MHz) (Figure 1)	2N6304 2N6305	NF	– –	– –	4.5 5.5	dB
FUNCTIONAL TEST						
Common-Emitter Amplifier Power Gain (I_C = 2.0 mAdc, V_{CE} = 5.0 Vdc, f = 450 MHz) (Figure 1)	2N6304 2N6305	G_{pe}	15 12	– –	– –	dB

*Indicates JEDEC Registered Data.

FIGURE 2 – COLLECTOR-BASE CAPACITANCE versus COLLECTOR BASE VOLTAGE

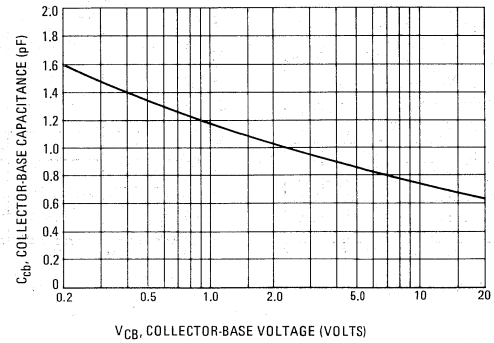


FIGURE 3 – CURRENT-GAIN-BANDWIDTH PRODUCT versus COLLECTOR CURRENT

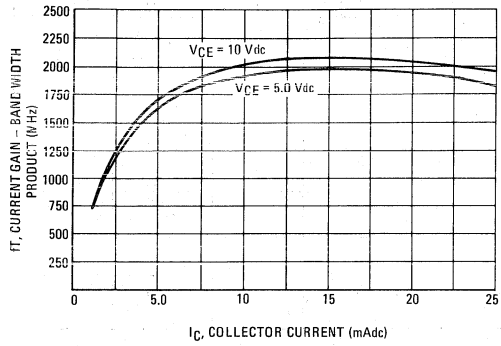


FIGURE 4 – COLLECTOR-BASE TIME CONSTANT versus EMITTER CURRENT

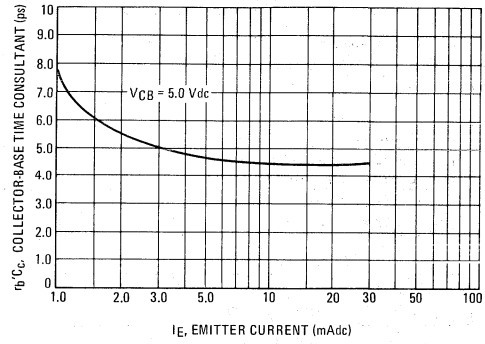


FIGURE 5 – REVERSE TRANSFER ADMITTANCE versus FREQUENCY

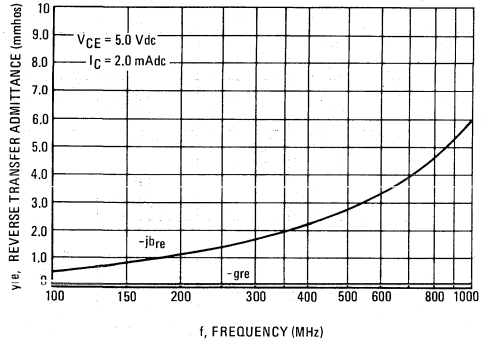


FIGURE 6 – INPUT ADMITTANCE versus FREQUENCY

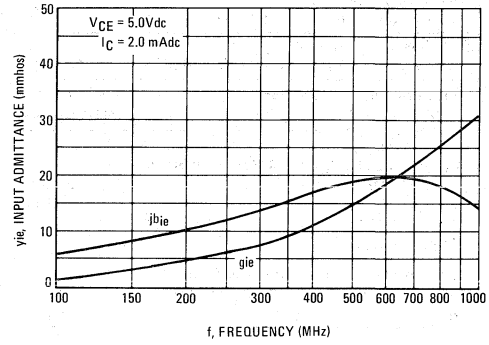


FIGURE 7 – OUTPUT ADMITTANCE versus FREQUENCY

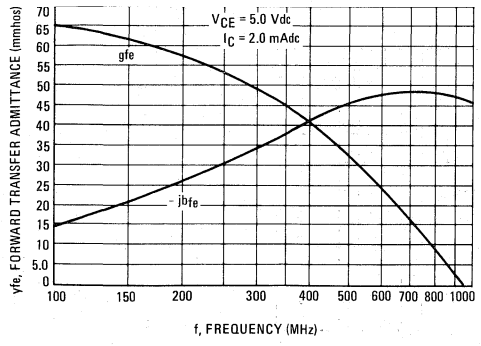


FIGURE 8 – FORWARD TRANSFER ADMITTANCE versus FREQUENCY

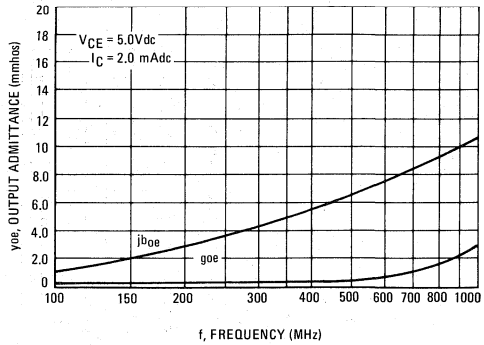


FIGURE 9 – S_{11}, INPUT REFLECTION COEFFICIENT

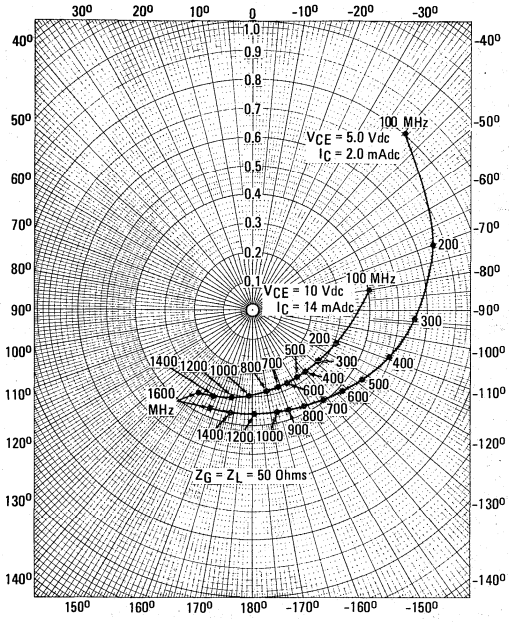


FIGURE 10 – S_{22}, OUTPUT REFLECTION COEFFICIENT

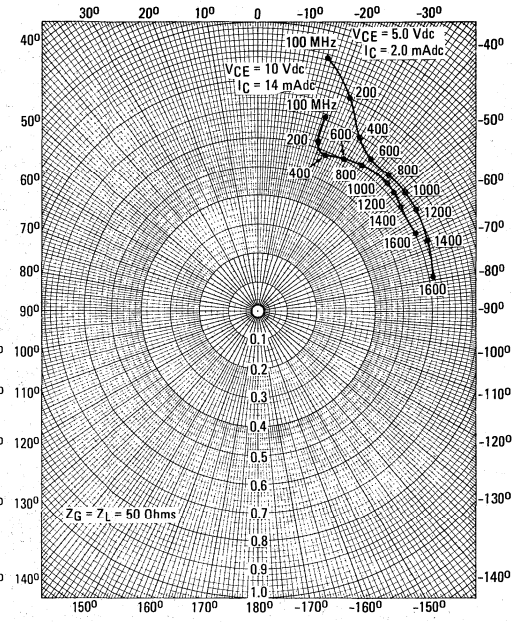


FIGURE 11 – S_{12}, REVERSE TRANSMISSION COEFFICIENT

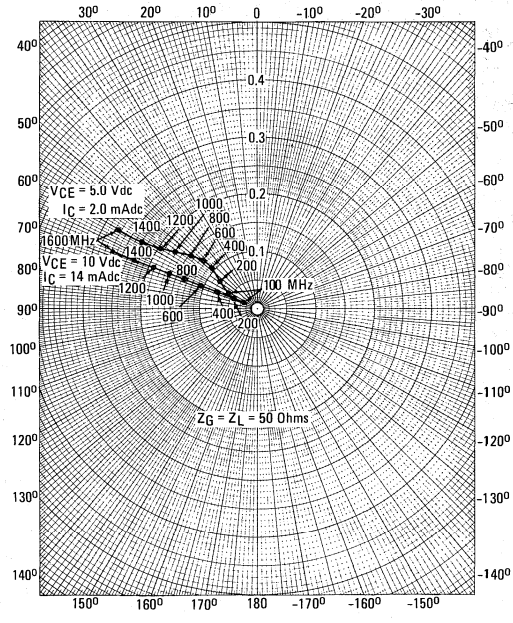
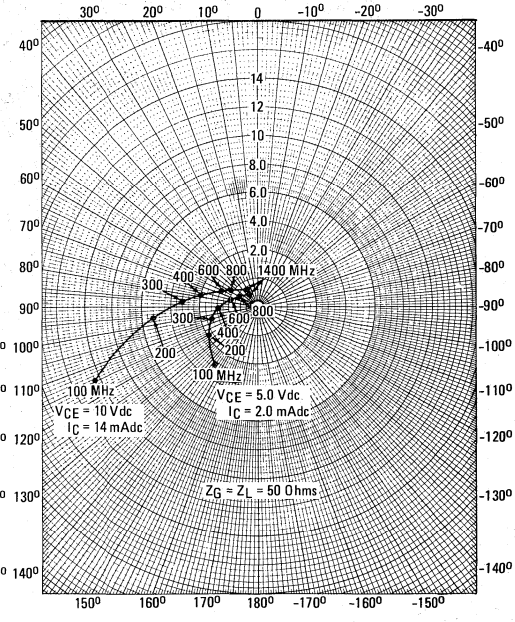
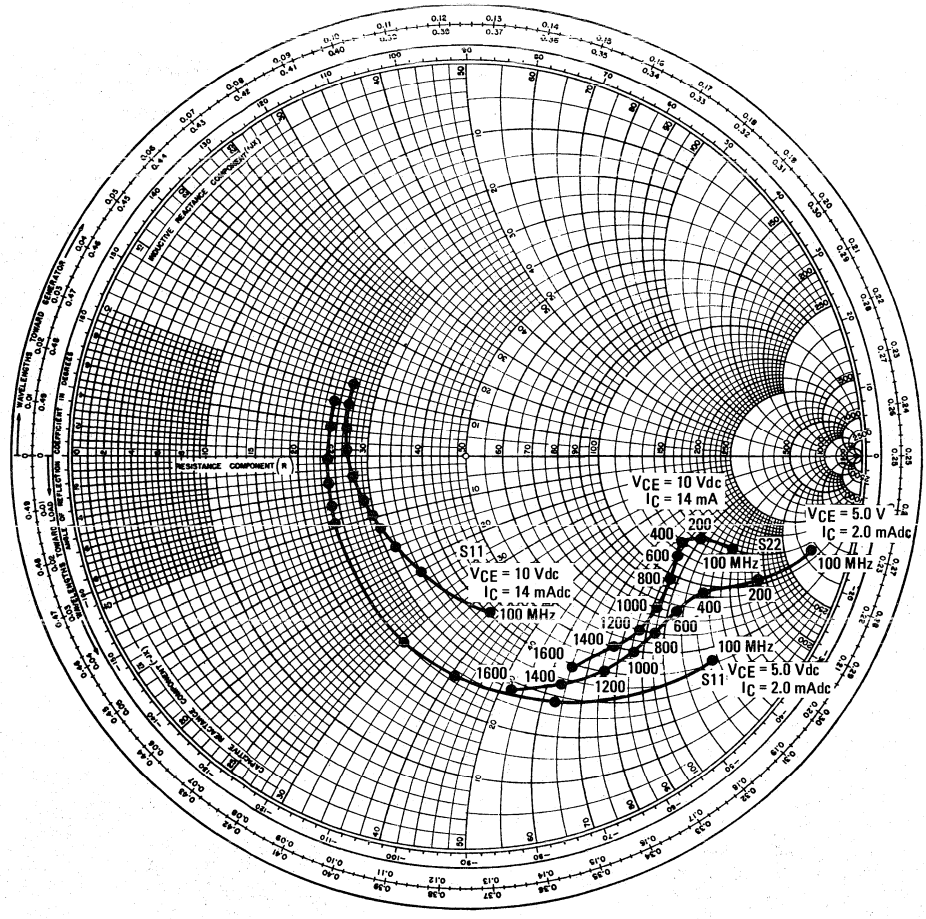


FIGURE 12 – S_{21}, FORWARD TRANSMISSION COEFFICIENT



3

FIGURE 13 – S_{11}, INPUT REFLECTION COEFFICIENT AND S_{22}, OUTPUT REFLECTION COEFFICIENT



2N6439

The RF Line

NPN SILICON RF POWER TRANSISTOR

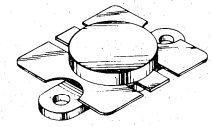
. . . designed primarily for wideband large-signal output amplifier stages in the 225-400 MHz frequency range.

- Guaranteed Performance in 225–400 MHz Broadband Amplifier @ 28 Vdc
  Output Power = 60 Watts over 225–400 MHz Band
  Minimum Gain = 7.8 dB @ 400 MHz
- Built-In Matching Network for Broadband Operation Using Double Match Technique
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR
- Gold Metallization System for High Reliability Applications

60 W – 225–400 MHz

CONTROLLED "Q" BROADBAND RF POWER TRANSISTOR

NPN SILICON



3

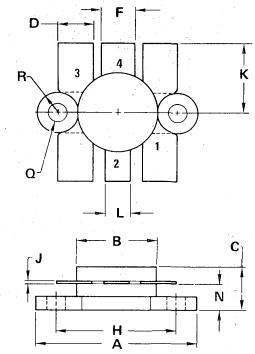
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	33	Vdc
Collector-Base Voltage	V_{CBO}	60	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	146 0.83	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.2	°C/W

(1)These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.



STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. EMITTER
4. BASE

NOTE: FLANGE IS ISOLATED IN ALL STYLES.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.14	0.960	0.990
B	12.45	12.95	0.490	0.510
C	5.97	7.62	0.235	0.300
D	5.33	5.58	0.210	0.220
E	2.16	3.04	0.085	0.120
F	5.08	5.33	0.200	0.210
H	18.29	18.54	0.720	0.730
J	0.10	0.15	0.004	0.006
K	10.29	11.17	0.405	0.440
L	3.81	4.06	0.150	0.160
N	3.81	4.31	0.150	0.170
Q	2.92	3.30	0.115	0.130
R	3.05	3.30	0.120	0.130
U	11.94	12.57	0.470	0.495

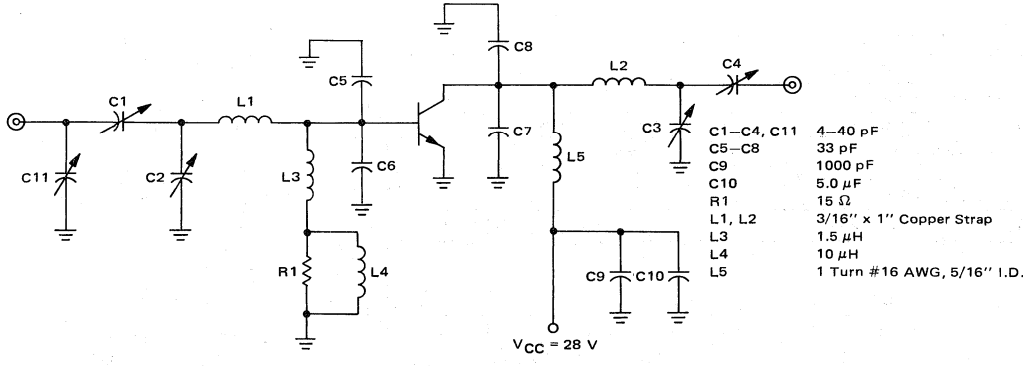
CASE 316-01

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	33	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	–	100	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	67	75	pF
BROADBAND FUNCTIONAL TESTS (Figure 6)					
Common-Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 60 W, f = 225–400 MHz)	G_{PE}	7.8	8.5	–	dB
Electrical Ruggedness (P_{out} = 60 W, V_{CC} = 28 Vdc, f = 400 MHz, VSWR 30:1 all phase angles)	–	No Degradation in P_{out}			–
NARROW BAND FUNCTIONAL TESTS (Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 60 W, f = 400 MHz)	G_{PE}	7.8	10	–	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 60 W, f = 400 MHz)	η	55	–	–	%

3

FIGURE 1 – 400 MHz TEST AMPLIFIER (NARROW BAND)



NARROW BAND DATA

FIGURE 2 — P_{out} versus FREQUENCY

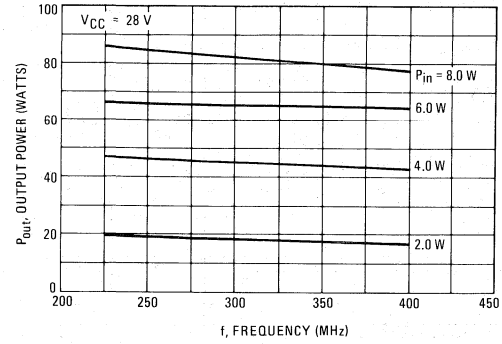


FIGURE 3 — OUTPUT POWER versus INPUT POWER

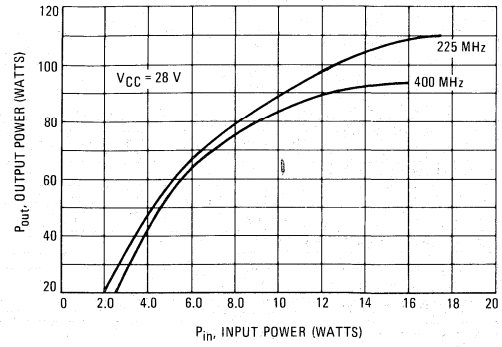


FIGURE 4 — POWER-GAIN versus FREQUENCY

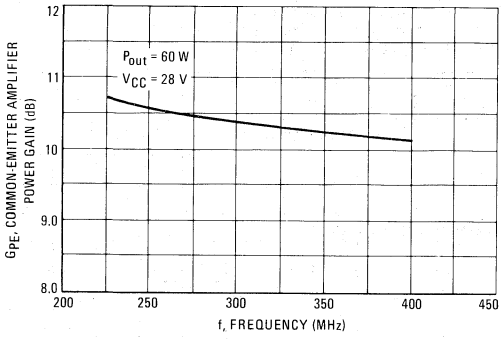


FIGURE 5 — OUTPUT POWER versus SUPPLY VOLTAGE

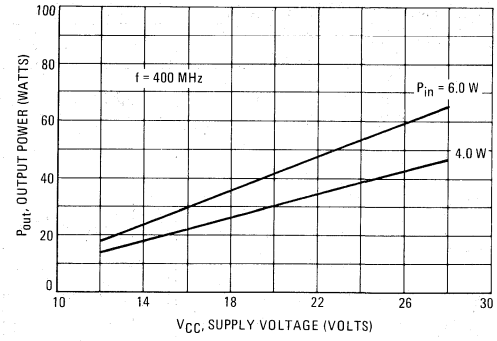


FIGURE 6 — OUTPUT POWER versus SUPPLY VOLTAGE

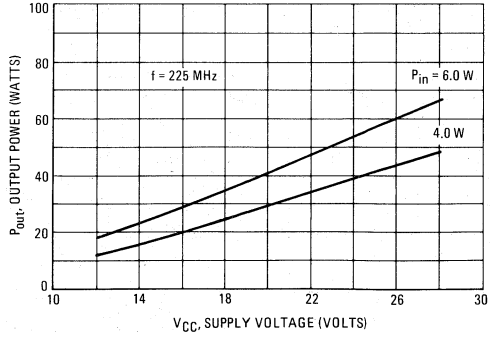
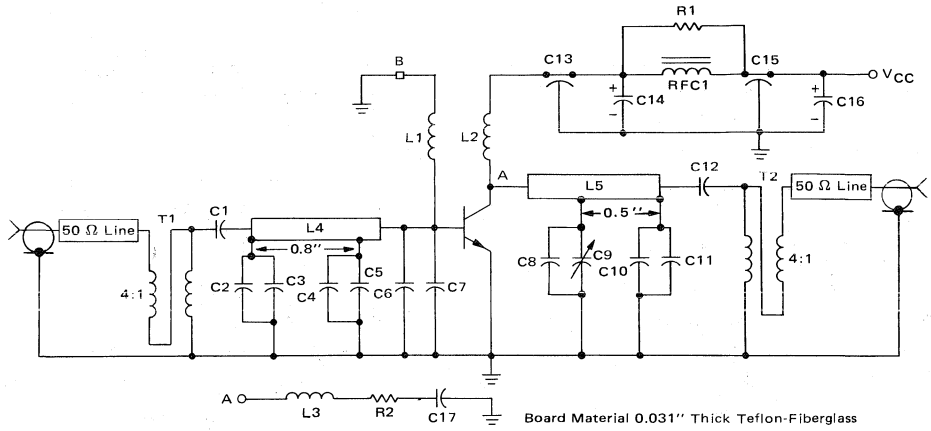


FIGURE 7 — 225-400 MHz BROADBAND TEST CIRCUIT SCHEMATIC



C1	68 pF	RFC1	Ferrite Bead Choke, Ferroxcube VK200 19/4B
C2, C4, C8, C10	27 pF	B	Ferroxcube 56-590-65/4B Ferrite Bead
C3, C5, C11	10 pF	T1, T2	25 Ohms (UT25) Miniature Coaxial Cable, 1 turn
C6, C7	51 pF	R1	11 Ω, 1 W
C9	1–10 pF JOHANSON	R2	20 Ω, 1/4 W
C12	100 pF	L1	10 Turns, #22 AWG, 1/8″ I.D.
C13, C15	680 pF	L2	4 Turns, #16 AWG, 1/4″ I.D.
C14, C16	1.0 μF, 35 V Tantalum	L3	6 Turns, #24 AWG, 1/8″ I.D.
C17	0.1 μF, ERIE Red Cap	L4, L5	1″ x 0.25″ Microstrip Line

Board Material 0.031″ Thick Teflon-Fiberglass

BROADBAND DATA (Circuit, Figure 7)

FIGURE 8 — POWER GAIN versus FREQUENCY

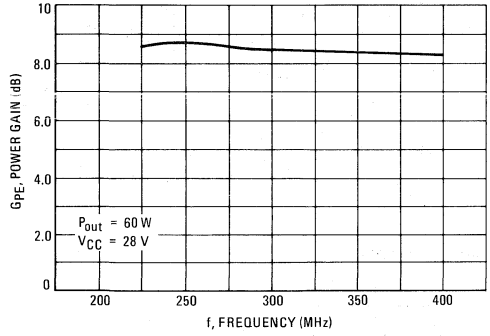


FIGURE 9 — EFFICIENCY versus FREQUENCY

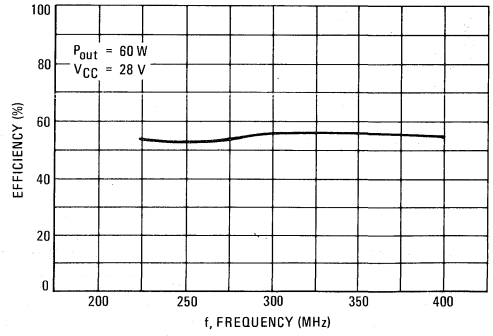


FIGURE 10 — INPUT VSWR versus FREQUENCY

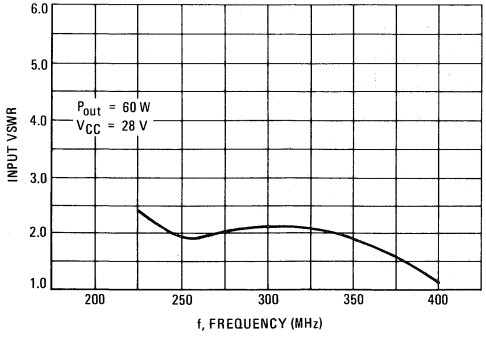
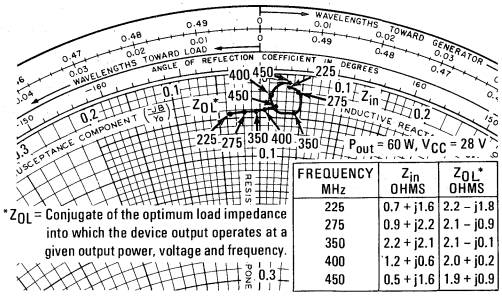


FIGURE 11 — SERIES EQUIVALENT INPUT-OUTPUT IMPEDANCE



FREQUENCY MHz	Z_{in} OHMS	Z_{OL}^* OHMS
225	0.7 + j1.6	2.2 – j1.8
275	0.9 + j2.2	2.1 – j0.9
350	2.2 + j2.1	2.1 – j0.1
400	1.2 + j0.6	2.0 + j0.2
450	0.5 + j1.6	1.9 + j0.9

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

2N6603

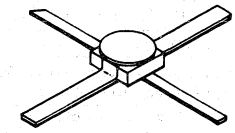
The RF Line

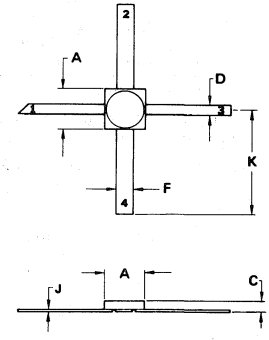
NF = 2.0 dB @ 1.0 GHz
HIGH FREQUENCY TRANSISTOR
NPN SILICON

NPN SILICON HIGH FREQUENCY TRANSISTOR

... designed for use in high-gain, low-noise, small signal, narrow and wideband amplifiers. Ideal for use in microstrip thin and thick film applications.

- Low Noise Figure –
  NF = 2.0 dB (Typ) @ f = 1.0 GHz
  = 2.9 dB (Typ) @ f = 2.0 GHz
- High Power Gain –
  MAG = 17 dB (Typ) @ f = 1.0 GHz
  = 11 dB (Typ) @ f = 2.0 GHz
- Ion Implantation and Gold Metallization
- Metal/Ceramic Hermetic Package
- JAN, JTX, JTXV Available





***MAXIMUM RATINGS (T_A = 25°C Free Air Temperature)**

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CBO}	25	Vdc
Emitter-Base Voltage	V_{EBO}	3.0	Vdc
Collector Current—Continuous	I_C	30	mAdc
Total Device Dissipation @ T_C = 125°C	P_D	400	mW
Derate Above 100°C		5.33	mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.29	2.67	0.090	0.105
C	0.89	1.40	0.035	0.055
D	0.41	0.61	0.016	0.024
F	0.89	1.09	0.035	0.043
J	0.08	0.15	0.003	0.006
K	4.45	5.84	0.175	0.230

NOTE:
1. DIMENSION K APPLIES TO ALL LEADS.

STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. BASE
4. EMITTER

CASE 303-01

Specification and Package Options

Devices using the same die type as the 2N6603:

MRF901 – 4 Lead Plastic Macro-T Case 302-01
MRF902 – 100 mil Metal/Ceramic Case 303-01
MRF904 – TO-72
MMBR901 – MiniBloc Plastic (SOT-23) TO-236
MRFC901 – Unencapsulated Chip

3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	15	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	25	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	50	nAdc
***ON CHARACTERISTICS**					
DC Current Gain (I_C = 15 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	–	200	–
***DYNAMIC CHARACTERISTICS**					
Collector-Base Capacitance (1) (V_{CB} = 10 Vdc, I_E = 0, 0.1 MHz ≤ f ≤ 1.0 MHz)	C_{cb}	0.25	–	0.75	pF
***FUNCTIONAL TEST**					
Common-Emitter Amplifier Power Gain (V_{CE} = 10 Vdc, I_C = 15 mA, f = 1.0 GHz–Figure 2)	G_{pe}	15	–	21	dB
Spot Noise Figure (R_S = Optimum–Figure 2) (V_{CE} = 10 Vdc, I_C = 5.0 mA, f = 1.0 GHz)	NF	1.0	–	2.5	dB
Power Gain at Optimum Noise Figure (V_{CE} = 10 Vdc, I_C = 5.0 mA, f = 1.0 GHz)	G_{NF}	10	–	–	dB
TYPICAL 2 GHz PERFORMANCE					
Maximum Available Gain (Figure 2) (2) (V_{CE} = 10 Vdc, I_C = 15 mA, f = 2.0 GHz)	MAG	–	11	–	dB
Noise Figure (R_S = Optimum–Figure 2) (V_{CE} = 10 Vdc, I_C = 5.0 mA, f = 2.0 GHz)	NF	–	2.9	–	dB

*Indicates JEDEC Registered Data.

(1) C_{cb} measurement employs a three-terminal capacitance bridge incorporating a guard circuit. The emitter terminal shall be connected to the guard terminal of the bridge.

(2) MAG is calculated from the S-Parameters using the equation $MAG = \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)}$

FIGURE 1 – BLOCK DIAGRAM FOR POWER GAIN AND NOISE FIGURE

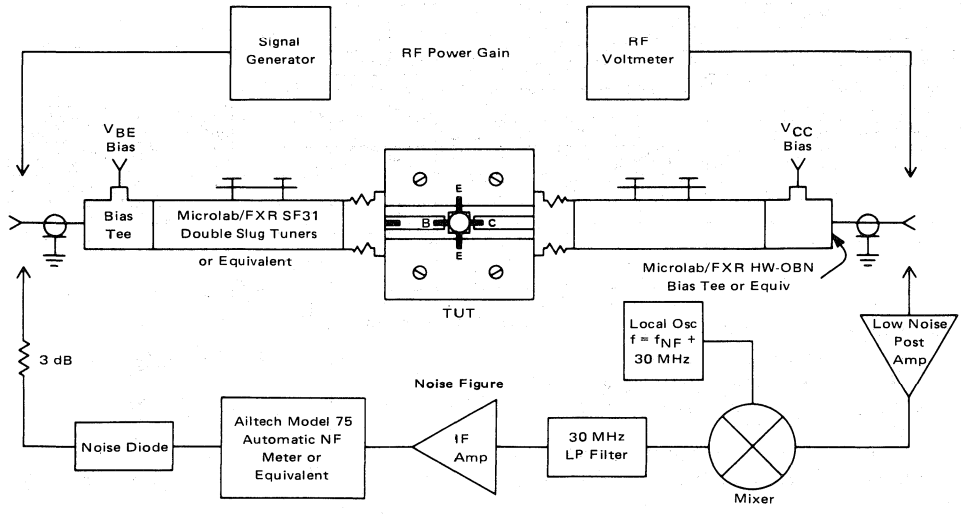


FIGURE 2 – POWER GAIN AND NOISE FIGURE versus FREQUENCY

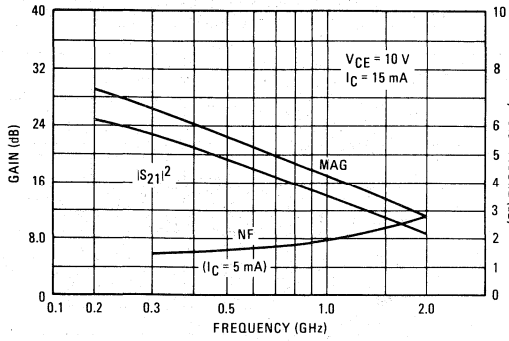


FIGURE 3 – OUTPUT CAPACITANCE versus VOLTAGE

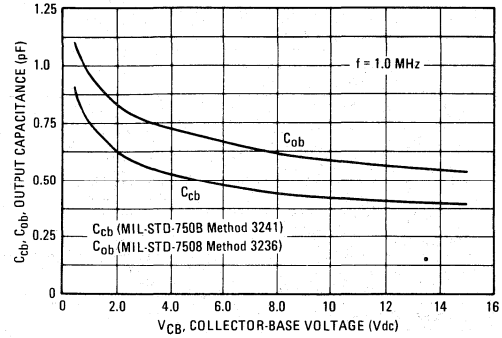


FIGURE 4 – CURRENT GAIN–BANDWIDTH PRODUCT versus COLLECTOR CURRENT

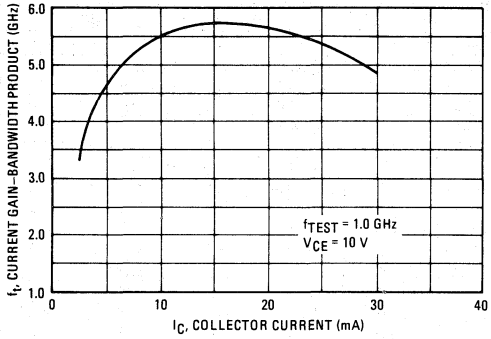


FIGURE 5 – POWER GAIN versus COLLECTOR CURRENT

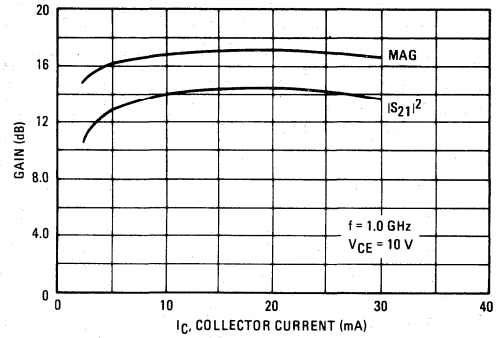
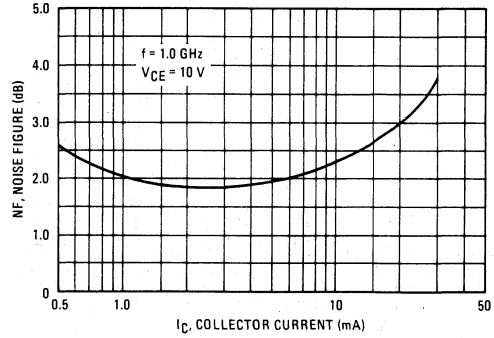
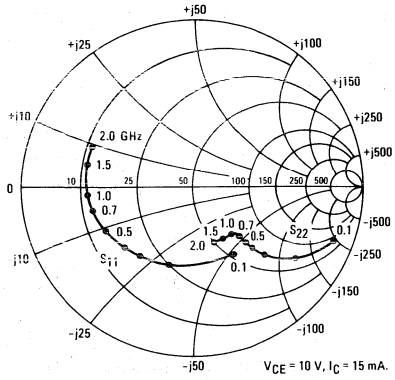


FIGURE 6 – NOISE FIGURE versus COLLECTOR CURRENT



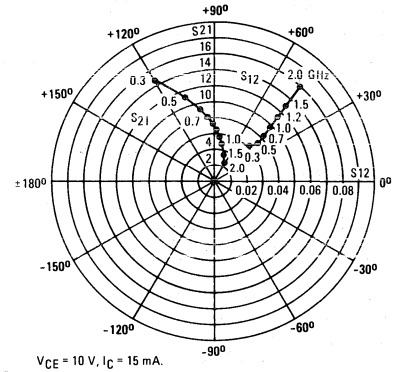
COMMON EMITTER SCATTERING PARAMETERS

FIGURE 7 – INPUT AND OUTPUT REFLECTION COEFFICIENTS versus FREQUENCY



V_{CE} = 10 V, I_C = 15 mA.

FIGURE 8 – FORWARD AND REVERSE TRANSMISSION COEFFICIENTS versus FREQUENCY



V_{CE} = 10 V, I_C = 15 mA.

S – PARAMETERS

V_{CE} (Volts)	I_C (mA)	Frequency (MHz)	S11		S21		S12		S22	
			|S11|	∠φ	|S21|	∠φ	|S12|	∠φ	|S22|	∠φ
5.0	5	100	0.69	−30	12.16	160	0.026	72	0.95	−16
		200	0.65	−61	11.03	143	0.046	59	0.84	−31
		500	0.63	−122	7.05	111	0.074	36	0.56	−54
		1000	0.64	−158	4.13	88	0.087	28	0.39	−68
		2000	0.65	170	2.14	61	0.107	29	0.33	−91
	10	100	0.52	−50	18.74	154	0.022	69	0.91	−22
		200	0.54	−92	15.53	135	0.037	53	0.74	−40
		500	0.62	−146	8.49	104	0.052	38	0.43	−62
		1000	0.65	−172	4.66	84	0.065	37	0.29	−75
		2000	0.67	162	2.38	60	0.094	42	0.26	−97
	15	100	0.42	−70	22.72	150	0.019	66	0.87	−26
		200	0.51	−113	17.72	130	0.030	50	0.68	−44
		500	0.63	−157	8.96	100	0.042	41	0.38	−64
		1000	0.66	−178	4.80	82	0.056	44	0.26	−75
		2000	0.69	159	2.43	59	0.090	48	0.24	−97
	30	100	0.39	−116	24.57	142	0.014	62	0.80	−29
		200	0.55	−145	17.17	120	0.021	49	0.58	−42
		500	0.67	−171	7.96	95	0.030	49	0.34	−49
		1000	0.69	175	4.18	78	0.047	56	0.29	−56
		2000	0.71	157	2.13	55	0.084	58	0.29	−81
10	5	100	0.71	−27	12.01	161	0.021	73	0.96	−13
		200	0.67	−55	11.10	145	0.039	60	0.87	−25
		500	0.63	−115	7.44	114	0.064	39	0.62	−44
		1000	0.64	−153	4.43	90	0.077	30	0.46	−55
		2000	0.64	172	2.27	62	0.094	31	0.39	−76
	10	100	0.55	−43	18.77	155	0.018	71	0.92	−18
		200	0.55	−83	16.00	137	0.031	54	0.78	−32
		500	0.60	−140	9.06	106	0.046	39	0.49	−48
		1000	0.63	−168	5.02	85	0.058	39	0.36	−56
		2000	0.65	164	2.55	60	0.084	43	0.33	−76
	15	100	0.46	−60	23.14	152	0.016	68	0.90	−21
		200	0.51	−103	18.39	131	0.027	52	0.72	−36
		500	0.61	−152	9.67	102	0.037	42	0.43	−49
		1000	0.64	−175	5.21	83	0.049	45	0.33	−54
		2000	0.66	161	2.61	59	0.079	51	0.31	−74
	30	100	0.39	−98	27.29	144	0.013	63	0.83	−24
		200	0.53	−135	19.38	122	0.019	50	0.63	−35
		500	0.64	−167	9.11	96	0.027	48	0.41	−39
		1000	0.66	177	4.77	79	0.042	55	0.36	−45
		2000	0.69	157	2.41	56	0.074	58	0.35	−67

2N6604

The RF Line

NF = 2.7 dB @ 1.0 GHz

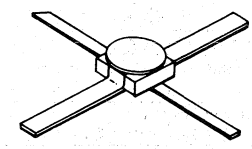
HIGH FREQUENCY TRANSISTOR

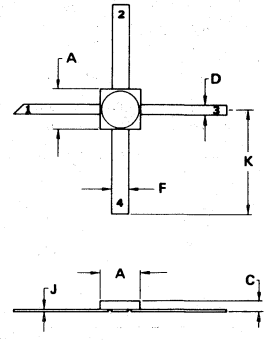
NPN SILICON

NPN SILICON HIGH FREQUENCY TRANSISTOR

. . . designed for use in high-frequency, low-noise, small-signal, narrow and wideband amplifiers. Ideal for use in microstrip thin and thick film applications.

- Low Noise Figure — NF = 2.7 dB (Typ) @ f = 1.0 GHz
- High Power Gain — G_U(max) = 16 dB (Typ) @ f = 1.0 GHz
- High Current — Specified Performance @ I_C = 30 mA
- Ion Implantation and Gold Metallization
- Metal/Ceramic Hermetic Package
- JAN, JTXV Available





*MAXIMUM RATINGS (T_A = 25°C Free Air Temperature)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CBO}	25	Vdc
Emitter-Base Voltage	V_{EBO}	3.0	Vdc
Collector Current—Continuous	I_C	50	mAdc
Total Device Dissipation @ T_C = 125°C Derate Above 75°C	P_D	500 6.66	mW mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.29	2.67	0.090	0.105
C	0.89	1.40	0.035	0.055
D	0.41	0.61	0.016	0.024
F	0.89	1.09	0.035	0.043
J	0.08	0.15	0.003	0.006
K	4.45	5.84	0.175	0.230

NOTE:
1. DIMENSION K APPLIES TO ALL LEADS.

STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. BASE
4. EMITTER

CASE 303-01

Specifications and Package Options

Devices using the same die type as the 2N6604:

MRF911 — 4 Lead Plastic Macro-T Case 302-01
MRF914 — TO-72
MMBR930 — MiniBloc Plastic (SOT-23) TO-236
BFR91 — 3 Lead Plastic Macro-T Case 302A-01
BFRC91 — Unencapsulated Chip

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	15	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	25	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	50	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 30 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	–	200	–
***DYNAMIC CHARACTERISTICS**					
Collector-Base Capacitance (1) (V_{CB} = 10 Vdc, I_E = 0, 0.1 MHz ≤ f ≤ 1.0 MHz)	C_{cb}	0.30	–	0.80	pF
***FUNCTIONAL TEST**					
Common-Emitter Amplifier Power Gain (Figure 2) (V_{CE} = 10 Vdc, I_C = 30 mAdc, f = 1.0 GHz)	G_{pe}	15	–	21	dB
Spot Noise Figure (R_S = Optimum – Figure 2) (V_{CE} = 10 Vdc, I_C = 5.0 mAdc, f = 1.0 GHz)	NF	1.5	–	3.0	dB
Power Gain at Optimum Noise Figure (V_{CE} = 10 Vdc, I_C = 5.0 mAdc, f = 1.0 GHz)	G_{NF}	9.0	–	–	dB
TYPICAL 2 GHz PERFORMANCE					
Maximum Unilateral Gain (Figure 2) (2) (V_{CE} = 10 Vdc, I_C = 30 mAdc, f = 2.0 GHz)	G_U(max)	–	10	–	dB
Noise Figure (R_S = Optimum – Figure 2) (V_{CE} = 10 Vdc, I_C = 5.0 mAdc, f = 2.0 GHz)	NF	–	4.3	–	dB

*Indicates JEDEC Registered Data.

(1) C_{cb} measurement employs a three-terminal capacitance bridge incorporating a guard circuit. The emitter terminal shall be connected to the guard terminal of the bridge.

(2) G_U(max) is calculated from the S-Parameters using the equation $G_U(max) = \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)}$

FIGURE 1 – BLOCK DIAGRAM FOR POWER GAIN AND NOISE FIGURE

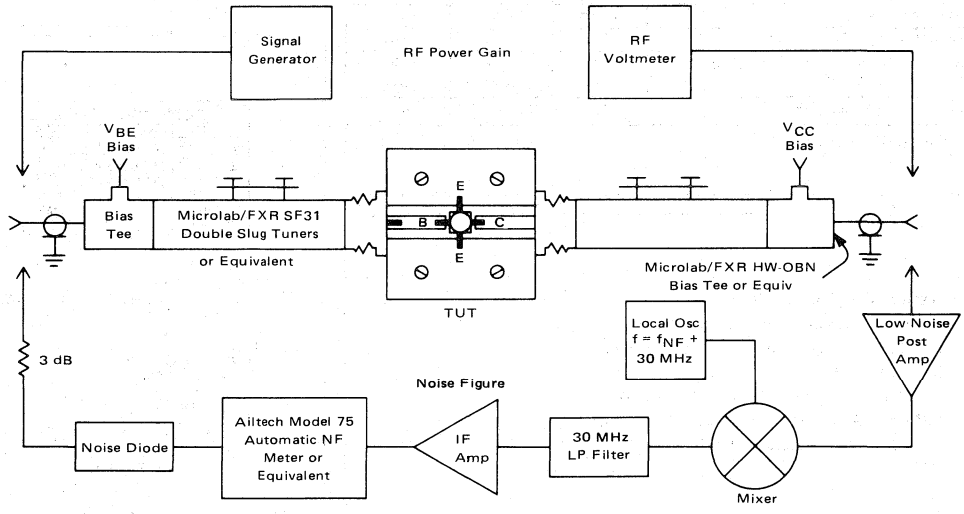


FIGURE 2 – POWER GAIN AND NOISE FIGURE versus FREQUENCY

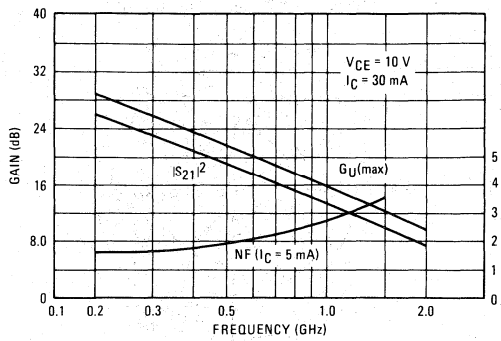


FIGURE 3 – OUTPUT CAPACITANCE versus VOLTAGE

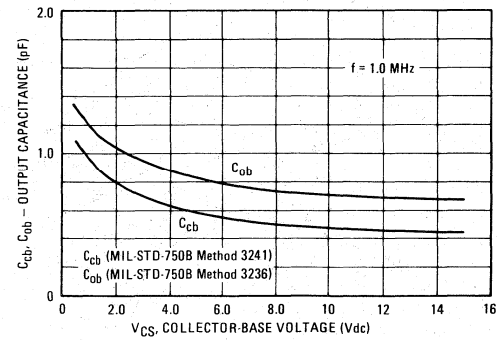


FIGURE 4 – CURRENT GAIN–BANDWIDTH PRODUCT versus COLLECTOR CURRENT

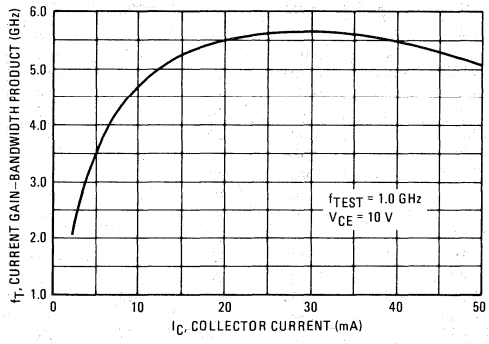


FIGURE 5 – POWER GAIN versus COLLECTOR CURRENT

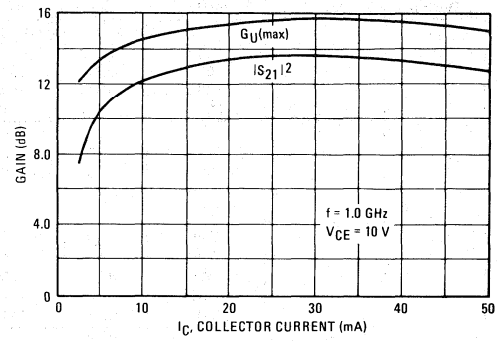
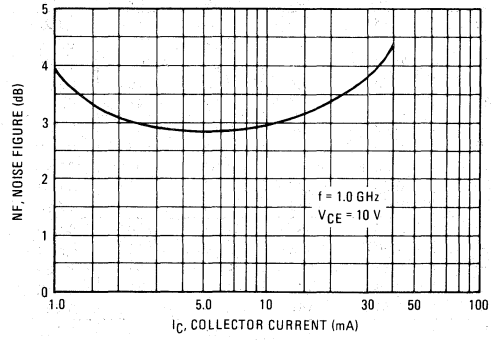


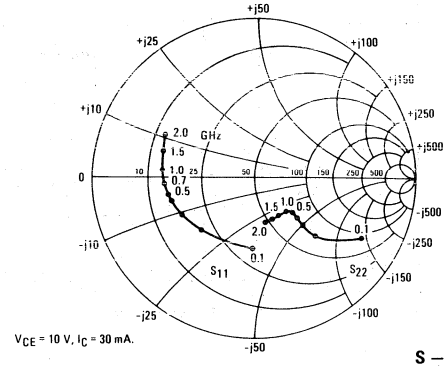
FIGURE 6 – NOISE FIGURE versus COLLECTOR CURRENT



3

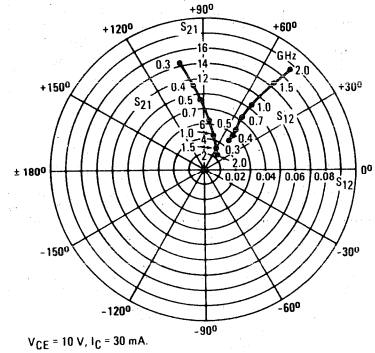
COMMON EMITTER SCATTERING PARAMETERS

FIGURE 7 – INPUT AND OUTPUT REFLECTION COEFFICIENTS versus FREQUENCY



V_{CE} = 10 V, I_C = 30 mA.

FIGURE 8 – FORWARD AND REVERSE TRANSMISSION COEFFICIENTS versus FREQUENCY



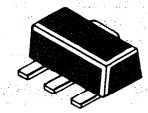
V_{CE} = 10 V, I_C = 30 mA.

S – PARAMETERS

V_{CE} (Volts)	I_C (mA)	Frequency (MHz)	S11		S21		S12		S22	
			|S11|	∠φ	|S21|	∠φ	|S12|	∠φ	|S22|	∠φ
5.0	5	100	0.72	−40	12.37	153	0.028	67	0.91	−18
		200	0.65	−78	10.38	133	0.048	51	0.76	−32
		500	0.61	−137	5.75	100	0.067	34	0.50	−45
		1000	0.61	−168	3.13	78	0.082	31	0.41	−54
		2000	0.63	161	1.58	47	0.112	30	0.41	−80
	10	100	0.57	−60	19.54	146	0.024	63	0.85	−27
		200	0.55	−105	14.70	125	0.038	47	0.64	−43
		500	0.59	−155	7.12	95	0.051	39	0.37	−55
		1000	0.61	−178	3.77	76	0.069	40	0.29	−62
		2000	0.64	156	1.91	50	0.106	39	0.30	−86
	30	100	0.43	−111	30.58	135	0.016	57	0.72	−39
		200	0.53	−145	19.35	114	0.022	49	0.46	−57
		500	0.62	−173	8.42	91	0.035	51	0.24	−69
		1000	0.63	172	4.36	75	0.058	54	0.18	−76
		2000	0.67	151	2.19	52	0.099	49	0.21	−99
	50	100	0.46	−134	32.34	129	0.013	57	0.64	−42
		200	0.57	−158	19.19	110	0.018	51	0.40	−56
		500	0.64	−178	8.13	89	0.031	57	0.22	−62
		1000	0.65	170	4.17	74	0.053	58	0.19	−70
		2000	0.70	150	2.10	52	0.092	54	0.22	−97
10	5	100	0.74	−36	12.34	154	0.023	69	0.93	−15
		200	0.67	−71	10.56	135	0.040	54	0.81	−25
		500	0.59	−131	6.09	102	0.058	37	0.57	−36
		1000	0.58	−164	3.32	79	0.073	33	0.50	−44
		2000	0.60	164	1.67	48	0.098	32	0.49	−69
	10	100	0.60	−52	19.75	148	0.020	65	0.87	−21
		200	0.56	−95	15.30	127	0.032	49	0.69	−33
		500	0.56	−149	7.69	97	0.044	41	0.45	−41
		1000	0.58	−174	4.07	77	0.061	42	0.39	−47
		2000	0.61	159	2.03	50	0.095	40	0.39	−70
	30	100	0.44	−94	32.03	136	0.014	59	0.75	−31
		200	0.50	−135	20.76	115	0.021	49	0.52	−41
		500	0.57	−168	9.13	91	0.032	52	0.33	−43
		1000	0.59	175	4.71	75	0.052	54	0.29	−48
		2000	0.64	154	2.34	52	0.089	49	0.30	−72
	50	100	0.44	−117	33.56	129	0.012	59	0.68	−31
		200	0.52	−150	19.94	109	0.017	50	0.47	−36
		500	0.59	−174	8.52	89	0.028	56	0.34	−35
		1000	0.61	173	4.38	75	0.049	57	0.32	−43
		2000	0.66	152	2.21	51	0.083	52	0.34	−70

BFQ17

RF TRANSISTOR
NPN SILICON



CASE 345-01, STYLE 1
SOT-89
(TO-243AA TYPE)

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	25	V
Collector-Emitter Voltage (RBE ≤ 50 Ω)	V_{CER}	40	V
Collector-Base Voltage	V_{CBO}	40	V
Emitter-Base Voltage	V_{EBO}	2.0	V
Collector Current — Continuous	I_C	300	mA
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Total Device Dissipation, T_A = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Storage Temperature	T_{stg}	150	°C
*Thermal Resistance Junction to Ambient	$R_{\theta JA}$	125	°C/W

*Package mounted on 99.5% alumina 10 x 12 x 0.6 mm.

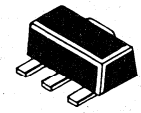
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 10 mA)	$V_{(BR)CEO}$	25	—	V
Collector-Base Breakdown Voltage (I_C = 10 μA)	$V_{(BR)CBO}$	40	—	V
Emitter-Base Breakdown Voltage (I_E = 10 μA)	$V_{(BR)EBO}$	2.0	—	V
Collector Cutoff Current (V_{CB} = 20 V) (V_{CB} = 20 V, T_A = 150°C)	I_{CBO}	 — —	 100 20	nA
Emitter Cutoff Current (V_{EB} = 1.0 V)	I_{EBO}	—	100	nA
ON CHARACTERISTICS				
DC Current Gain (I_C = 50 mA, V_{CE} = 5.0 V) (I_C = 150 mA, V_{CE} = 5.0 V)	h_{FE}	 25 25	 — —	—
Collector-Emitter Saturation Voltage (I_C = 100 mA, I_B = 10 mA)	$V_{CE(sat)}$	—	0.5	V
SMALL-SIGNAL CHARACTERISTICS				
Current-Gain — Bandwidth Product (V_{CE} = 15 V, I_C = 150 mA, f = 500 MHz)	f_T	1200(1)	—	MHz
Collector-Base Capacitance (V_{CB} = 15 V, f = 1.0 MHz)	C_{cb}	—	4.0	pF
Reverse Transfer Capacitance Common-Emitter (V_{CE} = 15 V, I_C = 10 mA, f = 1.0 MHz)	C_{re}	—	1.9	pF

(1) Typical only

BFQ19

RF TRANSISTOR
NPN SILICON



CASE 345-01, STYLE 1
SOT-89
(TO-243AA TYPE)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	V
Collector-Base Voltage	V_{CBO}	20	V
Emitter-Base Voltage	V_{EBO}	3.0	V
Collector Current Max (f > 1.0 MHz)	I_{CM}	150	mA
Collector Current — Average	I_{CAV}	75	mA
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Total Device Dissipation, T_A = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Storage Temperature	T_{stg}	150	°C
*Thermal Resistance Junction to Ambient	$R_{\theta JA}$	125	°C/W

*Package mounted on 99.5% alumina 10 x 12 x 0.6 mm.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 10 mA)	$V_{(BR)CEO}$	15	—	V
Collector-Base Breakdown Voltage (I_C = 10 μA)	$V_{(BR)CBO}$	20	—	V
Emitter-Base Breakdown Voltage (I_E = 10 μA)	$V_{(BR)EBO}$	3.0	—	V
Collector Cutoff Current (V_{CB} = 10 V)	I_{CBO}	—	100	nA
Emitter Cutoff Current (V_{EB} = 1.0 V)	I_{EBO}	—	100	nA
ON CHARACTERISTICS				
DC Current Gain (I_C = 50 mA, V_{CE} = 10 V) (I_C = 75 mA, V_{CE} = 10 V)	h_{FE}	 25 25	 — —	—
SMALL-SIGNAL CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 50 mA, V_{CE} = 10 V, f = 500 MHz) (I_C = 75 mA, V_{CE} = 10 V, f = 500 MHz)	f_T	 4.0 4.4	 — —	GHz
Collector-Base Capacitance (V_{CB} = 10 V, f = 1.0 MHz)	C_{cb}	—	1.6	pF
Capacitance Emitter-to-Base (V_{EB} = 0.5 V, f = 1.0 MHz)	C_{eb}	—	5.0	pF
Reverse Transfer Capacitance Common Emitter (V_{CE} = 10 V, I_C = 10 mA, f = 1.0 MHz)	C_{re}	—	1.3	pF
Noise Figure (I_C = 50 mA, V_{CE} = 10 V, f = 500 MHz)	NF	—	3.3	dB

BFR90

The RF Line

NPN SILICON HIGH FREQUENCY TRANSISTOR

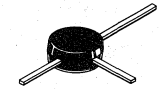
. . . designed primarily for use in high-gain, low-noise, small-signal amplifiers. Also used in applications requiring fast switching times.

- High Current-Gain – Bandwidth Product –
  f_T = 5.0 GHz (Typ) @ I_C = 14 mA
- Low Noise Figure –
  NF = 2.4 dB (Typ) @ f = 0.5 GHz
  = 3.0 dB (Typ) @ f = 1.0 GHz
- High Power Gain –
  G_{max} = 18 dB (Typ) @ f = 0.5 GHz
  = 12 dB (Typ) @ f = 1.0 GHz

f_T = 5.0 GHz @ 14 mA

HIGH FREQUENCY TRANSISTOR

NPN SILICON



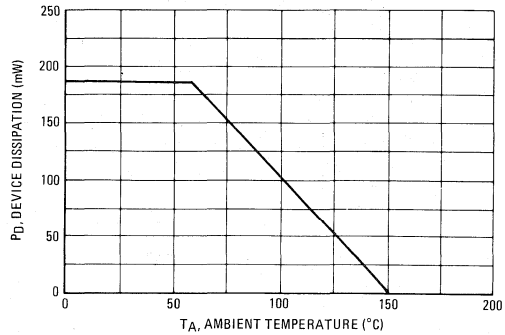
MAXIMUM RATINGS

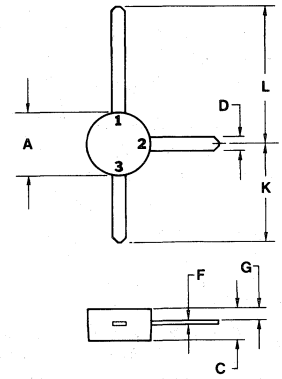
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CBO}	20	Vdc
Emitter-Base Voltage	V_{EBO}	3.0	Vdc
Collector Current – Continuous	I_C	30	mAdc
Total Device Dissipation @ T_A = 60°C	P_D	180	mW
Derate Above 60°C		2.0	mW/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	500	°C/W

FIGURE 1 – POWER DERATING





STYLE 2:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.44	5.21	0.175	0.205
C	1.90	2.54	0.075	0.100
D	0.94	0.99	0.033	0.039
F	0.20	0.30	0.008	0.012
G	0.76	1.14	0.030	0.045
K	7.24	8.13	0.285	0.320
L	10.54	11.43	0.415	0.450

CASE 317A-01

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	15	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	20	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}	–	–	50	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 14 mAdc, V_{CE} = 10 Vdc)	h_{FE}	25	–	250	–
DYNAMIC CHARACTERTISTICS					
Current-Gain Bandwidth Product (I_C = 14 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz)	f_T	–	5.0	–	GHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	–	0.5	1.0	pF
FUNCTIONAL TESTS					
Noise Figure	NF				dB
(I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz)		–	2.4	–	
(I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 GHz)		–	3.0	–	
Power Gain at Optimum Noise Figure	G_{NF}				dB
(I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz)		–	15	–	
(I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 GHz)		–	10	–	
Maximum Available Power Gain (1)	G_{max}				dB
(I_C = 14 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz)		–	18	–	
(I_C = 14 mAdc, V_{CE} = 10 Vdc, f = 1.0 GHz)		–	12	–	

(1) $G_{max} = \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)}$

FIGURE 2 – POWER GAIN AND NOISE FIGURE versus FREQUENCY

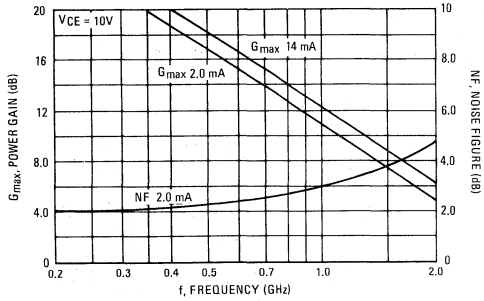


FIGURE 3 – POWER GAIN AND NOISE FIGURE versus COLLECTOR CURRENT

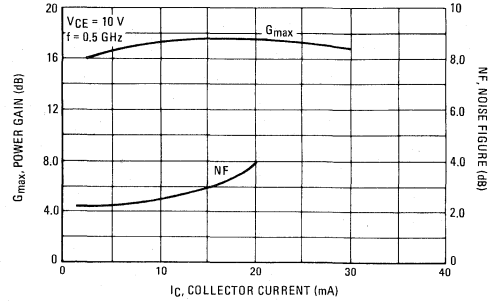


FIGURE 4 – S_{11} PARAMETERS

Frequency (MHz)		200		500		800		1000		1500	
V_{CE} (Volts)	I_C (mA)	S11	∠φ	S11	∠φ	S11	∠φ	S11	∠φ	S11	∠φ
5.0	2.0	0.77	-45	0.48	-90	0.33	-125	0.27	-160	0.28	170
	5.0	0.52	-60	0.25	-110	0.18	-150	0.18	170	0.21	145
	10	0.33	-75	0.15	-125	0.13	-175	0.15	150	0.20	130
	20	0.20	-95	0.12	-155	0.14	165	0.17	145	0.22	130
	30	0.17	-116	0.14	-170	0.17	160	0.21	145	0.26	130
10	2.0	0.79	-40	0.50	-80	0.33	-115	0.26	-150	0.25	175
	5.0	0.56	-55	0.27	-95	0.16	-135	0.13	-175	0.17	150
	10	0.39	-65	0.16	-105	0.10	-150	0.10	165	0.15	140
	20	0.25	-75	0.10	-120	0.09	-175	0.12	150	0.18	130
	30	0.25	-75	0.10	-120	0.09	-175	0.12	150	0.18	130

FIGURE 5 – S_{22} PARAMETERS

Frequency (MHz)		200		500		800		1000		1500	
V_{CE} (Volts)	I_C (mA)	S22	∠φ	S22	∠φ	S22	∠φ	S22	∠φ	S22	∠φ
5.0	2.0	0.89	-20	0.69	-30	0.61	-35	0.55	-35	0.52	-45
	5.0	0.75	-25	0.55	-30	0.50	-30	0.47	-30	0.43	-40
	10	0.64	-25	0.49	-25	0.45	-25	0.43	-30	0.40	-35
	20	0.57	-25	0.47	-20	0.44	-25	0.43	-25	0.40	-35
	30	0.55	-20	0.47	-20	0.46	-20	0.44	-25	0.42	-35
10	2.0	0.91	-15	0.74	-25	0.66	-30	0.62	-35	0.59	-40
	5.0	0.79	-20	0.61	-25	0.56	-25	0.54	-30	0.51	-35
	10	0.70	-20	0.56	-20	0.53	-25	0.51	-25	0.48	-35
	20	0.63	-20	0.54	-25	0.53	-20	0.51	-25	0.49	-35
	30	0.63	-15	0.56	-15	0.55	-20	0.54	-25	0.52	-35

FIGURE 6 – S_{21} PARAMETERS

Frequency (MHz)		200		500		800		1000		1500	
V_{CE} (Volts)	I_C (mA)	S21	∠φ	S21	∠φ	S21	∠φ	S21	∠φ	S21	∠φ
5.0	2.0	5.76	140	3.81	105	2.73	90	2.20	75	1.70	60
	5.0	9.92	125	5.24	95	3.50	80	2.80	70	2.10	60
	10	12.33	115	5.82	90	3.79	75	2.90	65	2.20	55
	20	13.62	105	6.00	85	3.88	75	2.95	65	2.25	55
	30	13.41	105	5.80	80	3.74	75	2.85	65	2.15	55
10	2.0	5.77	145	3.88	110	2.80	90	2.25	75	1.75	60
	5.0	10.05	130	5.42	95	3.60	80	2.85	70	2.10	60
	10	12.56	115	6.00	90	3.90	80	3.05	70	2.25	55
	20	13.77	110	6.13	85	3.92	75	3.05	65	2.20	55
	30	13.23	105	5.79	85	3.70	75	2.85	65	2.15	55

FIGURE 7 – S_{12} PARAMETERS

Frequency (MHz)		200		500		800		1000		1500	
V_{CE} (Volts)	I_C (mA)	S12	∠φ	S12	∠φ	S12	∠φ	S12	∠φ	S12	∠φ
5.0	2.0	0.06	65	0.10	55	0.12	55	0.14	55	0.17	60
	5.0	0.05	65	0.08	65	0.12	65	0.15	65	0.19	65
	10	0.04	65	0.08	70	0.12	70	0.15	70	0.20	65
	20	0.04	75	0.08	75	0.12	75	0.15	70	0.20	70
	30	0.03	75	0.07	75	0.11	75	0.15	75	0.19	70
10	2.0	0.05	70	0.03	55	0.11	55	0.12	55	0.15	60
	5.0	0.04	65	0.07	65	0.10	65	0.13	65	0.17	70
	10	0.04	65	0.07	70	0.10	70	0.13	70	0.17	70
	20	0.03	70	0.07	75	0.10	75	0.13	75	0.17	70
	30	0.03	75	0.06	75	0.10	75	0.13	75	0.17	70

BFR91

The RF Line

f_T = 5.0 GHz @ 30 mA

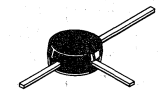
HIGH FREQUENCY TRANSISTOR

NPN SILICON

NPN SILICON HIGH FREQUENCY TRANSISTOR

. . . designed primarily for use in high-gain, low-noise, small-signal amplifiers. Also used in applications requiring fast switching times.

- High Current-Gain – Bandwidth Product –
  f_T = 5.0 GHz (Typ) @ I_C = 30 mA
- Low Noise Figure –
  NF = 1.9 dB (Typ) @ f = 0.5 GHz
- High Power Gain –
  G_{max} = 16 dB (Typ) @ f = 0.5 GHz



3

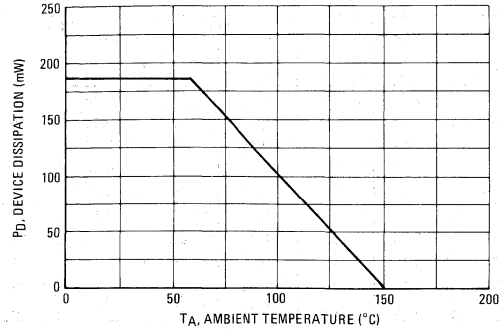
MAXIMUM RATINGS

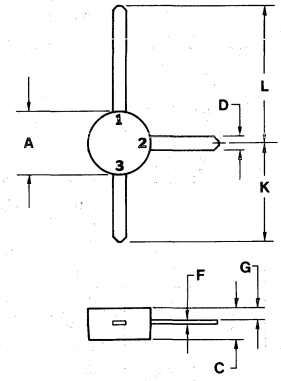
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	12	Vdc
Collector-Base Voltage	V_{CBO}	15	Vdc
Emitter-Base Voltage	V_{EBO}	3.0	Vdc
Collector Current – Continuous	I_C	35	mAdc
Total Device Dissipation @ T_A = 60°C	P_D	180	mW
Derate Above 60°C		2.0	mW/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	500	°C/W

FIGURE 1 – POWER DERATING





STYLE 2:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	4.44	5.21	0.175	0.205
C	1.90	2.54	0.075	0.100
D	0.94	0.99	0.033	0.039
F	0.20	0.30	0.008	0.012
G	0.76	1.14	0.030	0.045
K	7.24	8.13	0.285	0.320
L	10.54	11.43	0.415	0.450

CASE 317A-01

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	12	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	15	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 5.0 Vdc, I_E = 0)	I_{CBO}	–	–	50	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 30 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	25	–	250	–
DYNAMIC CHARACTERTISTICS					
Current-Gain Bandwidth Product (I_C = 30 mAdc, V_{CE} = 5.0 Vdc, f = 0.5 GHz)	f_T	–	5.0	–	GHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	–	0.7	1.0	pF
FUNCTIONAL TESTS					
Noise Figure	NF				dB
(I_C = 2.0 mAdc, V_{CE} = 5.0 Vdc, f = 0.5 GHz)		–	1.9	–	
(I_C = 2.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 GHz)		–	2.5	–	
Power Gain at Optimum Noise Figure	G_{NF}				dB
(I_C = 2.0 mAdc, V_{CE} = 5.0 Vdc, f = 0.5 GHz)		–	11	–	
(I_C = 2.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 GHz)		–	8.0	–	
Maximum Available Power Gain (1)	G_{max}				dB
(I_C = 30 mAdc, V_{CE} = 5.0 Vdc, f = 0.5 GHz)		–	16	–	
(I_C = 30 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 GHz)		–	10	–	

(1) $G_{max} = \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)}$

FIGURE 2 - POWER GAIN AND NOISE FIGURE versus FREQUENCY

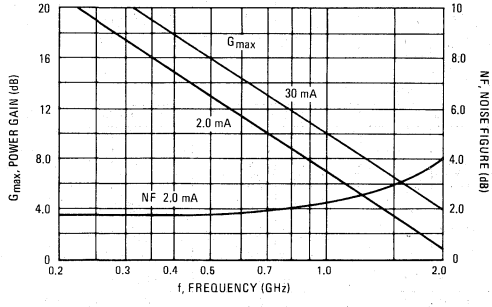


FIGURE 3 - POWER GAIN AND NOISE FIGURE versus COLLECTOR CURRENT

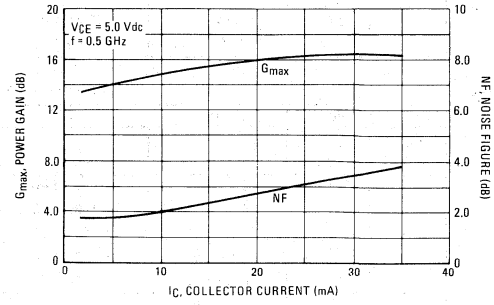


FIGURE 4 – S_{11} PARAMETERS

Frequency (MHz)		200		500		800		1000		1500	
V_{CE} (Volts)	I_C (mA)	S11	∠φ	S11	∠φ	S11	∠φ	S11	∠φ	S11	∠φ
5.0	2.0	0.72	-65	0.51	-125	0.46	-165	0.47	170	0.51	145
	5.0	0.49	-90	0.35	-150	0.34	175	0.36	155	0.41	135
	10	0.34	-110	0.28	-165	0.29	165	0.32	145	0.36	130
	20	0.26	-130	0.24	180	0.27	155	0.30	140	0.34	125
	30	0.24	-145	0.24	175	0.27	155	0.30	140	0.34	125
10	2.0	0.74	-60	0.51	-120	0.45	-160	0.45	170	0.49	150
	5.0	0.52	-80	0.33	-140	0.31	-175	0.32	160	0.37	145
	10	0.36	-95	0.24	-155	0.24	170	0.27	155	0.31	140
	20	0.25	-115	0.19	-170	0.21	160	0.24	145	0.29	130
	30	0.22	-120	0.19	-175	0.21	160	0.25	145	0.20	130

FIGURE 5 – S_{22} PARAMETERS

Frequency (MHz)		200		500		800		1000		1500	
V_{CE} (Volts)	I_C (mA)	S22	∠φ	S22	∠φ	S22	∠φ	S22	∠φ	S22	∠φ
5.0	2.0	0.83	-25	0.62	-35	0.55	-40	0.51	-45	0.49	-60
	5.0	0.66	-30	0.45	-35	0.40	-40	0.37	-40	0.34	-50
	10	0.52	-35	0.36	-35	0.32	-35	0.30	-35	0.27	-50
	20	0.42	-35	0.30	-30	0.27	-30	0.26	-30	0.22	-45
	30	0.38	-35	0.28	-25	0.26	-30	0.25	-30	0.21	-40
10	2.0	0.86	-20	0.67	-30	0.62	-35	0.58	-40	0.56	-50
	5.0	0.71	-25	0.53	-30	0.48	-30	0.45	-35	0.43	-45
	10	0.59	-30	0.45	-25	0.41	-30	0.40	-30	0.37	-40
	20	0.50	-25	0.40	-25	0.38	-25	0.37	-30	0.34	-40
	30	0.47	-25	0.40	-20	0.38	-25	0.37	-30	0.34	-35

FIGURE 6 – S_{21} PARAMETERS

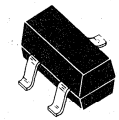
Frequency (MHz)		200		500		800		1000		1500	
V_{CE} (Volts)	I_C (mA)	S21	∠φ	S21	∠φ	S21	∠φ	S21	∠φ	S21	∠φ
5.0	2.0	5.25	130	3.06	95	2.10	75	1.70	65	1.20	50
	5.0	8.72	120	4.34	90	2.84	75	2.30	65	1.60	50
	10	10.85	110	4.92	85	3.22	70	2.60	65	1.80	50
	20	12.13	105	5.34	80	3.44	70	2.75	60	1.90	50
	30	12.50	100	5.42	80	3.47		2.75	60	1.90	50
10	2.0	5.36	135	3.20	95	2.20	80	1.85	65	1.30	50
	5.0	9.05	120	4.55	90	3.00	75	2.45	65	1.65	50
	10	11.37	110	5.22	85	3.40	75	2.65	65	1.85	50
	20	12.83	105	5.64	80	3.63	70	2.75	60	2.00	50
	30	13.10	100	5.62	80	3.63	70	2.75	60	2.00	50

FIGURE 7 – S_{12} PARAMETERS

Frequency (MHz)		200		500		800		1000		1500	
V_{CE} (Volts)	I_C (mA)	S12	∠φ	S12	∠φ	S12	∠φ	S12	∠φ	S12	∠φ
5.0	2.0	0.08	55	0.11	45	0.12	50	0.14	55	0.17	65
	5.0	0.06	55	0.09	60	0.13	65	0.17	65	0.22	65
	10	0.05	60	0.09	65	0.14	70	0.19	65	0.24	65
	20	0.05	70	0.07	70	0.15	70	0.19	70	0.25	65
	30	0.04	75	0.10	75	0.15	70	0.19	70	0.25	65
10	2.0	0.06	60	0.09	45	0.10	50	0.12	60	0.15	70
	5.0	0.05	60	0.08	60	0.11	65	0.15	65	0.19	70
	10	0.05	65	0.08	65	0.12	70	0.16	70	0.21	70
	20	0.04	70	0.08	70	0.13	70	0.17	70	0.22	70
	30	0.04	70	0.08	75	0.13	70	0.17	70	0.22	70

BFR92,A

RF TRANSISTOR
NPN SILICON



CASE 318-02/03, STYLE 6
SOT-23
(TO-236AA/AB)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CBO}	20	Vdc
Emitter-Base Voltage	V_{EBO}	2.0	Vdc
Collector Current — Continuous	I_C	25	mAdc
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Total Device Dissipation, T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Storage Temperature	T_{stg}	150	°C
*Thermal Resistance Junction to Ambient	$R_{\theta JA}$	357	°C/W

*Package mounted on 99.5% alumina 10 x 8 x 0.6 mm.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 10 mA)		$V_{(BR)CEO}$	15	—	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μA)		$V_{(BR)CBO}$	20	—	Vdc
Emitter-Base Breakdown Voltage (I_C = 100 μA)		$V_{(BR)EBO}$	2.0	—	Vdc
Collector Cutoff Current (V_{CB} = 10 V)	BFR92 BFR92A	I_{CBO}	— —	50 60	nA
ON CHARACTERISTICS					
DC Current Gain (I_C = 500 μA, V_{CE} = 10 V) (I_C = 14 mA, V_{CE} = 10 V)	 BFR92 BFR92A	h_{FE}	 25 40	 — —	—
Collector-Emitter Saturation Voltage (1) (I_C = 25 mA, I_B = 5.0 mA)		$V_{CE(sat)}$	—	0.5	Vdc
Base-Emitter Saturation Voltage (1) (I_C = 25 mA, I_B = 5.0 mA)		$V_{BE(sat)}$	—	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 14 mA, V_{CE} = 10 V, f = 500 MHz)		f_T	3.0	—	GHz
Noise Figure (V_{CE} = 1.5 V, I_C = 3.0 mA, R_S = 50 Ω, f = 500 MHz)		NF	—	3.0 (Typ)	dB
Capacitance-Collector to Base (V_{CB} = 10 Vdc, f = 1.0 MHz)		C_{cb}	—	0.7 (Typ)	pF

(1) Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

BFR93,A

RF TRANSISTOR
NPN SILICON



CASE 318-02/03, STYLE 6
SOT-23
(TO-236AA/AB)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	12	Vdc
Collector-Base Voltage	V_{CBO}	15	Vdc
Emitter-Base Voltage	V_{EBO}	2.0	Vdc
Collector Current — Continuous	I_C	35	mAdc
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Total Device Dissipation, T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Storage Temperature	T_{stg}	150	°C
*Thermal Resistance Junction to Ambient	$R_{\theta JA}$	357	°C/W

*Package mounted on 99.5% alumina 10 x 8 x 0.6 mm.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 10 mA)		$V_{(BR)CEO}$	12	—	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μA)		$V_{(BR)CBO}$	15	—	Vdc
Emitter-Base Breakdown Voltage (I_C = 100 μA)		$V_{(BR)EBO}$	2.0	—	Vdc
Collector Cutoff Current (V_{CE} = 10 V)		I_{CEO}	—	50	nA
Collector Cutoff Current (V_{CB} = 10 V)		I_{CBO}	—	50	nA
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 30 mA, V_{CE} = 5.0 V) (I_C = 30 mA, V_{CE} = 5.0 V)	 BFR93A BFR93	h_{FE}	 40 25	 — —	—
Collector-Emitter Saturation Voltage (1) (I_C = 35 mA, I_B = 7.0 mA)		$V_{CE(sat)}$	—	0.5	Vdc
Base-Emitter Saturation Voltage (1) (I_C = 35 mA, I_B = 7.0 mA)		$V_{BE(sat)}$	—	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 30 mA, V_{CE} = 5.0 V, f = 500 MHz)		f_T	3.0	—	GHz
Noise Figure (V_{CE} = 5.0 V, I_C = 2.0 mA, R_S = 50 Ω, f = 30 MHz)		NF	—	3.0	dB

(1) Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

BFR96
BFRC96
MRF961
MRF962
MRF965

The RF Line

NPN SILICON HIGH FREQUENCY TRANSISTORS

The BFR96 series transistors use the same state-of-the-art microwave transistor chip which features fine-line geometry, ion-implanted arsenic emitters and gold top metalization. These transistors are intended for low-to-medium power amplifiers requiring high gain, low noise figure, and low intermodulation distortion. The BFR96 and MRF961 are particularly suitable for broadband MATV/CATV amplifiers. The MRF962 uses a hermetic stripline, ceramic package and is intended for high reliability applications up to 2 GHz. The MRF965 makes an excellent VHF/UHF Class C driver amplifier for several hundred milliwatts power output.

f_T = 4.5 GHz @ 50 mA

HIGH FREQUENCY TRANSISTOR

NPN SILICON

3

MAXIMUM RATINGS		BFRC96 Chip	BFR96 Case 317A-01	MRF961 Case 317-01	MRF962 Case 303-01	MRF965 Case 26-03	
Ratings	**Symbol**	**Values**					**Unit**
Collector-Emitter Voltage	V_{CEO}	15	15	15	15	15	Vdc
Collector-Base Voltage	V_{CBO}	20	20	20	20	20	Vdc
Emitter-Base Voltage	V_{EBO}	3.0	3.0	3.0	3.0	3.0	Vdc
Collector Current — Continuous	I_C	100	100	100	100	100	mAdc
Total Device Dissipation @ T_C = 100°C(1)	P_D	0.75	0.5	0.5	0.75	0.75	Watts
Derate above T_C = 100°C		T_J = 200°C max	10	10	7.5	7.5	mW/°C
Storage Temperature	T_{stg}	−65 to +200	−65 to +150	−65 to +150	−65 to +200	−65 to +200	°C

NOTE 1. Case temperature measured on collector lead immediately adjacent to body of package.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	15	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	$V_{(BR)CBO}$	20	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	$V_{(BR)EBO}$	3.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}	–	–	100	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	–	200	–
DYNAMIC CHARACTERISTICS					
Current-Gain Bandwidth Product (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz)	f_T	–	4.5	–	GHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, Emitter Guarded) BFR96, MRF961, MRF962	C_{cb}	–	1.2	1.5	pF
MRF965		–	1.6	2.0	
FUNCTIONAL TESTS					
Noise Figure (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz)	NF	–	2.0	–	dB
Maximum Unilateral Gain/Insertion Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz) BFR96, MRF965	$G_U(max)$/ $\lvert S_{21}\rvert^2$	–/12	14.5/13	–	dB
MRF961		–/13.5	17/15	–	
MRF962		–/15	20.5/16.5	–	

NOTE 1. $G_U(max) = \dfrac{\lvert S_{21}\rvert^2}{(1 - \lvert S_{11}\rvert^2)(1 - \lvert S_{22}\rvert^2)}$

FIGURE 1 – MAXIMUM UNILATERAL GAIN versus FREQUENCY

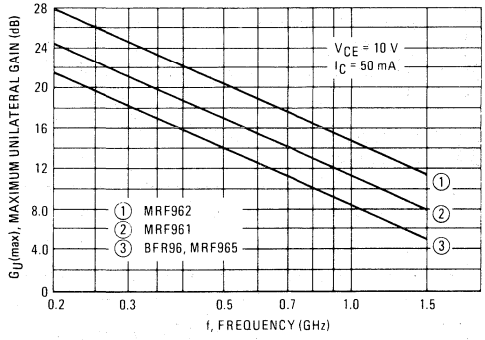


FIGURE 2 – $|S_{21}|^2$ versus FREQUENCY

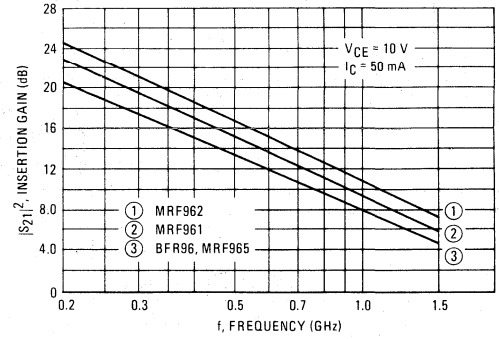


FIGURE 3 – MAXIMUM UNILATERAL GAIN versus COLLECTOR CURRENT

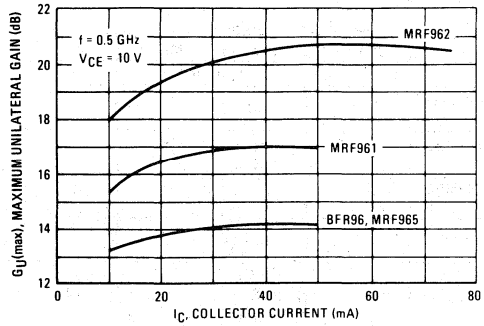


FIGURE 4 – GAIN-BANDWIDTH PRODUCT versus COLLECTOR CURRENT

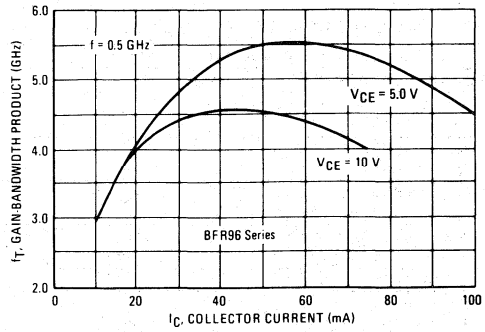


FIGURE 5 – NOISE FIGURE versus FREQUENCY

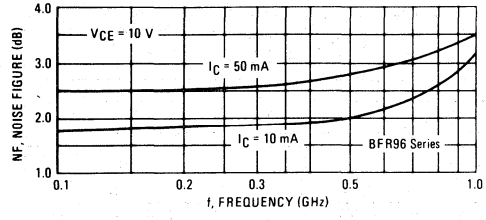


FIGURE 6 – NOISE FIGURE versus COLLECTOR CURRENT

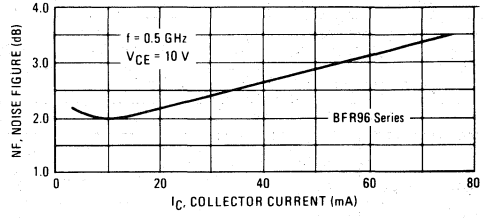


FIGURE 7 – COLLECTOR-BASE CAPACITANCE versus COLLECTOR-BASE VOLTAGE

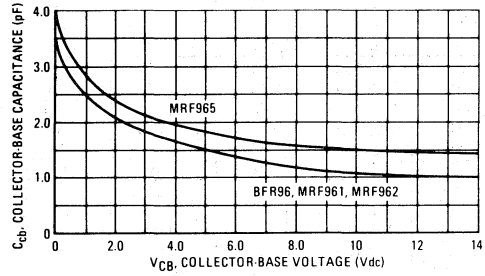


FIGURE 8 – OUTPUT POWER AND EFFICIENCY versus INPUT POWER (MRF965)

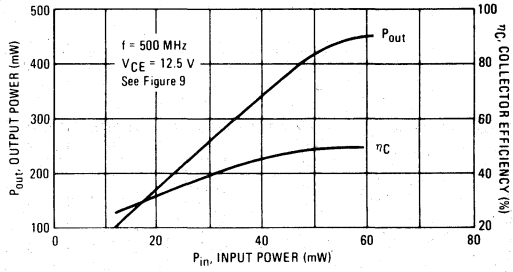
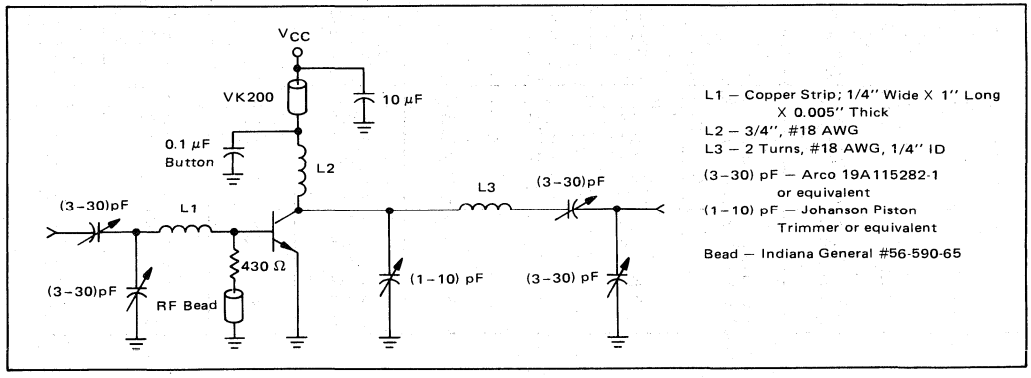
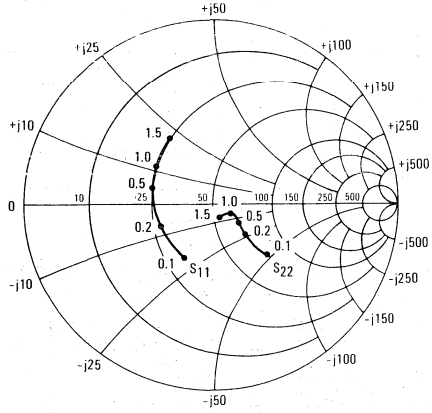


FIGURE 9 – MRF965 CLASS C AMPLIFIER @ 500 MHz, 400 mW

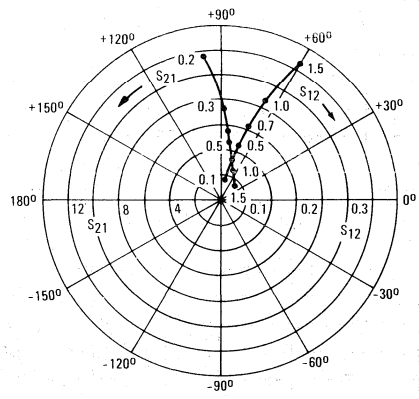


BFR96 COMMON-EMITTER S-PARAMETERS

INPUT/OUTPUT REFLECTION COEFFICIENTS versus FREQUENCY (V_{CE} = 10 V, I_C = 50 mA)



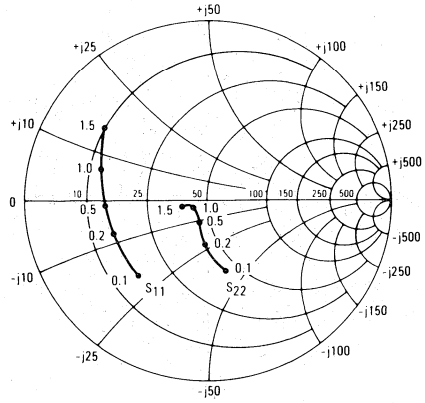
FORWARD/REVERSE TRANSMISSION COEFFICIENTS versus FREQUENCY (V_{CE} = 10 V, I_C = 50 mA)



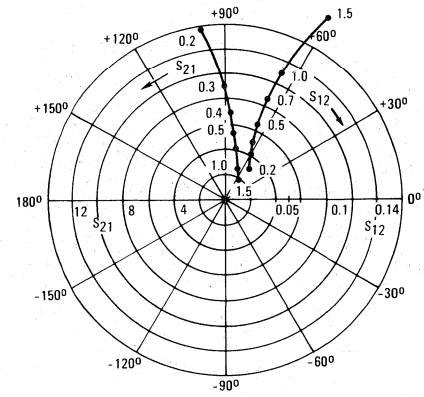
V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
5.0	10	100	0.51	-95	15.04	121	0.047	54	0.58	-48
		300	0.43	163	5.87	92	0.082	58	0.26	-63
		500	0.46	174	3.61	79	0.120	63	0.19	-63
		700	0.48	162	2.65	68	0.161	63	0.15	-64
		1000	0.48	146	1.92	57	0.220	63	0.12	-79
		1500	0.54	121	1.40	43	0.320	58	0.13	-118
	25	100	0.39	-122	19.41	112	0.037	60	0.42	-68
		300	0.39	-176	6.81	89	0.079	68	0.16	-94
		500	0.42	166	4.11	78	0.129	70	0.10	-103
		700	0.44	156	3.05	69	0.176	68	0.06	-119
		1000	0.44	142	2.20	59	0.244	64	0.06	-159
		1500	0.49	118	1.62	45	0.348	57	0.10	177
	50	100	0.35	-140	21.10	106	0.032	64	0.33	-81
		300	0.38	176	7.11	88	0.081	72	0.13	-116
		500	0.42	162	4.28	78	0.133	72	0.09	-136
		700	0.43	153	3.16	70	0.183	69	0.07	-163
		1000	0.42	140	2.28	60	0.252	65	0.08	165
		1500	0.47	116	1.66	47	0.357	57	0.12	155
10	10	100	0.53	-83	15.96	124	0.039	58	0.65	-36
		300	0.38	-154	6.44	94	0.070	59	0.35	-41
		500	0.41	-179	3.98	81	0.102	64	0.30	-39
		700	0.42	166	2.94	70	0.138	65	0.27	-39
		1000	0.42	151	2.12	60	0.191	66	0.24	-47
		1500	0.49	125	1.50	44	0.278	63	0.22	-72
	25	100	0.38	-104	20.85	115	0.032	60	0.48	-48
		300	0.32	-169	7.54	91	0.070	68	0.23	-48
		500	0.35	170	4.61	80	0.109	71	0.19	-43
		700	0.37	160	3.37	70	0.152	69	0.16	-39
		1000	0.37	146	2.43	61	0.210	67	0.13	-44
		1500	0.43	121	1.73	47	0.304	61	0.10	-74
	50	100	0.33	-119	22.69	109	0.029	63	0.39	-51
		300	0.30	-176	7.74	88	0.069	72	0.19	-47
		500	0.34	166	4.70	79	0.113	73	0.16	-40
		700	0.36	158	3.45	70	0.156	70	0.14	-35
		1000	0.36	144	2.46	61	0.217	66	0.11	-39
		1500	0.42	119	1.75	47	0.310	60	0.08	-72

MRF961 COMMON-EMITTER S-PARAMETERS

INPUT/OUTPUT REFLECTION COEFFICIENTS versus FREQUENCY (V_{CE} = 10 V, I_C = 50 mA)



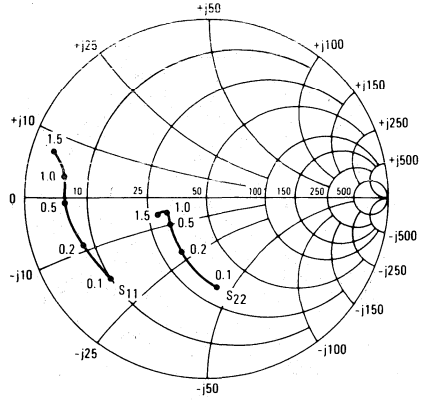
FORWARD/REVERSE TRANSMISSION COEFFICIENTS versus FREQUENCY (V_{CE} = 10 V, I_C = 50 mA)



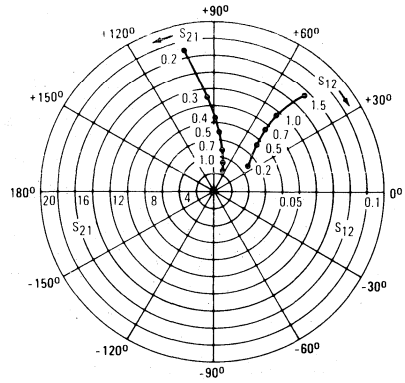
V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
5.0	10	100	0.65	-101	16.61	125	0.047	46	0.61	-56
		300	0.64	-160	6.61	96	0.064	39	0.27	-87
		500	0.66	-178	4.01	83	0.078	45	0.19	-98
		700	0.68	171	2.93	73	0.093	49	0.16	-108
		1000	0.68	160	2.07	63	0.119	53	0.16	-124
		1500	0.72	143	1.43	50	0.158	54	0.21	-141
	25	100	0.60	-129	22.41	115	0.034	44	0.49	-84
		300	0.63	-172	7.94	93	0.049	50	0.26	-132
		500	0.66	174	4.78	83	0.071	58	0.21	-150
		700	0.67	166	3.45	75	0.092	60	0.20	-164
		1000	0.67	156	2.46	66	0.124	61	0.21	-177
		1500	0.71	140	1.73	54	0.173	60	0.24	175
	50	100	0.59	-147	25.12	109	0.025	46	0.42	-104
		300	0.64	-178	8.47	91	0.046	60	0.28	-151
		500	0.67	171	5.05	83	0.070	65	0.26	-167
		700	0.68	164	3.67	75	0.093	65	0.25	-178
		1000	0.67	154	2.60	67	0.128	65	0.26	170
		1500	0.72	138	1.83	56	0.178	62	0.29	163
10	10	100	0.65	-90	17.47	128	0.040	50	0.67	-41
		300	0.61	-154	7.31	97	0.057	41	0.33	-57
		500	0.62	-174	4.46	84	0.069	46	0.25	-58
		700	0.64	175	3.27	74	0.084	50	0.22	-60
		1000	0.64	163	2.33	64	0.106	54	0.20	-72
		1500	0.69	145	1.56	50	0.140	57	0.22	-96
	25	100	0.57	-116	24.36	119	0.030	48	0.51	-62
		300	0.58	-167	8.10	94	0.045	52	0.20	-89
		500	0.61	178	5.43	83	0.070	58	0.14	-97
		700	0.63	169	3.93	75	0.084	60	0.10	-106
		1000	0.62	159	2.78	66	0.112	61	0.09	-124
		1500	0.67	142	1.91	53	0.156	60	0.12	-140
	50	100	0.55	-132	26.97	112	0.024	47	0.40	-73
		300	0.57	-173	9.32	91	0.042	59	0.16	-104
		500	0.60	174	5.58	82	0.064	64	0.11	-115
		700	0.62	167	4.04	74	0.086	64	0.08	-128
		1000	0.61	158	2.85	66	0.115	64	0.08	-149
		1500	0.67	141	1.96	55	0.158	61	0.12	-158

MRF962 COMMON-EMITTER S-PARAMETERS

INPUT/OUTPUT REFLECTION COEFFICIENTS versus FREQUENCY (V_{CE} = 10 V, I_C = 50 mA)



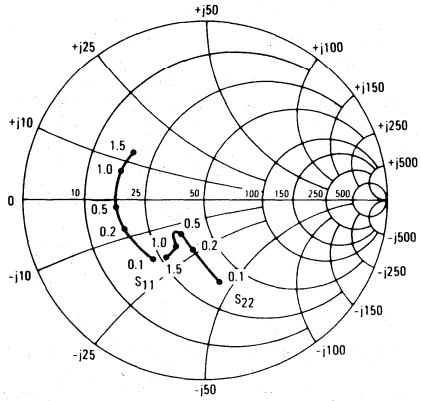
FORWARD/REVERSE TRANSMISSION COEFFICIENTS versus FREQUENCY (V_{CE} = 10 V, I_C = 50 mA)



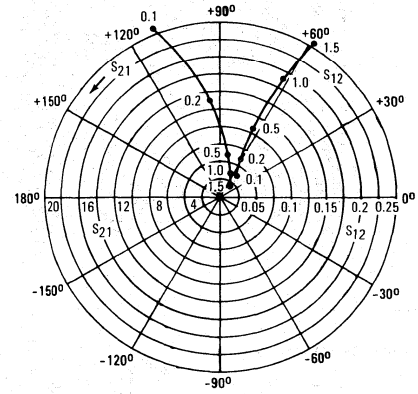
V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
5.0	10	100	0.70	−102	17.42	128	0.044	43	0.65	−57
		300	0.75	−156	7.11	98	0.058	24	0.32	−97
		500	0.78	−170	4.36	86	0.064	25	0.26	−110
		700	0.78	−176	3.16	77	0.071	26	0.23	−117
		1000	0.78	176	2.26	67	0.078	27	0.24	−126
		1500	0.79	167	1.51	54	0.092	29	0.31	−133
	25	100	0.69	−131	24.24	118	0.029	38	0.56	−87
		300	0.77	−167	8.76	95	0.039	32	0.35	−137
		500	0.79	−176	5.26	85	0.046	36	0.32	−150
		700	0.80	178	3.82	78	0.055	40	0.31	−158
		1000	0.79	173	2.72	70	0.067	42	0.32	−164
		1500	0.81	164	1.82	59	0.086	42	0.34	−167
	50	100	0.71	−147	27.72	113	0.021	37	0.53	−107
		300	0.78	−173	9.59	94	0.030	40	0.41	−152
		500	0.81	179	5.72	85	0.038	46	0.39	−163
		700	0.81	176	4.09	78	0.048	50	0.38	−169
		1000	0.81	171	2.89	71	0.061	51	0.38	−175
		1500	0.82	163	1.96	62	0.082	49	0.40	−177
10	10	100	0.71	−92	18.77	131	0.037	47	0.70	−44
		300	0.74	−150	8.09	100	0.051	28	0.34	−69
		500	0.75	−166	5.01	87	0.056	28	0.27	−75
		700	0.76	−174	3.62	78	0.064	28	0.24	−79
		1000	0.76	179	2.58	69	0.071	30	0.24	−88
		1500	0.77	168	1.72	55	0.085	31	0.31	−104
	25	100	0.67	−120	27.10	122	0.027	42	0.57	−68
		300	0.73	−163	10.27	97	0.035	36	0.27	−110
		500	0.76	−174	6.21	86	0.043	39	0.22	−124
		700	0.77	−179	4.48	78	0.051	41	0.20	−132
		1000	0.77	175	3.19	71	0.062	43	0.20	−139
		1500	0.78	166	2.13	59	0.080	42	0.25	−142
	50	100	0.68	−137	31.53	116	0.020	37	0.49	−85
		300	0.74	−169	11.17	95	0.028	40	0.27	−131
		500	0.77	−177	6.69	85	0.037	46	0.24	−144
		700	0.77	178	4.82	78	0.047	48	0.23	−152
		1000	0.77	173	3.42	71	0.059	50	0.23	−158
		1500	0.79	165	2.30	61	0.078	47	0.27	−159

MRF965 COMMON-EMITTER S-PARAMETERS

INPUT/OUTPUT REFLECTION COEFFICIENTS versus FREQUENCY (V_{CE} = 10 V, I_C = 50 mA)

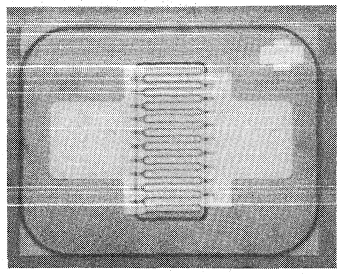


FORWARD/REVERSE TRANSMISSION COEFFICIENTS versus FREQUENCY (V_{CE} = 10 V, I_C = 50 mA)



V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
5.0	10	100	0.56	-102	13.87	121	0.054	48	0.58	-62
		300	0.57	-158	5.47	90	0.084	46	0.32	-94
		500	0.56	-169	3.40	77	0.110	52	0.27	-106
		700	0.52	178	2.53	69	0.136	54	0.39	-115
		1000	0.55	167	1.79	57	0.181	56	0.35	-112
		1500	0.54	150	1.27	42	0.242	57	0.43	-122
	25	100	0.48	-129	17.61	112	0.041	51	0.47	-85
		300	0.55	-169	6.38	89	0.076	57	0.30	-125
		500	0.54	-176	3.97	77	0.111	62	0.27	-138
		700	0.50	172	2.94	71	0.114	61	0.30	-143
		1000	0.53	162	2.08	61	0.198	60	0.32	-135
		1500	0.50	146	1.50	47	0.267	57	0.37	-140
	50	100	0.47	-144	19.34	107	0.035	56	0.42	-100
		300	0.55	-173	6.72	87	0.073	63	0.31	-138
		500	0.53	-179	4.17	77	0.112	66	0.29	-150
		700	0.50	168	3.10	71	0.147	64	0.33	-153
		1000	0.53	159	2.19	62	0.206	61	0.32	-146
		1500	0.50	143	1.59	49	0.277	58	0.36	-149
10	10	100	0.56	-92	14.67	123	0.047	50	0.63	-50
		300	0.53	-152	6.00	92	0.077	47	0.34	-73
		500	0.53	-165	3.74	78	0.100	53	0.29	-82
		700	0.49	-177	2.76	70	0.124	56	0.31	-93
		1000	0.52	170	1.96	57	0.166	58	0.38	-94
		1500	0.51	153	1.36	42	0.221	59	0.46	-108
	25	100	0.46	-117	19.10	115	0.036	53	0.49	-68
		300	0.50	-164	7.09	90	0.071	57	0.26	-99
		500	0.49	-172	4.39	78	0.102	62	0.23	-110
		700	0.45	175	3.25	71	0.133	61	0.25	-119
		1000	0.49	164	2.28	60	0.181	61	0.30	-112
		1500	0.47	148	1.61	46	0.246	59	0.37	-120
	50	100	0.42	-131	20.99	110	0.033	56	0.41	-79
		300	0.49	-169	7.46	88	0.069	62	0.24	-111
		500	0.48	-175	4.63	78	0.103	65	0.21	-123
		700	0.45	172	3.40	71	0.136	64	0.25	-129
		1000	0.48	162	2.39	61	0.188	62	0.29	-119
		1500	0.45	146	1.70	48	0.251	59	0.35	-126

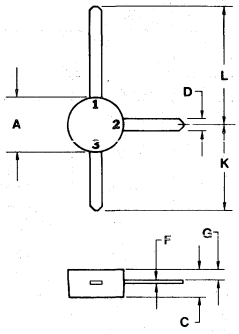
BFRC96 CHIP TOPOGRAPHY



Nominal Chip Size: 0.014" X 0.016" X 0.005"
Front Metalization: Gold
Back Metalization: Gold
Emitter/Base Bond Pad: 2.8 mil Dia.
#Emitter Fingers: 10
#Base Fingers: 11
Emitter Diffusion: Ion-Implanted Arsenic

3-LEAD PLASTIC MACRO-T

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.44	5.21	0.175	0.205
C	1.90	2.54	0.075	0.100
D	0.94	0.99	0.033	0.039
F	0.20	0.30	0.008	0.012
G	0.76	1.14	0.030	0.045
K	7.24	8.13	0.285	0.320
L	10.54	11.43	0.415	0.450

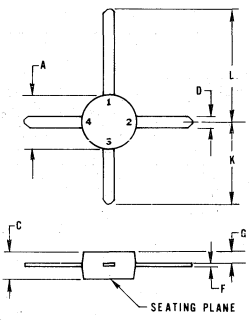


STYLE 2:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

CASE 317A-01

4 LEAD PLASTIC MACRO-T

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.44	5.21	0.175	0.205
C	1.90	2.54	0.075	0.100
D	0.84	0.99	0.033	0.039
F	0.20	0.30	0.008	0.012
G	0.76	1.14	0.030	0.045
K	7.24	8.13	0.285	0.320
L	10.54	11.43	0.415	0.450

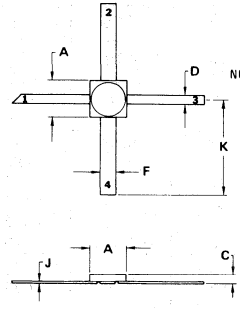


STYLE 2:
PIN 1. COLLECTOR
2. EMITTER
3. BASE
4. EMITTER

CASE 317-01

0.100" CERAMIC STRIPLINE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.29	2.67	0.090	0.105
C	0.89	1.40	0.035	0.055
D	0.41	0.61	0.016	0.024
F	0.89	1.09	0.035	0.043
J	0.08	0.15	0.003	0.006
K	4.45	5.84	0.175	0.230



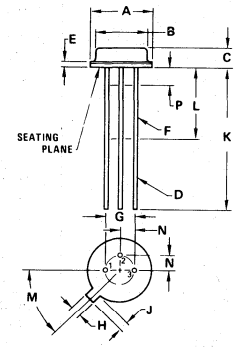
NOTE:
1. DIMENSION K APPLIES TO ALL LEADS.

PIN 1. COLLECTOR
2. EMITTER
3. BASE
4. EMITTER

CASE 303-01

TO-46

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	1.65	2.16	0.065	0.085
D	0.406	0.533	0.016	0.021
E	–	1.02	–	0.040
F	0.305	0.483	0.012	0.019
G	2.54 BSC		0.100 BSC	
H	0.914	1.17	0.036	0.046
J	0.711	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050



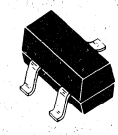
All JEDEC dimensions and notes apply

PIN 1. EMITTER
2. BASE
3. COLLECTOR

CASE 26-03

BFS17

RF TRANSISTOR
NPN SILICON



CASE 318-02/03, STYLE 6
SOT-23
(TO-236AA/AB)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CBO}	25	Vdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Total Device Dissipation, T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Storage Temperature	T_{stg}	150	°C
*Thermal Resistance Junction to Ambient	$R_{\theta JA}$	357	°C/W

*Package mounted on 99.5% alumina 10 x 8 x 0.6 mm.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 10 mA)	$V_{(BR)CEO}$	15	—	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μA)	$V_{(BR)CBO}$	25	—	Vdc
Collector Cutoff Current (V_{CE} = 10 V)	I_{CEO}	—	25	nA
Collector Cutoff Current (V_{CB} = 10 V)	I_{CBO}	—	25	nA
Emitter Cutoff Current (V_{EB} = 4.0 V)	I_{EBO}	—	100	μA
ON CHARACTERISTICS				
DC Current Gain (I_C = 2.0 mA, V_{CE} = 1.0 V) (I_C = 25 mA, V_{CE} = 1.0 V)	h_{FE}	 20 20	 150 —	—
Collector-Emitter Saturation Voltage (I_C = 10 mA, I_B = 1.0 mA)	$V_{CE(sat)}$	—	0.4	V
Base-Emitter Saturation Voltage (I_C = 10 mA, I_B = 1.0 mA)	$V_{BE(sat)}$	—	1.0	V
SMALL-SIGNAL CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 2.0 mA, V_{CE} = 5.0 V, f = 500 MHz) (I_C = 25 mA, V_{CE} = 5.0 V, f = 500 MHz)	f_T	 1.0 1.3*	 — —	GHz
Output Capacitance (V_{CB} = 10 V, f = 1.0 MHz)	CCB	—	1.0*	pF
Noise Figure (I_C = 2.0 mA, V_{CE} = 5.0 V, R_S = 50 Ω, f = 30 MHz)	NF	—	5.0*	dB

*Typ

BFW92A

The RF Line

f_T = 4.5 GHz @ 10 mA

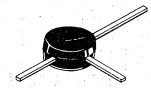
HIGH FREQUENCY TRANSISTOR

NPN SILICON

NPN SILICON HIGH FREQUENCY TRANSISTORS

. . . designed primarily for use in MATV/CATV amplifiers and other broadband linear applications demanding high power gain with low noise over a wide current range.

- High Power Gain — MAG = 16 dB (Typ) @ f = 0.5 GHz
- Low Noise Figure — NF = 2.7 dB (Typ) @ f = 0.5 GHz
- Ion-Implanted Arsenic Emitters
- Gold Top Metal
- Silicon Nitride Passivation
- Industry Standard Plastic Macro-T Package
- Compatible with Other BFW92 Types



3

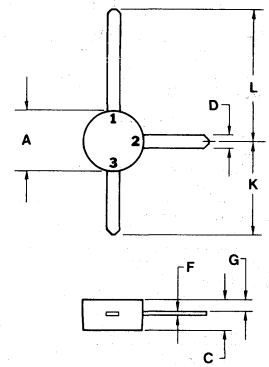
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CBO}	25	Vdc
Emitter-Base Voltage	V_{EBO}	2.5	Vdc
Collector-Current — Continuous	I_C	35	mAdc
Total Device Dissipation @ T_C = 105°C Derate Above 105°C	P_D	180 4.0	mW mW/°C
Storage Temperature Range	T_{stg}	-65 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction to Case (2)	$R_{\theta JC}$	250	°C/W

Note: Case temperature measured on collector lead immediately adjacent to body of package



STYLE 2.
PIN 1. COLLECTOR
2. EMITTER
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.44	5.21	0.175	0.205
C	1.90	2.54	0.075	0.100
D	0.94	0.99	0.033	0.039
F	0.20	0.30	0.008	0.012
G	0.76	1.14	0.030	0.045
K	7.24	8.13	0.285	0.320
L	10.54	11.43	0.415	0.450

CASE 317A-01

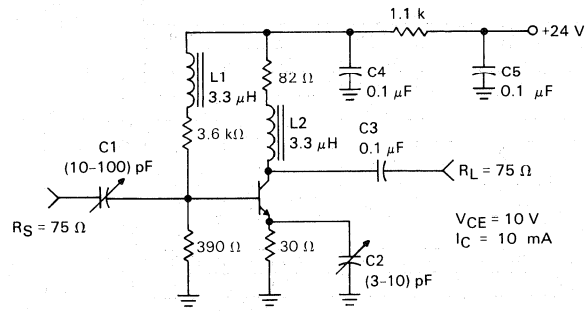
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	15	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	25	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	2.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}	—	—	50	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.0 mAdc, V_{CE} = 1.0 Vdc)	h_{FE}	20	50	150	—
DYNAMIC CHARACTERISTICS					
Current-Gain Bandwidth Product (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz)	f_T	—	4.5	—	GHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, f = 1.0 MHz, Emitter Guarded)	C_{cb}	—	0.5	1.0	pF
FUNCTIONAL PERFORMANCE					
Optimum Noise Figure (Tuned) (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz)	NF_{opt}	—	2.7	—	dB
Noise Figure (Untuned, R_S = R_L = 50 Ω) (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz)	NF	—	3.0	—	dB
Maximum Available Gain (1) (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz)	MAG	—	16	—	dB
Insertion Gain (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz)	$\|S_{21}\|^2$	—	14	—	dB

(1) $G_{max} = \dfrac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)}$

3

FIGURE 1 — 30-900 MHz BROADBAND AMPLIFIER



C3, C4, C5 — 0.1 μF Chip Capacitor
L1, L2 — 3.3 μH Molded Inductor

All Resistors 1/4 W, 20%

FIGURE 2 — BROADBAND GAIN (Circuit Figure 1)

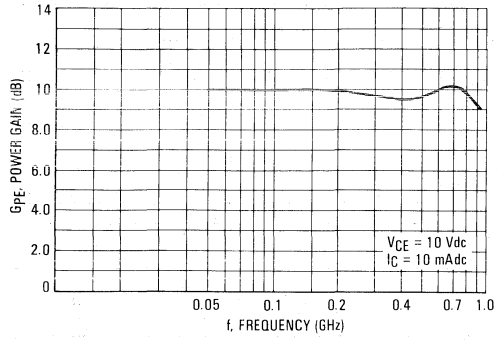


FIGURE 3 — 2nd AND 3rd ORDER INTERCEPT POINTS

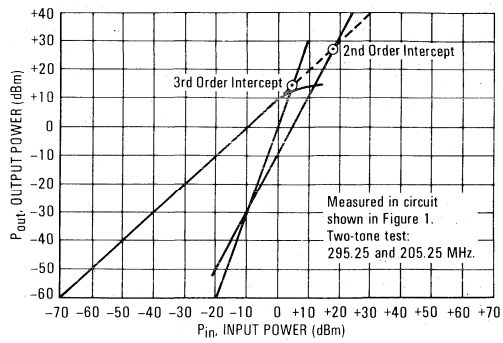


FIGURE 4 — MAXIMUM AVAILABLE GAIN versus FREQUENCY

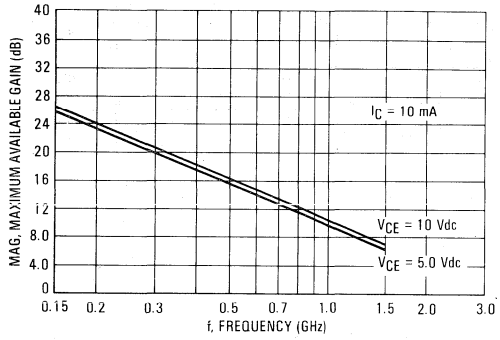


FIGURE 5 — $|S_{21}|^2$ versus FREQUENCY

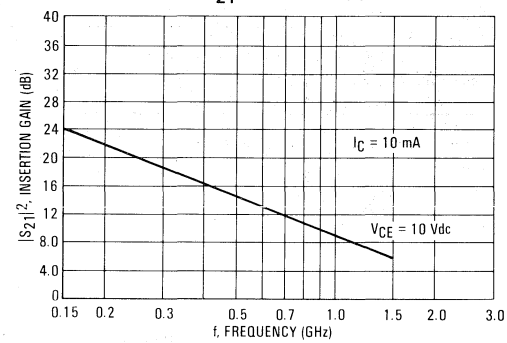


FIGURE 6 — MAXIMUM AVAILABLE GAIN versus COLLECTOR CURRENT

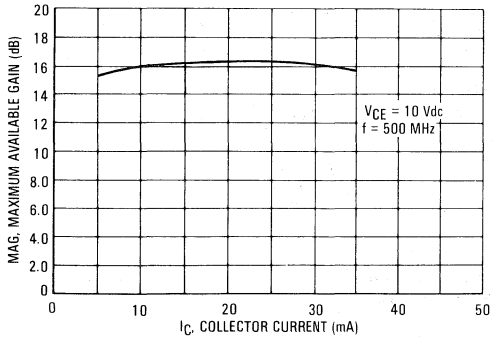


FIGURE 7 — GAIN-BANDWIDTH PRODUCT versus COLLECTOR CURRENT

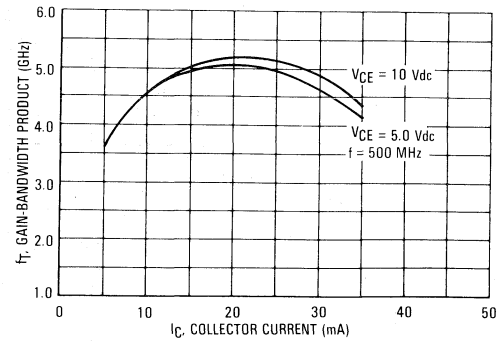


FIGURE 8 — NOISE FIGURE versus COLLECTOR CURRENT

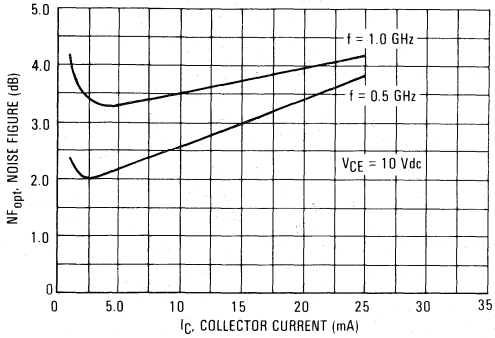


FIGURE 9 — NOISE FIGURE versus COLLECTOR CURRENT Untuned, $R_S = R_L = 50\ \Omega$

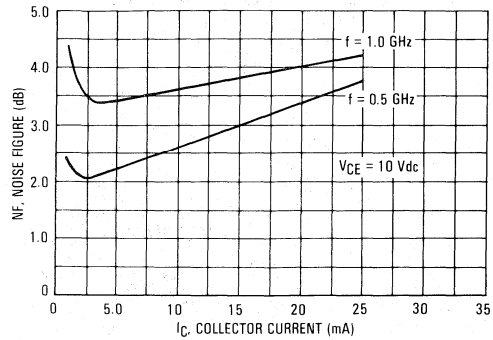


FIGURE 10 — NOISE FIGURE versus FREQUENCY

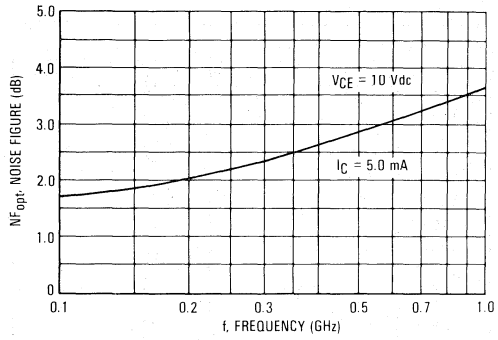


FIGURE 11 — NOISE FIGURE versus FREQUENCY Untuned $R_S = R_L = 50\ \Omega$

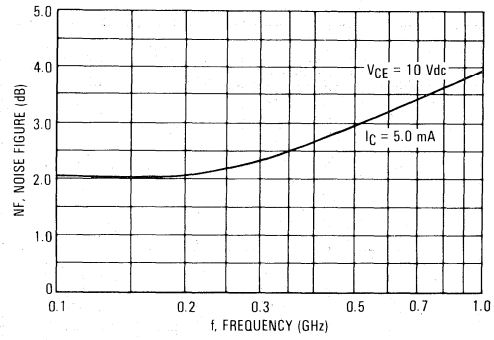


FIGURE 12 — C_{ib} INPUT CAPACITANCE versus EMITTER BASE VOLTAGE

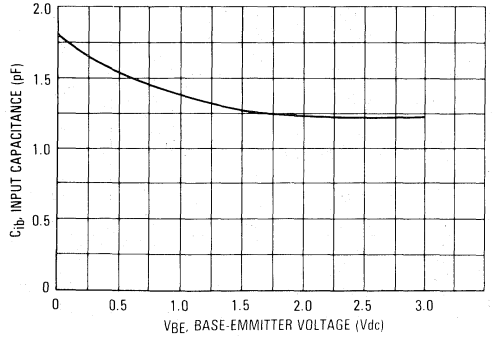
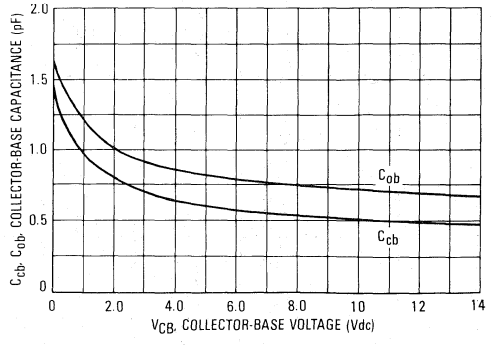


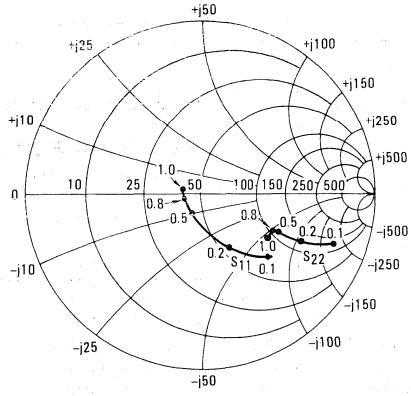
FIGURE 13 — COLLECTOR-BASE CAPACITANCE versus COLLECTOR-BASE VOLTAGE



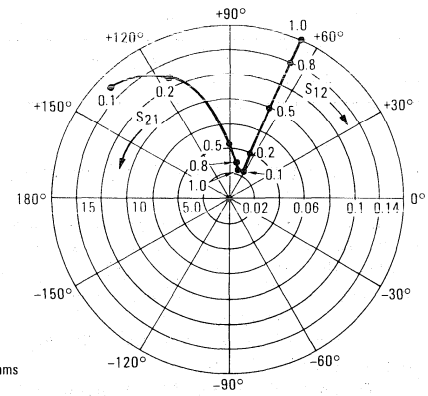
3

BFW92A COMMON-EMITTER S-PARAMETERS

INPUT/OUTPUT REFLECTION COEFFICIENTS versus FREQUENCY (V_{CE} = 10 V, I_C = 10 mA)



FORWARD/REVERSE TRANSMISSION COEFFICIENTS versus FREQUENCY (V_{CE} = 10 V, I_C = 10 mA)



Coordinates in Ohms

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
5.0	5.0	100	0.71	-33	11.2	145	0.031	69	0.87	-18
		200	0.49	-60	8.6	122	0.052	62	0.70	-26
		500	0.21	-119	4.5	92	0.094	61	0.48	-30
		800	0.17	-161	3.0	78	0.137	60	0.44	-36
		1000	0.16	176	2.5	71	0.164	60	0.44	-40
	10	100	0.52	-46	16.6	135	0.027	67	0.78	-23
		200	0.31	-75	11.2	113	0.044	65	0.58	-29
		500	0.14	-150	5.2	88	0.089	67	0.40	-29
		800	0.15	173	3.3	76	0.135	65	0.37	-34
		1000	0.16	154	2.8	70	0.164	64	0.37	-38
	15	100	0.40	-55	19.7	129	0.025	69	0.72	-26
		200	0.22	-88	12.1	109	0.041	68	0.52	-29
		500	0.14	-170	5.4	86	0.087	70	0.36	-27
		800	0.16	161	3.5	76	0.134	68	0.34	-33
		1000	0.17	145	2.9	69	0.164	66	0.35	-37
	20	100	0.33	-62	21.1	125	0.023	69	0.68	-27
		200	0.18	-99	12.5	106	0.039	69	0.49	-28
		500	0.14	178	5.5	85	0.086	72	0.35	-26
		800	0.17	155	3.5	75	0.133	69	0.33	-32
		1000	0.18	142	2.9	69	0.164	67	0.34	-37
	25	100	0.27	-69	21.9	122	0.022	70	0.65	-27
		200	0.15	-111	12.7	104	0.038	71	0.47	-27
		500	0.16	172	5.5	85	0.085	73	0.35	-25
		800	0.19	153	3.5	75	0.132	70	0.33	-31
		1000	0.20	140	2.9	69	0.163	68	0.33	-36
10	5.0	100	0.73	-30	11.1	146	0.026	71	0.90	-14
		200	0.53	-52	8.8	124	0.044	63	0.75	-21
		500	0.21	-98	4.7	94	0.082	62	0.57	-25
		800	0.14	-136	3.1	80	0.120	62	0.53	-30
		1000	0.11	-161	2.6	73	0.143	62	0.53	-34
	10	100	0.57	-39	16.7	137	0.023	70	0.82	-18
		200	0.35	-62	11.5	115	0.038	66	0.65	-23
		500	0.12	-117	5.4	89	0.078	69	0.50	-23
		800	0.09	-163	3.5	78	0.118	67	0.47	-28
		1000	0.09	168	2.9	71	0.144	66	0.48	-32
	15	100	0.46	-46	19.9	130	0.021	70	0.77	-20
		200	0.26	-68	12.6	110	0.035	68	0.60	-22
		500	0.09	-137	5.6	87	0.076	71	0.47	-21
		800	0.09	177	3.7	77	0.117	69	0.45	-27
		1000	0.10	153	3.0	71	0.143	68	0.46	-31
	20	100	0.39	-50	21.5	126	0.020	70	0.74	-21
		200	0.21	-73	13.0	107	0.034	71	0.58	-21
		500	0.08	-154	5.7	86	0.075	72	0.46	-20
		800	0.10	168	3.7	76	0.117	70	0.45	-27
		1000	0.11	148	3.0	71	0.142	69	0.45	-31
	25	100	0.34	-54	22.3	123	0.019	70	0.71	-20
		200	0.17	-79	13.0	105	0.033	71	0.57	-20
		500	0.08	-166	5.7	86	0.075	73	0.47	-19
		800	0.11	162	3.7	76	0.116	70	0.45	-26
		1000	0.13	144	3.0	70	0.141	69	0.46	-30

BFX89
BFY90

The RF Line

NPN SILICON HIGH-FREQUENCY TRANSISTORS

. . . designed for VHF and UHF applications where high-gain, low-noise and good intermodulation characteristics are required. Particularly suited for wideband MATV amplifiers.

- High Current-Gain — Bandwidth Product — f_T
  1.2 GHz (Min) @ I_C = 25 mAdc — BFX89
  1.3 GHz (Min) @ I_C = 25 mAdc — BFY90
- Low Noise Figure — NF
  6.5 dB (Max) @ f = 500 MHz — BFX89
  5.0 dB (Max) @ f = 500 MHz — BFY90
- High Power Gain — G_{pe}
  19 dB (Min) @ f = 200 MHz — BFX89
  21 dB (Typ) @ f = 200 MHz — BFY90
- JEDEC Equivalents — 2N6304, 2N6305

f_T = 2.0 GHz @ 10 mA

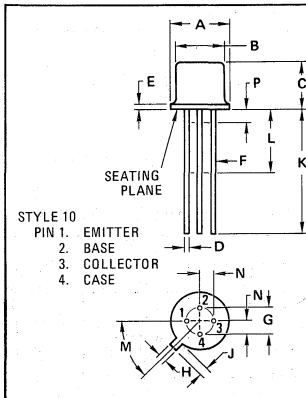
HIGH FREQUENCY TRANSISTORS

NPN SILICON



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CBO}	30	Vdc
Emitter-Base Voltage	V_{EBO}	2.5	Vdc
Collector-Current — Continuous	I_C	50	mAdc
Total Continuous Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	200 1.14	mW mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

CASE 20-3
TO-72

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)		$V_{(BR)CEO}$	15	—	—	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)		I_{CBO}	—	—	10	nAdc
ON CHARACTERISTICS						
DC Current Gain		h_{FE}				—
(I_C = 2.0 mAdc, V_{CE} = 1.0 Vdc)			25	—	150	
(I_C = 25 mAdc, V_{CE} = 1.0 Vdc)			20	—	125	
DYNAMIC CHARACTERISTICS						
Collector-Base Capacitance (1)	BFX89	C_{cbo}	—	0.85	1.7	pF
(V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	BFY90		—	0.85	1.5	
Emitter-Base Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)	BFY90	C_{ibo}	—	—	2.0	pF
Current-Gain-Bandwidth Product (2)		f_T				GHz
(I_C = 2.0 mA, V_{CE} = 5.0 Vdc, f = 500 MHz)	BFX89		—	1.0	—	
	BFY90		1.0	—	—	
(I_C = 25 mA, V_{CE} = 5.0 Vdc, f = 500 MHz)	BFX89		1.2	1.1	—	
	BFY90		1.3	—	—	
FUNCTIONAL TEST						
Common-Emitter Amplifier Power Gain (2)	BFX89	G_{pe}	19	—	—	dB
(V_{CE} = 10 Vdc, I_C = 8.0 mA, f = 200 MHz)	BFY90		—	21	—	
Spot Noise Figure (R_S = Optimum) (2)	BFX89	NF	—	2.5	6.5	dB
(V_{CE} = 5.0 Vdc, I_C = 2.0 mA, f = 500 MHz)	BFY90		—	2.5	5.0	

Notes 1. Pin 4 is not grounded.
2. Pin 4 is grounded.
3. $G_U(max)$ is calculated from the S-Parameters using the equation $G_U(max) = \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)}$

FIGURE 1 — POWER GAIN versus FREQUENCY

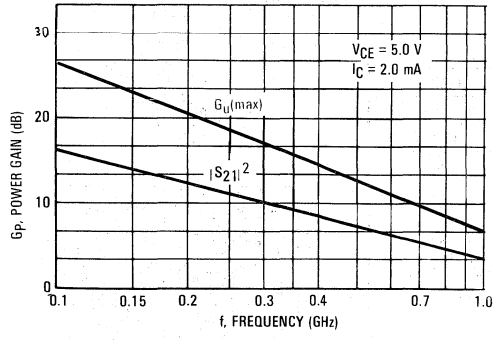


FIGURE 2 — POWER GAIN versus COLLECTOR CURRENT

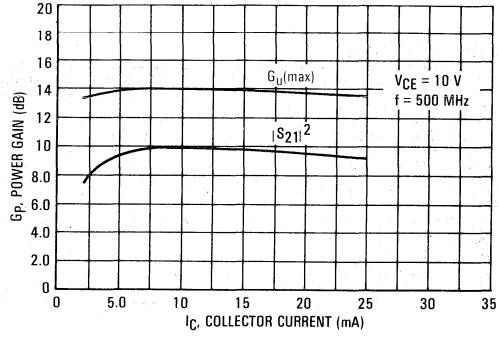


FIGURE 3 — NOISE FIGURE versus FREQUENCY

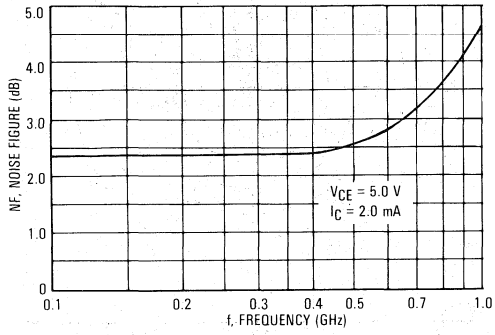


FIGURE 4 — NOISE FIGURE versus COLLECTOR CURRENT

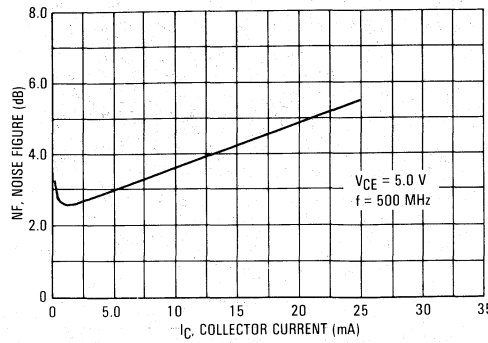


FIGURE 5 — CURRENT GAIN-BANDWIDTH PRODUCT versus COLLECTOR CURRENT

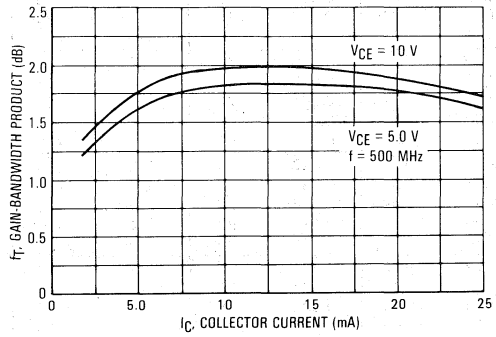
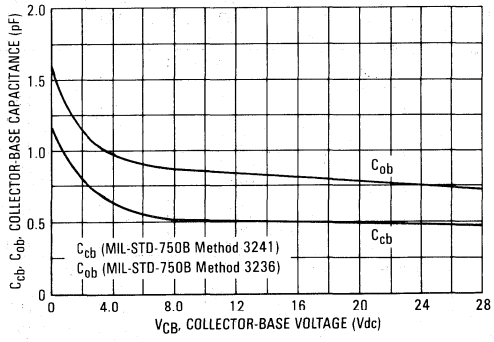


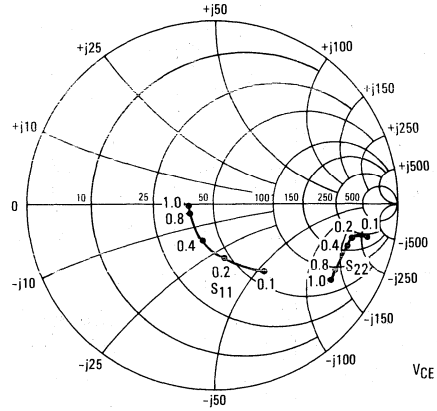
FIGURE 6 — OUTPUT CAPACITANCE versus VOLTAGE



3

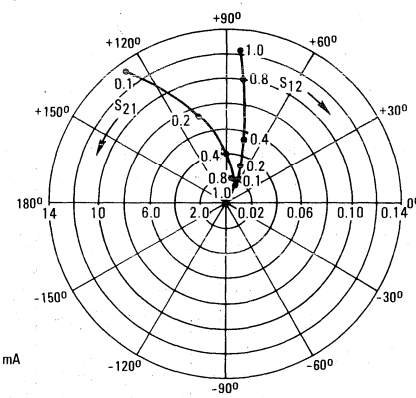
COMMON EMITTER SCATTERING PARAMETERS

FIGURE 7 — INPUT AND OUTPUT REFLECTION COEFFICIENTS versus FREQUENCY



Coordinates in Ohms

FIGURE 8 — FORWARD AND REVERSE TRANSMISSION COEFFICIENTS versus FREQUENCY



V_{CE} = 10 V, I_C = 10 mA

S — PARAMETERS

V_{CE} (Volts)	I_C (mA)	Frequency (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
5.0	2.0	100	0.81	-37	5.76	148	0.031	72	0.95	-11
		200	0.64	-66	4.56	127	0.050	63	0.87	-17
		400	0.41	-105	2.91	102	0.071	62	0.79	-23
		800	0.26	-157	1.63	77	0.105	74	0.75	-34
		1000	0.23	179	1.38	68	0.129	80	0.74	-41
	5.0	100	0.60	-54	9.73	133	0.026	68	0.87	-13
		200	0.41	-84	6.33	112	0.040	66	0.78	-17
		400	0.26	-121	3.54	92	0.064	72	0.73	-21
		800	0.19	-169	1.89	72	0.112	80	0.72	-31
		1000	0.17	168	1.59	64	0.140	82	0.71	-39
	10	100	0.71	-66	12.13	122	0.022	70	0.81	-14
		200	0.28	-96	7.11	104	0.036	71	0.73	-15
		400	0.19	-133	3.85	88	0.064	77	0.70	-19
		800	0.18	-178	2.00	69	0.115	83	0.71	-30
		1000	0.17	160	1.66	61	0.143	84	0.70	-37
	25	100	0.26	-88	12.79	112	0.019	73	0.76	-13
		200	0.20	-122	7.04	97	0.034	76	0.71	-13
		400	0.20	-156	3.68	83	0.062	81	0.70	-18
		800	0.23	165	1.88	65	0.114	86	0.71	-30
		1000	0.24	146	1.56	58	0.145	88	0.70	-38
10	2.0	100	0.83	-34	5.82	150	0.025	73	0.96	-9
		200	0.66	-61	4.60	129	0.042	65	0.89	-15
		400	0.42	-97	2.98	104	0.059	64	0.83	-20
		800	0.25	-147	1.69	79	0.088	77	0.80	-31
		1000	0.20	-172	1.42	70	0.108	82	0.79	-38
	5.0	100	0.63	-48	9.94	135	0.021	70	0.90	-11
		200	0.43	-76	6.54	114	0.034	68	0.82	-15
		400	0.26	-108	3.72	94	0.054	73	0.77	-19
		800	0.16	-155	1.98	74	0.095	83	0.77	-24
		1000	0.14	180	1.65	66	0.119	85	0.76	-36
	10	100	0.47	-57	12.42	125	0.019	70	0.85	-12
		200	0.30	-83	7.43	106	0.031	72	0.78	-14
		400	0.19	-113	4.04	90	0.054	78	0.75	-18
		800	0.14	-160	2.09	71	0.098	84	0.75	-28
		1000	0.13	173	1.73	64	0.121	86	0.75	-35
	25	100	0.32	-71	13.05	114	0.017	72	0.81	-11
		200	0.21	-99	7.27	99	0.029	76	0.77	-12
		400	0.16	-135	3.81	85	0.052	81	0.76	-16
		800	0.17	177	1.96	68	0.096	87	0.76	-28
		1000	0.18	154	1.62	61	0.120	89	0.76	-35

MD4957

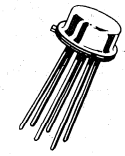
DUAL PNP SILICON ANNULAR 450-MHz AMPLIFIER

. . . designed for high-gain, low-noise amplifier, oscillator, and mixer applications.

- Low Noise Figure — NF = 3.0 dB (typ) @ 450 MHz
  6.0 dB (Typ) @ 1.0 GHz
- High Power Gain — Gpe = 18 dB (Typ) @ 450 MHz
  13 dB (Typ) @ 1.0 GHz
- High Gain-Bandwidth Product — fT = 1500 MHz (Typ)
- Low Collector-Base Capacitance — C_{cb} = 0.8 pF (Typ)

MULTIPLE DEVICES

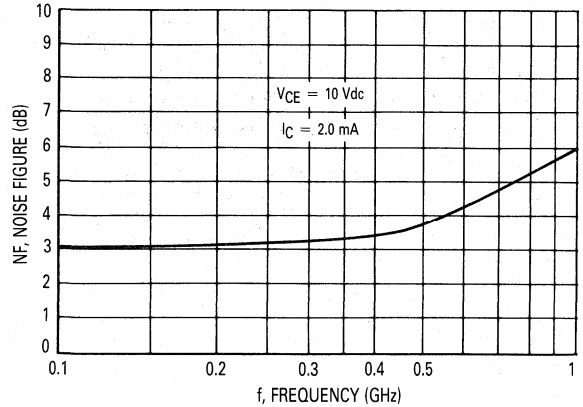
DUAL PNP SILICON AMPLIFIER

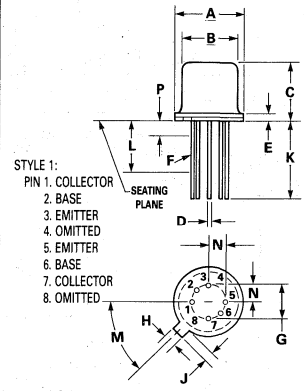


MAXIMUM RATINGS (each side)

Rating	Symbol	Value		Unit
Collector-Emitter Voltage	V_{CEO}	30		Vdc
Collector-Base Voltage	V_{CB}	30		Vdc
Emitter-Base Voltage	V_{EB}	3.0		Vdc
Collector Current	I_C	30		mAdc
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C
		One Side	Both Sides	
Total Device Dissipation @ T_A = 25°C	P_D	200	400	mW
Derate above 25°C		1.15	2.3	mW/°C

FIGURE 1 — NOISE FIGURE (TYPICAL) VS FREQUENCY





NOTE:
1. ALL RULES & NOTES ASSOCIATED WITH REFERENCED TO-78 (654-02) OUTLINE SHALL APPLY.

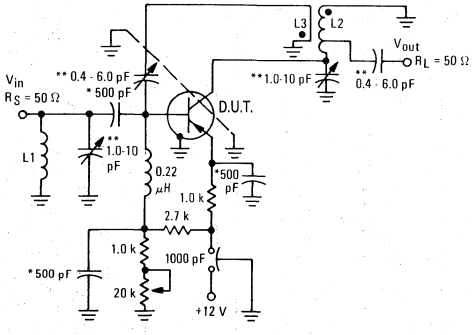
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	4.19	4.70	0.165	0.185
D	0.41	0.53	0.016	0.021
E	—	1.02	—	0.040
F	0.41	0.48	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.71	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	—	0.500	—
L	6.35	—	0.250	—
M	45° BSC		45° BSC	
N	2.54 BSC		0.100 BSC	
P	—	1.27	—	0.050

CASE 654-02

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	-	-	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	$V_{(BR)CBO}$	30	-	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	$V_{(BR)EBO}$	3.0	-	-	Vdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)	I_{CBO}	-	-	0.1	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.0 mAdc, V_{CE} = 10 Vdc)	h_{FE}	20	-	150	-
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	1000	1500	-	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{cb}	-	0.8	1.5	pF
Small-Signal Current Gain (I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	20	-	200	-
Collector-Base Time Constant (I_E = 2.0 mAdc, V_{CB} = 10 Vdc, f = 63.6 MHz)	$r_b'C_c$	-	10	20	ps
Noise Figure (I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 450 MHz) Figure 2	NF	-	3.0	-	dB
(I_C = 2.0 mAdc, V_{CE} = 10 Vdc, R_S = 50 ohms, f = 1.0 GHz)		-	6.0	-	
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CE} = 10 Vdc, I_C = 2.0 mAdc, f = 450 MHz)	G_{pe}	-	18	-	dB
(V_{CE} = 10 Vdc, I_C = 2.0 mAdc, R_S = 50 ohms, f = 1.0 GHz)		-	13	-	

FIGURE 2 — NOISE FIGURE AND POWER GAIN TEST CIRCUIT



*Button type capacitors
**Variable air piston type capacitors
1. L1 — silver plated brass bar, 1.0 in. lg by 0.25 in od.
2. L2 — silver plated brass bar, 1.5 in. lg by 0.25 in od. Tap is 0.25 in. from collector
3. L3 — ½ turn of AWG No. 16 wire 0.25 in. from and parallel to L2.
4. The noise source is a hot-cold body (All type 70 or equivalent) with a test receiver (All type 136 or equivalent).
5. Each half of dual transistor tested separately.

COMMON EMITTER Y PARAMETER VARIATIONS

Y PARAMETERS VS FREQUENCY

V_{CE} = 10 Vdc

I_C = 2.0 mA

FIGURE 3 — INPUT ADMITTANCE

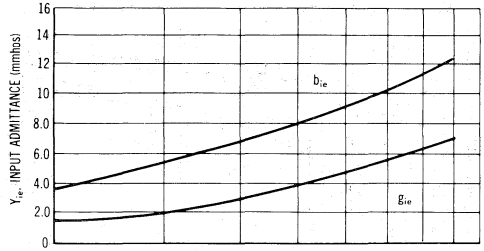


FIGURE 4 — FORWARD TRANSFER ADMITTANCE

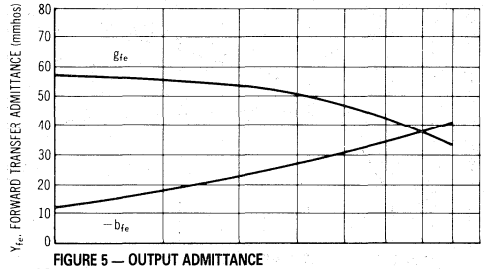


FIGURE 5 — OUTPUT ADMITTANCE

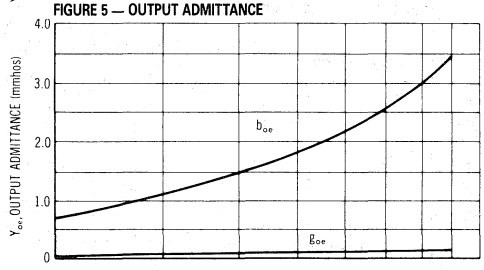
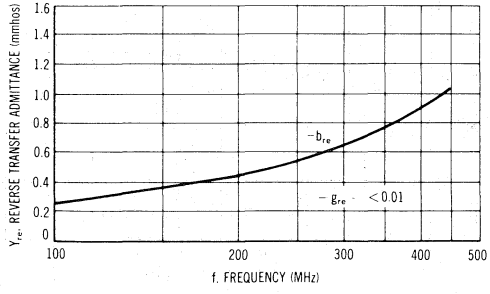


FIGURE 6 — REVERSE TRANSFER ADMITTANCE



Y PARAMETERS VS CURRENT

V_{CE} = 10 Vdc ——— V_{CE} = 15 Vdc — — —

f = 450 MHz

FIGURE 7 — INPUT ADMITTANCE

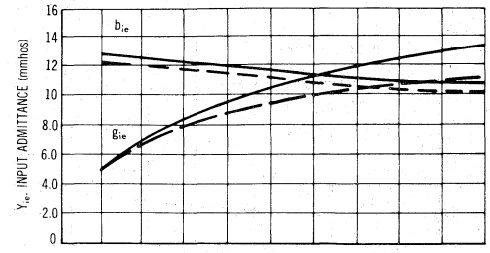


FIGURE 8 — FORWARD TRANSFER ADMITTANCE

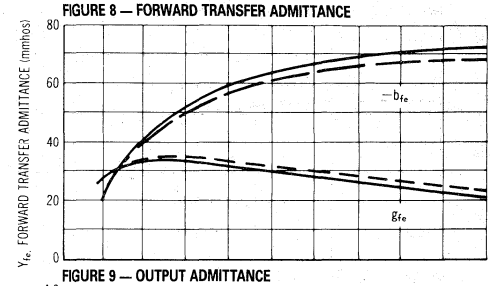


FIGURE 9 — OUTPUT ADMITTANCE

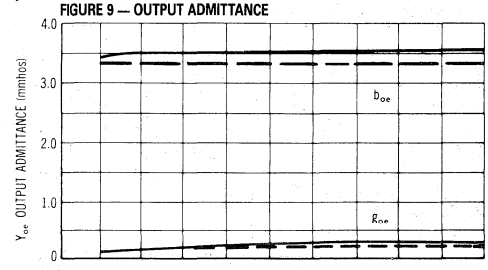
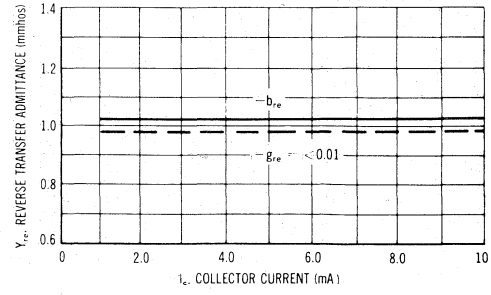


FIGURE 10 — REVERSE TRANSFER ADMITTANCE



COMMON BASE Y PARAMETER VARIATIONS

Y PARAMETERS versus FREQUENCY

V_{CB} = 10 Vdc

I_C = 2.0 mA

FIGURE 11 — INPUT ADMITTANCE

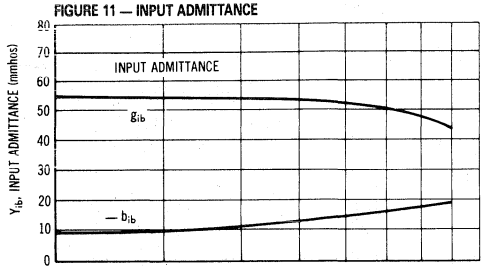


FIGURE 12 — FORWARD TRANSFER ADMITTANCE

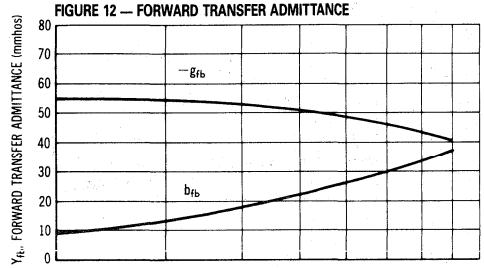


FIGURE 13 — OUTPUT ADMITTANCE

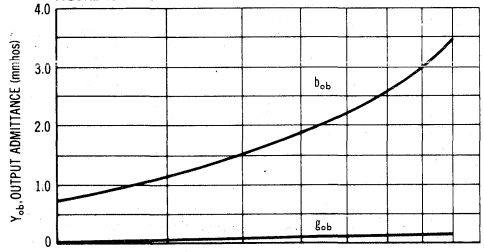
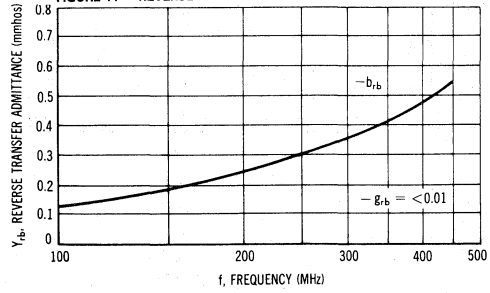


FIGURE 14 — REVERSE TRANSFER ADMITTANCE



Y PARAMETERS versus CURRENT

V_{CB} = 10 Vdc —— V_{CB} = 15 Vdc — — —

f = 450 MHz

FIGURE 15 — INPUT ADMITTANCE

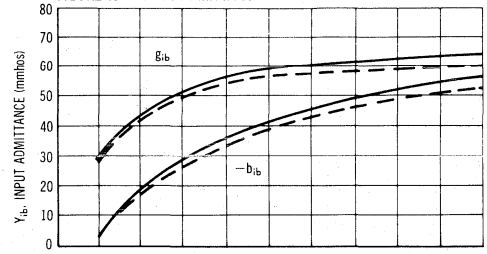


FIGURE 16 — FORWARD TRANSFER ADMITTANCE

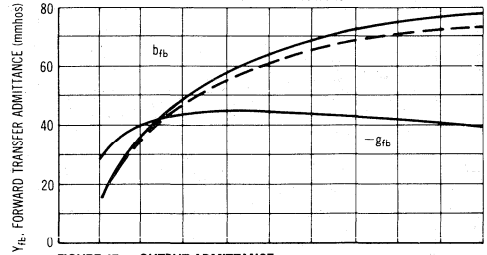


FIGURE 17 — OUTPUT ADMITTANCE

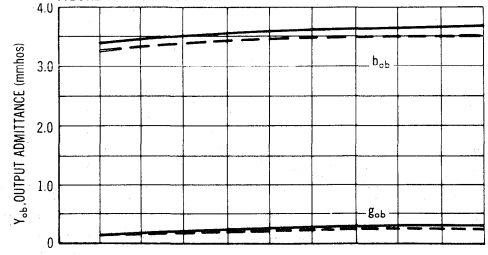
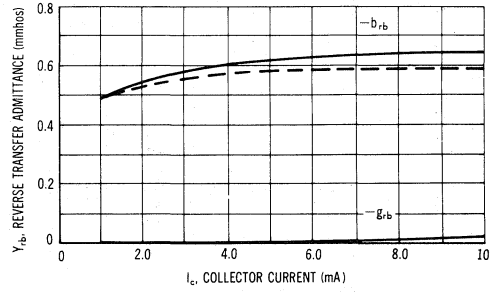


FIGURE 18 — REVERSE TRANSFER ADMITTANCE



MM4018

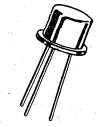
The RF Line

PNP SILICON RF POWER TRANSISTOR

PNP SILICON
RF POWER
TRANSISTOR

. . . designed for amplifier, frequency multiplier or oscillator applications in military and industrial equipment. Suitable for use as Class A, B, or C driver, or pre-driver stages in VHF applications.

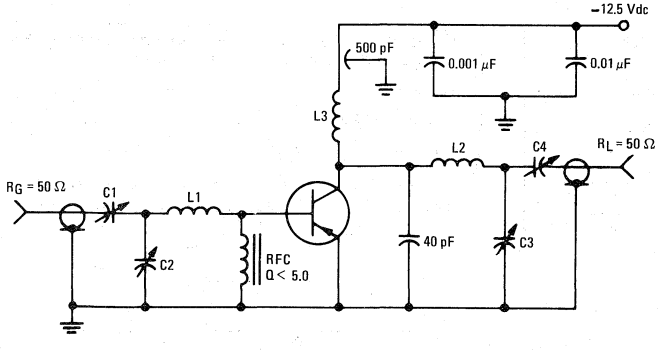
- Power Output – P_{out} = 0.5 W (Min) @ f = 175 MHz
- High Current-Gain – Bandwidth Product – f_T = 900 MHz (Typ) @ I_C = 50 mAdc



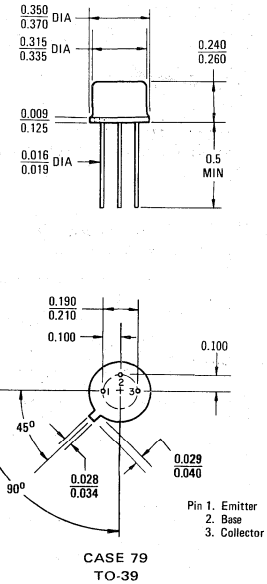
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current – Continuous	I_C	0.4	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	5.0 28.6	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

FIGURE 1 – 175 MHz OUTPUT POWER TEST CIRCUIT



C1, C2 3.0 – 30 pF, ARCO 461 OR EQUIVALENT
C3, C4 8.0 – 80 pF, ARCO 462 OR EQUIVALENT
L1 100 nH, 4 TURNS NO. 18 AWG, 1/4" I.D., 5/8" LENGTH
L2 40 nH, 2 TURNS NO. 18 AWG, 1/4" I.D., 1/2" LENGTH
L3 200 nH, 8 TURNS NO. 18 AWG, 1/4" I.D., 7/8" LENGTH



CASE 79
TO-39

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 5.0 mAdc, I_E = 0)	$V_{(BR)CBO}$	40	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, I_B = 0)	I_{CEO}	–	–	20	μAdc
Collector Cutoff Current (V_{CE} = 40 Vdc, V_{BE} = 0)	I_{CES}	–	–	0.1	mAdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	10	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 50 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	–	–	–
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 50 mAdc, V_{CE} = 15 Vdc, f = 100 MHz)	f_T	–	900	–	MHz
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	–	3.5	–	pF
FUNCTIONAL TEST					
Power Output (Figure 1) (P_{in} = 50 mW, V_{CC} = 12.5 Vdc, f = 175 MHz)	P_{out}	0.5	–	–	Watt
Collector Efficiency (Figure 1) (P_{in} = 50 mW, V_{CC} = 12.5 Vdc, f = 175 MHz)	η	45	55	–	%

FIGURE 2 – POWER OUTPUT versus POWER INPUT

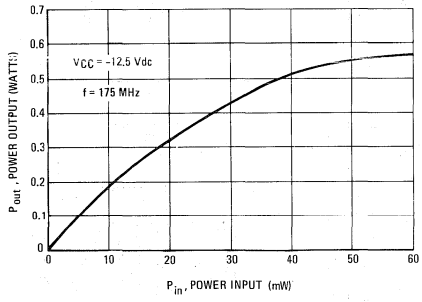


FIGURE 3 – PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY

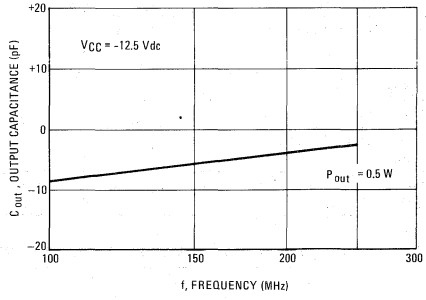


FIGURE 4 – PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

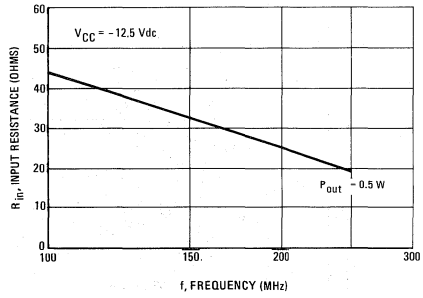
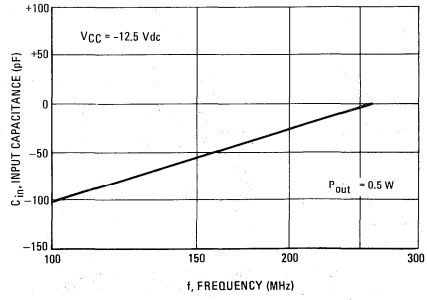


FIGURE 5 – PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY



MM4019

The RF Line

PNP SILICON HIGH FREQUENCY TRANSISTOR

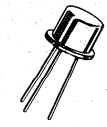
. . . designed for amplifier and oscillator applications in military and industrial equipment. Suitable for use as output, driver or pre-driver stages in UHF and VHF equipment.

- Specified 175 MHz, 28 Vdc Characteristics –
  Output Power = 2.5 Watts
  Efficiency = 50%

2.5 W – 175 MHz

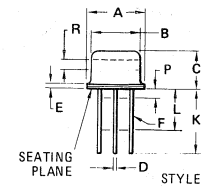
HIGH FREQUENCY TRANSISTOR

PNP SILICON

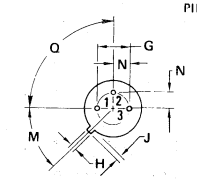


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current – Continuous	I_C	1.0	Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	5.0 28.6	Watts mW/^oC
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	^oC



STYLE 1
PIN 1. EMITTER
2. BASE
3. COLLECTOR



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

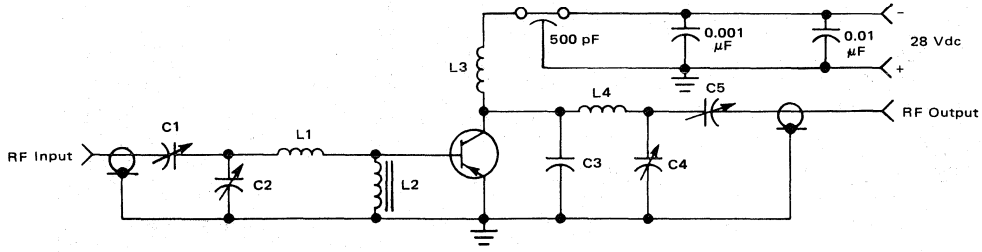
All JEDEC dimensions and notes apply.

CASE 79-02
TO-39

ELECTRICAL CHARACTERISTICS (T_A = 25° unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	$V_{(BR)CEO}$	40	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 10 mAdc, I_E = 0)	$V_{(BR)CBO}$	60	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 Adc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	–	–	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	–	0.1	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	–	–	–
Collector-Emitter Saturation Voltage (I_C = 250 mAdc, I_B = 50 mAdc)	$V_{CE(sat)}$	–	–	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain–Bandwidth Product (I_C = 100 mAdc, V_{CE} = 28 Vdc, f = 100 MHz)	f_T	–	750	–	MHz
Output Capacitance (V_{CB} = 30 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	–	7.5	–	pF
FUNCTIONAL TEST					
Power Input (P_{out} = 2.5 W, V_{CC} = 28 Vdc, f = 175 MHz)	P_{in}	–	–	0.25	Watt
Power Output (P_{in} = 0.5 W, V_{CC} = 28 Vdc, f = 400 MHz)	P_{out}	–	2.0	–	Watts
Collector Efficiency (P_{out} = 2.5 W, V_{CC} = 28 Vdc, f = 175 MHz)	η	50	–	–	%

FIGURE 1 – 175 MHz TEST CIRCUIT



C1,C2 3.0-30 pF, ARCO 461 or equivalent.
C3 40 pF
C4,C5 5.0-80 pF, ARCO 462 or equivalent.
L1 80 nH, 3 Turns #18 AWG, 1/4" I.D., 1/4" Length
L2 Ferrite Choke, VK-200 Ferroxcube, Q < 5
L3 0.15 µH, RF Choke
L4 27 nH, 2 Turns #18 AWG, 1/4" I.D., 3/8" Length

MM4049
MMC4049
MRF534
MRF536

The RF Line

PNP SILICON HIGH-FREQUENCY TRANSISTOR

. . . designed for use as a high-frequency current mode switch. Because of the extremely high Current-Gain — Bandwidth this transistor also makes an excellent RF amplifier and oscillator.

- High Current-Gain — Bandwidth Product —
  f_T = 4.0 GHz (Min) @ I_C = 20 mAdc — MM4049, MRF534
  f_T = 5.0 GHz (Min) @ I_C = 20 mAdc — MRF536
- Low Collector-Base Capacitance —
  C_{cb} = 1.25 pF (Max) @ V_{CB} = 5.0 Vdc

4.0 GHz @ 20 mAdc

HIGH FREQUENCY TRANSISTOR

PNP SILICON

MAXIMUM RATINGS

		MMC4049	MM4049	MRF534	MRF536	
		 Chip	 Case 20-03 TO-206AF	 Case 22-03 TO-206AA	 Case 317-01 Macro-X	
Ratings	**Symbol**			**Values**		**Unit**
Collector-Emitter Voltage	V_{CEO}	10	10	10	10	Vdc
Collector-Base Voltage	V_{CBO}	15	15	15	15	Vdc
Emitter-Base Voltage	V_{EBO}	4.5	4.5	4.5	4.5	Vdc
Collector Current — Continuous	I_C	30	30	30	30	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 $T_{J\,max}$=200°C	200 1.14	300 1.71	300 2.40	mW mW/°C
Operating and Storage Junction Temperature Junction	T_J, T_{stg}	-65 to +200	-65 to +200	-65 to +200	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 2.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	10	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	$V_{(BR)CBO}$	15	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	$V_{(BR)EBO}$	4.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}	—	—	10	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 25 mAdc, V_{CE} = 2.0 Vdc)	h_{FE}	20	—	200	—
DYNAMIC CHARACTERISTICS					
Current-Gain Bandwidth Product MRF534, MM4049 (I_C = 20 mAdc, V_{CE} = 5.0 Vdc, f = 500 MHz) MRF536	f_T	4.0 5.0	— —	— —	GHz
Collector-Base Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	—	—	1.3	pF
FUNCTIONAL TESTS					
Maximum Available Gain	MAG				dB
(I_C = 15 mAdc, V_{CE} = 5.0 Vdc, f = 500 MHz) MRF534		10	12	—	
(I_C = 15 mAdc, V_{CE} = 5.0 Vdc, f = 500 MHz) MM4049		11.5	13	—	
(I_C = 15 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 GHz) MRF536		8.5	10	—	

FIGURE 1 — CURRENT GAIN — BANDWIDTH PRODUCT versus CURRENT

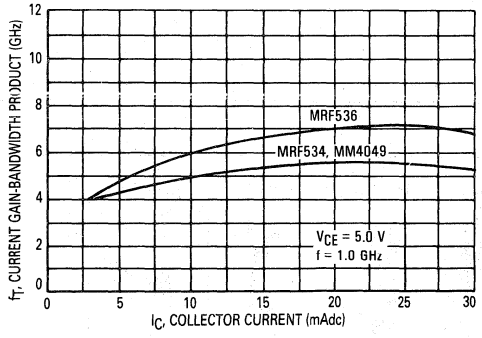


FIGURE 2 — MAXIMUM AVAILABLE GAIN versus COLLECTOR CURRENT

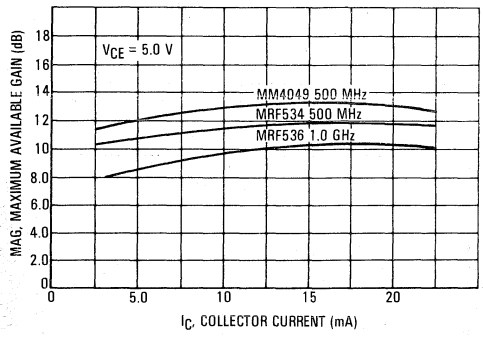
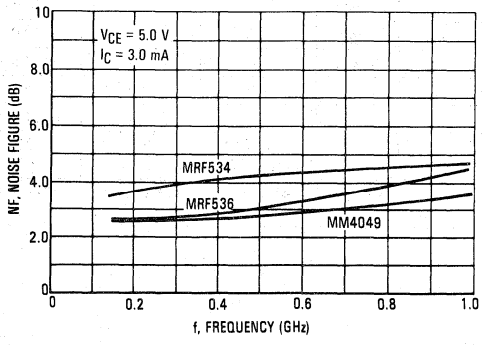


FIGURE 3 — NOISE FIGURE versus FREQUENCY



MRF534 COMMON-EMITTER S-PARAMETERS

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
5.0	5.0	200	0.734	-22	3.70	126	0.066	66	0.507	-39
		400	0.580	-28	2.56	108	0.116	65	0.409	-48
		600	0.444	-37	2.09	95	0.158	62	0.403	-52
		800	0.400	-47	1.80	86	0.195	56	0.364	-56
		1000	0.366	-47	1.55	79	0.234	51	0.348	-69
	10	200	0.645	-27	5.36	124	0.058	69	0.394	-43
		400	0.503	-33	3.44	106	0.109	71	0.316	-52
		600	0.376	-43	2.68	93	0.153	69	0.323	-52
		800	0.333	-54	2.24	84	0.192	65	0.290	-55
		1000	0.295	-54	1.91	77	0.233	61	0.276	-71
	20	200	0.586	-28	5.90	122	0.053	70	0.338	-52
		400	0.454	-34	3.73	105	0.099	73	0.259	-60
		600	0.329	-46	2.87	93	0.143	72	0.267	-58
		800	0.289	-59	2.38	85	0.181	68	0.240	-59
		1000	0.248	-58	2.04	77	0.221	65	0.235	-75
10	5.0	200	0.752	-21	4.28	125	0.066	70	0.550	-28
		400	0.624	-26	2.77	107	0.123	68	0.495	-38
		600	0.512	-34	2.19	94	0.168	65	0.503	-44
		800	0.476	-44	1.86	86	0.207	60	0.464	-51
		1000	0.447	-45	1.60	79	0.246	55	0.443	-64
	10	200	0.685	-24	5.47	123	0.060	71	0.442	-33
		400	0.553	-28	3.46	105	0.113	71	0.385	-42
		600	0.433	-37	2.68	93	0.156	68	0.397	-46
		800	0.391	-49	2.25	85	0.194	63	0.362	-51
		1000	0.359	-47	1.92	78	0.233	59	0.342	-65
	20	200	0.621	-26	6.38	121	0.055	71	0.372	-40
		400	0.488	-31	3.97	104	0.103	72	0.316	-48
		600	0.365	-41	3.04	93	0.145	70	0.332	-50
		800	0.323	-52	2.51	85	0.182	66	0.301	-54
		1000	0.290	-50	2.13	79	0.219	63	0.288	-68

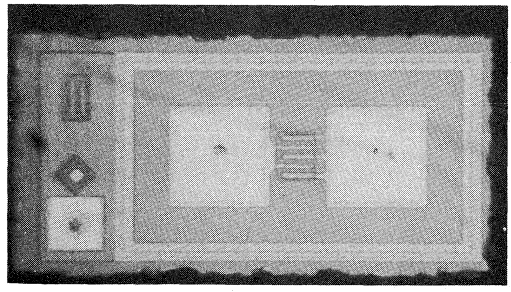
MM4049 COMMON-EMITTER S-PARAMETERS

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
5.0	5.0	200	0.634	-31	6.37	120	0.060	69	0.711	-23
		400	0.469	-34	3.95	93	0.107	65	0.602	-30
		600	0.379	-40	2.90	77	0.147	62	0.587	-33
		800	0.368	-51	2.32	65	0.183	56	0.55	-36
		1000	0.381	-54	1.93	55	0.223	50	0.528	-44
	10	200	0.523	-29	7.79	112	0.056	72	0.632	-23
		400	0.418	-28	3.74	89	0.104	68	0.543	-29
		600	0.344	-34	3.20	74	0.146	65	0.542	-32
		800	0.345	-46	2.54	64	0.184	58	0.513	-34
		1000	0.366	-50	2.09	54	0.225	52	0.493	-42
	20	200	0.454	-25	8.43	106	0.065	73	0.584	-21
		400	0.390	-23	4.67	85	0.105	70	0.513	-27
		600	0.325	-30	3.31	72	0.148	66	0.620	-30
		800	0.327	-44	2.61	62	0.188	59	0.497	-32
		1000	0.351	-48	2.15	52	0.231	52	0.476	-41
10	5.0	200	0.731	-25	5.83	121	0.053	70	0.736	-18
		400	0.589	-30	3.65	95	0.096	67	0.654	-26
		600	0.502	-38	2.71	79	0.132	64	0.645	-29
		800	0.496	-49	2.21	68	0.164	57	0.612	-33
		1000	0.499	-54	1.83	58	0.198	51	0.592	-42
	10	200	0.643	-25	7.37	114	0.051	71	0.668	-18
		400	0.542	-27	4.28	90	0.094	69	0.060	-25
		600	0.466	-34	3.10	76	0.132	65	0.603	-28
		800	0.465	-46	2.49	66	0.166	59	0.577	-31
		1000	0.476	-51	2.05	57	0.202	53	0.557	-40
	20	200	0.57	-23	8.44	109	0.049	73	0.621	-18
		400	0.496	-24	4.73	88	0.093	71	0.562	-24
		600	0.427	-31	3.38	75	0.131	67	0.572	-27
		800	0.427	-43	2.69	66	0.165	60	0.551	-30
		1000	0.445	-47	2.21	57	0.203	54	0.532	-38

MRF536 COMMON-EMITTER S-PARAMETERS

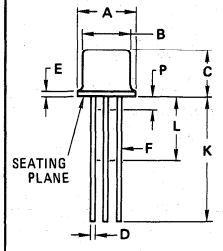
V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
5.0	5.0	400	0.401	-74	5.38	108	0.09	54	0.49	-48
		800	0.181	-102	3.03	86	0.138	51	0.35	-64
		1200	0.136	-157	2.13	70	0.181	48	0.32	-70
		1600	0.151	175	1.68	59	0.21	45	0.27	-80
		2000	0.16	148	1.44	52	0.24	41	0.269	-100
	10	400	0.289	-94	6.58	103	0.076	56	0.379	-56
		800	0.14	-137	3.55	84	0.122	55	0.266	-73
		1200	0.174	169	2.46	70	0.165	53	0.238	-77
		1600	0.196	154	1.93	60	0.196	50	0.198	-87
		2000	0.227	130	1.65	51	0.230	46	0.202	-110
	20	400	0.233	-118	7.28	99	0.066	60	0.296	-65
		800	0.163	-169	3.88	82	0.110	59	0.204	-84
		1200	0.233	156	2.65	69	0.153	57	0.179	-84
		1600	0.253	144	2.06	59	0.186	55	0.143	-96
		2000	0.290	123	1.75	50	0.220	51	0.160	-121
10	5.0	400	0.478	-54	5.14	109	0.086	58	0.535	-39
		800	0.279	-66	2.90	88	0.141	53	0.420	-55
		1200	0.166	-97	2.08	73	0.184	48	0.388	-62
		1600	0.151	-123	1.67	64	0.209	44	0.33	-72
		2000	0.110	-158	1.44	55	0.243	39	0.313	-90
	10	400	0.356	-67	6.59	105	0.075	59	0.418	-47
		800	0.182	-84	3.59	86	0.124	56	0.311	-62
		1200	0.119	-141	2.53	73	0.166	52	0.284	-67
		1600	0.131	-166	2.00	62	0.193	49	0.230	-76
		2000	0.135	154	1.72	55	0.226	45	0.222	-98
	20	400	0.26	-85	7.66	101	0.066	61	0.328	-53
		800	0.124	122	4.09	84	0.111	59	0.236	-69
		1200	0.148	172	2.83	72	0.152	56	0.216	-71
		1600	0.172	158	2.22	62	0.182	54	0.172	-80
		2000	0.201	130	1.88	54	0.214	50	0.171	-104

MMC4049 CHIP TOPOGRAPHY



Nominal Chip Size: 12 × 22 mils
Front Metalization: Aluminum
Back Metalization: Aluminum
Emitter/Base Bond Pad: 4.0 × 4.0 mils
#Emitter Fingers: 2
#Base Fingers: 3

OUTLINE DIMENSIONS

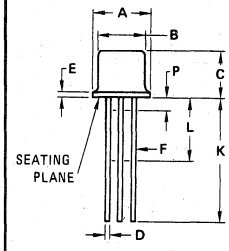


STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

CASE 20-03

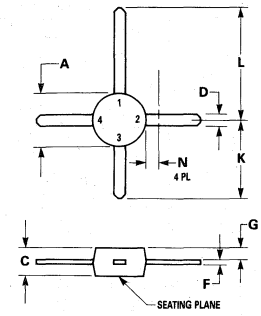


STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.406	0.533	0.016	0.021
E	–	0.762	–	0.030
F	0.406	0.483	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.914	1.17	0.036	0.046
J	0.711	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

All JEDEC notes and dimensions apply.

CASE 22-03



STYLE 2:
PIN 1. COLLECTOR
2. EMITTER
3. BASE
4. EMITTER

NOTE:
DIMENSION D NOT APPLICABLE IN ZONE N.

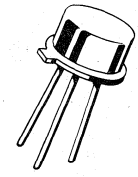
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.44	5.21	0.175	0.205
C	1.90	2.54	0.075	0.100
D	0.84	0.99	0.033	0.039
F	0.20	0.30	0.008	0.012
G	0.76	1.14	0.030	0.045
K	7.24	8.13	0.285	0.320
L	10.54	11.43	0.415	0.450
N	—	1.65	—	0.065

CASE 317-01

MM8000
MM8001

The RF Line

NPN SILICON
AMPLIFIER
TRANSISTORS



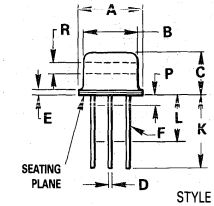
NPN SILICON HIGH-FREQUENCY TRANSISTOR

. . . designed for high-frequency C.A.T.V. amplifier applications. Suitable for use as output driver or pre-driver stages in VHF and UHF equipment.

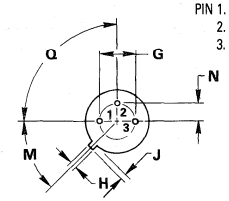
- High Current-Gain—Bandwidth Product —
  f_T = 900 MHz (Min) @ I_C = 50 mAdc (MM8001)
- Low Output Capacitance —
  C_{ob} = 3.5 pF (Max) @ V_{CB} = 30 Vdc
- Low Noise Figure —
  NF = 2.7 dB (Typ) @ I_C = 10 mAdc

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	3.5	Vdc
Collector Current	I_C	0.4	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	3.5 20	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	—	0.500	—
L	6.35	—	0.250	—
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
Q	90° NOM		90° NOM	
R	2.54	—	0.100	—

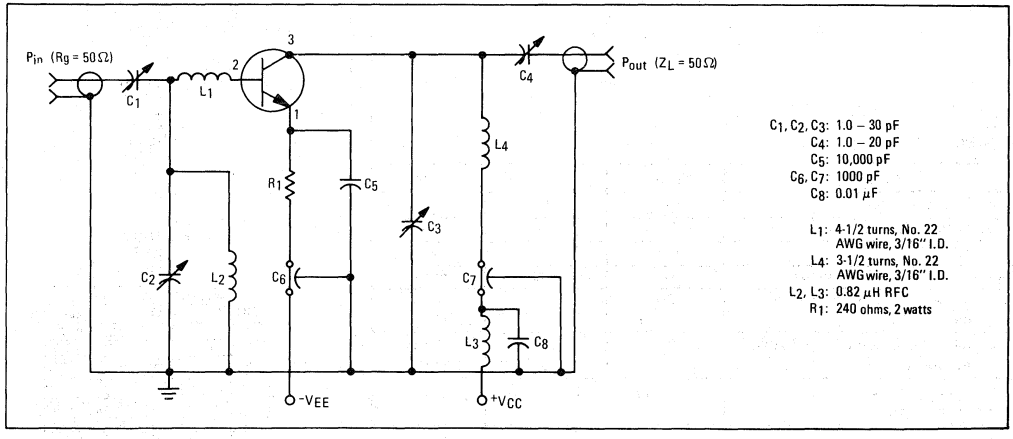
All JEDEC Dimensions and Notes Apply.

CASE 79-02

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (I_C = 5.0 mAdc, I_B = 0)		$V_{(BR)CEO(sus)}$	30	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)		$V_{(BR)CBO}$	40	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)		$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector Cutoff Current (V_{CE} = 28 Vdc, I_B = 0)		I_{CEO}	—	—	20	μAdc
ON CHARACTERISTICS						
DC Current Gain (I_C = 50 mAdc, V_{CE} = 15 Vdc)		h_{FE}	30	—	—	—
DYNAMIC CHARACTERISTICS						
Current-Gain — Bandwidth Product		f_T				MHz
(I_C = 25 mAdc, V_{CE} = 15 Vdc, f = 200 MHz)	MM8000		550	—	—	
	MM8001		700	—	—	
(I_C = 50 mAdc, V_{CE} = 15 Vdc, f = 200 MHz)	MM8000		700	—	—	
	MM8001		900	—	—	
(I_C = 100 mAdc, V_{CE} = 15 Vdc, f = 200 MHz)	MM8000		700	—	—	
	MM8001		900	—	—	
Output Capacitance (V_{CB} = 30 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	—	—	3.5	pF
Noise Figure Figure 1 (I_C = 10 mAdc, V_{CE} = 15 Vdc, f = 200 MHz)		NF	—	2.7	—	dB
FUNCTIONAL TESTS						
Common-Emitter Amplifier Power Gain Figure 1 (I_C = 10 mAdc, V_{CE} = 15 Vdc, f = 200 MHz)		G_{pe}	—	11.4	—	dB

FIGURE 1 – 200 MHz TEST CIRCUIT



MM8009

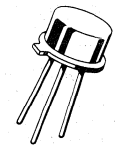
The RF Line

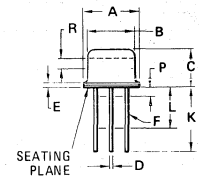
0.9 W – 1.0 GHz
RF POWER
TRANSISTOR
NPN SILICON

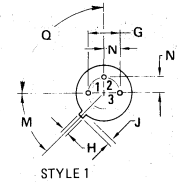
NPN SILICON RF POWER TRANSISTOR

. . . designed for amplifier, frequency multiplier, or oscillator applications in military and industrial equipment. Suitable for use as output, driver, or pre-driver stages in UHF equipment and as a fundamental frequency oscillator at 1.68 GHz.

- High Output Power – P_{out} = 0.9 Watt (Min) @ f = 1.0 GHz
- High Current-Gain–Bandwidth Product – f_T = 1000 MHz (Min) @ I_C = 50 mAdc
- Ideal for Radiosonde Applications – P_{out} (Oscillator) = 300 mW (Typ) @ f = 1.68 GHz







STYLE 1
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO-39

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	35	Vdc
Collector-Base Voltage	V_{CB}	45	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current – Continuous	I_C	400	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 5.71	Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	3.5 20	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	$V_{(BR)CBO}$	45	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	$V_{(BR)EBO}$	3.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, I_B = 0)	I_{CEO}	–	–	100	μAdc
Collector Cutoff Current (V_{CE} = 35 Vdc, V_{BE} = 0)	I_{CES}	–	–	10	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	20	–	–	–
DYNAMIC CHARACTERISTICS					
Current-Gain–Bandwidth Product (I_C = 50 mAdc, V_{CE} = 15 Vdc, f = 100 MHz)	f_T	1000	–	–	MHz
Output Capacitance (V_{CB} = 30 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	2.3	3.0	pF
FUNCTIONAL TEST					
Power Output (Figure 1) (P_{in} = 316 mW, V_{CE} = 28 Vdc, f = 1.0 GHz)	P_{out}	0.9	–	–	Watt
Power Output (Oscillator) (Figure 2) (V_{CE} = 20 Vdc, V_{EB} = 1.5 Vdc, f = 1.68 GHz) (Minimum Efficiency = 15%)	P_{out}	–	0.3	–	Watt
Collector Efficiency (P_{in} = 316 mW, V_{CE} = 28 Vdc, f = 1.0 GHz)	η	35	–	–	%

3

FIGURE 1 – 1.0 GHz POWER AMPLIFIER TEST CIRCUIT

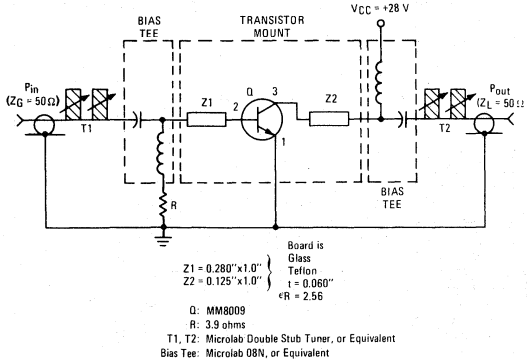


FIGURE 2 – 1.68 GHz POWER OSCILLATOR TEST CIRCUIT

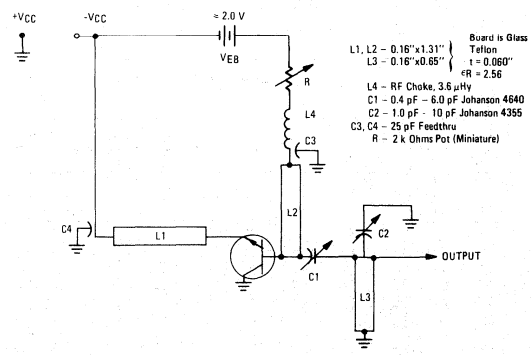


FIGURE 3 – POWER OUTPUT versus POWER INPUT

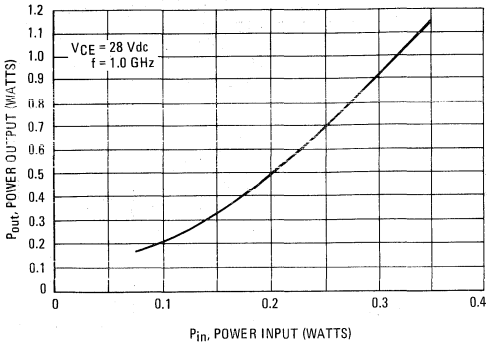


FIGURE 4 – POWER OUTPUT versus FREQUENCY

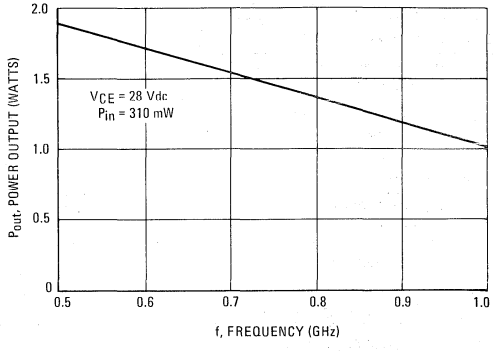


FIGURE 5 – POWER OUTPUT versus VOLTAGE

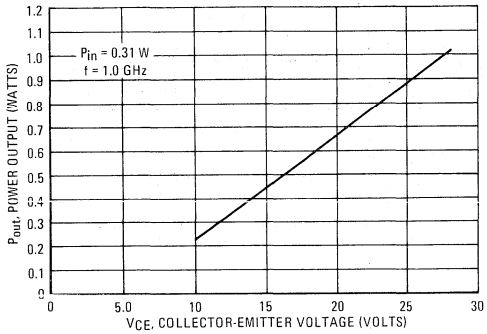


FIGURE 6 – OSCILLATOR POWER OUTPUT versus CURRENT

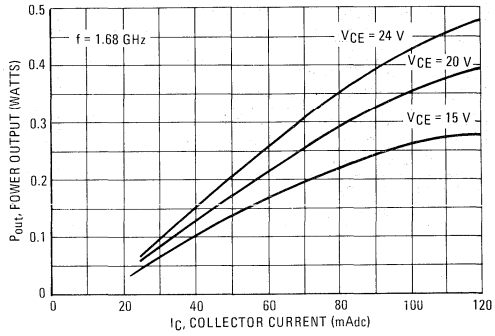


FIGURE 7 – CURRENT-GAIN–BANDWIDTH PRODUCT

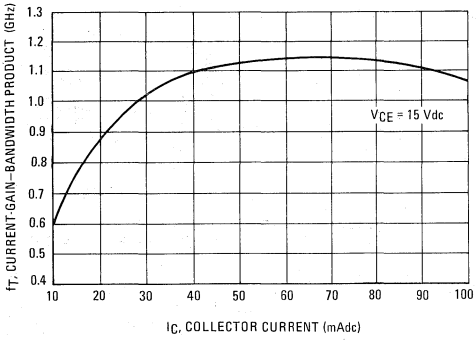
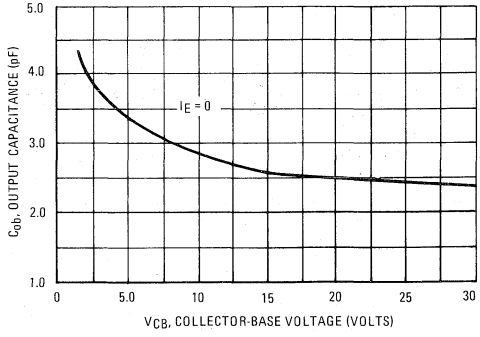


FIGURE 8 – OUTPUT CAPACITANCE versus VOLTAGE

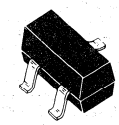


MMBR901

Die Source Same as MRF901

RF AMPLIFIER TRANSISTOR

NPN SILICON



CASE 318-02/03, STYLE 6
SOT-23
(TO-236AA/AB)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CBO}	25	Vdc
Emitter-Base Voltage	V_{EBO}	3.0	Vdc
Collector Current — Continuous	I_C	30	mAdc
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Total Device Dissipation, T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Storage Temperature	T_{stg}	150	°C
*Thermal Resistance Junction to Ambient	$R_{\theta JA}$	357	°C/W

*Package mounted on 99.5% alumina 10 x 8 x 0.6 mm.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

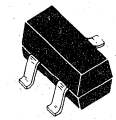
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	15	—	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	25	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	2.0	—	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	—	50	nAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 5.0 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	30	200	—
SMALL-SIGNAL CHARACTERISTICS				
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{obo}	—	1.0	pF
Common-Emitter Amplifier Power Gain (V_{CC} = 6.0 Vdc, I_C = 5.0 mAdc, f = 1.0 GHz)	G_{pe}(1)	16 (Typ)	—	dB
Noise Figure (I_C = 5.0 mAdc, V_{CE} = 6.0 Vdc, f = 1.0 GHz)	NF(1)	—	1.9 (Typ)	dB

(1) Noise figure and power gain measured on the Ailtech 7380 50Ω system.

MMBR920

RF AMPLIFIER/SWITCHING TRANSISTOR

NPN SILICON



CASE 318-02/03, STYLE 6
SOT-23
(TO-236AA/AB)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CBO}	20	Vdc
Emitter-Base Voltage	V_{EBO}	3.0	Vdc
Collector Current — Continuous	I_C	35	mAdc
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Total Device Dissipation, T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Storage Temperature	T_{stg}	150	°C
*Thermal Resistance Junction to Ambient	$R_{\theta JA}$	357	°C/W

*Package mounted on 99.5% alumina 10 x 8 x 0.6 mm.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

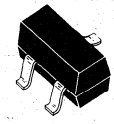
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	15	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	20	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	2.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}	—	—	50	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 14 mAdc, V_{CE} = 10 Vdc)	h_{FE}	25	—	250	—
SMALL SIGNAL CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 14 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz)	f_T	—	4.5	—	GHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	—	—	1.0	pF
Noise Figure (I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz) (I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 GHz)	NF(1)	 — —	 2.4 3.0	 — —	dB
Common-Emitter Amplifier Power Gain (I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz) (I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 GHz)	G_{pe}(1)	 — —	 15 10	 — —	dB

(1) Noise figure and power gain measured on the Ailtech 7380 50 Ω system.

MMBR930

AMPLIFIER/SWITCHING TRANSISTOR

NPN SILICON



CASE 318-02/03, STYLE 6
SOT-23
(TO-236AA/AB)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	12	Vdc
Collector-Base Voltage	V_{CBO}	15	Vdc
Emitter-Base Voltage	V_{EBO}	3.0	Vdc
Collector Current — Continuous	I_C	35	mAdc
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Total Device Dissipation, T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Storage Temperature	T_{stg}	150	°C
*Thermal Resistance Junction to Ambient	$R_{\theta JA}$	357	°C/W

*Package mounted on 99.5% alumina 10 x 8 x 0.6 mm.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	12	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	15	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 5.0 Vdc, I_E = 0)	I_{CBO}	—	—	50	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 30 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	25	—	250	—
SMALL-SIGNAL CHARACTERISTICS					
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	—	—	1.0	pF
Noise Figure (I_C = 2.0 mAdc, V_{CE} = 5.0 Vdc, f = 0.5 GHz) (I_C = 2.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 GHz)	NF(1)	 — —	 1.9 2.5	 — —	dB
Common-Emitter Amplifier Power Gain (I_C = 2.0 mAdc, V_{CE} = 5.0 Vdc, f = 0.5 GHz) (I_C = 2.0 mAdc, V_{CE} = 5.0 Vdc, f = 0.5 GHz)	G_{pe}(1)	 — —	 11 8.0	 — —	dB

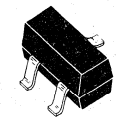
(1) Noise figure and power gain measured on the Ailtech 7380 50 Ω system.

MMBR931

Die Source Same as MRF931

RF AMPLIFIER TRANSISTOR

NPN SILICON



CASE 318-02/03, STYLE 6
SOT-23
(TO-236AA/AB)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	5.0	Vdc
Collector-Base Voltage	V_{CBO}	10	Vdc
Emitter-Base Voltage	V_{EBO}	2.0	Vdc
Collector Current — Continuous	I_C	5.0	mAdc
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Total Device Dissipation, T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Storage Temperature	T_{stg}	150	°C
*Thermal Resistance Junction to Ambient	$R_{\theta JA}$	357	°C/W

*Package mounted on 99.5% alumina 10 x 8 x 0.6 mm.

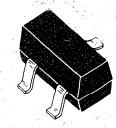
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 0.1 mAdc, I_B = 0)	$V_{(BR)CEO}$	5.0	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 0.01 mAdc, I_E = 0)	$V_{(BR)CBO}$	10	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	2.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 5.0 Vdc, I_E = 0)	I_{CBO}	—	—	50	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 0.25 mAdc, V_{CE} = 1.0 Vdc)	h_{FE}	30	—	150	—
SMALL-SIGNAL CHARACTERISTICS					
Collector-Base Capacitance (V_{CB} = 1.0 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	—	—	0.5	pF
Noise Figure (I_E = 0.25 mAdc, V_{CE} = 1.0 Vdc, f = 1.0 GHz)	NF(1)	—	4.3	—	dB
Gate Power Dissipation (I_E = 0.25 mAdc, V_{CE} = 1.0 Vdc, f = 1.0 GHz)	PG(1)	—	10	—	—

(1) Noise figure and power gain measured on the Ailtech 7380 50 Ω system.

MMBR2060

RF AMPLIFIER TRANSISTOR
NPN SILICON



CASE 318-02/03, STYLE 6
SOT-23
(TO-236AA/AB)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	14	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	50	mAdc
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Total Device Dissipation, T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Storage Temperature	T_{stg}	150	°C
*Thermal Resistance Junction to Ambient	$R_{\theta JA}$	357	°C/W

*Package mounted on 99.5% alumina 10 x 8 x 0.6 mm.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

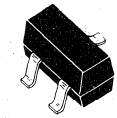
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	14	—	Vdc
Collector Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}	—	50	nAdc
Emitter Cutoff Current (V_{EB} = 4.0, I_C = 0)	I_{EBO}	—	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 5.0 mAdc, V_{CE} = 5.0 Vdc) (I_C = 20 mAdc, V_{CE} = 10 Vdc, f = 500 MHz)	h_{FE}	 20 2.0	 — —	—
Collector-Emitter Saturation Voltage (I_C = 80 mAdc, I_B = 8.0 mAdc)	$V_{CE(sat)}$	—	0.38	Vdc
Base-Emitter Saturation Voltage (I_C = 40 mAdc, I_B = 20 mAdc)	$V_{BE(sat)}$	—	0.98	Vdc
SMALL-SIGNAL CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 20 mAdc, V_{CE} = 1.0 Vdc, f = 100 MHz)	f_T	—	1.0	GHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0)	C_{cb}	—	1.0	pF
Emitter-Base Capacitance (V_{EB} = 0.5 Vdc, I_C = 0)	C_{eb}	—	3.0	pF
Noise Figure (V_{CE} = 10 Vdc, I_E = 1.5 mAdc, f = 450 MHz)	NF(1)	—	3.5	dB
Common-Emitter Amplifier Power Gain (V_{CE} = 10 Vdc, I_E = 1.5 mAdc, f = 450 Mhz)	G_{pe}(1)	12.5	—	dB

(1) Noise figure and power gain measured on the Ailtech 7380 50 Ω system.

MMBR2857

Die Source Same as 2N2857

RF TRANSISTOR
NPN SILICON



CASE 318-02/03, STYLE 6
SOT-23
(TO-236AA/AB)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CBO}	30	Vdc
Emitter-Base Voltage	V_{EBO}	2.5	Vdc
Collector Current — Continuous	I_C	40	mAdc
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Total Device Dissipation, T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Storage Temperature	T_{stg}	150	°C
*Thermal Resistance Junction to Ambient	$R_{\theta JA}$	357	°C/W

*Package mounted on 99.5% alumina 10 x 8 x 0.6 mm.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

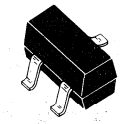
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 3.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	15	—	Vdc
Collector-Base Breakdown Voltage (I_C = 1.0 μAdc, I_E = 0)	$V_{(BR)CBO}$	30	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	$V_{(BR)EBO}$	2.5	—	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	—	0.05	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 3.0 mAdc, V_{CE} = 1.0 Vdc)	h_{FE}	30	—	—
SMALL-SIGNAL CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 4.0 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	1000	—	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{cb}	—	1.0	pF
Small-Signal Current Gain (I_C = 2.0 mAdc, V_{CE} = 6.0 Vdc, f = 1.0 kHz)	h_{fe}	50	—	—
Noise Figure (I_C = 1.5 mAdc, V_{CE} = 6.0 Vdc, R_S = 50 Ω, f = 450 MHz)	NF	—	4.5	dB
Common-Emitter Amplifier Power Gain (I_C = 1.5 mAdc, V_{CE} = 6.0 Vdc, f = 450 MHz)	G_{PE}	12.5	—	dB

MMBR4957

Die Source Same as 2N4957

RF AMPLIFIER TRANSISTOR

PNP SILICON



CASE 318-02/03, STYLE 6
SOT-23
(TO-236AA/AB)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	30	Vdc
Emitter-Base Voltage	V_{EBO}	3.0	Vdc
Collector Current — Continuous	I_C	30	mAdc
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Total Device Dissipation, T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Storage Temperature	T_{stg}	150	°C
*Thermal Resistance Junction to Ambient	$R_{\theta JA}$	357	°C/W

*Package mounted on 99.5% alumina 10 x 8 x 0.6 mm.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	—	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	$V_{(BR)CBO}$	30	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	$V_{(BR)EBO}$	3.0	—	Vdc
Collector Cutoff Current (V_{CB} = 10 Vdc, I_C = 0)	I_{CBO}	—	0.1	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 2.0 mAdc, V_{CE} = 10 Vdc)	h_{FE}	20	150	—
SMALL-SIGNAL CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_E = 2.0 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	1,200	—	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	—	0.8	pF
Common-Emitter Amplifier Power Gain(1) (V_{CE} = 10 Vdc, I_C = 2.0 mAdc, f = 450 MHz)	G_{pe}	17 (Typ)	—	dB
Noise Figure(1) (I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 450 MHz)	NF	—	3.0 (Typ)	dB

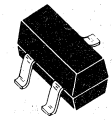
(1) Noise figure and power gain measured on the Ailtech 7380 50 Ω system.

MMBR5031

Die Source Same as 2N5031

RF AMPLIFIER TRANSISTOR

NPN SILICON



CASE 318-02/03, STYLE 6
SOT-23
(TO-236AA/AB)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	10	Vdc
Collector-Base Voltage	V_{CBO}	15	Vdc
Emitter-Base Voltage	V_{EBO}	3.0	Vdc
Collector Current — Continuous	I_C	20	mAdc
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Total Device Dissipation, T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Storage Temperature	T_{stg}	150	°C
*Thermal Resistance Junction to Ambient	$R_{\theta JA}$	357	°C/W

*Package mounted on 99.5% alumina 10 x 8 x 0.6 mm.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	10	—	Vdc
Collector-Base Breakdown Voltage (I_C = 0.01 mAdc, I_E = 0)	$V_{(BR)CBO}$	15	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.01 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.0	—	Vdc
Collector Cutoff Current (V_{CB} = 6.0 Vdc, I_E = 0)	I_{CBO}	—	10	nAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 1.0 mAdc, V_{CE} = 6.0 Vdc)	h_{FE}	25	300	—
SMALL-SIGNAL CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 5.0 mAdc, V_{CE} = 6.0 Vdc, f = 100 MHz)	f_T	1,000	—	MHz
Collector-Base Capacitance (V_{CE} = 6.0 Vdc, I_E = 0, f = 0.1 MHz)	C_{cb}	—	1.5	pF
Noise Figure (I_C = 1.0 mAdc, V_{CE} = 6.0 Vdc, f = 450 MHz)	NF(1)	—	2.5	dB
Common-Emitter Amplifier Power Gain (I_C = 1.0 mAdc, V_{CE} = 6.0 Vdc, f = 450 MHz)	G_{pe}(1)	14	25	dB

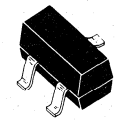
(1) Noise figure and power gain measure on Ailtech 7380 50 Ω system.

MMBR5179

Die Source Same as 2N5179

RF AMPLIFIER TRANSISTOR

NPN SILICON



CASE 318-02/03, STYLE 6
SOT-23
(TO-236AA/AB)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	12	Vdc
Collector-Base Voltage	V_{CBO}	20	Vdc
Emitter-Base Voltage	V_{EBO}	2.5	Vdc
Collector Current — Continuous	I_C	50	mAdc
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Total Device Dissipation, T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Storage Temperature	T_{stg}	150	°C
*Thermal Resistance Junction to Ambient	$R_{\theta JA}$	357	°C/W

*Package mounted on 99.5% alumina 10 x 8 x 0.6 mm.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 3.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	12	—	Vdc
Collector-Base Breakdown Voltage (I_C = 0.01 mAdc, I_E = 0)	$V_{(BR)CBO}$	20	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.01 mAdc, I_C = 0)	$V_{(BR)EBO}$	2.5	—	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	—	0.02	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 3.0 mAdc, V_{CE} = 1.0 Vdc)	h_{FE}	25	—	—
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{CE(sat)}$	—	0.4	Vdc
Base-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{BE(sat)}$	—	1.0	Vdc
SMALL SIGNAL CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 5.0 mAdc, V_{CE} = 6.0 Vdc, f = 100 MHz)	f_T	900	—	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 to 1.0 MHz)	C_{cb}	—	1.0	pF
Small Signal Current Gain (I_C = 2.0 mAdc, V_{CE} = 6.0 Vdc, f = 1.0 kHz)	h_{fe}	25	—	—
Noise Figure (I_C = 1.5 mAdc, V_{CE} = 6.0 Vdc, R_S = 50 Ω, f = 200 Mhz)	NF(1)	—	4.5	dB
Common-Emitter Amplifier Power Gain (V_{CE} = 6.0 Vdc, I_C = 5.0 mAdc, f = 200 MHz)	G_{pe}(1)	15	—	dB

(1) Noise figure and power gain measured on the Ailtech 7380 50 Ω system.

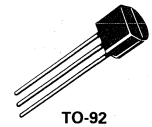
PNP Silicon High Frequency Transistors

MPS536
MMBR536

LOW NOISE
HIGH RF GAIN

. . . this high current gain-bandwidth transistor makes an excellent RF amplifier and oscillator. It is available in the surface mount SOT-23 as well as the popular TO-92 low cost plastic packages.

- High Current Gain-Bandwidth Product
  f_T = 5.5 GHz (typ) @ I_C = 20 mA — MMBR536
  f_T = 4.5 GHz (typ) @ I_C = 20 mA MPS536
- High Gain
  G_{NF} = 14 dB (typ) @ 10 mA/500 MHz
- Low Collector-Base Capacitance
  C_{cb} = 0.8 pF (typ) @ V_{CB} = 5 Vdc
- Tape and Reel Packaging Options



TO-92
CASE 29-02
MPS536



SOT-23
CASE 318
MMBR536
Standard and Low Profile

3

MAXIMUM RATINGS

Rating	Symbol	MPS536	MMBR536	Unit
Collector-Emitter Voltage	V_{CEO}	10	10	Vdc
Collector-Base Voltage	V_{CBO}	15	15	Vdc
Emitter-Base Voltage	V_{EBO}	4.5	4.5	Vdc
Collector Current — Continuous	I_C	30	30	mA
Power Dissipation @ T_A = 25°C Derate Above 25°C	P_D	625 5	200* 1.6	mW mW/°C
Storage Temperature	T_{stg}	−65 to +150	−65 to +150	°C

*Free air

ELECTRICAL CHARACTERISTICS (T_C = 25°C *For both package types unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 2 mA, I_B = 0)	$V_{(BR)CEO}$	10	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μA, I_E = 0)	$V_{(BR)CBO}$	15	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μA, I_C = 0)	$V_{(BR)EBO}$	4.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}	—	—	10	nAdc

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C *For both package types unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS						
DC Current Gain (I_C = 20 mA, V_{CE} = 5 V)		h_{FE}	20	—	200	—
DYNAMIC CHARACTERISTICS						
Current Gain-Bandwidth Product (I_C = 20 mAdc, V_{CE} = 5 Vdc, f = 1 GHz)	MPS536	f_T	—	4.5	—	GHz
	MMBR536		—	5.5	—	
Collector-Base Capacitance (V_{CB} = 5 Vdc, I_F = 0, f = 1 MHz)		C_{cb}	—	0.8	1.2	pF
FUNCTIONAL TESTS						
Gain @ Noise Figure (I_C = 10 mAdc, V_{CE} = 5 Vdc)	f = 500 MHz	G_{NF}	—	14	—	dB
	f = 1 GHz		—	8	—	
Noise Figure (I_C = 10 mAdc, V_{CE} = 5 Vdc)	f = 500 MHz	NF	—	4.5	—	dB
	f = 1 GHz		—	6	—	

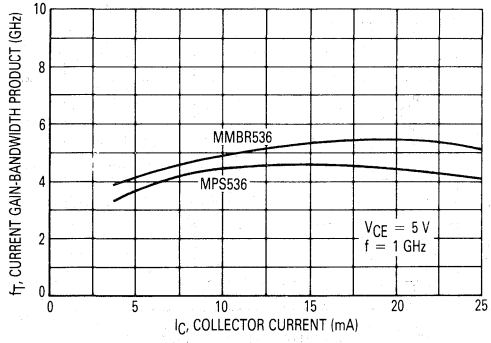


Figure 1. Current Gain-Bandwidth Product versus Collector Current

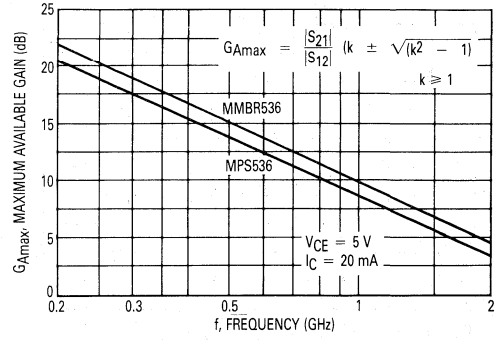


Figure 2. Maximum Available Gain (G_{Amax}) versus Frequency

TO-92 MPS536

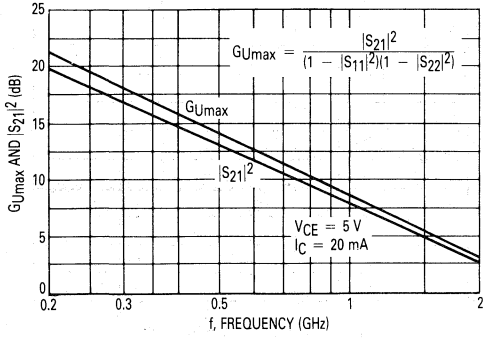


Figure 3. Maximum Unilateral Gain (G_{Umax}) and Insertion Gain ($|S_{21}|^2$) versus Frequency

SOT-23 MMBR536

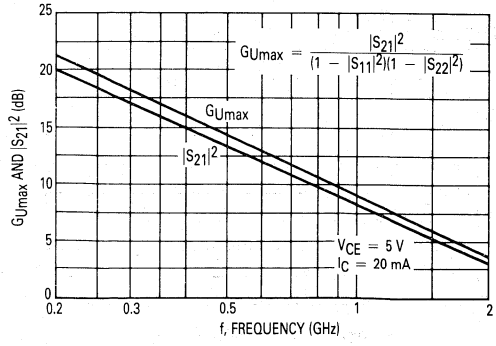


Figure 4. Maximum Unilateral Gain (G_{Umax}) and Insertion Gain ($|S_{21}|^2$) versus Frequency

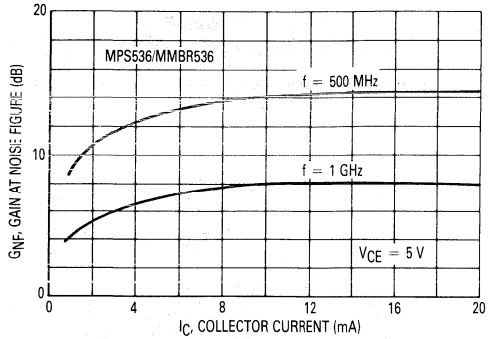


Figure 5. Gain at Noise Figure versus Collector Current

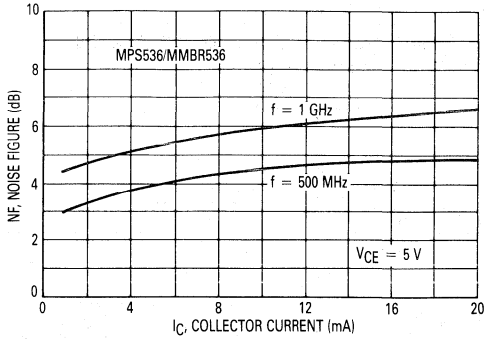


Figure 6. Noise Figure versus Collector Current

MPS536

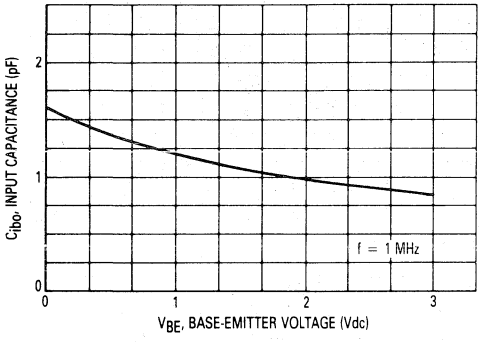


Figure 7. Input Capacitance versus Emitter-Base Voltage

MPS536

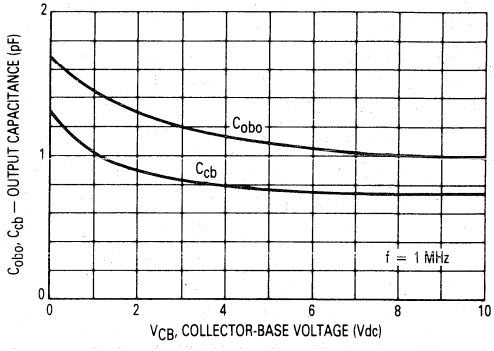


Figure 8. Output Capacitance versus Collector-Base Voltage

MMBR536

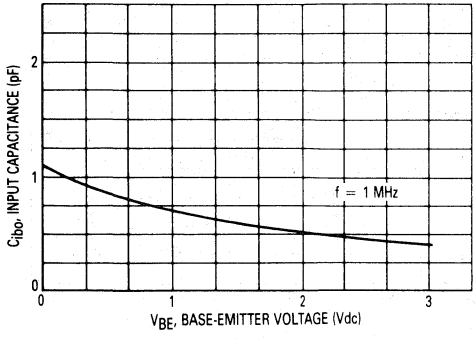


Figure 9. Input Capacitance versus Emitter-Base Voltage

MMBR536

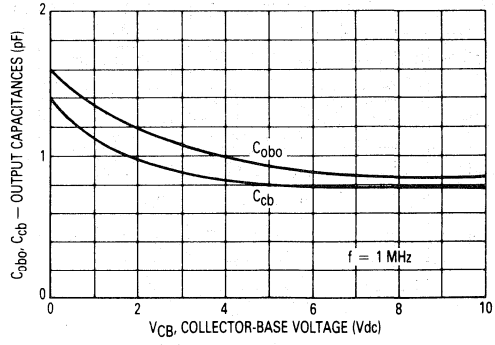
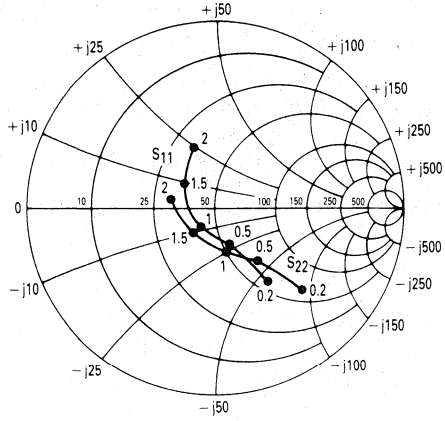


Figure 10. Output Capacitance versus Collector-Base Voltage

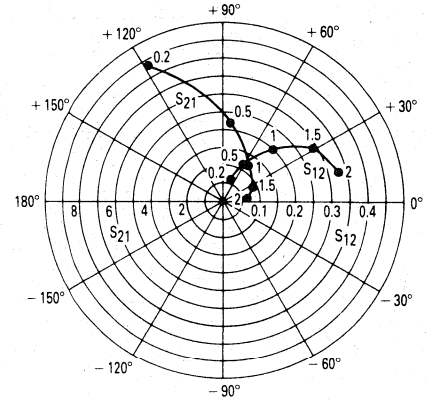
MPS536

INPUT/OUTPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{CE} = 10 V, I_C = 10 mA



MPS536

FORWARD/REVERSE TRANSMISSION COEFFICIENTS versus FREQUENCY
V_{CE} = 10 V, I_C = 10 mA



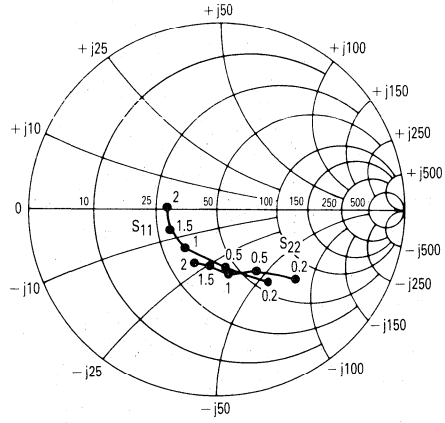
3

MPS536
COMMON EMITTER S-PARAMETERS

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
10	5	200	0.60	−43	6.60	125	0.07	68	0.71	−35
		500	0.30	−60	3.64	87	0.14	57	0.47	−43
		1000	0.17	−103	2.11	56	0.22	43	0.32	−69
		1500	0.15	156	1.70	28	0.30	28	0.22	−112
		2000	0.28	110	1.29	2	0.33	13	0.25	−174
	10	200	0.48	−52	8.78	118	0.06	69	0.62	−42
		500	0.21	−66	4.31	84	0.12	60	0.37	−46
		1000	0.12	−122	2.40	54	0.20	47	0.24	−73
		1500	0.18	138	1.90	29	0.29	31	0.16	−126
		2000	0.32	104	1.41	4	0.33	16	0.23	170
	20	200	0.38	−59	10.21	112	0.06	70	0.54	−46
		500	0.14	−76	4.72	81	0.12	63	0.30	−47
		1000	0.11	−144	2.58	53	0.20	49	0.19	−74
		1500	0.22	132	1.99	28	0.29	34	0.12	−139
		2000	0.35	103	1.46	4	0.33	19	0.22	161

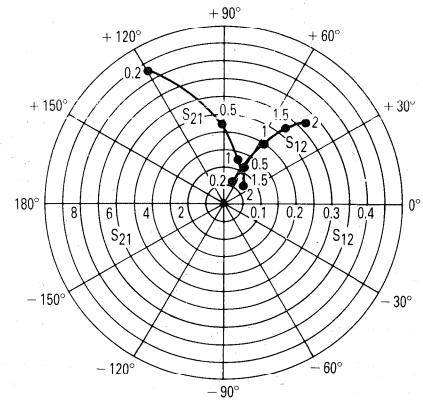
MMBR536

INPUT/OUTPUT REFLECTION COEFFICIENTS
versus
FREQUENCY
V_{CE} = 10 V, I_C = 10 mA



MMBR536

FORWARD AND REVERSE TRANSMISSION COEFFICIENTS
versus
FREQUENCY
V_{CE} = 10 V, I_C = 10 mA

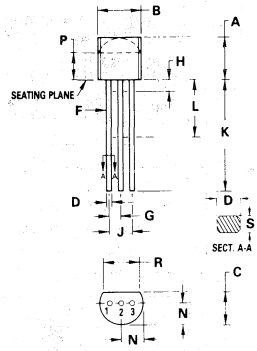


3

MMBR536
COMMON EMITTER S-PARAMETERS

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
10	5	200	0.60	−44	6.47	126	0.07	66	0.68	−35
		500	0.37	−70	3.57	97	0.14	60	0.48	−50
		1000	0.27	−105	2.16	74	0.22	53	0.40	−69
		1500	0.24	−138	1.62	58	0.29	46	0.37	−87
		2000	0.22	−166	1.38	44	0.33	42	0.34	−103
	10	200	0.48	−54	8.65	120	0.06	66	0.58	−40
		500	0.30	−82	4.32	94	0.12	62	0.38	−58
		1000	0.24	−122	2.52	74	0.20	57	0.32	−78
		1500	0.24	−155	1.84	59	0.27	51	0.30	−96
		2000	0.24	178	1.54	46	0.32	47	0.28	−112
	20	200	0.39	−63	10.10	115	0.06	67	0.49	−50
		500	0.25	−94	4.77	91	0.11	65	0.32	−65
		1000	0.24	−136	2.72	73	0.19	60	0.27	−84
		1500	0.24	−167	1.96	58	0.26	54	0.26	−102
		2000	0.26	168	1.63	46	0.32	50	0.25	−119

OUTLINE DIMENSIONS



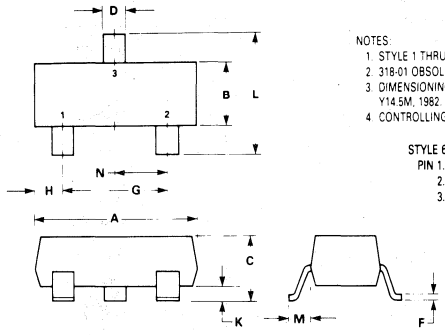
NOTES:
1. CONTOUR OF PACKAGE BEYOND ZONE "P" IS UNCONTROLLED.
2. DIM "F" APPLIES BETWEEN "H" AND "L". DIM. "D" & "S" APPLIES BETWEEN "L" & 12.70 mm (0.5") FROM SEATING PLANE. LEAD DIM IS UNCONTROLLED IN "H" & BEYOND 12.70 mm (0.5") FROM SEATING PLANE.

All JEDEC dimensions and notes apply

STYLE 2:
PIN 1. BASE
2. EMMITTER
3. COLLECTOR

TO-92
CASE 29-02
TO-226AA
PLASTIC

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	—	2.54	—	0.100
J	2.41	2.67	0.095	0.105
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.03	2.67	0.080	0.105
P	2.92	—	0.115	—
R	3.43	—	0.135	—
S	0.36	0.41	0.014	0.016

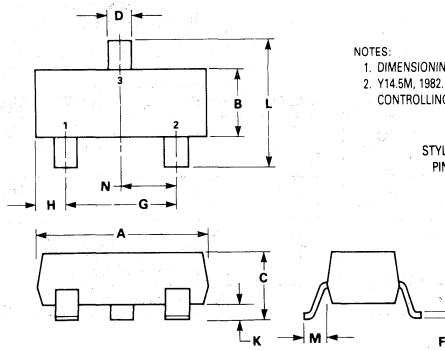


NOTES:
1. STYLE 1 THRU 5 OBSOLETE
2. 318-01 OBSOLETE, NEW STD 318-02.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: MILLIMETERS.

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

SOT-23
CASE 318-02
TO-236AA
Standard

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.85	1.20	0.033	0.0472
D	0.37	0.46	0.0150	0.0177
F	0.085	0.130	0.0034	0.0051
G	1.78	2.04	0.0701	0.0807
H	0.51	0.60	0.0200	0.0236
K	0.10	0.25	0.0040	0.0098
L	2.10	2.50	0.0830	0.0984
M	0.45	0.60	0.0180	0.0236
N	0.89	1.02	0.0350	0.0401



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
CONTROLLING DIMENSION: MILLIMETERS.

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

SOT-23
CASE 318-03
TO-236AB
Low Profile

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.89	1.11	0.035	0.044
D	0.37	0.46	0.015	0.0177
F	0.085	0.130	0.0034	0.0051
G	1.78	2.04	0.0701	0.0807
H	0.51	0.60	0.0200	0.0236
K	0.013	0.100	0.0005	0.0040
L	2.10	2.50	0.0830	0.0984
M	0.45	0.60	0.018	0.0236
N	0.89	1.02	0.0350	0.0401

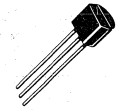
NPN Silicon High Frequency Transistors

MPS571
MXR571
MMBR571

LOW NOISE
HIGH RF GAIN

. . . designed for low noise, wide dynamic range front-end amplifiers and low-noise VCO's. Available in two surface-mountable plastic package styles, as well as the popular TO-92 package. This Motorola series of small-signal plastic transistors offers superior quality and performance at low cost.

- High Gain-Bandwidth Product
  f_T = 8 GHz (Typ) @ 50 mA
- Low Noise Figure
  NF = 2 dB (Typ) @ 500 MHz
- High Gain
  G_{NF} = 17 dB (Typ) @ 30 mA/500 MHz
- State-of-the-Art Technology
  Fine Line Geometry
  Ion-Implanted Arsenic Emitters
  Gold Top Metallization and Wires
  Silicon Nitride Passivation
- Tape and Reel Packaging Options
- MMBR571 Available in Low Profile, Add L Suffix



TO-92
CASE 29
MPS571



SOT-89
CASE 345
MXR571



SOT-23
CASE 318
MMBR571
Standard and Low Profile

3

MAXIMUM RATINGS

Ratings	Symbol	MPS571	MXR571	MMBR571	Unit
Collector-Emitter Voltage	V_{CEO}	10			Vdc
Collector-Base Voltage	V_{CBO}	20			Vdc
Emitter-Base Voltage	V_{EBO}	3			Vdc
Collector Current — Continuous	I_C	80			mA
Power Dissipation @ T_A = 25°C	P_D	625	400 (Free Air)	200 (Free Air)	mW
Storage Temperature	T_{stg}	−55 to +150			°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Collector-Emitter Breakdown Voltage (I_C = 0.1 mAdc, I_B = 0)			$V_{(BR)CEO}$	10	12	—	Vdc
Collector-Base Breakdown Voltage (I_C = 1 mAdc, I_E = 0)			$V_{(BR)CBO}$	20	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 50 μAdc, I_C = 0)			$V_{(BR)EBO}$	2.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 8 Vdc, I_E = 0)			I_{CBO}	—	—	10	μAdc
ON CHARACTERISTICS							
DC Current Gain (I_C = 30 mAdc, V_{CE} = 5 Vdc)			h_{FE}	50	—	300	—
DYNAMIC CHARACTERISTICS							
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)			C_{cb}	—	0.7	1	pF
Current Gain-Bandwidth Product (V_{CE} = 5 Vdc, I_C = 50 mAdc, f = 1 GHz)	MPS571		f_T	—	6	—	GHz
	MXR571			—	7	—	
	MMBR571			—	8	—	
FUNCTIONAL TESTS							
Gain @ Noise Figure (I_C = 10 mAdc, V_{CE} = 5 Vdc)	MPS571	f = 0.5 GHz	G_{NF}	—	14	—	dB
		f = 1 GHz		—	9	—	
	MXR571	f = 0.5 GHz		—	15	—	
		f = 1 GHz		—	9.5	—	
	MMBR571	f = 0.5 GHz		—	16.5	—	
		f = 1 GHz		—	10.5	—	
Noise Figure (I_C = 10 mAdc, V_{CE} = 5 Vdc)	MPS571	f = 0.5 GHz	NF	—	2	—	dB
		f = 1 GHz		—	2.6	—	
	MXR571	f = 0.5 GHz		—	2.1	—	
		f = 1 GHz		—	2.7	—	
	MMBR571	f = 0.5 GHz		—	2	—	
		f = 1 GHz		—	2.6	—	

Figure 1. Maximum Available Gain versus Frequency

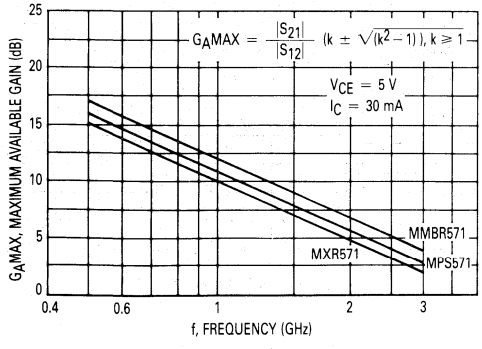


Figure 2. Current Gain-Bandwidth versus Collector Current @ 1 GHz

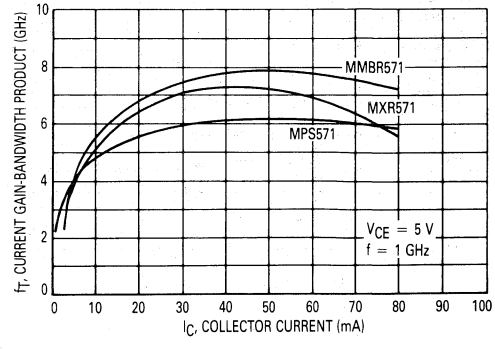
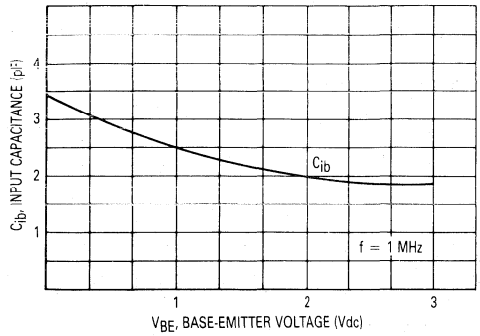
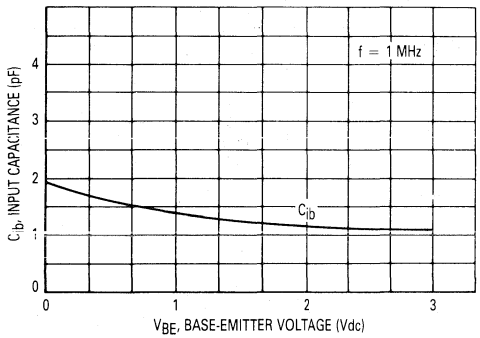


Figure 3. Input Capacitance versus Emitter Base Voltage

(a) TO-92 MPS571



(b) SOT-89 MXR571



(c) SOT-23 MMBR571

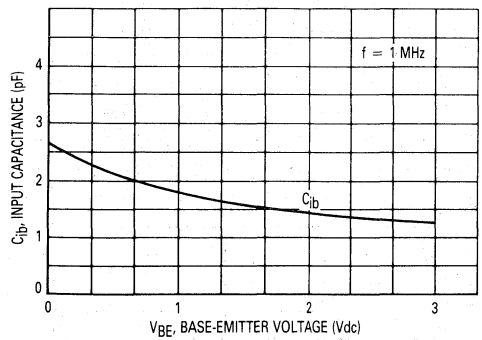
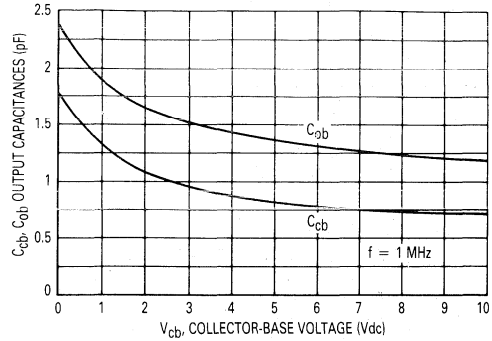
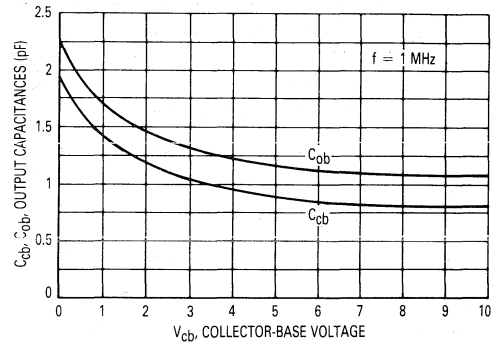


Figure 4. Output Capacitances versus Collector-Base Voltage

(a) TO-92 MPS571



(b) SOT-89 MXR571



(c) SOT-23 MMBR571

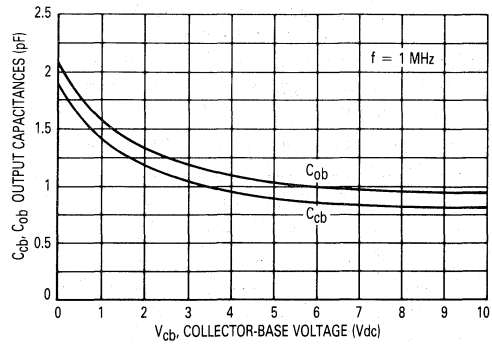
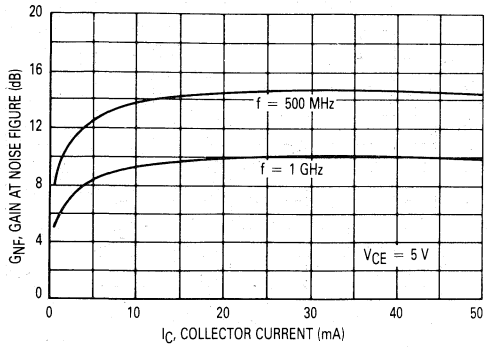
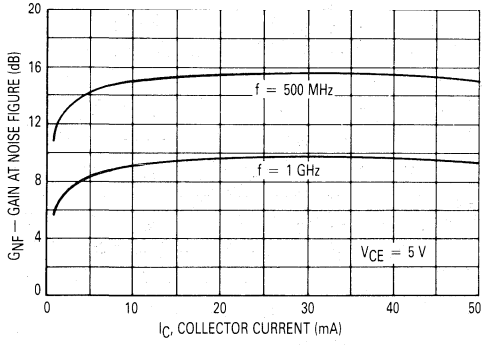


Figure 5. Gain at Noise Figure versus Collector Current

(a) TO-92 MPS571



(b) SOT-89 MXR571



(c) SOT-23 MMBR571

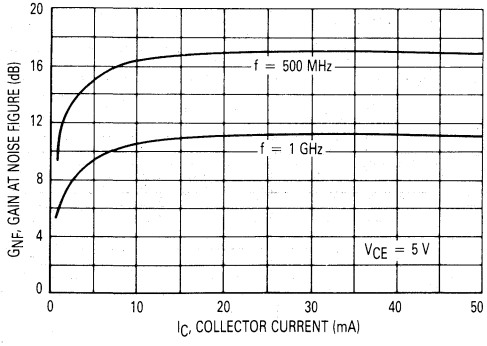
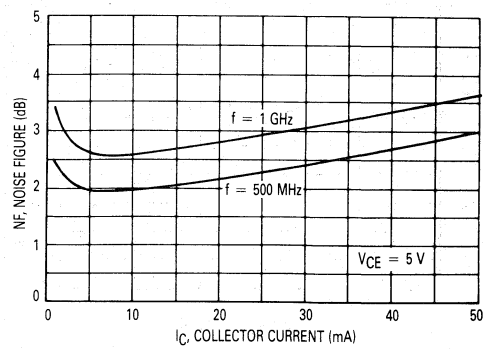
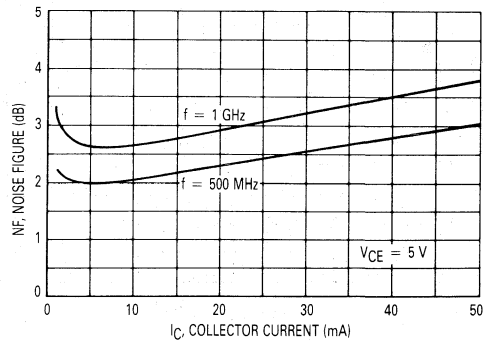


Figure 6. Noise Figure versus Collector Current

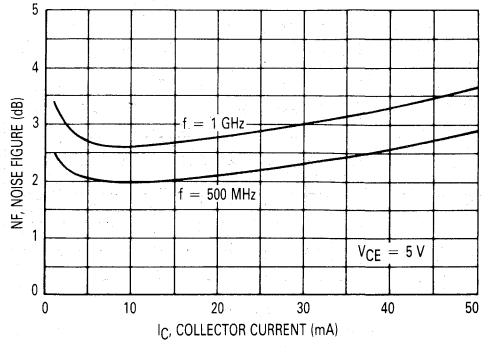
(a) TO-92 MPS571



(b) SOT-89 MXR571



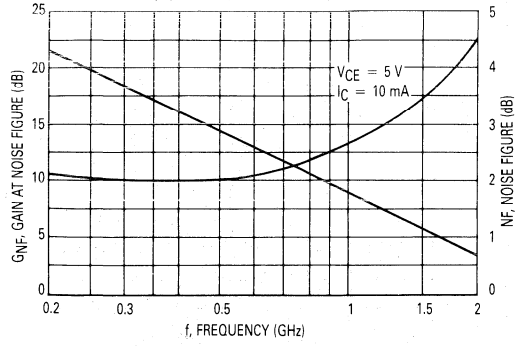
(c) SOT-23 MMBR571



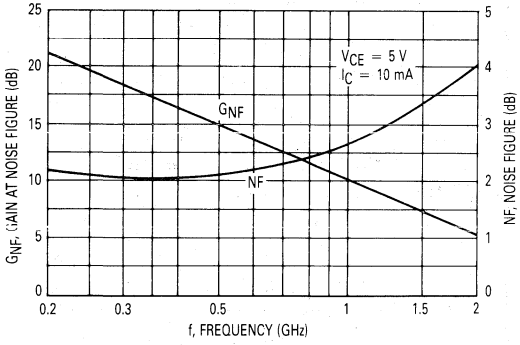
3

Figure 7. Gain at Noise Figure and Noise Figure versus Frequency

(a) TO-92 MPS571



(b) SOT-89 MXR571



(c) SOT-23 MMBR571

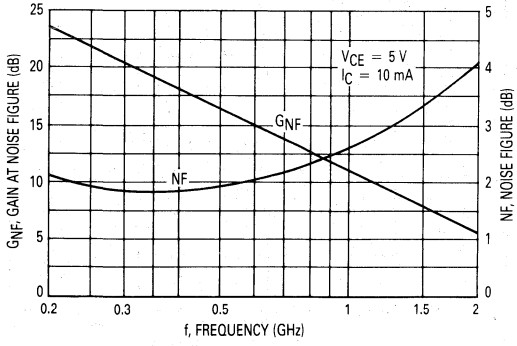
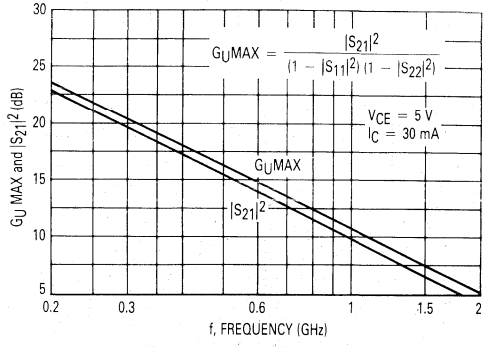
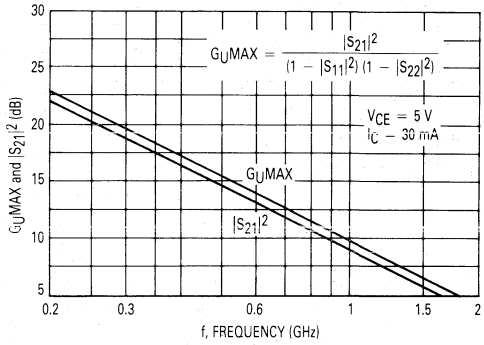


Figure 8. Maximum Unilateral Gain and Insertion Gain versus Frequency

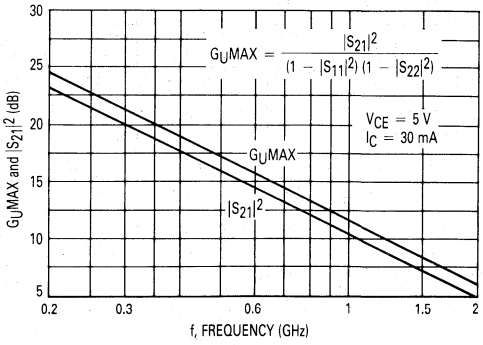
(a) TO-92 MPS571



(b) SOT-89 MXR571



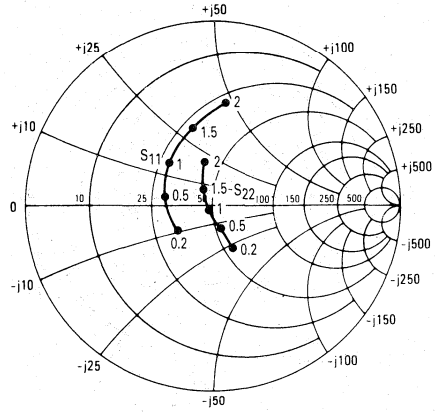
(c) SOT-23 MMBR571



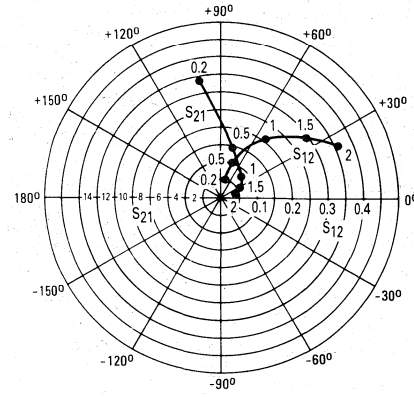
3

TO-92 MPS571

INPUT/OUTPUT REFLECTION COEFFICIENTS versus FREQUENCY
V_{CE} = 5 V, I_C = 30 mA



FORWARD/REVERSE TRANSMISSION COEFFICIENTS versus FREQUENCY
V_{CE} = 5 V, I_C = 30 mA



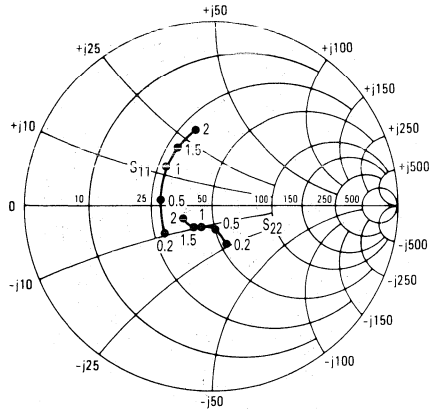
3

COMMON EMITTER S-PARAMETERS

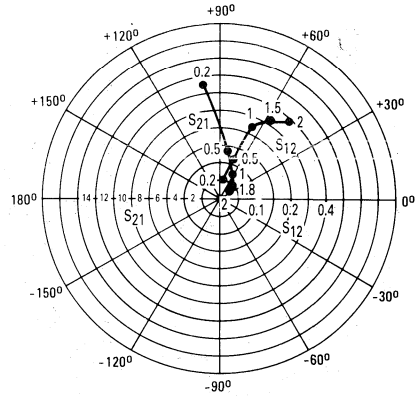
V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
5	5	200	0.62	−80	8.22	122	0.07	56	0.63	−44
		500	0.40	−148	4.52	87	0.11	50	0.36	−58
		1000	0.39	155	2.51	54	0.16	48	0.23	−78
		1500	0.46	122	1.86	32	0.23	42	0.15	−114
		2000	0.59	100	1.50	14	0.31	33	0.14	173
	15	200	0.33	−121	12.88	105	0.05	67	0.37	−59
		500	0.28	−175	5.62	79	0.10	65	0.18	−67
		1000	0.32	143	2.99	53	0.19	55	0.08	−94
		1500	0.40	117	2.14	32	0.27	42	0.07	171
		2000	0.55	95	1.74	17	0.35	30	0.198	117
	30	200	0.23	−143	13.65	99	0.05	75	0.26	−62
		500	0.23	169	5.75	76	0.11	70	0.13	−68
		1000	0.30	130	3.05	50	0.21	55	0.04	−136
		1500	0.41	106	2.11	28	0.29	38	0.12	130
		2000	0.56	85	1.70	11	0.36	23	0.26	102
	50	200	0.21	−158	13.96	96	0.05	79	0.21	−61
		500	0.23	162	5.82	75	0.11	72	0.11	−66
		1000	0.30	128	3.09	49	0.21	56	0.03	−149
		1500	0.41	105	2.11	28	0.29	39	0.12	127
		2000	0.56	84	1.70	11	0.36	23	0.27	100

SOT-89 MXR571

INPUT/OUTPUT REFLECTION COEFFICIENTS
versus FREQUENCY
V_{CE} = 5 V, I_C = 30 mA



FORWARD/REVERSE TRANSMISSION
COEFFICIENTS versus FREQUENCY
V_{CE} = 5 V, I_C = 30 mA



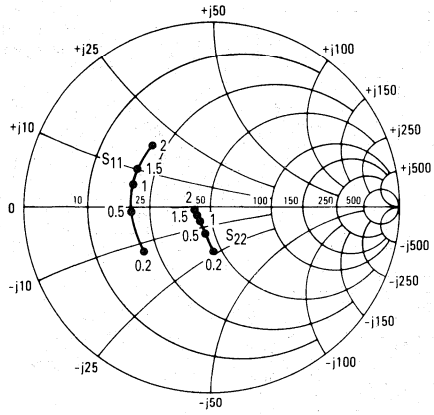
3

COMMON EMITTER S-PARAMETERS

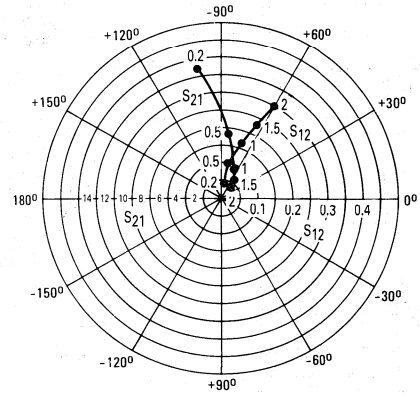
V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
5	5	200	0.60	−84	7.94	120	0.08	56	0.58	−45
		500	0.39	−152	4.17	86	0.11	54	0.34	−56
		1000	0.39	161	2.32	62	0.19	58	0.27	−71
		1500	0.44	132	1.64	45	0.26	55	0.25	−90
		2000	0.49	106	1.33	31	0.32	52	0.26	−106
	15	200	0.33	−126	11.89	101	0.06	67	0.32	−63
		500	0.29	−178	5.13	81	0.11	69	0.18	−73
		1000	0.33	148	2.75	62	0.22	65	0.15	−99
		1500	0.37	123	1.93	47	0.30	56	0.16	−118
		2000	0.42	100	1.55	34	0.37	49	0.17	−139
	30	200	0.28	−149	12.74	97	0.05	74	0.23	−69
		500	0.27	174	5.37	79	0.11	73	0.13	−82
		1000	0.32	144	2.85	62	0.22	66	0.13	−112
		1500	0.36	120	2.02	47	0.31	57	0.15	−132
		2000	0.40	98	1.62	35	0.38	49	0.17	−152
	50	200	0.26	−162	13.03	94	0.05	77	0.18	−71
		500	0.27	169	5.43	79	0.12	75	0.11	−85
		1000	0.32	142	2.88	62	0.22	67	0.12	−117
		1500	0.36	119	2.02	47	0.31	57	0.15	−137
		2000	0.40	97	1.60	35	0.38	49	0.17	−155

SOT-23 MMBR571

INPUT/OUTPUT REFLECTION COEFFICIENTS versus FREQUENCY
V_{CE} = 5 V, I_C = 30 mA



FORWARD/REVERSE TRANSMISSION COEFFICIENTS versus FREQUENCY
V_{CE} = 5 V, I_C = 30 mA

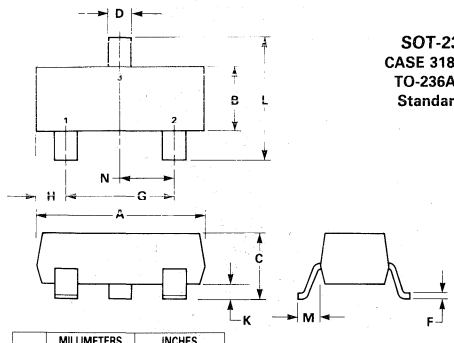


3

COMMON EMITTER S-PARAMETERS

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
5	5	200	0.68	−82	8.41	126	0.07	53	0.61	−45
		500	0.52	−142	4.62	93	0.10	46	0.35	−60
		1000	0.50	179	2.57	72	0.14	53	0.26	−71
		1500	0.51	161	1.82	57	0.19	58	0.24	−77
		2000	0.52	143	1.48	45	0.24	59	0.22	−86
	15	200	0.46	125	13.65	108	0.05	60	0.35	−73
		500	0.43	−169	6.03	86	0.09	66	0.17	−94
		1000	0.44	168	3.20	72	0.16	67	0.14	−111
		1500	0.45	152	2.21	58	0.22	64	0.11	−118
		2000	0.46	137	1.80	48	0.29	59	0.10	−131
	30	200	0.42	−148	14.79	102	0.04	68	0.26	−87
		500	0.41	−177	6.31	84	0.09	72	0.14	−115
		1000	0.42	165	3.35	71	0.16	70	0.12	−135
		1500	0.44	151	2.29	59	0.23	65	0.11	−144
		2000	0.44	135	1.84	48	0.30	60	0.10	−157
	50	200	0.41	−159	15.14	98	0.04	73	0.21	−96
		500	0.42	179	6.38	83	0.09	75	0.13	−124
		1000	0.43	163	3.35	70	0.16	71	0.12	−143
		1500	0.44	148	2.32	58	0.23	66	0.10	−151
		2000	0.45	134	1.84	48	0.30	60	0.09	−163

OUTLINE DIMENSIONS

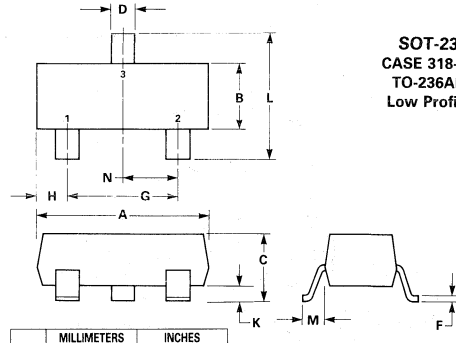


SOT-23
CASE 318-02
TO-236AA
Standard

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.85	1.20	0.033	0.0472
D	0.37	0.46	0.0150	0.0177
F	0.085	0.130	0.0034	0.0051
G	1.78	2.04	0.0701	0.0807
H	0.51	0.60	0.0200	0.0236
K	0.10	0.25	0.0040	0.0098
L	2.10	2.50	0.0830	0.0984
M	0.45	0.60	0.0180	0.0236
N	0.89	1.02	0.0350	0.0401

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
CONTROLLING DIMENSION: MILLIMETERS.



SOT-23
CASE 318-03
TO-236AB
Low Profile

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.89	1.11	0.035	0.044
D	0.37	0.46	0.015	0.0177
F	0.085	0.130	0.0034	0.0051
G	1.78	2.04	0.0701	0.0807
H	0.51	0.60	0.0200	0.0236
K	0.013	0.100	0.0005	0.0040
L	2.10	2.50	0.0830	0.0984
M	0.45	0.60	0.018	0.0236
N	0.89	1.02	0.0350	0.0401

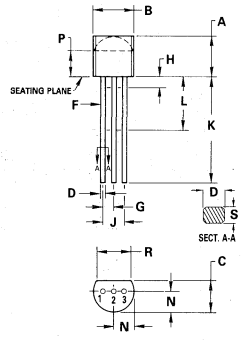
STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
CONTROLLING DIMENSION: MILLIMETERS.

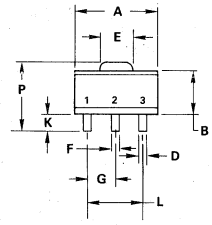
NOTES:
1. CONTOUR OF PACKAGE BEYOND ZONE "P" IS UNCONTROLLED.
2. DIM "F" APPLIES BETWEEN "H" AND "L". DIM "D" & "S" APPLIES BETWEEN "L" & 12.70 mm (0.5") FROM SEATING PLANE. LEAD DIM IS UNCONTROLLED IN "H" & BEYOND 12.70 mm (0.5") FROM SEATING PLANE.

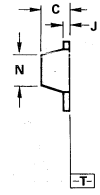
TO-92
CASE 29-02
TO-226AA
PLASTIC

STYLE 2:
PIN 1. BASE
2. EMMITTER
3. COLLECTOR



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	—	2.54	—	0.100
J	2.41	2.67	0.095	0.105
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.03	2.67	0.080	0.105
P	2.92	—	0.115	—
R	3.43	—	0.135	—
S	0.36	0.41	0.014	0.016





SOT-89
CASE 345-01
PLASTIC

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.40	4.60	0.174	0.181
B	2.29	2.60	0.091	0.102
C	1.40	1.60	0.056	0.062
D	0.36	0.48	0.015	0.018
E	1.62	1.80	0.064	0.070
F	0.44	0.53	0.018	0.020
G	1.50 BSC		0.059 BSC	
J	0.35	0.44	0.014	0.017
K	0.80	1.04	0.032	0.040
L	3.00 BSC		0.118 BSC	
N	2.04	2.28	0.081	0.089
P	3.94	4.25	0.156	0.167

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

NOTES:
1. DIMENSIONS A AND B ARE DATUMS.
2. -T- IS SEATING PLANE.
3. POSITIONAL TOLERANCE FOR LEADS: ⌖ 0.10 (0.004) Ⓜ T BⓈ AⓈ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.
5. CONTROLLING DIM: MILLIMETERS.

MPS901
MPS1983

NPN SILICON HIGH-FREQUENCY TRANSISTOR

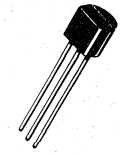
. . . designed primarily for use in high-gain, low-noise small-signal amplifiers.

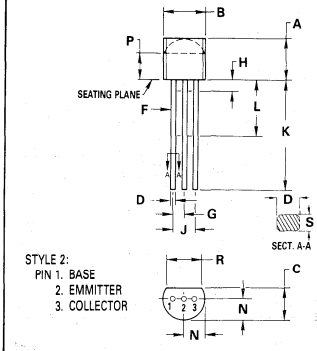
- High Current-Gain-Bandwidth Product — f_T = 4.5 GHz (Typ) @ I_C = 15 mAdc
- High Power Gain — G_{pe} = 12 dB (Typ) @ f = 900 MHz
- Low Noise Figure — NF = 2.4 dB (Typ) @ f = 900 MHz
- Low Feedback Capacitance — C_{cb} = 0.5 pF (Typ) @ V_{cb} = 10 V
- Die Source Same as MRF901

2.4 dB @ 900 MHz

HIGH FREQUENCY TRANSISTOR

NPN SILICON





NOTES:
1. CONTOUR OF PACKAGE BEYOND ZONE "P" IS UNCONTROLLED.
2. DIM "F" APPLIES BETWEEN "H" AND "L". DIM "D" & "S" APPLIES BETWEEN "L" & 12.70 mm (0.5") FROM SEATING PLANE. LEAD DIM IS UNCONTROLLED IN "H" & BEYOND 12.70 mm (0.5") FROM SEATING PLANE.

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	—	2.54	—	0.100
J	2.41	2.67	0.095	0.105
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.03	2.67	0.080	0.105
P	2.92	—	0.115	—
R	3.43	—	0.135	—
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply

CASE 29-02
TO-226AA

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CBO}	25	Vdc
Emitter-Base Voltage	V_{EBO}	2.0	Vdc
Collector Current — Continuous	I_C	30	mA
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 3.0	mW mW/°C
Operating Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	15	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	25	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	2.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	—	—	50	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 10 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	80	200	—
DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwidth Product I_C = 15 mAdc, V_{CE} = 10 Vdc, f = 1.0 GHz)	f_T	—	4.5	—	GHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	—	0.5	1.0	pF
Noise Figure (Figure 1) (I_C = 5.0 mAdc, V_{CE} = 10 Vdc, f = 900 MHz)	NF	—	2.4	—	dB
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (Figure 1) (I_C = 10 mA, V_{CE} = 10 Vdc, f = 900 MHz)	G_{pe}	—	12	—	dB

FIGURE 1 — 900 MHz TEST CIRCUIT SCHEMATIC

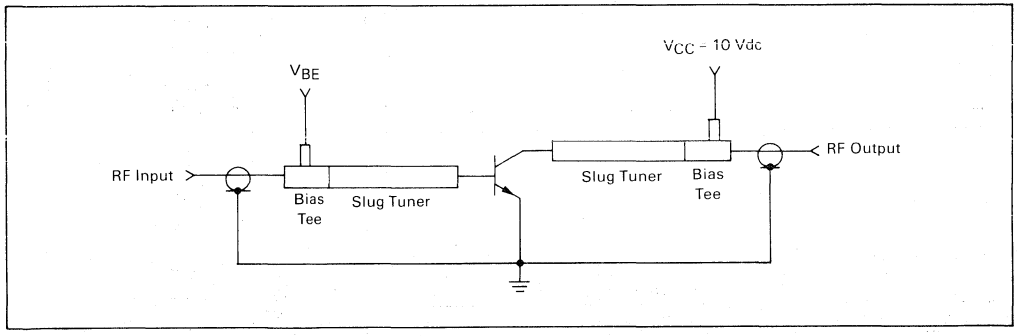


FIGURE 2 — CURRENT GAIN-BANDWIDTH PRODUCT versus COLLECTOR CURRENT

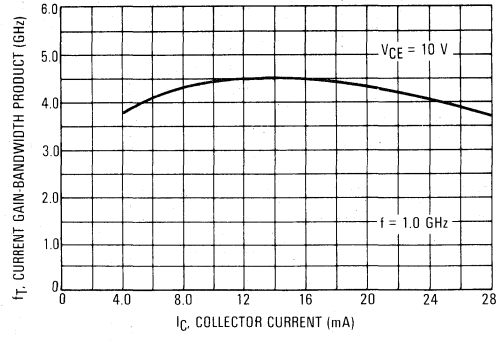


FIGURE 3 — MAXIMUM AVAILABLE GAIN versus COLLECTOR CURRENT

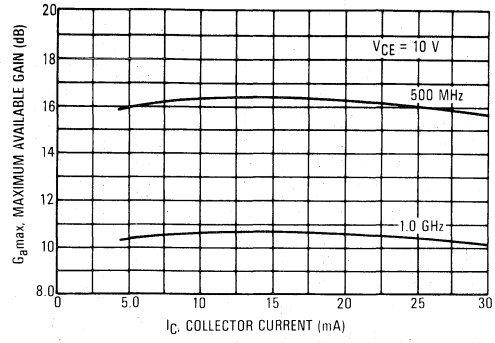


FIGURE 4 — $|S_{21}|^2$ versus FREQUENCY

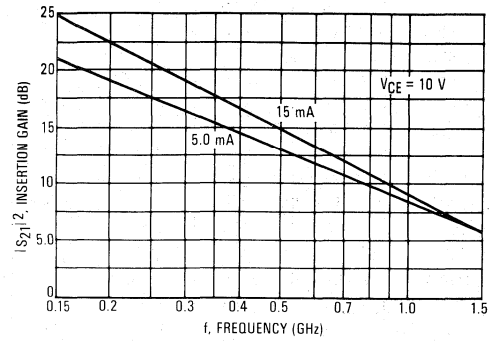


FIGURE 5 — NOISE FIGURE versus COLLECTOR CURRENT

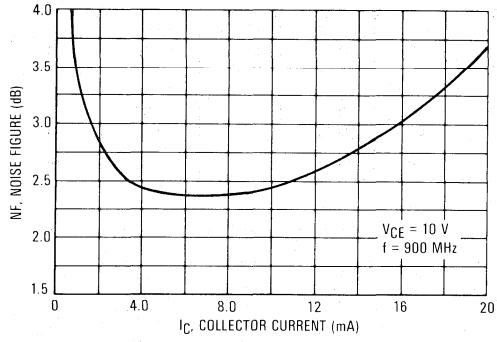


FIGURE 6 — NOISE FIGURE versus FREQUENCY

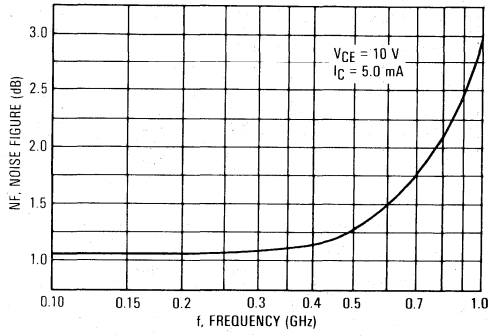


FIGURE 7 — INPUT CAPACITANCE versus EMITTER-BASE VOLTAGE

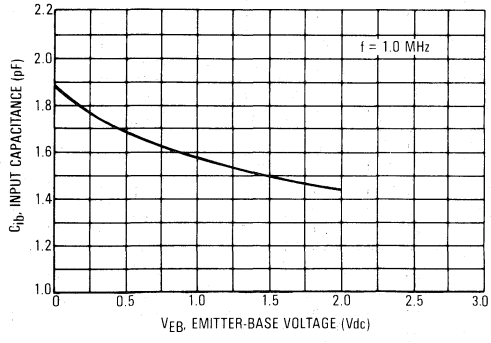
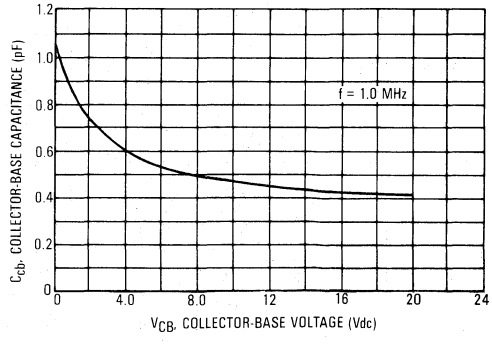


FIGURE 8 — COLLECTOR-BASE CAPACITANCE versus COLLECTOR-BASE VOLTAGE



3

TABLE I

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
5.0	5.0	100	0.76	-35	9.42	142	0.03	67	0.85	-18
		200	0.60	-63	7.98	122	0.05	58	0.70	-26
		500	0.28	-127	4.79	84	0.09	55	0.53	-35
		1000	0.27	148	2.71	50	0.15	51	0.42	-51
		1500	0.43	113	2.02	23	0.21	42	0.28	-79
	10	100	0.57	-51	14.80	131	0.03	65	0.75	-22
		200	0.36	-87	10.80	108	0.04	62	0.60	-26
		500	0.18	-151	5.23	77	0.08	62	0.48	-31
		1000	0.25	136	2.86	47	0.15	55	0.39	-48
		1500	0.42	109	2.12	22	0.22	42	0.25	-75
	15	100	0.42	-67	17.80	123	0.02	66	0.69	-22
		200	0.26	-105	11.50	101	0.04	66	0.56	-23
		500	0.17	-169	5.27	74	0.08	66	0.47	-28
		1000	0.26	131	2.86	46	0.15	57	0.39	-47
		1500	0.43	108	2.12	21	0.22	44	0.25	-73
	20	100	0.33	-82	18.66	117	0.02	67	0.66	-21
		200	0.22	-120	11.54	98	0.03	68	0.55	-21
		500	0.17	-171	5.16	72	0.08	67	0.48	-27
		1000	0.28	129	2.80	45	0.15	58	0.40	-45
		1500	0.45	107	2.07	19	0.22	45	0.27	-71
	25	100	0.28	-103	18.11	113	0.02	68	0.64	-20
		200	0.22	-138	11.03	95	0.03	70	0.55	-19
		500	0.20	169	4.94	71	0.08	68	0.50	-25
		1000	0.32	128	2.68	43	0.15	60	0.42	-44
		1500	0.49	106	1.98	17	0.22	47	0.30	-71
	30	100	0.31	-127	16.10	109	0.02	67	0.64	-16
		200	0.28	-156	9.69	93	0.03	70	0.57	-16
		500	0.28	160	4.32	69	0.07	70	0.53	-25
		1000	0.39	125	2.37	41	0.14	63	0.46	-44
		1500	0.55	104	1.73	15	0.21	51	0.34	-72

3

TABLE II

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
10	5.0	100	0.79	-33	9.36	144	0.03	68	0.88	-15
		200	0.63	-58	7.97	124	0.04	58	0.74	-22
		500	0.28	-117	4.87	86	0.07	57	0.60	-31
		1000	0.23	153	2.80	53	0.13	56	0.50	-46
		1500	0.38	116	2.09	26	0.19	48	0.38	-69
	10	100	0.60	-48	14.87	132	0.02	66	0.79	-18
		200	0.39	-79	11.06	110	0.03	63	0.65	-21
		500	0.16	-135	5.38	79	0.07	64	0.56	-28
		1000	0.20	138	2.97	50	0.13	59	0.47	-44
		1500	0.37	111	2.21	25	0.20	49	0.36	-66
	15	100	0.46	-61	18.20	124	0.02	66	0.74	-18
		200	0.28	-94	11.94	102	0.03	66	0.62	-19
		500	0.14	-154	5.45	76	0.07	67	0.55	-26
		1000	0.22	131	2.97	48	0.13	61	0.48	-42
		1500	0.38	109	2.21	24	0.20	50	0.36	-64
	20	100	0.37	-72	19.38	119	0.02	67	0.71	-17
		200	0.23	-105	11.97	99	0.03	68	0.61	-18
		500	0.14	-172	5.36	74	0.07	69	0.56	-24
		1000	0.23	128	2.91	47	0.13	62	0.48	-41
		1500	0.40	108	2.16	22	0.20	51	0.37	-64
	25	100	0.32	-86	19.40	115	0.02	68	0.70	-16
		200	0.22	-119	11.67	97	0.03	69	0.61	-16
		500	0.19	-176	5.28	74	0.06	70	0.57	-23
		1000	0.26	127	2.82	46	0.13	63	0.50	-41
		1500	0.43	107	2.09	21	0.19	53	0.40	-63
	30	100	0.29	-103	18.29	112	0.02	68	0.70	-14
		200	0.22	-135	10.86	95	0.03	70	0.62	-15
		500	0.20	165	4.82	72	0.06	72	0.59	-22
		1000	0.31	125	2.63	44	0.12	66	0.53	-41
		1500	0.47	106	1.95	19	0.19	55	0.43	-64

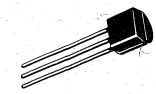
NPN Silicon High Frequency Transistors

MPS911
MXR911
MMBR911

LOW NOISE
HIGH RF GAIN

. . . designed for low noise, wide dynamic range front-end amplifiers and low-noise VCO's. Available in two surface-mountable plastic package styles, as well as the popular TO-92 package. This Motorola series of small-signal plastic transistors offers superior quality and performance at low cost.

- High Gain-Bandwidth Product
  f_T = 7 GHz (Typ) @ 30 mA
- Low Noise Figure
  NF = 1.7 dB (Typ) @ 500 MHz
- High Gain
  G_{NF} = 17 dB (Typ) @ 10 mA/500 MHz
- State-of-the-Art Technology
  Fine Line Geometry
  Ion-Implanted Arsenic Emitters
  Gold Top Metallization and Wires
  Silicon Nitride Passivation
- Tape and Reel Packaging Options
- MMBR911 Available in Low Profile, Add L Suffix



TO-92
CASE 29
MPS911



SOT-89
CASE 345
MXR911



SOT-23
CASE 318
MMBR911
Standard and Low Profile

MAXIMUM RATINGS

Ratings	Symbol	MPS911	MXR911	MMBR911	Unit
Collector-Emitter Voltage	V_{CEO}	12			Vdc
Collector-Base Voltage	V_{CBO}	20			Vdc
Emitter-Base Voltage	V_{EBO}	3			Vdc
Collector Current — Continuous	I_C	60			mA
Power Dissipation @ T_A = 25°C	P_D	625	400 (Free Air)	200 (Free Air)	mW
Storage Temperature	T_{stg}	−55 to +150			°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Collector-Emitter Breakdown Voltage (I_C = 1 mAdc, I_B = 0)			$V_{(BR)CEO}$	12	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)			$V_{(BR)CBO}$	20	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mA, I_C = 0)			$V_{(BR)EBO}$	3	—	—	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)			I_{CBO}	—	—	50	nAdc
ON CHARACTERISTICS							
DC Current Gain (I_C = 30 mAdc, V_{CE} = 10 Vdc)			h_{FE}	30	—	200	—
DYNAMIC CHARACTERISTICS							
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)			C_{cb}	—	—	1	pF
Current Gain-Bandwidth Product (V_{CE} = 10 Vdc, I_C = 30 mAdc, f = 1 GHz)	MPS911		f_T	—	7	—	GHz
	MXR911			—	7	—	
	MMBR911			—	6	—	
FUNCTIONAL TESTS							
Gain @ Noise Figure (I_C = 10 mAdc, V_{CE} = 10 Vdc)	MPS911	f = 0.5 GHz	G_{NF}	—	16.5	—	dB
		f = 1 GHz		—	11	—	
	MXR911	f = 0.5 GHz		—	16	—	
		f = 1 GHz		—	8.5	—	
	MMBR911	f = 0.5 GHz		—	17	—	
		f = 1 GHz		—	11	—	
Noise Figure (I_C = 10 mAdc, V_{CE} = 10 Vdc)	MPS911	f = 0.5 GHz	NF	—	1.7	—	dB
		f = 1 GHz		—	2.7	—	
	MXR911	f = 0.5 GHz		—	2	—	
		f = 1 GHz		—	2.6	—	
	MMBR911	f = 0.5 GHz		—	2	—	
		f = 1 GHz		—	2.9	—	

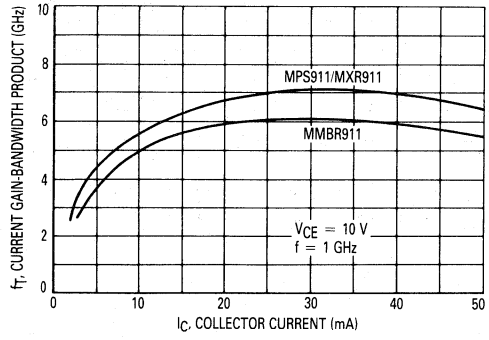
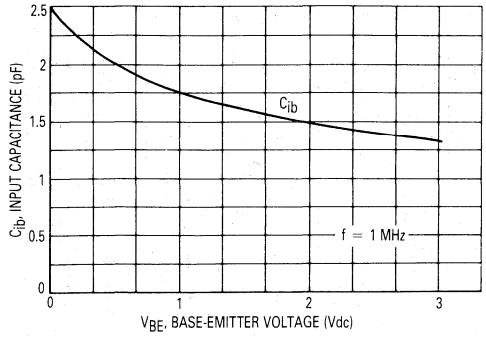
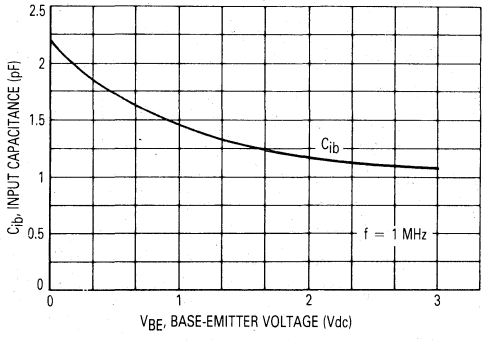


Figure 1. Current Gain-Bandwidth versus Collector Current @ 1 GHz

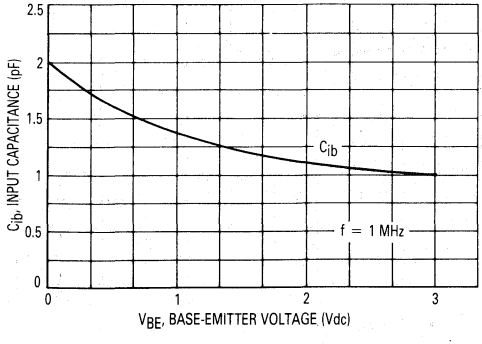
Figure 2. Input Capacitance versus Base-Emitter Voltage



(a) TO-92 MPS911

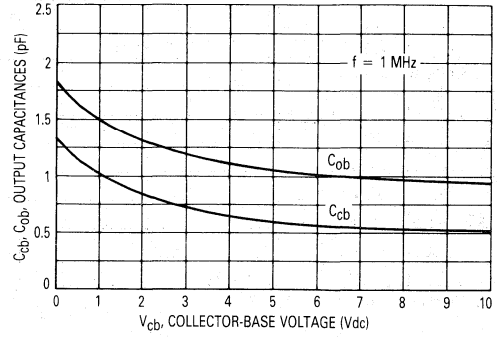


(b) SOT-89 MXR911

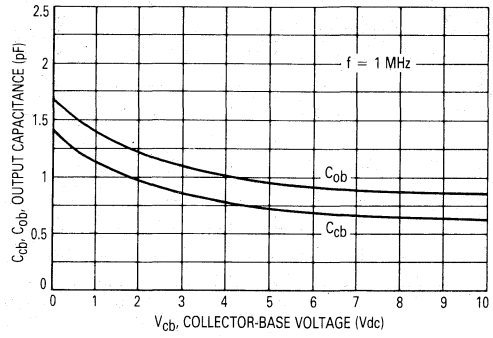


(c) SOT-23 MMBR911

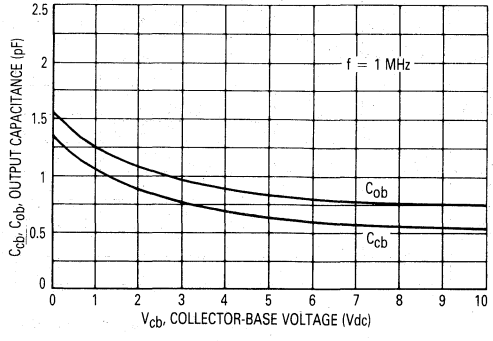
Figure 3. Output Capacitances versus Collector-Base Voltage



(a) TO-92 MPS911

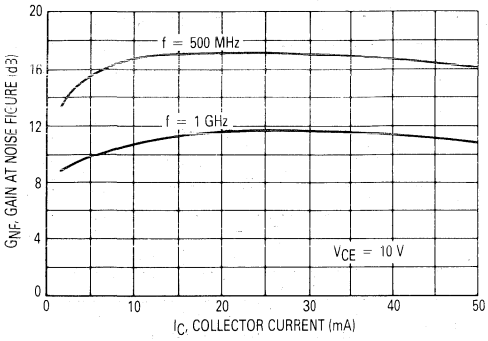


(b) SOT-89 MXR911

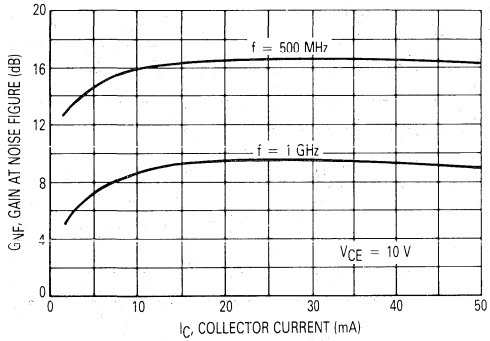


(c) SOT-23 MMBR911

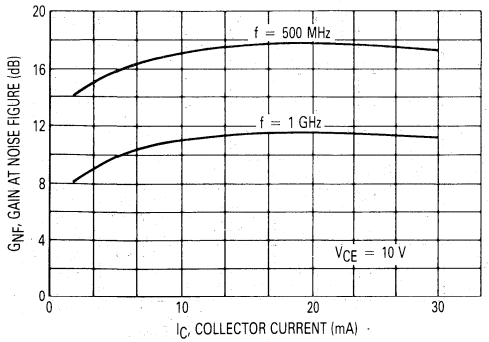
Figure 4. Gain at Noise Figure versus Collector Current



(a) TO-92 MPS911

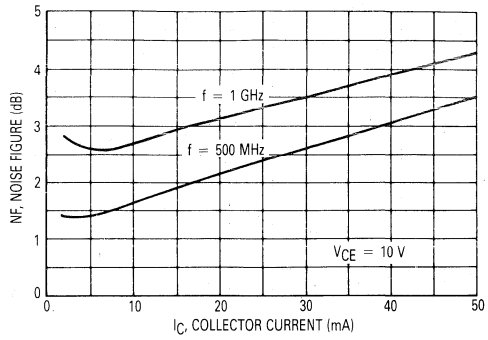


(b) SOT-89 MXR911

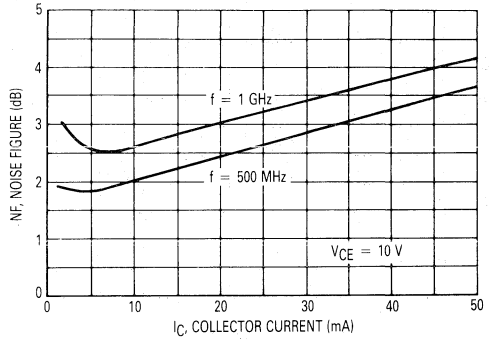


(c) SOT-23 MMBR911

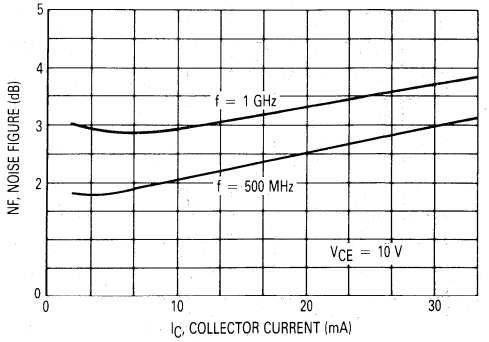
Figure 5. Noise Figure versus Collector Current



(a) TO-92 MPS911

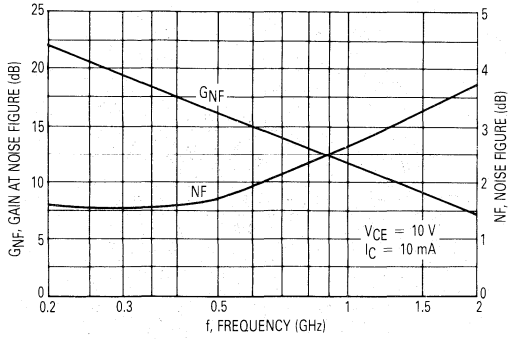


(b) SOT-89 MXR911

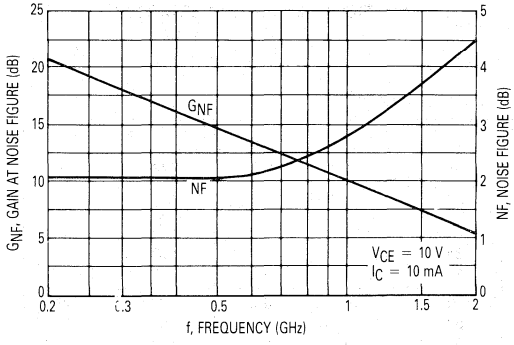


(c) SOT-23 MMBR911

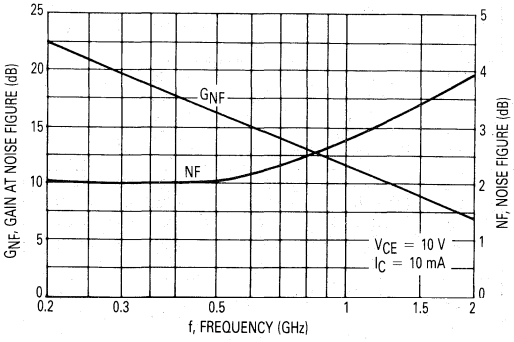
Figure 6. Gain at Noise Figure and Noise Figure versus Frequency



(a) TO-92 MPS911

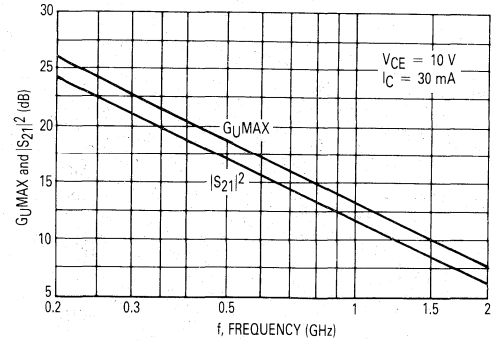


(b) SOT-89 MXR911

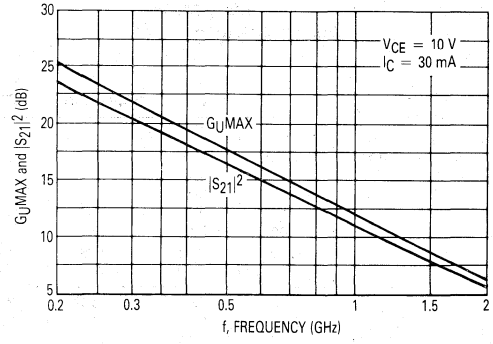


(c) SOT-23 MMBR911

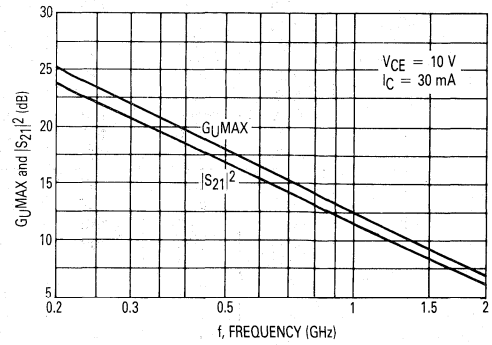
Figure 7. Maximum Unilateral Gain and Insertion Gain versus Frequency



(a) TO-92 MPS911



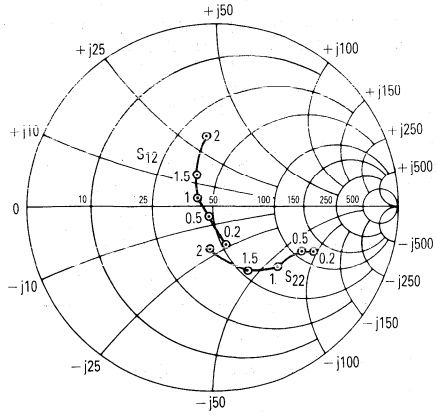
(b) SOT-89 MXR911



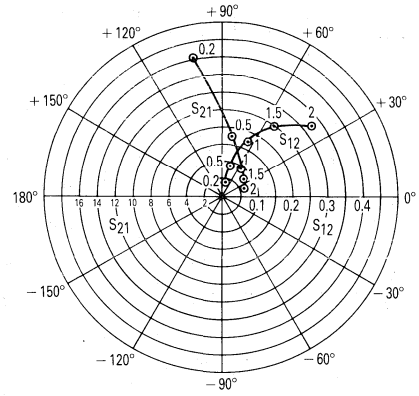
(c) SOT-23 MMBR911

3

TO-92 MPS911



INPUT AND OUTPUT REFLECTION COEFFICIENTS versus FREQUENCY
V_{CE} = 10 V, I_C = 30 mA



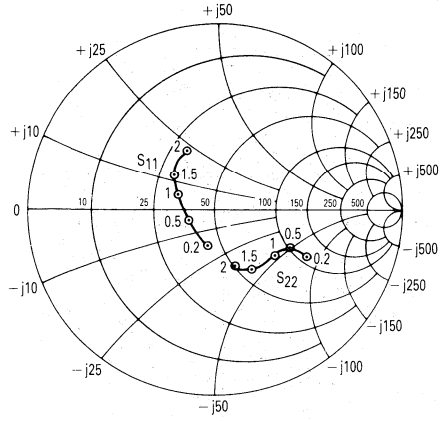
FORWARD AND REVERSE TRANSMISSION COEFFICIENTS versus FREQUENCY
V_{CE} = 10 V, I_C = 30 mA

3

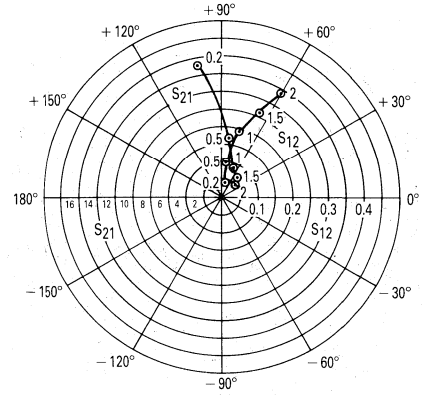
COMMON EMITTER S-PARAMETERS

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
10	2	200	0.78	−46	4.42	134	0.06	69	0.95	−18
		500	0.46	−107	3.35	98	0.10	56	0.78	−30
		1000	0.30	172	2.23	61	0.14	54	0.66	−48
		1500	0.41	118	1.66	34	0.20	51	0.57	−70
		2000	0.60	89	1.43	11	0.29	45	0.46	−107
	5	200	0.72	−55	8.75	126	0.05	68	0.87	−23
		500	0.31	−107	5.23	92	0.09	63	0.68	−31
		1000	0.18	178	3.05	61	0.15	60	0.57	−46
		1500	0.27	122	2.22	38	0.22	52	0.50	−66
		2000	0.45	94	1.90	17	0.30	43	0.38	−97
	10	200	0.48	−64	12.79	114	0.04	73	0.74	−24
		500	0.16	−100	6.19	85	0.09	71	0.60	−29
		1000	0.09	165	3.45	59	0.17	63	0.50	−44
		1500	0.22	112	2.50	36	0.25	50	0.41	−65
		2000	0.41	90	2.14	16	0.32	38	0.26	−98
	20	200	0.29	−67	15.30	106	0.04	78	0.65	−23
		500	0.08	−92	6.76	82	0.09	75	0.55	−27
		1000	0.06	144	3.71	58	0.17	64	0.46	−43
		1500	0.20	108	2.65	30	0.25	51	0.37	−63
		2000	0.38	89	2.25	18	0.32	38	0.23	−94
	30	200	0.20	−70	16.04	103	0.04	80	0.61	−22
		500	0.05	−97	6.90	81	0.09	77	0.53	−25
		1000	0.07	138	3.76	58	0.17	66	0.46	−41
		1500	0.20	109	2.68	38	0.25	52	0.37	−61
		2000	0.38	90	2.28	20	0.32	40	0.24	−91
	50	200	0.13	−78	15.26	99	0.04	82	0.62	−18
		500	0.03	−145	6.48	79	0.09	78	0.56	−23
		1000	0.11	126	3.55	56	0.17	67	0.49	−40
		1500	0.24	105	2.56	36	0.25	53	0.39	−62
		2000	0.43	87	2.17	17	0.32	40	0.25	−95

SOT-89 MXR911



INPUT/OUTPUT REFLECTION COEFFICIENTS versus FREQUENCY
V_{CE} = 10 V, I_C = 30 mA

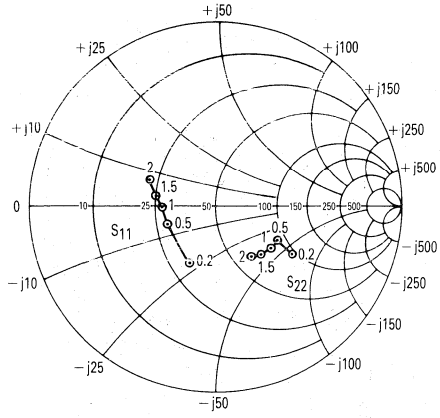


FORWARD AND REVERSE TRANSMISSION COEFFICIENTS versus FREQUENCY
V_{CE} = 10 V, I_C = 30 mA

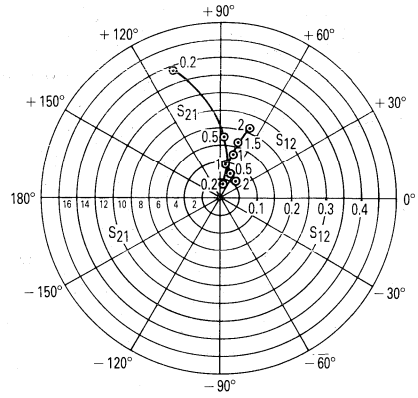
COMMON EMITTER S-PARAMETERS

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
10	2	200	0.80	−46	5.04	130	0.07	67	0.91	−18
		500	0.52	−100	3.58	100	0.11	56	0.74	−27
		1000	0.36	−173	2.32	72	0.16	59	0.64	−37
		1500	0.41	147	1.71	51	0.21	63	0.59	−50
		2000	0.48	118	1.36	37	0.27	65	0.56	−64
	5	200	0.65	−60	8.65	128	0.06	67	0.81	−24
		500	0.34	−115	5.10	93	0.10	65	0.61	−30
		1000	0.26	177	2.90	71	0.17	67	0.54	−38
		1500	0.32	143	2.11	53	0.23	64	0.49	−50
		2000	0.40	116	1.67	39	0.30	62	0.45	−65
	10	200	0.44	−72	11.87	118	0.05	70	0.70	−27
		500	0.21	−123	6.04	89	0.10	71	0.53	−31
		1000	0.19	171	3.27	70	0.18	70	0.47	−39
		1500	0.27	140	2.35	53	0.25	65	0.42	−53
		2000	0.35	115	1.88	41	0.32	60	0.38	−68
	20	200	0.27	−83	14.16	108	0.05	74	0.59	−28
		500	0.13	−138	6.57	85	0.10	75	0.47	−29
		1000	0.16	161	3.48	69	0.19	72	0.42	−39
		1500	0.24	135	2.49	53	0.26	65	0.37	−54
		2000	0.33	113	1.98	41	0.34	59	0.33	−71
	30	200	0.18	−95	14.93	103	0.04	77	0.54	−26
		500	0.11	−153	6.70	83	0.10	76	0.44	−27
		1000	0.16	156	3.52	68	0.19	73	0.41	−38
		1500	0.24	133	2.50	54	0.26	66	0.36	−54
		2000	0.33	112	2.00	42	0.34	60	0.32	−71
	50	200	0.15	−111	14.26	101	0.04	79	0.53	−22
		500	0.12	−160	6.45	82	0.09	77	0.46	−24
		1000	0.19	152	3.39	68	0.18	73	0.43	−37
		1500	0.27	130	2.41	53	0.26	67	0.38	−51
		2000	0.35	110	1.92	41	0.33	61	0.34	−68

SOT-23 MMBR911



INPUT/OUTPUT REFLECTION COEFFICIENTS
versus FREQUENCY
V_{CE} = 10 V, I_C = 30 mA



FORWARD AND REVERSE TRANSMISSION
COEFFICIENTS versus FREQUENCY
V_{CE} = 10 V, I_C = 30 mA

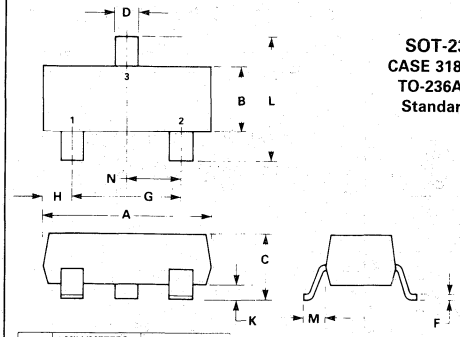
3

COMMON EMITTER S-PARAMETERS

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
10	2	200	0.82	−45	4.14	145	0.06	66	0.88	−16
		500	0.60	−96	3.23	112	0.09	49	0.71	−27
		1000	0.47	−149	2.16	85	0.11	49	0.62	−34
		1500	0.46	−179	1.59	71	0.13	55	0.58	−43
		2000	0.47	162	1.35	57	0.16	62	0.56	−51
	5	200	0.66	−63	8.63	134	0.05	64	0.75	−25
		500	0.43	−117	5.29	100	0.07	58	0.55	−31
		1000	0.37	−163	3.05	82	0.11	63	0.48	−36
		1500	0.38	176	2.17	70	0.15	65	0.45	−44
		2000	0.40	160	1.81	57	0.19	65	0.43	−51
	10	200	0.49	−83	12.70	124	0.04	65	0.62	−30
		500	0.33	−134	6.42	94	0.07	66	0.44	−32
		1000	0.32	−171	3.53	80	0.12	70	0.41	−36
		1500	0.35	173	2.46	69	0.16	69	0.38	−45
		2000	0.37	159	2.04	58	0.20	66	0.35	−52
	20	200	0.36	−103	15.25	114	0.03	69	0.52	−32
		500	0.28	−149	6.95	90	0.06	72	0.39	−30
		1000	0.29	−176	3.73	78	0.12	73	0.37	−35
		1500	0.33	172	2.60	68	0.17	71	0.34	−43
		2000	0.36	158	2.14	58	0.21	67	0.32	−52
	30	200	0.32	−114	15.64	109	0.03	71	0.48	−29
		500	0.27	−156	6.92	88	0.06	73	0.38	−27
		1000	0.29	−178	3.71	78	0.12	74	0.37	−33
		1500	0.34	170	2.58	68	0.16	72	0.34	−44
		2000	0.37	156	2.13	57	0.21	68	0.32	−51

OUTLINE DIMENSIONS

SOT-23
CASE 318-02
TO-236AA
Standard

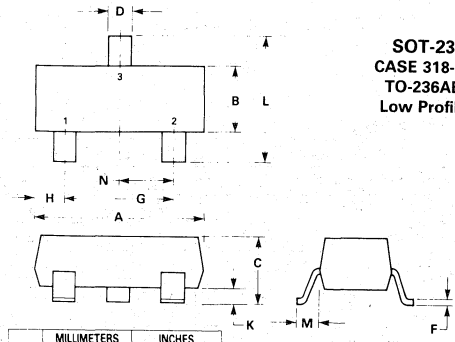


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.85	1.20	0.033	0.0472
D	0.37	0.46	0.0150	0.0177
F	0.085	0.130	0.0034	0.0051
G	1.78	2.04	0.0701	0.0807
H	0.51	0.60	0.0200	0.0236
K	0.10	0.25	0.0040	0.0098
L	2.10	2.50	0.0830	0.0984
M	0.45	0.60	0.0180	0.0236
N	0.89	1.02	0.0350	0.0401

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI
2. Y14.5M, 1982.
CONTROLLING DIMENSION: MILLIMETERS

SOT-23
CASE 318-03
TO-236AB
Low Profile



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.89	1.11	0.035	0.044
D	0.37	0.46	0.015	0.0177
F	0.085	0.130	0.0034	0.0051
G	1.78	2.04	0.0701	0.0807
H	0.51	0.60	0.0200	0.0236
K	0.013	0.100	0.0005	0.0040
L	2.10	2.50	0.0830	0.0984
M	0.45	0.60	0.018	0.0236
N	0.89	1.02	0.0350	0.0401

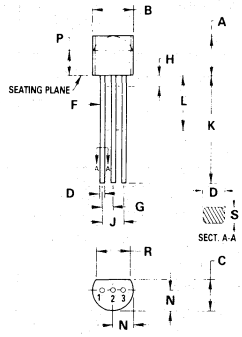
STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI
2. Y14.5M, 1982.
CONTROLLING DIMENSION: MILLIMETERS.

NOTES:
1. CONTOUR OF PACKAGE BEYOND ZONE "P" IS UNCONTROLLED.
2. DIM "F" APPLIES BETWEEN "H" AND "L". DIM "D" & "S" APPLIES BETWEEN "L" & 12.70 mm (0.5") FROM SEATING PLANE. LEAD DIM IS UNCONTROLLED IN "H" & BEYOND 12.70 mm (0.5") FROM SEATING PLANE.

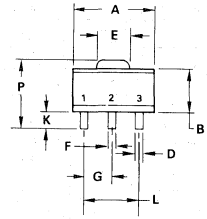
TO-92
CASE 29-02
TO-226AA
PLASTIC

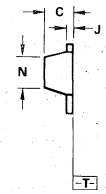
STYLE 2:
PIN 1. BASE
2. EMMITTER
3. COLLECTOR



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	—	2.54	—	0.100
J	2.41	2.67	0.095	0.105
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.03	2.67	0.080	0.105
P	2.92	—	0.115	—
R	3.43	—	0.135	—
S	0.36	0.41	0.014	0.016

SOT-89
CASE 345-01
PLASTIC





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.40	4.60	0.174	0.181
B	2.29	2.60	0.091	0.102
C	1.40	1.60	0.056	0.062
D	0.36	0.48	0.015	0.018
E	1.62	1.80	0.064	0.070
F	0.44	0.53	0.018	0.020
G	1.50 BSC		0.059 BSC	
J	0.35	0.44	0.014	0.017
K	0.80	1.04	0.032	0.040
L	3.00 BSC		0.118 BSC	
N	2.04	2.28	0.081	0.089
P	3.94	4.25	0.156	0.167

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

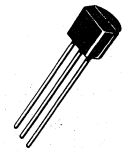
NOTES:
1. DIMENSIONS A AND B ARE DATUMS.
2. -T- IS SEATING PLANE.
3. POSITIONAL TOLERANCE FOR LEADS:
⌖ | 0.10 (0.004) Ⓜ | T | BⓈ | AⓈ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.
5. CONTROLLING DIM: MILLIMETERS.

3

MPS3866

Die Source Same as 2N3866

AMPLIFIER TRANSISTOR
NPN SILICON



CASE 29-02, STYLE 1
TO-92
(TO-226AA)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	55	Vdc
Emitter-Base Voltage	V_{EBO}	3.5	Vdc
Collector Current — Continuous	I_C	0.4	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W

3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, R_{BE} = 10 Ω)	$V_{CER(sus)}$	55	—	Vdc
Collector-Emitter Sustaining Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{CEO(sus)}$	30	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	—	Vdc
Collector Cutoff Current (V_{CE} = 28 Vdc, I_B = 0)	I_{CEO}	—	0.02	mAdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = −1.5 Vdc (Rev.), T_C = 150°C) (V_{CE} = 55 Vdc, V_{BE} = −1.5 Vdc (Rev.))	I_{CEX}	— —	5.0 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 3.5 Vdc, I_C = 0)	I_{EBO}	—	0.1	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 360 mAdc, V_{CE} = 5.0 Vdc)(1) (I_C = 50 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0 10	— 200	—
Collector-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 20 mAdc)	$V_{CE(sat)}$	—	1.0	Vdc
SMALL-SIGNAL CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 50 mAdc, V_{CE} = 15 Vdc, f = 200 MHz)	f_T	500	—	MHz
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{obo}	—	3.0	pF
FUNCTIONAL TEST				
Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 1.0 W, f = 400 MHz)	G_{pe}	10	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 1.0 W, f = 400 MHz)	η	45	—	%

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

MRF134

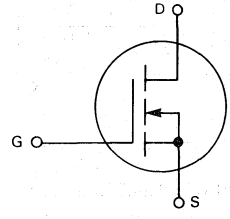
The RF TMOS Line

N-CHANNEL ENHANCEMENT-MODE
TMOS RF POWER FIELD-EFFECT TRANSISTOR

. . . designed for wideband large-signal amplifier and oscillator applications in the 2.0 to 400 MHz range.

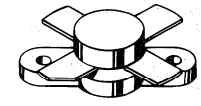
- Guaranteed 28 Volt, 150 MHz Performance
  - Output Power = 5.0 Watts
  - Minimum Gain = 11 dB
  - Efficiency — 55% (Typical)
- Small-Signal and Large-Signal Characterization
- Typical Performance at 400 MHz, 28 Vdc, 5.0 W
  - Output = 10.6 dB Gain
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR
- Low Noise Figure — 2.0 dB (Typ) at 200 mA, 150 MHz
- Excellent Thermal Stability, Ideally Suited For Class A Operation

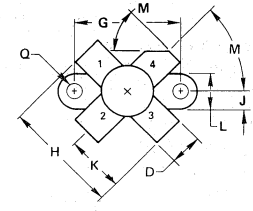
TMOS™

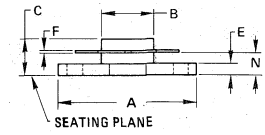


5.0 W 2.0-400 MHz

N-CHANNEL TMOS
BROADBAND RF POWER
FET







STYLE 2:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	9.40	9.91	0.370	0.390
C	5.82	7.14	0.229	0.281
D	5.46	5.97	0.215	0.235
E	2.16	2.67	0.085	0.105
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	20.07	20.57	0.790	0.810
K	10.03	10.29	0.395	0.405
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.81	4.57	0.150	0.180
Q	2.87	3.30	0.113	0.130

CASE 211-07

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain — Source Voltage	V_{DSS}	65	Vdc
Drain — Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate — Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	0.9	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	17.5 0.10	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

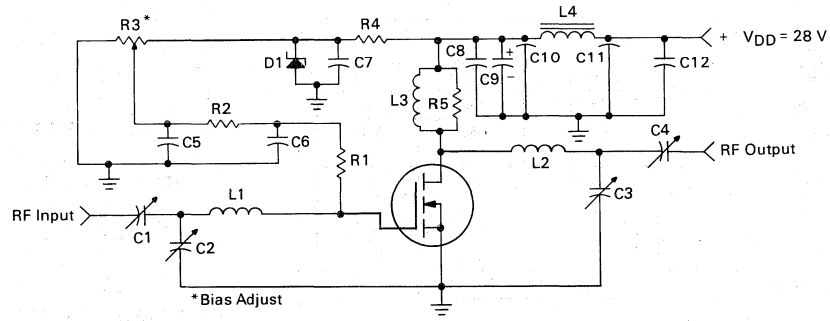
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	1.0	mAdc
Gate-Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (I_D = 10 mA, V_{DS} = 10 V)	$V_{GS(th)}$	1.0	3.5	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 100 mA)	g_{fs}	80	110	—	mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	7.0	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	9.7	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	2.3	—	pF
FUNCTIONAL CHARACTERISTICS					
Noise Figure (V_{DS} = 28 Vdc, I_D = 200 mA, f = 150 MHz)	NF	—	2.0	—	dB
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 5.0 W, I_{DQ} = 50 mA) f = 150 MHz (Fig. 1) f = 400 MHz (Fig. 14)	G_{ps}	11 —	14 10.6	— —	dB
Drain Efficiency (Fig. 1) (V_{DD} = 28 Vdc, P_{out} = 5.0 W, f = 150 MHz, I_{DQ} = 50 mA)	η	50	55	—	%
Electrical Ruggedness (Fig. 1) (V_{DD} = 28 Vdc, P_{out} = 5.0 W, f = 150 MHz, I_{DQ} = 50 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			

FIGURE 1 — 150 MHz TEST CIRCUIT



C1, C4 — Arco 406, 15–115 pF
C2 — Arco 403, 3–35 pF
C3 — Arco 402, 1.5–20 pF
C5, C6, C7, C8, C12 — 0.1 μF Erie Redcap
C9 — 10 μF, 50 V
C10, C11 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener
L1 — 3 Turns, 0.310″ ID, #18 AWG Enamel, 0.2″ Long
L2 — 3-1/2 Turns, 0.310″ ID, #18 AWG Enamel, 0.25″ Long
L3 — 20 Turns, #20 AWG Enamel Wound on R5
L4 — Ferroxcube VK-200 — 19/4B
R1 — 68 Ω, 1.0 W Thin Film
R2 — 10 kΩ, 1/4 W
R3 — 10 Turns, 10 kΩ Beckman Instruments 8108
R4 — 1.8 kΩ, 1/2 W
R5 — 1.0 MΩ, 2.0 W Carbon
Board — G10, 62 mils

FIGURE 2 — OUTPUT POWER versus INPUT POWER

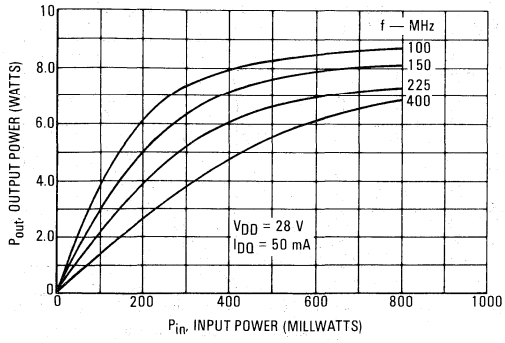


FIGURE 3 — OUTPUT POWER versus INPUT POWER

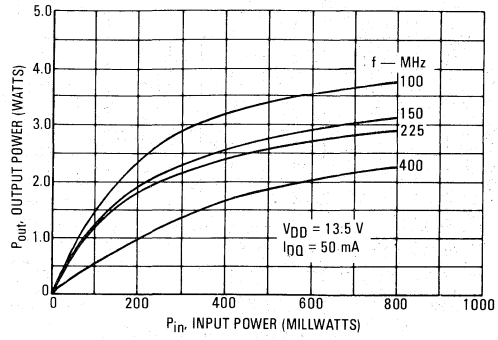


FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 100 MHz

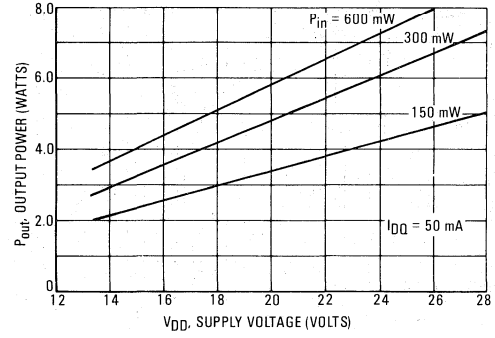


FIGURE 5 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 150 MHz

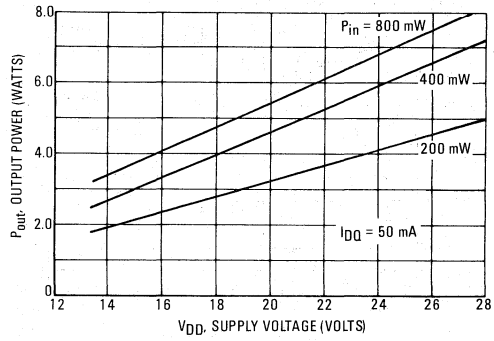


FIGURE 6 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 225 MHz

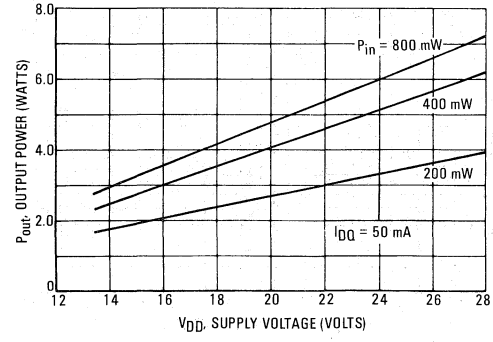


FIGURE 7 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 400 MHz

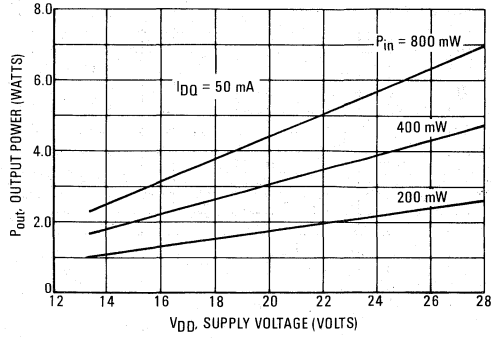


FIGURE 8 — OUTPUT POWER versus GATE VOLTAGE

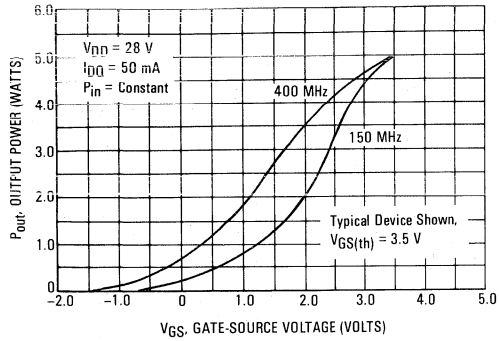


FIGURE 9 — DRAIN CURRENT versus GATE VOLTAGE (TRANSFER CHARACTERISTICS)

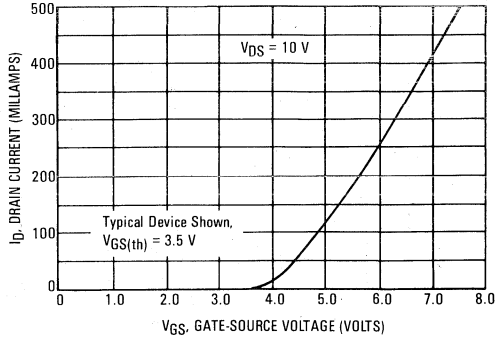


FIGURE 10 — GATE-SOURCE VOLTAGE versus CASE TEMPERATURE

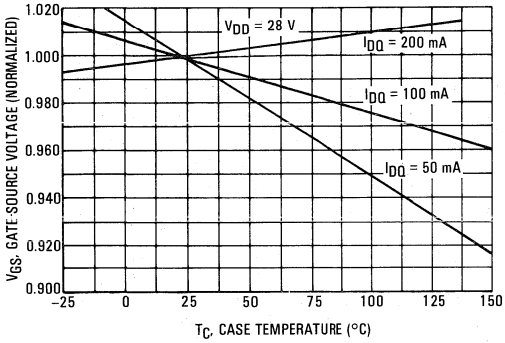


FIGURE 11 — MAXIMUM AVAILABLE GAIN versus FREQUENCY

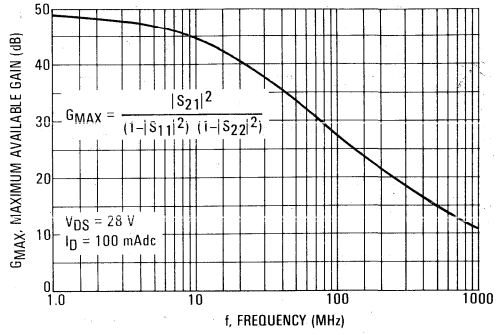


FIGURE 12 — CAPACITANCE versus VOLTAGE

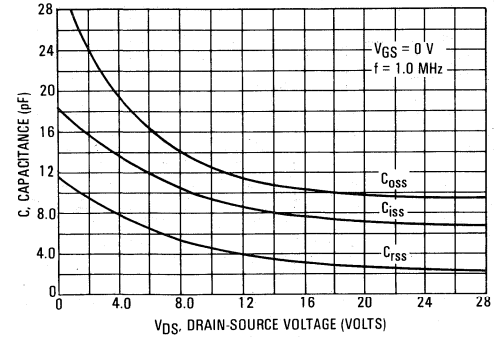


FIGURE 13 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

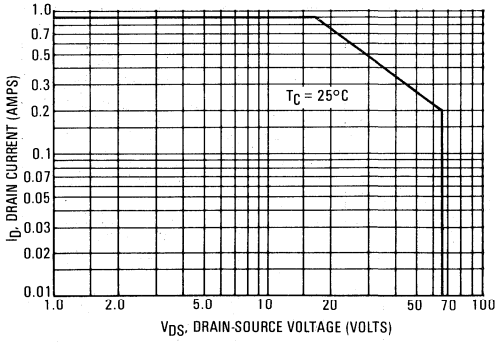
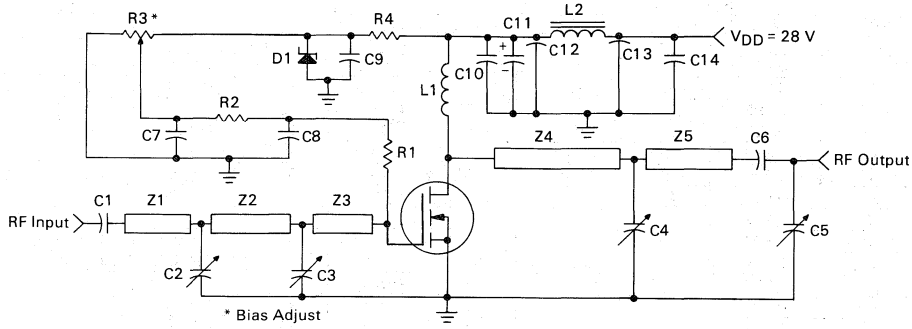


FIGURE 14 — 400 MHz TEST CIRCUIT



C1, C6 — 270 pF, ATC 100 mils
C2, C3, C4, C5 — 0–20 pF Johanson
C7, C9, C10, C14 — 0.1 μF Erie Redcap, 50 V
C8 — 0.001 μF
C11 — 10 μF, 50 V
C12, C13 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener
L1 — 6 Turns, 1/4″ ID, #20 AWG Enamel
L2 — Ferroxcube VK-200 — 19/4B
R1 — 68 Ω, 1.0 W Thin Film
R2 — 10 kΩ, 1/4 W
R3 — 10 Turns, 10 kΩ Beckman Instruments 8108
R4 — 1.8 kΩ, 1/2 W
Z1 — 1.4″ × 0.166″ Microstrip
Z2 — 1.1″ × 0.166″ Microstrip
Z3 — 0.95″ × 0.166″ Microstrip
Z4 — 2.2″ × 0.166″ Microstrip
Z5 — 0.85″ × 0.166″ Microstrip
Board — Glass Teflon, 62 mils

FIGURE 15 — LARGE-SIGNAL SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCES, Z_{in}†, Z_{OL}*

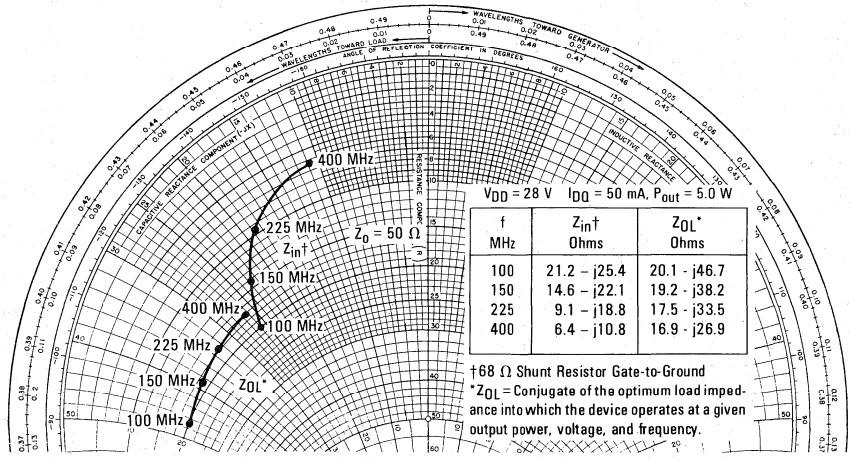


FIGURE 16 — COMMON SOURCE SCATTERING PARAMETERS
V_{DS} = 28 V, I_D = 100 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
1.0	0.989	-1.0	11.27	179	0.0014	89	0.954	-1.0
2.0	0.989	-2.0	11.27	179	0.0028	89	0.954	-2.0
5.0	0.988	-5.0	11.26	176	0.0069	86	0.954	-4.0
10	0.985	-10	11.20	173	0.014	83	0.951	-9.0
20	0.977	-20	10.99	166	0.027	76	0.938	-18
30	0.965	-30	10.66	159	0.039	69	0.918	-26
40	0.950	-39	10.25	153	0.051	63	0.895	-34
50	0.931	-47	9.777	147	0.060	57	0.867	-42
60	0.912	-53	9.359	142	0.069	53	0.846	-49
70	0.892	-58	8.960	138	0.077	49	0.828	-56
80	0.874	-62	8.583	135	0.085	46	0.815	-62
90	0.855	-66	8.190	131	0.091	43	0.801	-68
100	0.833	-70	7.808	128	0.096	40	0.785	-74
110	0.827	-73	7.661	125	0.101	38	0.784	-77
120	0.821	-76	7.515	122	0.107	36	0.784	-82
130	0.814	-79	7.368	119	0.113	34	0.784	-85
140	0.808	-82	7.222	116	0.119	32	0.783	-88
150	0.802	-86	7.075	114	0.125	31	0.783	-90
160	0.788	-89	6.810	112	0.127	30	0.780	-92
170	0.774	-92	6.540	110	0.128	28	0.774	-94
180	0.763	-94	6.220	108	0.130	26	0.762	-98
190	0.751	-97	5.903	106	0.132	24	0.760	-100
200	0.740	-100	5.784	104	0.134	23	0.758	-103
225	0.719	-104	5.334	100	0.136	20	0.757	-107
250	0.704	-108	4.904	97	0.139	19	0.758	-110
275	0.687	-113	4.551	92	0.141	16	0.757	-114
300	0.673	-117	4.219	89	0.141	14	0.750	-117
325	0.668	-120	3.978	86	0.142	12	0.757	-120
350	0.669	-123	3.737	83	0.142	10	0.766	-121
375	0.662	-125	3.519	80	0.143	9.0	0.768	-123
400	0.654	-127	3.325	77	0.142	8.0	0.772	-124
425	0.650	-129	3.170	75	0.140	7.0	0.772	-125
450	0.638	-131	3.048	72	0.141	6.0	0.783	-125
475	0.614	-132	2.898	71	0.136	6.0	0.786	-126
500	0.641	-133	2.833	68	0.136	5.0	0.795	-127
525	0.638	-135	2.709	66	0.135	5.0	0.801	-127
550	0.633	-137	2.574	64	0.133	4.0	0.802	-128
575	0.628	-138	2.481	62	0.131	5.0	0.805	-128
600	0.625	-140	2.408	60	0.129	5.0	0.814	-128
625	0.619	-142	2.334	58	0.128	5.0	0.818	-129
650	0.617	-144	2.259	56	0.125	6.0	0.824	-130
675	0.618	-146	2.192	55	0.123	7.0	0.834	-130
700	0.619	-147	2.124	53	0.122	8.0	0.851	-131
725	0.618	-150	2.061	51	0.120	9.0	0.859	-132
750	0.614	-152	1.983	49	0.118	11	0.857	-133
775	0.609	-154	1.908	48	0.119	13	0.865	-133
800	0.562	-155	1.877	49	0.118	15	0.872	-133
825	0.587	-156	1.869	46	0.119	16	0.869	-134
850	0.593	-158	1.794	44	0.118	18	0.875	-135
875	0.597	-160	1.749	43	0.119	18	0.881	-135
900	0.598	-162	1.700	41	0.118	18	0.889	-136
925	0.592	-164	1.641	40	0.115	18	0.888	-138
950	0.588	-166	1.590	39	0.112	20	0.877	-138
975	0.586	-168	1.572	39	0.108	23	0.864	-137
1000	0.590	-171	1.551	37	0.107	28	0.863	-137

The Power RF characterization data were measured with a 68 ohm resistor shunting the MRF134 input port. The scattering parameters were measured on the MRF134 device alone with no external components.

FIGURE 17 — S_{11}, INPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 100 mA

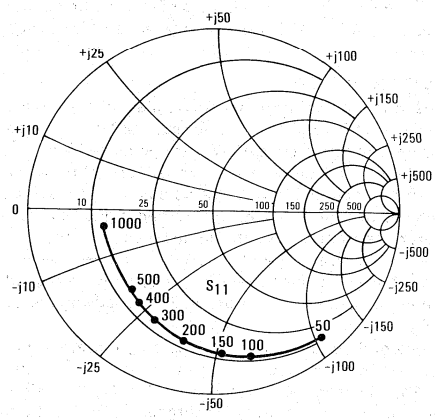


FIGURE 18 — S_{12}, REVERSE TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 100 mA

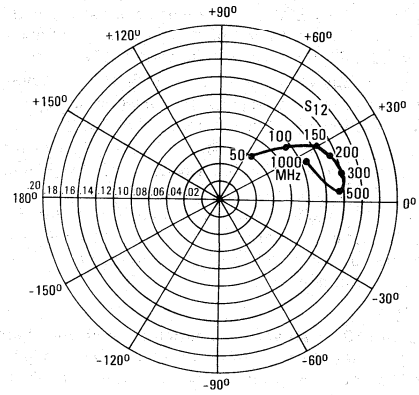


FIGURE 19 — S_{21}, FORWARD TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 100 mA

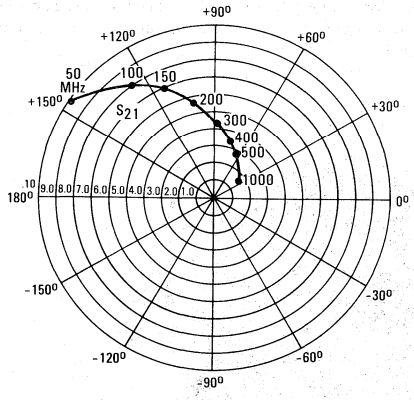
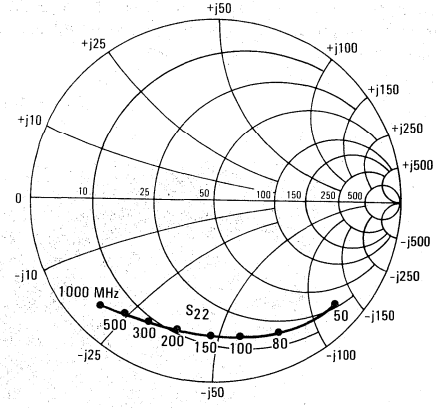


FIGURE 20 — S_{22}, OUTPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 100 mA



DESIGN CONSIDERATIONS

The MRF134 is a TMOS RF power N-Channel enhancement mode field-effect transistor (FET) designed especially for VHF power amplifier and oscillator applications. Motorola TMOS FETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V-groove vertical power FETs.

Motorola Application Note AN-211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of TMOS RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF134 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 9 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF134 was characterized at I_{DQ} = 50 mA, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF134 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC, and modulation systems. (See Figure 8.)

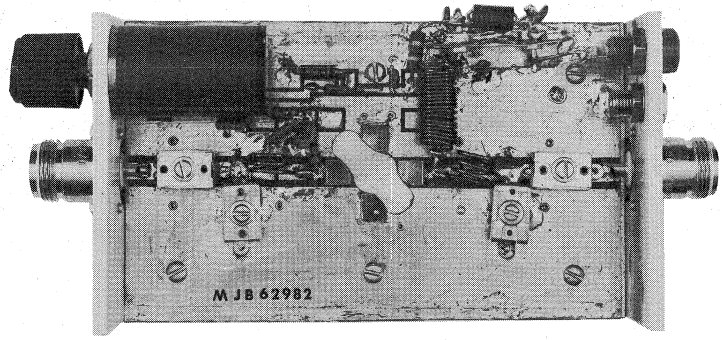
AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar VHF transistors are suitable for MRF134. See Motorola Application Note AN-721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of TMOS FETs helps ease the task of broadband network design. Both small signal scattering parameters and large signal impedances are provided. While the s-parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of TMOS power FETs.

RF power FETs are triode devices and, therefore, not unilateral. This, coupled with the very high gain of the MRF134, yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. The MRF134 was characterized with a 68-ohm input shunt loading resistor. Two port parameter stability analysis with the MRF134 s-parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN-215A for a discussion of two port network theory and stability.

Input resistive loading is not feasible in low noise applications. The MRF134 noise figure data was generated in a circuit with drain loading and a low loss input network.

FIGURE 21 — 150 MHz TEST CIRCUIT



MRF136
MRF136Y

The RF TMOS Line
RF Power Field-Effect Transistors
N-Channel Enhancement Mode TMOS

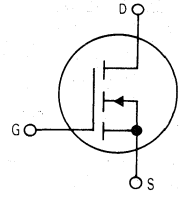
15 W, 30 W 2–400 MHz
N-CHANNEL
TMOS BROADBAND
RF POWER FETs

. . . designed for wideband large-signal amplifier and oscillator applications in the 2 to 400 MHz range, in either single ended or push-pull configuration.

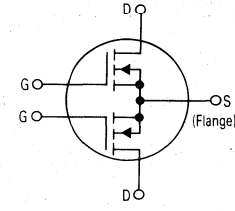
- Guaranteed 28 Volt, 150 MHz Performance
  MRF136
  Output Power = 15 Watts
  Narrowband Gain = 16 dB (Typ)
  Efficiency = 60% (Typical)
  MRF136Y
  Output Power = 30 Watts
  Broadband Gain = 14 dB (Typ)
  Efficiency = 54% (Typical)
- Small-Signal and Large-Signal Characterization
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR
- Space Saving Package For Push-Pull Circuit Applications — MRF136Y
- Excellent Thermal Stability, Ideally Suited For Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques

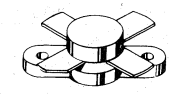
TMOS™

MRF136

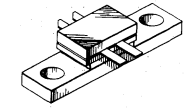


MRF136Y





MRF136
CASE 211-07



MRF136Y
CASE 319B-01

MAXIMUM RATINGS

Rating	Symbol	Value		Unit
		MRF136	MRF136Y	
Drain-Source Voltage	V_{DSS}	65	65	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	65	65	Vdc
Gate-Source Voltage	V_{GS}	±40		Vdc
Drain-Current — Continuous	I_D	2.5	5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	55 0.314	100 0.571	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150		°C
Operating Junction Temperature	T_J	200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
		MRF136	MRF136Y	
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.2	1.75	°C/W

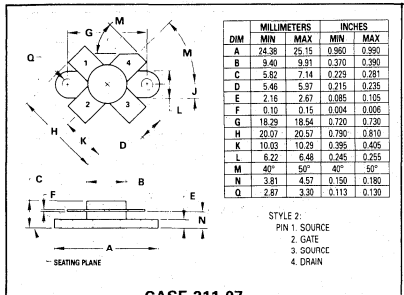
Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (NOTE 1)					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero-Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	2	mAdc
Gate-Source Leakage Current (V_{GS} = 40 V, V_{DS} = 0)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS (NOTE 1)					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 25 mA)	$V_{GS(th)}$	1	3	6	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 250 mA)	g_{fs}	250	400	—	mmhos
DYNAMIC CHARACTERISTICS (NOTE 1)					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	24	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	27	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	5.5	—	pF
FUNCTIONAL CHARACTERISTICS (NOTE 2)					
Noise Figure MRF136 (V_{DS} = 28 Vdc, I_D = 500 mA, f = 150 MHz)	NF	—	1	—	dB
Common Source Power Gain (Figure 1) MRF136 (V_{DD} = 28 Vdc, P_{out} = 15 W, f = 150 MHz, I_{DQ} = 25 mA)	G_{ps}	13	16	—	dB
Common Source Power Gain (Figure 2) MRF136Y (V_{DD} = 28 Vdc, P_{out} = 30 W, f = 150 MHz, I_{DQ} = 100 mA)	G_{ps}	12	14	—	dB
Drain Efficiency (Figure 1) MRF136 (V_{DD} = 28 Vdc, P_{out} = 15 W, f = 150 MHz, I_{DQ} = 25 mA)	η	50	60	—	%
Drain Efficiency (Figure 2) MRF136Y (V_{DD} = 28 Vdc, P_{out} = 30 W, f = 150 MHz, I_{DQ} = 100 mA)	η	50	54	—	%
Electrical Ruggedness (Figure 1) MRF136 (V_{DD} = 28 Vdc, P_{out} = 15 W, f = 150 MHz, I_{DQ} = 25 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			
Electrical Ruggedness (Figure 2) MRF136Y (V_{DD} = 28 Vdc, P_{out} = 30 W, f = 150 MHz, I_{DQ} = 100 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			

Notes: 1. For MRF136Y, each side measured separately.
2. For MRF136Y measured in push-pull configuration.

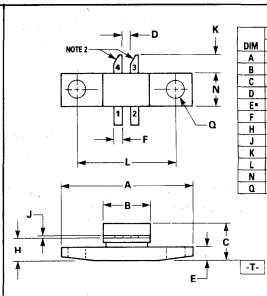
OUTLINE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	9.40	9.91	0.370	0.390
C	5.82	7.14	0.229	0.281
D	5.46	5.97	0.215	0.235
E	2.16	2.67	0.085	0.105
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	20.07	20.57	0.790	0.810
K	10.03	10.29	0.395	0.405
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.81	4.57	0.150	0.180
Q	2.87	3.30	0.113	0.130

STYLE 2:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

CASE 211-07

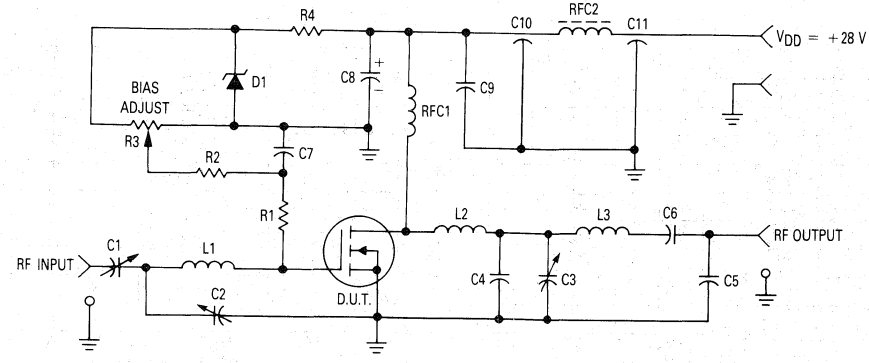


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.51	25.02	0.965	0.985
B	9.02	9.52	0.355	0.375
C	5.84	6.60	0.230	0.260
D	1.40	1.65	0.055	0.065
E*	2.69	2.94	0.106	0.116
F	1.4	1.65	0.055	0.065
H	4.06	4.31	0.160	0.170
J	0.10	0.15	0.004	0.006
K	3.05	3.55	0.120	0.140
L	18.42 BSC		0.725 BSC	
N	5.72	6.12	0.225	0.241
Q	3.18	3.42	0.125	0.135

STYLE 1:
PIN 1. GATE (INPUT)
2. GATE (INPUT)
3. DRAIN (OUTPUT)
4. DRAIN (OUTPUT)
SOURCE IS FLANGE

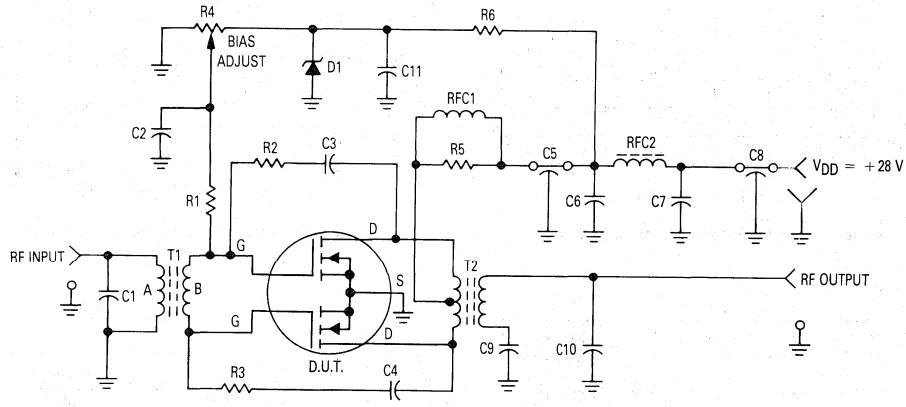
NOTES:
1. POSITIONAL TOLERANCE FOR Q HOLES.
⌖ | ⌀ 0.15 (0.006) Ⓜ | T | A Ⓜ | N Ⓜ
2. IDENTIFICATION NOTCH:
1.0 mm (0.04) MINIMUM x 45°.
3. DIMENSION D APPLIES 2 PLACES.
DIMENSION K APPLIES 2 PLACES.
DIMENSION Q APPLIES 2 PLACES.
DIMENSION F APPLIES 4 PLACES.
4. DIMENSIONS A AND N ARE DATUMS AND T IS A DATUM SURFACE.
5. DIMENSION B APPLIES TO LEAD FRAME AND Be0.
6. POSITIONAL TOLERANCE FOR F TERMINAL AND DIMENSION B:
⌖ | .38 (.015) Ⓜ | T | A Ⓜ | N Ⓜ
7. DIMENSIONING AND TOLERANCING PER Y14.5M, 1982.

CASE 319B-01



C1, C2 — Arco 406, 15–115 pF or Equivalent
C3 — Arco 404, 8–60 pF or Equivalent
C4 — 43 pF Mini-Unelco or Equivalent
C5 — 24 pF Mini-Unelco or Equivalent
C6 — 680 pF, 100 Mils Chip
C7 — 0.01 μF Ceramic
C8 — 100 μF, 40 V
C9 — 0.1 μF Ceramic
C10, C11 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener
L1 — 2 Turns, 0.29″ ID, #18 AWG, 0.10″ Long
L2 — 2 Turns, 0.23″ ID, #18 AWG, 0.10″ Long
L3 — 2-1/4 Turns, 0.29″ ID, #18 AWG, 0.125″ Long
RFC1 — 20 Turns, 0.30″ ID, #20 AWG Enamel Closewound
RFC2 — Ferroxcube VK-200 — 19/4B
R1 — 27 Ω, 1 W Thin Film
R2 — 10 kΩ, 1/4 W
R3 — 10 Turns, 10 kΩ
R4 — 1.8 kΩ, 1/2 W
Board Material — 0.062″ G10, 1 oz. Cu Clad, Double Sided

Figure 1. 150 MHz Test Circuit (MRF136)



C1 — 5 pF
C2, C3, C4, C6, C7, C9, C11 — 0.1 μF Ceramic
C5, C8 — 680 pF Feedthru
C10 — 15 pF
D1 — 1N4740 Motorola Zener
RFC1 — 17 Turns, #24 AWG Wound on R5
RFC2 — Ferroxcube VK-200-19/4B or Equivalent
R1 — 10 kΩ, 1/4 W
R2, R3 — 560 Ω, 1/2 W
R4 — 10 Turns, 10 kΩ
R5 — 56 kΩ, 1 W
R6 — 1.6 kΩ, 1/4 W
T1 — Primary Winding — 3 Turns #28 Enameled Wire.
— Secondary Winding — 2 Turns #28 Enameled Wire.
Both windings wound through a Fair/Rite Balun 65 core.
Part #2865002402.
T2 — 1:1 Transformer Wound Bifilar — 2 Turns Twisted Pair #24 Enameled Wire through a Indiana General Balun Q1 core. Part #18006-1-Q1. Primary winding center tapped.
Board Material — 0.062″ G10, 1 oz. Cu Clad, Double Sided

Figure 2. 30–150 MHz Test Circuit (MRF136Y)

MRF136

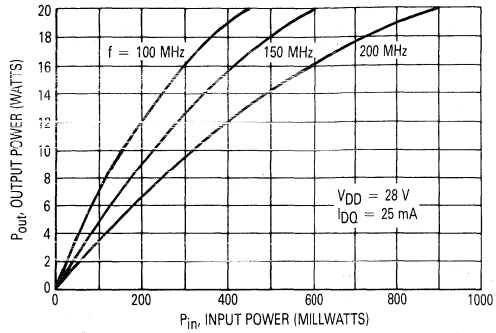


Figure 3. Output Power versus Input Power

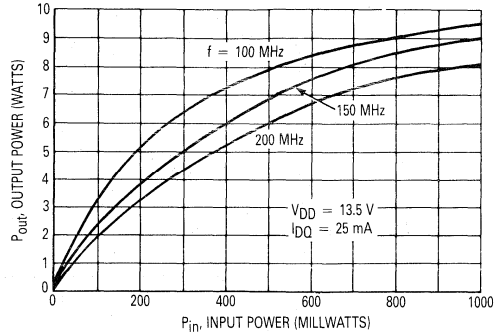


Figure 4. Output Power versus Input Power

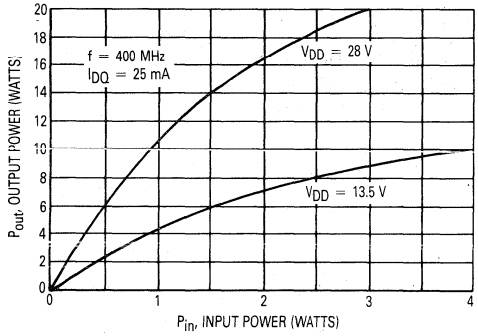


Figure 5. Output Power versus Input Power

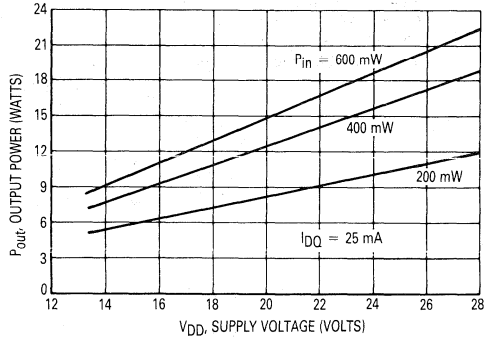


Figure 6. Output Power versus Supply Voltage
f = 100 MHz

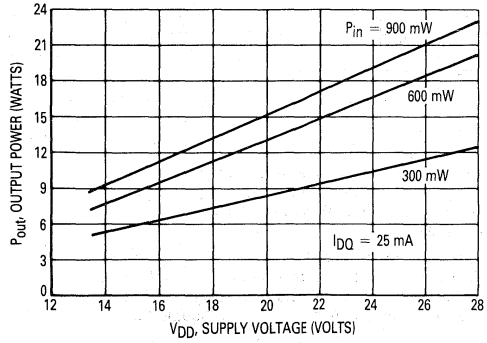


Figure 7. Output Power versus Supply Voltage
f = 150 MHz

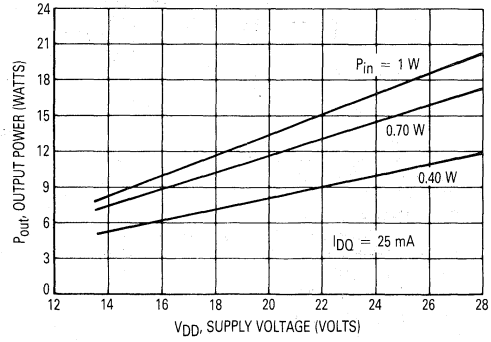


Figure 8. Output Power versus Supply Voltage
f = 200 MHz

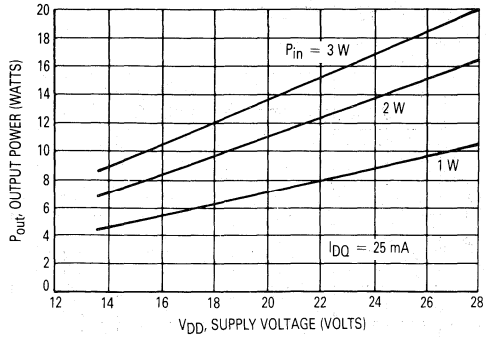


Figure 9. Output Power versus Supply Voltage
f = 400 MHz
MRF136

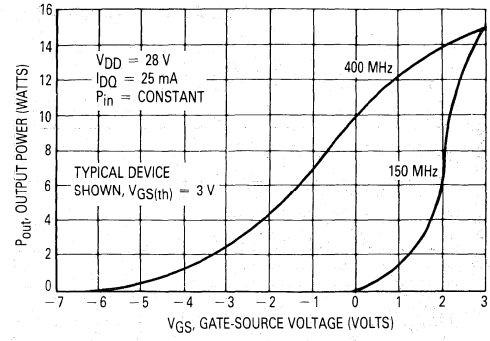


Figure 10. Output Power versus Gate Voltage
MRF136

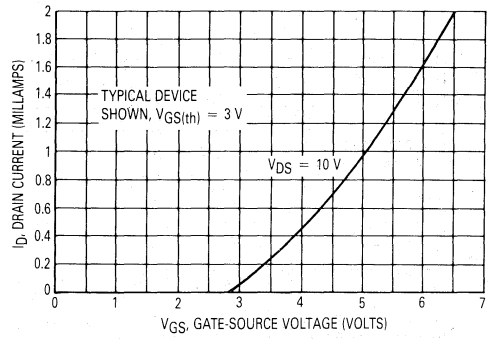


Figure 11. Drain Current versus Gate Voltage
(Transfer Characteristics)*
MRF136/MRF136Y

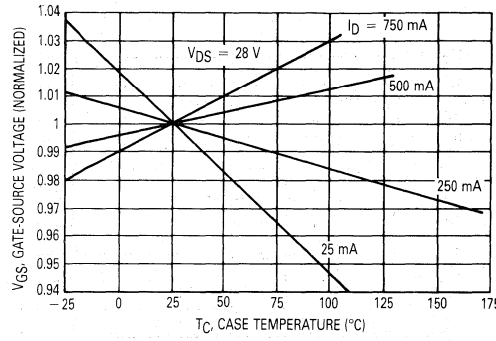


Figure 12. Gate-Source Voltage versus
Case Temperature*
MRF136/MRF136Y

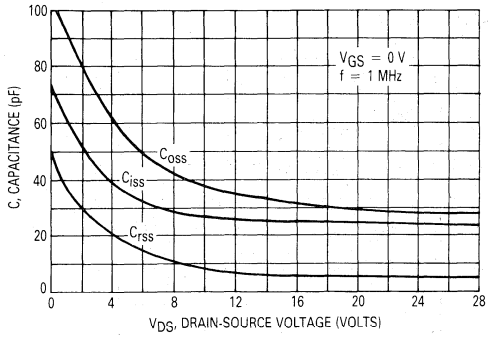


Figure 13. Capacitance versus Drain-Source Voltage*
MRF136/MRF136Y

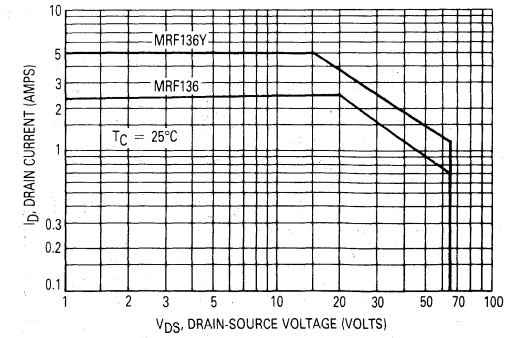


Figure 14. DC Safe Operating Area
MRF136/MRF136Y

*Data shown applies to MRF136 and each half of MRF136Y.

MRF136Y
TYPICAL PERFORMANCE IN BROADBAND TEST CIRCUIT
(Refer to Figure 2)

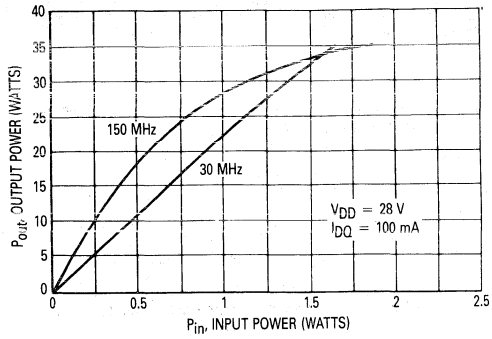


Figure 15. Output Power versus Input Power

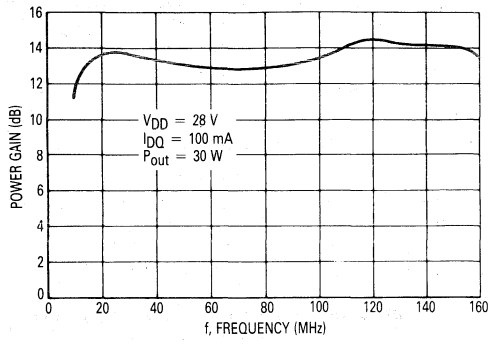


Figure 16. Power Gain versus Frequency

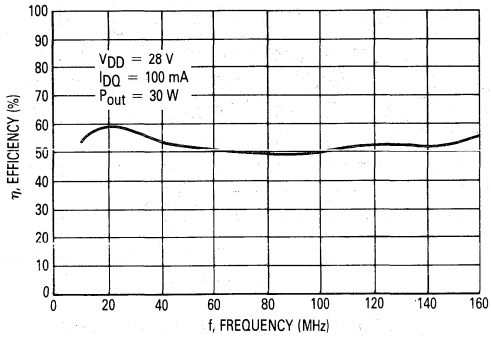


Figure 17. Drain Efficiency versus Frequency

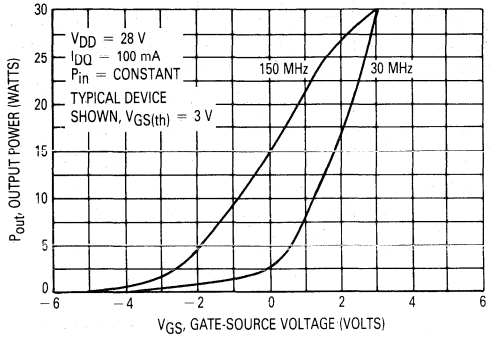


Figure 18. Output Power versus Gate Voltage

TYPICAL 400 MHz PERFORMANCE

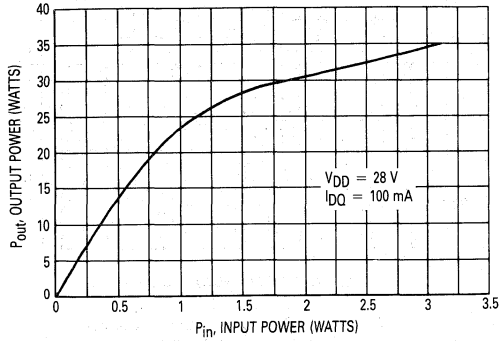


Figure 19. Output Power versus Input Power
f = 400 MHz

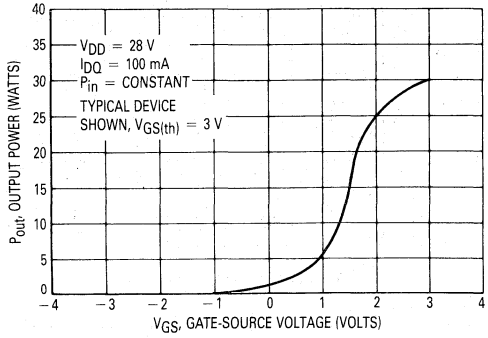
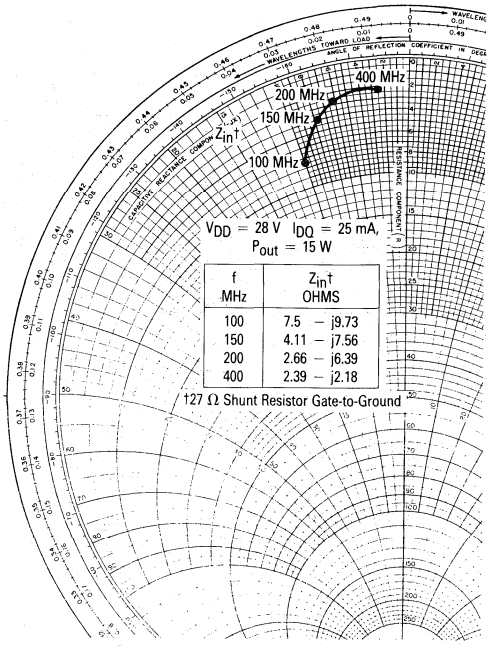


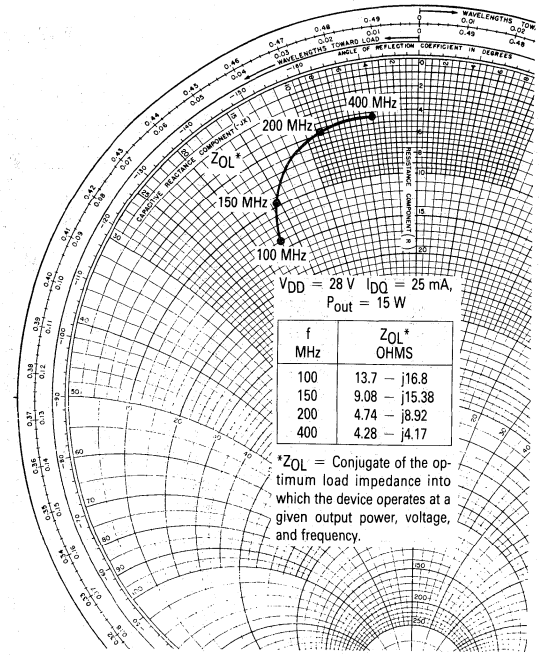
Figure 20. Output Power versus Gate Voltage
f = 400 MHz



f MHz	Z_{in}† OHMS
100	7.5 − j9.73
150	4.11 − j7.56
200	2.66 − j6.39
400	2.39 − j2.18

†27 Ω Shunt Resistor Gate-to-Ground

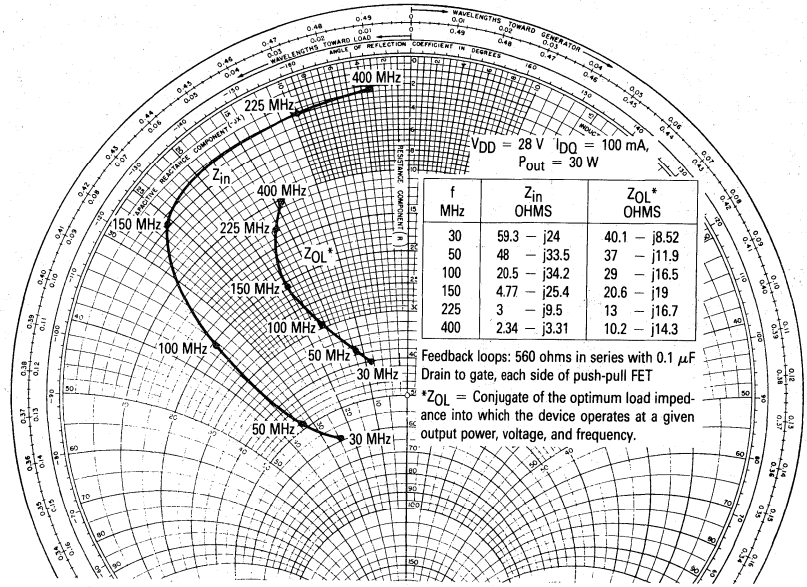
Figure 21. Large-Signal Series Equivalent Input Impedance, Z_{in}† MRF136



f MHz	Z_{OL}* OHMS
100	13.7 − j16.8
150	9.08 − j15.38
200	4.74 − j8.92
400	4.28 − j4.17

*Z_{OL} = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

Figure 22. Large-Signal Series Equivalent Output Impedance, Z_{OL}* MRF136



f MHz	Z_{in} OHMS	Z_{OL}* OHMS
30	59.3 − j24	40.1 − j8.52
50	48 − j33.5	37 − j11.9
100	20.5 − j34.2	29 − j16.5
150	4.77 − j25.4	20.6 − j19
225	3 − j9.5	13 − j16.7
400	2.34 − j3.31	10.2 − j14.3

Feedback loops: 560 ohms in series with 0.1 μF Drain to gate, each side of push-pull FET

*Z_{OL} = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

Figure 23. Input and Output Impedance MRF136Y

MRF136

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
2.0	0.988	-11	41.19	173	0.006	67	0.729	-12
5.0	0.970	-27	40.07	164	0.014	62	0.720	-31
10	0.923	-52	35.94	149	0.026	54	0.714	-58
20	0.837	-88	27.23	129	0.040	36	0.690	-96
30	0.784	-111	20.75	117	0.046	27	0.684	-118
40	0.751	-125	16.49	108	0.048	22	0.680	-131
50	0.733	-135	13.41	103	0.050	19	0.679	-139
60	0.720	-142	11.43	99	0.050	16	0.678	-145
70	0.709	-147	9.871	96	0.050	14	0.679	-149
80	0.707	-152	8.663	93	0.051	13	0.683	-153
90	0.706	-155	7.784	91	0.051	13	0.682	-155
100	0.708	-157	7.008	88	0.051	13	0.680	-157
110	0.711	-159	6.435	86	0.051	14	0.681	-158
120	0.714	-161	5.899	85	0.051	15	0.682	-159
130	0.717	-163	5.439	82	0.052	16	0.684	-160
140	0.720	-164	5.068	80	0.052	17	0.684	-161
150	0.723	-165	4.709	80	0.052	18	0.686	-161
160	0.727	-166	4.455	78	0.052	18	0.690	-161
170	0.732	-167	4.200	77	0.052	18	0.694	-162
180	0.735	-168	3.967	75	0.052	19	0.699	-162
190	0.738	-169	3.756	74	0.052	19	0.703	-163
200	0.740	-170	3.545	73	0.052	20	0.706	-163
225	0.746	-171	3.140	69	0.053	22	0.717	-163
250	0.742	-172	2.783	67	0.053	25	0.724	-163
275	0.744	-173	2.540	64	0.054	27	0.724	-163
300	0.751	-174	2.323	60	0.055	29	0.736	-163
325	0.757	-175	2.140	58	0.058	32	0.749	-163
350	0.760	-176	1.963	54	0.059	35	0.758	-163
375	0.762	177	1.838	52	0.062	38	0.768	-163
400	0.774	-179	1.696	50	0.065	41	0.783	-163
425	0.775	-179	1.590	48	0.068	43	0.793	-163
450	0.781	+179	1.493	46	0.071	46	0.805	-163
475	0.787	+177	1.415	43	0.074	47	0.813	-164
500	0.792	+176	1.332	40	0.079	48	0.825	-164
525	0.797	+175	1.259	38	0.083	50	0.831	-164
550	0.801	+175	1.185	37	0.088	51	0.843	-164
575	0.810	+174	1.145	36	0.094	52	0.855	-164
600	0.816	+173	1.091	34	0.101	52	0.869	-165
625	0.818	+171	1.041	32	0.106	53	0.871	-165
650	0.825	+170	0.994	30	0.112	53	0.884	-165
675	0.834	+169	0.962	29	0.119	53	0.890	-165
700	0.837	+168	0.922	27	0.127	53	0.906	-166
725	0.836	+167	0.879	25	0.133	52	0.909	-167
750	0.841	+166	0.838	25	0.140	53	0.917	-167
775	0.844	+165	0.824	24	0.148	52	0.933	-167
800	0.846	+163	0.785	21	0.154	50	0.941	-168

Figure 24. Common Source Scattering Parameters
V_{DS} = 28 V, I_D = 0.5 A

MRF136

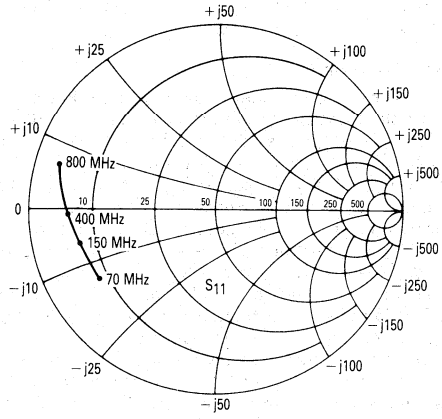


Figure 25. S_{11}, Input Reflection Coefficient versus Frequency
V_{DS} = 28 V I_D = 0.5 A

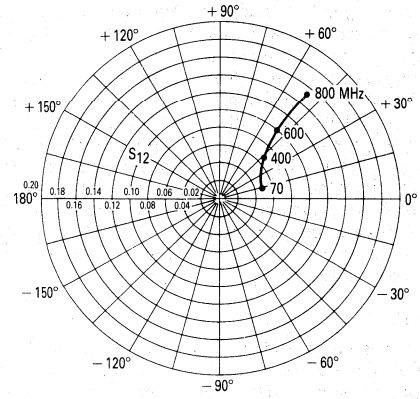


Figure 26. S_{12}, Reverse Transmission Coefficient versus Frequency
V_{DS} = 28 V I_D = 0.5 A

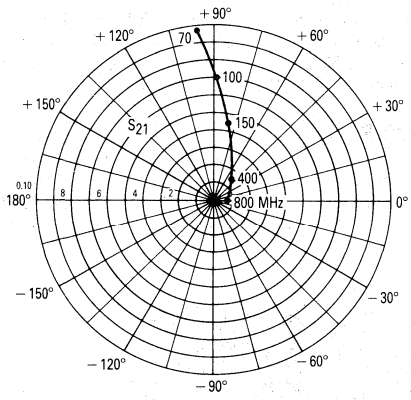


Figure 27. S_{21}, Forward Transmission Coefficient versus Frequency
V_{DS} = 28 V I_D = 0.5 A

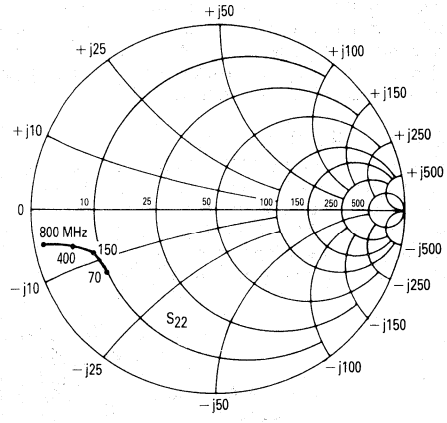


Figure 28. S_{22}, Output Reflection Coefficient versus Frequency
V_{DS} = 28 V I_D = 0.5 A

3

DESIGN CONSIDERATIONS

The MRF136 and MRF136Y are TMOS RF power N-Channel enhancement mode field-effect transistors (FETs) designed especially for HF and VHF power amplifier applications. Motorola TMOS FETs feature planar design for optimum manufacturability.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of TMOS RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF136 and MRF136Y are enhancement mode FETs and, therefore, do not conduct when drain voltage is applied without gate bias. A positive gate voltage causes drain current to flow (see Figure 11). RF power FETs require forward bias for optimum gain and power output. A Class AB condition with quiescent drain current (I_{DQ}) in the 25–100 mA range is sufficient for many applications. For special requirements such as linear amplification, I_{DQ} may have to be adjusted to optimize the critical parameters.

The MOS gate is a dc open circuit. Since the gate bias circuit does not have to deliver any current to the FET, a simple resistive divider arrangement may sometimes suffice for this function. Special applications may require more elaborate gate bias systems.

GAIN CONTROL

Power output of the MRF136 and MRF136Y may be controlled from rated values down to the milliwatt region (>20 dB reduction in power output with constant input power) by varying the dc gate voltage. This feature, not available in bipolar RF power devices, facilitates the incorporation of manual gain control, AGC/ALC, and modulation schemes into system designs. A full range of power output control may require dc gate voltage excursions into the negative region.

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for the MRF136 and MRF136Y. See Motorola Application Note AN721, Impedance Matching Networks Applied to RF Power Transistors. Both small signal scattering parameters (MRF136 only) and large signal impedance parameters are provided. Large signal impedances should be used for network designs wherever possible. While the s parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is particularly useful at frequencies outside those presented in the large signal impedance plots.

RF power FETs are triode devices and are therefore not unilateral. This, coupled with their very high gain, yields a device capable of self oscillation. Stability may be achieved using techniques such as drain loading, input shunt resistive loading, or feedback. S parameter stability analysis can provide useful information in the selection of loading and/or feedback to insure stable operation. The MRF136 was characterized with a 27 ohm input shunt loading resistor, while the MRF136Y was characterized with a resistive feedback loop around each of its two active devices.

For further discussion of RF amplifier stability and the use of two port parameters in RF amplifier design, see Motorola Application Note AN215A on page 6-204 in the RF Device Data (DL110 Rev 1).

LOW NOISE OPERATION

Input resistive loading will degrade noise performance, and noise figure may vary significantly with gate driving impedance. A low loss input matching network with its gate impedance optimized for lowest noise is recommended.

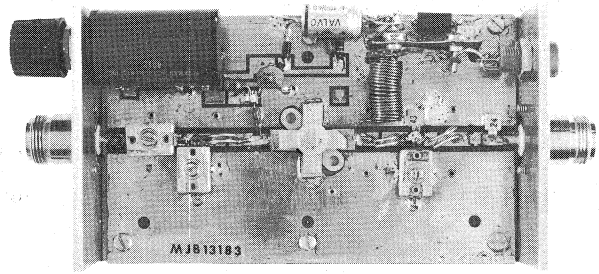


Figure 29. MRF136 Test Circuit

MRF137

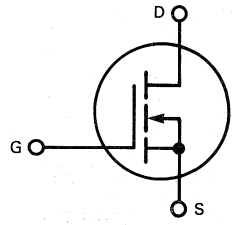
The RF TMOS Line

N-CHANNEL ENHANCEMENT-MODE
TMOS RF POWER FIELD-EFFECT TRANSISTOR

. . . designed for wideband large-signal output and driver stages in the 2.0 to 400 MHz range.

- Guaranteed 28 Volt, 150 MHz Performance
  Output Power = 30 Watts
  Minimum Gain = 13 dB
  Efficiency = 60% (Typical)
- Small-Signal and Large-Signal Characterization
- Typical Performance at 400 MHz, 28 Vdc, 30 W
  Output = 7.7 dB Gain
- 100% Tested for Load Mismatch at All Phase Angles with 30:1 VSWR
- Low Noise Figure — 1.5 dB (Typ) at 1.0 A, 150 MHz
- Excellent Thermal Stability, Ideally Suited for Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques

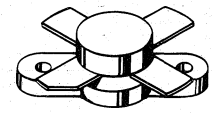
TMOS™

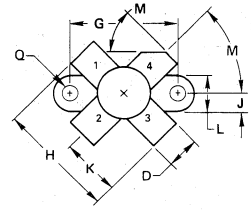


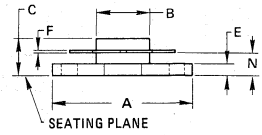
30 W 2.0-400 MHz

N-CHANNEL TMOS
BROADBAND RF POWER

FET







STYLE 2:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	9.40	9.91	0.370	0.390
C	5.82	7.14	0.229	0.281
D	5.46	5.97	0.215	0.235
E	2.16	2.67	0.085	0.105
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	20.07	20.57	0.790	0.810
K	10.03	10.29	0.395	0.405
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.81	4.57	0.150	0.180
Q	2.87	3.30	0.113	0.130

CASE 211-07

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate-Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	5.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 0.571	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

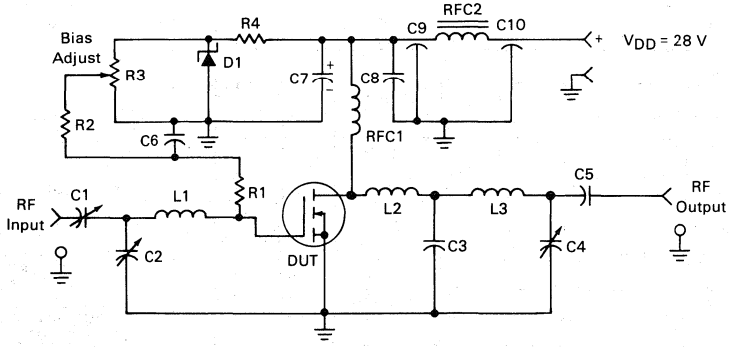
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 10 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	4.0	mAdc
Gate-Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 25 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 500 mA)	g_{fs}	500	750	—	mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	48	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	54	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	11	—	pF
FUNCTIONAL CHARACTERISTICS					
Noise Figure (V_{DS} = 28 Vdc, I_D = 1.0 A, f = 150 MHz)	NF	—	1.5	—	dB
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 30 W, I_{DQ} = 25 mA) f = 150 MHz (Figure 1)	G_{ps}	13	16	—	dB
f = 400 MHz (Figure 14)		—	7.7	—	
Drain Efficiency (Figure 1) (V_{DD} = 28 Vdc, P_{out} = 30 W, f = 150 MHz, I_{DQ} = 25 mA)	η	50	60	—	%
Electrical Ruggedness (Figure 1) (V_{DD} = 28 Vdc, P_{out} = 30 W, f = 150 MHz, I_{DQ} = 25 mA, VSWR 30:1 at All Phase Angles)	ψ	No Degradation in Output Power			

FIGURE 1 — 150 MHz TEST CIRCUIT



C1 — Arco 406, 15–115 pF, or equivalent
C2 — Arco 403, 3.0–35 pF, or equivalent
C3 — 56 pF Mini-Unleco, or equivalent
C4 — Arco 404, 8.0–60 pF, or equivalent
C5 — 680 pF, 100 Mils Chip
C6 — 0.01 μF, 100 V, Disc Ceramic
C7 — 100 μF, 40 V
C8 — 0.1 μF, 50 V, Disc Ceramic
C9, C10 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener

L1 — 2 Turns, 0.29" ID, #18 AWG Enamel, Closewound
L2 — 1¼ Turns, 0.2" ID, #18 AWG Enamel, Closewound
L3 — 2 Turns, 0.2" ID, #18 AWG Enamel, Closewound
RFC1 — 20 Turns, 0.30" ID, #20 AWG Enamel, Closewound
RFC2 — Ferroxcube VK-200 — 19/4B
R1 — 10 kΩ, ½ W Thin Film
R2 — 10 kΩ, ¼ W
R3 — 10 Turns, 10 kΩ
R4 — 1.8 kΩ, ½ W
Board — G10, 62 Mils

FIGURE 2 — OUTPUT POWER versus INPUT POWER

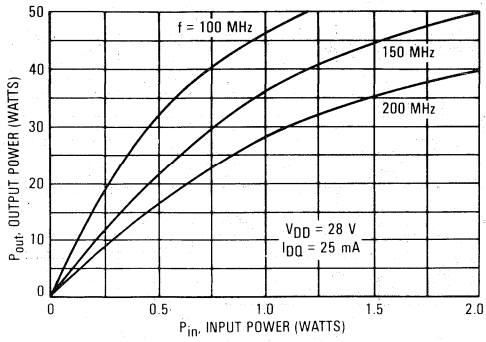


FIGURE 3 — OUTPUT POWER versus INPUT POWER

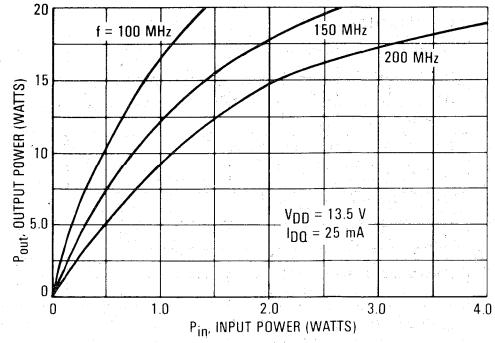


FIGURE 4 — OUTPUT POWER versus INPUT POWER

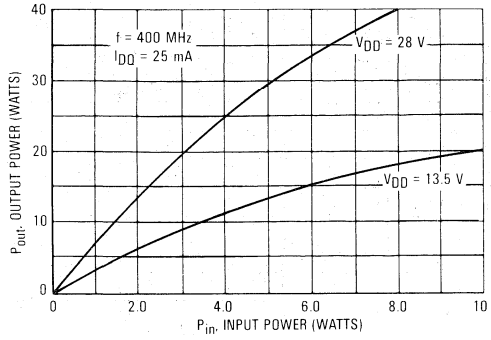


FIGURE 5 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 100 MHz

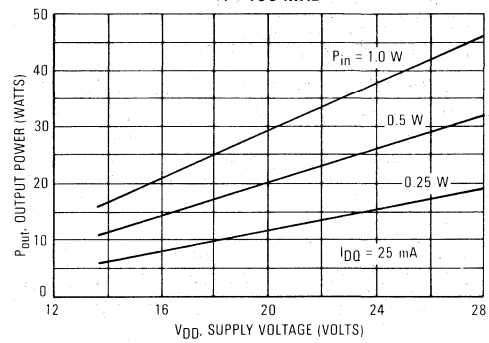


FIGURE 6 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 150 MHz

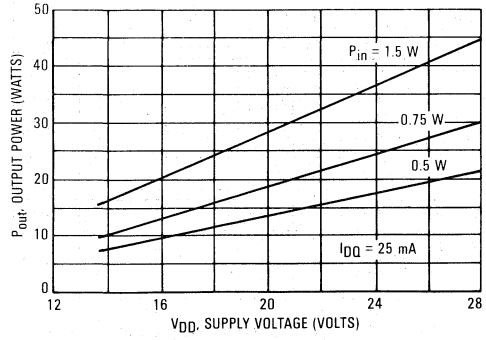
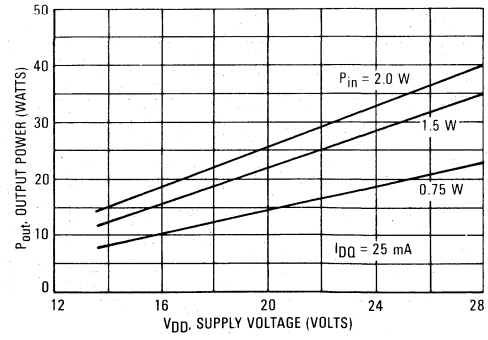


FIGURE 7 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 200 MHz



3

FIGURE 8 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 400 MHz

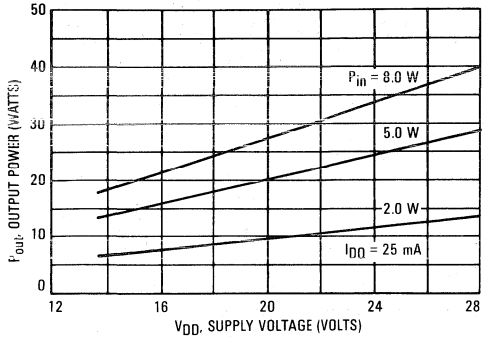


FIGURE 9 — OUTPUT POWER versus GATE VOLTAGE

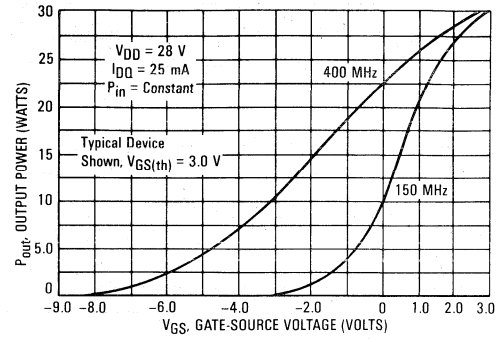


FIGURE 10 — DRAIN CURRENT versus GATE VOLTAGE
(TRANSFER CHARACTERISTICS)

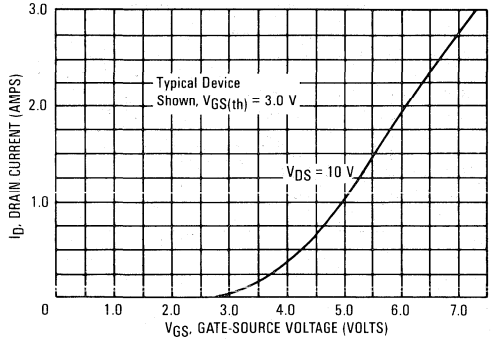


FIGURE 11 — GATE SOURCE VOLTAGE versus
CASE TEMPERATURE

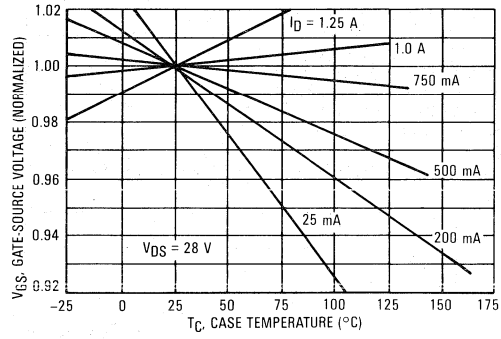


FIGURE 12 — CAPACITANCE versus
DRAIN-SOURCE VOLTAGE

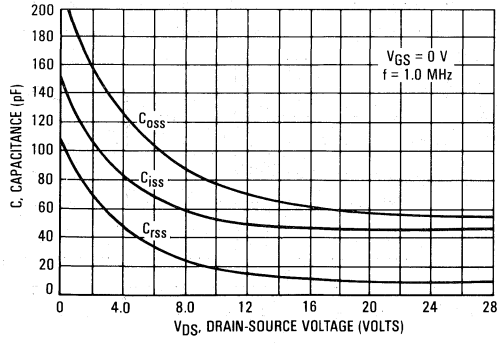


FIGURE 13 — DC SAFE OPERATING AREA

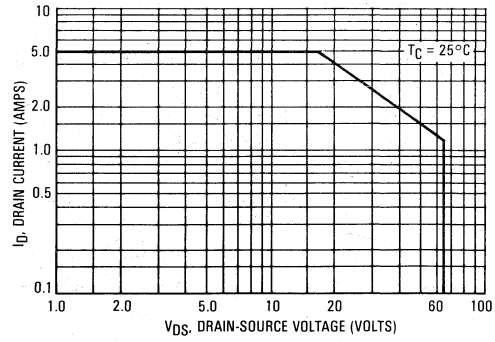
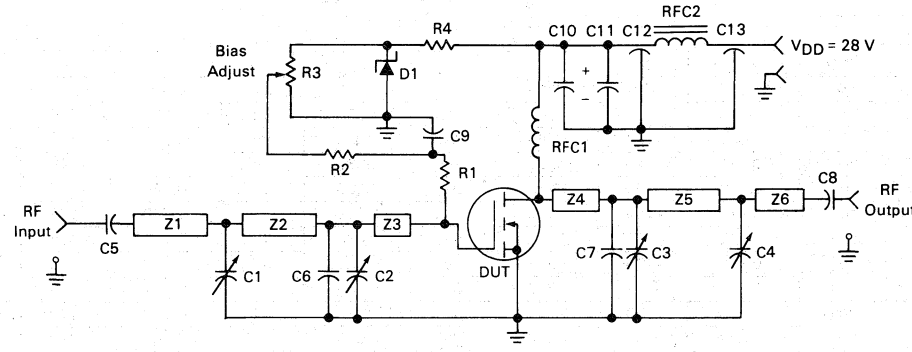
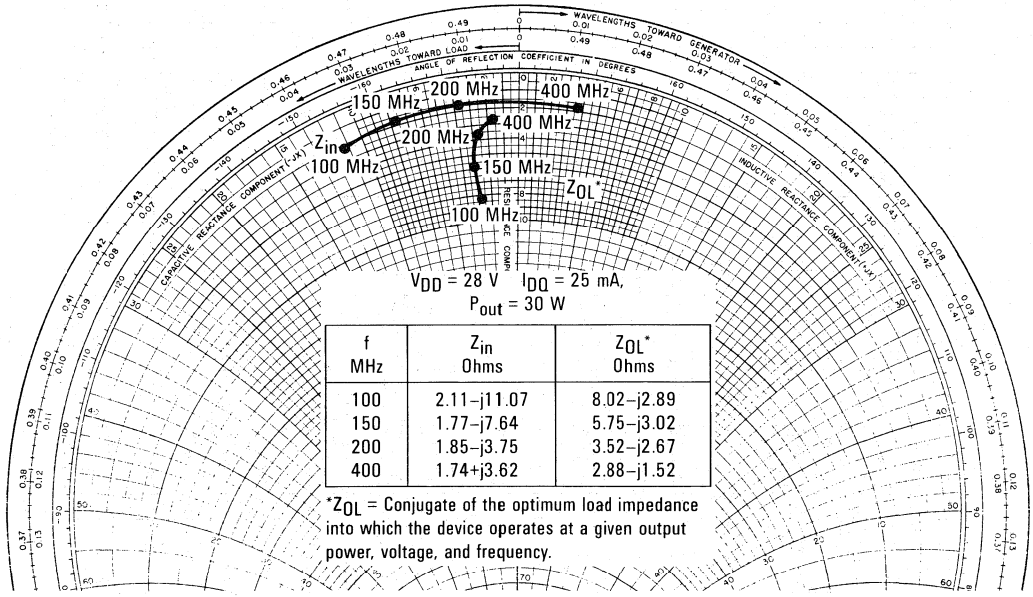


FIGURE 14 — 400 MHz TEST CIRCUIT



C1, C2, C3, C4 — 0–20 pF Johanson, or equivalent
C5, C8 — 270 pF, 100 Mil Chip
C6, C7 — 24 pF Mini-Unleco, or equivalent
C9 — 0.01 μF, 100 V, Disc Ceramic
C10 — 100 μF, 40 V
C11 — 0.1 μF, 50 V, Disc Ceramic
C12, C13 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener
R1, R2 — 10 kΩ, ¼ W
R3 — 10 Turns, 10 kΩ
R4 — 1.8 kΩ, ½ W
Z1 — 2.9" × 0.166" Microstrip
Z2, Z4 — 0.35" × 0.166" Microstrip
Z3 — 0.40" × 0.166" Microstrip
Z5 — 1.05" × 0.166" Microstrip
Z6 — 1.9" × 0.166" Microstrip
RFC1 — 6 Turns, 0.300" ID, #20 AWG Enamel, Closewound
RFC2 — Ferroxcube VK-200 — 19/4B
Board — Glass Teflon, 62 Mils

FIGURE 15 — LARGE-SIGNAL SERIES EQUIVALENT INPUT AND OUTPUT IMPEDANCE, Z_{in}, Z_{OL}*



f MHz	Z_{in} Ohms	Z_{OL}* Ohms
100	2.11–j11.07	8.02–j2.89
150	1.77–j7.64	5.75–j3.02
200	1.85–j3.75	3.52–j2.67
400	1.74+j3.62	2.88–j1.52

*Z_{OL} = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

FIGURE 16 — COMMON SOURCE SCATTERING PARAMETERS
50 Ω SYSTEM
V_{DS} = 28 V, I_D = 0.75 A

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
2.0	0.977	-32	59.48	163	0.011	67	0.661	-36
5.0	0.919	-70	48.67	142	0.024	44	0.692	-78
10	0.852	-109	33.50	122	0.032	29	0.747	-117
20	0.817	-140	19.05	106	0.037	16	0.768	-146
30	0.814	-153	13.11	99	0.038	14	0.774	-157
40	0.811	-159	9.88	95	0.038	13	0.782	-162
50	0.812	-164	7.98	92	0.038	12	0.787	-165
60	0.813	-166	6.66	89	0.038	12	0.787	-168
70	0.815	-168	5.708	86	0.038	11	0.787	-169
80	0.816	-170	5.003	84	0.038	11	0.787	-170
90	0.817	-171	4.560	83	0.038	12	0.787	-171
100	0.817	-172	4.170	81	0.039	13	0.787	-172
110	0.818	-173	3.670	80	0.039	13	0.788	-172
120	0.820	-173	3.420	79	0.039	13	0.788	-173
130	0.821	-173	3.170	79	0.039	13	0.788	-173
140	0.822	-174	2.980	78	0.039	13	0.788	-173
150	0.823	-175	2.826	77	0.039	14	0.788	-173
160	0.824	-175	2.650	76	0.039	14	0.790	-174
170	0.825	-176	2.438	75	0.039	14	0.792	-174
180	0.827	-176	2.325	73	0.039	15	0.793	-174
190	0.829	-177	2.175	72	0.039	16	0.796	-174
200	0.831	-177	2.084	71	0.039	16	0.799	-174
225	0.836	-178	1.824	69	0.039	18	0.805	-174
250	0.846	-178	1.621	66	0.039	21	0.816	-174
275	0.853	-179	1.462	64	0.039	23	0.822	-174
300	0.853	-179	1.319	61	0.040	25	0.833	-174
325	0.856	-179	1.194	59	0.040	27	0.828	-174
350	0.857	+179	1.089	56	0.040	30	0.842	-174
375	0.861	+179	1.014	54	0.042	32	0.849	-174
400	0.865	+178	0.927	51	0.043	35	0.856	-174
425	0.875	+178	0.876	49	0.045	37	0.866	-174
450	0.881	+178	0.810	46	0.046	40	0.870	-174
475	0.886	+177	0.755	44	0.046	43	0.875	-174
500	0.887	+177	0.694	41	0.051	43	0.888	-174
525	0.888	+176	0.677	39	0.052	43	0.890	-174
550	0.896	+176	0.625	36	0.055	45	0.898	-174
575	0.907	+175	0.603	34	0.058	45	0.913	-174
600	0.910	+175	0.585	32	0.061	45	0.918	-174
625	0.910	+174	0.563	30	0.065	45	0.945	-174
650	0.920	+174	0.543	28	0.069	46	0.952	-174
675	0.938	+173	0.533	26	0.074	47	0.974	-174
700	0.943	+171	0.515	24	0.078	47	0.958	-176
725	0.934	+170	0.491	22	0.079	46	0.953	-177
750	0.940	+170	0.475	22	0.084	48	0.943	-177
775	0.953	+169	0.477	21	0.090	48	0.957	-177
800	0.959	+168	0.467	17	0.093	48	0.957	-179

FIGURE 17 — S_{11}, INPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 0.75 A

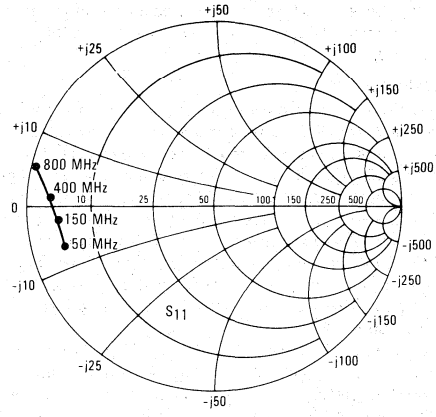


FIGURE 18 — S_{12}, REVERSE TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 0.75 A

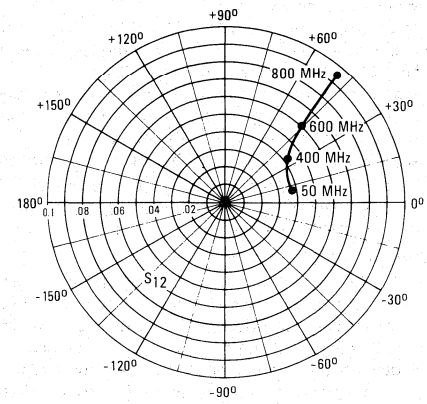


FIGURE 19 — S_{21}, FORWARD TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 0.75 A

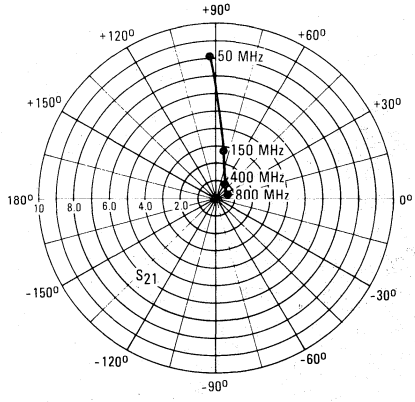
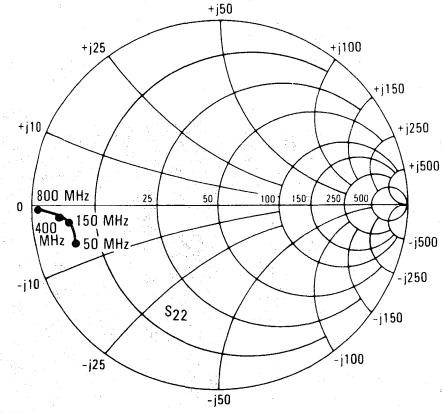


FIGURE 20 — S_{22}, OUTPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 0.75 A



3

DESIGN CONSIDERATIONS

The MRF137 is a TMOS RF power N-Channel enhancement mode field-effect transistor (FET) designed especially for VHF power amplifier applications. Motorola TMOS FETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V-groove vertical power FETs.

Motorola Application Note AN-211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of TMOS RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF137 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 10 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF137 was characterized at I_{DQ} = 25 mA, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

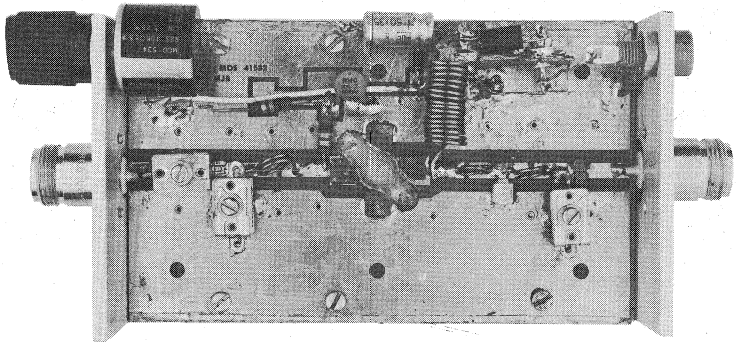
Power output of the MRF137 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC, and modulation systems. (See Figure 9.)

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar VHF transistors are suitable for MRF137. See Motorola Application Note AN-721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of TMOS FETs helps ease the task of broadband network design. Both small signal scattering parameters and large signal impedances are provided. While the s-parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of TMOS power FETs.

RF power FETs are triode devices and, therefore, not unilateral. This, coupled with the very high gain of the MRF137, yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. Two port parameter stability analysis with the MRF137 s-parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN-215A for a discussion of two port network theory and stability.

FIGURE 21 — 150 MHz TEST CIRCUIT



MRF138

The RF TMOS Line

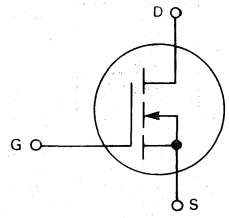
N-CHANNEL ENHANCEMENT-MODE
TMOS RF POWER FIELD-EFFECT TRANSISTOR

. . . designed for power amplifier applications in industrial, commercial and amateur radio equipment to 175 MHz.

- Superior High Order IMD
- Specified 28 Volts, 30 MHz Characteristics

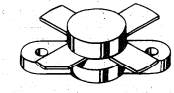
  Output Power = 30 Watts
  Power Gain = 17 dB (Typ)
  Efficiency = 40% (Typ)
- $IMD_{(d3)}$ (30 W PEP) = –30 dB (Typ)
- $IMD_{(d11)}$ (30 W PEP) = –60 dB (Typ)
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR

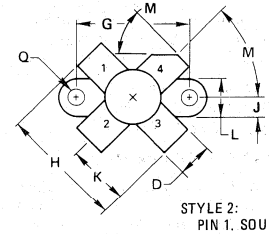
TMOS™



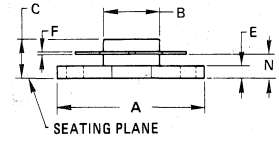
30 W 2.0–175 MHz

N-CHANNEL TMOS
LINEAR RF POWER
FET





STYLE 2:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	9.40	9.91	0.370	0.390
C	5.82	7.14	0.229	0.281
D	5.46	5.97	0.215	0.235
E	2.16	2.67	0.085	0.105
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	20.07	20.57	0.790	0.810
K	10.03	10.29	0.395	0.405
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.81	4.57	0.150	0.180
Q	2.87	3.30	0.113	0.130

CASE 211-07

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate-Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	6.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	115 0.66	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.52	°C/W

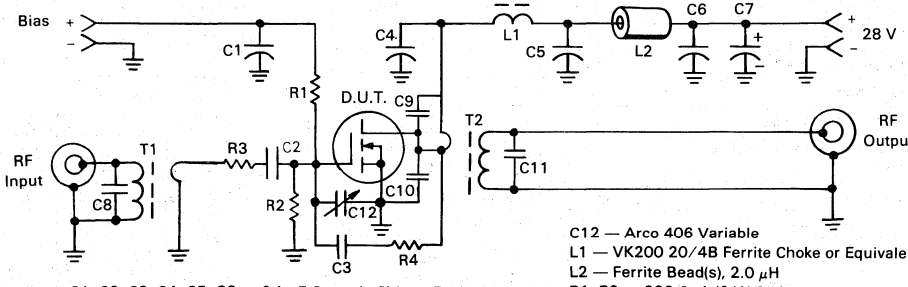
Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 10 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	5.0	mAdc
Gate-Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 10 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V, I_D = 2.5 A)	$V_{DS(on)}$	—	—	2.5	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 2.5 A)	g_{fs}	0.8	1.2	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}	—	55	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	70	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	14	—	pF
FUNCTIONAL TESTS (SSB)					
Common Source Amplifier Power Gain (V_{DD} = 28 V, P_{out} = 30 W (PEP), I_{DQ} = 100 mA) (30 MHz) (Fig. 1) (150 MHz) (Fig. 6)	G_{ps}	— —	17 14	— —	dB
Drain Efficiency (Figure 1) (V_{DD} = 28 V, f = 30 MHz, I_{DQ} = 100 mA) (30 W PEP) (30 W CW)	η	— —	40 50	— —	%
Intermodulation Distortion (Figure 1) (V_{DD} = 28 V, P_{out} = 30 W (PEP), f = 30; 30.001 MHz, I_{DQ} = 100 mA)	$IMD_{(d3)}$ $IMD_{(d11)}$	— —	-30 -60	— —	dB
Load Mismatch (Figure 1) (V_{DD} = 28 V, P_{out} = 30 W (PEP), f = 30; 30.001 MHz, I_{DQ} = 100 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			
CLASS A PERFORMANCE					
Intermodulation Distortion (1) and Power Gain (V_{DD} = 28 V, P_{out} = 10 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 1.0 A)	G_{PS} $IMD_{(d3)}$ $IMD_{(d9-13)}$	— — —	20 -50 -70	— — —	dB

(1) To MIL-STD-1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.

FIGURE 1 — 2-50 MHz BROADBAND TEST CIRCUIT



C1, C2, C3, C4, C5, C6 — 0.1 μF Ceramic Chip or Equivalent
C7 — 10 μF, 100 V Electrolytic
C8 — 10 pF Dipped Mica
C9 — 68 pF Dipped Mica
C10, C11 — 47 pF Dipped Mica
C12 — Arco 406 Variable
L1 — VK200 20/4B Ferrite Choke or Equivalent (3.0 μH)
L2 — Ferrite Bead(s), 2.0 μH
R1, R2 — 200 Ω, 1/2 W Carbon
R3 — 2.2 Ω, 1/2 W Carbon
R4 — 330 Ω, 1.0 W Carbon
T1 — 4:1 Impedance Transformer
T2 — 1:4 Impedance Transformer

FIGURE 2 — POWER GAIN versus FREQUENCY

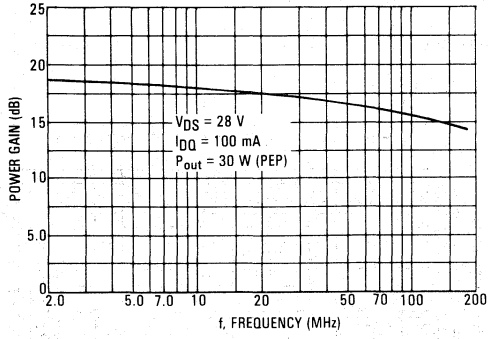


FIGURE 3 — OUTPUT POWER versus INPUT POWER

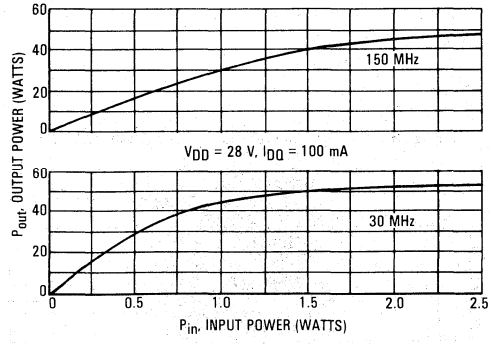


FIGURE 4 — IMD versus P_{out}

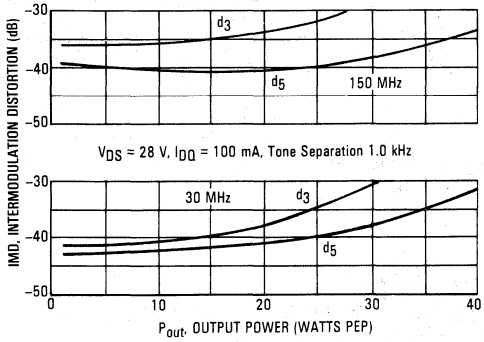


FIGURE 5 — COMMON SOURCE UNITY CURRENT GAIN FREQUENCY versus DRAIN CURRENT

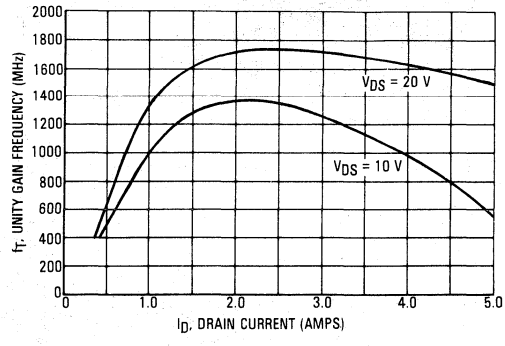
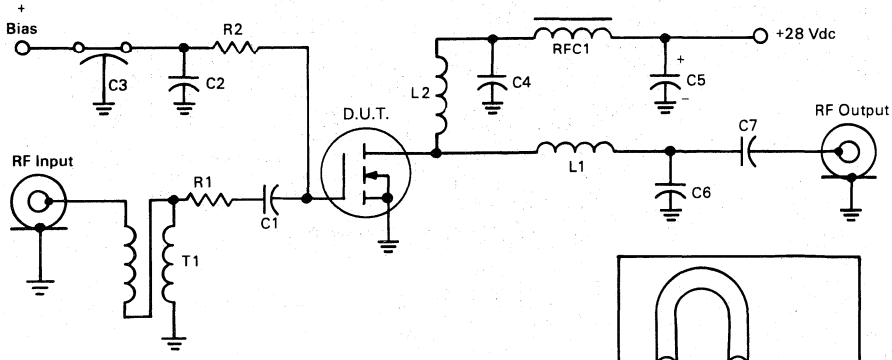


FIGURE 6 — 150 MHz TEST CIRCUIT



C1 — 91 pF Unelco Type MCM 01/010
C2, C4 — 0.1 μF Erie Red Cap
C3 — Allen Bradley 680 pF Feed Thru
C5 — 1.0 μF, 50 Vdc Electrolytic
C6 — Arco 402 Varible
C7 — Arco 404 Variable
L1 — 2 Turns # 18 AWG, 5/16″ ID

L2 — 4 Turns # 18 AWG, 5/16″ ID
R1 = 1.0 Ohm, 1/4 W Carbon
R2 — 2000 Ohm, 1/4 W Carbon
RFC1 — VK200 21/4B
T1 — 4:1 Transformer, 1.75″ Subminiature Coaxial Cable

T1 — 4:1 Impedance Ratio Transformer, Line Impedance = 25 Ω

FIGURE 7 — GATE VOLTAGE versus DRAIN CURRENT

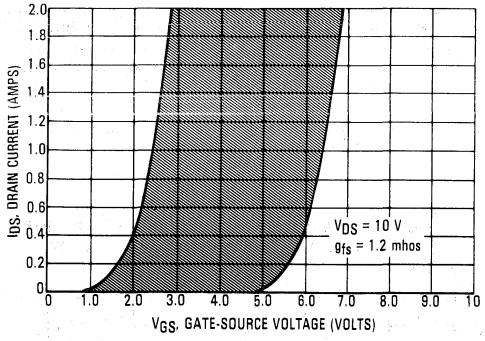
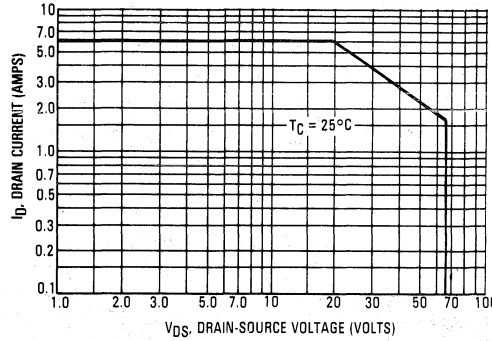
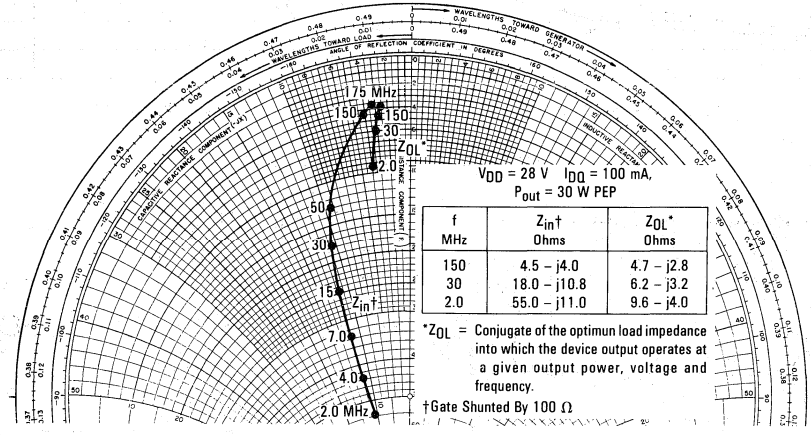


FIGURE 8 — DC SAFE OPERATING AREA



3

FIGURE 9 — LARGE-SIGNAL SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCE, Z_{in}†, Z_{OL}*



V_{DD} = 28 V I_{DQ} = 100 mA,
P_{out} = 30 W PEP

f MHz	Z_{in}† Ohms	Z_{OL}* Ohms
150	4.5 – j4.0	4.7 – j2.8
30	18.0 – j10.8	6.2 – j3.2
2.0	55.0 – j11.0	9.6 – j4.0

*Z_{OL} = Conjugate of the optimun load impedance into which the device output operates at a given output power, voltage and frequency.

†Gate Shunted By 100 Ω

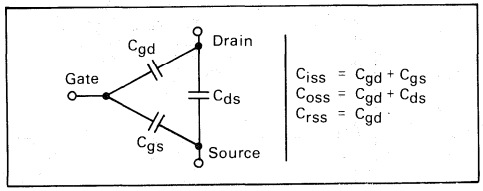
TMOS POWER FET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate-to-drain (C_{gd}), and gate-to-source (C_{gs}). The PN junction formed during the fabrication of the TMOS FET results in a junction capacitance from drain-to-source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the interterminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 5 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate-source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the TMOS FET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate-to-source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended.

3

EQUIVALENT TRANSISTOR PARAMETER TERMINOLOGY

Collector	Drain
Emitter	Source
Base	Gate
$V_{(BR)CES}$	$V_{(BR)DSS}$
I_C	I_D
I_{CES}	I_{DSS}
I_{EBO}	I_{GSS}
$V_{BE(on)}$	$V_{GS(th)}$
$V_{CE(sat)}$	$V_{DS(on)}$
C_{ib}	C_{iss}
C_{ob}	C_{oss}
h_{fe}	g_{fs}
$R_{CE(sat)} = \frac{V_{CE(sat)}}{I_C}$	$r_{DS(on)} = \frac{V_{DS(on)}}{I_D}$

MRF140

The RF TMOS Line

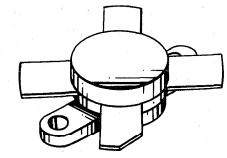
150 W 2.0-150 MHz

N-CHANNEL TMOS LINEAR RF POWER FET

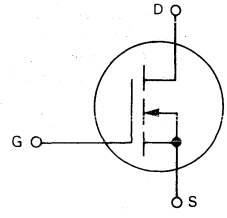
N-CHANNEL ENHANCEMENT-MODE TMOS RF POWER FIELD-EFFECT TRANSISTOR

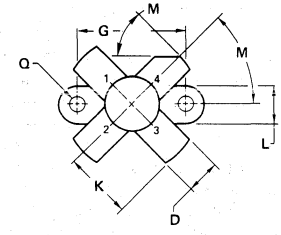
. . . designed primarily for linear large-signal output stages in the 2–150 MHz frequency range.

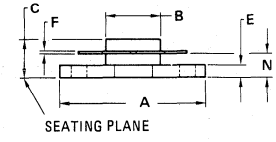
- Specified 28 Volts, 30 MHz Characteristics
  - Output Power = 150 Watts
  - Power Gain = 15 dB (Typ)
  - Efficiency = 40% (Typ)
- Superior High Order IMD
- $IMD_{(d3)}$ (150 W PEP) = –30 dB Typ
- $IMD_{(d11)}$ (150 W PEP) = –60 dB Typ
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR



TMOS™







STYLE 2:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	11.81	12.95	0.465	0.510
C	5.82	6.98	0.229	0.275
D	5.46	5.97	0.216	0.235
E	2.13	2.79	0.084	0.110
F	0.08	0.18	0.003	0.007
G	18.29	18.54	0.720	0.730
K	11.05	–	0.435	–
L	6.22	6.48	0.246	0.255
M	45° NOM		45° NOM	
N	3.66	4.52	0.144	0.178
Q	2.92	3.30	0.115	0.130

CASE 211-11

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain — Source Voltage	V_{DSS}	65	Vdc
Drain — Gate Voltage	V_{DGO}	65	Vdc
Gate — Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	16	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 1.7	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.6	°C/W

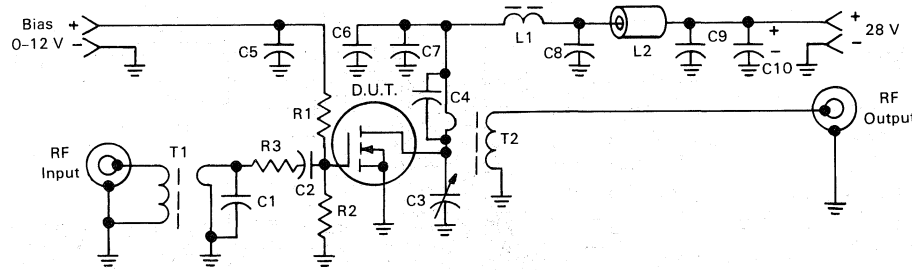
Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 100 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0)	I_{DSS}	—	—	5.0	mAdc
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	5.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V, I_D = 10 Adc)	$V_{DS(on)}$	—	—	1.5	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 5.0 A)	g_{fs}	4.0	—	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	450	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	450	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	100	—	pF
FUNCTIONAL TESTS (SSB)					
Common Source Amplifier Power Gain (30 MHz) (V_{DD} = 28 V, P_{out} = 150 W (PEP), I_{DQ} = 250 mA) (150 MHz)	G_{ps}	— —	15 6.0	— —	dB
Drain Efficiency (V_{DD} = 28 V, P_{out} = 150 W (PEP), f = 30; 30.001 MHz, I_D (Max) = 6.5 A)	η	—	40	—	%
Intermodulation Distortion (1) (V_{DD} = 28 V, P_{out} = 150 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 250 mA)	$IMD_{(d3)}$ $IMD_{(d11)}$	— —	-30 -60	— —	dB
Load Mismatch (V_{DD} = 28 V, P_{out} = 150 W (PEP), f = 30; 30.001 MHz, I_{DQ} = 250 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			

(1) To MIL-STD-1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.

FIGURE 1 — 30 MHz TEST CIRCUIT (CLASS AB)



C1 — 820 pF Dipped Mica
C2, C5, C6, C7, C8, C9 — 0.1 μF Ceramic Chip or Monolythic with Short Leads
C3 — Arco 469
C4 — 560 pF Unencapsulated Mica or Dipped Mica with Short Leads
C10 — 10 μF/100 V Electrolytic

L1 — VK200/4B Ferrite Choke or Equivalent, 3.0 μH
L2 — Ferrite Bead(s), 2.0 μH
R1, R2 — 51Ω/1.0 W Carbon
R3 — 1.0 Ω/1.0 W Carbon
T1 — 16:1 Broadband Transformer
T2 — 1:25 Broadband Transformer

FIGURE 2 — POWER GAIN versus FREQUENCY

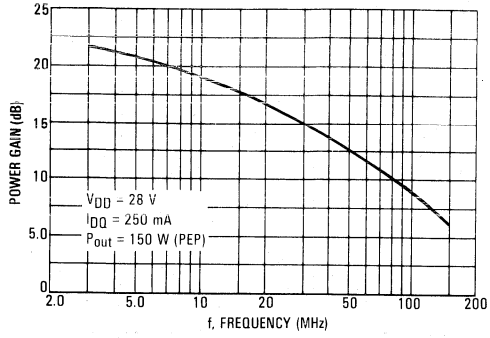


FIGURE 3 — OUTPUT POWER versus INPUT POWER

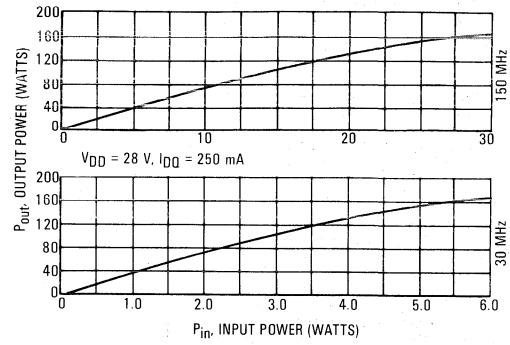


FIGURE 4 — IMD versus P_{out}

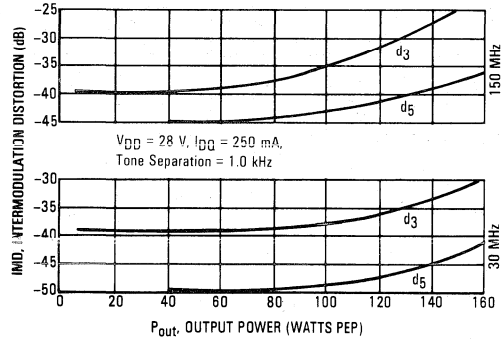


FIGURE 5 — COMMON SOURCE UNITY GAIN FREQUENCY versus DRAIN CURRENT

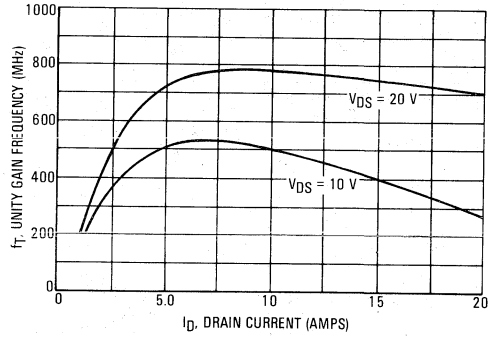


FIGURE 6 — GATE VOLTAGE versus DRAIN CURRENT

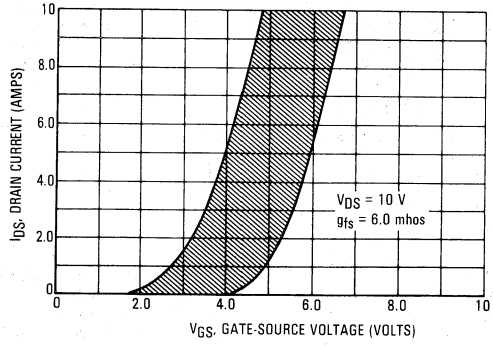
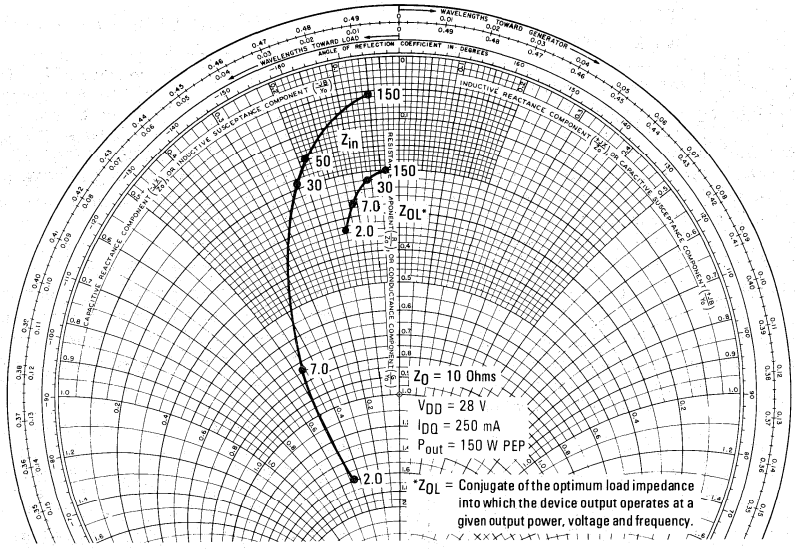


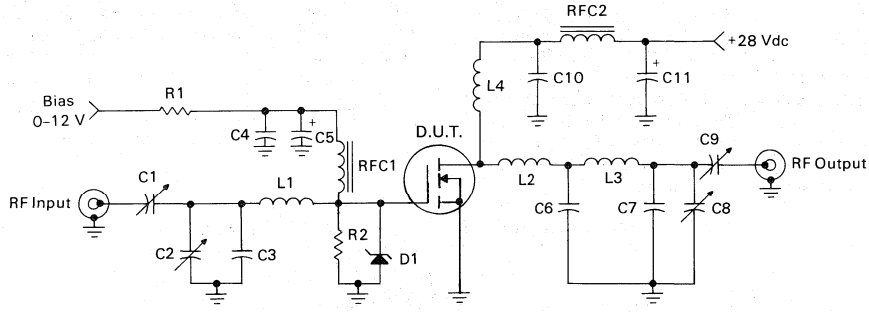
FIGURE 7 — SERIES EQUIVALENT IMPEDANCE



NOTE: Gate Shunted by 25 Ohms.

3

FIGURE 8 — 150 MHz TEST CIRCUIT (CLASS AB)



C1, C2, C8 — Arco 463 or equivalent
C3 — 25 pF Unelco
C4 — 0.1 μF Ceramic
C5 — 1.0 μF, 15 WV Tantalum
C6 — 150 pF Unelco J101
C7 — 25 μF Unelco J101
C9 — Arco 262 or equivalent
C10 — 0.05 μF Ceramic
C11 — 15 μF, 35 WV Electrolytic

L1 — 3/4″ #18 AWG into Hairpin
L2 — Printed Line, 0.200″ × 0.500″
L3 — 7/8″ #16 AWG into Hairpin
L4 — 2 Turns #16 AWG, 5/16 ID
RFC1 — 5.6 μH Molded Choke
RFC2 — VK200-4B
R1, R2 — 150 Ω, 1.0 W Carbon

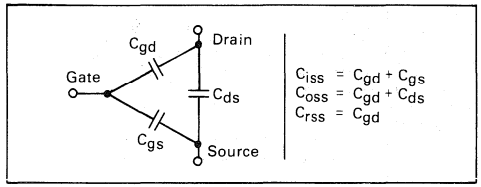
TMOS POWER FET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate-to-drain (C_{gd}), and gate-to-source (C_{gs}). The PN junction formed during the fabrication of the TMOS FET results in a junction capacitance from drain-to-source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the interterminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 5 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate-source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the TMOS FET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate-to-source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended.

EQUIVALENT TRANSISTOR PARAMETER TERMINOLOGY

Collector	Drain
Emitter	Source
Base	Gate
$V_{(BR)CES}$	$V_{(BR)DSS}$
V_{CBO}	V_{DGO}
I_C	I_D
I_{CES}	I_{DSS}
I_{EBO}	I_{GSS}
$V_{BE(on)}$	$V_{GS(th)}$
$V_{CE(sat)}$	$V_{DS(on)}$
C_{ib}	C_{iss}
C_{ob}	C_{oss}
h_{fe}	g_{fs}
$R_{CE(sat)} = \frac{V_{CE(sat)}}{I_C}$	$r_{DS(on)} = \frac{V_{DS(on)}}{I_D}$

MRF148

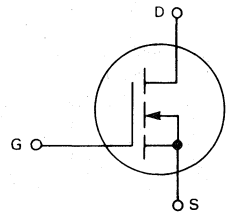
The RF TMOS Line

N-CHANNEL ENHANCEMENT-MODE
TMOS RF POWER FIELD-EFFECT TRANSISTOR

. . . designed for power amplifier applications in industrial, commercial and amateur radio equipment to 175 MHz.

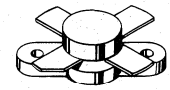
- Superior High Order IMD
- Specified 50 Volts, 30 MHz Characteristics
  Output Power = 30 Watts
  Power Gain = 18 dB (Typ)
  Efficiency = 40% (Typ)
- $IMD_{(d3)}$ (30 W PEP) = -35 dB (Typ)
- $IMD_{(d11)}$ (30 W PEP) = -60 dB (Typ)
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR

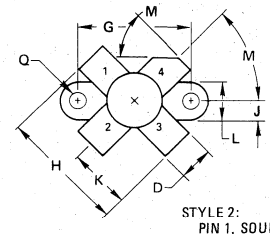
TMOS™



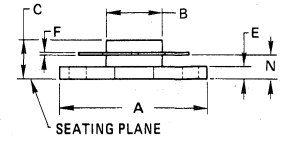
30 W 2.0-175 MHz

N-CHANNEL TMOS
LINEAR RF POWER
FET





STYLE 2:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	9.40	9.91	0.370	0.390
C	5.82	7.14	0.229	0.281
D	5.46	5.97	0.215	0.235
E	2.16	2.67	0.085	0.105
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	20.07	20.57	0.790	0.810
K	10.03	10.29	0.395	0.405
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.81	4.57	0.150	0.180
Q	2.87	3.30	0.113	0.130

CASE 211-07

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain — Source Voltage	V_{DSS}	120	Vdc
Drain — Gate Voltage	V_{DGO}	120	Vdc
Gate — Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	6.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	115 0.66	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.52	°C/W

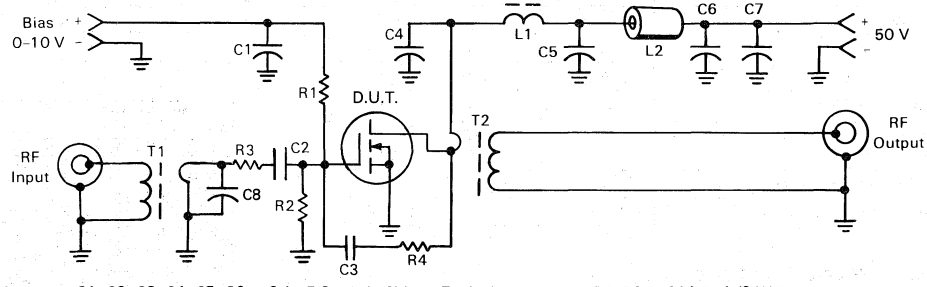
Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 10 mA)	$V_{(BR)DSS}$	125	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 50 V, V_{GS} = 0)	I_{DSS}	—	—	1.0	mAdc
Gate-Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 10 mA)	$V_{GS(th)}$	1.0	3.0	5.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V, I_D = 2.5 A)	$V_{DS(on)}$	—	—	5.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 2.5 A)	g_{fs}	0.8	1.2	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 50 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}	—	50	—	pF
Output Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	35	—	pF
Reverse Transfer Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	8.0	—	pF
FUNCTIONAL TESTS (SSB)					
Common Source Amplifier Power Gain (30 MHz) (V_{DD} = 50 V, P_{out} = 30 W (PEP), I_{DQ} = 100 mA) (175 MHz)	G_{ps}	— —	18 15	— —	dB
Drain Efficiency (30 W PEP) (V_{DD} = 50 V, f = 30 MHz, I_{DQ} = 100 mA) (30 W CW)	η	— —	40 50	— —	%
Intermodulation Distortion (V_{DD} = 50 V, P_{out} = 30 W (PEP), f = 30; 30.001 MHz, I_{DQ} = 100 mA)	$IMD_{(d3)}$ $IMD_{(d11)}$	— —	-35 -60	— —	dB
Load Mismatch (V_{DD} = 50 V, P_{out} = 30 W (PEP), f = 30; 30.001 MHz, I_{DQ} = 100 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			
CLASS A PERFORMANCE					
Intermodulation Distortion (1) and Power Gain (V_{DD} = 50 V, P_{out} = 10 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 1.0 A)	G_{PS} $IMD_{(d3)}$ $IMD_{(d9-13)}$	— — —	20 -50 -70	— — —	dB

(1) To MIL-STD-1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.

FIGURE 1 — 2-50 MHz BROADBAND TEST CIRCUIT



C1, C2, C3, C4, C5, C6 — 0.1 μF Ceramic Chip or Equivalent
C7 — 10 μF, 100 V Electrolytic
C8 — 100 pF Dipped Mica
L1 — VK200 20/4B Ferrite Choke or Equivalent (3.0 μH)
L2 — Ferrite Bead(s), 2.0 μH

R1, R2 — 200 Ω, 1/2 W Carbon
R3 — 4.7 Ω, 1/2 W Carbon
R4 — 470 Ω, 1.0 W Carbon
T1 — 4:1 Impedance Transformer
T2 — 1:2 Impedance Transformer

FIGURE 2 — POWER GAIN versus FREQUENCY

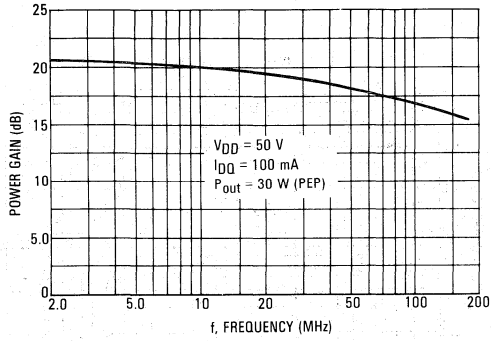


FIGURE 3 — OUTPUT POWER versus INPUT POWER

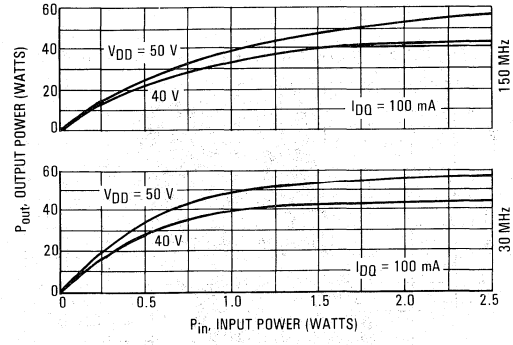


FIGURE 4 — IMD versus P_{out}

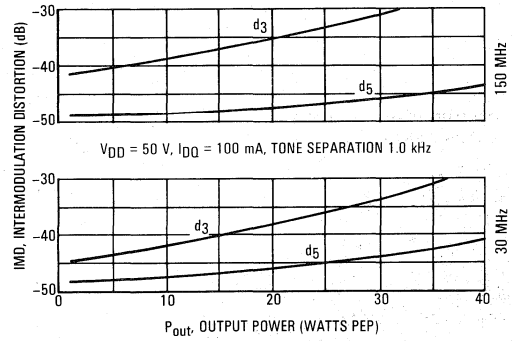


FIGURE 5 — COMMON SOURCE UNITY GAIN FREQUENCY versus DRAIN CURRENT

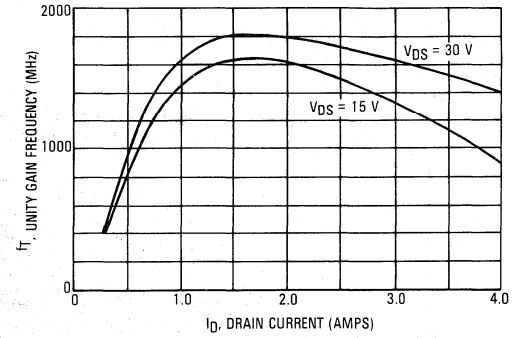
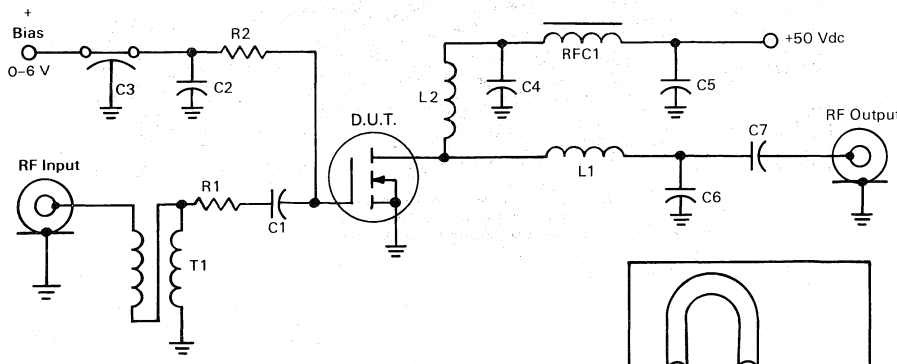


FIGURE 6 — 150 MHz TEST CIRCUIT



C1 — 91 pF Unelco Type MCM 01/010
C2, C4 — 0.1 μF Erie Red Cap
C3 — Allen Bradley 680 pF Feed Thru
C5 — 1.0 μF, 50 Vdc Electrolytic
C6 — 15 pF Unelco Type J101
C7 — 24 pF Unelco Type MCM 01/010
L1 — 2 Turns # 18 AWG, 5/16″ ID

L2 — 4 Turns # 18 AWG, 5/16″ ID
R1 = 1.0 Ohm, 1/4 W Carbon
R2 — 2000 Ohm, 1/4 W Carbon
RFC1 — VK200 21/4B
T1 — 4:1 Transformer, 1.75″ Subminiature Coaxial Cable

T1 — 4:1 Impedance Ratio Transformer, Line Impedance = 25 Ω

FIGURE 7 — GATE VOLTAGE versus DRAIN CURRENT

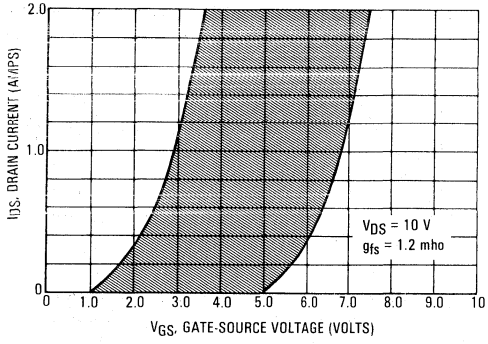


FIGURE 8 — DC SAFE OPERATING AREA (SOA)

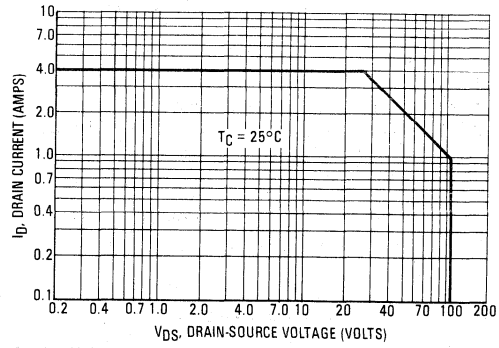
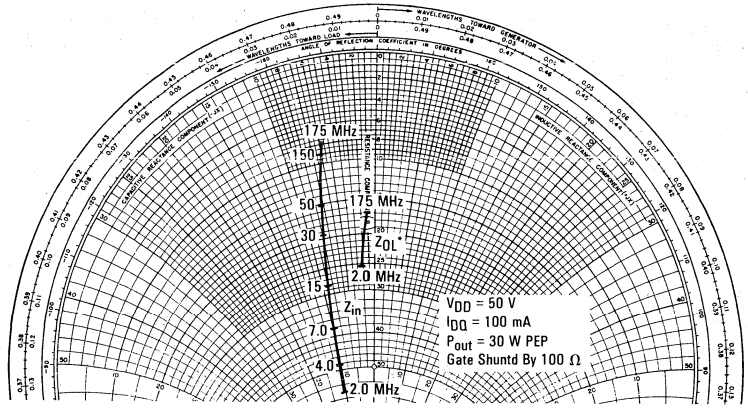


FIGURE 9 — IMPEDANCE COORDINATES — 50-OHM CHARACTERISTIC IMPEDANCE



*Z_{OL} = Conjugate of the optimun load impedance into which the device output operates at a given output power, voltage and frequency.

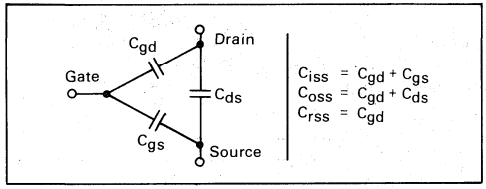
TMOS POWER FET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate-to-drain (C_{gd}), and gate-to-source (C_{gs}). The PN junction formed during the fabrication of the TMOS FET results in a junction capacitance from drain-to-source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the interterminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 5 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate-source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the TMOS FET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate-to-source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended.

EQUIVALENT TRANSISTOR PARAMETER TERMINOLOGY

Collector	Drain
Emitter	Source
Base	Gate
$V_{(BR)CES}$	$V_{(BR)DSS}$
V_{CBO}	V_{DGO}
I_C	I_D
I_{CES}	I_{DSS}
I_{EBO}	I_{GSS}
$V_{BE(on)}$	$V_{GS(th)}$
$V_{CE(sat)}$	$V_{DS(on)}$
C_{ib}	C_{iss}
C_{ob}	C_{oss}
h_{fe}	g_{fs}
$R_{CE(sat)} = \frac{V_{CE(sat)}}{I_C}$	$r_{DS(on)} = \frac{V_{DS(on)}}{I_D}$

MRF150

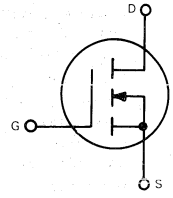
The RF TMOS Line

N-CHANNEL ENHANCEMENT-MODE
TMOS RF POWER FIELD-EFFECT TRANSISTOR

. . . designed primarily for linear large-signal output stages in the 2-175 MHz frequency range.

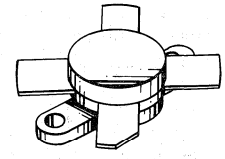
- Specified 50 Volts, 30 MHz Characteristics
  - Output Power = 150 Watts
  - Power Gain = 17 dB (Typ)
  - Efficiency = 45% (Typ)
- Superior High Order IMD
- $IMD_{(d3)}$ (150 W PEP) = -32 dB (Typ)
- $IMD_{(d11)}$ (150 W PEP) = -60 dB (Typ)
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR

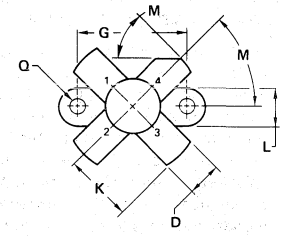
TMOS™

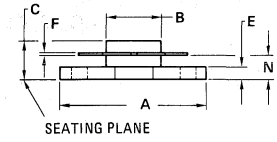


150 W 2.0-175 MHz

N-CHANNEL TMOS LINEAR RF POWER FET







STYLE 2:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	11.81	12.95	0.465	0.510
C	5.82	6.98	0.229	0.275
D	5.46	5.97	0.216	0.235
E	2.13	2.79	0.084	0.110
F	0.08	0.18	0.003	0.007
G	18.29	18.54	0.720	0.730
K	11.05	–	0.435	–
L	6.22	6.48	0.246	0.255
M	45° NOM		45° NOM	
N	3.66	4.52	0.144	0.178
Q	2.92	3.30	0.115	0.130

CASE 211-11

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain — Source Voltage	V_{DSS}	125	Vdc
Drain — Gate Voltage	V_{DGO}	125	Vdc
Gate — Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	16	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 1.71	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.6	°C/W

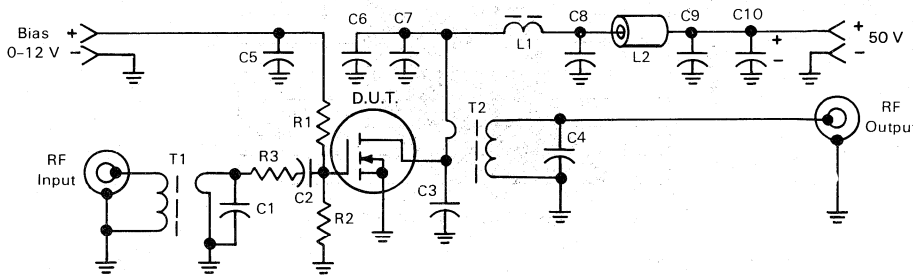
Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 100 mA)	$V_{(BR)DSS}$	125	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 50 V, V_{GS} = 0)	I_{DSS}	—	—	5.0	mAdc
Gate-Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	5.0	Vdc
Drain-Source On-Voltage ((V_{GS} = 10 V, I_D = 10 A)	$V_{DS(on)}$	—	—	5.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 5.0 A)	g_{fs}	4.0	5.0	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 50 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}	—	350	—	pF
Output Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	250	—	pF
Reverse Transfer Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	50	—	pF
FUNCTIONAL TESTS (SSB)					
Common Source Amplifier Power Gain (V_{DD} = 50 V, P_{out} = 150 W (PEP), I_{DQ} = 250 mA)	G_{ps}	— —	17 8.0	— —	dB
Drain Efficiency (V_{DD} = 50 V, P_{out} = 150 W (PEP), f = 30; 30.001 MHz, I_D (Max) = 3.75 A)	η	—	45	—	%
Intermodulation Distortion (1) (V_{DD} = 50 V, P_{out} = 150 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 250 mA)	$IMD_{(d3)}$ $IMD_{(d11)}$	— —	-32 -60	— —	dB
Load Mismatch (V_{DD} = 50 V, P_{out} = 150 W (PEP), f = 30; 30.001 MHz, I_{DQ} = 250 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			
CLASS A PERFORMANCE					
Intermodulation Distortion (1) and Power Gain (V_{DD} = 50 V, P_{out} = 50 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 3.0 A)	G_{PS} $IMD_{(d3)}$ $IMD_{(d9-13)}$	— — —	20 -50 -75	— — —	dB

(1) To MIL-STD-1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.

FIGURE 1 — 30 MHz TEST CIRCUIT (CLASS AB)



C1 — 470 pF Dipped Mica
C2, C5, C6, C7, C8, C9 — 0.1 μF Ceramic Chip or Monolythic with Short Leads
C3 — 200 pF Unencapsulated Mica or Dipped Mica with Short Leads
C4 — 15 pF Unencapsulated Mica or Dipped Mica with Short Leads
C10 — 10 μF/100 V Electrolytic
L1 — VK200/4B Ferrite Choke or Equivalent, 3.0 μH
L2 — Ferrite Bead(s), 2.0 μH
R1, R2 — 51Ω/1.0 W Carbon
R3 — 3.3 Ω/1.0 W Carbon (or 2× 6.8 Ω/1/2 W in Parallel
T1 — 9:1 Broadband Transformer
T2 — 1:9 Broadband Transformer

FIGURE 2 — POWER GAIN versus FREQUENCY

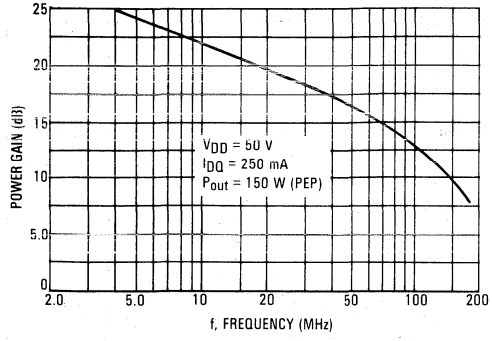


FIGURE 3 — OUTPUT POWER versus INPUT POWER

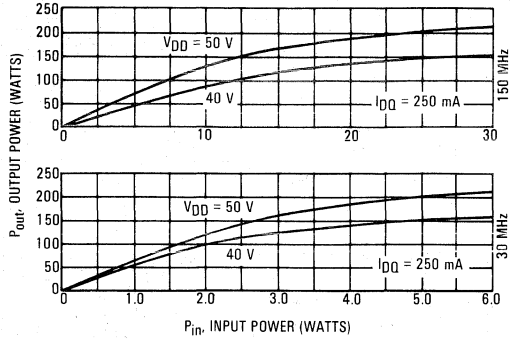


FIGURE 4 — IMD versus P_{out}

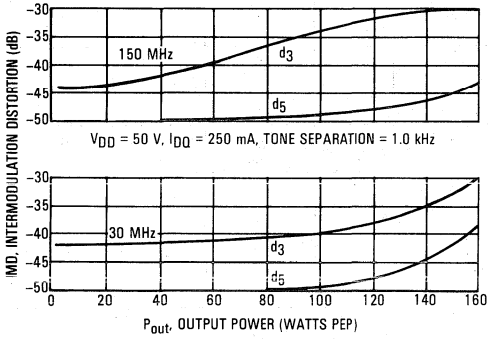


FIGURE 5 — COMMON SOURCE UNITY GAIN FREQUENCY versus DRAIN CURRENT

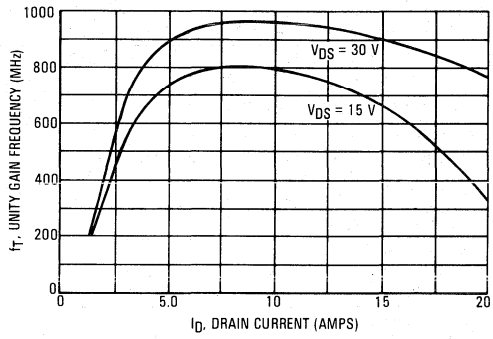


FIGURE 6 — GATE VOLTAGE versus DRAIN CURRENT

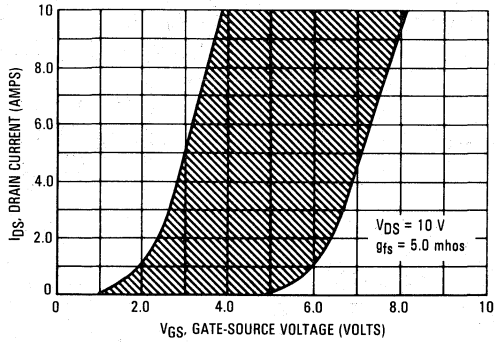
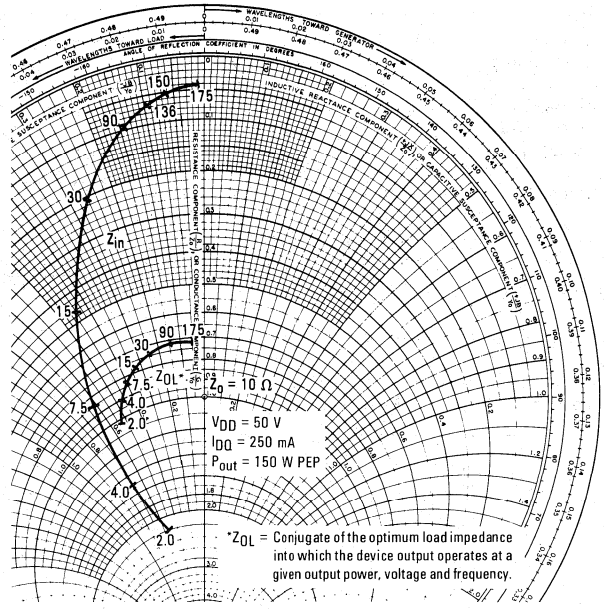
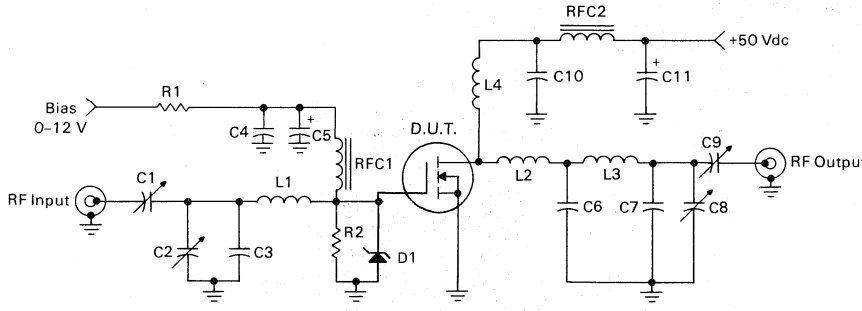


FIGURE 7 — SERIES EQUIVALENT IMPEDANCE



NOTE: Gate Shunted By 25 Ohms.

FIGURE 8 — 150 MHz TEST CIRCUIT (CLASS AB)



C1, C2, C8 — Arco 463 or equivalent
C3 — 25 pF Unelco
C4 — 0.1 μF Ceramic
C5 — 1.0 μF, 15 WV Tantalum
C6 — 250 pF Unelco J101
C7 — 25 μF Unelco J101
C9 — Arco 262 or equivalent
C10 — 0.05 μF Ceramic
C11 — 15 μF, 60 WV Electrolytic

D1 — 1N5347 Zener Diode
L1 — 3/4″ #18 AWG into Hairpin
L2 — Printed Line, 0.200″ × 0.500″
L3 — 1″ #16 AWG into Hairpin
L4 — 2 Turns #16 AWG, 5/16 ID
RFC1 — 5.6 μH Choke
RFC2 — VK200-4B
R1, R2 — 150 Ω, 1.0 W Carbon

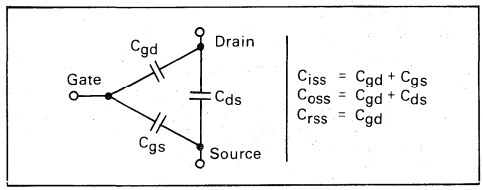
TMOS POWER FET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate-to-drain (C_{gd}), and gate-to-source (C_{gs}). The PN junction formed during the fabrication of the TMOS FET results in a junction capacitance from drain-to-source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the interterminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 5 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate-source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the TMOS FET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate-to-source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended.

EQUIVALENT TRANSISTOR PARAMETER TERMINOLOGY

Collector	Drain
Emitter	Source
Base	Gate
$V_{(BR)CES}$	$V_{(BR)DSS}$
V_{CBO}	V_{DGO}
I_C	I_D
I_{CES}	I_{DSS}
I_{EBO}	I_{GSS}
$V_{BE(on)}$	$V_{GS(th)}$
$V_{CE(sat)}$	$V_{DS(on)}$
C_{ib}	C_{iss}
C_{ob}	C_{oss}
h_{fe}	g_{fs}
$R_{CE(sat)} = \frac{V_{CE(sat)}}{I_C}$	$r_{DS(on)} = \frac{V_{DS(on)}}{I_D}$

MRF153

The RF TMOS Line

Power Field Effect Transistor

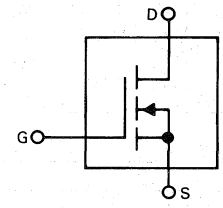
N-Channel Enhancement Mode TMOS RF

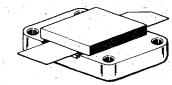
. . . designed primarily for linear large-signal output stages in the 2–100 MHz frequency range.

- Specified 50 Volts, 30 MHz Characteristics
  Output Power = 300 Watts
  Power Gain = 17 dB (Typ)
  Efficiency = 45% (Typ)

TMOS™

TMOS LINEAR RF POWER FETs 300 WATTS 2–100 MHz





CASE 368-01

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	125	Vdc
Drain-Gate Voltage	V_{DGO}	125	Vdc
Gate-Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	40	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	700 4	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature	T_J	200	°C

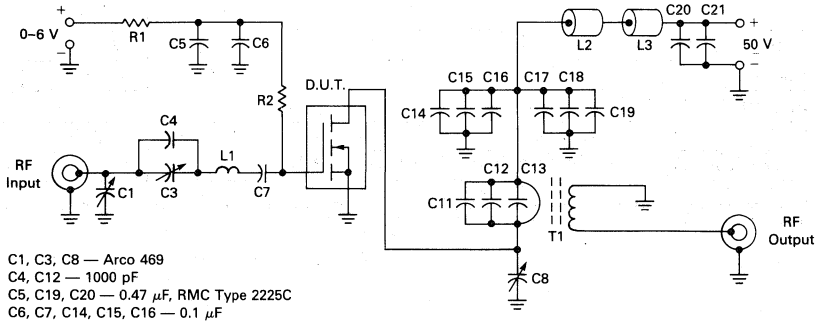
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.25	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 100 mA)	$V_{(BR)DSS}$	125	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 50 V, V_{GS} = 0)	I_{DSS}	—	—	10	mAdc
Gate-Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	3	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1	3	5	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V, I_D = 20 A)	$V_{DS(on)}$	—	—	5	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 10 A)	g_{fs}	8	10	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz)	C_{iss}	—	800	—	pF
Output Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	500	—	pF
Reverse Transfer Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	100	—	pF
FUNCTIONAL TESTS					
Common Source Amplifier Power Gain (V_{DD} = 50 V, P_{out} = 300 W, I_{DQ} = 400 mA)	G_{ps}	—	17	—	dB
Drain Efficiency (V_{DD} = 50 V, P_{out} = 300 W, f = 30 MHz)	η	—	45	—	%
Intermodulation Distortion (V_{DD} = 50 V, P_{out} = 300 $W_{(PEP)}$, f1 = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 40 mA)	$IMD_{(d3)}$	—	−25	—	dB



C1, C3, C8 — Arco 469
C4, C12 — 1000 pF
C5, C19, C20 — 0.47 μF, RMC Type 2225C
C6, C7, C14, C15, C16 — 0.1 μF
C11 — 470 pF
C13 — Two Unencapsulated 1000 pF Mica, in Series
C17, C18 — 0.039 μF
C21 — 10 μF/100 V Electrolytic
R1, R2 — 10 Ohms/2W Carbon
L1 — 2 Turns #16 AWG, 1/2" ID, 1/4" Long

L2, L3 — Ferrite Beads, Fair-Rite Products Corp. #2673000801
T1 — RF Transformer, 1:16 Impedance Ratio. See Motorola Application Note AN-749, Figure 4 for details.
Ferrite Material: 2 Each, Fair-Rite Products Corp. #2667540001

All capacitors ATC type 100/200 chips or equivalent unless otherwise noted.

Figure 1. 30 MHz Test Circuit

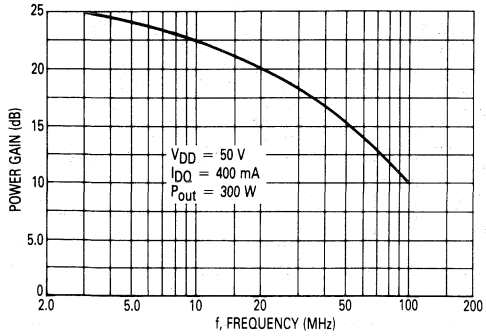


Figure 2. Power Gain versus Frequency

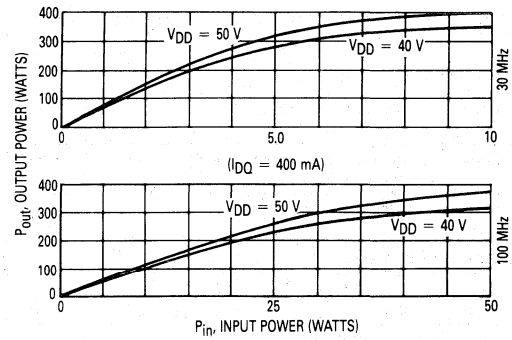


Figure 3. Output Power versus Input Power

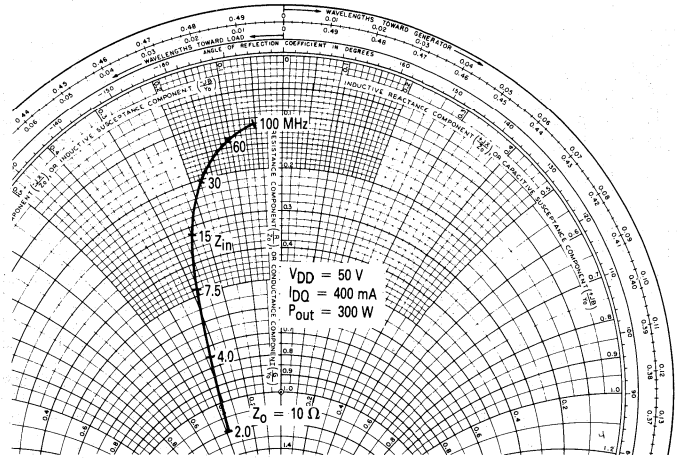
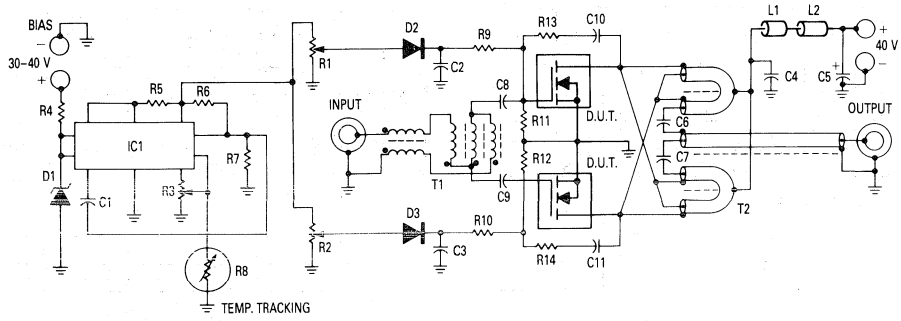


Figure 4. Series Equivalent Impedance



C1 — 1000 pF Ceramic
C2, C3, C4, C8, C9, C10, C11 — 0.1 μF Ceramic
C5 — 10 μF/100 V Electrolytic
C6, C7 — 0.1 μF Ceramic, (ATC 200/823 or Equivalent)
D1 — 28 V Zener, 1N5362 or Equivalent
D3 — 1N4148
IC1 — MC1723
L1, L2 — Fair-Rite Products Corp. Ferrite Beads #2673000801
R1, R2, R3 — 10 k Trimpot
R4 — 1.0 k / 1.0 W
R5 — 10 Ohms
R6 — 2.0 k
R7 — 10 k
R8 — Thermistor, 10 k (25°C), 2.5 k (75°C)
R9, R10 — 100 Ohms
R11, R12 — 1.0 k
R13, R14 — 50–100 Ohms, 4 x 2 W Carbon in Parallel
T1 — 9:1 Transformer, Trifilar and Balun Wound on Separate Fair-Rite Products Corp. Balun Cores #286100012, 5 Turns Each.
T2 — 1:9 Transformer, Balun 50 Ohm CO-AX Cable RG-188, Low Impedance Lines W.L. Gore 16 Ohms CO-AX Type CXN 1837. Each Winding Threaded Through Two Fair-Rite Products Corp. #2661540001 Ferrite Sleeves (6 Each).

Figure 5. 20–80 MHz 500 W Broadband Amplifier

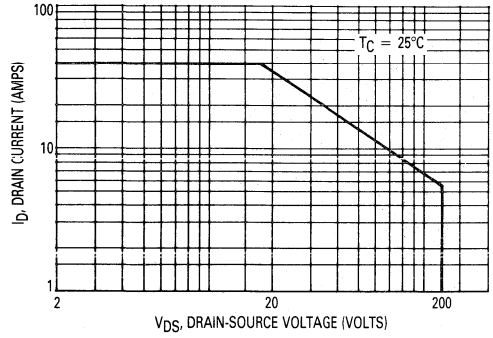


Figure 6. DC Safe Operating Area

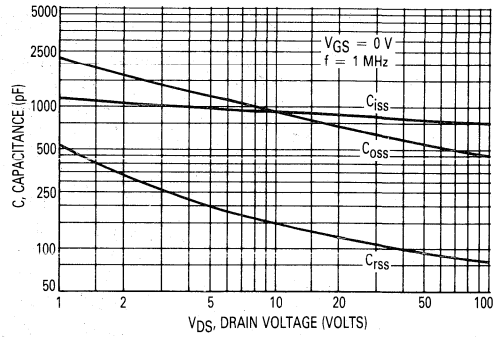


Figure 7. Capacitance versus Drain Voltage

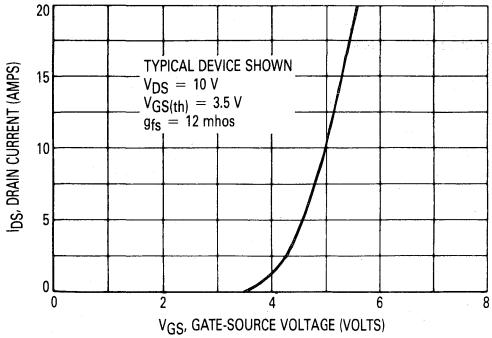


Figure 8. Gate Voltage versus Drain Current

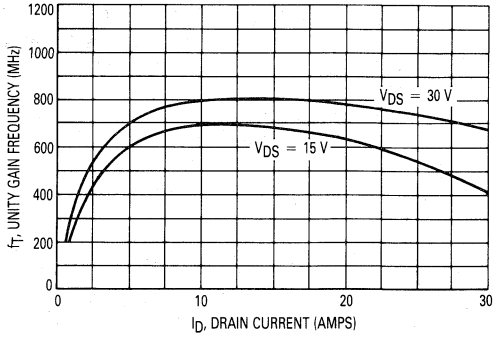


Figure 9. Common Source Unity Gain Frequency versus Drain Current

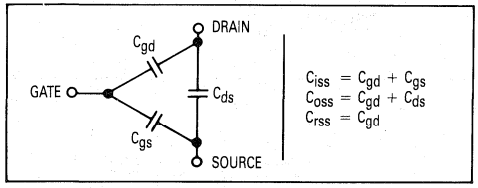
TMOS POWER FET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate-to-drain (C_{gd}), and gate-to-source (C_{gs}). The PN junction formed during the fabrication of the TMOS FET results in a junction capacitance from drain-to-source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the interterminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 5 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate-source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the TMOS FET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate-to-source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate-to-source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

MOUNTING OF HIGH POWER RF POWER TRANSISTORS

The package of this device is designed for conduction cooling. It is extremely important to minimize the thermal resistance between the device flange and the heat dissipator.

Since the device mounting flange is made of soft copper, it may be deformed during various stages of handling or during transportation. It is recommended that the user makes a final inspection on this before the device installation. ±0.0005″ is considered sufficient for the flange bottom.

The same applies to the heat dissipator in the device mounting area. If copper heatsink is not used, a copper head spreader is strongly recommended between the device mounting surfaces and the main heatsink. It should be at least 1/4″ thick and extend at least one inch from the flange edges. A thin layer of thermal compound in all interfaces is, of course, essential. The recommended torque on the 4-40 mounting screws should be in the area of 4–5 lbs.-inch, and spring type lock washers along with flat washers are recommended.

For die temperature calculations, the Δ temperature from a corner mounting screw area to the bottom center of the flange is approximately 5°C and 10°C under normal operating conditions (dissipation 150 W and 300 W respectively).

The main heat dissipator must be sufficiently large and have low R_θ for moderate air velocity, unless liquid cooling is employed.

CIRCUIT CONSIDERATIONS

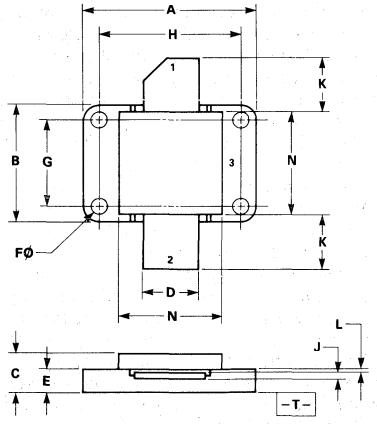
At high power levels (500 W and up), the circuit layout becomes critical due to the low impedance levels and high RF currents associated with the output matching. Some of the components, such as capacitors and inductors must also withstand these currents. The component losses are directly proportional to the operating fre-

quency. The manufacturers specifications on capacitor ratings should be consulted on these aspects prior to design.

Push-pull circuits are less critical in general, since the ground referenced RF loops are practically eliminated, and the impedance levels are higher for a given power output. High power broadband transformers are also easier to design than comparable LC matching networks.

EQUIVALENT TRANSISTOR PARAMETER TERMINOLOGY

Collector	Drain
Emitter	Source
Base	Gate
$V_{(BR)CES}$	$V_{(BR)DSS}$
V_{CBO}	V_{DGO}
I_C	I_D
I_{CES}	I_{DSS}
I_{EBO}	I_{GSS}
$V_{BE(on)}$	$V_{GS(th)}$
$V_{CE(sat)}$	$V_{DS(on)}$
C_{ib}	C_{iss}
C_{ob}	C_{oss}
h_{fe}	g_{fs}
$R_{CE(sat)} = \frac{V_{CE(sat)}}{I_C}$	$r_{DS(on)} = \frac{V_{DS(on)}}{I_D}$



STYLE 2:
PIN 1. DRAIN
2. GATE
3. SOURCE

NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS BOTH A DATUM AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR F DIAMETER. ⌖ ϕ 0.25 (.010) Ⓜ | T | A Ⓜ | B Ⓜ |
3. DIMENSIONING AND TOLERANCING PER Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	37.85	38.35	1.490	1.510
B	25.15	25.65	0.990	1.010
C	8.38	8.89	0.330	0.350
D	12.45	12.95	0.490	0.510
E	4.95	5.21	0.195	0.205
F	3.05	3.30	0.120	0.130
G	19.05 BSC		0.750 BSC	
H	31.75 BSC		1.250 BSC	
J	1.14	1.39	0.045	0.055
K	10.54	11.05	0.415	0.435
L	0.10	0.15	0.004	0.006
N	22.87	23.11	0.890	0.910

CASE 368-01

MRF154

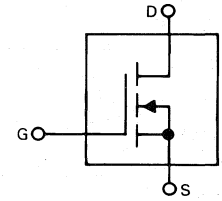
The RF TMOS Line
Power Field Effect Transistor
N-Channel Enhancement Mode TMOS RF

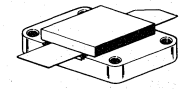
. . . designed primarily for linear large-signal output stages in the 2–100 MHz frequency range.

- Specified 50 Volts, 30 MHz Characteristics
  Output Power = 600 Watts
  Power Gain = 17 dB (Typ)
  Efficiency = 45% (Typ)

TMOS™

TMOS LINEAR RF POWER FETs 600 WATTS 2–100 MHz





CASE 368-01

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	125	Vdc
Drain-Gate Voltage	V_{DGO}	125	Vdc
Gate-Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	60	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1350 7.7	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature	T_J	200	°C

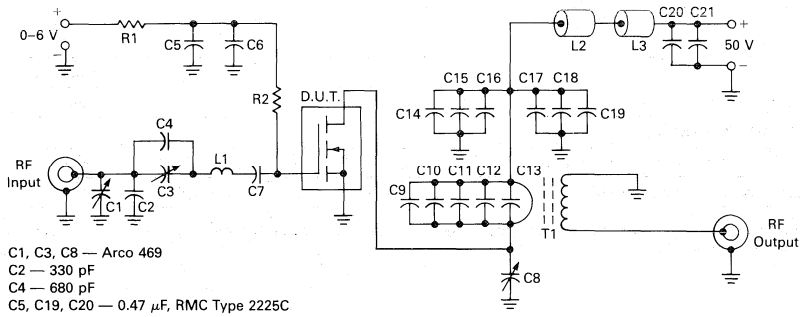
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.13	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 100 mA)	$V_{(BR)DSS}$	125	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 50 V, V_{GS} = 0)	I_{DSS}	—	—	20	mAdc
Gate-Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	5	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1	3	5	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V, I_D = 40 A)	$V_{DS(on)}$	—	—	5	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 20 A)	g_{fs}	16	20	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz)	C_{iss}	—	1600	—	pF
Output Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	1000	—	pF
Reverse Transfer Capacitance (V_{DS} = 50 V, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	200	—	pF
FUNCTIONAL TESTS					
Common Source Amplifier Power Gain (V_{DD} = 50 V, P_{out} = 600 W, I_{DQ} = 800 mA, f = 30 MHz)	G_{ps}	—	17	—	dB
Drain Efficiency (V_{DD} = 50 V, P_{out} = 600 W, I_{DQ} = 800 mA, f = 30 MHz)	η	—	45	—	%
Intermodulation Distortion (V_{DD} = 50 V, P_{out} = 600 W(PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{DQ} = 800 mA)	IMD(d3)	—	−25	—	dB



C1, C3, C8 — Arco 469
C2 — 330 pF
C4 — 680 pF
C5, C19, C20 — 0.47 μF, RMC Type 2225C
C6, C7, C14, C15, C16 — 0.1 μF
C9, C10, C11 — 470 pF
C12 — 1000 pF
C13 — Two Unencapsulated 1000 pF Mica, in Series
C17, C18 — 0.039 μF
C21 — 10 μF/100 V Electrolytic
R1, R2 — 10 Ohms/2W Carbon
L1 — 2 Turns #16 AWG, 1/2" ID, 3/8" Long
L2, L3 — Ferrite Beads, Fair-Rite Products Corp. #2673000801
T1 — RF Transformer, 1:25 Impedance Ratio. See Motorola Application Note AN-749, Figure 4 for details. Ferrite Material: 2 Each, Fair-Rite Products Corp. #2667540001

All capacitors ATC type 100/200 chips or equivalent unless otherwise noted.

FIGURE 1 — 30 MHz TEST CIRCUIT

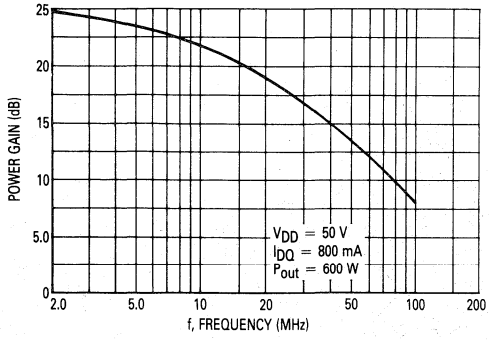


Figure 2. Power Gain versus Frequency

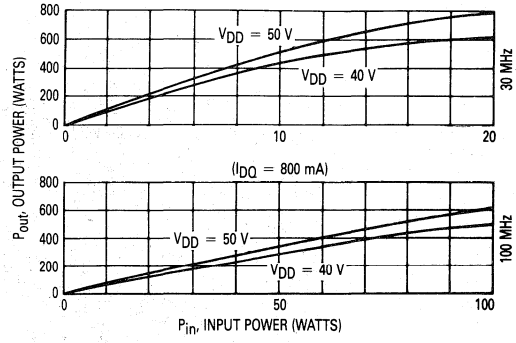


Figure 3. Output Power versus Input Power

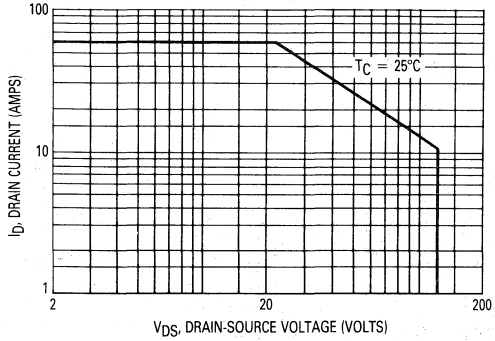


Figure 4. DC Safe Operating Area

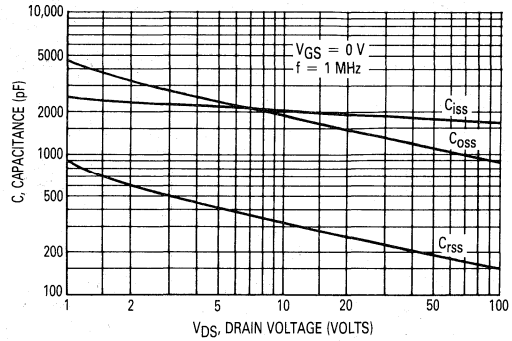


Figure 5. Capacitance versus Drain Voltage

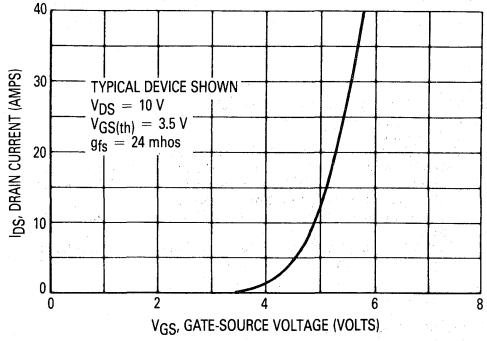


Figure 6. Gate Voltage versus Drain Current

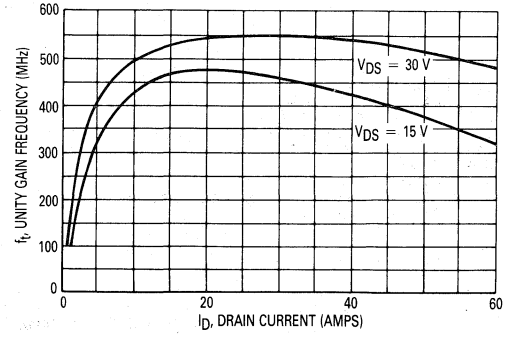


Figure 7. Common Source Unity Gain Frequency versus Drain Current

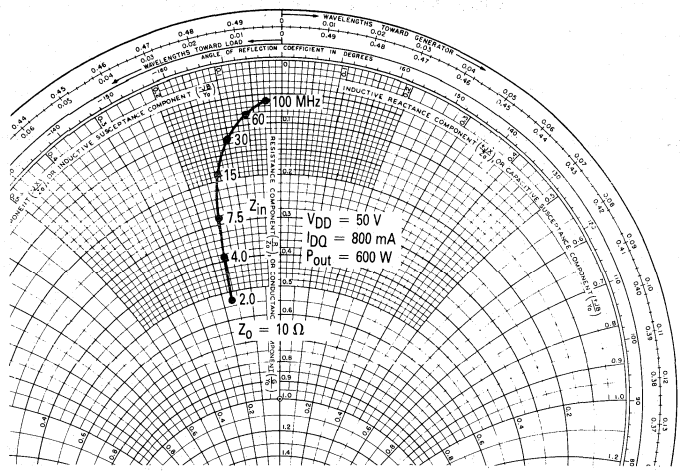
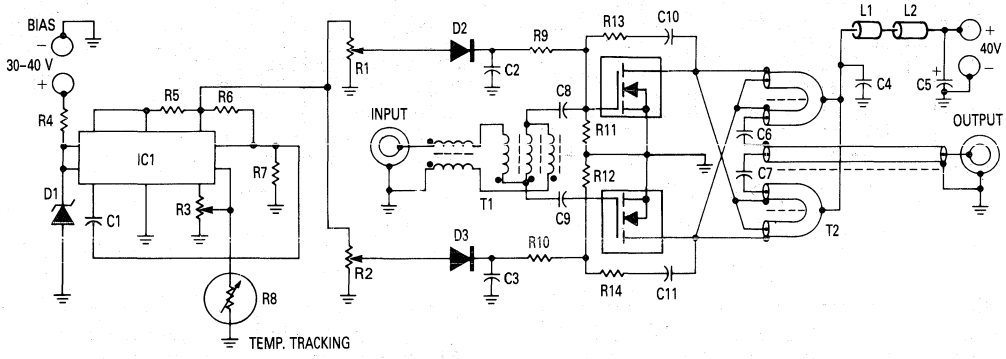


Figure 8. Series Equivalent Impedance



C1 — 1000 pF Ceramic
C2, C3, C4, C8, C9, C10, C11 — 0.1 μF Ceramic
C5 — 10 μF/100 V Electrolytic
C6, C7 — 0.1 μF Ceramic, (ATC 200/823 or Equivalent)
D1 — 28 V Zener, 1N5362 or Equivalent
D3 — 1N4148
IC1 — MC1723
L1, L2 — Fair-Rite Products Corp. Ferrite Beads #2673000801
R1, R2, R3 — 10 k Trimpot
R4 — 1.0 k / 1.0 W
R5 — 10 Ohms
R6 — 2.0 k
R7 — 10 k
R8 — Thermistor, 10 k (25°C), 2.5 k (75°C)
R9, R10 — 100 Ohms
R11, R12 — 1.0 k
R13, R14 — 50–100 Ohms, 4 x 2 W Carbon in Parallel
T1 — 9:1 Transformer, Trifilar and Balun Wound on Separate Fair-Rite Products Corp. Balun Cores #286100012, 5 Turns Each.
T2 — 1:9 Transformer, Balun 50 Ohm CO-AX Cable RG-188, Low Impedance Lines W.L. Gore 16 Ohms CO-AX Type CXN 1837.
Each Winding Threaded Through Two Fair-Rite Products Corp. #2661540001 Ferrite Sleeves (6 Each).

Figure 9. 20–80 MHz 1 kW Broadband Amplifier

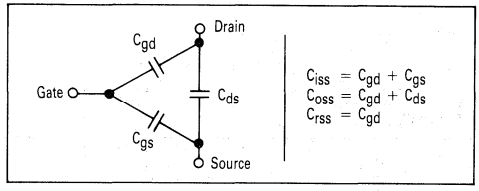
TMOS POWER FET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate-to-drain (C_{gd}), and gate-to-source (C_{gs}). The PN junction formed during the fabrication of the TMOS FET results in a junction capacitance from drain-to-source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the interterminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain data presented, Figure 5 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to f_T for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate-source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the TMOS FET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate-to-source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate-to-source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

MOUNTING OF HIGH POWER RF POWER TRANSISTORS

The package of this device is designed for conduction cooling. It is extremely important to minimize the thermal resistance between the device flange and the heat dissipator.

Since the device mounting flange is made of soft copper, it may be deformed during various stages of handling or during transportation. It is recommended that the user makes a final inspection on this before the device installation. ±0.0005″ is considered sufficient for the flange bottom.

The same applies to the heat dissipator in the device mounting area. If copper heatsink is not used, a copper head spreader is strongly recommended between the device mounting surfaces and the main heatsink. It should be at least 1/4″ thick and extend at least one inch from the flange edges. A thin layer of thermal compound in all interfaces is, of course, essential. The recommended torque on the 4-40 mounting screws should be in the area of 4–5 lbs.-inch, and spring type lock washers along with flat washers are recommended.

For die temperature calculations, the Δ temperature from a corner mounting screw area to the bottom center of the flange is approximately 5°C and 10°C under normal operating conditions (dissipation 150 W and 300 W respectively).

The main heat dissipator must be sufficiently large and have low R_θ for moderate air velocity, unless liquid cooling is employed.

CIRCUIT CONSIDERATIONS

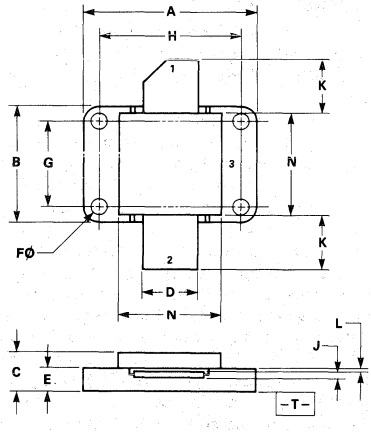
At high power levels (500 W and up), the circuit layout becomes critical due to the low impedance levels and high RF currents associated with the output matching. Some of the components, such as capacitors and inductors must also withstand these currents. The component losses are directly proportional to the operating frequency. The manufacturers specifications on capacitor ratings should be consulted on these aspects prior to design.

Push-pull circuits are less critical in general, since the ground referenced RF loops are practically eliminated, and the impedance levels are higher for a given power output. High power broadband transformers are also easier to design than comparable LC matching networks.

EQUIVALENT TRANSISTOR PARAMETER TERMINOLOGY

Collector	Drain
Emitter	Source
Base	Gate
$V_{(BR)CES}$	$V_{(BR)DSS}$
V_{CBO}	V_{DGO}
I_C	I_D
I_{CES}	I_{DSS}
I_{EBO}	I_{GSS}
$V_{BE(on)}$	$V_{GS(th)}$
$V_{CE(sat)}$	$V_{DS(on)}$
C_{ib}	C_{iss}
C_{ob}	C_{oss}
h_{fe}	g_{fs}
$R_{CE(sat)} = \frac{V_{CE(sat)}}{I_C}$	$r_{DS(on)} = \frac{V_{DS(on)}}{I_D}$

OUTLINE DIMENSIONS



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS BOTH A DATUM AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR F DIAMETER. ⌖ | ϕ 0.25 (.010) Ⓜ | T | A Ⓜ | B Ⓜ |
3. DIMENSIONING AND TOLERANCING PER Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

STYLE 2:
PIN 1. DRAIN
2. GATE
3. SOURCE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	37.85	38.35	1.490	1.510
B	25.15	25.65	0.990	1.010
C	8.38	8.89	0.330	0.350
D	12.45	12.95	0.490	0.510
E	4.95	5.21	0.195	0.205
F	3.05	3.30	0.120	0.130
G	19.05 BSC		0.750 BSC	
H	31.75 BSC		1.250 BSC	
J	1.14	1.39	0.045	0.055
K	10.54	11.05	0.415	0.435
L	0.10	0.15	0.004	0.006
N	22.87	23.11	0.890	0.910

CASE 368-01

MRF161

The RF Line

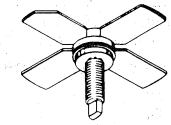
5.0 W 2.0–400 MHz

N-CHANNEL TMOS BROADBAND RF POWER FET

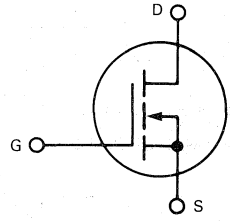
N-CHANNEL ENHANCEMENT-MODE TMOS RF POWER FIELD-EFFECT TRANSISTOR

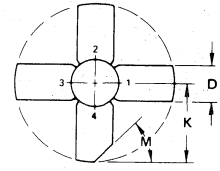
. . . designed for wideband large-signal amplifier and oscillator applications in the 2.0 to 400 MHz range.

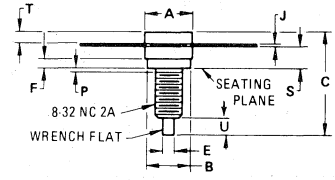
- Guaranteed 28 Volt, 400 MHz Performance
  Output Power = 5.0 Watts
  Minimum Gain = 11 dB
  Efficiency = 50% (Typical)
- Small-Signal and Large-Signal Characterization
- 100% Tested for Load Mismatch At All Phase Angles With 30:1 VSWR
- Low Noise Figure — 3.0 dB (Typ) at 100 mA, 400 MHz
- Excellent Thermal Stability, Ideally Suited For Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques



TMOS™







STYLE 3:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.06	7.26	0.278	0.286
B	6.20	6.50	0.244	0.256
C	14.99	16.51	0.590	0.650
D	5.46	5.96	0.215	0.235
E	1.40	1.65	0.055	0.065
F	1.52	–	0.060	–
J	0.08	0.17	0.003	0.007
K	11.05	–	0.435	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
S	3.00	3.25	0.118	0.128
T	1.40	1.78	0.055	0.070
U	2.92	3.68	0.115	0.145

CASE 244-04

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate-Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	0.9	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	17.5 0.10	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

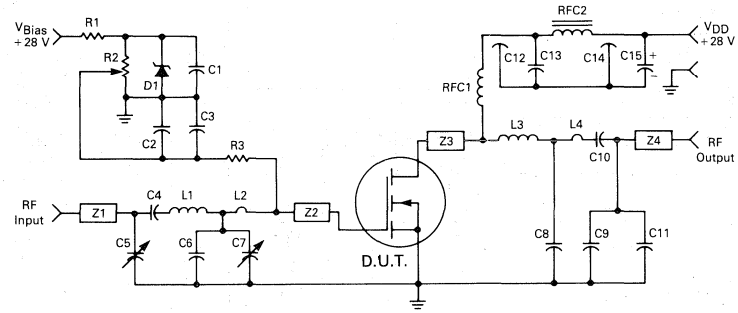
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Resonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	1.0	mAdc
Gate-Source Leakage Current (V_{GS} = 40 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 10 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 100 mA)	g_{fs}	80	110	—	mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	7.0	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	9.7	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	2.3	—	pF
FUNCTIONAL CHARACTERISTICS (Figure 1)					
Noise Figure (V_{DS} = 28 Vdc, I_D = 100 mA, f = 400 MHz, Z_S = 67.6 + j14.1, Z_L = 14.5 + j25.7)	NF	—	3.0	—	dB
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 5.0 W, f = 400 MHz, I_{DQ} = 50 mA)	G_{ps}	11	13.5	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 5.0 W, f = 400 MHz, I_{DQ} = 50 mA)	η	45	50	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 5.0 W, f = 400 MHz, I_{DQ} = 50 mA, VSWR 30:1 at All Phase Angles)	ψ	No Degradation in Output Power			

FIGURE 1 — 400 MHz TEST CIRCUIT



C1, C2, C13 — 0.1 μF, 50 V Disc Ceramic
C3 — 0.01 μF, 100 V Disc Ceramic
C4, C10 — 220 pF, 100 Mil Chip Cap
C5 — 1–10 pF Johanson or Equivalent
C6 — 5.0 pF Mini-Unleco or Equivalent
C7 — 1–20 pF Johanson or Equivalent
C8 — 15 pF, 100 Mil ATC Chip Cap or Equivalent
C9, C11 — 2.2, 100 Mil ATC Chip Cap or Equivalent
C12, C14 — 680 pF Feedthru
C15 — 50 μF, 35 V
R1 — 1.6 kΩ, 1/4 W
R2 — 10 Turns 10 kΩ
R3 — 10 k, 1/2 W
D1 — 1N5347B Motorola Zener or Equivalent

L1 — 1-3/4 Turns, 0.185" ID 0.08" Long #20 AWG Enamel — (25 nH)
L2 — #20 AWG Enamel, Hairpin 0.353" — (10.5 nH), 0.185"

L3 — 1-3/4 Turns, 0.128" ID 0.11" Long #18 AWG Enamel — (15 nH)
L4 — #18 AWG Enamel, Hairpin 0.410" — (12.5 nH), 0.185"

RFC1 — 10 Turns, 0.300" ID #20 AWG Enamel Closewound
RFC2 — Ferroxcube VK-200
Z1 — 0.82" x 0.164" Microstrip — (Z_O = 50 Ω)
Z2, Z3 — 0.60" x 0.25" Microstrip
Z4 — 0.76" x 0.164" Microstrip — (Z_O = 50 Ω)
Board-Glass Teflon, 62 Mils, ϵ_r = 2.56

FIGURE 2 — OUTPUT POWER versus INPUT POWER

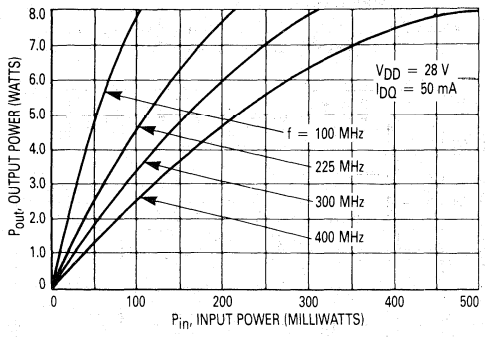


FIGURE 3 — OUTPUT POWER versus INPUT POWER

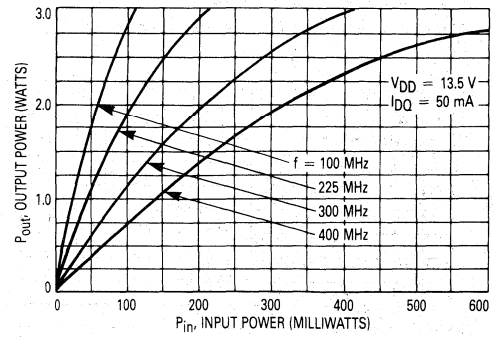


FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 400 MHz

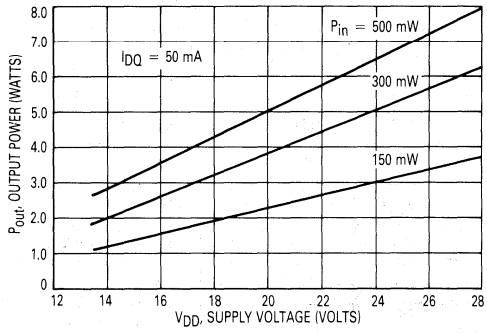


FIGURE 5 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 300 MHz

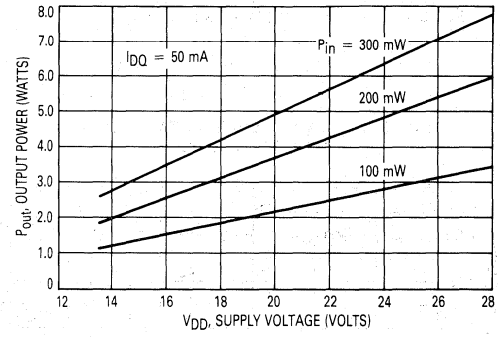


FIGURE 6 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 225 MHz

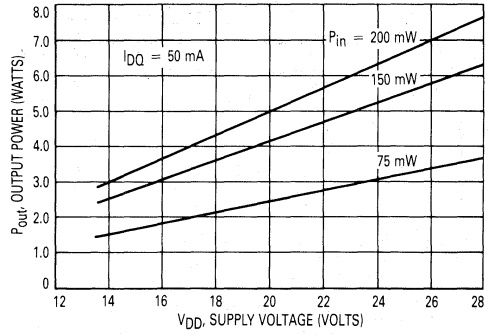


FIGURE 7 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 100 MHz

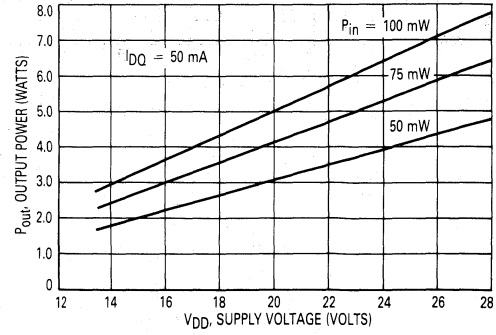


FIGURE 8 — OUTPUT POWER versus GATE VOLTAGE

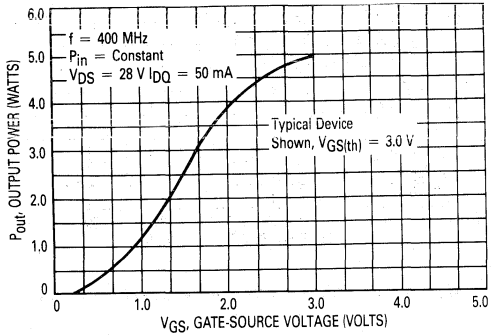


FIGURE 9 — DRAIN CURRENT versus GATE VOLTAGE (TRANSFER CHARACTERISTICS)

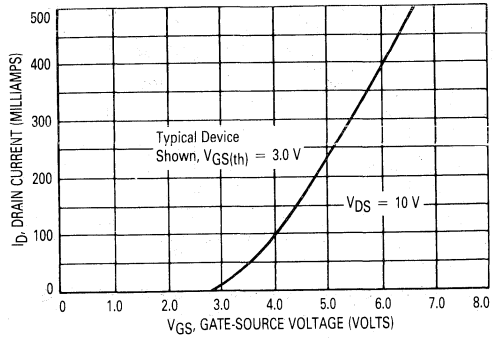


FIGURE 10 — GATE-SOURCE VOLTAGE versus CASE TEMPERATURE

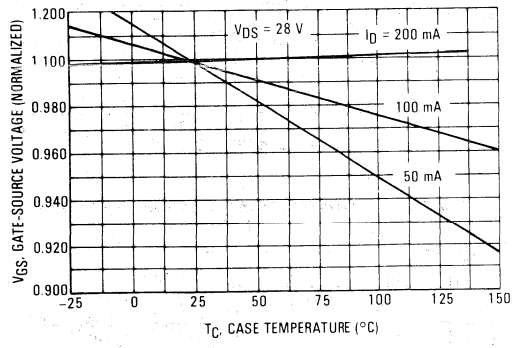


FIGURE 11 — CAPACITANCE versus VOLTAGE

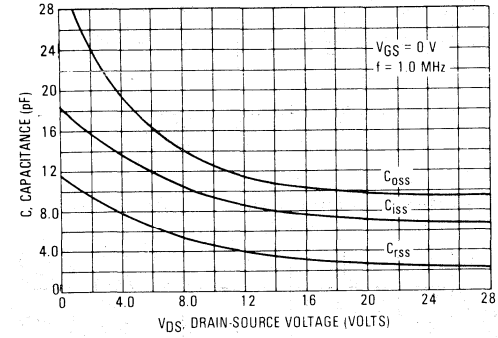


FIGURE 12 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

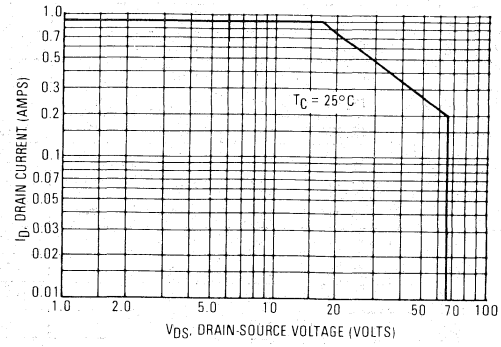
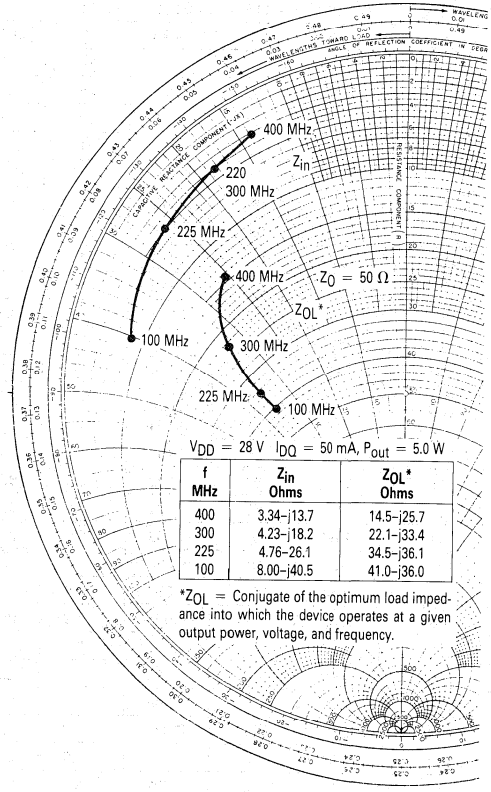


FIGURE 13 — LARGE-SIGNAL SERIES EQUIVALENT INPUT AND OUTPUT IMPEDANCE, Z_{in}, Z_{OL}*



f MHz	Z_{in} Ohms	Z_{OL}* Ohms
400	3.34–j13.7	14.5–j25.7
300	4.23–j18.2	22.1–j33.4
225	4.76–26.1	34.5–j36.1
100	8.00–j40.5	41.0–j36.0

*Z_{OL} = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

FIGURE 14 — COMMON SOURCE SCATTERING PARAMETERS
50 OHM SYSTEM
V_{DS} = 28 V, I_D = 250 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
2.0	1.000	−1.69	13.64	178	0.002	62	0.947	−1.84
5.0	1.000	−4.63	13.60	176	0.005	69	0.945	−4.00
10	0.997	−8.95	13.70	173	0.010	80	0.941	−7.92
20	0.989	−17.49	13.36	167	0.022	73	0.929	−15.8
30	0.977	−26	13.07	162	0.032	71	0.915	−23
40	0.968	−34	12.76	156	0.042	67	0.902	−30
50	0.949	−42	12.31	151	0.050	61	0.885	−37
60	0.930	−49	11.88	146	0.058	57	0.866	−43
70	0.913	−56	11.45	141	0.066	53	0.846	−49
80	0.897	−62	10.96	137	0.072	50	0.831	−55
90	0.885	−68	10.50	133	0.078	46	0.817	−60
100	0.867	−74	10.00	129	0.081	43	0.800	−65
110	0.853	−78	9.54	125	0.085	40	0.787	−69
120	0.838	−84	8.92	122	0.090	37	0.775	−74
130	0.819	−88	8.75	119	0.093	35	0.762	−78
140	0.812	−92	8.30	116	0.096	31	0.755	−81
150	0.800	−96	7.95	113	0.098	28	0.742	−86
160	0.785	−99	7.54	111	0.100	26	0.735	−89
170	0.775	−103	7.25	109	0.102	24	0.728	−93
180	0.765	−105	6.85	106	0.103	23	0.725	−96
190	0.755	−108	6.60	104	0.104	21	0.720	−98
200	0.740	−111	6.20	100	0.106	18	0.719	−99
225	0.735	−116	5.71	96	0.110	16	0.715	−103
250	0.723	−121	5.17	92	0.112	12	0.708	−107
275	0.720	−124	4.80	89	0.113	10	0.706	−110
300	0.716	−128	4.43	85	0.112	7.0	0.706	−113
325	0.715	−130	4.17	83	0.111	4.0	0.717	−115
350	0.715	−133	3.87	79	0.111	3.0	0.720	−117
375	0.715	−135	3.67	76	0.111	1.0	0.728	−118
400	0.711	−137	3.43	74	0.109	0	0.729	−119
425	0.714	−139	3.25	71	0.104	0	0.738	−120
450	0.717	−140	3.11	69	0.104	−2.0	0.743	−121
475	0.719	−141	2.95	67	0.103	−3.0	0.757	−122
500	0.722	−142	2.81	65	0.102	−4.0	0.770	−122
525	0.723	−144	2.69	62	0.099	−6.0	0.777	−123
550	0.727	−144	2.55	61	0.097	−6.0	0.787	−123
575	0.729	−145	2.46	59	0.097	−7.0	0.802	−124
600	0.733	−146	2.37	57	0.094	−7.0	0.814	−124
625	0.734	−147	2.29	55	0.090	−8.0	0.824	−126
650	0.740	−148	2.19	54	0.087	−8.0	0.830	−127
675	0.749	−149	2.12	53	0.085	−6.0	0.849	−127
700	0.758	−149	2.07	51	0.084	−6.0	0.879	−127
725	0.761	−150	1.99	49	0.082	−5.0	0.886	−127
750	0.763	−151	1.93	48	0.081	−4.0	0.905	−127
775	0.765	−151	1.90	48	0.079	−3.0	0.919	−128
800	0.770	−152	1.83	46	0.076	−1.0	0.921	−128

FIGURE 15 — S_{11}, INPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V, I_D = 250 mA

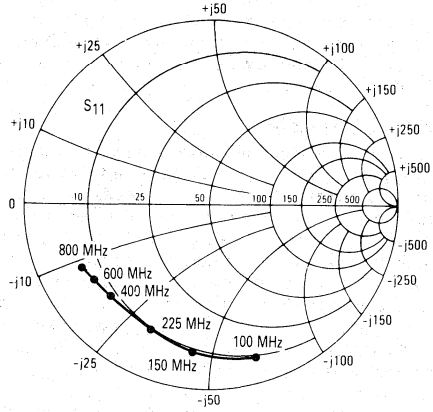


FIGURE 16 — S_{12}, REVERSE TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V, I_D = 250 mA

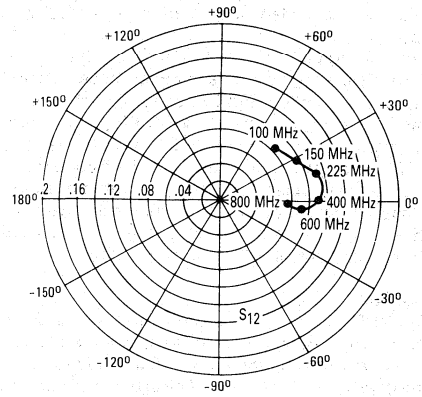


FIGURE 17 — S_{21}, FORWARD TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V, I_D = 250 mA

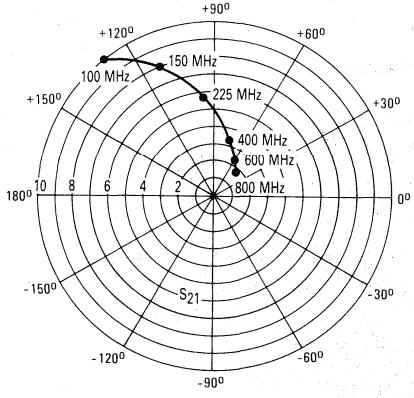
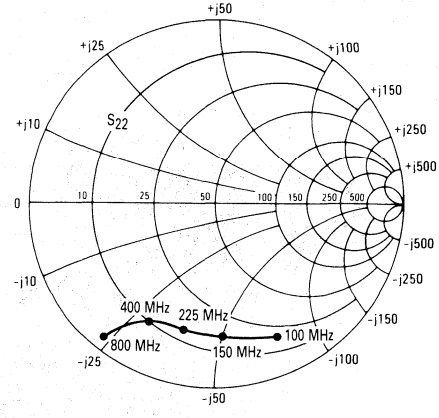


FIGURE 18 — S_{22}, OUTPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{OS} = 28 V, I_D = 250 mA



3

DESIGN CONSIDERATIONS

The MRF161 is a TMOS RF power N-Channel enhancement mode field-effect transistor (FET) designed especially for UHF power amplifier and oscillator applications. Motorola TMOS FETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V-groove vertical power FETs.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of TMOS RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF161 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 9 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF161 was characterized at I_{DQ} = 50 mA, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some applications may require a more elaborate bias system.

GAIN CONTROL

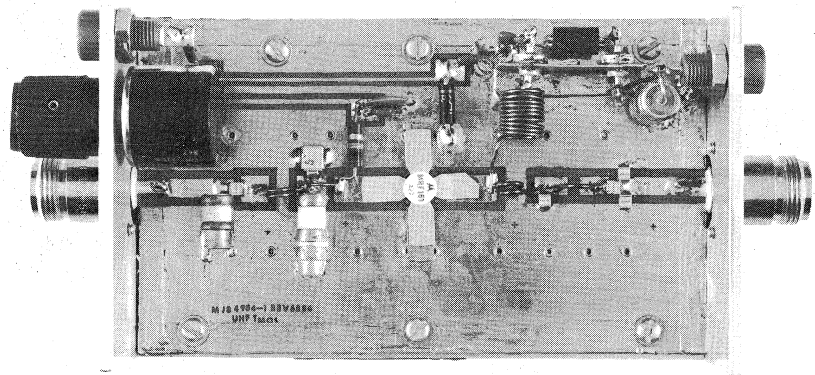
Power output of the MRF161 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC, and modulation systems. (See Figure 8.)

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar UHF transistors are suitable for the MRF161. See Motorola Application Note AN721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of TMOS FETs helps ease the task of broadband network design. Both small signal scattering parameters and large signal impedances are provided. While the s-parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of TMOS power FETs.

RF power FETs are triode devices and, therefore, not unilateral. This, coupled with the very high gain of the MRF161, yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. Two port parameter stability analysis with the MRF161 s-parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A for a discussion of two port network theory and stability.

FIGURE 19 — 400 MHz TEST CIRCUIT



MRF162

The RF Line

15 W 2.0-400 MHz

N-CHANNEL TMOS
BROADBAND RF POWER

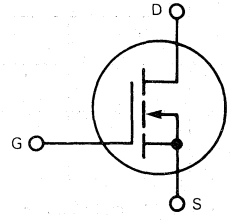
FET

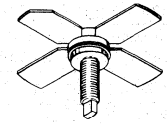
N-CHANNEL ENHANCEMENT-MODE TMOS RF POWER FIELD-EFFECT TRANSISTOR

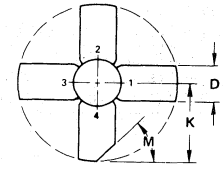
. . . designed for wideband large-signal output and driver applications in the 2.0 to 400 MHz range.

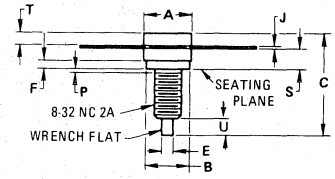
- Guaranteed 28 Volt, 400 MHz Performance
  Output Power = 15 Watts
  Minimum Gain = 11 dB
  Efficiency = 50% (Typical)
- Small-Signal and Large-Signal Characterization
- 100% Tested for Load Mismatch At All Phase Angles With 30:1 VSWR
- Low Noise Figure – 2.0 dB (Typ) at 300 mA, 400 MHz
- Excellent Thermal Stability, Ideally Suited For Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques

TMOS™









STYLE 3:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.06	7.26	0.278	0.286
B	6.20	6.50	0.244	0.256
C	14.99	16.51	0.590	0.650
D	5.46	5.96	0.215	0.235
E	1.40	1.65	0.055	0.065
F	1.52	–	0.060	–
J	0.08	0.17	0.003	0.007
K	11.05	–	0.435	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
S	3.00	3.25	0.118	0.128
T	1.40	1.78	0.055	0.070
U	2.92	3.68	0.115	0.145

CASE 244-04

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate-Source Voltage	V_{GS}	+40	Vdc
Drain Current — Continuous	I_D	2.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.286	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

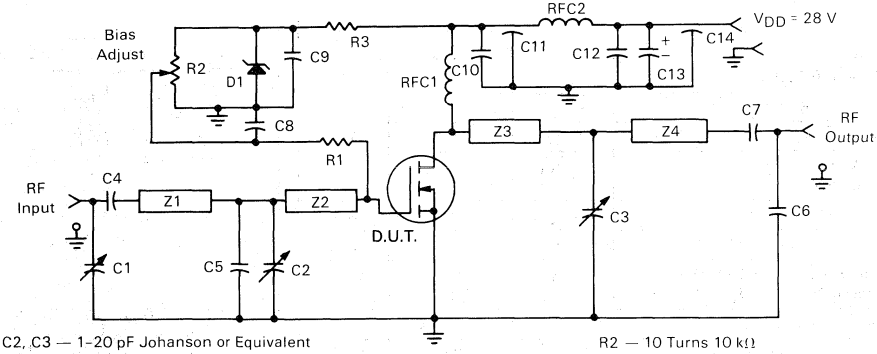
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.5	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	2.0	mAdc
Gate-Source Leakage Current (V_{GS} = 40 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 25 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 250 mA)	g_{fs}	250	400		mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	24	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	27	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	5.5	—	pF
FUNCTIONAL CHARACTERISTICS (Figure 1)					
Noise Figure (V_{DS} = 28 Vdc, I_D = 300 mA, f = 400 MHz, Z_S = 5.9 + j7.8 Ω, Z_L = 3.78 + j5.75 Ω)	NF	—	2.0	—	dB
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 15 W, f = 400 MHz, I_{DQ} = 50 mA)	G_{ps}	11	13.6	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 15 W, f = 400 MHz, I_{DQ} = 50 mA)	η	45	50	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 15 W, f = 400 MHz, I_{DQ} = 50 mA, VSWR 30:1 at All Phase Angles)	ψ	No Degradation in Output Power			

FIGURE 1 — 400 MHz TEST CIRCUIT



C1, C2, C3 — 1-20 pF Johanson or Equivalent
C4, C7 — 270 pF, 100 Mil Chip Cap
C5 — 18 pF Mini-Unleco or Equivalent
C6 — 12 pF, 100 Mil Chip Cap
C8 — 0.01 μF, 50 V Disc Ceramic
C9, C10, C12 — 0.1 μF, 50 V Disc Ceramic
C11, C14 — 680 pF Feedthru
C13 — 20 μF, 50 V
D1 — 1N5925A Motorola Zener
R1 — 10 kΩ, 1/4 W
R2 — 10 Turns 10 kΩ
R3 — 1.6 kΩ, 1/4 W
RFC1 — 10 Turns, 0.300" ID #20 AWG Enamel Closewound
RFC2 — Ferroxcube VK-200 — 19/4B
Z1 — 1.5" × 0.250" Microstrip
Z2 — 0.6" × 0.250" Microstrip
Z3 — 1.3" × 0.250" Microstrip
Z4 — 0.85" × 0.250" Microstrip
Board — Glass Teflon, 62 Mils, ϵ_r = 2.56

FIGURE 2 — OUTPUT POWER versus INPUT POWER

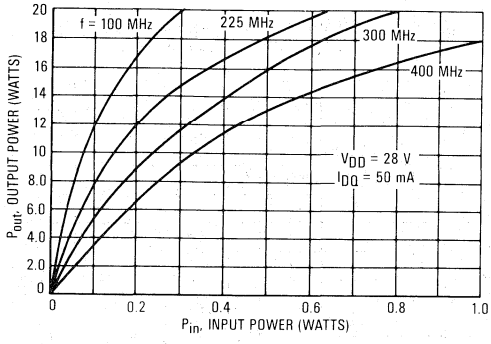


FIGURE 3 — OUTPUT POWER versus INPUT POWER

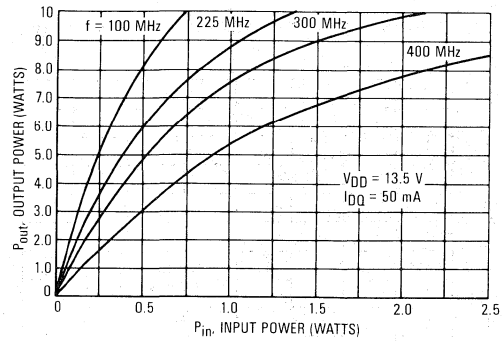


FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 400 MHz

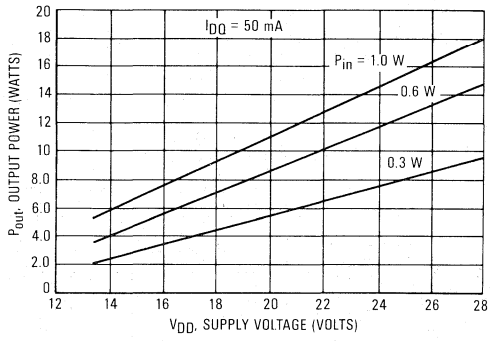


FIGURE 5 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 300 MHz

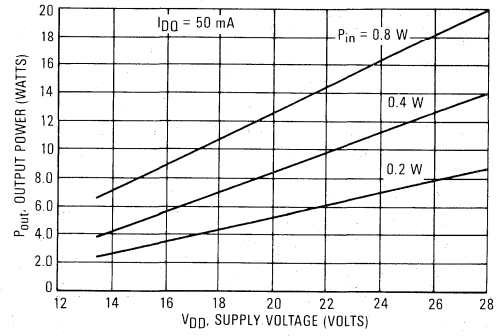


FIGURE 6 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 225 MHz

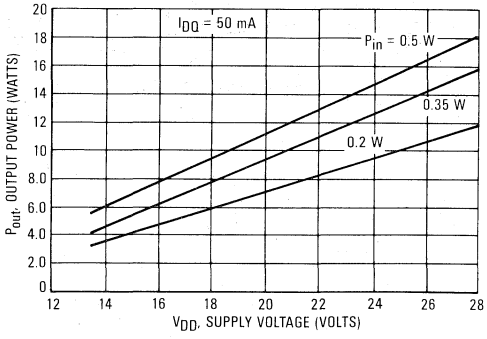
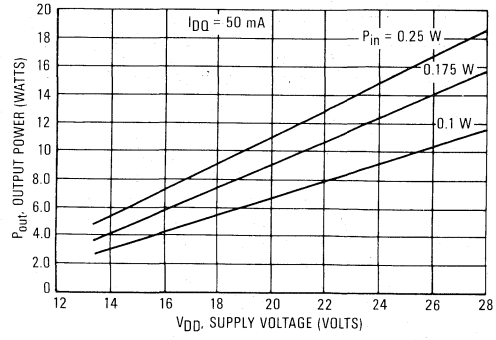


FIGURE 7 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 100 MHz



3

FIGURE 8 — OUTPUT POWER versus GATE VOLTAGE

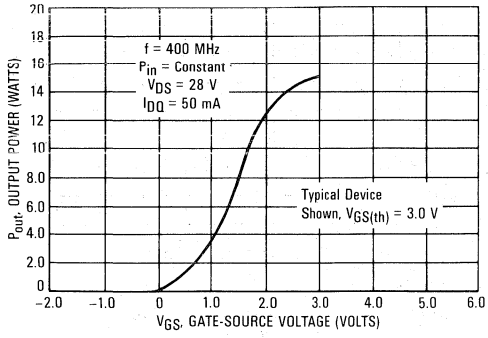


FIGURE 9 — DRAIN CURRENT versus GATE VOLTAGE (TRANSFER CHARACTERISTICS)

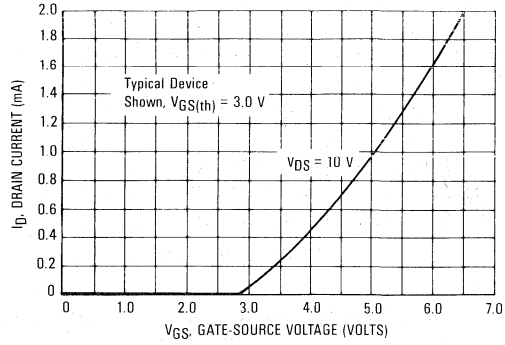


FIGURE 10 — GATE-SOURCE VOLTAGE versus CASE TEMPERATURE

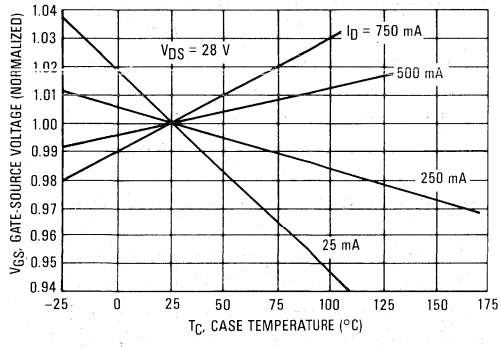


FIGURE 11 — CAPACITANCE versus DRAIN-SOURCE VOLTAGE

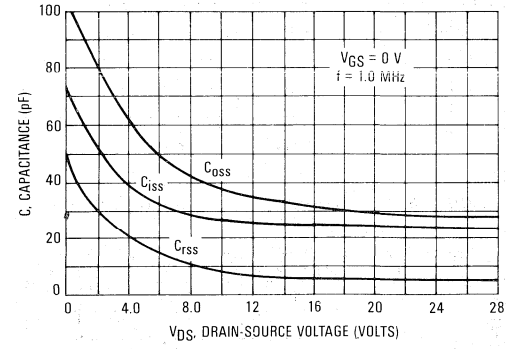


FIGURE 12 — DC SAFE OPERATING AREA

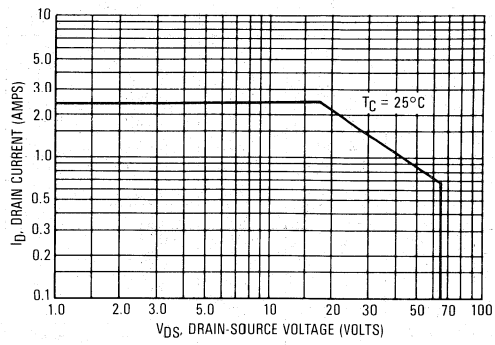
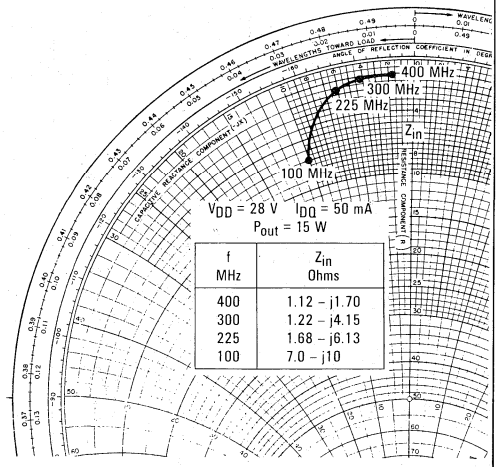
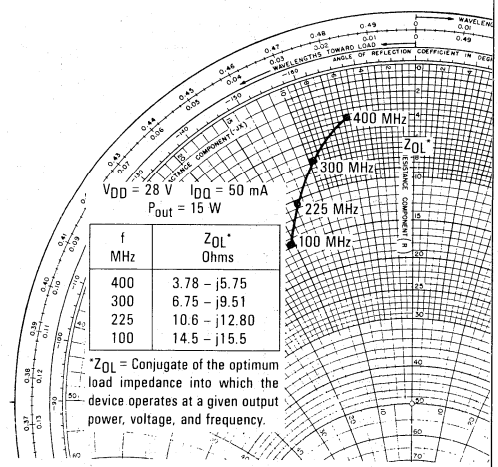


FIGURE 13 — LARGE SIGNAL SERIES EQUIVALENT INPUT IMPEDANCE, Z_{in}



f MHz	Z_{in} Ohms
400	1.12 – j1.70
300	1.22 – j4.15
225	1.68 – j6.13
100	7.0 – j10

FIGURE 14 — LARGE SIGNAL SERIES EQUIVALENT OUTPUT IMPEDANCE, Z_{OL}*



f MHz	Z_{OL}* Ohms
400	3.78 – j5.75
300	6.75 – j9.51
225	10.6 – j12.80
100	14.5 – j15.5

*Z_{OL} = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

3

FIGURE 15 — COMMON SOURCE SCATTERING PARAMETERS
50 OHM SYSTEM
V_{DS} = 28 V, I_D = 0.5 A

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
2.0	0.996	-11	34.29	171	0.007	+80	0.730	-12
5.0	0.983	-27	33.00	159	0.016	+73	0.729	-30
10	0.943	-51	31.76	147	0.030	+60	0.728	-57
20	0.871	-86	24.38	130	0.047	+41	0.726	-94
30	0.833	-109	18.82	118	0.054	+30	0.727	-116
40	0.811	-123	14.93	110	0.058	+23	0.728	-129
50	0.796	-133	12.42	105	0.060	+18	0.729	-138
60	0.788	-140	10.45	101	0.061	+14	0.729	-143
70	0.782	-145	9.13	97	0.061	+11	0.729	-148
80	0.779	-149	8.01	94	0.062	+8.9	0.731	-151
90	0.777	-152	7.12	92	0.062	+7.1	0.733	-153
100	0.776	-155	6.48	89	0.062	+5.3	0.735	-155
110	0.775	-157	5.92	87	0.062	+3.9	0.737	-156
120	0.775	-158	5.45	85	0.062	+2.4	0.739	-158
130	0.775	-160	5.03	83	0.062	+1.5	0.741	-159
140	0.775	-161	4.69	81	0.062	+0.4	0.743	-159
150	0.775	-162	4.37	80	0.061	-0.6	0.744	-160
160	0.777	-163	4.10	78	0.062	-1.3	0.746	-161
170	0.777	-163	3.87	77	0.061	-2.2	0.748	-161
180	0.778	-164	3.65	75	0.061	-2.8	0.750	-161
190	0.780	-165	3.46	74	0.061	-3.7	0.753	-162
200	0.781	-165	3.29	72	0.060	-4.2	0.755	-162
225	0.784	-166	2.87	69	0.060	-5.8	0.765	-163
250	0.788	-166	2.57	66	0.059	-7.7	0.770	-163
275	0.790	-167	2.30	64	0.059	-9.0	0.780	-163
300	0.792	-167	2.20	62	0.059	-11	0.795	-163
325	0.794	-168	1.94	57	0.059	-12	0.812	-163
350	0.794	-169	1.78	56	0.058	-15	0.815	-163
375	0.799	-169	1.67	54	0.057	-16	0.826	-163
400	0.805	-169	1.56	51	0.055	-17	0.836	-163
425	0.815	-169	1.45	50	0.054	-17	0.862	-163
450	0.825	-169	1.39	47	0.053	-17	0.860	-162
475	0.834	-170	1.32	45	0.052	-17	0.871	-162
500	0.837	-170	1.23	42	0.051	-16	0.871	-162
525	0.838	-171	1.16	41	0.050	-14	0.872	-162
550	0.843	-171	1.11	39	0.048	-13	0.883	-162
575	0.845	-172	1.07	37	0.048	-12	0.894	-162
600	0.855	-172	1.03	35	0.046	-10	0.901	-163
625	0.856	-173	0.977	33	0.045	-9.0	0.905	-163
650	0.875	-173	0.947	32	0.044	-7.0	0.921	-163
675	0.885	-173	0.914	30	0.044	-5.0	0.938	-163
700	0.888	-174	0.873	27	0.043	-4.0	0.949	-164
725	0.892	-174	0.841	27	0.042	-1.0	0.947	-164
750	0.900	-174	0.821	26	0.043	+2.0	0.970	-164
775	0.910	-175	0.814	24	0.044	+4.0	0.978	-164
800	0.918	-176	0.775	22	0.045	+8.0	0.978	-164

FIGURE 16 — S_{11}, INPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V, I_D = 0.5 A

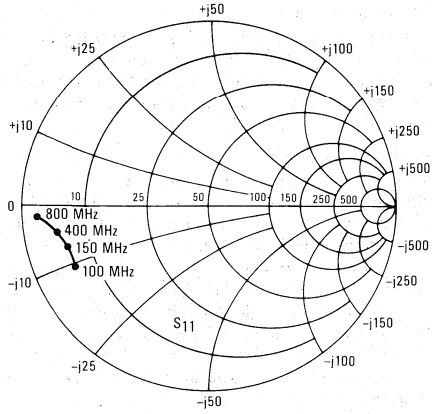


FIGURE 17 — S_{12}, REVERSE TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V, I_D = 0.5 A

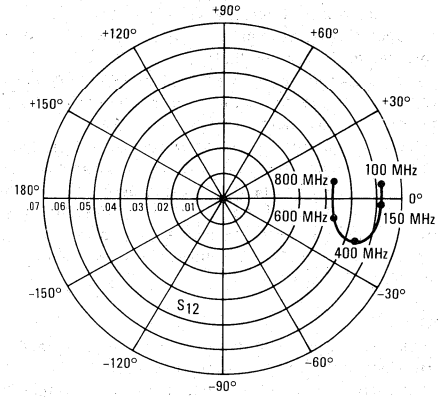


FIGURE 18 – S_{21}, FORWARD TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} 28 V, I_D 0.5 A

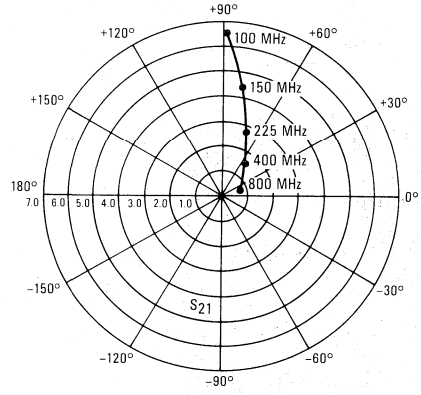
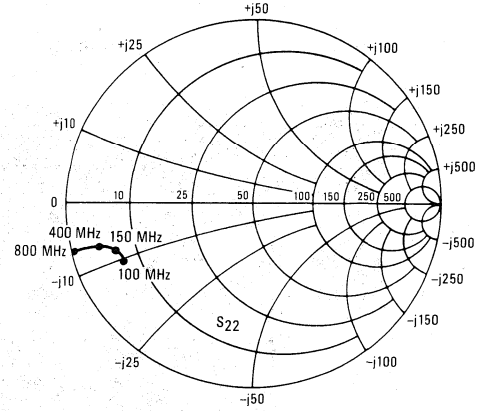


FIGURE 19 – S_{22}, OUTPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} 28 V, I_D 0.5 A



3

DESIGN CONSIDERATIONS

The MRF162 is a TMOS RF power N-Channel enhancement mode field-effect transistor (FET) designed especially for UHF power amplifier applications. Motorola TMOS FETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V-groove vertical power FETs.

Motorola Application Note AN-211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of TMOS RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF162 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 9 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF162 was characterized at I_{DQ} = 50 mA, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some applications may require a more elaborate bias system.

GAIN CONTROL

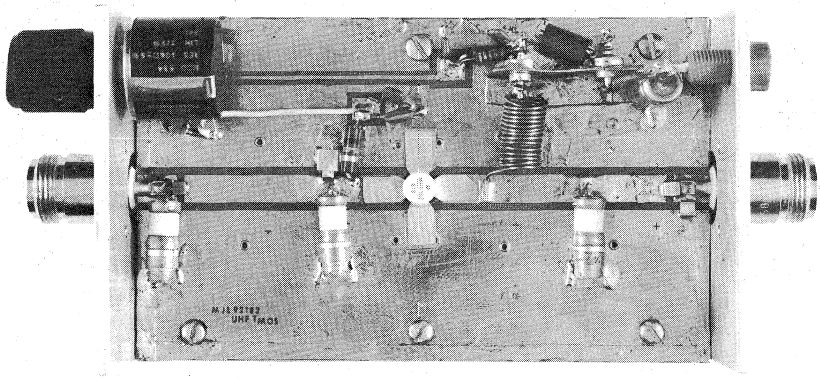
Power output of the MRF162 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC, and modulation systems. (See Figure 8.)

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar UHF transistors are suitable for the MRF162. See Motorola Application Note AN-721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of TMOS FETs helps ease the task of broadband network design. Both small signal scattering parameters and large signal impedances are provided. While the s-parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of TMOS power FETs.

RF power FETs are triode devices and, therefore, not unilateral. This, coupled with the very high gain of the MRF162, yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. Two port parameter stability analysis with the MRF162 s-parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN-215A for a discussion of two port network theory and stability.

FIGURE 20 — 400 MHz TEST CIRCUIT



MRF163

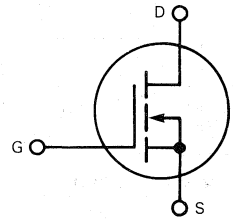
The RF Line

N-CHANNEL ENHANCEMENT-MODE
TMOS RF POWER FIELD-EFFECT TRANSISTOR

. . . designed for wideband large-signal output and driver applications in the 2.0 to 400 MHz range.

- Guaranteed 28 Volt, 400 MHz Performance
  Output Power = 25 Watts
  Minimum Gain = 10 dB
  Efficiency = 50% (Typical)
- Small-Signal and Large-Signal Characterization
- 100% Tested for Load Mismatch At All Phase Angles With 30:1 VSWR
- Low Noise Figure — 2.5 dB (Typ) at 500 mA, 400 MHz
- Excellent Thermal Stability, Ideally Suited For Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques

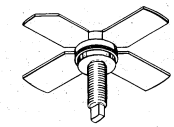
TMOS™

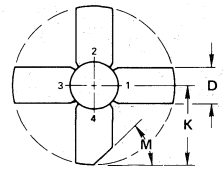


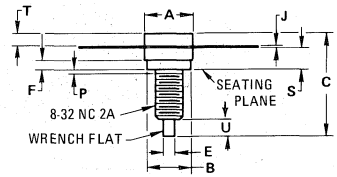
25 W 2.0-400 MHz

N-CHANNEL TMOS
BROADBAND RF POWER

FET







STYLE 3:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.06	7.26	0.278	0.286
B	6.20	6.50	0.244	0.256
C	14.99	16.51	0.590	0.650
D	5.46	5.96	0.215	0.235
E	1.40	1.65	0.055	0.065
F	1.52	–	0.060	–
J	0.08	0.17	0.003	0.007
K	11.05	–	0.435	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
S	3.00	3.25	0.118	0.128
T	1.40	1.78	0.055	0.070
U	2.92	3.68	0.115	0.145

CASE 244-04

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate-Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	5.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	87.5 0.500	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

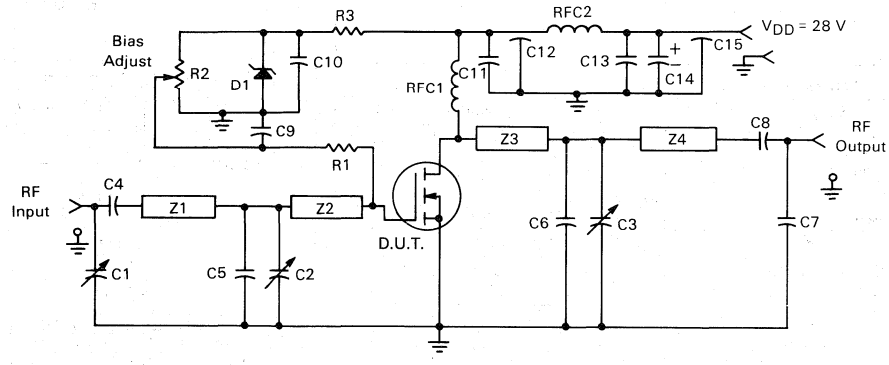
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 10 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	4.0	mAdc
Gate-Source Leakage Current (V_{GS} = 40 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 25 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 500 mA)	g_{fs}	500	750	—	mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	48	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	54	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	11	—	pF
FUNCTIONAL CHARACTERISTICS (Figure 1)					
Noise Figure (V_{DS} = 28 Vdc, I_D = 500 mA, f = 400 MHz, Z_S = 3.23 + j2.57 Ω, Z_L = 2.11 + j2.97 Ω)	NF	—	2.5	—	dB
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 25 W, f = 400 MHz, I_{DQ} = 25 mA)	G_{ps}	10	12	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 25 W, f = 400 MHz, I_{DQ} = 25 mA)	η	45	50	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 25 W, f = 400 MHz, I_{DQ} = 25 mA, VSWR 30:1 at All Phase Angles)	ψ	No Degradation in Output Power			

FIGURE 1 — 400 MHz TEST CIRCUIT



C1, C2, C3 — 1-20 pF Johanson or Equivalent
C4, C8 — 270 pF, 100 Mil Chip Cap
C5, C6 — 18 pF Mini-Unleco or Equivalent
C7 — 12 pF Mini-Unleco or Equivalent
C9 — 0.01 μF, 50 V Disc Ceramic
C10, C11, C13 — 0.1 μF, 50 V Disc Ceramic
C12, C15 — 680 pF Feedthru
C14 — 20 μF, 50 V
D1 — 1N5925A Motorola Zener
R1 — 10 kΩ, 1/4 W
R2 — 10 Turns 10 kΩ
R3 — 1.6 kΩ, 1/4 W
RFC1 — 10 Turns, 0.300" ID #20 AWG Enamel Closewound
RFC2 — Ferroxcube VK-200 — 19/4B
Z1 — 1.350" × 0.250" Microstrip
Z2 — 0.600" × 0.250" Microstrip
Z3 — 0.710" × 0.250" Microstrip
Z4 — 1.300" × 0.250" Microstrip
Board — Glass Teflon, 62 Mils, ϵ_r = 2.56

FIGURE 2 — OUTPUT POWER versus INPUT POWER

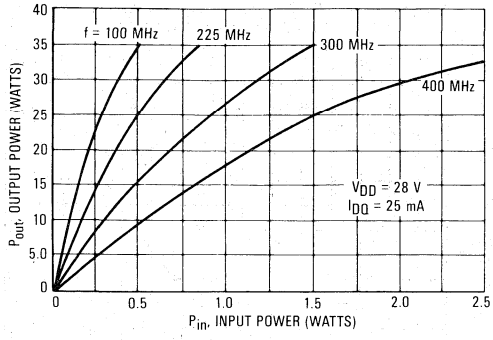


FIGURE 3 — OUTPUT POWER versus INPUT POWER

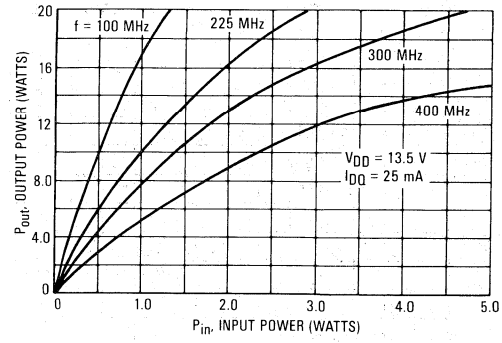


FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 400 MHz

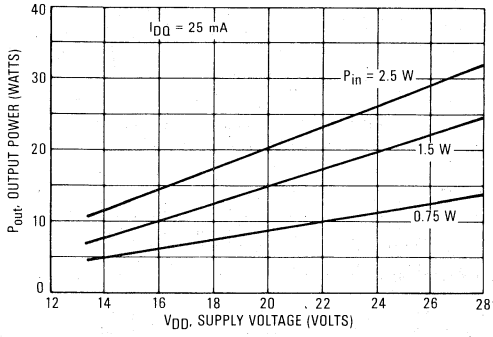


FIGURE 5 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 300 MHz

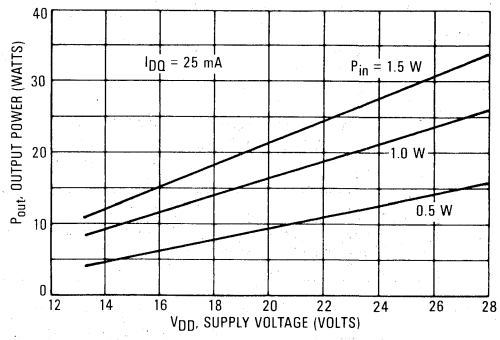


FIGURE 6 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 225 MHz

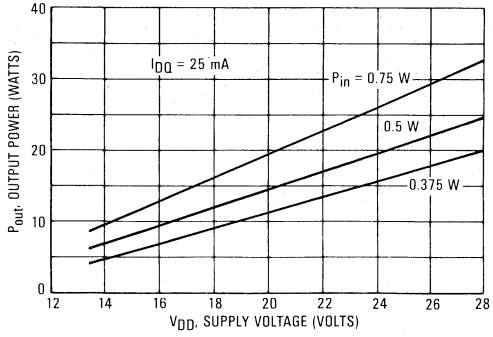
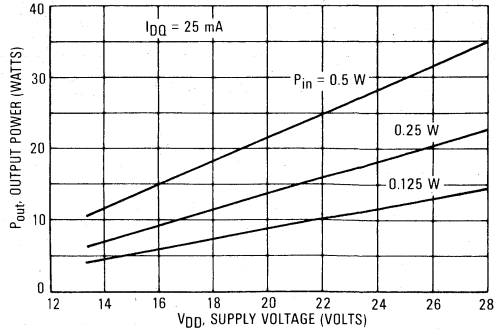


FIGURE 7 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 100 MHz



3

FIGURE 8 — OUTPUT POWER versus GATE VOLTAGE

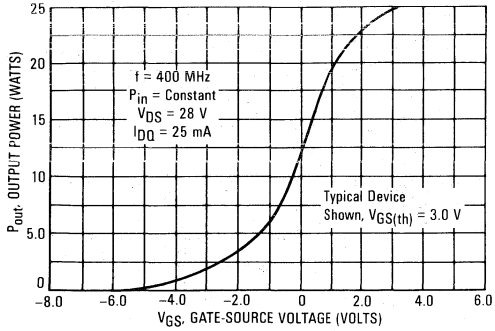
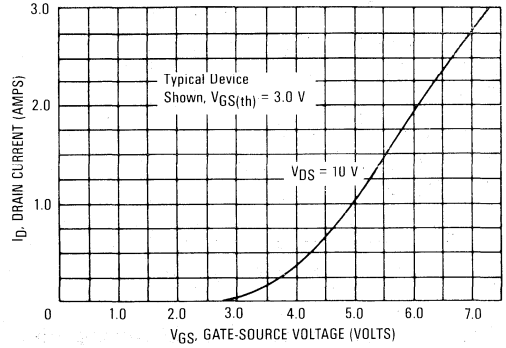


FIGURE 9 — DRAIN CURRENT versus GATE VOLTAGE (TRANSFER CHARACTERISTICS)



3

FIGURE 10 — GATE-SOURCE VOLTAGE versus CASE TEMPERATURE

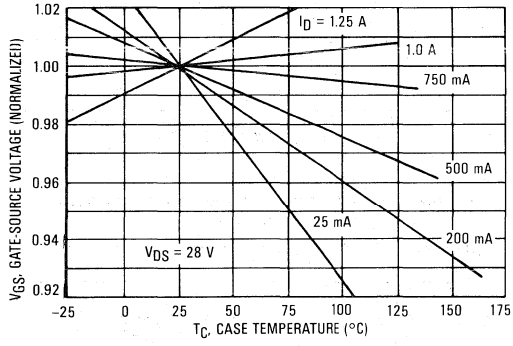


FIGURE 11 — CAPACITANCE versus DRAIN-SOURCE VOLTAGE

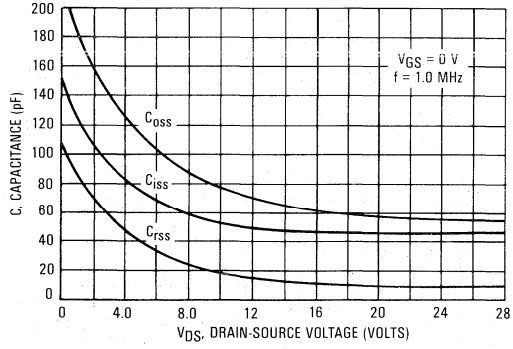


FIGURE 12 — DC SAFE OPERATING AREA

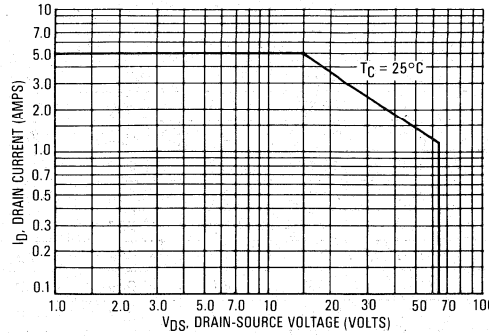
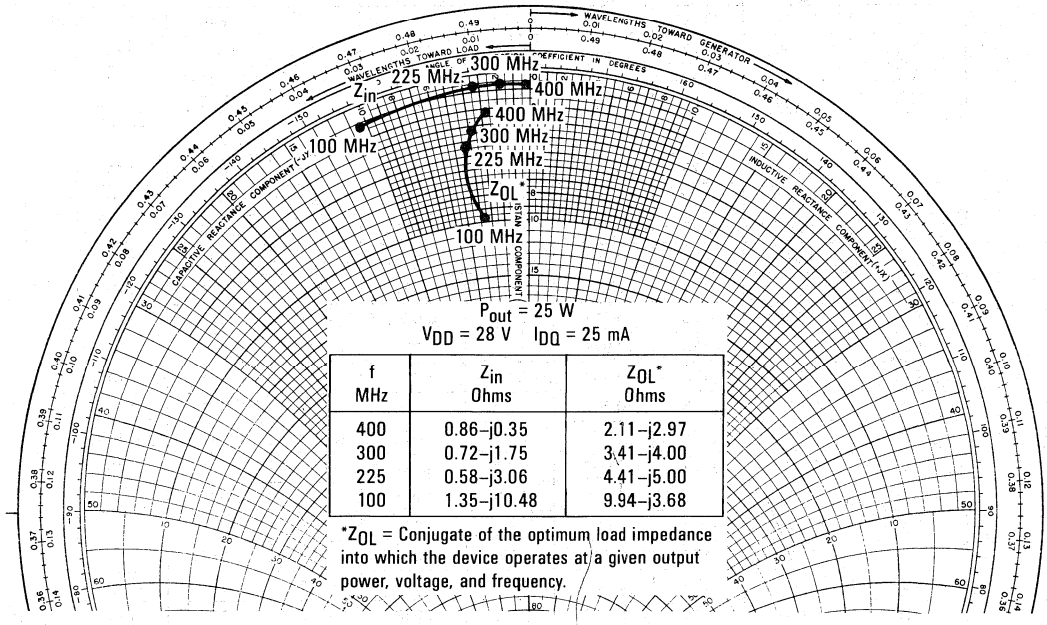


FIGURE 13 — INPUT AND OUTPUT IMPEDANCE



P_{out} = 25 W
V_{DD} = 28 V I_{DQ} = 25 mA

f MHz	Z_{in} Ohms	Z_{OL}^* Ohms
400	0.86–j0.35	2.11–j2.97
300	0.72–j1.75	3.41–j4.00
225	0.58–j3.06	4.41–j5.00
100	1.35–j10.48	9.94–j3.68

*Z_{OL} = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

FIGURE 14 — COMMON SOURCE SCATTERING PARAMETERS
50 OHM SYSTEM
V_{DS} = 28 V, I_D = 0.5 A

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
2.0	0.985	-30	56.97	166	0.010	+63.9	0.611	-36
10	0.875	-105	34.12	125	0.032	+30.6	0.736	-116
25	0.841	-145	16.17	104	0.038	+9.2	0.798	-152
50	0.833	-162	8.201	92.7	0.038	+1.6	0.800	-165
75	0.836	-167	5.496	86.8	0.037	-2.5	0.802	-168
100	0.838	-170	4.121	82.3	0.039	-3.0	0.804	-170
125	0.838	-171	3.255	78.6	0.039	-5.8	0.809	-170
150	0.840	-172	2.718	74.3	0.037	-8.5	0.815	-171
175	0.844	-173	2.326	70.8	0.037	-9.6	0.819	-171
200	0.849	-173	2.027	67.2	0.036	-10.4	0.824	-171
225	0.851	-173	1.782	64.0	0.036	-10.3	0.833	-171
250	0.857	-173	1.593	60.9	0.034	-11.7	0.839	-171
275	0.862	-173	1.438	58.9	0.035	-11.1	0.844	-171
300	0.866	-173	1.319	55.6	0.033	-12.1	0.846	-170
325	0.872	-173	1.209	52.3	0.032	-12.7	0.861	-170
350	0.875	-173	1.110	49.0	0.031	-13.4	0.873	-170
375	0.879	-173	1.030	46.7	0.031	-12.2	0.876	-170
400	0.882	-173	0.966	44.1	0.030	-14.6	0.883	-170
425	0.888	-173	0.904	41.3	0.029	-13.4	0.888	-170
450	0.891	-173	0.836	39.4	0.028	-11.7	0.895	-170
475	0.893	-173	0.792	37.1	0.027	-8.8	0.902	-170
500	0.901	-173	0.748	35.2	0.027	-6.1	0.911	-170
525	0.906	-173	0.715	32.4	0.025	-6.0	0.921	-170
550	0.911	-173	0.679	30.2	0.024	-6.0	0.928	-170
575	0.912	-173	0.637	28.7	0.024	3.9	0.934	-170
600	0.913	-173	0.605	26.9	0.024	-1.0	0.939	-170
625	0.919	-174	0.579	25.3	0.024	+1.0	0.947	-170
650	0.921	-174	0.566	23.0	0.025	+10.1	0.961	-170
675	0.927	-174	0.540	22.6	0.025	+12.1	0.963	-170
700	0.927	-174	0.510	19.9	0.025	+16.5	0.966	-170
725	0.927	-173	0.485	19.5	0.025	+23.1	0.967	-170
750	0.933	-174	0.481	17.4	0.026	+25.3	0.967	-170
775	0.937	-174	0.453	17.2	0.028	+28.0	0.976	-170
800	0.942	-174	0.448	16.8	0.030	+33.8	0.976	-170

FIGURE 15 — S_{11}, INPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V, I_D = 0.5 A

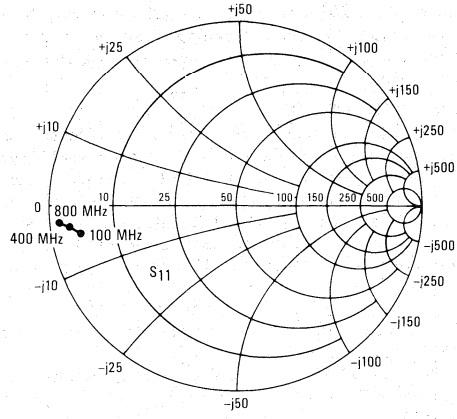


FIGURE 16 — S_{12}, REVERSE TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V, I_D = 0.5 A

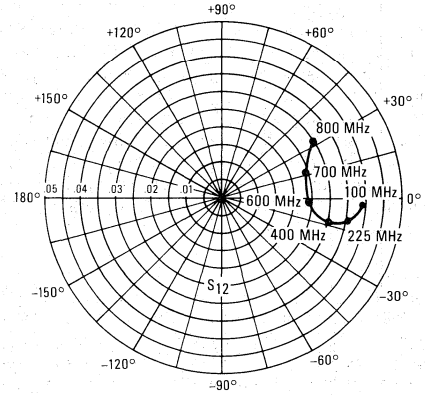


FIGURE 17 — S_{21}, FORWARD TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V, I_D = 0.5 A

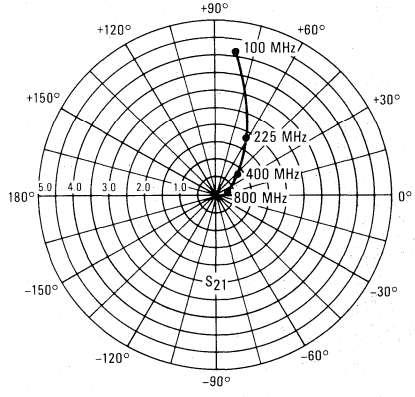
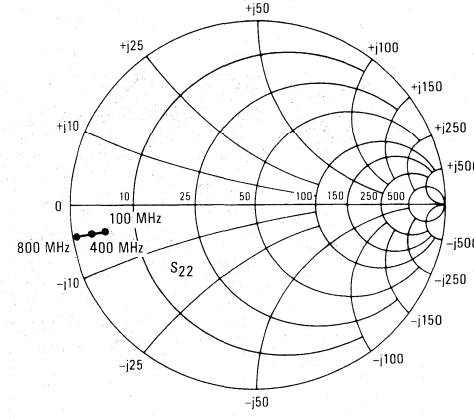


FIGURE 18 — S_{22}, OUTPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V, I_D = 0.5 A



3

DESIGN CONSIDERATIONS

The MRF163 is a TMOS RF power N-Channel enhancement mode field-effect transistor (FET) designed especially for UHF power amplifier applications. Motorola TMOS FETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V-groove vertical power FETs.

Motorola Application Note AN-211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of TMOS RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF163 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 9 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF163 was characterized at I_{DQ} = 25 mA, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some applications may require a more elaborate bias system.

GAIN CONTROL

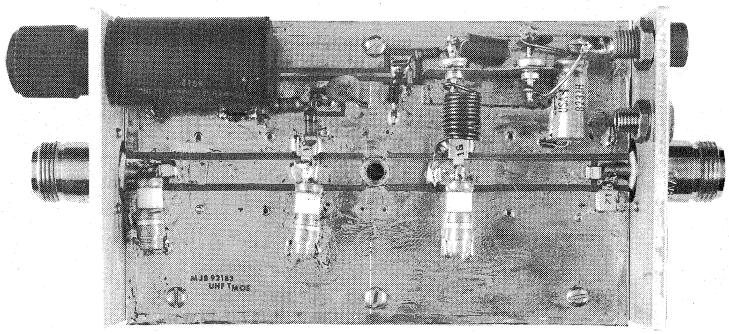
Power output of the MRF163 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC, and modulation systems. (See Figure 8.)

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar UHF transistors are suitable for the MRF163. See Motorola Application Note AN-721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of TMOS FETs helps ease the task of broadband network design. Both small signal scattering parameters and large signal impedances are provided. While the s-parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of TMOS power FETs.

RF power FETs are triode devices and, therefore, not unilateral. This, coupled with the very high gain of the MRF163, yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. Two port parameter stability analysis with the MRF163 s-parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN-215A for a discussion of two port network theory and stability.

FIGURE 19 — 400 MHz TEST CIRCUIT



MRF171

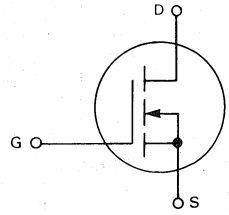
The RF TMOS Line

N-CHANNEL ENHANCEMENT-MODE
TMOS RF POWER FIELD-EFFECT TRANSISTOR

. . . designed primarily for wideband large-signal output and driver stages in the 2.0–200 MHz frequency range.

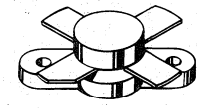
- Guaranteed Performance at 150 MHz, 28 Vdc
  - Output Power = 45 Watts
  - Minimum Gain = 12 dB
  - Efficiency = 50% (Min)
- Facilitates Manual Gain Control, ALC and Modulation Techniques
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR
- Excellent Thermal Stability, Ideally Suited for Class A Operation
- Low Noise Figure — 1.5 dB Typ at 1.0 A, 150 MHz

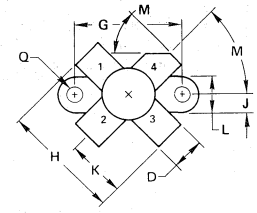
TMOS™



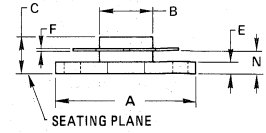
45 W 2.0–200 MHz

N-CHANNEL TMOS
BROADBAND RF POWER
FET





STYLE 2:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	9.40	9.91	0.370	0.390
C	5.82	7.14	0.229	0.281
D	5.46	5.97	0.215	0.235
E	2.16	2.67	0.085	0.105
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	20.07	20.57	0.790	0.810
K	10.03	10.29	0.395	0.405
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.81	4.57	0.150	0.180
Q	2.87	3.30	0.113	0.130

CASE 211-07

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Drain-Gate Voltage	V_{DGR}*	65	Vdc
Gate-Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	4.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	115 0.66	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.52	°C/W

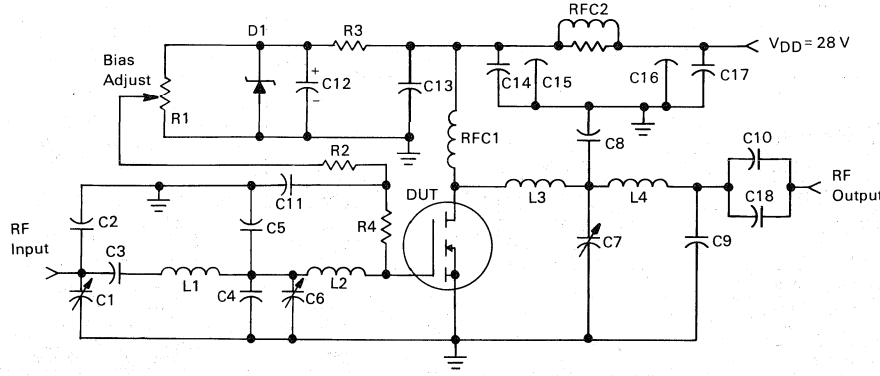
*R_{GS} = 1.0 MΩ

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 10 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	5.0	mAdc
Gate-Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 25 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 1.0 A)	g_{fs}	0.7	1.1	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	55	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	70	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	14	—	pF
FUNCTIONAL CHARACTERISTICS					
Noise Figure (V_{DS} = 28 Vdc, I_D = 1.0 A, f = 150 MHz)	NF	—	1.5	—	dB
Common Source Power Gain (Figure 1) (V_{DD} = 28 Vdc, P_{out} = 45 W, f = 150 MHz, I_{DQ} = 25 mA)	G_{ps}	12	15	—	dB
Drain Efficiency (Figure 1) (V_{DD} = 28 Vdc, P_{out} = 45 W, f = 150 MHz, I_{DQ} = 25 mA)	η	50	60	—	%
Electrical Ruggedness (Figure 1) (V_{DD} = 28 Vdc, P_{out} = 45 W, f = 150 MHz, I_{DQ} = 25 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			

FIGURE 1 — 150 MHz TEST CIRCUIT



C1, C6, C7 — 1.0–20 pF Johanson
C2, C4, C5, C8 — 63 pF ATC Chip (100 mils)
C3, C10, C18 — 680 pF ATC Chip (100 mils)
C9 — 12 pF ATC Chip (100 mils)
C11, C13, C14, C17 — 0.1 μF Erie Redcap, 50 V
C12 — 25 μF, 50 V
C15, C16 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener
L1 — 2 Turns, #18 AWG, 0.3″ ID, 0.3″ Long
L2 — 1-1/4 Turns, #18 AWG, 0.21″ ID
L3 — 1-1/4 Turns, #18 AWG, 0.21″ ID
L4 — 2 Turns, #18 AWG, 0.23″ ID, 0.15″ Long
RFC1 — 20 Turns, #20 AWG Enameled, 0.3″ ID, Close Wound
RFC2 — 15 Turns, #20 AWG Enameled on 2.0 W, 10 Ω Resistor
R1 — 10 kΩ, 10 Turns Helipot 7216-R10K-L.25
R2 — 10 kΩ, 1/4 W
R3 — 1.8 kΩ, 1/2 W
R4 — 47 Ω, 1/2 W

FIGURE 2 — OUTPUT POWER versus INPUT POWER

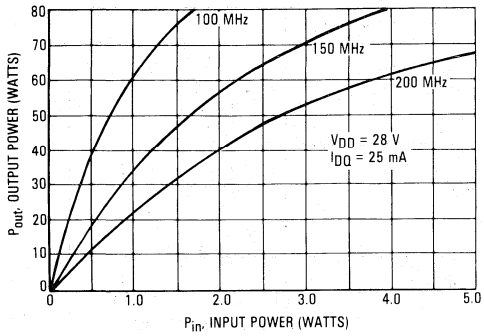


FIGURE 3 — OUTPUT POWER versus INPUT POWER

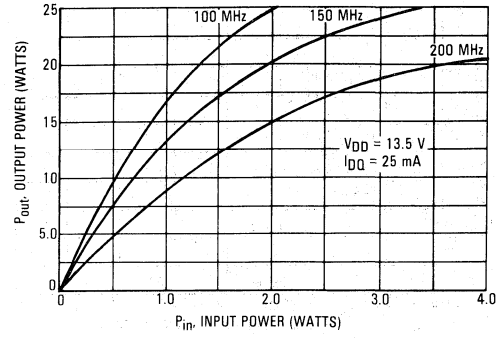


FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 100 MHz

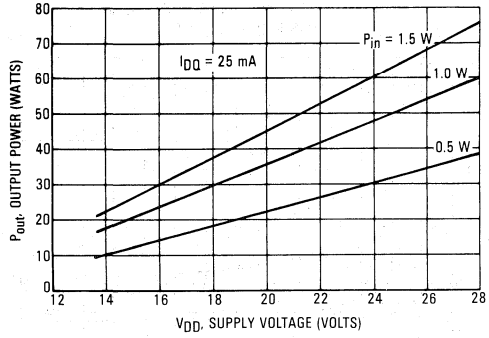


FIGURE 5 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 150 MHz

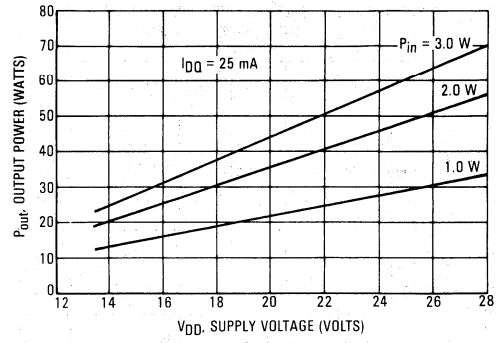


FIGURE 6 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 200 MHz

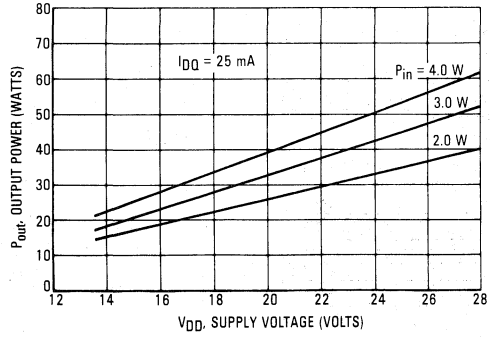
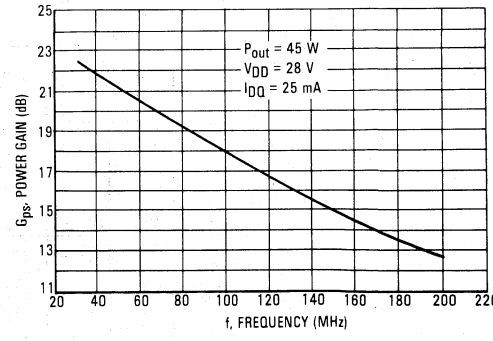


FIGURE 7 — POWER GAIN versus FREQUENCY



3

FIGURE 8 — OUTPUT POWER versus GATE VOLTAGE

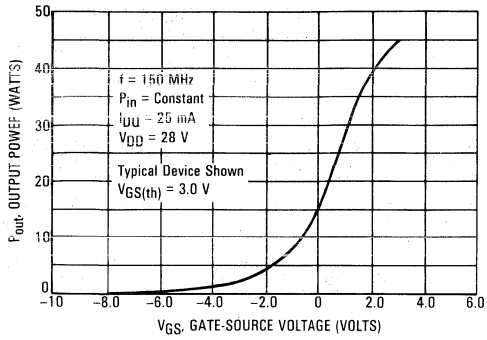


FIGURE 9 — DRAIN CURRENT versus GATE VOLTAGE (TRANSFER CHARACTERISTICS)

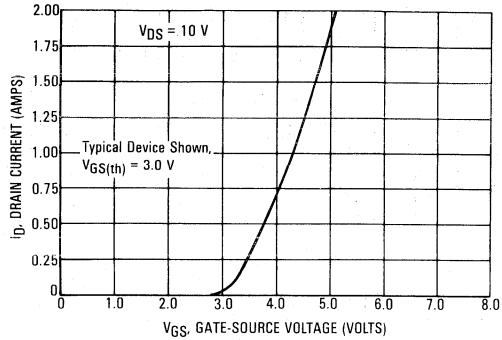


FIGURE 10 — GATE-SOURCE VOLTAGE versus CASE TEMPERATURE

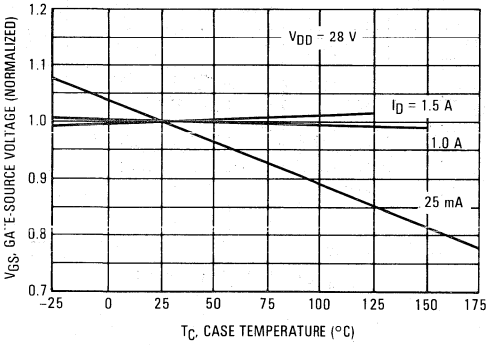


FIGURE 11 — CAPACITANCE versus DRAIN VOLTAGE

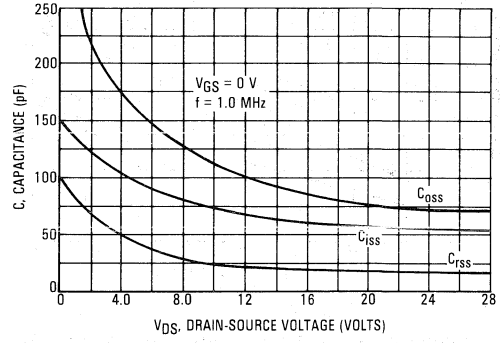


FIGURE 12 — DC SAFE OPERATING AREA

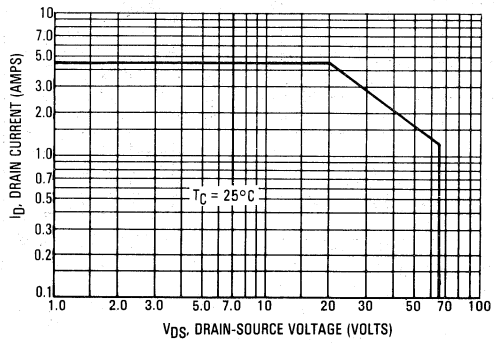


FIGURE 13 — COMMON SOURCE SCATTERING PARAMETERS
V_{DS} = 28 V, I_D = 0.5 A

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
2.0	0.966	-50	72.4	153	0.014	63	0.674	-59
5.0	0.891	-97	50.8	128	0.025	39	0.757	-109
10	0.841	-132	30.1	110	0.030	23	0.801	-141
20	0.821	-155	15.9	99	0.032	14	0.818	-160
30	0.817	-162	10.7	93	0.032	11	0.822	-166
40	0.816	-167	8.06	90	0.032	10	0.823	-169
50	0.816	-169	6.45	88	0.032	11	0.825	-171
60	0.816	-171	5.37	85	0.032	11	0.826	-172
70	0.816	-172	4.60	84	0.032	12	0.828	-173
80	0.816	-172	4.01	82	0.032	13	0.829	-174
90	0.816	-173	3.56	80	0.033	14	0.830	-174
100	0.816	-173	3.15	77	0.034	15	0.832	-174
110	0.816	-173	2.85	76	0.035	16	0.832	-175
120	0.816	-173	2.59	75	0.036	18	0.832	-175
130	0.817	-174	2.40	74	0.036	19	0.832	-175
140	0.817	-174	2.23	72	0.037	20	0.834	-175
150	0.820	-174	2.09	71	0.037	21	0.835	-175
160	0.823	-174	1.97	70	0.037	22	0.836	-175
170	0.825	-175	1.85	69	0.037	23	0.839	-175
180	0.826	-175	1.75	68	0.037	25	0.840	-175
190	0.829	-175	1.66	67	0.037	26	0.843	-175
200	0.832	-175	1.59	66	0.038	27	0.845	-175
250	0.844	-176	1.24	61	0.039	37	0.856	-175
300	0.855	-176	1.02	55	0.042	45	0.867	-174
350	0.862	-177	0.88	51	0.047	53	0.878	-174
400	0.868	-178	0.76	48	0.052	59	0.885	-174
450	0.873	-179	0.67	45	0.059	64	0.897	-174
500	0.907	+179	0.63	42	0.067	67	0.892	-175

FIGURE 14 — S_{11}, INPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 0.5 A

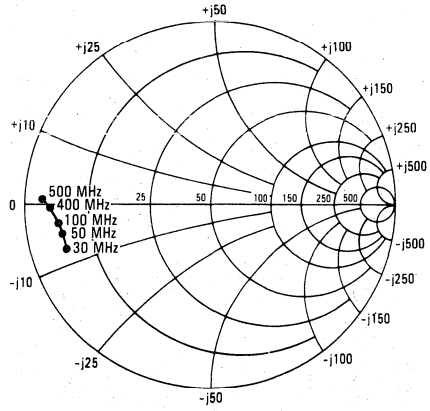


FIGURE 15 — S_{12}, REVERSE TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 0.5 A

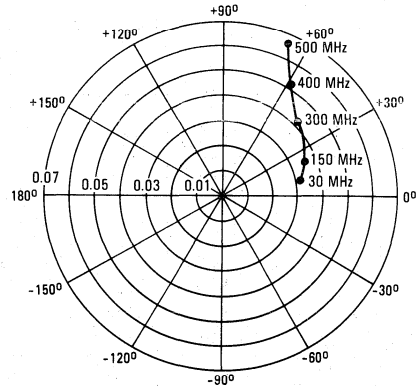


FIGURE 16 — S_{21}, FORWARD TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 0.5 A

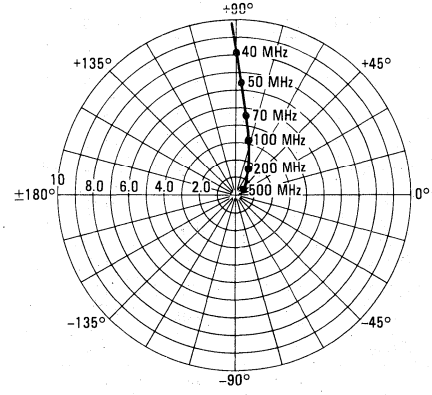
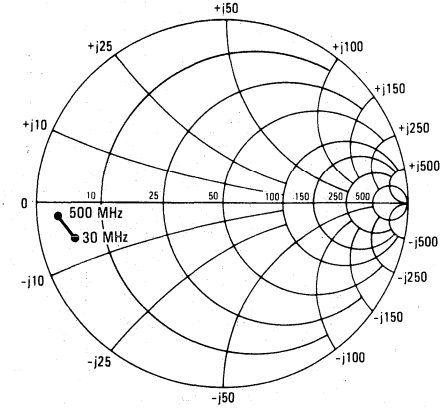


FIGURE 17 — S_{22}, OUTPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 0.5 A



DESIGN CONSIDERATIONS

The MRF171 is a TMOS RF power N-Channel enhancement mode field-effect transistor (FET) designed especially for VHF power amplifier and oscillator applications. Motorola TMOS FETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with "V-groove" vertical power FETs.

Motorola Application Note AN-211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of TMOS RF power FETs include high-gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF171 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 9 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF171 was characterized at I_{DQ} = 25 mA, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF171 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitiates the design of manual gain control, AGC/ALC, and modulation systems. (See Figure 8.)

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar VHF transistors are suitable for MRF171. See Motorola Application Note AN-721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of TMOS FETs helps ease the task of broadband network design. Both small-signal scattering parameters and large-signal impedances are provided. While the s-parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of TMOS power FETs.

RF power FETs are triode devices and, therefore, not unilateral. This, coupled with the very high gain of the MRF171, yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. The MRF171 was characterized with a 47-ohm input shunt loading resistor. Two port parameter stability analysis with the MRF 171 s-parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN-215A for a discussion of two-port network theory and stability.

Input resistive loading is not feasible in low noise applications. The MRF171 noise figure data was generated in a circuit with drain loading and a low loss input network.

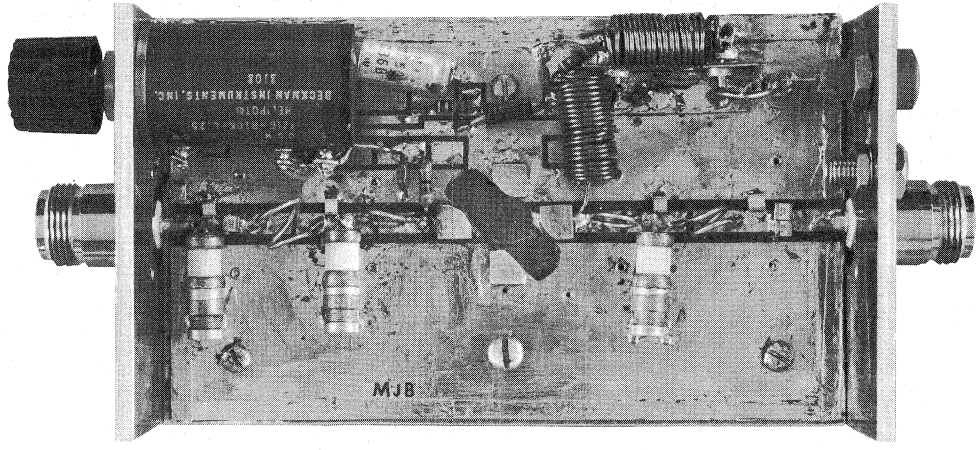
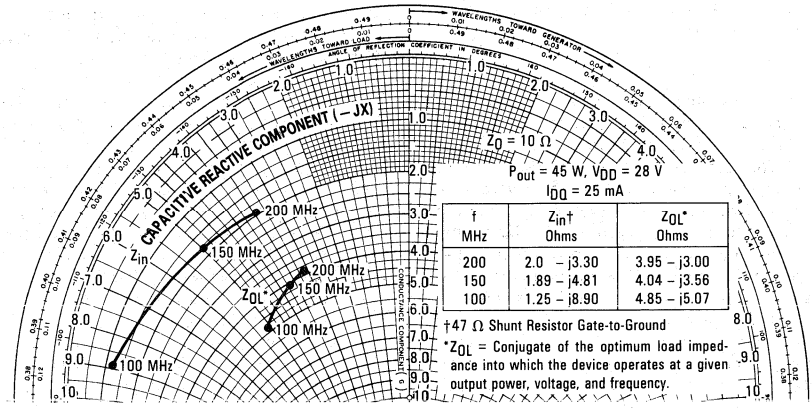


FIGURE 18 — 150 MHz TEST CIRCUIT

FIGURE 19 — LARGE-SIGNAL SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCE



f MHz	Z_{in}† Ohms	Z_{OL}^* Ohms
200	2.0 – j3.30	3.95 – j3.00
150	1.89 – j4.81	4.04 – j3.56
100	1.25 – j8.90	4.85 – j5.07

†47 Ω Shunt Resistor Gate-to-Ground

*Z_{OL} = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

MRF172

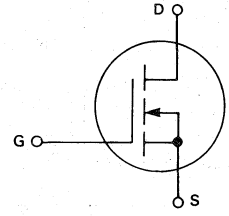
The RF TMOS Line

N-CHANNEL ENHANCEMENT-MODE
TMOS RF POWER FIELD-EFFECT TRANSISTOR

. . . designed primarily for wideband large-signal output and driver stages in the 2.0–200 MHz frequency range.

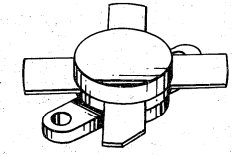
- Guaranteed Performance at 150 MHz, 28 Vdc
  Output Power = 80 Watts
  Minimum Gain = 10 dB
  Efficiency = 50% (Min)
- Excellent Thermal Stability, Ideally Suited for Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR
- Low Noise Figure— 1.5 dB Typ at 2.0 A, 150 MHz

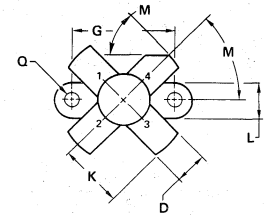
TMOS™

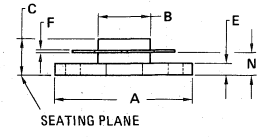


80 W 2.0–200 MHz

N-CHANNEL TMOS
BROADBAND RF POWER
FET







STYLE 2:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	11.81	12.95	0.465	0.510
C	5.82	6.98	0.229	0.275
D	5.46	5.97	0.216	0.235
E	2.13	2.79	0.084	0.110
F	0.08	0.18	0.003	0.007
G	18.29	18.54	0.720	0.730
K	11.05	–	0.435	–
L	6.22	6.48	0.246	0.255
M	45° NOM		45° NOM	
N	3.66	4.52	0.144	0.178
Q	2.92	3.30	0.115	0.130

CASE 211-11

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain — Source Voltage	V_{DSS}	65	Vdc
Drain — Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate — Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	9.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	220 1.26	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

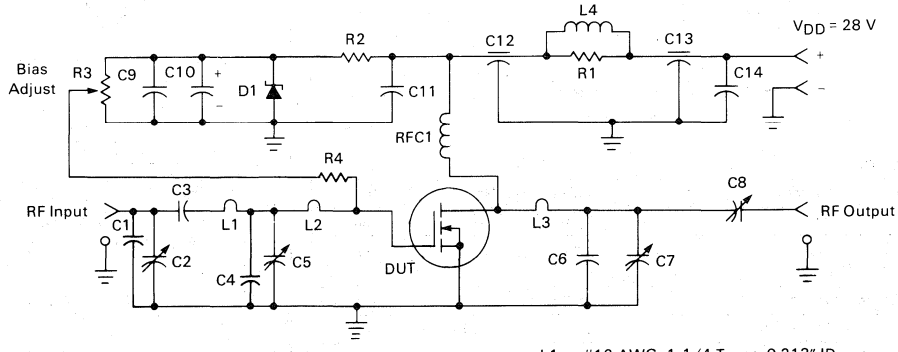
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.80	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 50 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	5.0	mAdc
Gate-Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 50 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 2.0 A)	g_{fs}	1.2	1.8	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	100	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	135	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	26	—	pF
FUNCTIONAL CHARACTERISTICS (Figure 1)					
Noise Figure (V_{DD} = 28 Vdc, I_D = 2.0 A, f = 150 MHz)	NF	—	1.5	—	dB
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA)	G_{ps}	10	12.3	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA)	η	50	60	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			

FIGURE 1 — 150 MHz TEST CIRCUIT



C1 — 25 pF Unleco
C2, C5, C7 — Arco 462, 5–80 pF
C3 — 100 pF Unleco
C4 — 40 pF Unleco
C6 — 60 pF Unleco
C8 — Arco 463, 9–180 pF
C9, C11, C14 — 0.1 μF Erie Redcap
C10 — 50 μF, 50 V
C12, C13 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener

L1 — #16 AWG, 1-1/4 Turns, 0.213″ ID
L2 — #16 AWG, Hairpin 0.25″ × 0.062″
L3 — #14 AWG, Hairpin 0.47″ × 0.2″
L4 — 10 Turns #16 AWG Enameled Wire on R1
RFC1 — 18 Turns #16 AWG Enameled Wire, 0.3″ ID
R1 — 10 Ω, 2.0 W
R2 — 1.8 kΩ, 1/2 W
R3 — 10 kΩ, 10 Turn Bourns
R4 — 10 kΩ, 1/4 W

FIGURE 2 — OUTPUT POWER versus INPUT POWER

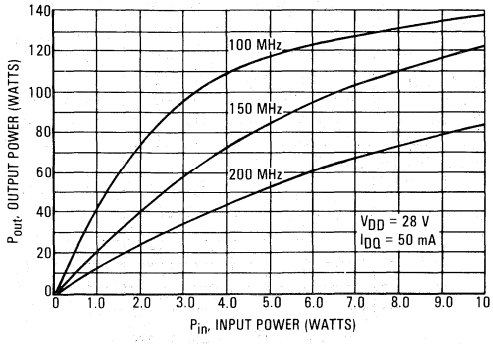


FIGURE 3 — OUTPUT POWER versus INPUT POWER

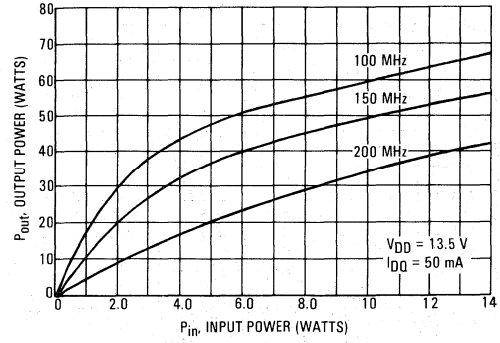


FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 100 MHz

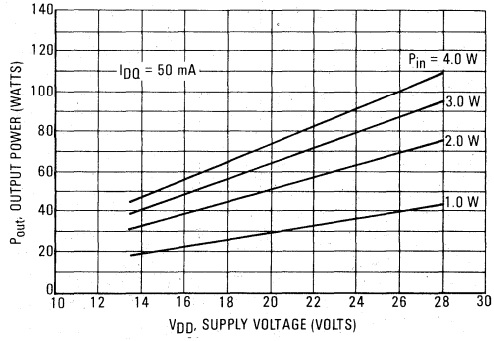


FIGURE 5 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 150 MHz

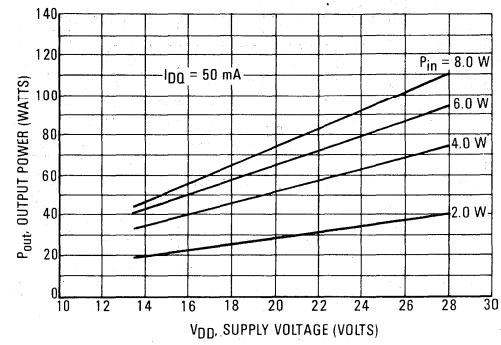


FIGURE 6 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 200 MHz

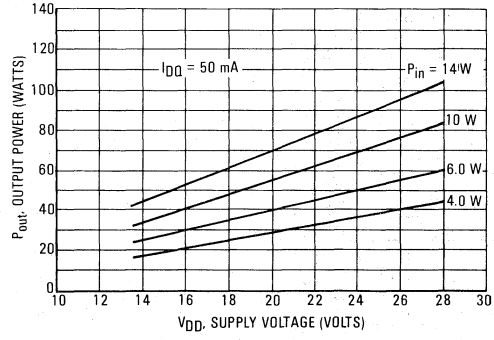


FIGURE 7 — POWER GAIN versus FREQUENCY

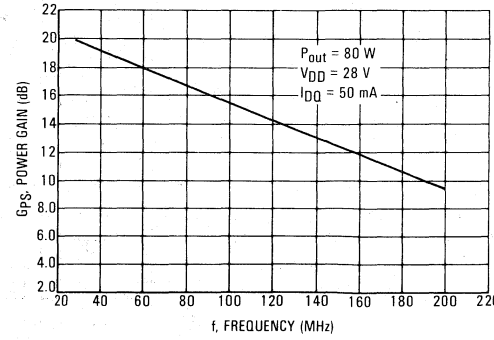


FIGURE 8 — OUTPUT POWER versus GATE VOLTAGE

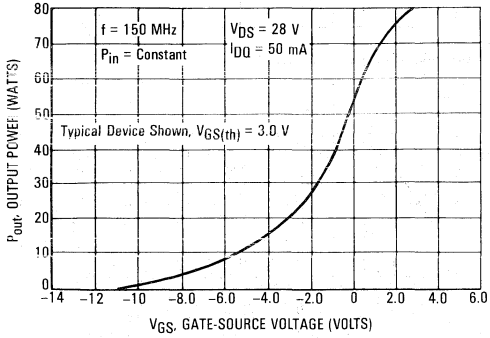


FIGURE 9 — DRAIN CURRENT versus GATE VOLTAGE (TRANSFER CHARACTERISTICS)

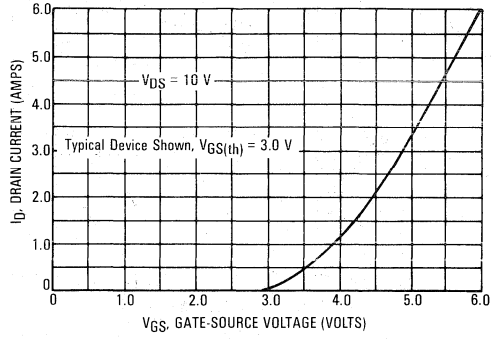


FIGURE 10 — GATE-SOURCE VOLTAGE versus CASE TEMPERATURE

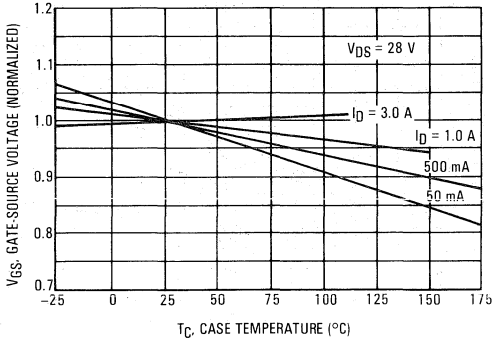


FIGURE 11 — CAPACITANCE versus DRAIN VOLTAGE

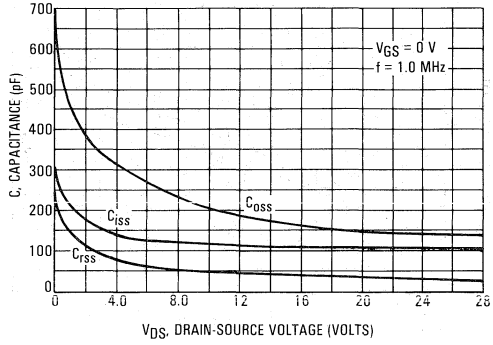


FIGURE 12 — DC SAFE OPERATING AREA

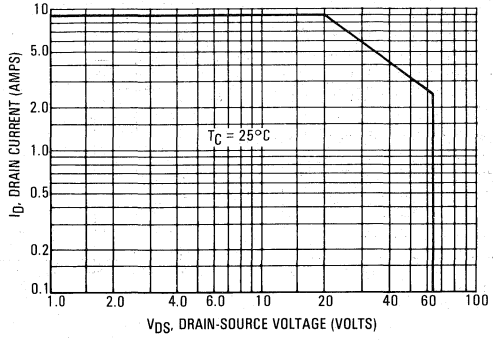


FIGURE 13 — COMMON SOURCE SCATTERING PARAMETERS
V_{DS} = 28 V, I_D = 2.0 A

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
2.0	0.928	-112	87.5	122	0.013	34	0.776	-128
5.0	0.902	-149	40.5	104	0.015	17	0.857	-158
10	0.897	-164	20.7	96	0.016	12	0.872	-169
20	0.896	-172	10.4	90	0.016	13	0.876	-174
30	0.896	-175	6.94	88	0.016	17	0.877	-176
40	0.896	-176	5.20	85	0.017	21	0.878	-177
50	0.897	-177	4.15	83	0.017	25	0.879	-177
60	0.897	-177	3.45	82	0.017	29	0.880	-177
70	0.898	-178	2.95	80	0.018	33	0.881	-177
80	0.899	-178	2.57	78	0.019	37	0.882	-177
90	0.901	-178	2.27	76	0.020	40	0.883	-177
100	0.903	-178	2.00	74	0.021	42	0.885	-177
110	0.905	-178	1.80	73	0.022	44	0.887	-177
120	0.907	-178	1.62	71	0.024	45	0.888	-177
130	0.908	-178	1.51	70	0.026	47	0.895	-177
140	0.909	-178	1.39	70	0.027	49	0.895	-177
150	0.910	-178	1.30	69	0.028	51	0.895	-177
160	0.911	-178	1.22	68	0.029	51	0.897	-177
170	0.912	-179	1.14	66	0.030	52	0.899	-177
180	0.921	-179	1.08	65	0.032	54	0.900	-177
190	0.921	-179	1.01	64	0.033	55	0.903	-177
200	0.922	-179	0.974	63	0.035	56	0.905	-177
210	0.920	-179	0.928	61	0.036	58	0.907	-176
220	0.915	-179	0.872	60	0.038	59	0.907	-176
230	0.915	-179	0.828	60	0.040	60	0.914	-176
240	0.917	-179	0.793	59	0.042	61	0.917	-176
250	0.922	-179	0.772	59	0.044	62	0.918	-176
260	0.927	+179	0.744	57	0.046	62	0.920	-176
270	0.928	+179	0.714	57	0.048	63	0.920	-176
280	0.929	+179	0.689	56	0.049	64	0.923	-176
290	0.929	+179	0.662	55	0.051	65	0.923	-176
300	0.938	+179	0.642	55	0.053	65	0.923	-176

FIGURE 14 — S_{11}, INPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 2.0 A

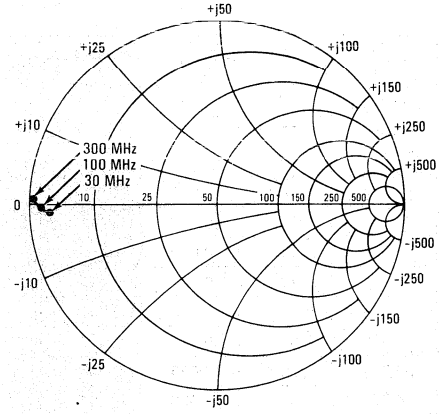


FIGURE 15 — S_{12}, REVERSE TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 2.0 A

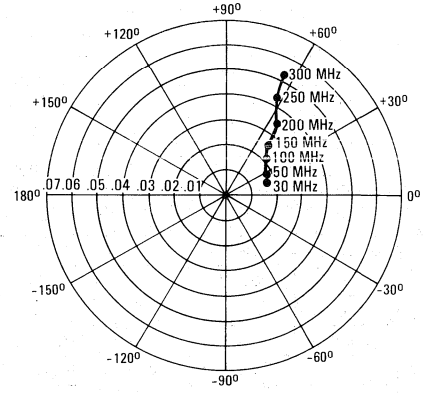


FIGURE 16 — S_{21}, FORWARD TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 2.0 A

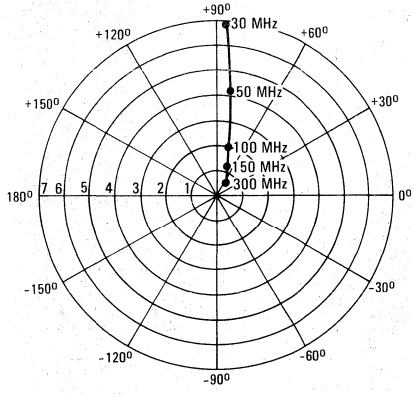
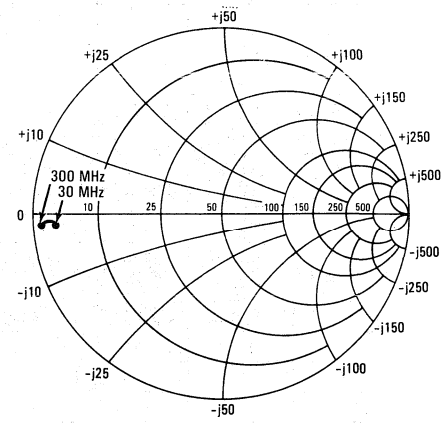


FIGURE 17 — S_{22}, OUTPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 2.0 A



DESIGN CONSIDERATIONS

The MRF172 is a TMOS RF power N-channel enhancement mode field-effect transistor (FET) designed for VHF power amplifier applications. Motorola TMOS FETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V-groove MOS power FETs.

Motorola Application Note AN-211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of TMOS RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF172 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 9 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF172 was characterized at I_{DQ} = 50 mA, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF172 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC, and modulation systems. (See Figure 8.)

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar VHF transistors are suitable for MRF172. See Motorola Application Note AN-721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of TMOS FETs helps ease the task of broadband network design. Both small-signal scattering parameters and large-signal impedances are provided. While the s-parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of TMOS power FETs.

FIGURE 18 — 150 MHz TEST CIRCUIT

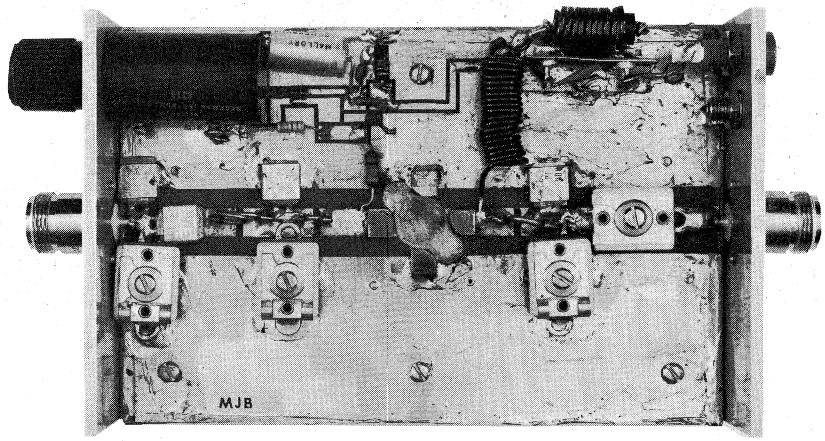
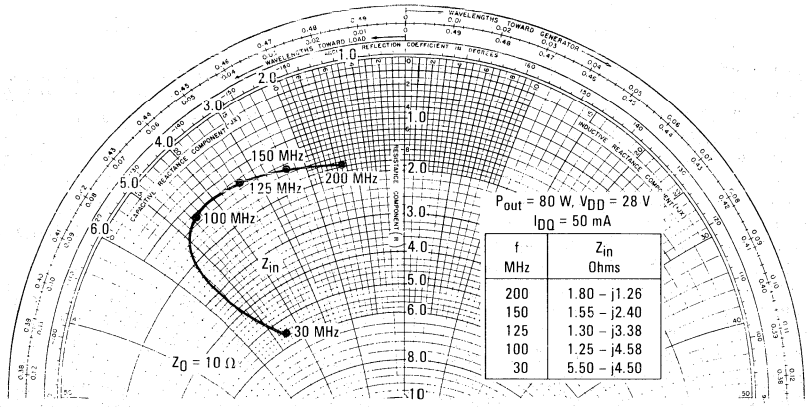
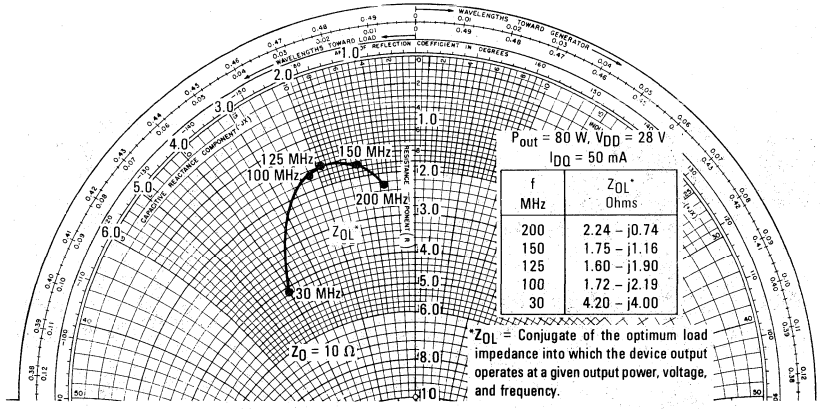


FIGURE 19 — SERIES EQUIVALENT INPUT IMPEDANCE, Z_{in}



f MHz	Z_{in} Ohms
200	1.80 – j1.26
150	1.55 – j2.40
125	1.30 – j3.38
100	1.25 – j4.58
30	5.50 – j4.50

FIGURE 20 — SERIES EQUIVALENT OUTPUT IMPEDANCE, Z_{OL}^*



f MHz	Z_{OL}^* Ohms
200	2.24 – j0.74
150	1.75 – j1.16
125	1.60 – j1.90
100	1.72 – j2.19
30	4.20 – j4.00

*Z_{OL}^* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

MRF174

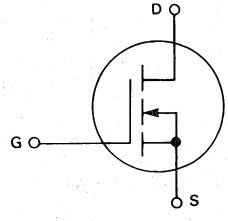
The RF TMOS Line

N-CHANNEL ENHANCEMENT-MODE
TMOS RF POWER FIELD-EFFECT TRANSISTOR

. . . designed primarily for wideband large-signal output and driver stages in the 2.0–200 MHz frequency range.

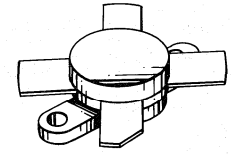
- Guaranteed Performance at 150 MHz, 28 Vdc
  - Output Power = 125 Watts
  - Minimum Gain = 9.0 dB
  - Efficiency = 50% (Min)
- Excellent Thermal Stability, Ideally Suited for Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR
- Low Noise Figure — 3.0 dB Typ at 2.0 A, 150 MHz

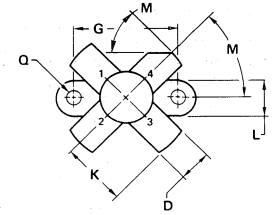
TMOS™

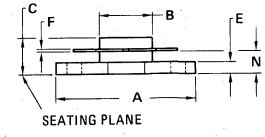


125 W 2.0–200 MHz

N-CHANNEL TMOS
BROADBAND RF POWER
FET







STYLE 2:
PIN 1. SOURCE
2. GATE
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	11.81	12.95	0.465	0.510
C	5.82	6.98	0.229	0.275
D	5.46	5.97	0.216	0.235
E	2.13	2.79	0.084	0.110
F	0.08	0.18	0.003	0.007
G	18.29	18.54	0.720	0.730
K	11.05	–	0.435	–
L	6.22	6.48	0.246	0.255
M	45° NOM		45° NOM	
N	3.66	4.52	0.144	0.178
Q	2.92	3.30	0.115	0.130

CASE 211-11

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain — Source Voltage	V_{DSS}	65	Vdc
Drain — Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate — Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	13	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	270 1.54	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

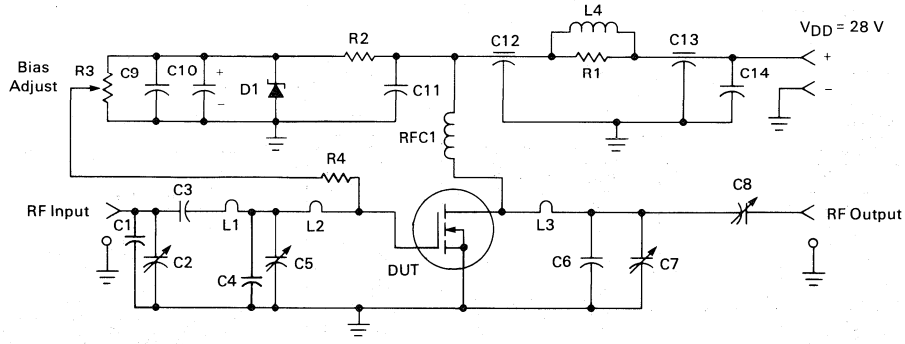
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.65	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 50 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	10	mAdc
Gate-Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 3.0 A)	g_{fs}	1.75	2.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	175	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	230	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	40	—	pF
FUNCTIONAL CHARACTERISTICS (Figure 1)					
Noise Figure (V_{DD} = 28 Vdc, I_D = 2.0 A, f = 150 MHz)	NF	—	3.0	—	dB
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 125 W, f = 150 MHz, I_{DQ} = 100 mA)	G_{ps}	9.0	11.8	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 125 W, f = 150 MHz, I_{DQ} = 100 mA)	η	50	60	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 125 W, f = 150 MHz, I_{DQ} = 100 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			

FIGURE 1 — 150 MHz TEST CIRCUIT



C1 — 35 pF Unleco
C2, C5 — Arco 462, 5–80 pF
C3 — 100 pF Unleco
C4 — 25 pF Unleco
C6 — 40 pF Unleco
C7 — Arco 461, 2.7–30 pF
C8 — Arco 463, 9–180 pF
C9, C11, C14 — 0.1 μF Erie Redcap
C10 — 50 μF, 50 V
C12, C13 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener

L1 — #16 AWG, 1-1/4 Turns, 0.213″ ID
L2 — #16 AWG, Hairpin 0.25″
L3 — #14 AWG, Hairpin 0.062″ wide, 0.47″ / 0.2″
L4 — 10 Turns #16 AWG Enameled Wire on R1
RFC1 — 18 Turns #16 AWG Enameled Wire, 0.3″ ID
R1 — 10 Ω, 2.0 W
R2 — 1.8 kΩ, 1/2 W
R3 — 10 kΩ, 10 Turn Bourns
R4 — 10 kΩ, 1/4 W

FIGURE 2 — OUTPUT POWER versus INPUT POWER

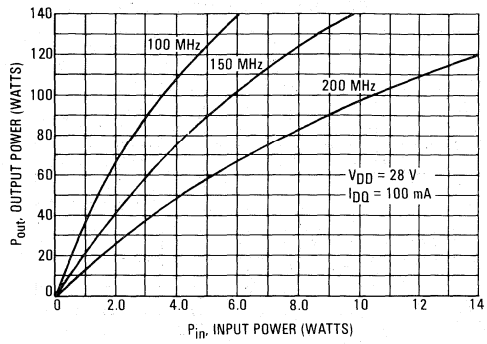


FIGURE 3 — OUTPUT POWER versus INPUT POWER

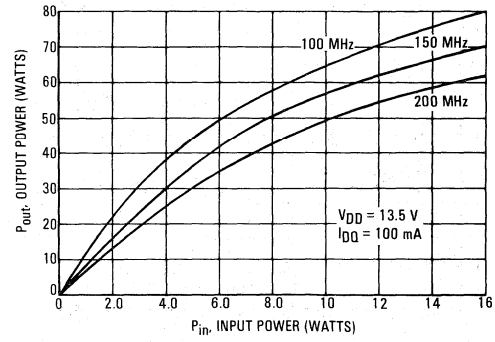


FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 100 MHz

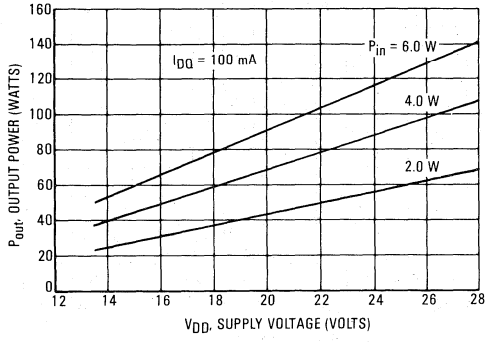


FIGURE 5 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 150 MHz

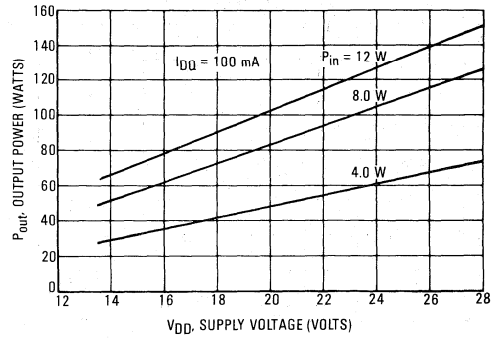


FIGURE 6 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 200 MHz

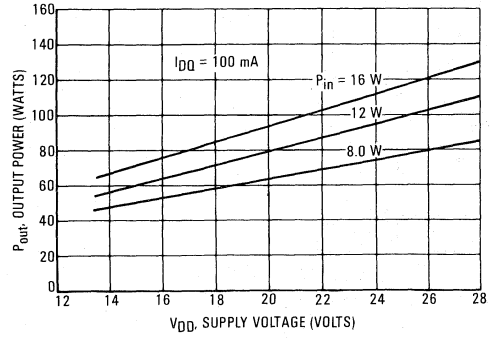
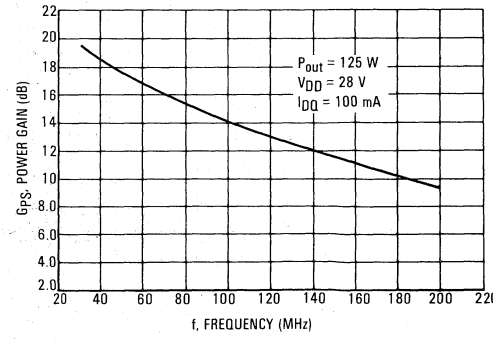


FIGURE 7 — POWER GAIN versus FREQUENCY



3

FIGURE 8 — OUTPUT POWER versus GATE VOLTAGE

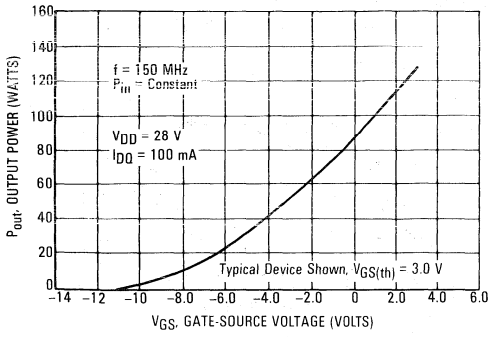


FIGURE 9 — DRAIN CURRENT versus GATE VOLTAGE (TRANSFER CHARACTERISTICS)

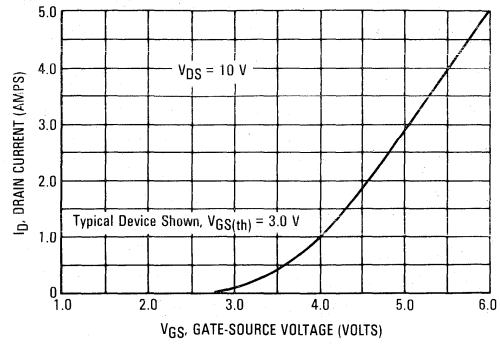


FIGURE 10 — GATE-SOURCE VOLTAGE versus CASE TEMPERATURE

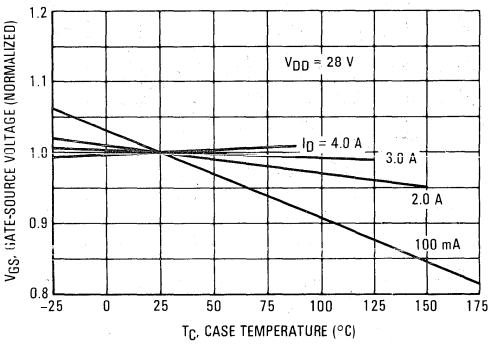


FIGURE 11 — CAPACITANCE versus DRAIN VOLTAGE

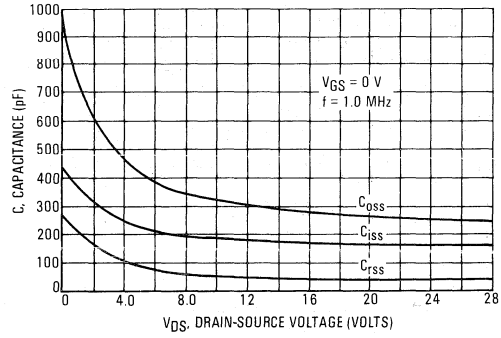


FIGURE 12 — DC SAFE OPERATING AREA

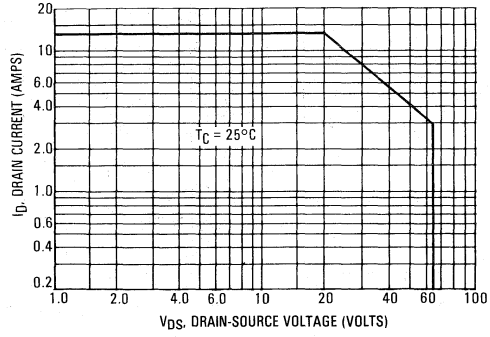


FIGURE 13 — COMMON SOURCE SCATTERING PARAMETERS
V_{DS} = 28 V, I_D = 3.0 A

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
2.0	0.932	-133	74.0	112	0.011	23	0.835	-151
5.0	0.923	-160	31.6	98	0.011	12	0.886	-168
10	0.921	-170	16.0	93	0.011	10	0.896	-174
20	0.921	-175	8.00	88	0.011	12	0.899	-177
30	0.921	-177	5.32	86	0.011	16	0.900	-178
40	0.921	-177	3.98	83	0.012	21	0.901	-178
50	0.922	-178	3.17	81	0.012	26	0.902	-178
60	0.923	-178	2.63	79	0.012	30	0.903	-178
70	0.924	-178	2.24	77	0.013	34	0.904	-178
80	0.925	-178	1.95	75	0.013	39	0.906	-178
90	0.927	-178	1.72	73	0.014	43	0.907	-178
100	0.930	-178	1.50	71	0.016	45	0.910	-178
110	0.930	-178	1.31	70	0.018	46	0.912	-178
120	0.931	-178	1.19	68	0.019	47	0.914	-178
130	0.942	-178	1.10	67	0.019	49	0.919	-178
140	0.936	-178	1.01	66	0.021	50	0.921	-178
150	0.938	-178	0.936	65	0.021	53	0.922	-178
160	0.938	-178	0.879	64	0.022	53	0.923	-178
170	0.940	-178	0.830	63	0.023	54	0.923	-177
180	0.942	-178	0.780	61	0.024	56	0.924	-177
190	0.942	-178	0.737	60	0.026	59	0.928	-177
200	0.952	-178	0.705	59	0.027	58	0.929	-177
210	0.950	-178	0.668	57	0.029	61	0.934	-177
220	0.942	-178	0.626	56	0.030	61	0.933	-177
230	0.943	-178	0.592	56	0.032	62	0.939	-177
240	0.946	-177	0.566	55	0.033	64	0.941	-177
250	0.952	-177	0.545	54	0.035	64	0.943	-177
260	0.958	-177	0.523	53	0.036	65	0.946	-177
270	0.956	-177	0.500	52	0.038	67	0.943	-177
280	0.960	-177	0.481	52	0.039	68	0.946	-177
290	0.956	-178	0.460	51	0.042	68	0.944	-177
300	0.955	-178	0.443	50	0.043	68	0.947	-177

FIGURE 14 — S_{11}, INPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 3.0 A

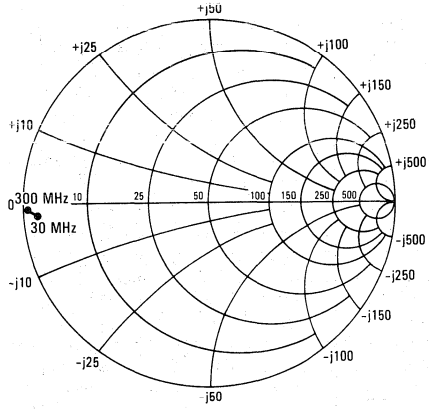


FIGURE 15 — S_{12}, REVERSE TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 3.0 A

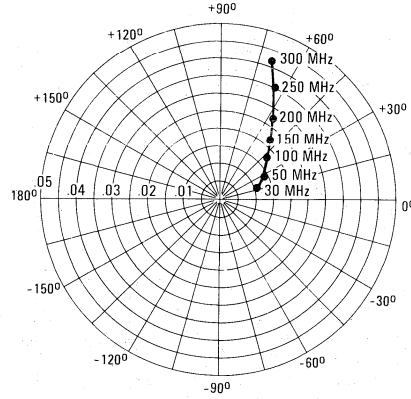


FIGURE 16 — S_{21}, FORWARD TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 3.0 A

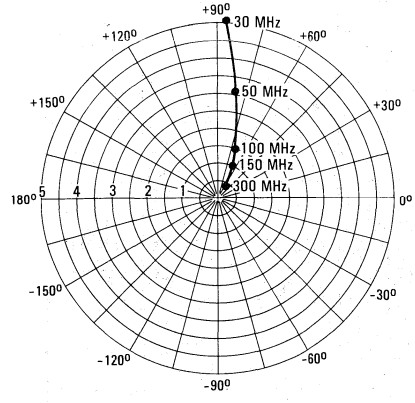
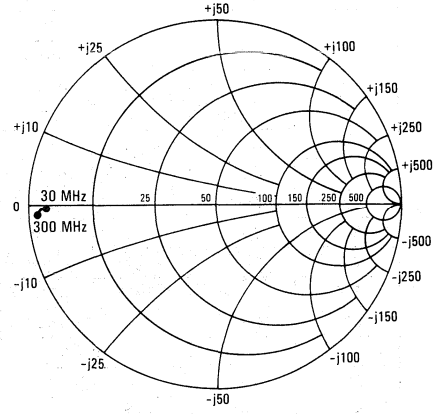


FIGURE 17 — S_{22}, OUTPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 3.0 A



DESIGN CONSIDERATIONS

The MRF174 is a TMOS RF power N-channel enhancement mode field-effect transistor (FET) designed for VHF power amplifier applications. Motorola TMOS FETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V-groove MOS power FETs.

Motorola Application Note AN-211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of TMOS RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF174 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 9 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF174 was characterized at I_{DQ} = 100 mA, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF174 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC, and modulation systems. (See Figure 8.)

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar VHF transistors are suitable for MRF174. See Motorola Application Note AN-721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of TMOS FETs helps ease the task of broadband network design. Both small-signal scattering parameters and large-signal impedances are provided. While the s-parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of TMOS power FETs.

FIGURE 18 — 150 MHz TEST CIRCUIT

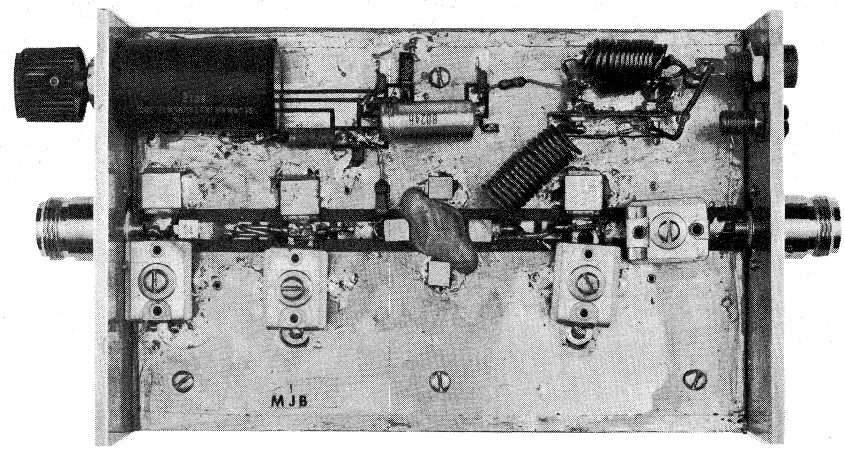
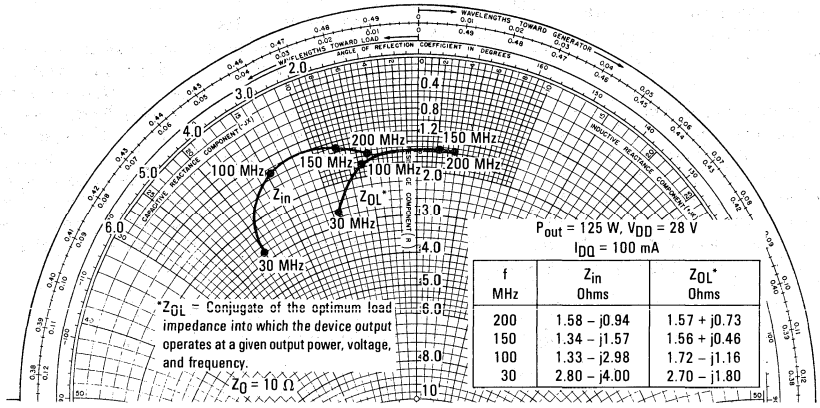


FIGURE 19 — SERIES EQUIVALENT INPUT AND OUTPUT IMPEDANCE, Z_{in}, Z_{OL}*



P_{out} = 125 W, V_{DD} = 28 V
I_{DQ} = 100 mA

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
200	1.58 – j0.94	1.57 + j0.73
150	1.34 – j1.57	1.56 + j0.46
100	1.33 – j2.98	1.72 – j1.16
30	2.80 – j4.00	2.70 – j1.80

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MRF226

The RF Line

13 W – 225 MHz

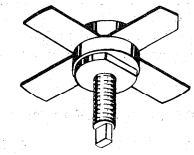
RF POWER TRANSISTOR

NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed for 12.5 Volt large-signal power amplifier applications in communication equipment operating at 225 MHz.

- Specified 12.5 Volt, 225 MHz Characteristics —
  Output Power = 13 Watts
  Minimum Gain = 9.0 dB
  Efficiency = 50%
- Characterized With Series Equivalent Large-Signal Impedance Parameters
- Designed to Withstand Load Mismatch at all Phase Angles with 20:1 VSWR



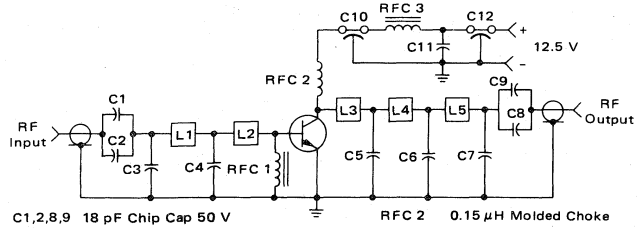
3

MAXIMUM RATINGS

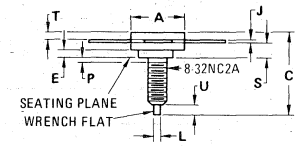
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	2.5	Adc
Total Device Dissipation @ $T_C = 25^oC$(1) Derate above 25^oC	P_D	45 257	Watts mW/^oC
Storage Temperature Range	T_{stg}	−65 to +150	^oC
Stud Torque (2)	—	6.5	In. Lb.

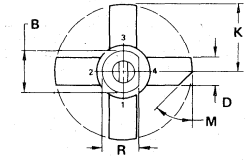
(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as Class C RF amplifiers.
(2) For repeated assembly, use 5 In. Lb.

FIGURE 1 – 225 MHz TEST CIRCUIT SCHEMATIC



C1,2,8,9	18 pF Chip Cap 50 V	RFC 2	0.15 μH Molded Choke
C3	15 pF UNELCO	L1	0.15 x 3.15 inch Microstrip
C4,5	80 pF UNELCO	L2	0.15 x 0.55 inch Microstrip
C6	25 pF UNELCO	L3	0.15 x 1.4 inch Microstrip
C7	7.0 pF UNELCO	L4	0.15 x 2.35 inch Microstrip
C10,12	680 pF Feedthru ALLEN BRADLEY	L5	0.15 x 0.5 inch Microstrip
C11	1.0 μF, 35 V Tantalum	Board is G10 3 x 5 x 0.062 inch	
RFC 1,3	Ferroxcube VK200	$\epsilon_R = 5$	





STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	17.02	20.07	0.670	0.790
D	5.46	5.97	0.215	0.235
E	1.78	–	0.070	–
J	0.08	0.18	0.003	0.007
K	12.45	–	0.490	–
L	1.40	1.78	0.055	0.070
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.11	2.54	0.083	0.100
U	2.49	3.35	0.098	0.132

NOTE.
CASE 145-09 USE 8-32NC2A STUD

CASE 145A-09

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector Emitter Breakdown Voltage (I_C = 15 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	–	Vdc
Collector-Base Breakdown Voltage (I_C = 5.0 mAdc, I_E = 0)	$V_{(BR)CBO}$	36	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 2.5 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	0.25	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0	–	–
FUNCTIONAL TEST (Figure 1)				
Common-Emitter Amplifier Power Gain (P_{out} = 13 W, V_{CC} = 12.5 Vdc, f = 225 MHz)	G_{PE}	9.0	–	dB
Collector Efficiency (P_{out} = 13 W, V_{CC} = 12.5 Vdc, f = 225 MHz)	η	50	–	%

FIGURE 2 – OUTPUT POWER versus INPUT POWER

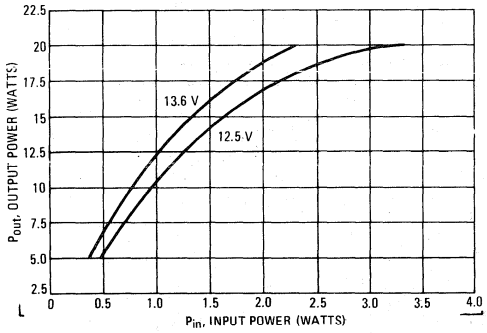
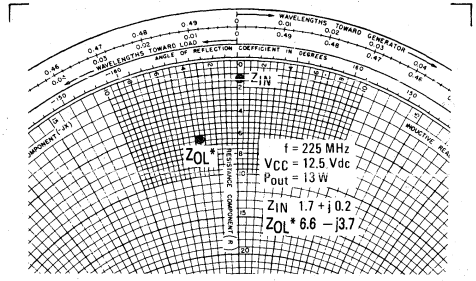


FIGURE 3 – SERIES EQUIVALENT IMPEDANCE



*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

MRF227

The RF Line

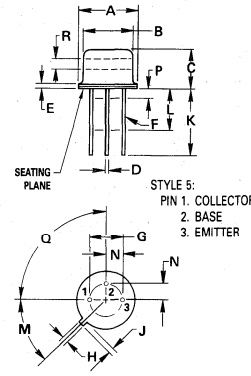
3 W – 225 MHz
RF POWER
TRANSISTOR
NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed for 12.5 Volt large-signal power amplifier applications in communication equipment operating at 225 MHz. Ideally suited for Class E citizens band radio.

- Specified 12.5 Volt, 225 MHz Characteristics –
  Output Power = 3.0 Watts
  Minimum Gain = 13.5 dB
  Efficiency = 60%
- Characterized With Series Equivalent Large-Signal Impedance Parameters
- Grounded Emitter TO-39 Package for High Gain and Excellent Heat Dissipation
- Replaces Medium Power Stud Mount Devices





DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	9.02	9.30	0.355	0.366
B	8.00	8.51	0.315	0.335
C	4.19	4.57	0.165	0.180
D	0.43	0.53	0.017	0.021
E	0.43	0.89	0.017	0.035
F	0.41	0.48	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.71	0.86	0.028	0.034
J	0.74	1.02	0.029	0.040
K	12.70	—	0.500	—
M	45°NOM		45°NOM	
N	2.54 TYP		0.100 TYP	
Q	90° NOM		90° NOM	

NOTE: The pin configuration on this version of the TO-39 package differs from the common isolated emitter type.

All JEDEC dimensions and notes apply.

CASE 79-03

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Collector Current – Continuous	I_C	600	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	8.0 46	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 55°C)	I_{CES}	–	–	10	mAdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	20	–	200	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	–	15	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (P_{out} = 3.0 W, V_{CC} = 12.5 Vdc, f = 225 MHz)	G_{PE}	13.5	15	–	dB
Collector Efficiency (P_{out} = 3.0 W, V_{CC} = 12.5 Vdc, f = 225 MHz)	η	60	–	–	%

3

FIGURE 1 – 225 MHz TEST CIRCUIT

C1,C2,C3,C4	ARCO 420
C5	1000 pF, UNELCO
C6	0.047 pF, ERIE
C7	1.0 pF, TANTALUM
L1	#18 AWG, 1" Wire Length
L2	VK200-4 Ferroxcube
L3	1 Turn, #18 AWG, 1/4" ID x 2" Wire Length
L4	0.15 μH DELEVAN Molded Choke

Board – Glass Teflon, ϵ_R = 2.56, t = 0.062"
Input/Output Connectors – Type N

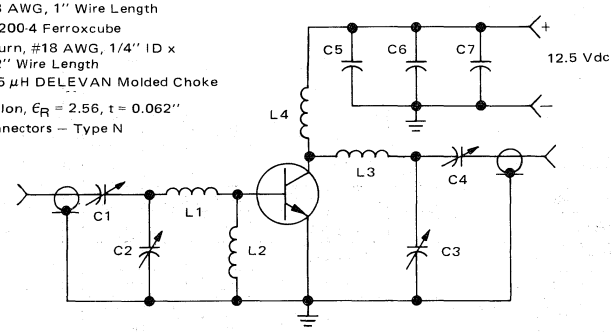


FIGURE 2 – INPUT POWER versus OUTPUT POWER – 12.5 V

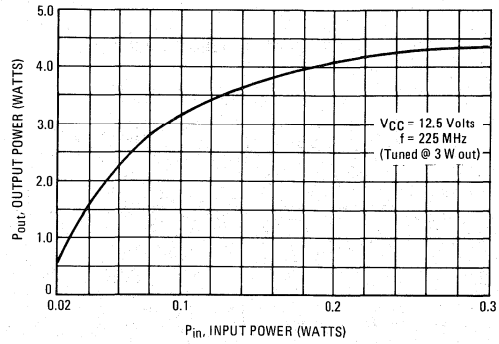


FIGURE 3 – INPUT POWER versus OUTPUT POWER – 13.6 V

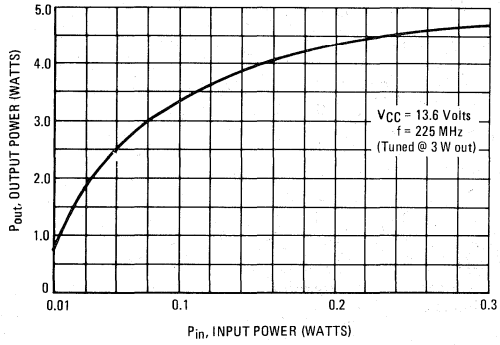


FIGURE 4 – INPUT POWER versus OUTPUT POWER – 7.5 V

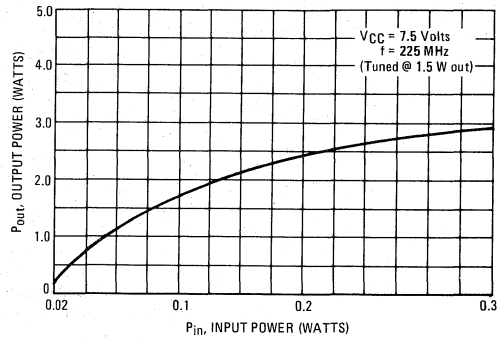


FIGURE 5 – OUTPUT POWER versus SUPPLY VOLTAGE

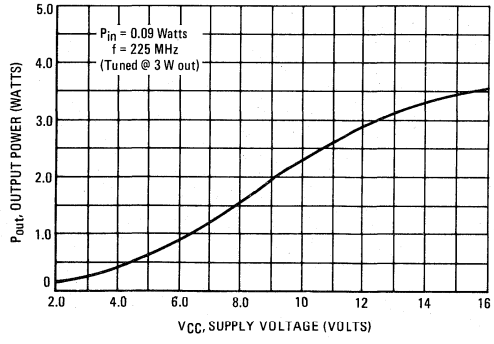
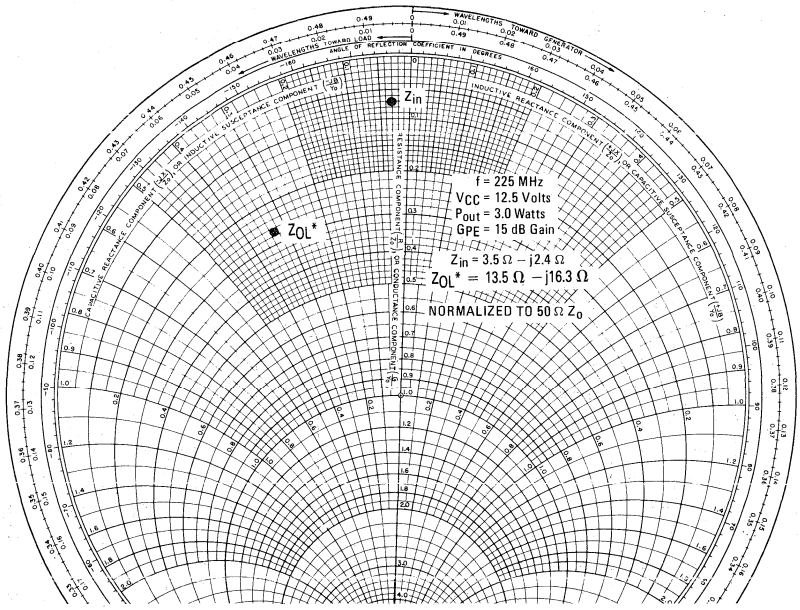


FIGURE 6 – SERIES EQUIVALENT IMPEDANCE



*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

MRF229

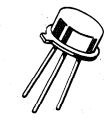
The RF Line

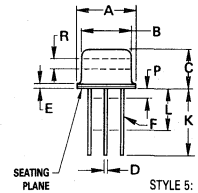
1.5 W — 90 MHz
RF POWER
TRANSISTOR
NPN SILICON

NPN SILICON RF POWER TRANSISTORS

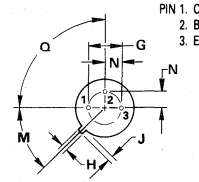
. . . designed for 12.5 Volt, mid-band large-signal amplifier applications in industrial and commercial FM equipment operating in the 40 to 100 MHz range.

- Specified 12.5 Volt, 90 MHz Characteristics —
  Output Power = 1.5 Watts
  Minimum Gain = 10 dB
  Efficiency = 55%
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Characterized with Parallel Equivalent Large-Signal Impedance Parameters
- MRF229 — Emitter Connected to Case





STYLE 5:
PIN 1. COLLECTOR
2. BASE
3. EMITTER



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	9.02	9.30	0.355	0.366
B	8.00	8.51	0.315	0.335
C	4.19	4.57	0.165	0.180
D	0.43	0.53	0.017	0.021
E	0.43	0.89	0.017	0.035
F	0.41	0.48	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.71	0.86	0.028	0.034
J	0.74	1.02	0.029	0.040
K	12.70	—	0.500	—
M	45°NOM		45°NOM	
N	2.54 TYP		0.100 TYP	
Q	90° NOM		90° NOM	

NOTE: The pin configuration on this version of the TO-39 package differs from the common isolated emitter type.

All JEDEC dimensions and notes apply.

CASE 79-03

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	0.5	Adc
Total Device Dissipation @ $T_C = 25^oC$ (1). Derate above 25^oC	P_D	5.0 28.6	Watts $mW/^oC$
Storage Temperature Range	T_{stg}	-65 to +200	^oC

THERMAL CHARACTERISTICS

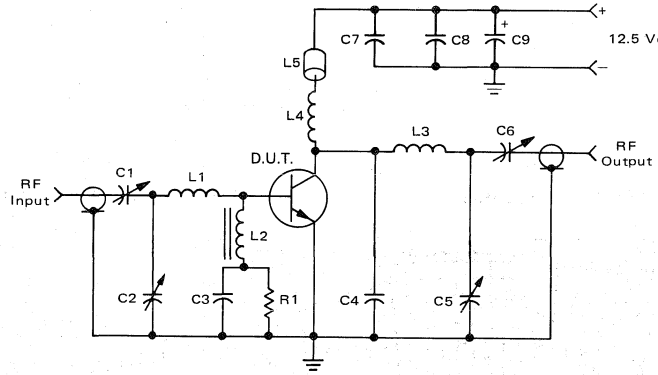
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R\theta JC$	35	$^oC/W$

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as Class C RF Amplifiers.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 25 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 25 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.25 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	0.5	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0	–	–
DYNAMIC CHARACTERISTICS				
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	25	pF
FUNCTIONAL TESTS (Figure 1)				
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 1.5 W, f = 90 MHz)	G_{PE}	10	–	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 1.5 W, f = 90 MHz)	η	55	–	%
Load Mismatch (V_{CC} = 12.5 Vdc, P_{out} = 1.5 W, f = 90 MHz, $T_C \leq 25°C$)	–	No Degradation in Output Power		

FIGURE 1 – 90 MHz TEST CIRCUIT SCHEMATIC



C1	5.0-80 pF, ARCO 462	C9	20 μF, 15 Vdc TANTALUM
C2,C6	25-280 pF, ARCO 464	L1	2 Turns, #18 AWG, 3/8" I.D. 3/8" Long
C3	250 pF UNELCO	L2	2.5 Turns, #20 AWG, on Ferrite Bead. FERROXCUBE 56-590-65-3B
C4	10 pF UNELCO	L3	3 Turns, #18 AWG, 3/8" I.D., 1/2" Long
C5	9.0-180 pF, ARCO 463	L4	0.68 μH, 9230-16 MILLER Molded Choke
C7	1000 pF UNELCO	L5	Ferrite Bead, FERROXCUBE 56-590-65-3B
C8	0.47 μF ERIE Disc Ceramic	R1	4.7 OHM, 1/2 W, 10% Carbon

Input/Output Connectors – Type BNC

FIGURE 2 – OUTPUT POWER versus INPUT POWER

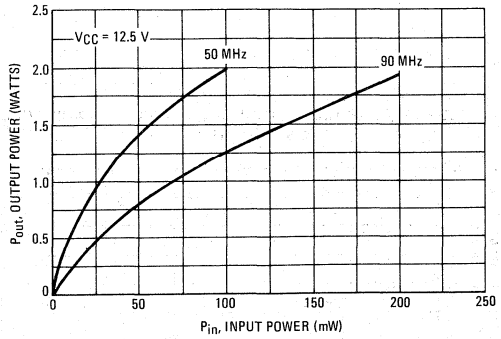


FIGURE 3 – OUTPUT POWER versus FREQUENCY

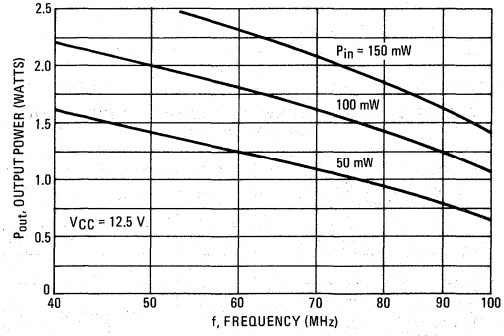


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

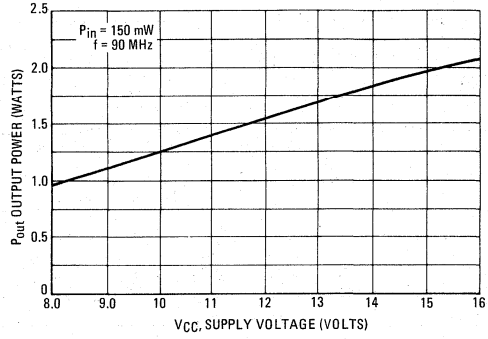
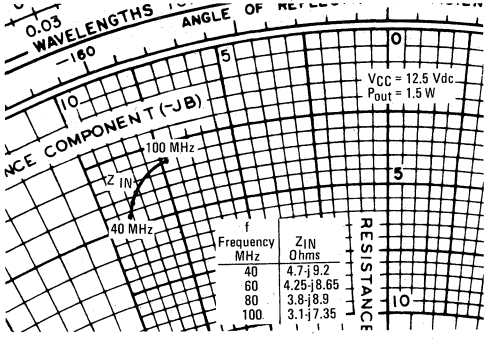
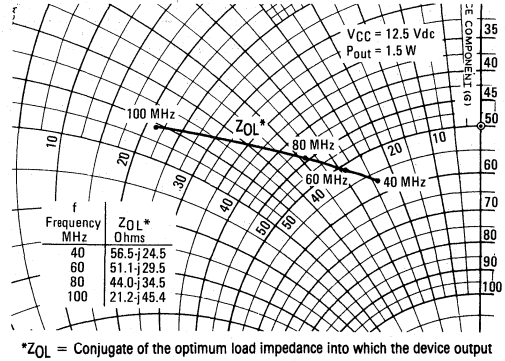


FIGURE 5

SERIES EQUIVALENT INPUT IMPEDANCE



SERIES EQUIVALENT OUTPUT IMPEDANCE



*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

FIGURE 6 – PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

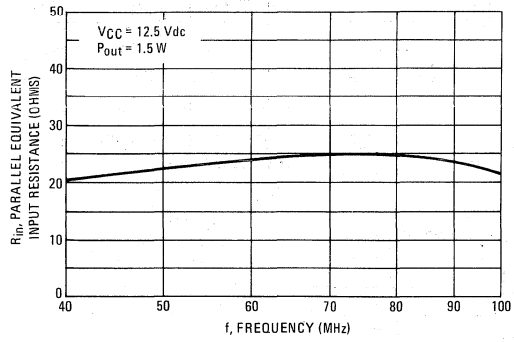


FIGURE 7 – PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

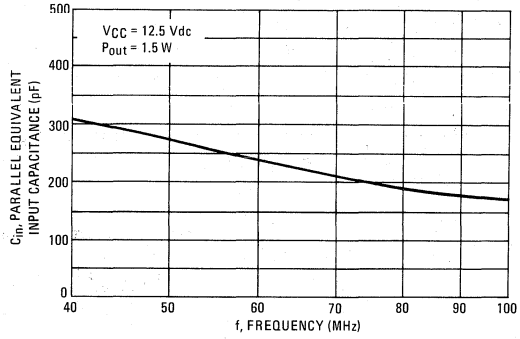


FIGURE 8 – PARALLEL EQUIVALENT OUTPUT RESISTANCE versus FREQUENCY

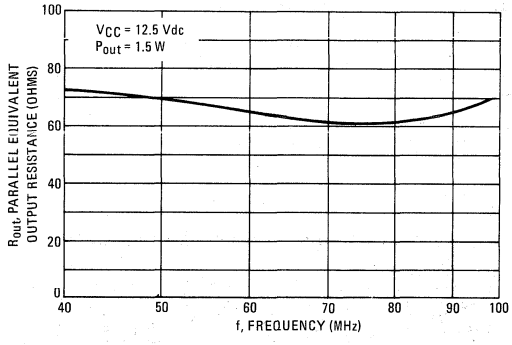
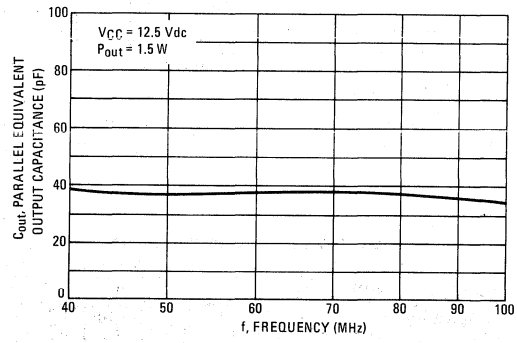


FIGURE 9 – PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY



MRF232

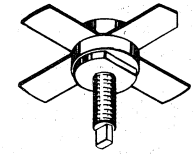
The RF Line

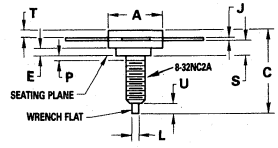
NPN SILICON RF POWER TRANSISTORS

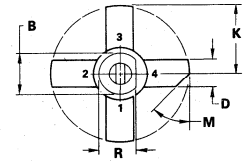
. . . designed for 12.5 Volt, mid-band large-signal amplifier applications in industrial and commercial FM equipment operating in the 40 to 100 MHz range.

- Specified 12.5 Volt, 90 MHz Characteristics –
  Output Power = 7.5 Watts
  Minimum Gain = 9.0 dB
  Efficiency = 55%
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Characterized with Parallel Equivalent Large-Signal Impedance Parameters

7.5 W – 90 MHz
RF POWER TRANSISTOR
NPN SILICON







STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	2.0	Adc
Total Device Dissipation @ $T_C = 25^oC$ (1) Derate above 25^oC	P_D	20 114	Watts $mW/^oC$
Storage Temperature Range	T_{stg}	−65 to +150	^oC
Stud Torque (2)	—	6.5	In. Lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.75	$^oC/W$

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as Class C RF Amplifiers.
(2) For repeated assembly use 5 In. Lb.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	17.02	20.07	0.670	0.790
D	5.46	5.97	0.215	0.235
E	1.78	—	0.070	—
J	0.08	0.18	0.003	0.007
K	12.45	—	0.490	—
L	1.40	1.78	0.055	0.070
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.11	2.54	0.083	0.100
U	2.49	3.35	0.098	0.132

CASE 145A-09

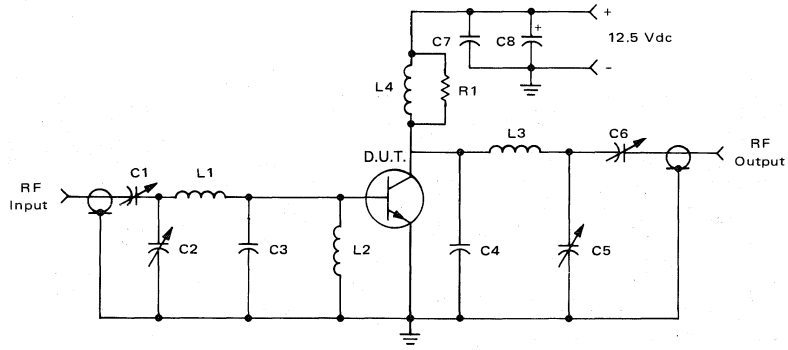
3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 2.5 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	1.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	–	–
DYNAMIC CHARACTERISTICS				
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	55	pF
FUNCTIONAL TESTS (Figure 1)				
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 7.5 W, f = 90 MHz)	G_{PE}	9.0	–	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 7.5 W, f = 90 MHz)	η	55	–	%
Load Mismatch (V_{CC} = 12.5 Vdc, P_{out} = 7.5 W, f = 90 MHz, $T_C \leq 25°C$)	–	No Degradation in Output Power		

3

FIGURE 1 – 90 MHz TEST CIRCUIT SCHEMATIC



C1,C6	5.0-80 pF, ARCO 462	L1	3 Turns, #18 AWG, 3/8" I.D., 3/8" Long
C2,C5	9.0-180 pF, ARCO 463	L2	FERROXCUBE VK200-20-4B Ferrite Choke
C3,C4	100 pF UNELCO	L3	3 Turns, #18 AWG, 5/16" I.D., 3/8" Long
C7	1000 pF UNELCO	L4	10 Turns, #22 AWG, on R1
C8	4.7 μF, 15 Vdc, TANTALUM	R1	340 Ohm, 1 W Carbon
		Input/Output Connectors – Type BNC	

FIGURE 2 – OUTPUT POWER versus INPUT POWER

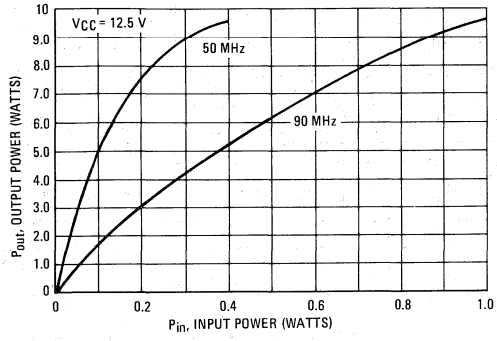


FIGURE 3 – OUTPUT POWER versus FREQUENCY

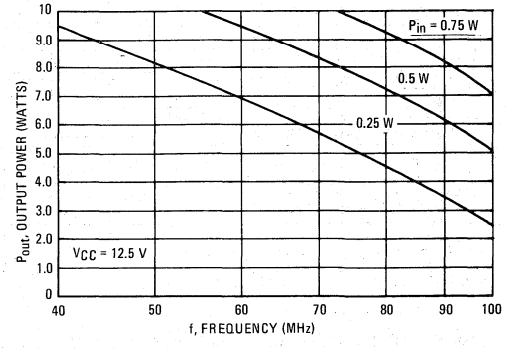


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

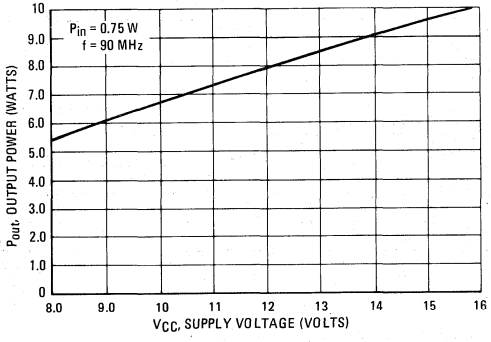
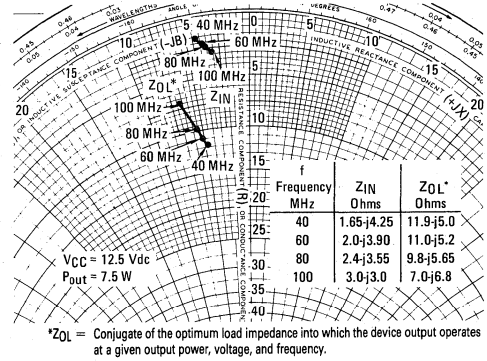


FIGURE 5 – SERIES EQUIVALENT IMPEDANCE



f Frequency MHz	Z_{IN} Ohms	Z_{OL}* Ohms
40	1.65-j4.25	11.9-j5.0
60	2.0-j3.90	11.0-j5.2
80	2.4-j3.55	9.8-j5.65
100	3.0-j3.0	7.0-j6.8

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

3

FIGURE 6 – PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

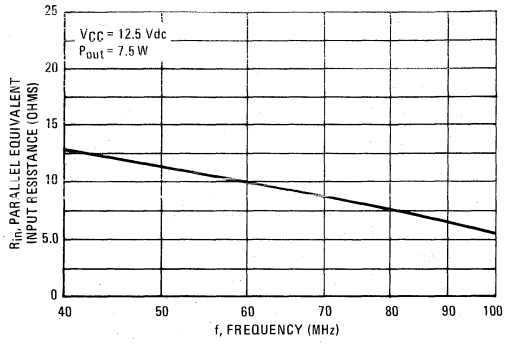


FIGURE 7 – PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

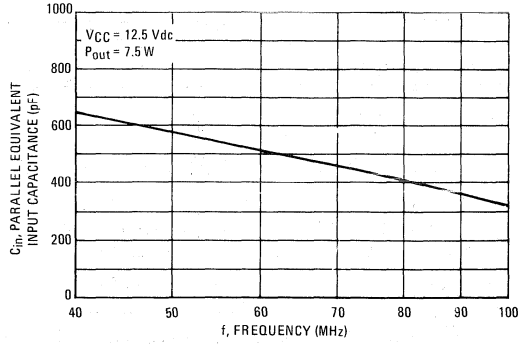


FIGURE 8 – PARALLEL EQUIVALENT OUTPUT RESISTANCE versus FREQUENCY

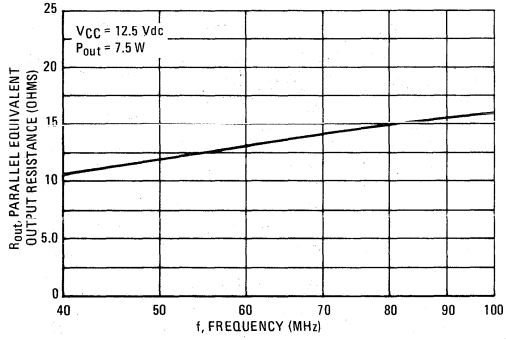
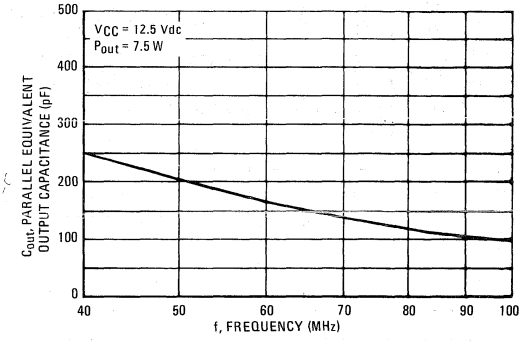


FIGURE 9 – PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY



MRF233

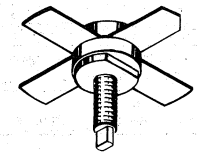
The RF Line

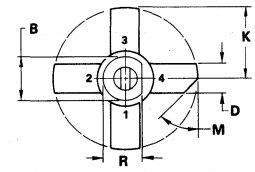
15 W – 90 MHz
RF POWER
TRANSISTOR
NPN SILICON

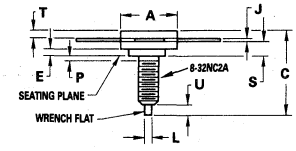
NPN SILICON RF POWER TRANSISTORS

. . . designed for 12.5 Volt, mid-band large-signal amplifier applications in industrial and commercial FM equipment operating in the 40 to 100 MHz range.

- Specified 12.5 Volt, 90 MHz Characteristics –
  Output Power = 15 Watts
  Minimum Gain = 10 dB
  Efficiency = 55%
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Characterized with Parallel Equivalent Large-Signal Impedance Parameters







STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	17.02	20.07	0.670	0.790
D	5.46	5.97	0.215	0.235
E	1.78	—	0.070	—
J	0.08	0.18	0.003	0.007
K	12.45	—	0.490	—
L	1.40	1.78	0.055	0.070
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.11	2.54	0.083	0.100
U	2.49	3.35	0.098	0.132

CASE 145A-09

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	3.5	Adc
Total Device Dissipation @ $T_C = 25^oC$ (1) Derate Above 25^oC	P_D —	50 285	Watts mW/^oC
Storage Temperature Range	T_{stg}	−65 to +150	^oC
Stud Torque (2)	—	6.5	In-lb

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.5	$^oC/W$

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as Class C RF amplifiers.
(2) For Repeated Assembly use 5 In. Lb.

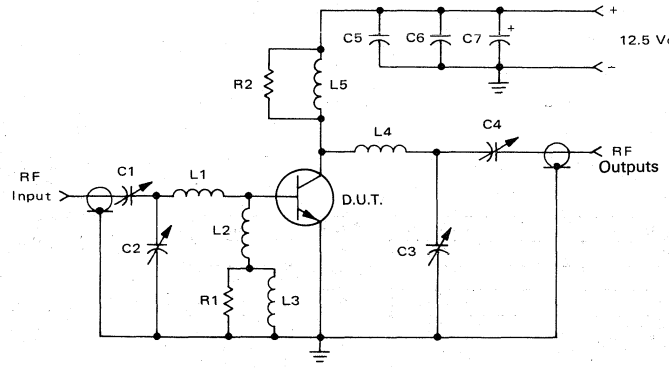
3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0	–	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	100	120	pF
FUNCTIONAL TESTS (Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 15 W, f = 90 MHz)	G_{PE}	10	–	–	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 15 W, f = 90 MHz)	η	55	–	–	%
Load Mismatch (V_{CC} = 12.5 Vdc, P_{out} = 15 W, f = 90 MHz, $T_C \leq 25°C$)	–	No Degradation in Output Power			

3

FIGURE 1 – 90 MHz TEST CIRCUIT SCHEMATIC



C1,C3 9.0-180 pF, ARCO 463
C2,C4 25-280 pF ARCO 464
C5 1000 pF UNELCO
C6 0.01 μF ERIE Disc Ceramic
C7 1.0 μF, 35 Vdc TANTALUM
L1 2 Turns, #18 AWG, 3/8" I.D., 1/4" Long
L2 0.22 μH, 9230-04 MILLER Molded Choke
L3 2.2 μH, 9230-200 MILLER Molded Choke
L4 2 Turns, #18 AWG, 3/8" I.D., 3/8" Long
L5 10 Turns, #16 AWG, Wound On R2.
R1 15 Ohm, 1/2 W, 10% Carbon
R2 68 Ohm, 1 Watt, 10% Carbon
Input/Output Connectors – Type BNC

FIGURE 2 – OUTPUT POWER versus INPUT POWER

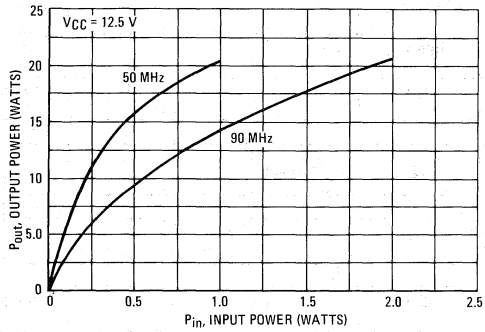


FIGURE 3 – OUTPUT POWER versus FREQUENCY

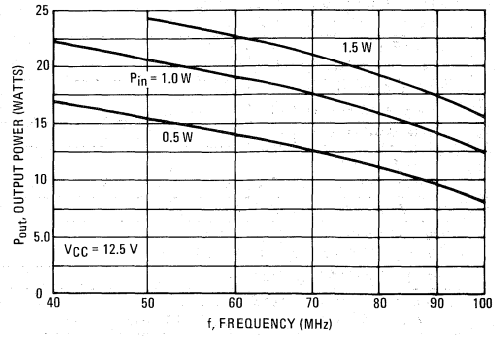


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

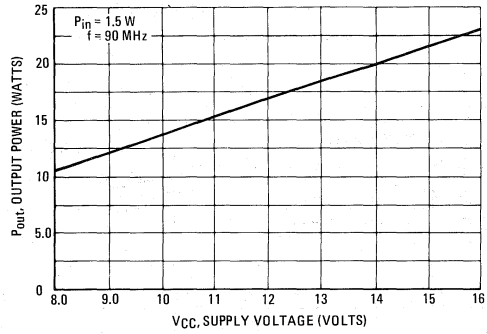
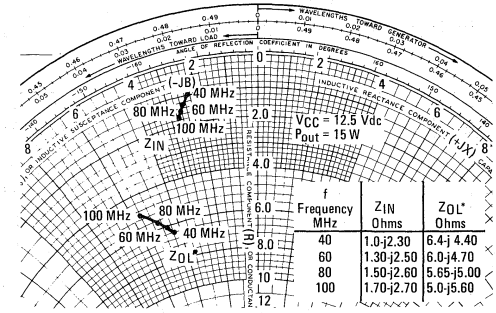


FIGURE 5 – SERIES EQUIVALENT IMPEDANCE



*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

FIGURE 6 – PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

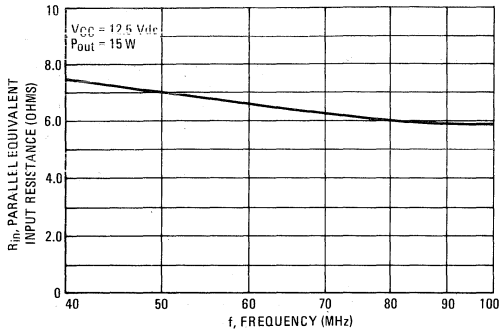


FIGURE 7 – PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

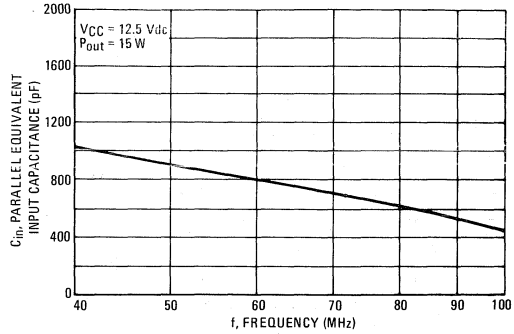


FIGURE 8 – PARALLEL EQUIVALENT OUTPUT RESISTANCE versus FREQUENCY

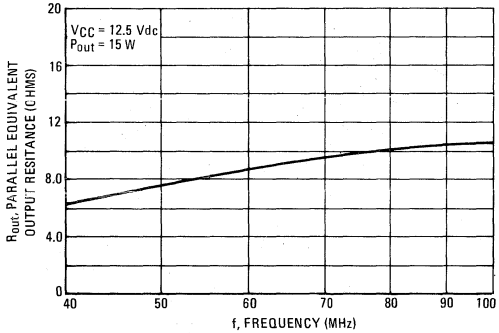
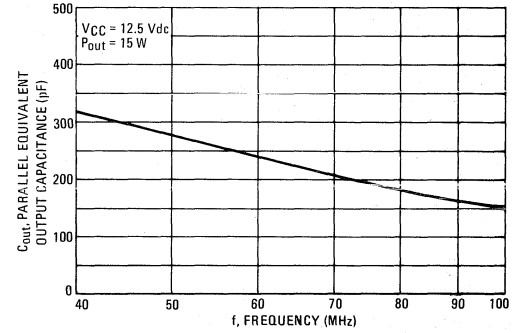


FIGURE 9 – PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY



MRF234

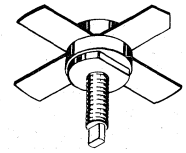
The RF Line

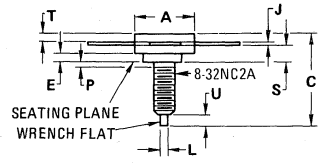
25 W – 90 MHz
RF POWER
TRANSISTOR
NPN SILICON

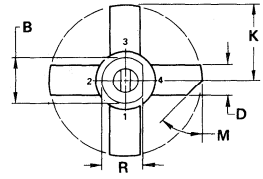
NPN SILICON RF POWER TRANSISTORS

. . . designed for 12.5 Volt, mid-band large-signal amplifier applications in industrial and commercial FM equipment operating in the 40 to 100 MHz range.

- Specified 12.5 Volt, 90 MHz Characteristics –
  Output Power = 25 Watts
  Minimum Gain = 9.5 dB
  Efficiency = 55%
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR.
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Characterized with Parallel Equivalent Large-Signal Impedance Parameters







STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	17.02	20.07	0.670	0.790
D	5.46	5.97	0.215	0.235
E	1.78	–	0.070	–
J	0.08	0.18	0.003	0.007
K	12.45	–	0.490	–
L	1.40	1.78	0.055	0.070
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.11	2.54	0.083	0.100
U	2.49	3.35	0.098	0.132

CASE 145A-09

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current – Continuous	I_C	4.0	Adc
Total Device Dissipation @ $T_C = 25^oC$ (1) Derate above 25^oC	P_D	70 400	Watts $mW/^oC$
Storage Temperature Range	T_{stg}	–65 to+150	^oC
Stud Torque (2)	–	6.5	In. Lb.

THERMAL CHARACTERISTICS

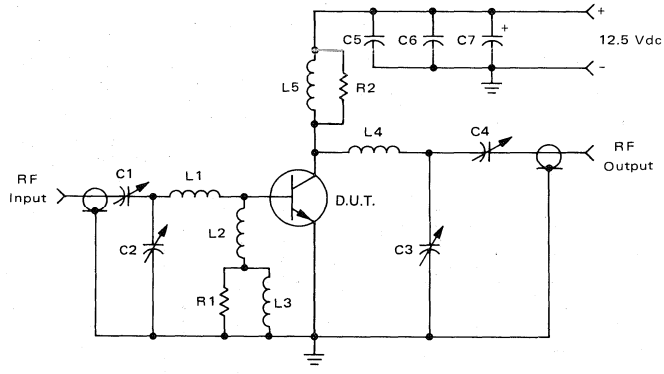
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	$^oC/W$

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as Class C RF Amplifiers.
(2) For repeated assembly use 5 In. Lb.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 200 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 200 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0	–		
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	100	120	pF
FUNCTIONAL TESTS (Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 25 W, f = 90 MHz)	G_{PE}	9.5	–	–	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 25 W, f = 90 MHz)	η	55	–	–	%
Load Mismatch (V_{CC} = 12.5 Vdc, P_{out} = 25 W, f = 90 MHz, $T_C \leq 25°C$	–	No Degradation in Output Power			

FIGURE 1 – 90 MHz TEST CIRCUIT SCHEMATIC



C1,C4	5.0-80 pF, ARCO 462
C2,C3	25-280 pF, ARCO 464
C5	1000 pF UNELCO
C6	0.047 µF, ERIE disc ceramic
C7	10 µF, 15 Vdc TANTALUM
L1	1 Turn, #16 AWG, 3/8" I.D., 1/8" Long
L2	0.22 µH, 9230-04 MILLER Molded Choke
L3	22 µH, 9230-52 MILLER Molded Choke
L4	2 Turns, #14 AWG, 3/8" I.D., 1/4" Long
L5	10 Turns, #18 AWG, 1/4" I.D., wound on R2
R1	15 Ohms, 1/2 W, 10%
R2	47 Ohm, 1 W Carbon
	Input/Output Connector – Type BNC

FIGURE 2 – OUTPUT POWER versus INPUT POWER

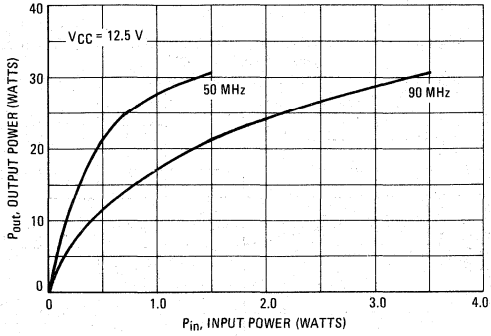


FIGURE 3 – OUTPUT POWER versus FREQUENCY

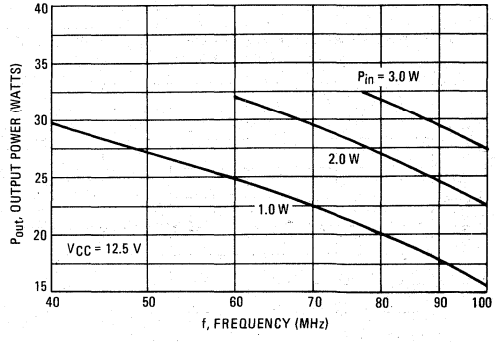


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

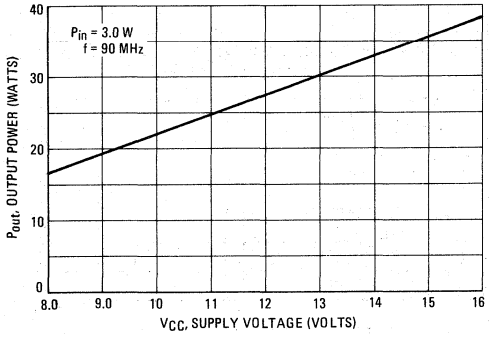
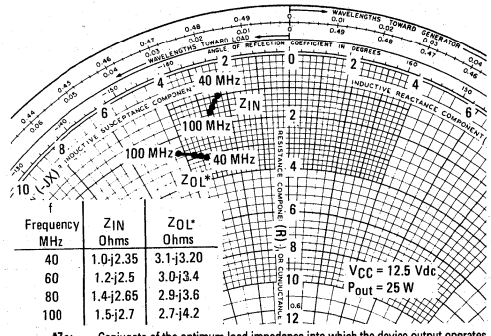


FIGURE 5 – SERIES EQUIVALENT IMPEDANCE



Frequency MHz	Z_{IN} Ohms	Z_{OL}* Ohms
40	1.0-j2.35	3.1-j3.20
60	1.2-j2.5	3.0-j3.4
80	1.4-j2.65	2.9-j3.6
100	1.5-j2.7	2.7-j4.2

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

3

FIGURE 6 – PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

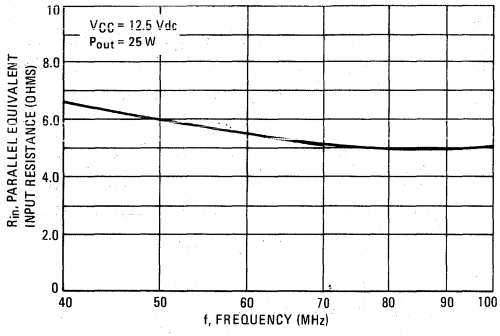


FIGURE 7 – PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

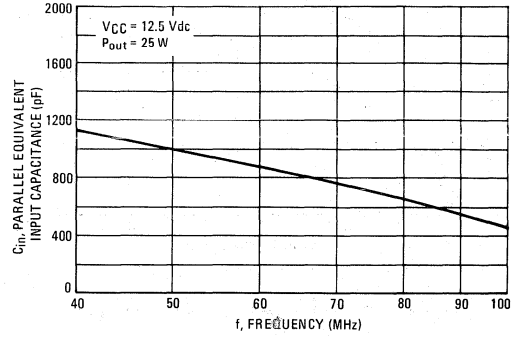


FIGURE 8 – PARALLEL EQUIVALENT OUTPUT RESISTANCE versus FREQUENCY

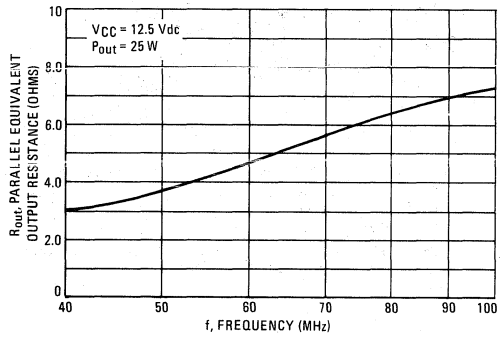
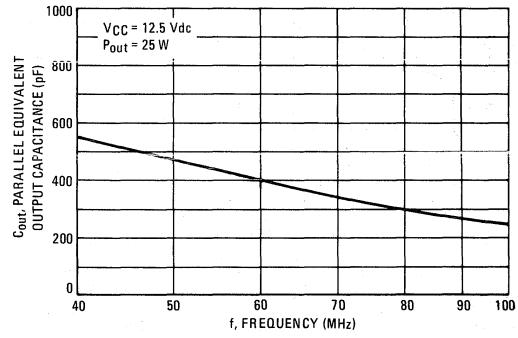


FIGURE 9 – PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY



MRF237

The RF Line

NPN SILICON RF POWER TRANSISTOR

. . . designed for 12.5 Volt large-signal power amplifier applications in communication equipment operating to 225 MHz.

- Specified 12.5 Volt, 175 MHz Characteristics —
  Output Power = 4.0 Watts
  Minimum Gain = 12 dB
  Efficiency = 50%
- Characterized With Series Equivalent Large-Signal Impedance Parameters
- Grounded Emitter TO-39 Package for High Gain and Excellent Heat Dissipation
- Replaces Medium Power Stud Mount Devices

4 W — 175 MHz
RF POWER TRANSISTOR
NPN SILICON



3

MAXIMUM RATINGS

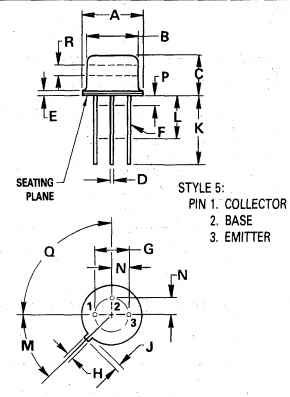
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	1.0	Adc
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	8.0 45.7	Watts mW/^oC
Storage Temperature Range	T_{stg}	−65 to +200	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	22	$^oC/W$

ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C =5.0 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	—	—	0.25	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0	—	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	—	15	20	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (P_{out} = 4.0 W, V_{CC} = 12.5 Vdc, f = 175 MHz)	G_{PE}	12	14	—	dB
Collector Efficiency (P_{out} = 4.0 W, V_{CC} = 12.5 Vdc, f = 175 MHz)	η	50	62	—	%

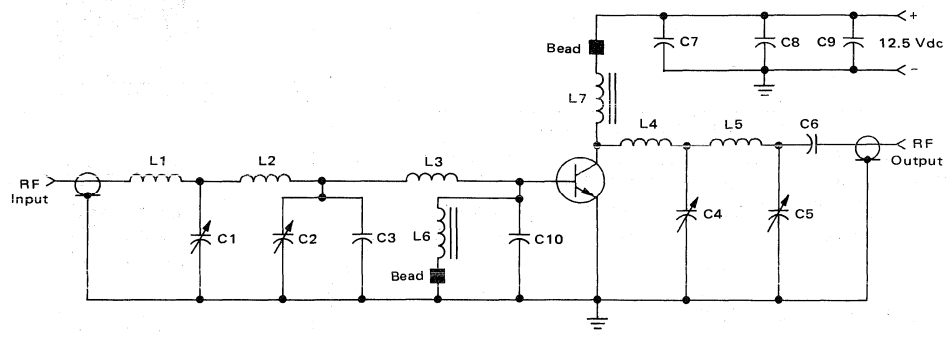


NOTE:
1. ALL RULES AND NOTES ASSOCIATED WITH TO-39 OUTLINE SHALL APPLY.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.02	9.30	0.355	0.366
B	8.00	8.51	0.315	0.335
C	4.19	.57	0.165	0.180
D	0.43	0.53	0.017	0.021
E	0.43	0.89	0.017	0.035
F	0.41	0.48	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.71	0.86	0.028	0.034
J	0.74	1.02	0.029	0.040
K	12.70	—	0.500	—
M	45°NOM		45°NOM	
N	2.54 TYP		0.100 TYP	
Q	90° NOM		90° NOM	

CASE 79-03

FIGURE 1 – 175 MHz TEST CIRCUIT SCHEMATIC



C1,C4,C5	3.0 - 180 pF, ARCO 463	L1	1/2 Turn, #16 AWG, 0.5" I.D.
C2	1.75 - 30 pF, ARCO 461	L2	1", #16 AWG
C3	40 pF, UNELCO	L3	0.75" #16 AWG
C6	0.01 μF, ERIE	L4,L5	1 Turn, #16 AWG, 0.5" I.D.
C7	0.1 μF, ERIE REDCAP	L6	0.15 μH Molded Choke
C8	1.0 μF, TANTALUM	L7	1.2 μH Molded Choke
C9	1000 pF, UNELCO	Beads	FERRITE Beads, FERROXCUBE
C10	100 pF UNELCO		#56-570-65/3B

FIGURE 2 – OUTPUT POWER versus INPUT POWER

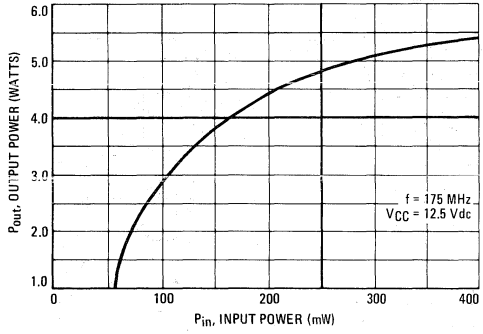


FIGURE 3 – OUTPUT POWER versus FREQUENCY

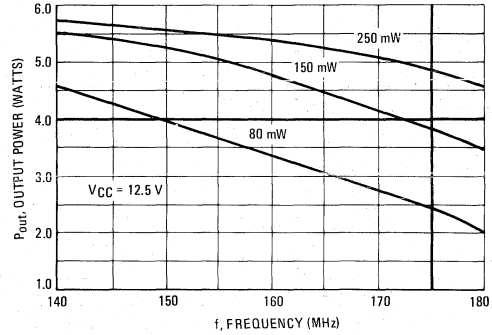


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

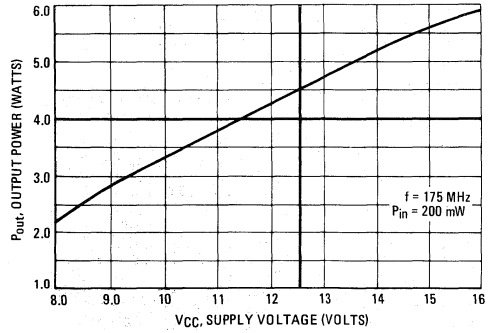
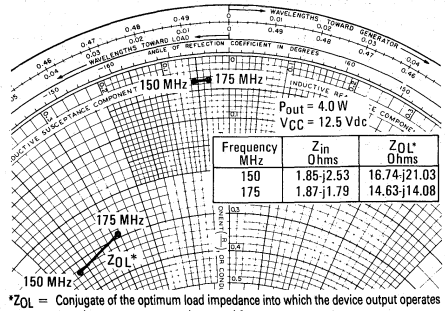


FIGURE 5 – SERIES EQUIVALENT IMPEDANCE



Frequency MHz	Z_{in} Ohms	Z_{OL}* Ohms
150	1.85-j2.53	16.74-j21.03
175	1.87-j1.79	14.63-j14.08

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

MRF240
MRF240A

The RF Line

NPN SILICON RF POWER TRANSISTOR

. . . designed for 13.6 volt VHF large-signal class C and class AB linear power amplifier applications in commercial and industrial equipment.

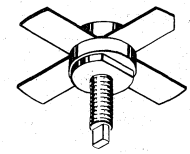
- High Common Emitter Power Gain
- Specified 13.6 V, 160 MHz Performance:
  Output Power = 40 Watts
  Power Gain = 9.0 dB Min
  Efficiency = 55% Min
- Load Mismatch Capability at Rated Voltage and RF Drive
- Silicon Nitride Passivated
- Low Intermodulation Distortion, d_3 = -30 dB Typ

See AN791 for description of a 35 W pep, 145 MHz linear amplifier.

40 W — 145–175 MHz

RF POWER TRANSISTOR

NPN SILICON



3

MAXIMUM RATINGS

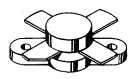
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	8.0	Adc
Total Device Dissipation @ T_C = 25°C (1)	P_D	100	Watts
Derate above 25°C		0.57	W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	1.75	°C/W

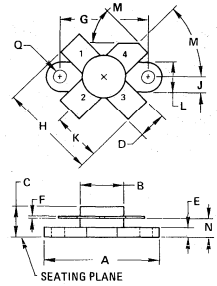
(1) This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF amplifier.

(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

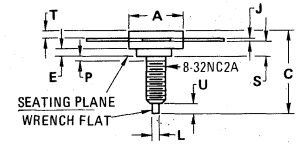


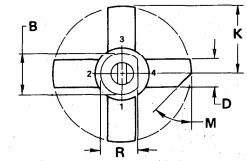
STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

MRF240A
CASE 211-07



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	9.40	9.91	0.370	0.390
C	5.82	7.14	0.229	0.281
D	5.46	5.97	0.215	0.235
E	2.16	2.67	0.085	0.105
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	20.07	20.57	0.790	0.810
K	10.03	10.29	0.395	0.405
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.81	4.57	0.150	0.180
Q	2.87	3.30	0.113	0.130





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	17.02	20.07	0.670	0.790
D	5.46	5.97	0.215	0.235
E	1.78	–	0.070	–
J	0.08	0.18	0.003	0.007
K	12.45	–	0.490	–
L	1.40	1.78	0.055	0.070
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.11	2.54	0.083	0.100
U	2.49	3.35	0.098	0.132

STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

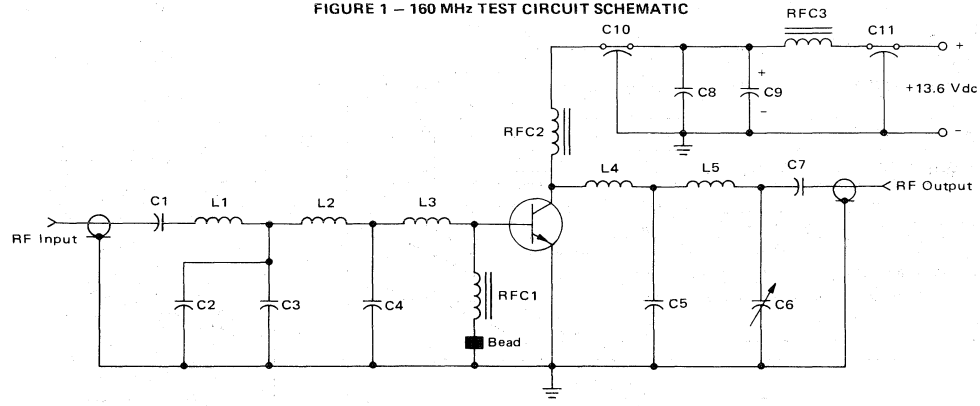
CASE 145A-09
MRF240

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	70	150	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	90	125	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 13.6 Vdc, P_{out} = 40 W, f = 160 MHz)	G_{PE}	9.0	10	–	dB
Collector Efficiency (V_{CC} = 13.6 Vdc, P_{out} = 40 W, f = 160 MHz)	η	55	–	–	%
TYPICAL SSB PERFORMANCE					
Intermodulation Distortion (1) (V_{CC} = 13.6 Vdc, P_{out} = 35 W(PEP), f1 = 146 MHz, f2 = 146.002 MHz, I_{CQ} = 50 mAdc)	IMD (d_3)	–	-30	–	dB

(1) To MIL-STD-1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.

FIGURE 1 – 160 MHz TEST CIRCUIT SCHEMATIC



C1	200 pF, 350 Vdc, UNELCO	C10,C11	680 pF ALLEN BRADLEY Feedthru	L3	1.2 x 0.6 cm Brass Pad
C2	100 pF, 350 Vdc, UNELCO	RFC1	0.15 μH Molded Choke	L4	1.2 x 0.6 cm Brass Pad and 2.0 x 0.2 cm AIRLINE Inductor
C3	40 pF, 350 Vdc, UNELCO	RFC2	10 Turns, #18 AWG on 470 Ohm, 1 Watt Resistor	Board:	G10, ϵ_r = 5, t = 62 mils 2 sided, 2 oz. Clad
C4,C5	80 pF, 350 Vdc, UNELCO	Bead	FERROXCUBE Bead		
C6	1.0–20 pF, ARCO Trimmer	RFC3	FERROXCUBE Choke, VK200-4B	Connectors:	Type N
C7	100 pF 350 Vdc, UNELCO	L1	3.3 x 0.2 cm AIRLINE Inductor		
C8	0.1 μF ERIE Disc Ceramic	L2	1.0 x 0.2 cm AIRLINE Inductor		
C9	1.0 μF TANTALUM				

FIGURE 2 – POWER GAIN versus FREQUENCY

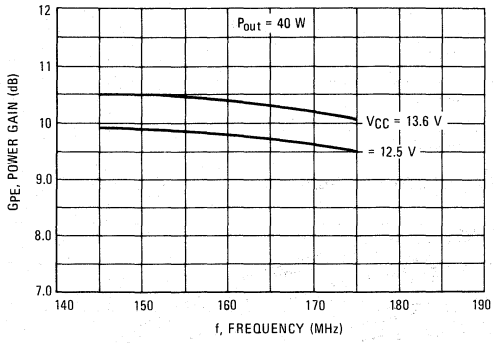


FIGURE 3 – OUTPUT POWER versus INPUT POWER

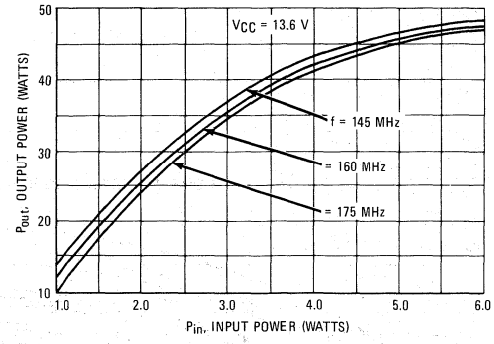


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE
145 MHz

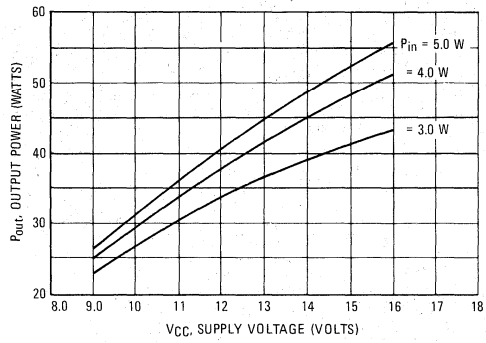


FIGURE 5 – OUTPUT POWER versus SUPPLY VOLTAGE
160 MHz

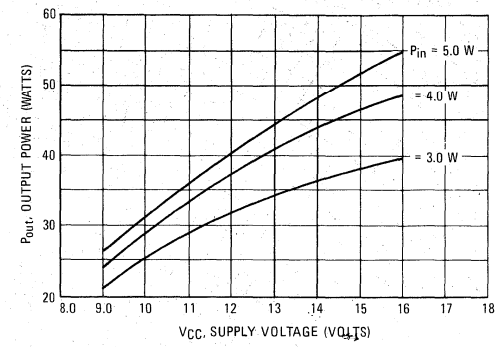


FIGURE 6 – OUTPUT POWER versus SUPPLY VOLTAGE
175 MHz

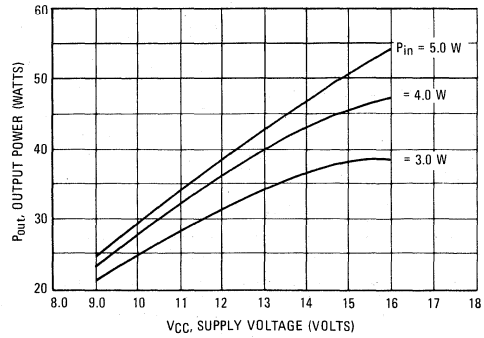
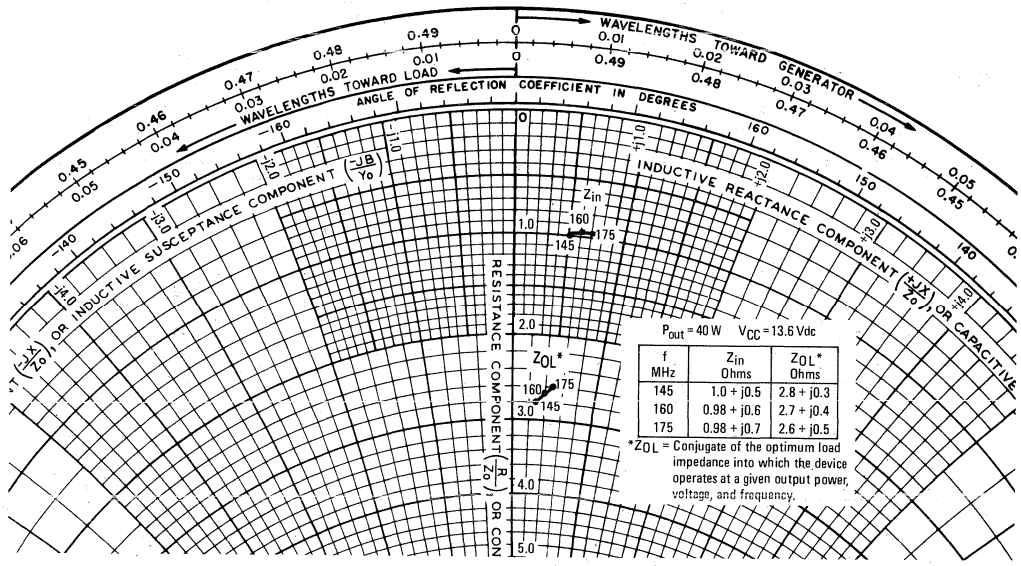


FIGURE 7 – SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCES



MRF247

The RF Line

75 W — 175 MHz

CONTROLLED Q
RF POWER
TRANSISTOR

NPN SILICON

NPN SILICON RF POWER TRANSISTOR

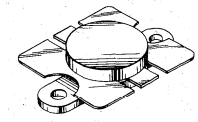
. . . designed for 12.5 Volt VHF large-signal amplifier applications in industrial and commercial FM equipment operating to 175 MHz.

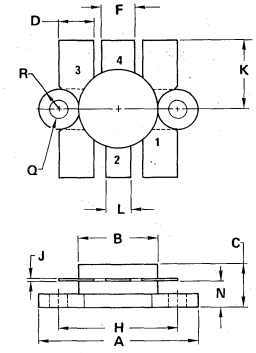
- Specified 12.5 Volt, 175 MHz Characteristics —

  Output Power = 75 Watts
  Minimum Gain = 7.0 dB
  Efficiency = 55%

- Characterized With Series Equivalent Large-Signal Impedance Parameters
- Internal Matching Network Optimized for Minimum Gain Frequency Slope Response Over the Range 136 to 175 MHz
- Load Mismatch Capability at Rated P_{out} and Supply Voltage

See AN-791 for Description of a 75 W PEP, 145 MHz Linear Amplifier.





STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. EMITTER
4. BASE
FLANGE-ISOLATED

CASE 316-01

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Peak	I_C	20	Adc
Total Device Dissipation @ $T_C = 25^oC$ (1) Derate Above 25^oC	P_D	250 1.43	Watts $W/^oC$
Storage Temperature Range	T_{stg}	-65 to +150	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R\theta JC$	0.7	$^oC/W$

(1) This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF amplifier.

(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	12.45	12.95	0.490	0.510
C	5.97	7.62	0.235	0.300
D	5.33	5.59	0.210	0.220
F	5.08	5.33	0.200	0.210
H	18.29	18.54	0.720	0.730
J	0.10	0.15	0.004	0.006
K	10.29	—	0.405	—
L	3.81	4.06	0.150	0.160
N	3.81	4.32	0.150	0.170
Q	2.92	3.30	0.115	0.130
R	3.05	3.30	0.120	0.130

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	75	150	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	235	300	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 75 Watts, f = 175 MHz)	G_{PE}	7.0	8.5	–	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 75 Watts, f = 175 MHz)	η	55	60	–	%
Load Mismatch (V_{CC} = 12.5 Vdc, P_{out} = 75 Watts, f = 175 MHz, VSWR = 30:1 All Phase Angles)	ψ	No Degradation In Output Power			

3

FIGURE 1 – OUTPUT POWER versus INPUT POWER

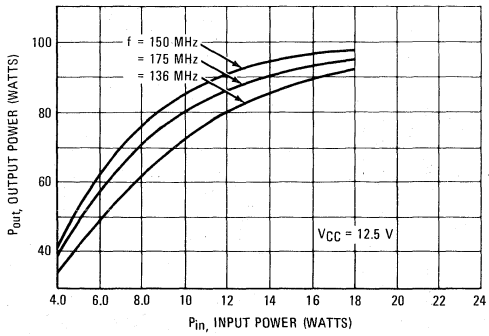


FIGURE 2 – POWER GAIN versus FREQUENCY

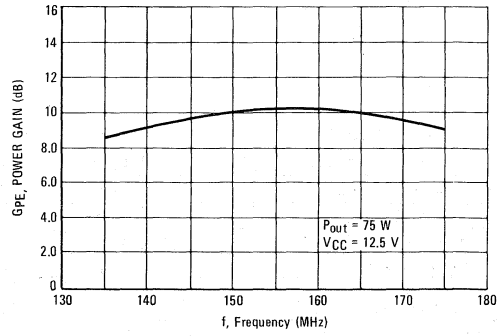


FIGURE 3 – OUTPUT POWER versus SUPPLY VOLTAGE
136 MHz

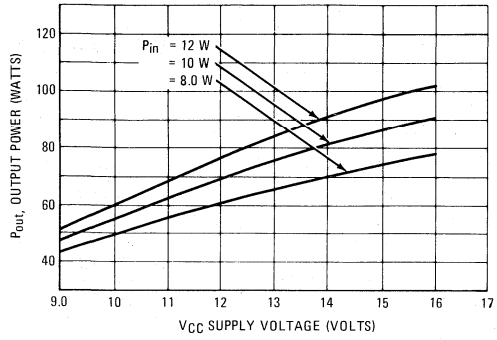


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE
150 MHz

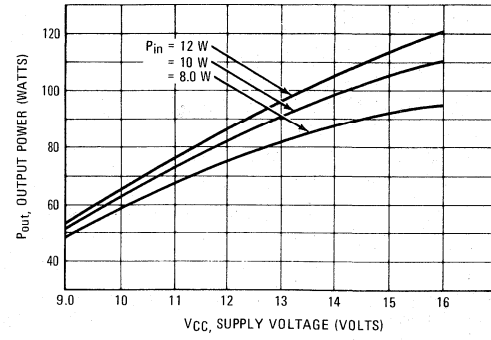


FIGURE 5 – OUTPUT POWER versus SUPPLY VOLTAGE
175 MHz

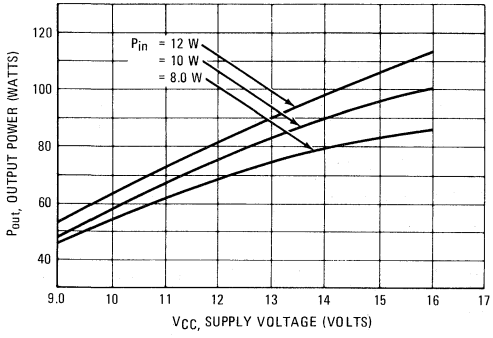
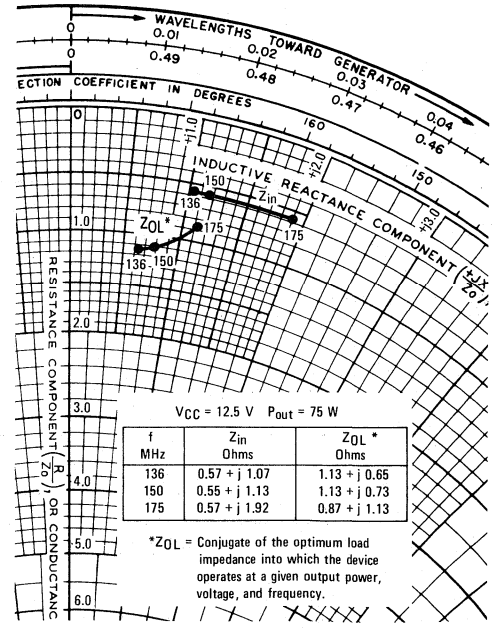


FIGURE 6 – SERIES EQUIVALENT IMPEDANCES



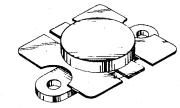
MRF248

The RF Line
NPN Silicon RF Power Transistor

80 WATTS, 175 MHz CONTROLLED Q RF POWER TRANSISTOR NPN SILICON

. . . designed for 12.5 volt VHF large-signal amplifier applications in industrial and commercial FM equipment operating to 175 MHz.

- Typical 12.5 Volt, 175 MHz Characteristics in Broadband Circuit:
  Output Power = 80 Watts
  Gain = 11.3 dB
  Efficiency = 59%
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internal Matching Network Optimized for Broadband Operation
- Ion Implanted Emitter Ballast Resistors for Improved Load Mismatch Capability at Elevated Drive and Voltage



CASE 316-01

3

MAXIMUM RATINGS

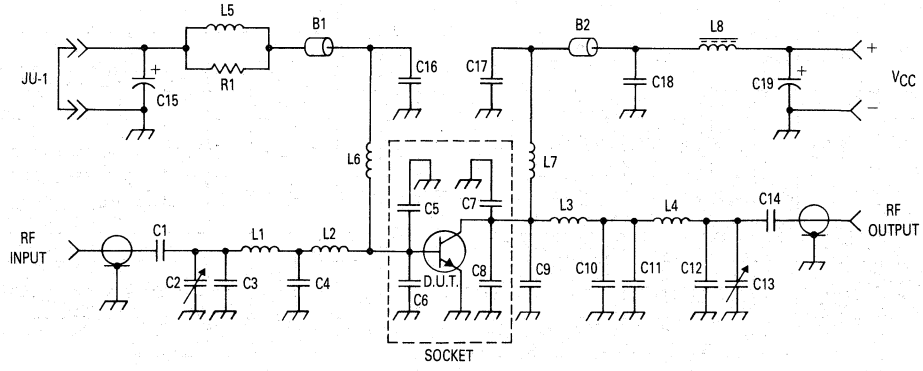
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16.5	Vdc
Collector-Base Voltage	V_{CBO}	38	Vdc
Emitter-Base Voltage	V_{EBO}	4	Vdc
Collector-Current — Continuous	I_C	15	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	250 1.43	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Emitter-Base Breakdown Voltage (I_E = 5 mAdc, I_C = 0)	$V_{(BR)EBO}$	4	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	16.5	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	38	—	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0)	I_{CES}	—	—	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 2 Adc, V_{CE} = 5 Vdc)	h_{FE}	20	—	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1 MHz)	C_{ob}	—	270	350	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 80 W, f = 175 MHz)	G_{pe}	10	11.3	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 80 W, f = 175 MHz)	η_c	50	59	—	%
Load Mismatch (V_{CC} = 15.5 Vdc, P_{in} = 2 dB Overdrive, f = 175 MHz, VSWR = 30:1 All Phase Angles)	ψ	No Degradation In Output Power			



C1, C14 — 1000 pF Chip Cap, ATC100B102JC50
C3 — 15 pF Unelco, Standex J-101-15
C2, C13 — 1–20 pF Johanson
C4 — 150 pF Unelco, Standex J-101-150
C5 — 300 pF Chip Cap, ATC100B301JC200
C6, C8 — 270 pF Chip Cap, ATC100B271JC200
C7 — 240 pF Chip Cap, ATC100B241JC200
C9, C11 — 80 pF Unelco, Standex J-101-80
C10 — 100 pF Unelco, Standex J-101-100
C12 — 30 pF Unelco, Standex J-101-30
C15, C19 — 10 μF/35 V
C16, C17 — 91 pF Mini-Unelco, Standex 3HS0006-91
C18 — 0.001 μF

L1 — 3 Turns #18 AWG, 0.165″ ID
L2, L3 — 0.2″W x 0.3″L, 5 mil Cu Sheet
L4 — 2 Turns #18 AWG, 0.165″ ID
L5 — 5.6 μH Choke, Cambion
L6, L7 — 3 Turns #18 AWG, 0.13″ ID
L8 — Ferrite Choke, Ferroxcube VK200-20-4B
B1, B2 — Ferrite Bead, Ferroxcube 56-590-65-3B
R1 — 10 Ω, 1/2 Watt
Board Material — 0.062″ G-10, 2 oz. Cu, $\epsilon_r \simeq 4.5$
JU-1 — Jumper for V_{re} Test Port

Figure 1. 135–175 MHz Broadband Test Circuit

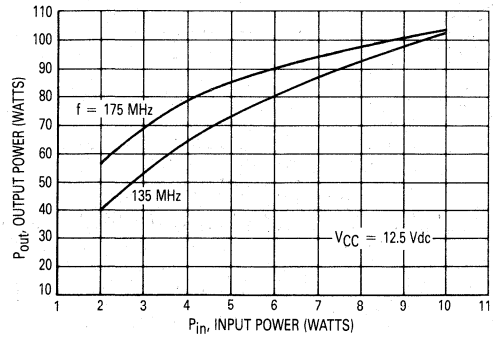


Figure 2. Output Power versus Input Power

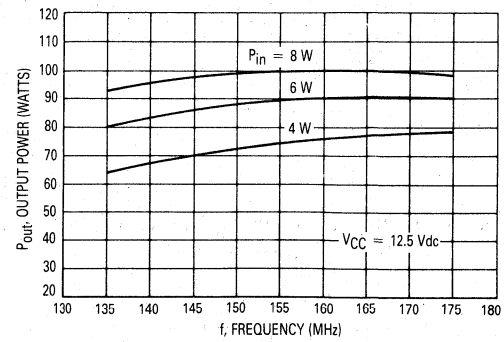


Figure 3. Output Power versus Frequency

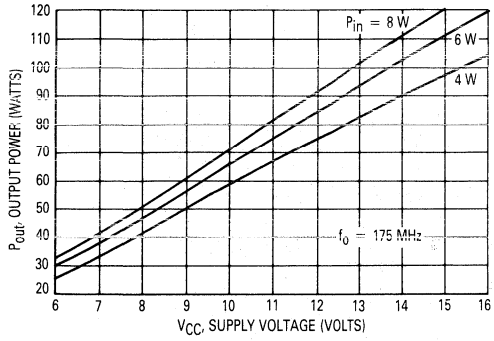


Figure 4. Output Power versus Voltage

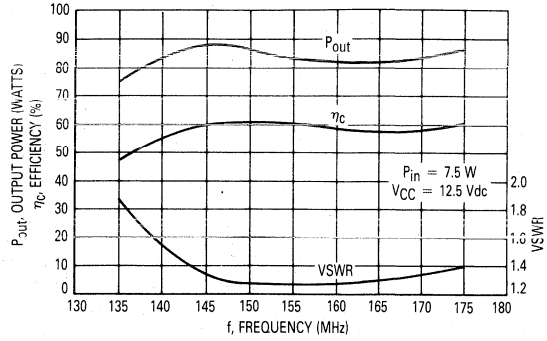
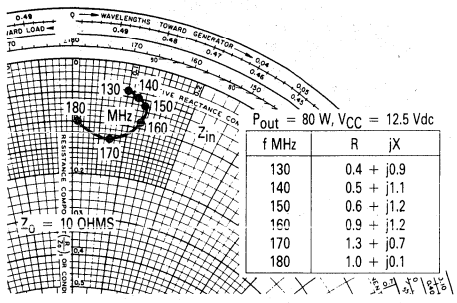
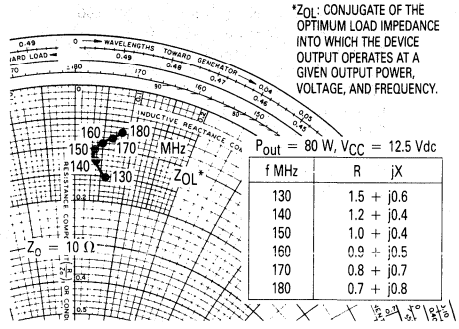


Figure 5. Typical Broadband Performance



f MHz	R	jX
130	0.4	+ j0.9
140	0.5	+ j1.1
150	0.6	+ j1.2
160	0.9	+ j1.2
170	1.3	+ j0.7
180	1.0	+ j0.1

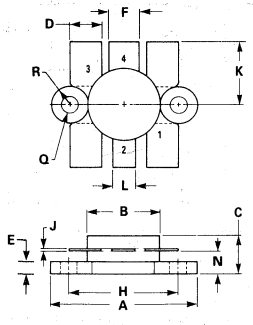
Figure 6. Z_{in}, Input Impedance



f MHz	R	jX
130	1.5	+ j0.6
140	1.2	+ j0.4
150	1.0	+ j0.4
160	0.9	+ j0.5
170	0.8	+ j0.7
180	0.7	+ j0.8

Figure 7. Z_{OL}*, Output Impedance

OUTLINE DIMENSIONS

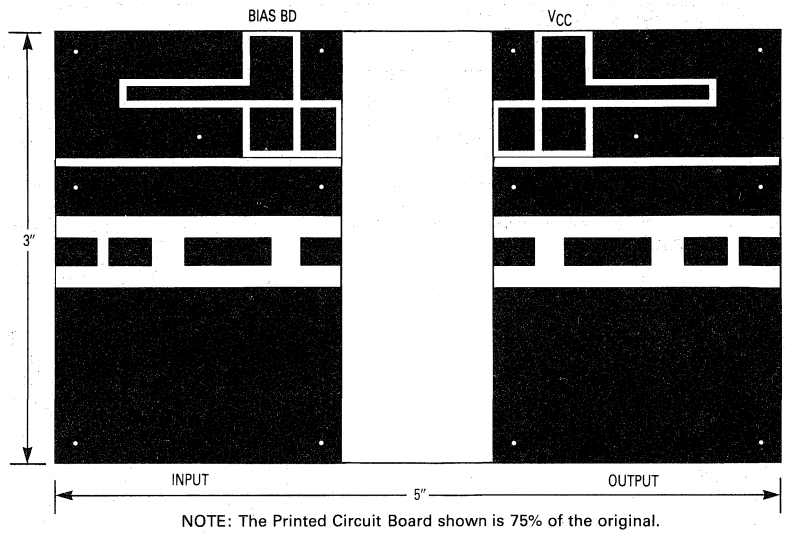


STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. EMITTER
4. BASE

CASE 316-01

NOTE:
FLANGE IS ISOLATED IN ALL STYLES.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.14	0.960	0.990
B	12.45	12.95	0.490	0.510
C	5.97	7.62	0.235	0.300
D	5.33	5.58	0.210	0.220
E	2.16	3.04	0.085	0.120
F	5.08	5.33	0.200	0.210
H	18.29	18.54	0.720	0.730
J	0.10	0.15	0.004	0.006
K	10.29	11.17	0.405	0.440
L	3.81	4.06	0.150	0.160
N	3.81	4.31	0.150	0.170
Q	2.92	3.30	0.115	0.130
R	3.05	3.30	0.120	0.130
U	11.94	12.57	0.470	0.495



NOTE: The Printed Circuit Board shown is 75% of the original.

Figure 8. MRF248 Photomaster

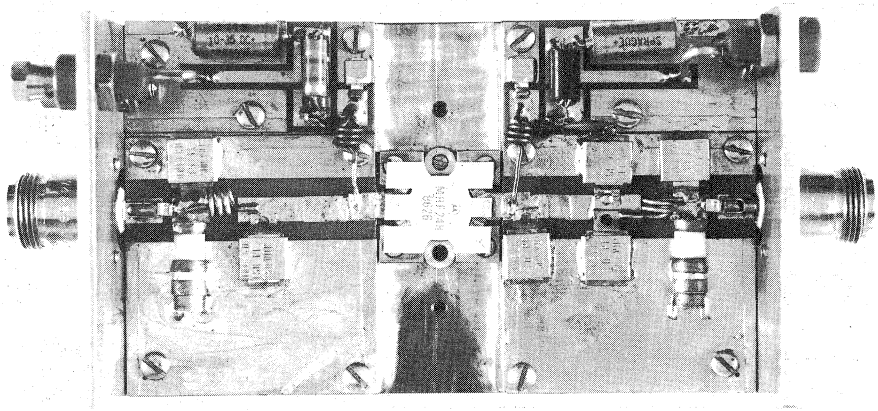


Figure 9. 136–175 MHz Test Circuit

MRF260

The RF Line

5 W 136–175 MHz

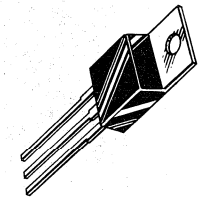
RF POWER TRANSISTOR

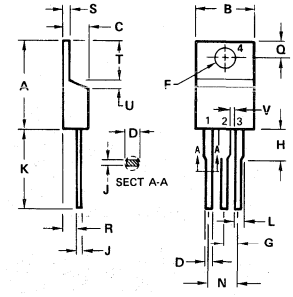
NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed for 12.5-volt VHF large-signal power amplifier applications in commercial and industrial equipment.

- Low-Cost Common-Emitter TO-220 Package
- Specified 12.5 V, 175 MHz Performance:
  - Output Power 5.0 Watts
  - Power Gain 10 dB Min
  - Efficiency 55% Min
- Load Mismatch Capability at High Line and rated RF Input
- Other Devices in the Series:
  - MRF262 15 Watts
  - MRF264 30 Watts





STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

NOTE:
1. DIM. L & H APPLIES TO ALL LEADS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

CASE 221A-02

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	1.0	Adc
Total Device Dissipation @ $T_C = 25^oC$ (1) Derate above 25^oC	P_D	12 68.5	Watts $mW/^oC$
Storage Temperature Range	T_{stg}	−65 to +150	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	14.6	$^oC/W$

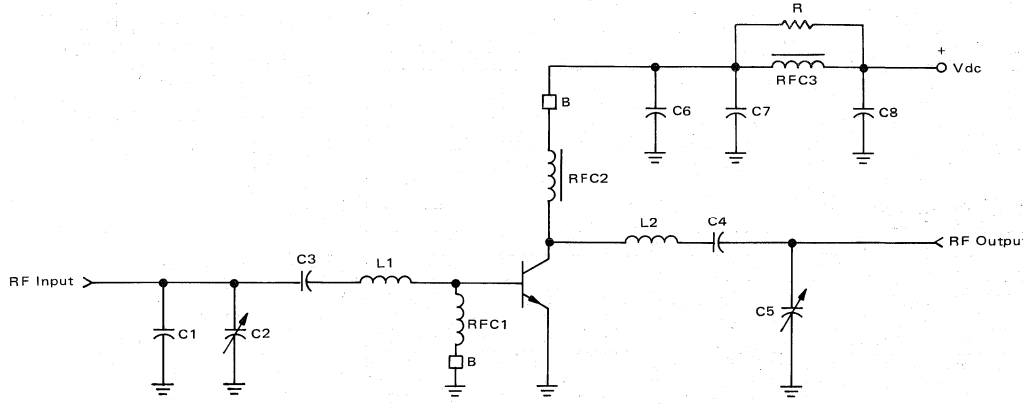
(1) This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF amplifier.

(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	0.25	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0	–	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	15	20	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 5.0 W, f = 175 MHz)	G_{PE}	10	11	–	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 5.0 W, f = 175 MHz)	η	55	–	–	%

FIGURE 1 – 175 MHz TEST CIRCUIT



C1 – 40 pF Underwood
C2, C5 – Johanson Trimmer #JMC-5501
C3 – 60 pF Underwood
C4 – 25 pF Underwood
C6 – 1000 pF Underwood
C7 – 0.1 μF Erie Red Cap
C8 – 100 μF Electrolytic, 15 V

L1 – 1-1/2 Turns, #18 AWG, 3/16" ID, l = 1/8"
L2 – 3 Turns, #18 AWG, 5/16" ID, l = 1/4"
R – 10 Ω, 1.0 W
B – Ferroxcube Bead 56-590-65-3B
RFC1 – 0.15 μH Molded Coil
RFC2 – 0.15 μH Molded Coil
RFC3 – Ferroxcube VK200-20-4B
Board Material:
Teflon Fiberglass – G10, thickness = 0.062 inches.

FIGURE 2 – POWER GAIN versus FREQUENCY

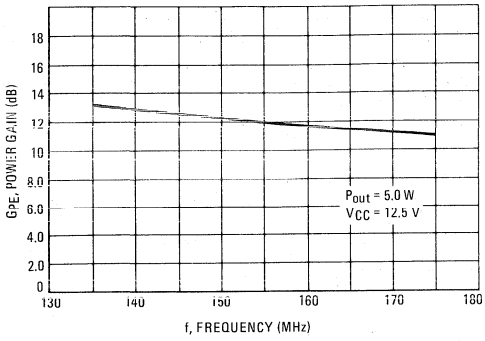


FIGURE 3 – OUTPUT POWER versus INPUT POWER

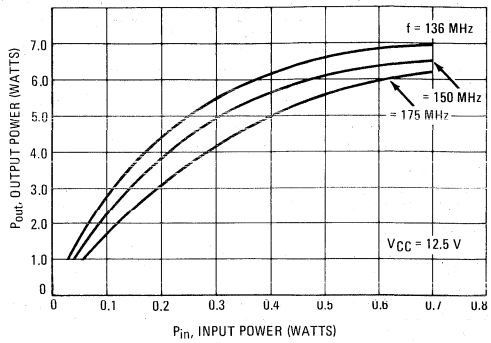


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE
136 MHz

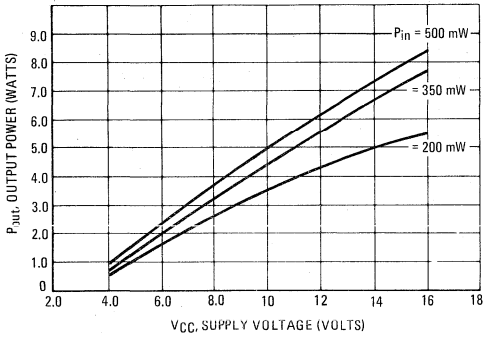


FIGURE 5 – OUTPUT POWER versus SUPPLY VOLTAGE
150 MHz

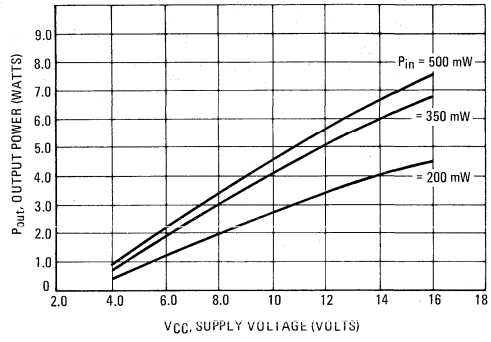


FIGURE 6 – OUTPUT POWER versus SUPPLY VOLTAGE
175 MHz

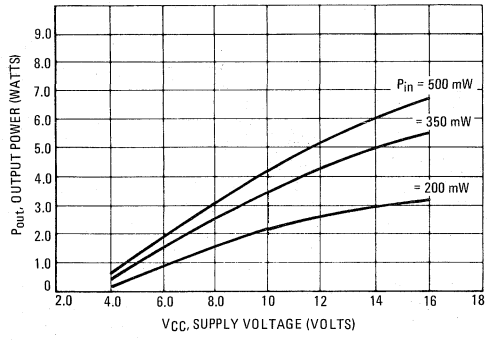


FIGURE 7 – SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCES

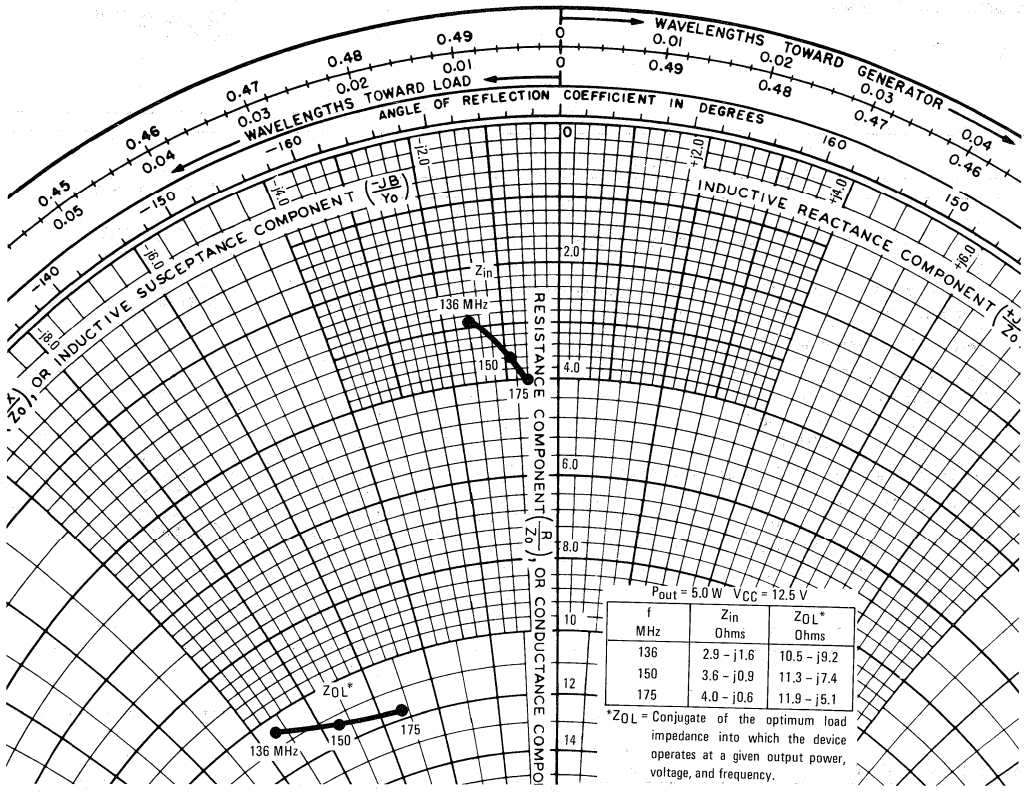
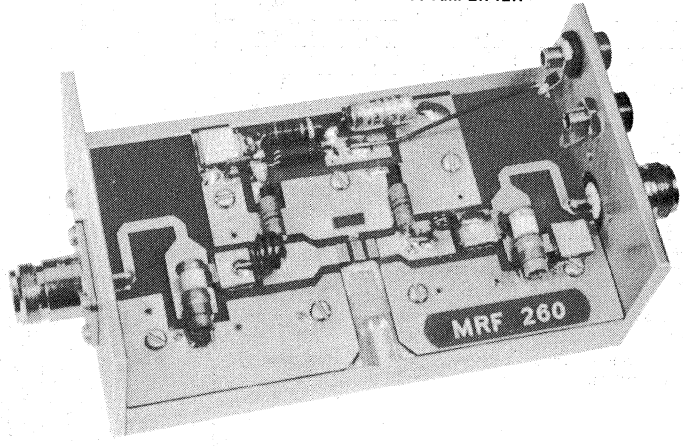


FIGURE 8 – 175 MHz TEST AMPLIFIER



MRF261

The RF Line

NPN SILICON RF POWER TRANSISTOR

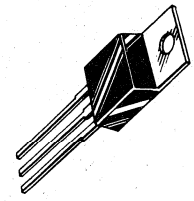
. . . designed for 12.5-volt VHF large-signal power amplifier applications in commercial and industrial equipment.

- Low-Cost, Common-Emitter TO-220 Package
- Specified 12.5 V, 175 MHz Performance —
  Output Power = 10 Watts
  Power Gain = 5.2 dB Min
  Efficiency = 50% Min
- Load Mismatch Capability at High Line and RF Overdrive
- Other Devices in the Series —
  MRF260 5.0 Watts
  MRF262 15 Watts
  MRF264 30 Watts

10 W 136-175 MHz

RF POWER TRANSISTOR

NPN SILICON



3

MAXIMUM RATINGS

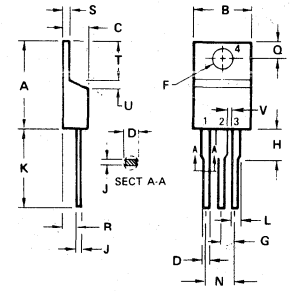
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Continuous	I_C	2.0	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	30 171	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	5.85	°C/W

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.



STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

NOTE:
1. DIM. L & H APPLIES TO ALL LEADS.

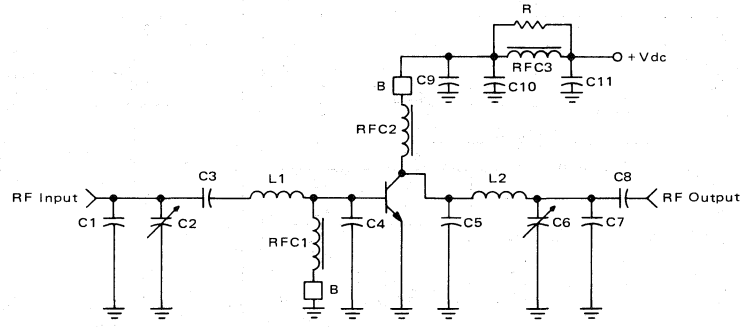
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

CASE 221A-02

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 2.5 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	—	—	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	65	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	35	50	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 10 W, f = 175 MHz)	G_{PE}	5.2	7.0	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 10 W, f = 175 MHz)	η	50	—	—	%

FIGURE 1 — 175-MHz TEST CIRCUIT



C1 — 10 pF Underwood
C2, C6 — Johanson Trimmer #5501
C3 — 60 pF Underwood
C4 — 150 pF Underwood
C5 — 100 pF Underwood
C7, C8 — 15 pF Underwood
C9 — 1000 pF Underwood
C10 — 0.1 μF Erie Red Cap
C11 — 100 μF Electrolytic, 15 Vdc

L1 — 2 Turns, #18 AWG, 5/16" ID
L2 — 1-1/2 Turns, #18 AWG, 5/16" ID
R — 10 Ω, 1.0 W
B — Ferroxcube Bead 56-590-65-3B
RFC1 — 0.15 μH Molded Coil
RFC2 — 6 Turns #18 Wire, 5/16" ID
RFC3 — VK200-20/4B
Board Material — Teflon Fiberglass
t = 0.062"

FIGURE 2 – POWER GAIN versus FREQUENCY

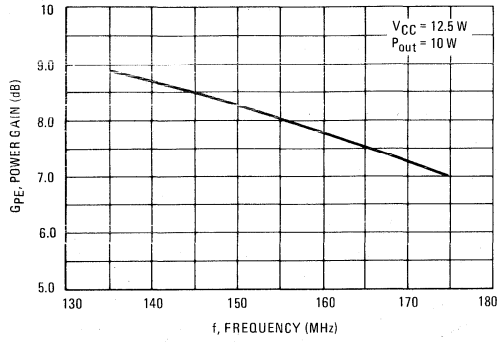


FIGURE 3 – OUTPUT POWER versus INPUT POWER

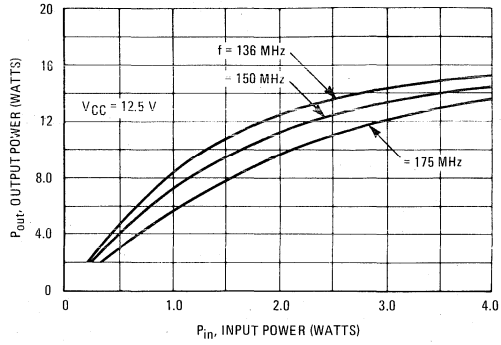


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE
136 MHz

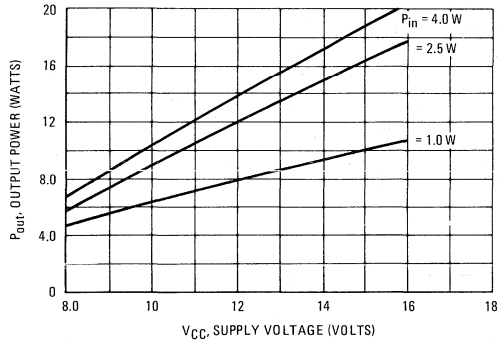


FIGURE 5 – OUTPUT POWER versus SUPPLY VOLTAGE
150 MHz

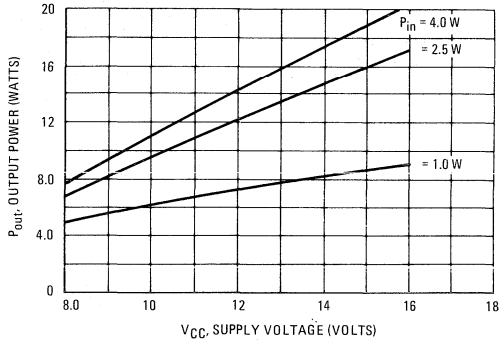


FIGURE 6 – OUTPUT POWER versus SUPPLY VOLTAGE
175 MHz

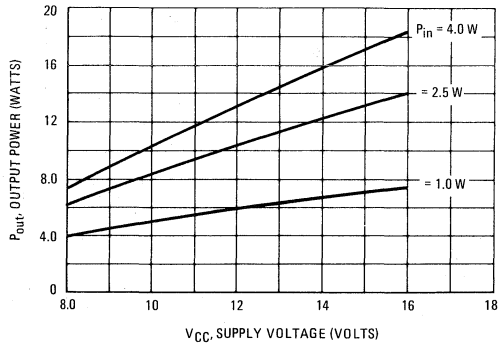
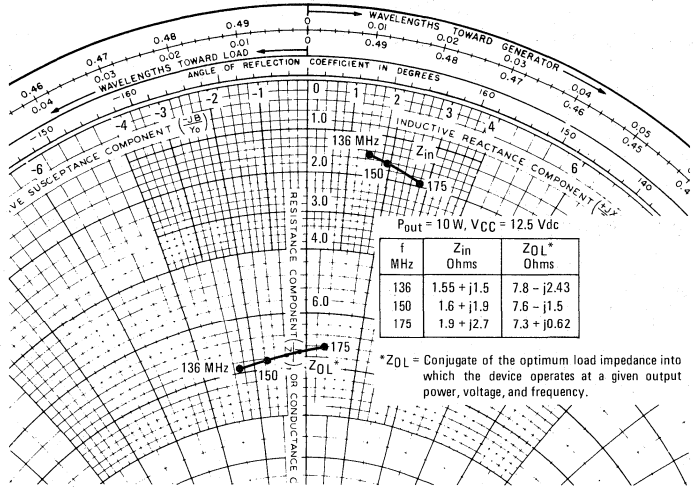


FIGURE 7 – SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCES



f MHz	Z_{in} Ohms	Z_{OL}* Ohms
136	1.55 + j1.5	7.8 – j2.43
150	1.6 + j1.9	7.6 – j1.5
175	1.9 + j2.7	7.3 + j0.62

*Z_{OL} = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

3

MRF262

The RF Line

15 W 136–175 MHz

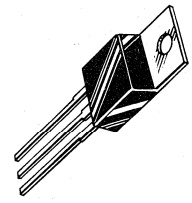
RF POWER TRANSISTOR

NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed for 12.5-volt VHF large-signal power amplifier applications in commercial and industrial equipment.

- Low-Cost Common-Emitter TO-220 Package
- Specified 12.5 V, 175 MHz Performance:
  - Output Power 15 Watts
  - Power Gain 6.3 dB Min
  - Efficiency 55% Min
- Load Mismatch Capability at Rated Voltage and RF Drive
- Other Devices in the Series:
  - MRF260 5.0 Watts
  - MRF264 30 Watts



3

MAXIMUM RATINGS

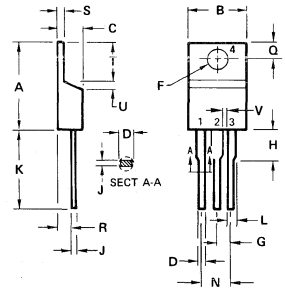
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	2.5	Adc
Total Device Dissipation @ $T_C = 25^oC$ (1) Derate above 25^oC	P_D	40 225	Watts $mW/^oC$
Storage Temperature Range	T_{stg}	−65 to +150	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	4.38	$^oC/W$

(1) This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF amplifier.

(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.



STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

NOTE:
1. DIM. L & H APPLIES TO ALL LEADS.

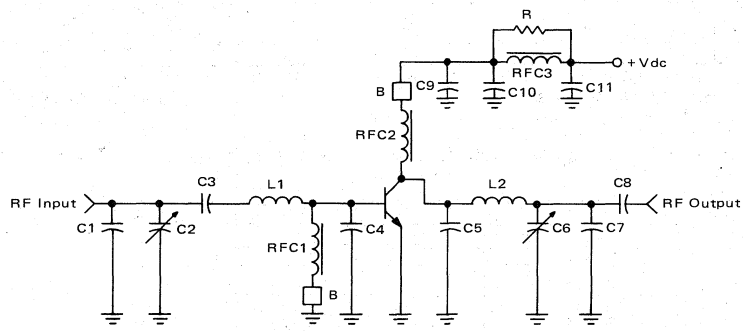
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

CASE 221A-02

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 2.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	0.5	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0	–	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz	C_{ob}	–	40	60	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 15 W, f = 175 MHz)	G_{PE}	6.3	8.2	–	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 15 W, f = 175 MHz)	η	55	–	–	%

FIGURE 1 – 175 MHz TEST CIRCUIT



C1 – 10 pF Underwood
C2, C6 – Johanson Trimmer #5501
C3 – 60 pF Underwood
C4 – 150 pF Underwood
C5 – 100 pF Underwood
C7, C8 – 15 pF Underwood
C9 – 1000 pF Underwood
C10 – 0.1 μF Erie Red Cap
C11 – 100 μF Electrolytic, 15 Vdc

L1 – 2 Turns, #18 AWG, 5/16" ID
L2 – 1-1/2 Turns, #18 AWG, 5/16" ID
R – 10 Ω, 1.0 W
B – Ferroxcube Bead 56-590-65-3B
RFC1 – 0.15 μH Molded Coil
RFC2 – 6 Turns #18 Wire, 5/16" ID
RFC3 – VK200-20/4B
Board Material – Teflon Fiberglass
t = 0.062"

FIGURE 2 – POWER GAIN versus FREQUENCY

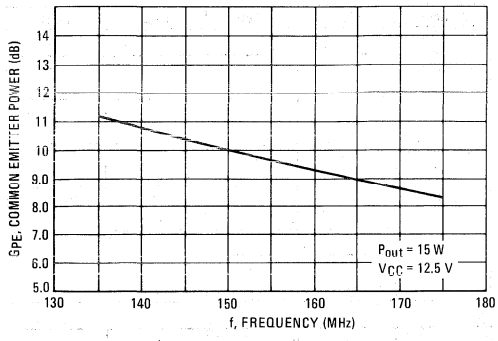


FIGURE 3 – OUTPUT POWER versus INPUT POWER

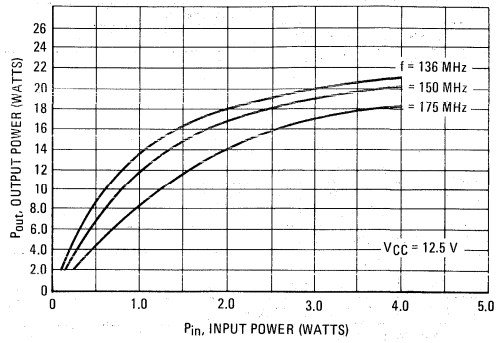


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE
136 MHz

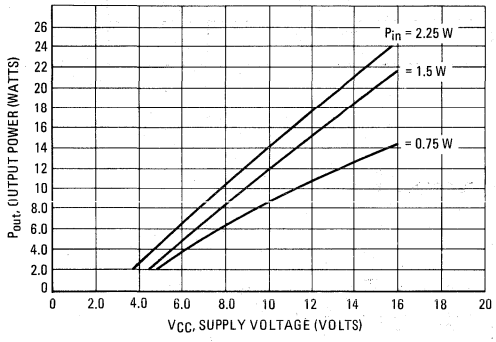


FIGURE 5 – OUTPUT POWER versus SUPPLY VOLTAGE
150 MHz

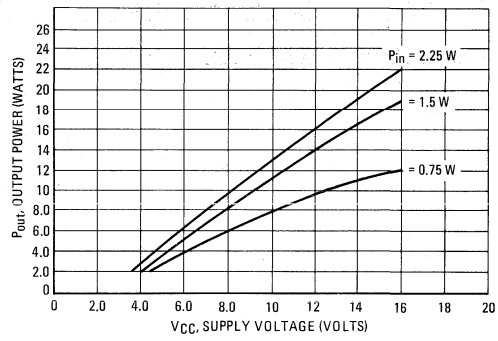


FIGURE 6 – OUTPUT POWER versus SUPPLY VOLTAGE
175 MHz

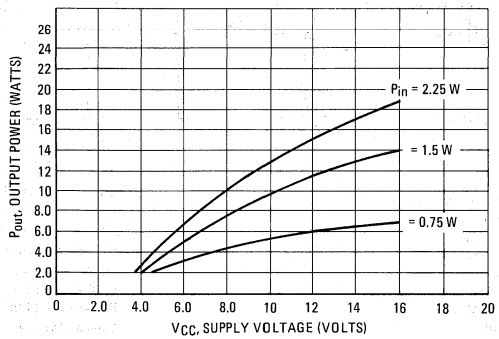


FIGURE 7 – SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCES

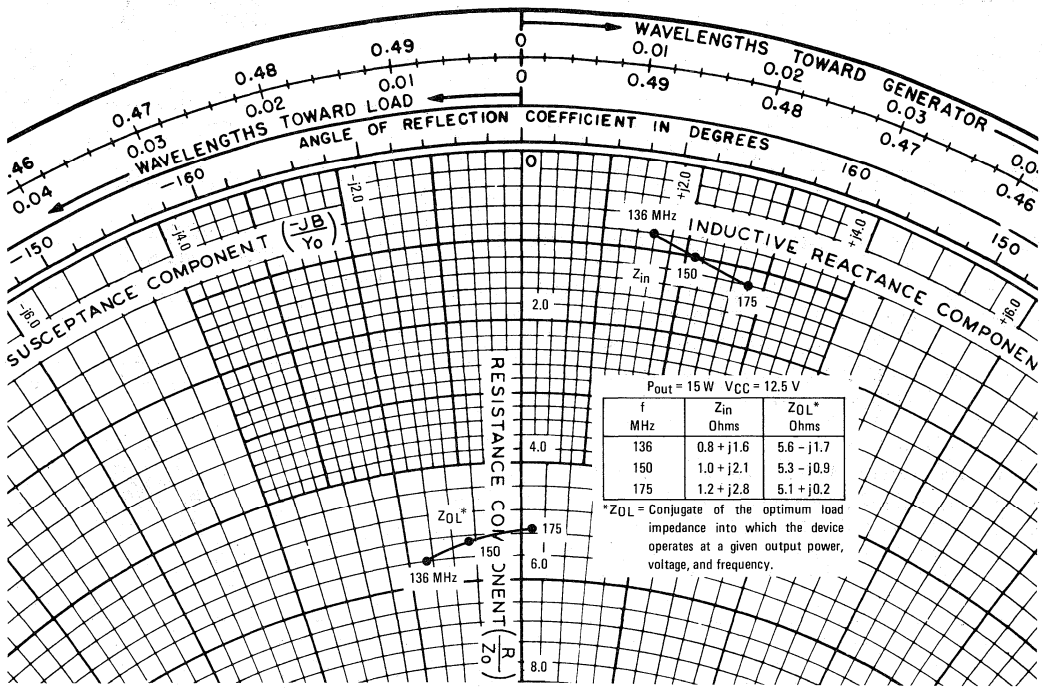
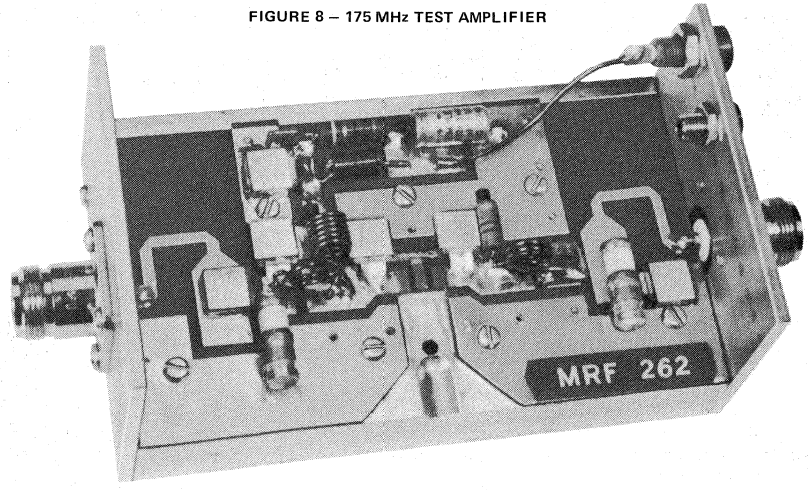


FIGURE 8 – 175 MHz TEST AMPLIFIER



MRF264

The RF Line

30 W 136–175 MHz

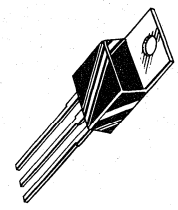
RF POWER TRANSISTOR

NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed for 12.5-volt VHF large-signal power amplifier applications in commercial and industrial FM equipment.

- Low-Cost, Common-Emitter TO-220 Package
- Specified 12.5 V, 175 MHz Performance —
  Output Power = 30 Watts
  Power Gain = 5.2 dB Min
  Efficiency = 60% Min
- Load Mismatch Capability at High Line and RF Overdrive
- Other Devices in the Series —
  MRF260 5.0 Watts
  MRF261 10 Watts
  MRF262 15 Watts



3

MAXIMUM RATINGS

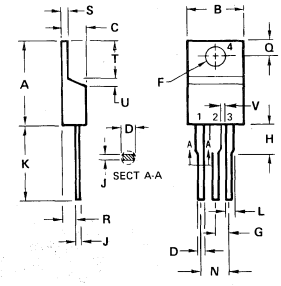
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Continuous	I_C	6.0	Adc
Total Device Dissipation @ T_A = 25°C (1) Derate above 25°C	P_D	80 0.64	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	1.56	°C/W

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.



STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

NOTE:
1. DIM. L & H APPLIES TO ALL LEADS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

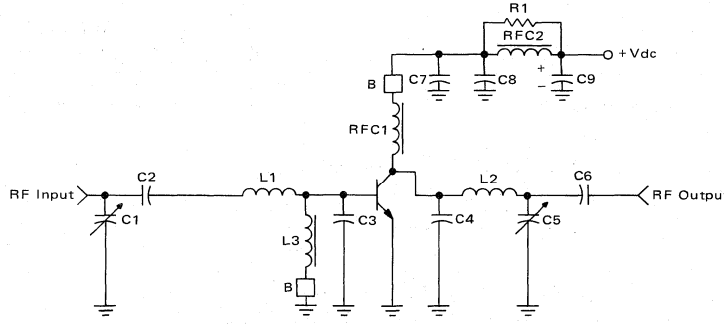
CASE 221A-02

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CES}	—	—	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	20	50	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	70	85	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 30 W, f = 175 MHz)	G_{PE}	5.2	6.0	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 30 W, f = 175 MHz)	η	60	—	—	%

3

FIGURE 1 – 175 MHz TEST CIRCUIT



C1, C5 – 1.0-20 pF Johanson
C2 – 25 pF Unelco
C3 – 120 pF Unelco
C4 – 100 pF Unelco
C6 – 15 pF Unelco
C7 – 1000 pF Unelco
C8 – 0.1 pF Erie Redcap
C9 – 100 μF, Electrolytic, 15 Vdc

L1 – 2-1/2 Turns, #16 AWG 0.35" ID
L2 – 2 Turns, #16 AWG 0.25" ID
L3 – 0.15 μH Molded Choke

RFC1 – 5 Turns, #18 AWG 0.25" ID
RFC2 – Ferroxcube VK200 21/4B

R1 – 10 Ω, 2.0 W

B – Ferroxcube Bead 56-590-65-3B

FIGURE 2 – POWER GAIN versus FREQUENCY

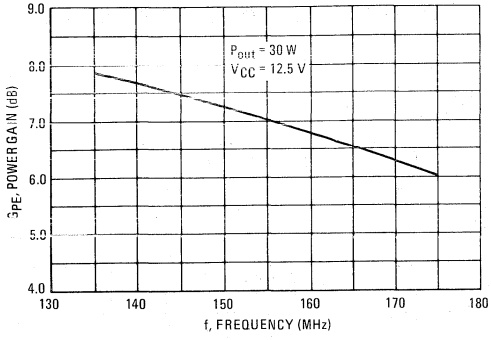


FIGURE 3 – OUTPUT POWER versus INPUT POWER

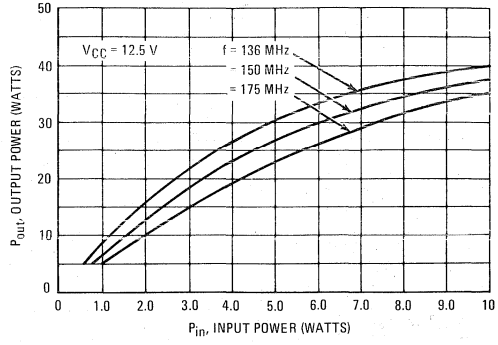


FIGURE 4 – OUTPUT POWER SUPPLY VOLTAGE
136 MHz

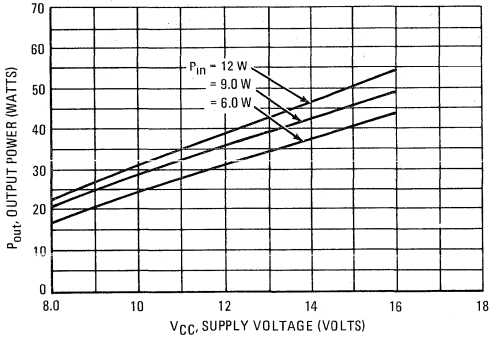


FIGURE 5 – OUTPUT POWER versus SUPPLY VOLTAGE
150 MHz

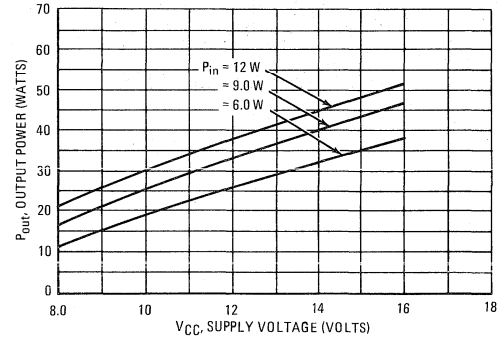


FIGURE 6 – OUTPUT POWER versus SUPPLY VOLTAGE
175 MHz

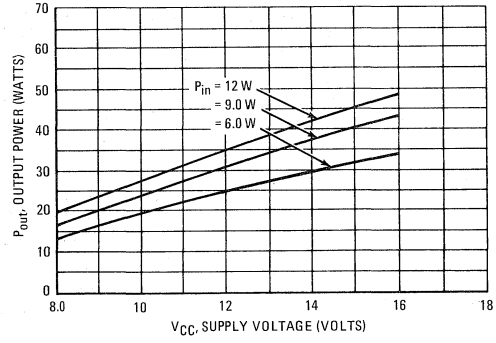
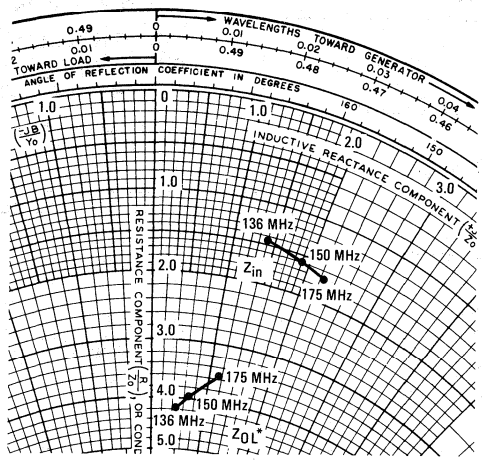


FIGURE 7 – SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCES



P_{out} = 30 W, V_{CC} = 12.5 V

f MHz	Z_{in} Ohms	Z_{OL}^* Ohms
136	1.44 + j1.4	4.16 + j0.48
150	1.55 + j1.92	3.96 + j0.65
175	1.67 + j2.22	3.59 + j1.17

*Z_{OL} = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

3

MRF309

The RF Line

NPN SILICON RF POWER TRANSISTOR

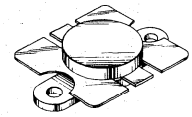
. . . designed primarily for wideband large-signal output amplifier stages in the 420–450 MHz frequency range.

- Guaranteed Performance in 450 MHz Amplifier @ 28 Vdc
  Output Power = 50 Watts
  Minimum Gain = 7.0 dB @ 450 MHz
- Built-In Matching Network for Broadband Operation Using Double Match Technique
- 100% Tested for Load Mismatch at all Phase Angles with 20:1 VSWR
- Engineering Bulleting, EB67, describes the construction of a 100 W (PEP), 420 to 450 MHz linear amplifier using a pair of MRF309's

50 W–450 MHz

CONTROLLED "Q" BROADBAND RF POWER TRANSISTOR

NPN SILICON



3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	33	Vdc
Collector-Base Voltage	V_{CBO}	60	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	146 0.83	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

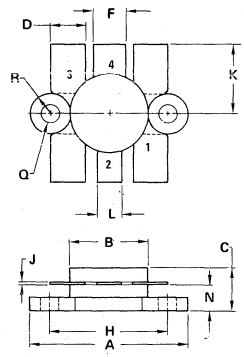
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.2	°C/W

(1)These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

MATCHING PROCEDURE

In the push-pull circuit configuration it is preferred that the transistors are used as matched pairs to obtain optimum performance.

The matching procedure used by Motorola consists of measuring h_{FE} at the data sheet conditions and color coding the device to predetermined h_{FE} ranges within the normal h_{FE} limits. A color dot is added to the marking on top of the cap. Any two devices with the same color dot can be paired together to form a matched set of units.



STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. EMITTER
4. BASE
FLANGE-ISOLATED

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	12.45	12.95	0.490	0.510
C	5.97	7.62	0.235	0.300
D	5.33	5.59	0.210	0.220
F	5.08	5.33	0.200	0.210
H	18.29	18.54	0.720	0.730
J	0.10	0.15	0.004	0.006
K	10.29	–	0.405	–
L	3.81	4.06	0.150	0.160
N	3.81	4.32	0.150	0.170
Q	2.92	3.30	0.115	0.130
R	3.05	3.30	0.120	0.130

CASE 316-01

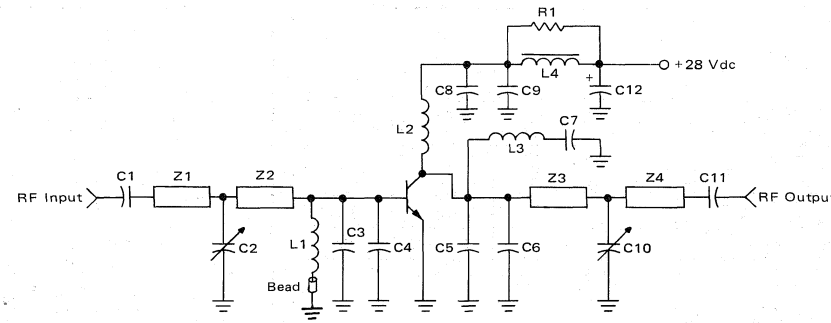
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	33	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	–	100	–
FUNCTIONAL TESTS (Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 50 W, f = 450 MHz)	G_{PE}	7.0	8.0	–	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 50 W, f = 450 MHz)	η	50	–	–	%
Electrical Ruggedness (P_{out} = 50 W, V_{CC} = 28 Vdc, f = 450 MHz, VSWR 20:1 all phase angles)	–	No Degradation in P_{out}			
Series Equivalent Input/Output Impedance (V_{CC} = 28 Vdc, P_{out} = 50 W, f = 450 MHz)	Z_{in} 0.7 + j1.6		Z_{OL}* 1.9 + j0.9		

NOTE: For linear operation, apply forward bias such that I_{CQ} (no RF signal) is 5.0–50 mA.

*Z_{OL} = Conjugate of the load impedance into which the device output operates at a given output power, supply voltage and frequency.

FIGURE 1 – 450 MHz TEST AMPLIFIER



C3, C4, C5 – Underwood 25 pF
C2, C10 – Johanson #JMC 5501 1–20 pF
C6 – Underwood 15 pF
C7, C8 – 0.1 μF Erie Red Cap, 100 V
C9 – Underwood 80 pF
C1, C11 – Underwood 40 pF
C12 – 1.0 μF Tantalum

Z1 – Microstrip 0.200" W X 0.900" L
Z2 – Microstrip 0.200" W X 0.200" L
Z3 – Microstrip 0.200" W X 0.500" L
Z4 – Microstrip 0.200" W X 0.650" L

L1, L3 – RFC, 0.15 μH Molded Coil
L2 – RFC, 4 Turns #20 Wire, 3/8" ID, 1/2" long
L4 – RFC, Ferroxcube VK200 19/4B

R1 – 5.6 Ω

Bead – Ferroxcube 56-590-65/4B

Board Material – 0.062" Thick glass – Teflon, ϵ_r = 2.56

MRF313

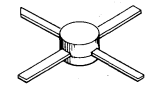
The RF Line

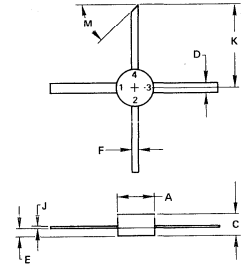
1.0 W — 400 MHz
HIGH FREQUENCY
TRANSISTOR
NPN SILICON

NPN SILICON HIGH FREQUENCY TRANSISTOR

. . . designed for wide band amplifier, driver or oscillator applications in military, mobile, and aircraft radio.

- Specified 28 Volt, 400 MHz Characteristics —
  Output Power = 1.0 Watt
  Minimum Gain = 15 dB
  Efficiency = 45%.
- Emitter Ballast and Low Current Density for Improved MTBF
- Common Emitter for Improved Stability





STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.08	5.59	0.200	0.220
C	2.41	3.30	0.095	0.130
D	1.40	1.65	0.055	0.065
E	1.02	1.27	0.040	0.050
F	0.64	0.89	0.025	0.035
J	0.08	0.18	0.003	0.007
K	11.05	—	0.435	—
M	45° NOM		45° NOM	

MRF313
CASE 305A-01

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector — Emitter Voltage	V_{CEO}	30	Vdc
Collector — Base Voltage	V_{CBO}	40	Vdc
Emitter — Base Voltage	V_{EBO}	3.0	Vdc
Collector Current — Continuous	I_C	150	mAdc
Total Device Dissipation @ $T_C = 25^oC$	P_D	2.5	Watts
Derate above 25^oC		35	$mW/^oC$
Storage Temperature Range	T_{stg}	−65 to +150	^oC

THERMAL CHARACTERISTICS

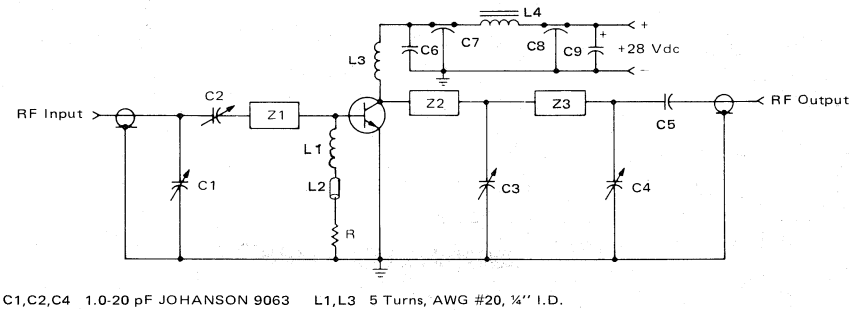
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	28.5	$^oC/W$

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	35	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	35	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0)	I_{CEO}	–	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 10 Vdc)	h_{FE}	20	60	150	–
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 100 mAdc, V_{CE} = 20 Vdc, f = 200 MHz)	f_T	–	2.5	–	GHz
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	3.5	5.0	pF
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain(1) (V_{CC} = 28 Vdc, P_{out} = 1.0 W, f = 400 MHz)	G_{pe}	15	16	–	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 1.0 W, f = 400 MHz)	η	–	45	–	%
Series Equivalent Input Impedance (V_{CC} = 28 Vdc, P_{out} = 1.0 W, f = 400 MHz)	Z_{in}	–	6.4-j4.8	–	Ohms
Series Equivalent Output Impedance (V_{CC} = 28 Vdc, P_{out} = 1.0 W, f = 400 MHz)	Z_{out}	–	75-j45	–	Ohms

(1) Class C

FIGURE 1 – 400 MHz POWER GAIN TEST CIRCUIT



C1,C2,C4 1.0-20 pF JOHANSON 9063
C3 1.0-10 pF JOHANSON
C5 150 pF Chip
C6 0.1 μF
C7,C8 680 pF Feedthru
C9 1.0 μF TANTALUM

L1,L3 5 Turns, AWG #20, ¼" I.D.
L2 Ferrite Bead, FERROXCUBE No. 56-590-65/4B
L4 FERROXCUBE VK200-20/4B
Input/Output Connectors – Type N
Board – Glass Teflon, ϵ = 2.56, t = 0.062"

R 4.7 Ohms, ¼ W
Z1 2.0" x 0.1" MICROSTRIP LINE
Z2,Z3 2.6" x 0.1" MICROSTRIP LINE

3

MRF314
MRF314A

The RF Line

NPN SILICON RF POWER TRANSISTOR

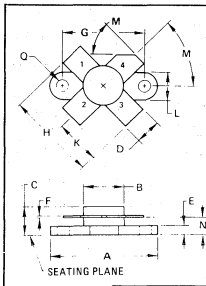
. . . designed primarily for wideband large-signal driver and output amplifier stages in the 30–200 MHz frequency range.

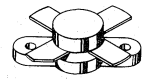
- Guaranteed Performance at 150 MHz, 28 Vdc
  Output Power = 30 Watts
  Minimum Gain = 10 dB
- 100% Tested for Load Mismatch at All Phase Angles with 30:1 VSWR
- Gold Metallization System for High Reliability Applications

30 W–30–200 MHz

RF POWER TRANSISTOR

NPN SILICON





MRF314

STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	24.64	24.89	0.970	0.980
B	9.40	9.91	0.370	0.390
C	5.82	7.14	0.229	0.281
D	5.46	5.97	0.215	0.235
E	2.16	2.67	0.085	0.105
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	20.07	20.57	0.790	0.810
K	10.03	10.28	0.395	0.405
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.81	4.57	0.150	0.180
Q	2.87	3.30	0.113	0.130

CASE 211-07

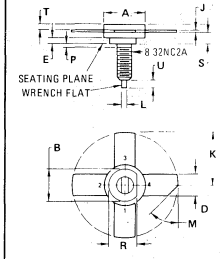
MAXIMUM RATINGS

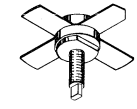
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	35	Vdc
Collector-Base Voltage	V_{CBO}	65	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	3.4	Adc
Total Device Dissipation @ $T_C = 25^oC$ (1) Derate above 25^oC	P_D	82 0.47	Watts $W/^oC$
Storage Temperature Range	T_{stg}	-65 to +150	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.13	$^oC/W$

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.





MRF314A

STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	17.02	20.07	0.670	0.790
D	5.46	5.97	0.215	0.235
E	1.78	–	0.070	–
J	0.08	0.18	0.003	0.007
K	12.45	–	0.490	–
L	1.40	1.78	0.055	0.070
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.11	2.54	0.083	0.100
U	2.49	3.35	0.098	0.132

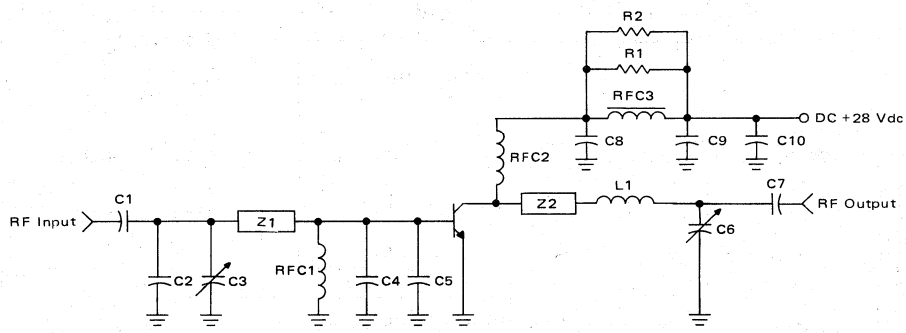
CASE 145A-09

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 30 mAdc, I_B = 0)	$V_{(BR)CEO}$	35	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 30 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	65	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 30 mAdc, I_E = 0)	$V_{(BR)CBO}$	65	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 3.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	–	3.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.5 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	–	80	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 30 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	30	40	pF
FUNCTIONAL TESTS (Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 30 W, f = 150 MHz)	G_{PE}	10	13.5	–	db
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 30 W, f = 150 MHz)	η	50	–	–	%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 30 W, f = 150 MHz, VSWR = 30:1 all phase angles	–	No Degration in Power Output			

FIGURE 1 – 150 MHz TEST CIRCUIT



C1, C7 – 18 pF, 100 mil ATC
C2 – 68 pF, 100 mil ATC
C3, C6 – Johanson #JMC 5501
C4 – 270 pF, 100 mil ATC
C5 – 240 pF, 100 mil ATC
C8, C9 – 100 pF Underwood
C10 – 1.0 μF Tantalum

L1 – 2 Turns, 2.5" #20 Wire, ID = 0.275"

R1, R2 – 10 Ω, 1.0 W

RFC1 – 15 μH Molded Coil
RFC2 – 2 Turns, 2.5" #20 Wire, ID = 0.2"
RFC3 – Ferroxcube VK200–19/4B

Z1 – Microstrip 0.168" W x 1.6" L
Z2 – Microstrip 0.168" W x 1.2" L

Board – Glass Teflon $\epsilon_R \approx 2.55$

TYPICAL PERFORMANCE CURVES

FIGURE 2 – OUTPUT POWER versus INPUT POWER

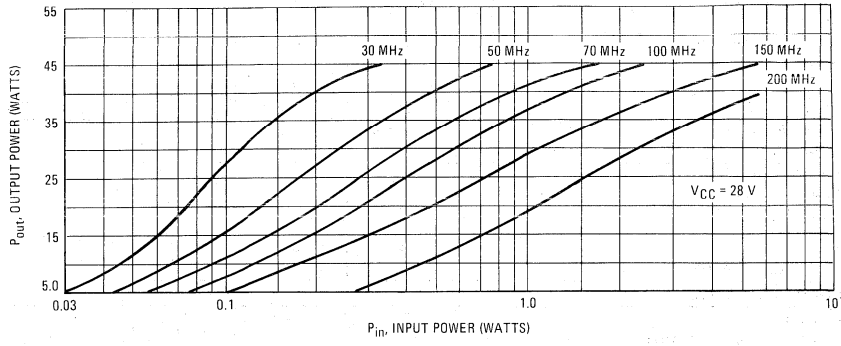


FIGURE 3 – OUTPUT POWER versus INPUT POWER

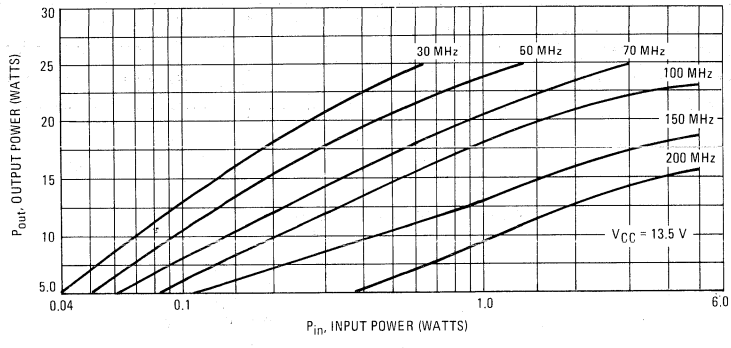


FIGURE 4 – POWER GAIN versus FREQUENCY

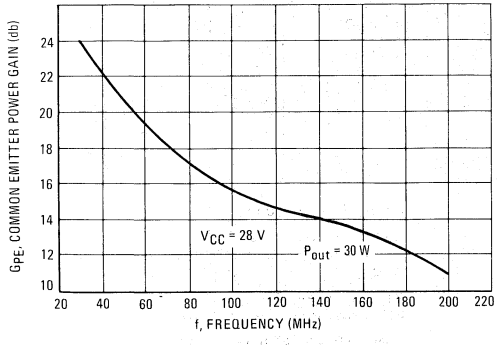


FIGURE 5 – EFFICIENCY (η%) versus FREQUENCY

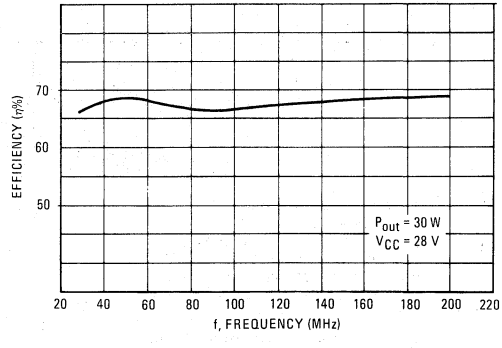
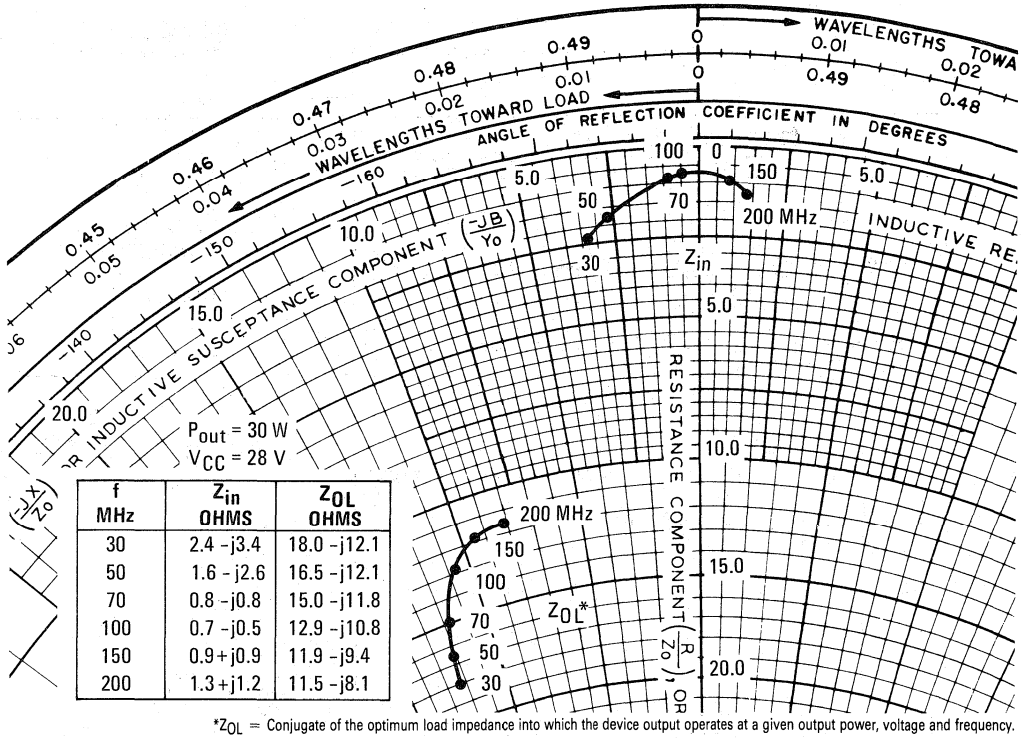


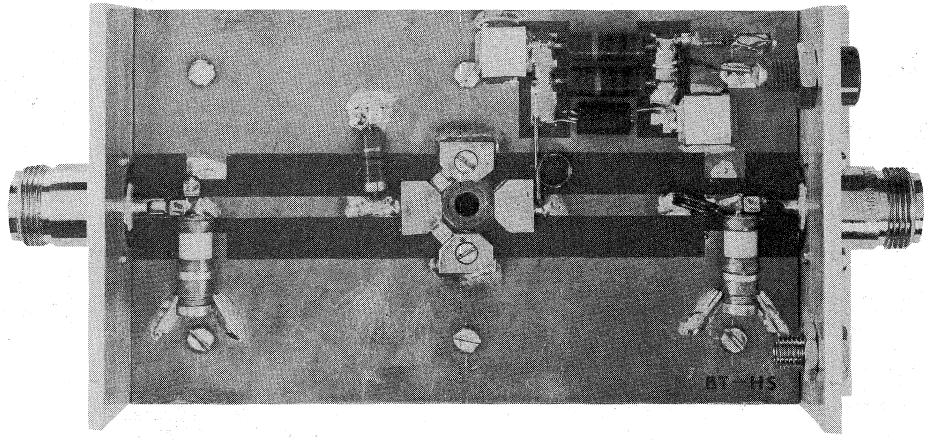
FIGURE 6 – SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCE



f MHz	Z_{in} OHMS	Z_{OL} OHMS
30	2.4 -j3.4	18.0 -j12.1
50	1.6 - j2.6	16.5 -j12.1
70	0.8 -j0.8	15.0 -j11.8
100	0.7 -j0.5	12.9 -j10.8
150	0.9+j0.9	11.9 -j9.4
200	1.3+j1.2	11.5 -j8.1

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

FIGURE 7 – TEST FIXTURE



3

MRF315
MRF315A

The RF Line

45 W – 30-200 MHz

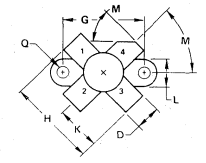
RF POWER TRANSISTOR

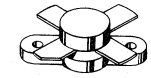
NPN SILICON

NPN SILICON RF POWER TRANSISTOR

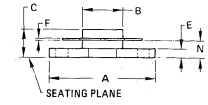
. . . designed primarily for wideband large-signal output amplifier stages in the 30–200 MHz frequency range.

- Guaranteed Performance at 150 MHz, 28 Vdc
  - Output Power = 45 Watts
  - Minimum Gain = 9.0 dB
- 100% Tested for Load Mismatch at All Phase Angles with 30:1 VSWR
- Gold Metallization System for High Reliability Applications





MRF315



STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	24.64	24.89	0.970	0.980
B	9.40	9.91	0.370	0.390
C	5.82	7.14	0.229	0.281
D	5.46	5.97	0.215	0.235
E	2.16	2.67	0.085	0.105
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	20.07	20.57	0.790	0.810
K	10.03	10.29	0.395	0.405
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.81	4.57	0.150	0.180
Q	2.87	3.30	0.113	0.130

CASE 211-07

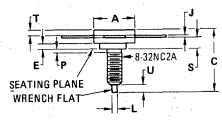
MAXIMUM RATINGS

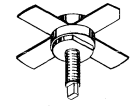
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	35	Vdc
Collector-Base Voltage	V_{CBO}	65	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	4.0	Adc
Total Device Dissipation @ $T_C = 25^oC$ (1) Derate above 25^oC	P_D	110 0.63	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

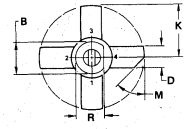
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.59	°C/W

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.





MRF315A



STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

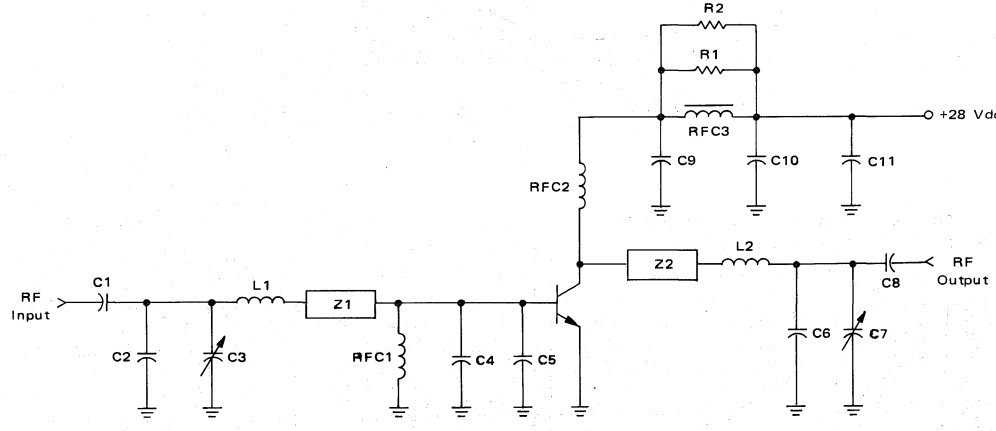
DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	17.02	20.07	0.670	0.790
D	5.46	5.97	0.215	0.235
E	1.78	–	0.070	–
J	0.08	0.18	0.003	0.007
K	12.45	–	0.490	–
L	1.40	1.78	0.055	0.070
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.11	2.54	0.083	0.100
U	2.49	3.35	0.098	0.132

CASE 145A-09

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 40 mAdc, I_B = 0)	$V_{(BR)CEO}$	35	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 40 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	65	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 40 mAdc, I_E = 0)	$V_{(BR)CBO}$	65	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 4.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E - 0)	I_{CBO}	–	–	4.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	–	80	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 30 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	45	60	pF
FUNCTIONAL TESTS (Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 45 W, f = 150 MHz)	G_{PE}	9.0	11	–	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 45 W, f = 150 MHz)	η	50	–	–	%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 45 W, f = 150 MHz, VSWR = 30:1 all phase angles)	No Degradation in Power Output				

FIGURE 1 – 150 MHz TEST CIRCUIT



C1 – 30 pF, 100 mil ATC
C2 – 47 pF, 100 mil ATC
C3, C7 – Johanson #JMC 5501
C4, C5 – 200 pF, 100 mil ATC
C6 – 24 pF, 100 mil ATC
C8 – 27 pF, 100 mil ATC
C9, C10 – 100 pF Underwood
C11 – 1.0 μF Tantalum

L1 – 0.5" #18 Wire
L2 – 2 Turns, 1.5" #20 Wire, ID = 0.15"
Z1, Z2 – Microstrip 0.168" W x 1.25" L
RFC1 – 15 μH Molded Coil
RFC2 – 2 Turns, 2.5" #18 Wire, ID = 0.2"
RFC3 – Ferroxcube VK200–19/4B
R1, R2 – 10 Ω, 1.0 W
Board – Glass Teflon $\epsilon_R \approx 2.55$

TYPICAL PERFORMANCE CURVES

FIGURE 2 – OUTPUT POWER versus INPUT POWER

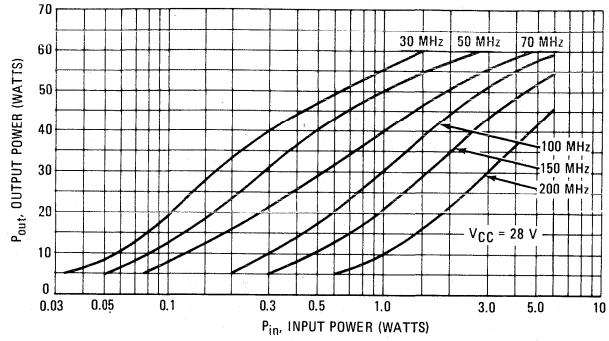


FIGURE 3 – OUTPUT POWER versus INPUT POWER

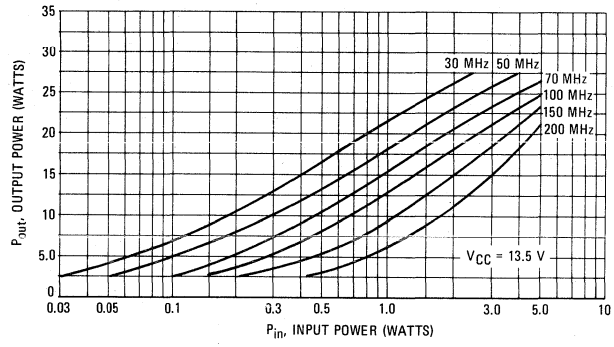


FIGURE 4 – POWER GAIN versus FREQUENCY

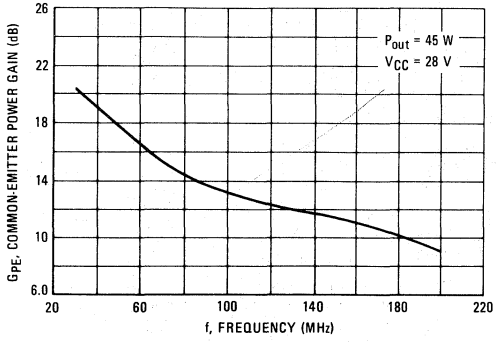


FIGURE 5 – EFFICIENCY versus FREQUENCY

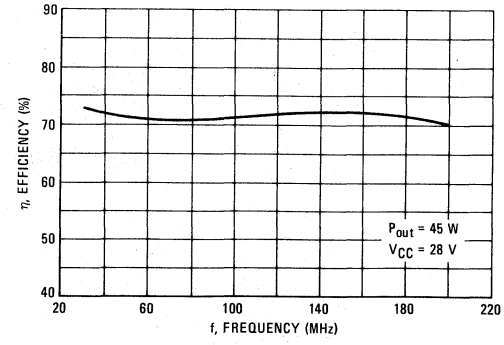
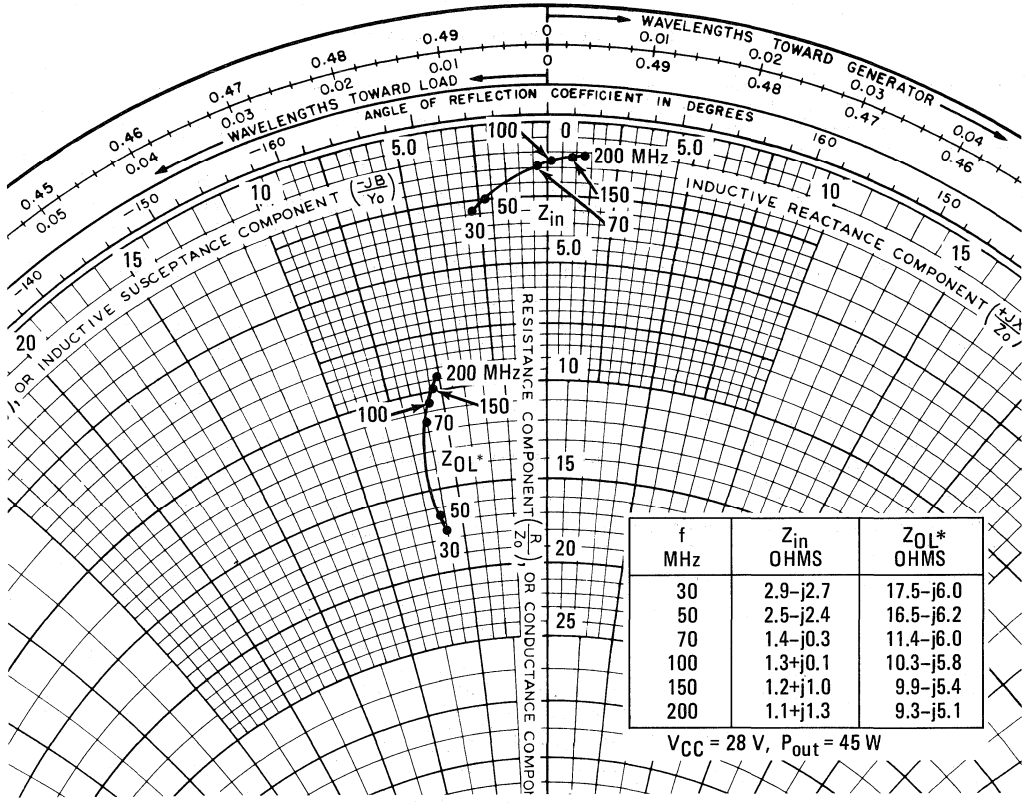
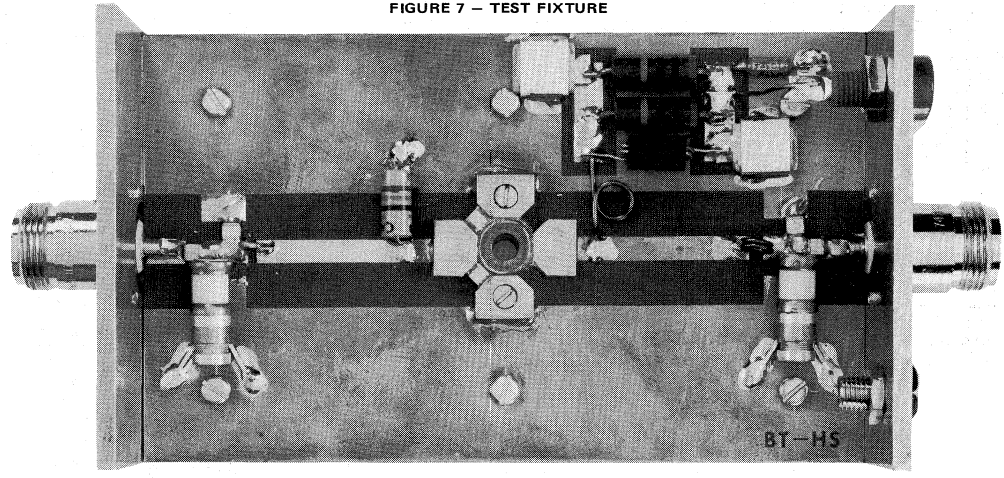


FIGURE 6 – SERIES EQUIVALENT INPUT-OUTPUT IMPEDANCE



*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

FIGURE 7 – TEST FIXTURE



MRF316

The RF Line

80 W — 30-200 MHz

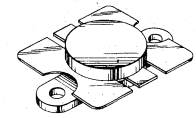
CONTROLLED "Q"
BROADBAND RF POWER
TRANSISTOR

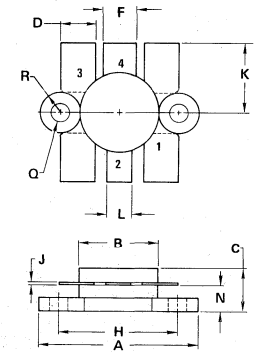
NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed primarily for wideband large-signal output amplifier stages in the 30—200 MHz frequency range.

- Guaranteed Performance at 150 MHz, 28 Vdc
  Output Power = 80 Watts
  Minimum Gain = 10 dB
- Built-In Matching Network for Broadband Operation
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR
- Gold Metallization System for High Reliability Applications





STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. EMITTER
4. BASE
FLANGE-ISOLATED

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	35	Vdc
Collector-Base Voltage	V_{CBO}	65	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous Peak	I_C	9.0 13.5	Adc
Total Device Dissipation @ $T_C = 25^oC$ (1) Derate above 25^oC	P_D	220 1.26	Watts $W/^oC$
Storage Temperature Range	T_{stg}	-65 to +150	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.8	$^oC/W$

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

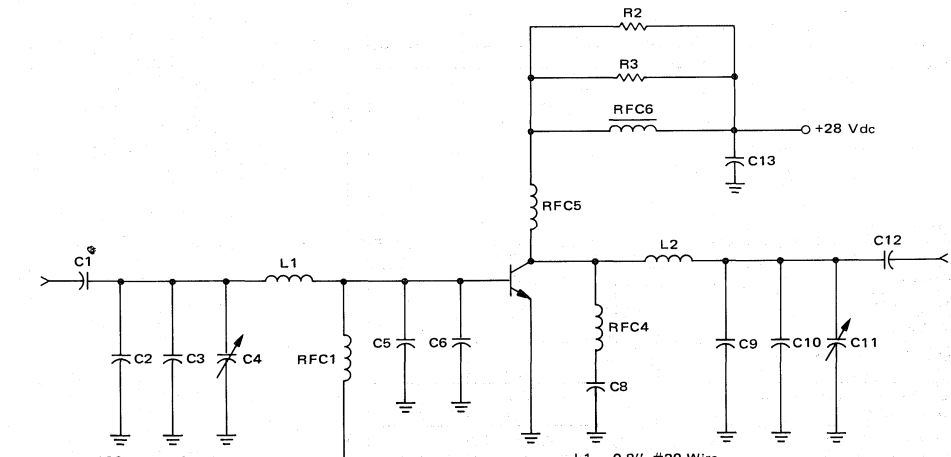
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	12.45	12.95	0.490	0.510
C	5.97	7.62	0.235	0.300
D	5.33	5.59	0.210	0.220
F	5.08	5.33	0.200	0.210
H	18.29	18.54	0.720	0.730
J	0.10	0.15	0.004	0.006
K	10.29	–	0.405	–
L	3.81	4.06	0.150	0.160
N	3.81	4.32	0.150	0.170
Q	2.92	3.30	0.115	0.130
R	3.05	3.30	0.120	0.130

CASE 316-01

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	35	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	65	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 50 mAdc, I_E = 0)	$V_{(BR)CBO}$	65	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	–	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	–	80	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	130	200	pF
NARROW BAND FUNCTIONAL TESTS (Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 80 W, f = 150 MHz)	G_{PE}	10	13	–	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 80 W, f = 150 MHz)	η	55	–	–	%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 80 W CW, f = 150 MHz, VSWR 30:1 all phase angles)	ψ	No Degradation in Power Output			

FIGURE 1 – 150 MHz TEST AMPLIFIER



C1 – 22 pF 100 mil ATC
C2, C3 – 24 pF 100 mil ATC
C4, C11 – 0.8–20 pF JMC #5501 Johanson
C5 – 200 pF 100 mil ATC
C6 – 240 pF 100 mil ATC
C7 – Dipped Mica 1000 pF
C8 – 0.1 μF Erie Red Cap
C9, C10, C12 – 30 pF 100 mil ATC
C13 – 1.0 μF Tantalum

L1 – 0.8", #20 Wire
L2 – 1.0", #20 Wire

RFC1, RFC4 – 0.15 μH Molded Coil
RFC2, RFC3 – Ferroxcube Bead 56-590-65-3B
RFC5 – 2.5", #20 Wire, 1.5 Turns
RFC6 – Ferroxcube VK200 – 19/4B

R1 – 10 Ω, 1/2 W
R2, R3 – 10 Ω, 1 W

TYPICAL PERFORMANCE CURVES

FIGURE 2 – OUTPUT POWER versus INPUT POWER

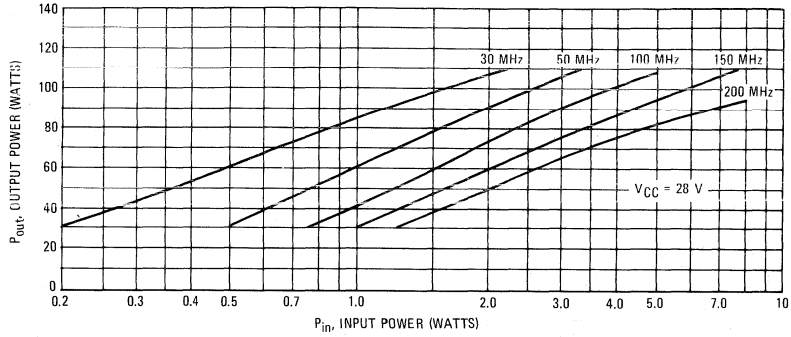


FIGURE 3 – POWER GAIN versus FREQUENCY

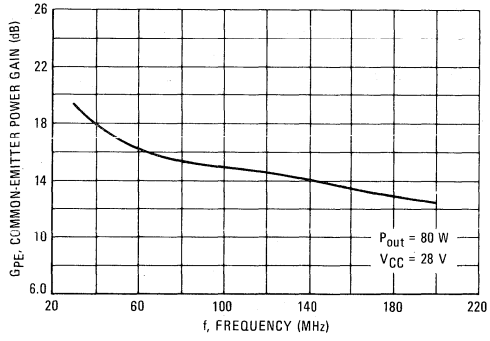


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE
f = 100 MHz

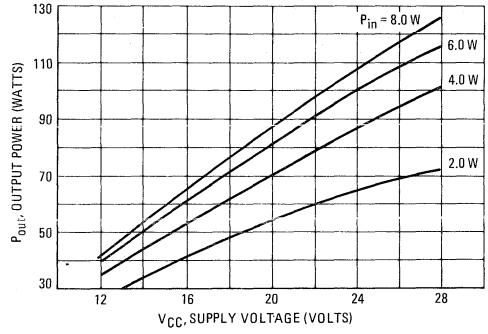


FIGURE 5 – OUTPUT POWER versus SUPPLY VOLTAGE
f = 150 MHz

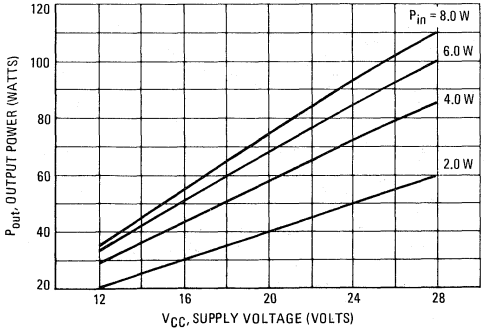


FIGURE 6 – OUTPUT POWER versus SUPPLY VOLTAGE
f = 200 MHz

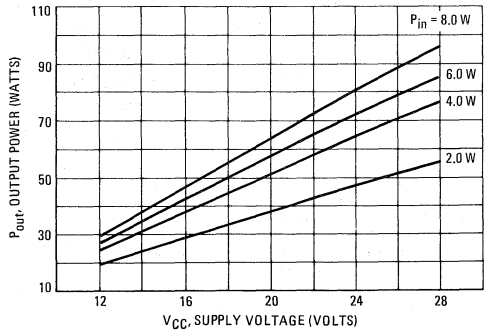
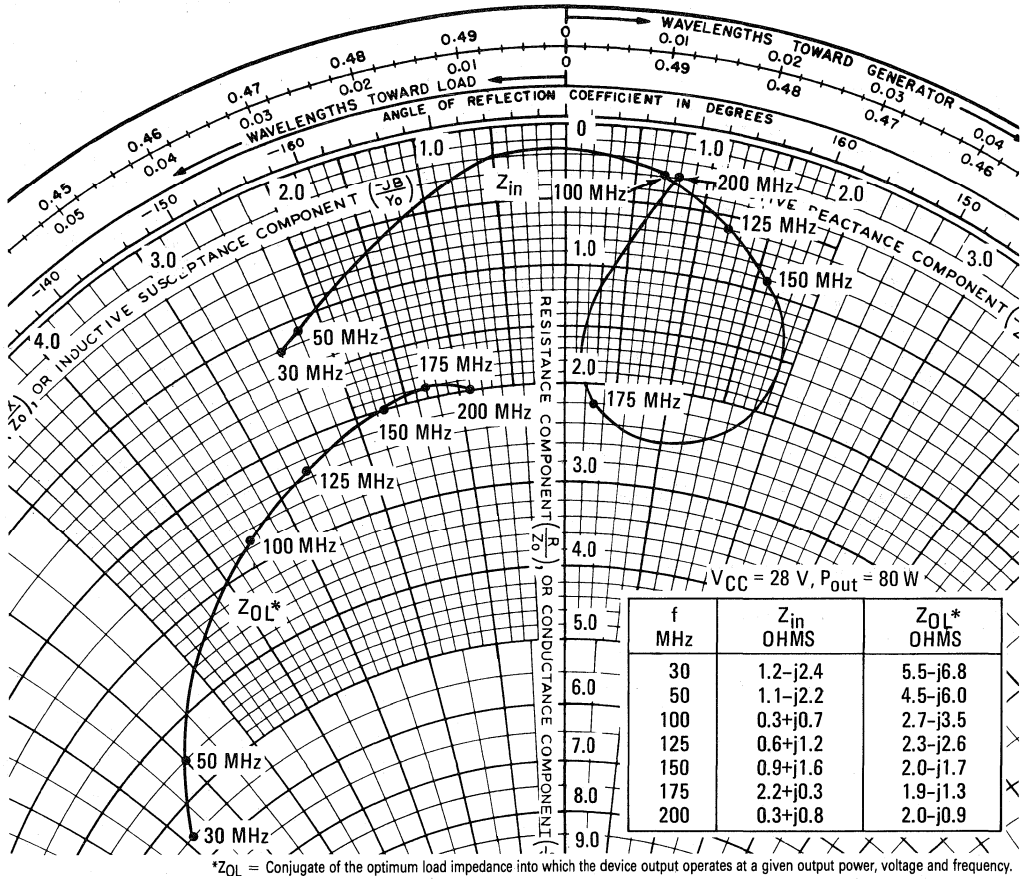


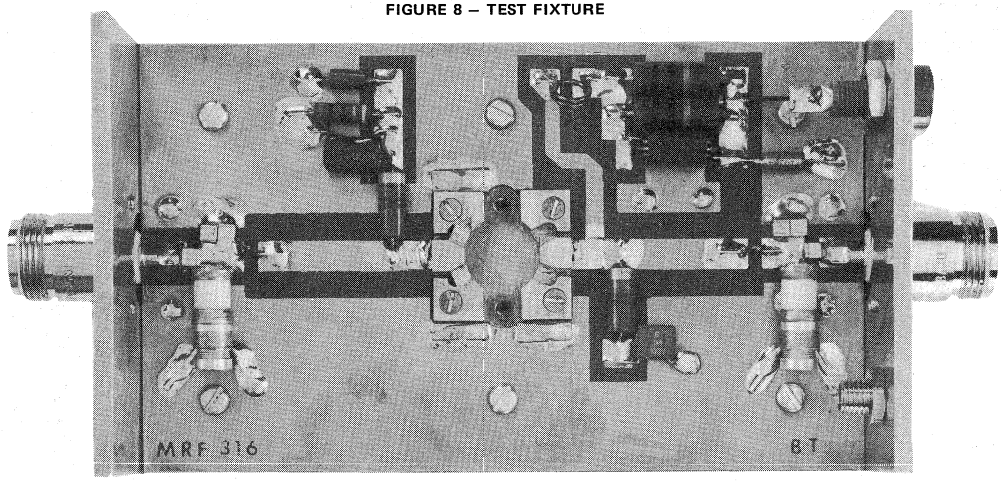
FIGURE 7 – SERIES EQUIVALENT INPUT-OUTPUT IMPEDANCE



f MHz	Z_{in} OHMS	Z_{OL}* OHMS
30	1.2–j2.4	5.5–j6.8
50	1.1–j2.2	4.5–j6.0
100	0.3+j0.7	2.7–j3.5
125	0.6+j1.2	2.3–j2.6
150	0.9+j1.6	2.0–j1.7
175	2.2+j0.3	1.9–j1.3
200	0.3+j0.8	2.0–j0.9

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

FIGURE 8 – TEST FIXTURE



MRF317

The RF Line

100 W – 30 – 200 MHz

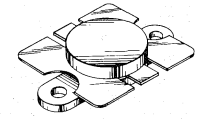
CONTROLLED Q
BROADBAND RF POWER
TRANSISTOR

NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed primarily for wideband large signal output amplifier stages in 30 – 200 MHz frequency range.

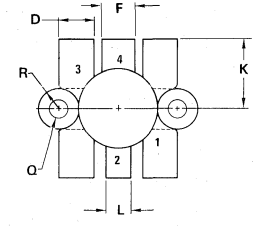
- Guaranteed Performance at 150 MHz and 28 Vdc
  Output Power = 100 W
  Minimum Gain = 9 dB
- Built-In Matching Network for Broadband Operation
- 100% Tested for Load Mismatch at All Phase Angles with 30:1 VSWR
- Gold Metallization System for High Reliability
- High Output Saturation Power – Ideally Suited for 30 W Carrier/ 120 W Peak AM Amplifier Service
- Guaranteed Performance in Broadband Test Fixture



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	35	Vdc
Collector-Base Voltage	V_{CBO}	65	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current – Continuous – Peak (10 seconds)	I_C	12 18	Adc
Total Device Dissipation @ $T_C = 25^oC$ (1) Derate Above 25^oC	P_D	270 1.54	Watts $W/^oC$
Storage Temperature Range	T_{stg}	-65 to +150	^oC
THERMAL CHARACTERISTICS			
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.65	$^oC/W$

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF Amplifiers.



STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. EMITTER
4. BASE
FLANGE-ISOLATED

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	12.45	12.95	0.490	0.510
C	5.97	7.62	0.235	0.300
D	5.33	5.59	0.210	0.220
F	5.08	5.33	0.200	0.210
H	18.29	18.54	0.720	0.730
J	0.10	0.15	0.004	0.006
K	10.29	–	0.405	–
L	3.81	4.06	0.150	0.160
N	3.81	4.32	0.150	0.170
Q	2.92	3.30	0.115	0.130
R	3.05	3.30	0.120	0.130

CASE 316-01

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, I_B = 0)	$V_{(BR)CEO}$	35	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	65	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 mAdc, I_E = 0)	$V_{(BR)CBO}$	65	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	–	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	25	80	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	200	250	pF
FUNCTIONAL TESTS (FIGURE 2)					
Common-Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 100 W, f = 150 MHz , I_C(Max) = 6.5 Adc)	G_{PE}	9.0	10	–	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 100 W, f = 150 MHz , I_C(Max) = 6.5 Adc)	η	55	60	–	%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 100 W CW, f = 150 MHz, VSWR = 30:1 all phase angles)	ψ	No Degradation in Output Power			

FIGURE 1 – BROADBAND (110-160 MHz) TEST FIXTURE

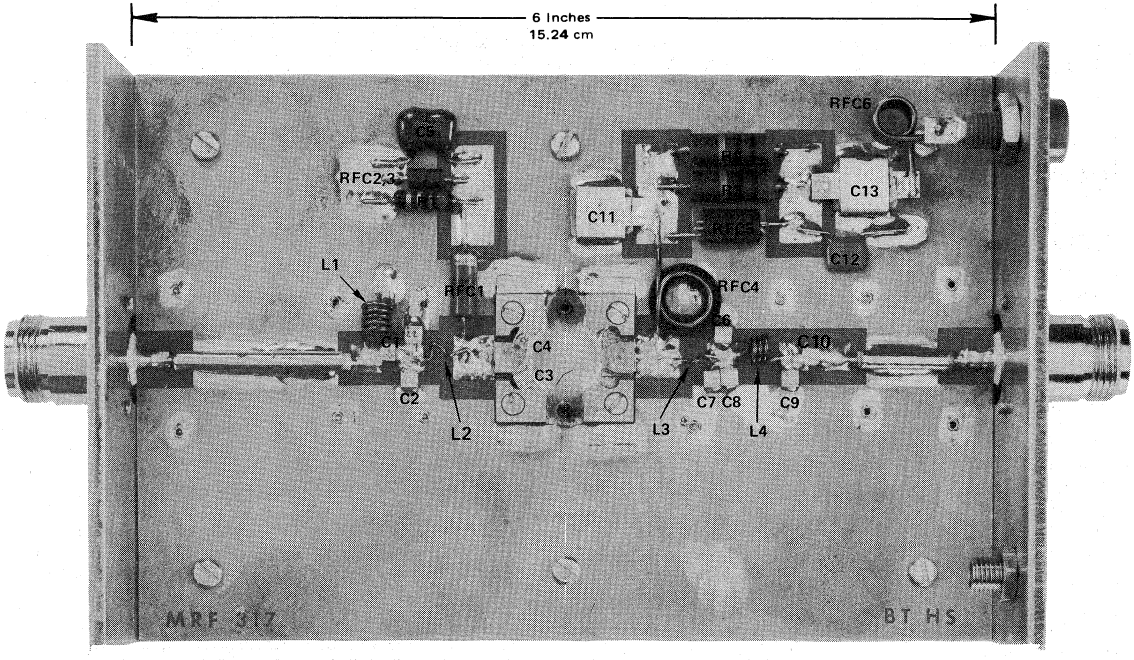
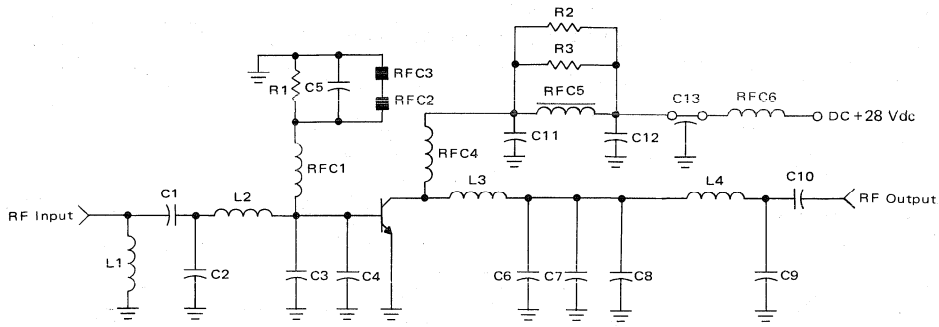


FIGURE 2 – 110-160 MHz BROADBAND AMPLIFIER – TEST FIXTURE



C1, C9 – 39 pF, 100 mil ATC
C2 – 120 pF, 100 mil ATC
C3, C4 – 360 pF, 100 mil ATC
C5 – 1000 pF Dipped Mica
C6, C7 – 100 pF, 100 mil ATC*
C8 – 18 pF, 100 mil ATC*
C10 – 43 pF, 100 mil ATC
C11 – 60 pF, Underwood
C12 – 0.1 μF Erie Redcap
C13 – 1000 pF, Underwood J102

L1 – 50 nH
L2 – 6.0 nH
L3 – 8.0 nH
L4 – 32 nH
RFC1 – 0.15 μH Molded Coil
RFC2, RFC3 – Ferroxcube Bead 56-590-65/3B
RFC4 – 1 Turn, #18 Wire, 2.0" L
RFC5 – Ferroxcube VK200 19/4B
RFC6 – 7 Turns, #18 Wire, 0.3" ID
R1 – 10 Ω 1/2 W
R2, R3 – 10 Ω 1 W
*Combination of C6, C7, C8 equals 220 pF.

3

FIGURE 3 – POWER GAIN versus FREQUENCY BROADBAND TEST FIXTURE

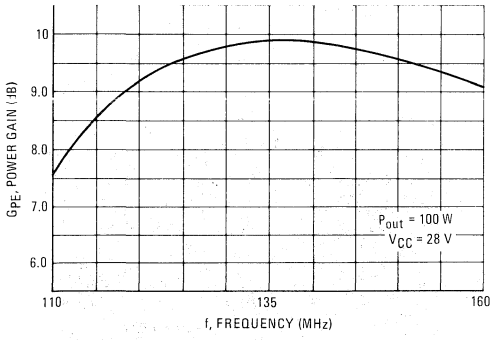
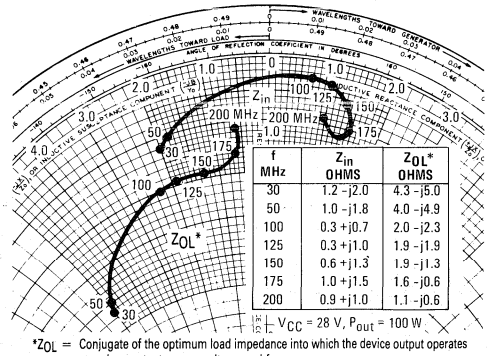


FIGURE 4 – SERIES EQUIVALENT INPUT-OUTPUT IMPEDANCE



f MHz	Z_{in} OHMS	Z_{OL}^* OHMS
30	1.2 -j2.0	4.3 -j5.0
50	1.0 -j1.8	4.0 -j4.9
100	0.3 +j0.7	2.0 -j2.3
125	0.3 +j1.0	1.9 -j1.9
150	0.6 +j1.3	1.9 -j1.3
175	1.0 +j1.5	1.6 -j0.6
200	0.9 +j1.0	1.1 -j0.6

V_{CC} = 28 V, P_{out} = 100 W

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

FIGURE 5 – EFFICIENCY versus FREQUENCY BROADBAND TEST FIXTURE

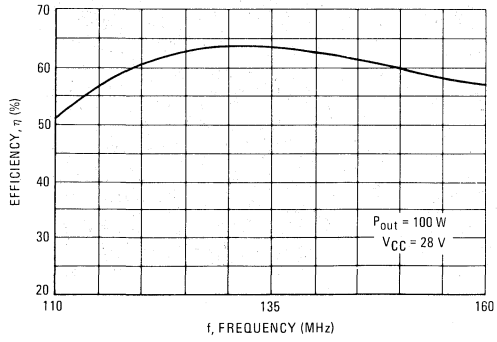
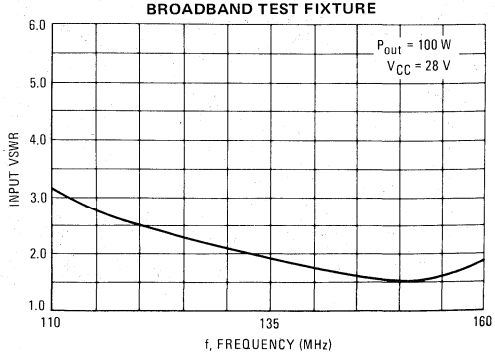


FIGURE 6 – INPUT VSWR versus FREQUENCY BROADBAND TEST FIXTURE



TYPICAL PERFORMANCE CURVES

FIGURE 7 – OUTPUT POWER versus INPUT POWER

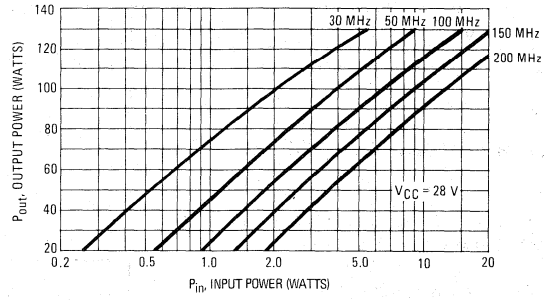


FIGURE 8 – POWER GAIN versus FREQUENCY

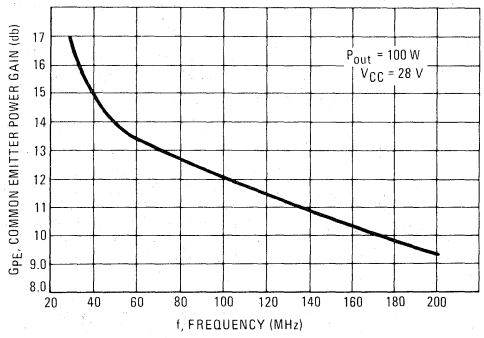


FIGURE 9 – POWER OUTPUT versus SUPPLY VOLTAGE
f = 100 MHz

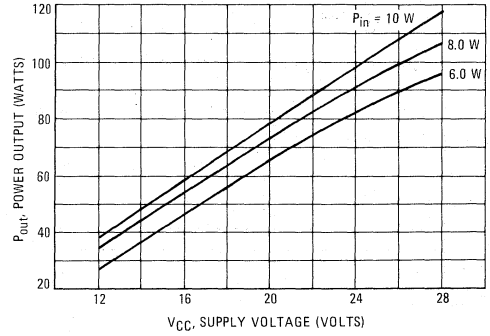


FIGURE 10 – POWER OUTPUT versus SUPPLY VOLTAGE
f = 150 MHz

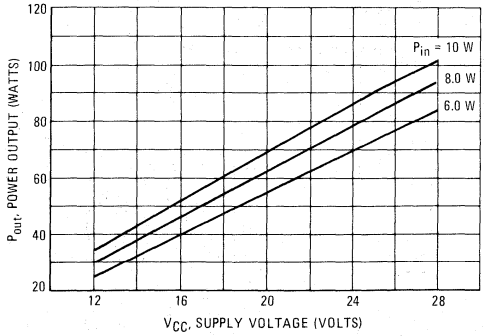
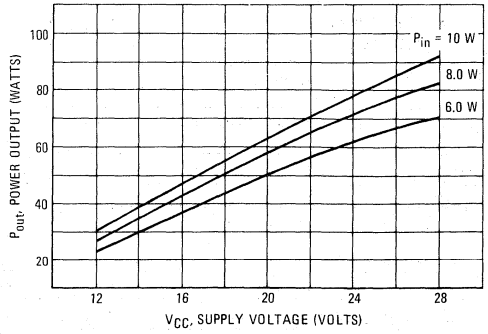


FIGURE 11 – POWER OUTPUT versus SUPPLY VOLTAGE
f = 200 MHz



3

MRF321

The RF Line

10 W — 400 MHz

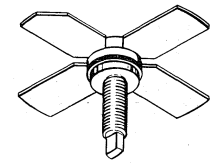
RF POWER TRANSISTOR

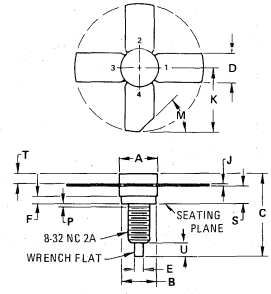
NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed primarily for wideband large-signal driver and predriver amplifier stages in the 200–500 MHz frequency range.

- Guaranteed Performance at 400 MHz and 28 Vdc
  Output Power = 10 Watts
  Minimum Gain = 12 dB
  Efficiency = 50%
- 100% Tested for Load Mismatch at All Phase Angles with 30:1 VSWR
- Gold Metallization System for High Reliability
- Computer-Controlled Wirebonding Gives Consistent Input Impedance





STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.06	7.26	0.278	0.286
B	6.20	6.50	0.244	0.256
C	14.99	16.51	0.590	0.650
D	5.46	5.97	0.215	0.235
E	1.40	1.65	0.055	0.065
F	1.52	–	0.060	–
J	0.08	0.18	0.003	0.007
K	11.05	–	0.435	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
S	3.00	3.25	0.118	0.128
T	1.40	1.78	0.055	0.070
U	2.92	3.68	0.115	0.145

CASE 244-04

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	33	Vdc
Collector-Base Voltage	V_{CBO}	60	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous — Peak	I_C	1.1 1.5	Adc
Total Device Dissipation @ $T_A = 25^oC$ (1) Derate above 25^oC	P_D	27 160	Watts $mW/^oC$
Storage Temperature Range	T_{stg}	−65 to +150	^oC

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

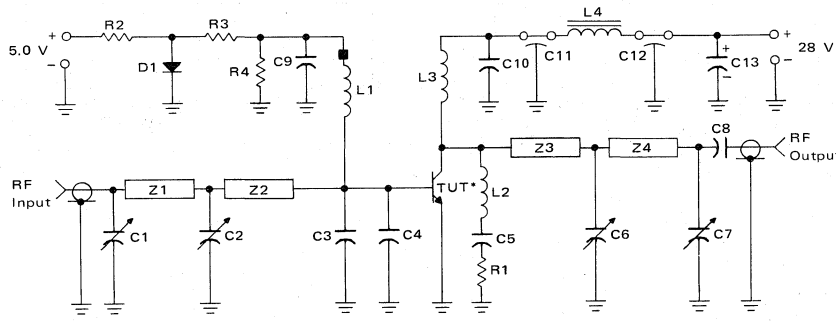
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.4	$^oC/W$

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	33	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 20 mAdc, I_E = 0)	$V_{(BR)CBO}$	60	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 2.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 500 mA, V_{CE} = 5.0 Vdc)	h_{FE}	20	–	80	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	10	12	pF
FUNCTIONAL TESTS (FIGURE 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 10 W, f = 400 MHz)	G_{PE}	12	13	–	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 10 W, f = 400 MHz)	η	50	60	–	%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 10, f = 400 MHz, VSWR = 30:1 all phase angles)	ψ	No Degradation in Output Power			

FIGURE 1 – 400 MHz TEST CIRCUIT



C1, C2, C3 – 1.0–20 pF Johanson Trimmer (JMC 5501)
C3, C4 – 47 pF ATC Chip Capacitor
C5, C10 – 0.1 μF Erie Redcap
C7 – 0.5–10 pF Johanson Trimmer (JMC 5201)
C8 – 0.018 μF Vitramon Chip Capacitor
C9 – 200 pF UNELCO Capacitor
C11, C12 – 680 pF Feedthru
C13 – 1 μF, 50 Volt Tantalum Capacitor

R1 – 5.1 Ω, 1/4 Watt
R2 – 120 Ω, 1 Watt
R3 – 20 Ω, 1/2 Watt
R4 – 47 Ω, 1/2 Watt

L1 – 0.33 μH Molded Choke with Ferroxcube Bead (Ferroxcube 56-590-65/4B) on Ground End of Coil
L2 – 4 Turns #20 Enamel, 1/8" ID
L3 – 6 Turns #20 Enamel, 1/4" ID
L4 – Ferroxcube VK200-19/4B

Z1 – Microstrip 0.1" W x 1.35" L
Z2 – Microstrip 0.1" W x 0.55" L
Z3 – Microstrip 0.1" W x 0.8" L
Z4 – Microstrip 0.1" W x 1.75" L

D1 – 1N4001

Board – Glass Teflon, ϵ_R = 2.56, t = 0.062"

Input/Output Connectors – Type N

*Transistor Under Test

FIGURE 2 – OUTPUT POWER versus FREQUENCY

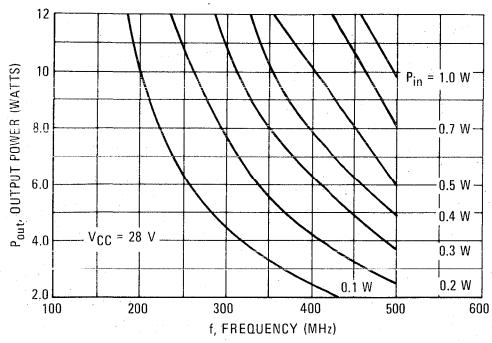


FIGURE 3 – OUTPUT POWER versus INPUT POWER

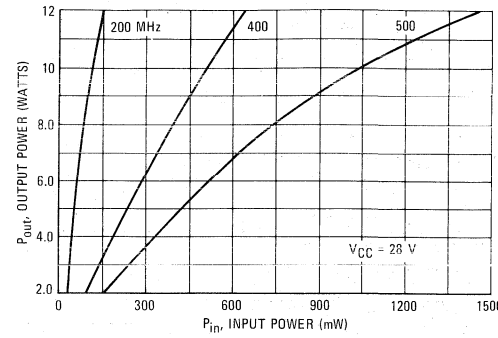


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

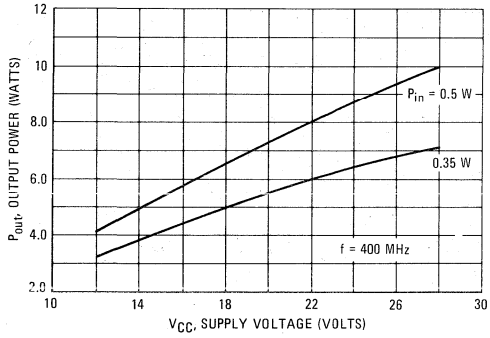


FIGURE 5 – POWER GAIN versus FREQUENCY

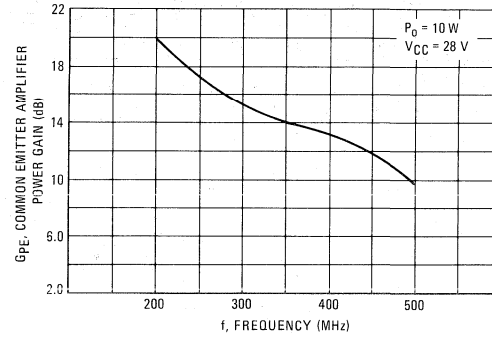
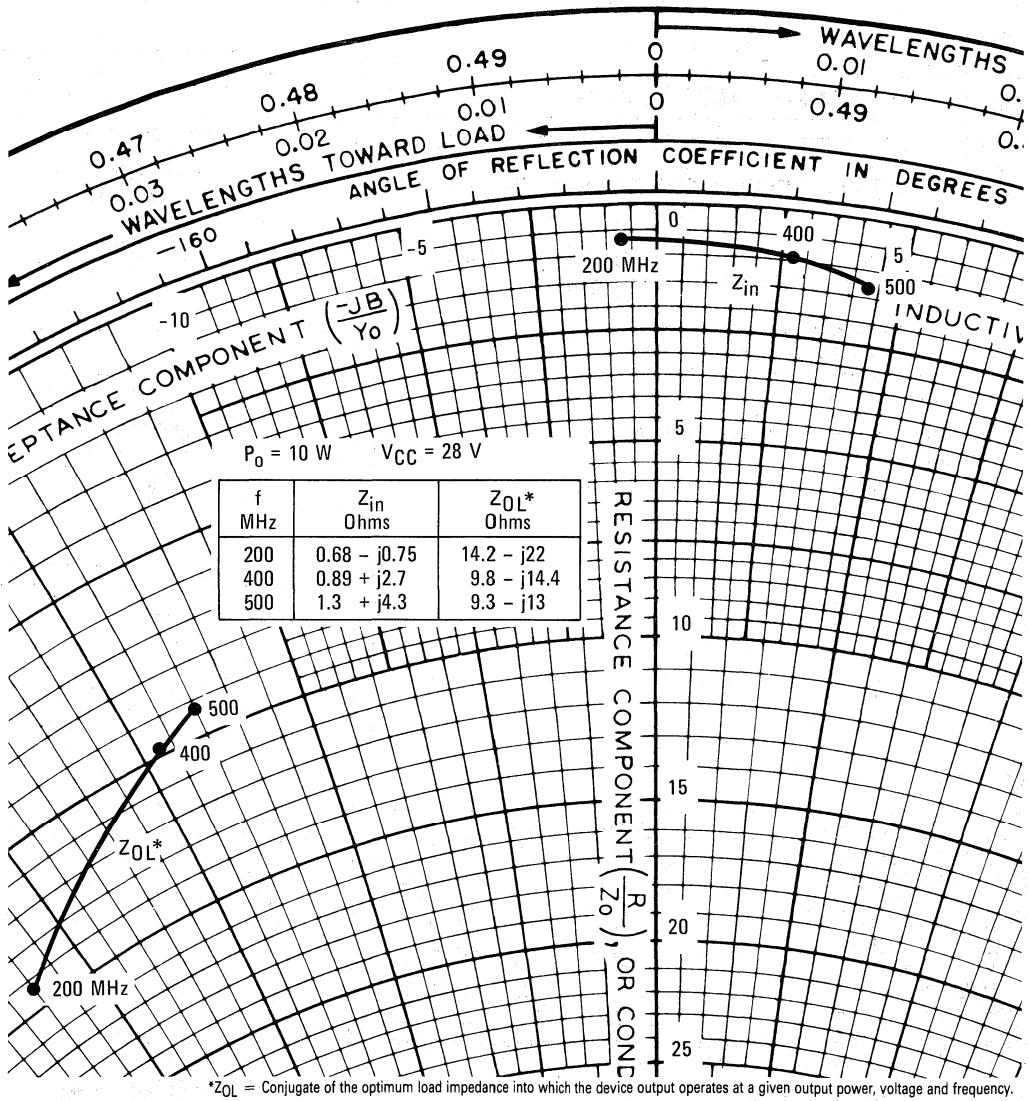


FIGURE 6 – SERIES EQUIVALENT IMPEDANCE



f MHz	Z_{in} Ohms	Z_{OL}* Ohms
200	0.68 – j0.75	14.2 – j22
400	0.89 + j2.7	9.8 – j14.4
500	1.3 + j4.3	9.3 – j13

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

3

MRF323

The RF Line

NPN SILICON RF POWER TRANSISTOR

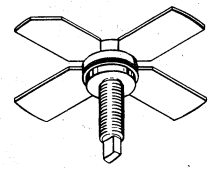
. . . designed primarily for wideband large-signal driver and predriver amplifier stages in the 200-500 MHz frequency range.

- Guaranteed Performance at 400 MHz and 28 V
  Output Power = 20 Watts
  Minimum Gain = 10 dB
  Efficiency = 50%
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR
- Gold Metallization System for High Reliability
- Computer-Controlled Wirebonding Gives Consistent Input Impedance

20 W – 400 MHz

RF POWER TRANSISTOR

NPN SILICON



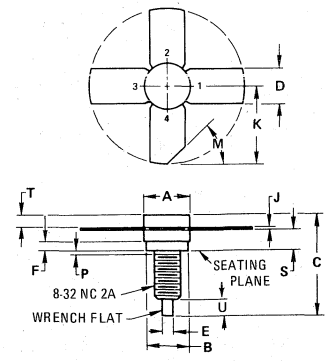
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	33	Vdc
Collector-Base Voltage	V_{CBO}	60	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous — Peak	I_C	2.2 3.0	Adc
Total Device Dissipation @ $T_C = 25^oC$ (1) Derate above 25^oC	P_D	55 310	Watts mW/^{o}C
Storage Temperature Range	T_{stg}	−65 to +150	^{o}C

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.2	^{o}C/W



STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

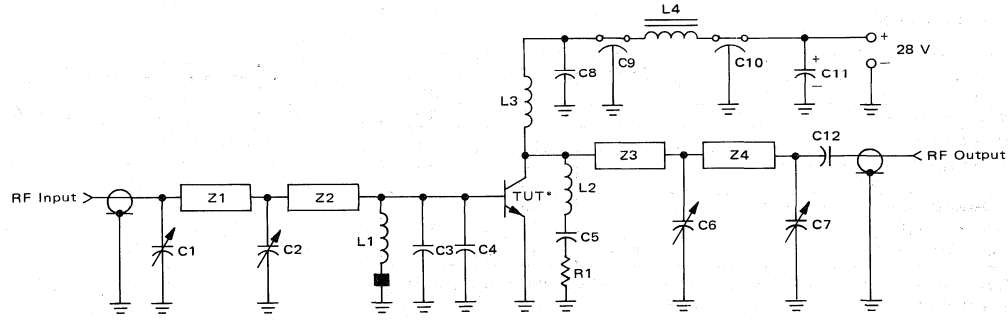
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.06	7.26	0.278	0.286
B	6.20	6.50	0.244	0.256
C	14.99	16.51	0.590	0.650
D	5.46	5.97	0.215	0.235
E	1.40	1.65	0.055	0.065
F	1.52	–	0.060	–
J	0.08	0.18	0.003	0.007
K	11.05	–	0.435	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
S	3.00	3.25	0.118	0.128
T	1.40	1.78	0.055	0.070
U	2.92	3.68	0.115	0.145

CASE 244-04

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	33	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 20 mAdc, I_E = 0)	$V_{(BR)CBO}$	60	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 2.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	–	80	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	20	24	pF
FUNCTIONAL TESTS (Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 20 W, f = 400 MHz)	G_{PE}	10	11	–	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 20 W, f = 400 MHz)	η	50	60	–	%
Load Mismatch (V_{CC} = 28 V, P_{out} = 20 W, f = 400 MHz, VSWR = 30:1 all phase angles)	ψ	No Degradation in Output Power			

FIGURE 1 – 400 MHz TEST CIRCUIT



C1, C2, C6 – 1.0-20 pF Johanson Trimmer (JMC 5501)
C3, C4 – 47 pF ATC Chip Capacitor
C5, C8 – 0.1 μF Erie Redcap
C7 – 0.5-10 pF Johanson Trimmer (JMC 5201)
C9, C10 – 680 pF Feedthru
C11 – 1.0 μF 50 Volt Tantalum
C12 – 0.018 μF Vitramon Chip Capacitor
R1 – 5.1 Ω 1/4 Watt
L1 – 0.33 μH Molded Choke with Ferroxcube Bead (Ferroxcube 56-590-65/4B) on Ground End
L2 – 6 Turns #20 Enamel, ¼" ID, Closewound
L3 – 4 Turns #20 Enamel, 1/8" ID, Closewound
L4 – Ferroxcube VK200 – 19/4B
Z1 – Microstrip 0.1" W x 1.35" L
Z2 – Microstrip 0.1" W x 0.55" L
Z3 – Microstrip 0.1" W x 0.8" L
Z4 – Microstrip 0.1" W x 1.75" L
Board – Glass Teflon $\in_R$ = 2.56 t = 0.062"
Input/Output Connectors – Type N
*Transistor Under Test

3

FIGURE 2 – OUTPUT POWER versus FREQUENCY

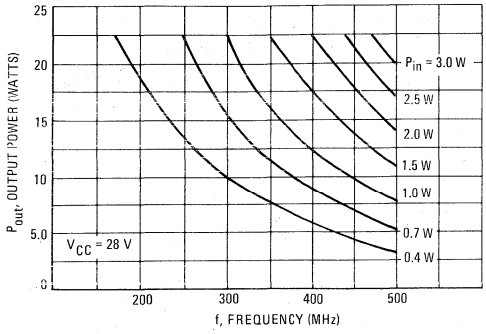


FIGURE 3 – OUTPUT POWER versus INPUT POWER

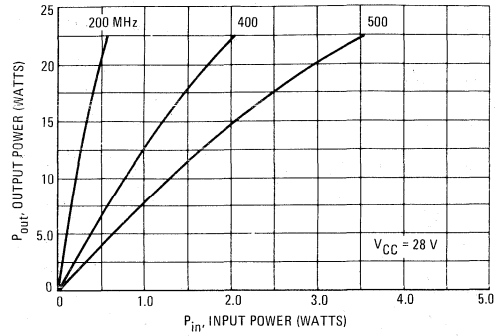


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

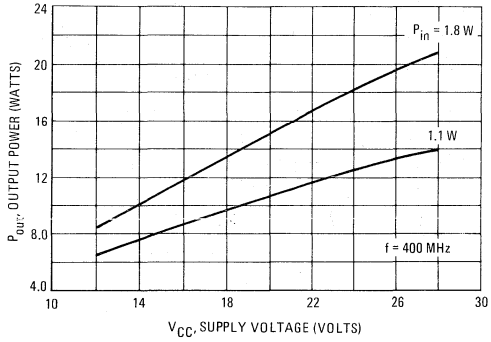
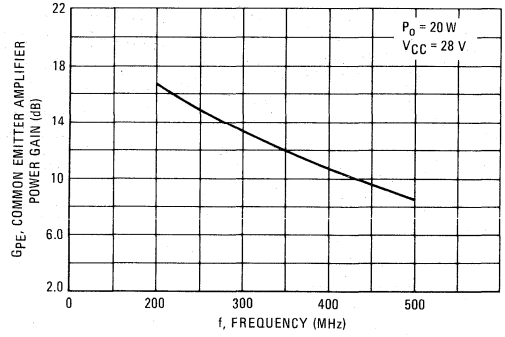
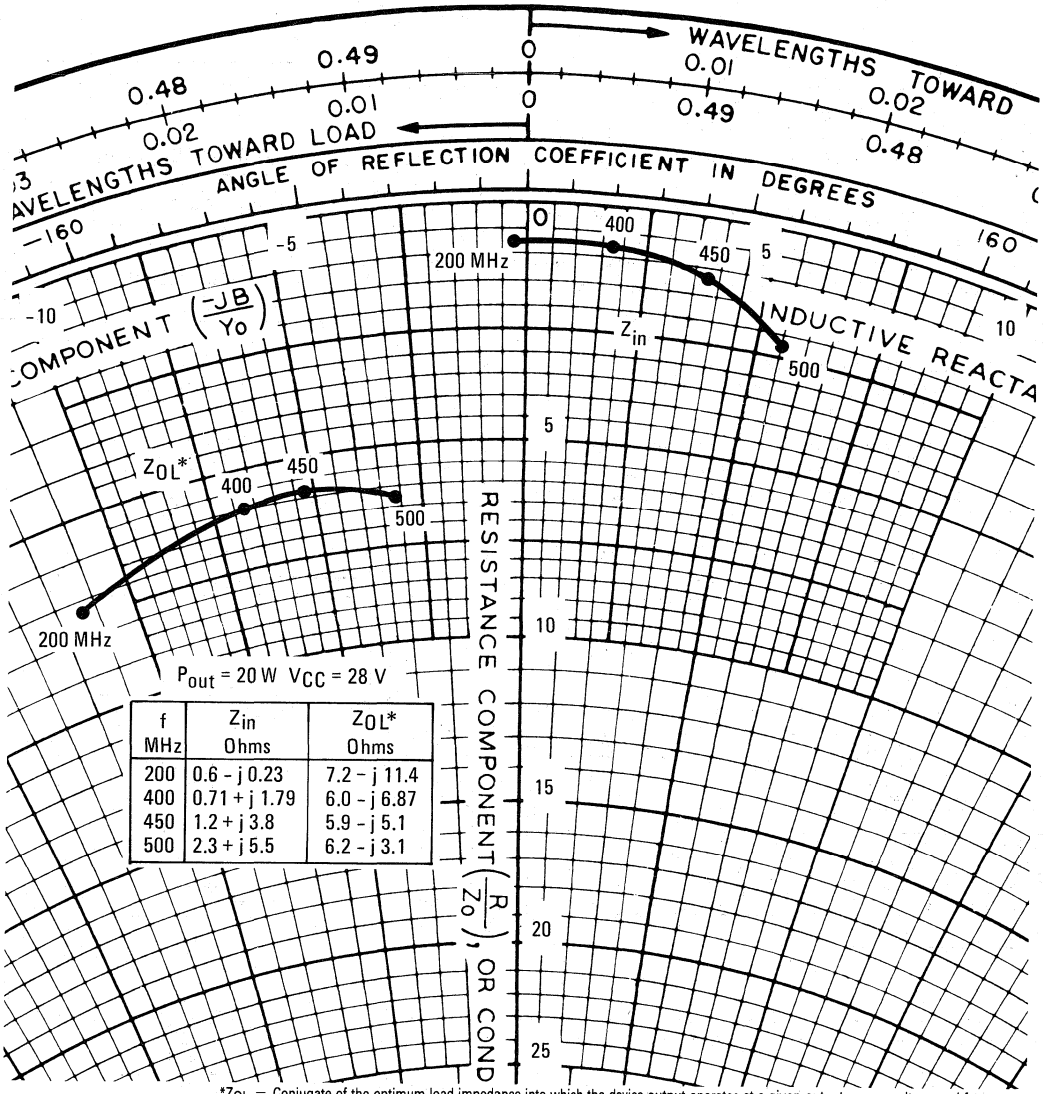


FIGURE 5 – POWER GAIN versus FREQUENCY



3

FIGURE 6 – SERIES EQUIVALENT IMPEDANCE



f MHz	Z_{in} Ohms	Z_{OL}* Ohms
200	0.6 - j 0.23	7.2 - j 11.4
400	0.71 + j 1.79	6.0 - j 6.87
450	1.2 + j 3.8	5.9 - j 5.1
500	2.3 + j 5.5	6.2 - j 3.1

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

MRF325

The RF Line

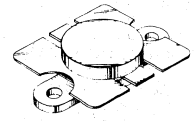
NPN SILICON RF POWER TRANSISTOR

. . . designed primarily for wideband large-signal output and driver amplifier stages in the 100-500 MHz frequency range.

- Specified 28 Volt, 400 MHz Characteristics —
  Output Power = 30 Watts
  Minimum Gain = 8.5 dB
  Efficiency = 54% (Min)
- Built-In Matching Network for Broadband Operation Using Internal Matching Techniques
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR
- Gold Metallization for High Reliability Applications

30 W — 225-400 MHz
CONTROLLED "Q"
BROADBAND RF POWER
TRANSISTOR

NPN SILICON



3

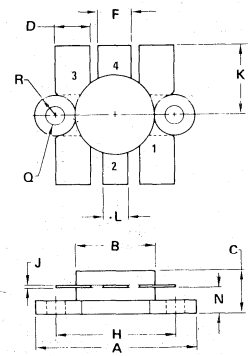
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	33	Vdc
Collector-Base Voltage	V_{CBO}	60	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous — Peak	I_C	3.4 4.5	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	82 0.47	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.13	°C/W

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.



STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. EMITTER
4. BASE
FLANGE-ISOLATED

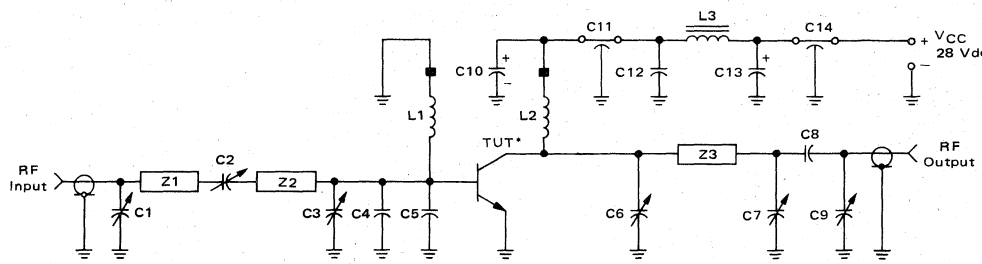
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	12.45	12.95	0.490	0.510
C	5.97	7.62	0.235	0.300
D	5.33	5.59	0.210	0.220
F	5.08	5.33	0.200	0.210
H	18.29	18.54	0.720	0.730
J	0.10	0.15	0.004	0.006
K	10.29	—	0.405	—
L	3.81	4.06	0.150	0.160
N	3.81	4.32	0.150	0.170
Q	2.92	3.30	0.115	0.130
R	3.05	3.30	0.120	0.130

CASE 316-01

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 30 mAdc, I_B = 0)	$V_{(BR)CEO}$	33	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 30 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 3.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 30 mAdc, I_E = 0)	$V_{(BR)CBO}$	60	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	–	3.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.5 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	–	80	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	30	40	pF
FUNCTIONAL TESTS (Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 30 W, f = 400 MHz)	G_{PE}	8.5	9.5	–	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 30 W, f = 400 MHz)	η	50	60	–	%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 30 W, f = 400 MHz, VSWR = 30:1 all angles)	ψ	No Degradation in Output Power			

FIGURE 1 – 400 MHz TEST CIRCUIT



C1, C9 – 1.0–10 pF Johanson Capacitor (JMC 5201)
C2, C3, C6, C7 – 1.0–20 pF Johanson Capacitor (JMC 5501)
C4, C5 – 36 pF ATC 100-mil Chip Capacitor
C8 – 100 pF UNELCO
C10, C13 – 1.0 μF 50 V Tantalum
C11, C14 – 680 pF Feedthru
C12 – 0.1 μF Erie Redcap
L1 – 8 Turns #26 AWG Enameled, 1/16" ID Closewound with Ferroxcube Bead (#56-590-65/4B) on Ground End
L2 – 14 Turns, #22 AWG Enameled, Closewound on a 470 Ω, 2 Watt Resistor with Ferroxcube Bead (#56-590-65/4B) on Cold End of L2
L3 – Ferroxcube VK200-19/4B Ferrite Choke
Z1 – Microstrip 0.19" W x 0.88" L
Z2 – Microstrip 0.28" W x 1.0" L
Z3 – Microstrip 0.31" W x 1.25" L
Board – Glass Teflon ∈R = 2.56, t = 0.062"
Input/Output Connectors – Type N

TUT Socket Lead Frame Etched from 80-mil-Thick Copper
*Transistor Under Test

FIGURE 2 – OUTPUT POWER versus INPUT POWER

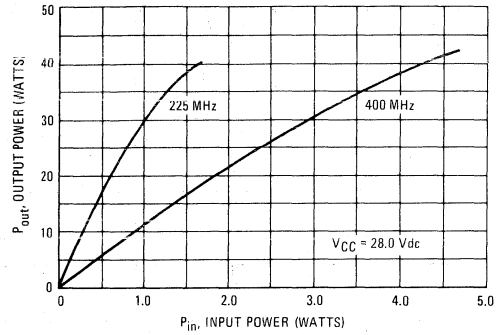


FIGURE 3 – OUTPUT POWER versus SUPPLY VOLTAGE – 225 MHz

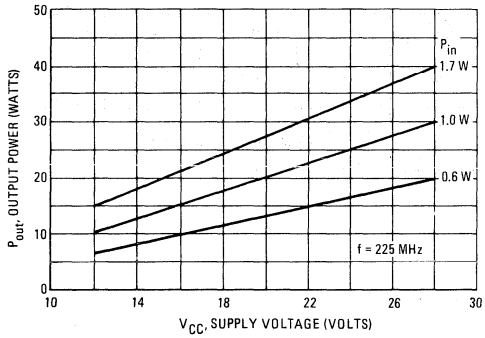


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE – 400 MHz

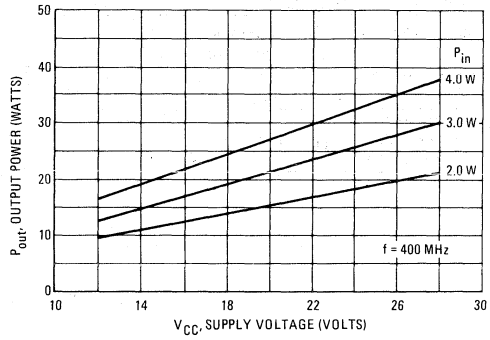
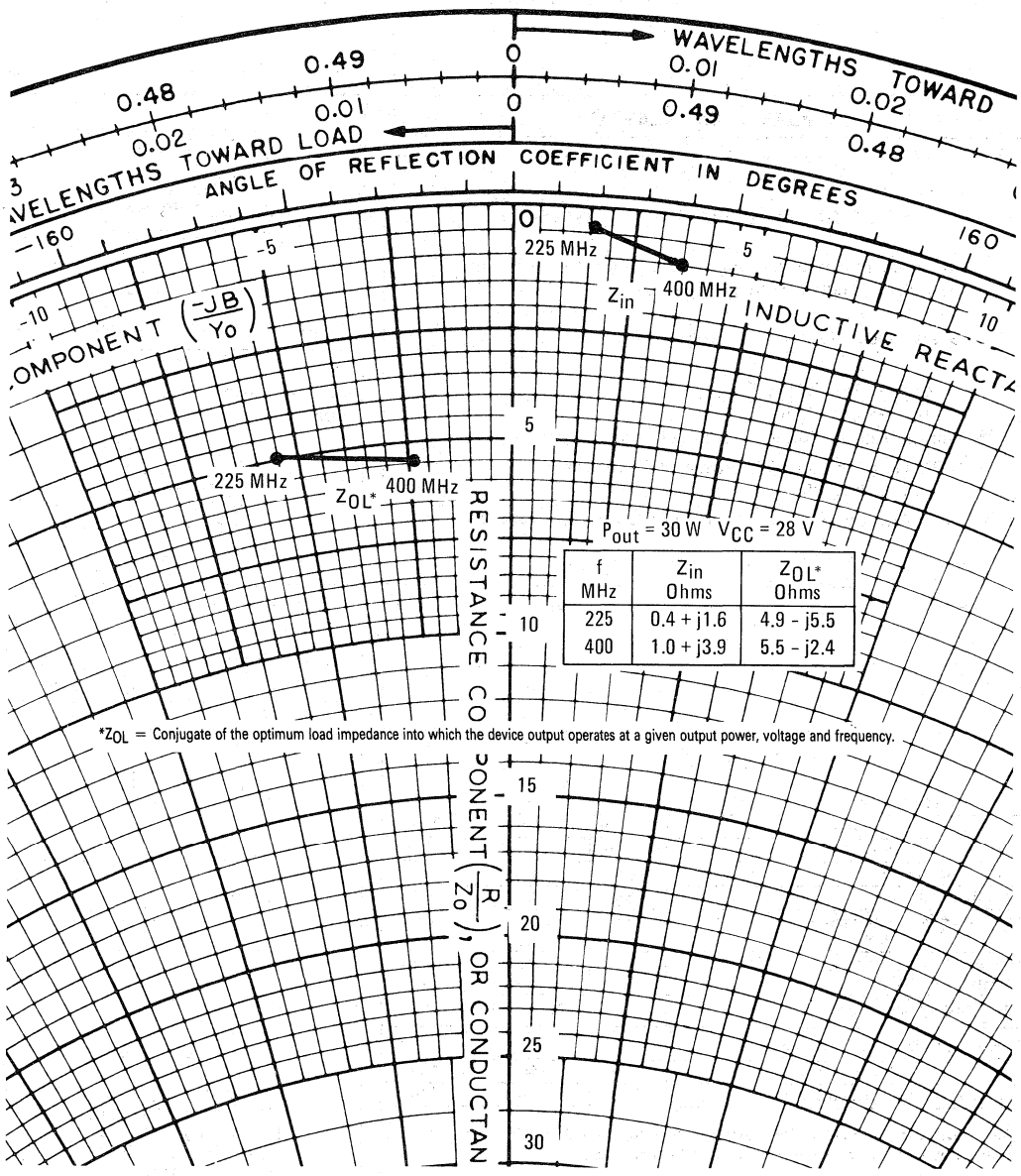


FIGURE 5 – SERIES EQUIVALENT IMPEDANCE



MRF326

The RF Line

40 W – 225–400 MHz

CONTROLLED "Q"
BROADBAND RF POWER
TRANSISTOR

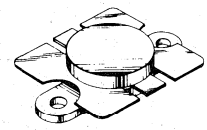
NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed primarily for wideband large-signal output amplifier stages in the 100-500 MHz frequency range.

- Guaranteed Performance @ 400 MHz, 28 Vdc

  Output Power = 40 Watts
  Minimum Gain = 9.0 dB
- Built-In Matching Network for Broadband Operation
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR
- Gold Metallization System for High Reliability Applications



3

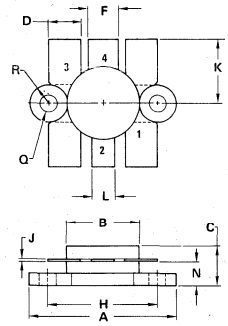
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	33	Vdc
Collector-Base Voltage	V_{CBO}	60	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous Peak	I_C	4.5 6.0	Adc
Total Device Dissipation @ $T_C = 25^oC$ (1) Derate above 25^oC	P_D	110 0.63	Watts $W/^oC$
Storage Temperature Range	T_{stg}	−65 to +150	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.6	$^oC/W$

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.



STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. EMITTER
4. BASE
FLANGE-ISOLATED

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	12.45	12.95	0.490	0.510
C	5.97	7.62	0.235	0.300
D	5.33	5.59	0.210	0.220
F	5.08	5.33	0.200	0.210
H	18.29	18.54	0.720	0.730
J	0.10	0.15	0.004	0.006
K	10.29	–	0.405	–
L	3.81	4.06	0.150	0.160
N	3.81	4.32	0.150	0.170
Q	2.92	3.30	0.115	0.130
R	3.05	3.30	0.120	0.130

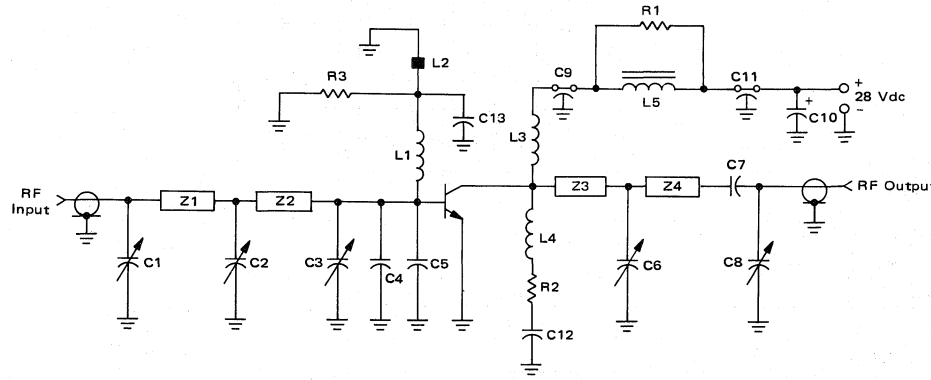
CASE 316-01

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 40 mAdc, I_B = 0)	$V_{(BR)CEO}$	33	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 40 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 4.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 40 mAdc, I_E = 0)	$V_{(BR)CBO}$	60	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	–	4.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	50	80	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	45	60	pF
FUNCTIONAL TESTS (Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 40 W, f = 400 MHz, I_C Max = 2.85 Adc)	G_{PE}	9.0	11	–	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 40 W, f = 400 MHz, I_C Max = 2.85 Adc)	η	50	–	–	%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 40 W CW, f = 400 MHz, VSWR = 30:1 all phase angles)	Ψ	No Degradation in Power Output			

3

FIGURE 1 – 400 MHz TEST AMPLIFIER



C1 – 1.0-10 pF Johanson, Capacitor (JMC 5201)
C2, C3, C6, C8 – 1.0-20 pF Johanson Capacitor
C4, C5 – 36 pF ATC "B" Style Chip Capacitor
C7, C9, C13 – 100 pF UNELCO Capacitor
C11 – 680 pF Feedthru
C10 – 1.0 μF 50 V Tantalum
C12 – 0.1 μF Erie Redcap
L1 – 8 Turns #26 AWG Enameled, 1/16" ID Closewound
L2, L5 – Ferroxcube VK200-19/4B Ferrite Choke
L3 – 8 Turns #20 AWG Enameled, 1/4" ID Closewound
L4 – 4 Turns #26 AWG 0.1" ID
R1 – 10 Ohm 2.0 W Carbon
R2, R3 – 10 Ohm 1.0 W Carbon
Z1 – Microstrip 0.19" W x 1.28" L
Z2 – Microstrip 0.28" W x 1.0" L
Z3 – Microstrip 0.31" W x 1.0" L
Z4 – Microstrip 0.31" W x 0.9" L
Board – Glass Teflon ϵ_R = 2.56 t = 0.062"
Input/Output Connectors – Type N UG58 A/U

FIGURE 2 – OUTPUT POWER versus INPUT POWER

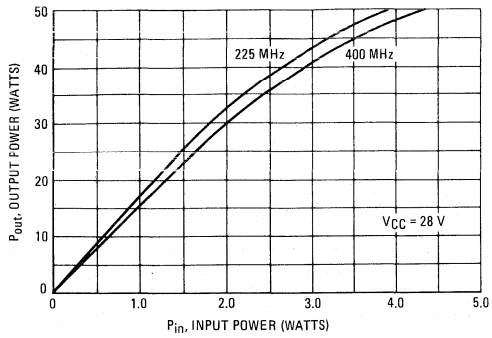


FIGURE 3 – OUTPUT POWER versus SUPPLY VOLTAGE
f = 225 MHz

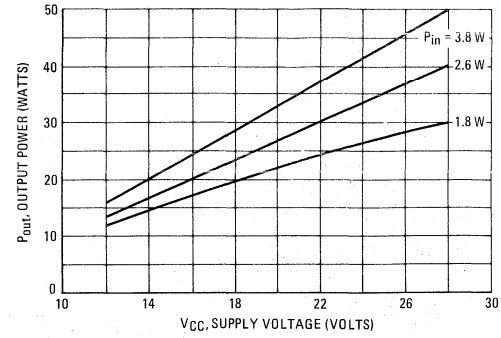
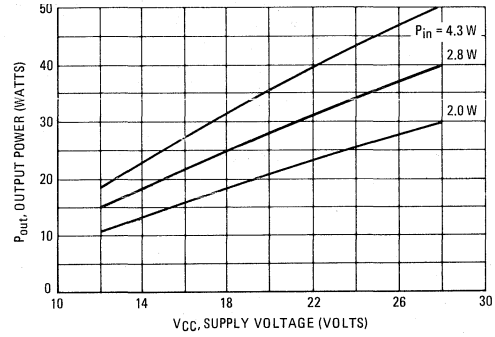
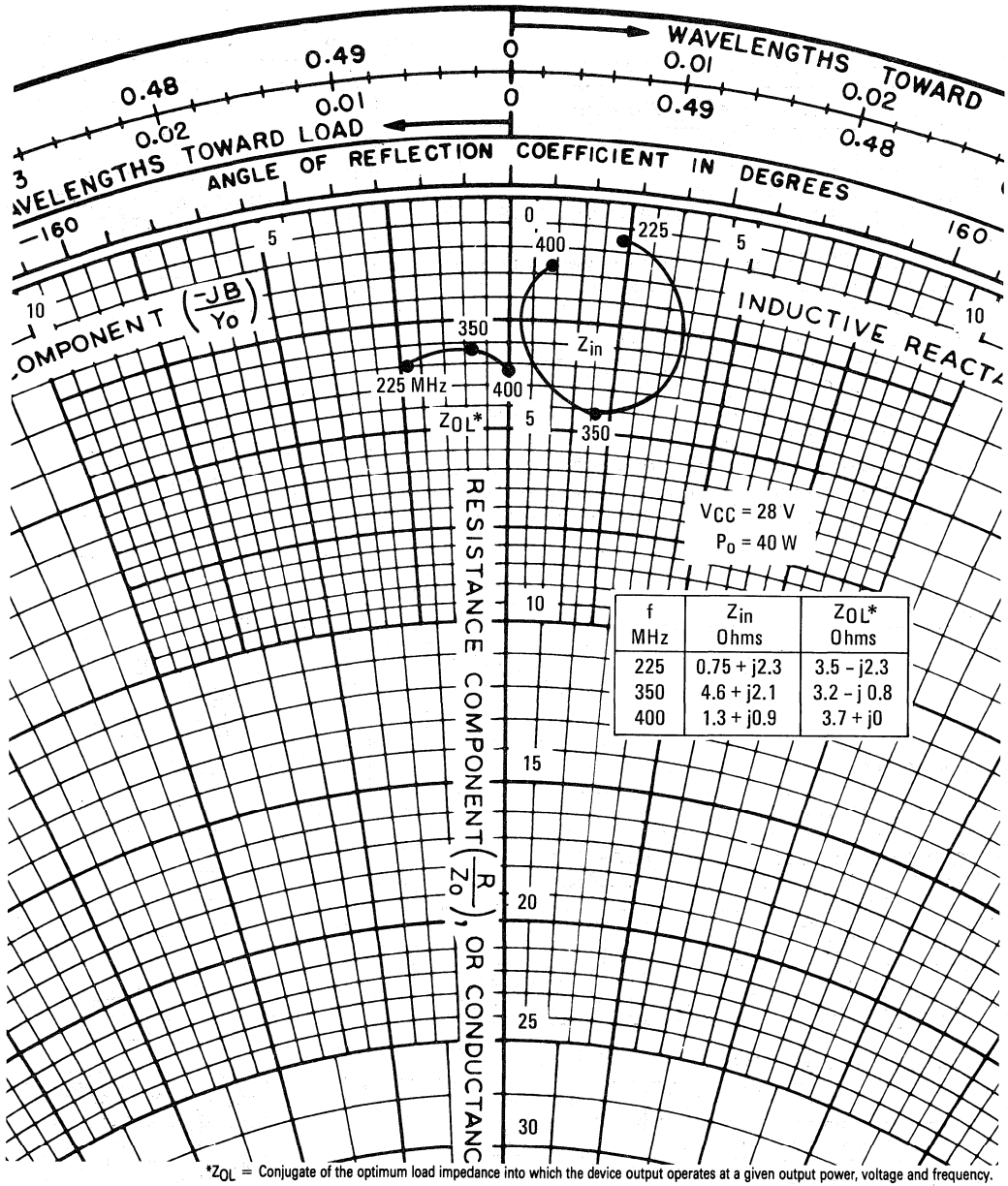


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE
f = 400 MHz



3

FIGURE 5 – SERIES EQUIVALENT INPUT-OUTPUT IMPEDANCE



f MHz	Z_{in} Ohms	Z_{OL}* Ohms
225	0.75 + j2.3	3.5 - j2.3
350	4.6 + j2.1	3.2 - j 0.8
400	1.3 + j0.9	3.7 + j0

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

MRF327

The RF Line

NPN SILICON RF POWER TRANSISTOR

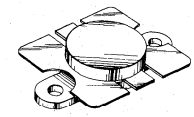
. . . designed primarily for wideband large-signal output amplifier stages in the 100-500 MHz frequency range.

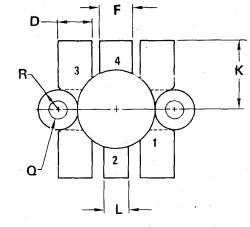
- Guaranteed Performance @ 400 MHz, 28 Vdc
  Output Power = 80 Watts over 225–400 MHz Band
  Minimum Gain = 7.3 dB @ 400 MHz
- Built-in Matching Network for Broadband Operation Using Double Match Technique
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR
- Gold Metallization System for High Reliability Applications
- Characterized for 100–500 MHz

80 W – 100-500 MHz

CONTROLLED "Q" BROADBAND RF POWER TRANSISTOR

NPN SILICON





STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. EMITTER
4. BASE
FLANGE-ISOLATED

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	12.45	12.95	0.490	0.510
C	5.97	7.62	0.235	0.300
D	5.33	5.59	0.210	0.220
F	5.08	5.33	0.200	0.210
H	18.29	18.54	0.720	0.730
J	0.10	0.15	0.004	0.006
K	10.29	–	0.405	–
L	3.81	4.06	0.150	0.160
N	3.81	4.32	0.150	0.170
Q	2.92	3.30	0.115	0.130
R	3.05	3.30	0.120	0.130

CASE 316-01

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	33	Vdc
Collector-Base Voltage	V_{CBO}	60	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous — Peak	I_C	9.0 12.0	Adc
Total Device Dissipation @ $T_C = 25^oC$ (1) Derate above 25^oC	P_D	250 1.43	Watts $W/^oC$
Storage Temperature Range	T_{stg}	−65 to+150	^oC

THERMAL CHARACTERISTICS

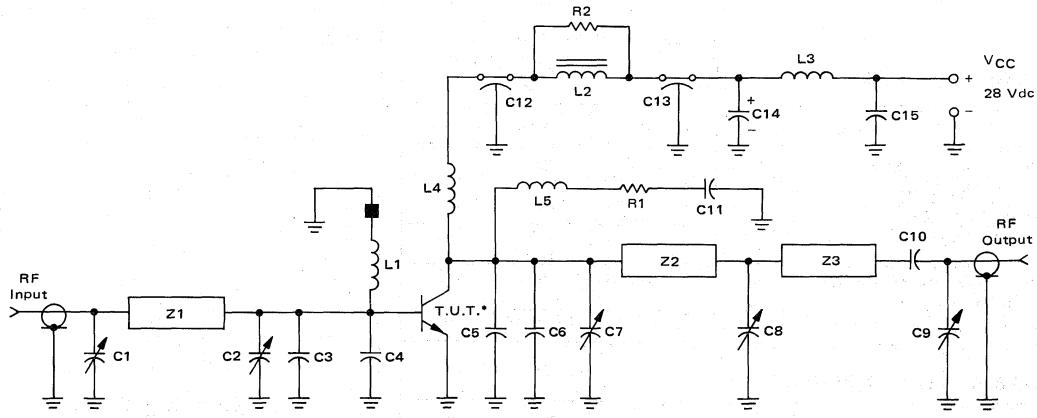
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	$^oC/W$

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 80 mAdc, I_B = 0)	$V_{(BR)CEO}$	33	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 80 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 8.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 80 mAdc, I_C = 0)	$V_{(BR)CBO}$	60	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	–	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	–	80	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	100	145	pF
FUNCTIONAL TESTS (Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 80 W, f = 400 MHz)	G_{PE}	7.3	9.0	–	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 80 W, f = 400 MHz)	η	50	60	–	%
Load Mismatch (V_{CC} = 28 V, P_{out} = 80 W, f = 400 MHz, VSWR 30:1 all phase angles)	ψ	No Degradation in Output Power			

FIGURE 1 – 400 MHz TEST CIRCUIT



C1, C2, C7, C8, C9 – 1.0-20 pF Piston Trimmer (Johanson JMC 5501)
C3, C4 – 36 pF ATC 100 mil Chip Capacitor
C5, C6 – 43 pF ATC 100-mil Chip Capacitor
C10 – 100 pF UNELCO
C11, C15 – 0.1 μF Erie Redcap
C12, C13 – 680 pF Feedthru
C14 – 1.0 μF 50 V Tantalum
L1 – 4 Turns #22 AWG Enameled, 3/16" ID Closewound with Ferroxcube Bead (#56-590-65/4B) on Ground End of Coil
L2 – Ferroxcube VK200-19/4B Ferrite Choke
L3 – 7 Turns #18 AWG, 11/16" Long, Wound on a 100 kΩ 2 Watt Resistor
L4 – 6 Turns #20 AWG Enameled, 3/16" ID Closewound
L5 – 4 Turns #22 AWG Enameled, 1/8" ID Closewound
Z1 – Microstrip 0.2" W x 1.5" L
Z2 – Microstrip 0.17" W x 1.16" L
Z3 – Microstrip 0.17" W x 0.63" L
R1, R2 – 10 Ω 2 Watt
Board – Glass Teflon $\in$R = 2.56, t = 0.062"
Input/Output Connectors Type N
T.U.T. Socket Lead Frame Etched from 80 mil Thick Copper
*Transistor Under Test

FIGURE 2 – POWER GAIN versus FREQUENCY

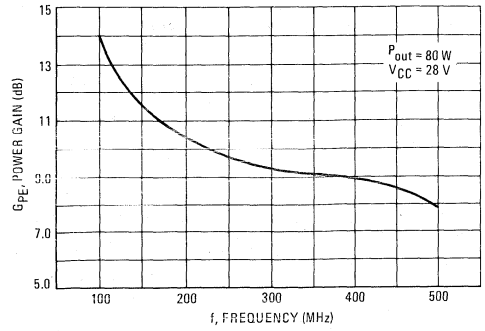


FIGURE 3 – OUTPUT POWER versus FREQUENCY

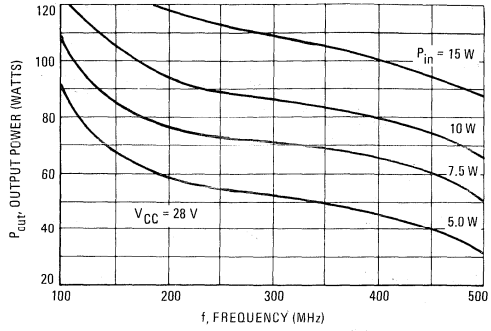


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE
f = 225 MHz

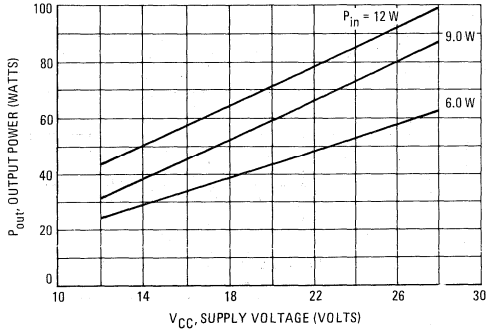


FIGURE 5 – OUTPUT POWER versus SUPPLY VOLTAGE
f = 400 MHz

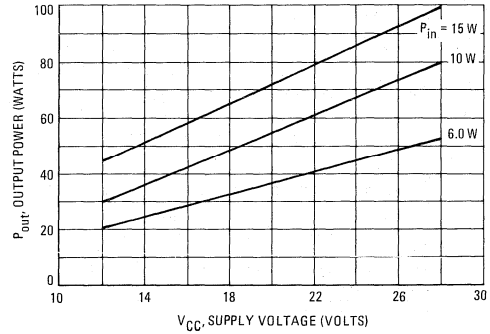


FIGURE 6 – OUTPUT POWER versus INPUT POWER

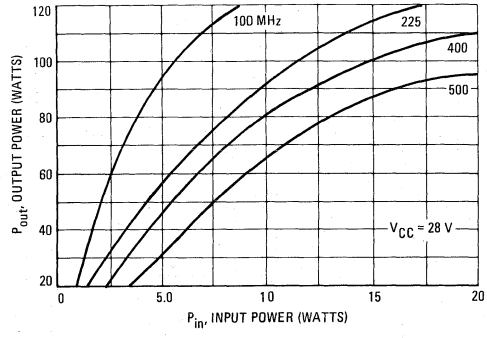
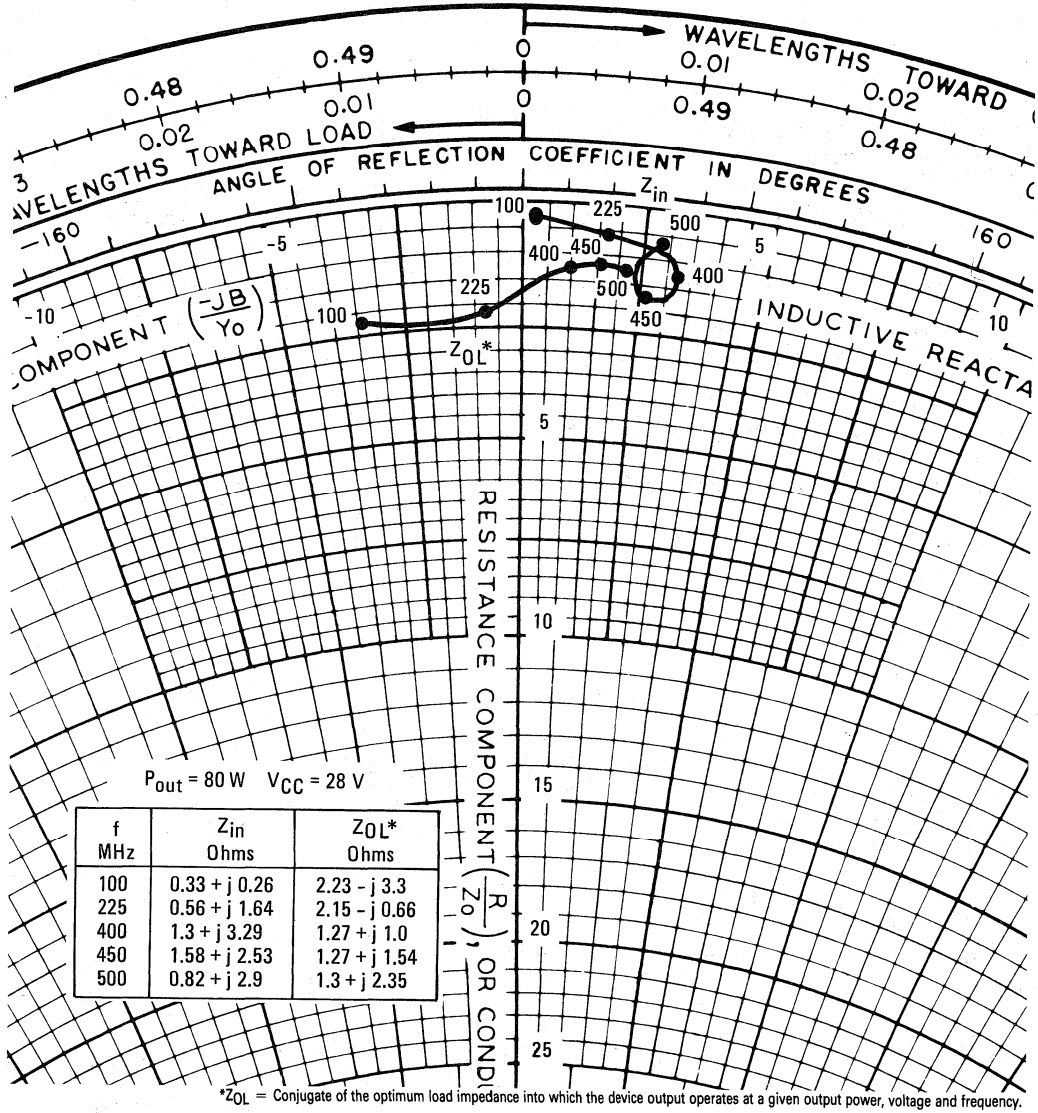


FIGURE 7 – SERIES EQUIVALENT INPUT-OUTPUT IMPEDANCE



f MHz	Z_{in} Ohms	Z_{OL}* Ohms
100	0.33 + j 0.26	2.23 - j 3.3
225	0.56 + j 1.64	2.15 - j 0.66
400	1.3 + j 3.29	1.27 + j 1.0
450	1.58 + j 2.53	1.27 + j 1.54
500	0.82 + j 2.9	1.3 + j 2.35

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

MRF329

The RF Line

NPN SILICON RF POWER TRANSISTOR

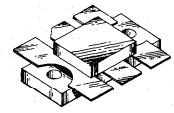
. . . designed primarily for wideband large-signal output and driver amplifier stages in the 100–500 MHz frequency range.

- Specified 28 Volt, 400 MHz Characteristics –
  Output Power = 100 Watts
  Minimum Gain = 7.0 dB
  Efficiency = 50% (Min)
- Built-In Matching Network for Broadband Operation Using Double Match Technique
- 100% Tested for Load Mismatch at All Phase Angles With 3:1 VSWR
- Gold Metallization System for High Reliability
- Replacement for MRF328

100 W – 100–500 MHz

CONTROLLED "Q" BROADBAND RF POWER TRANSISTOR

NPN SILICON



3

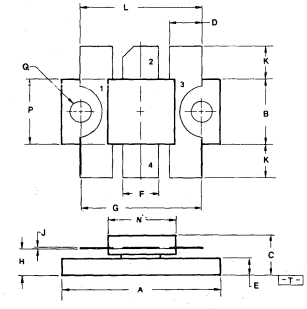
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	60	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous — Peak	I_C	9.0 12.0	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	270 1.54	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	0.65	°C/W

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.
(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.



STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. EMITTER
4. BASE

NOTES:
1. DIMENSIONS -A- AND -B- ARE DATUMS.
2. POSITIONAL TOLERANCE FOR MOUNTING HOLES: ⌖ ⌀ 0.13(0.005)Ⓜ T AⓂ BⓂ
3. -T- IS SEATING PLANE.
4. DIM "D" FOUR PLACES; DIM "F" TWO PLACES.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

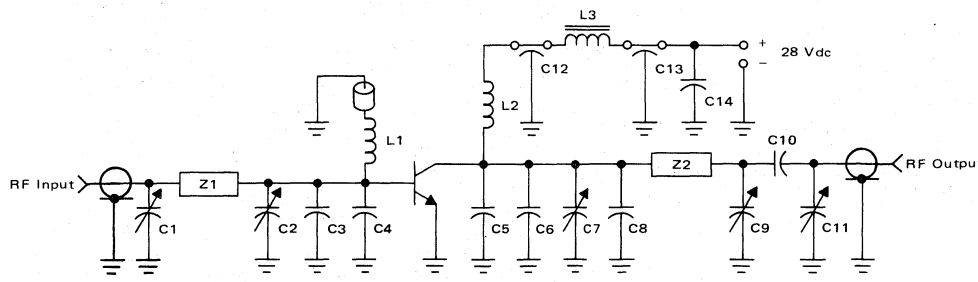
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.51	25.02	0.965	0.985
B	9.91	10.41	0.390	0.410
C	6.73	7.24	0.265	0.285
D	4.83	5.33	0.190	0.210
E	2.42	2.92	0.095	0.115
F	5.47	5.96	0.215	0.235
G	18.42 BSC		0.725 BSC	
H	3.94	4.44	0.155	0.175
J	0.10	0.15	0.004	0.006
K	4.95	5.21	0.195	0.205
L	18.80	19.55	0.740	0.770
N	10.54	10.80	0.415	0.425
P	9.91	10.16	0.390	0.400
Q	3.05	3.42	0.120	0.135

CASE 333-03

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 80 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 80 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 8.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 80 mAdc, I_E = 0)	$V_{(BR)CBO}$	60	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	–	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	–	80	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	95	125	pF
FUNCTIONAL TESTS (Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 100 W, f = 400 MHz)	G_{PE}	7.0	9.7	–	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 100 W, f = 400 MHz)	η	50	60	–	%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 100 W, f = 400 MHz VSWR = 3:1 all angles)	ψ	No Degradation in Output Power			

FIGURE 1 – 400 MHz TEST CIRCUIT



C1, C2, C7, C9 – 1.0–20 pF Johanson (JMC 5501)
C3, C4 – 36 pF 100 mil Chip Cap (ATC)
C5, C6 – 50 pF 100 mil Chip Cap (ATC)
C8 – 30 pF 100 mil Chip Cap (ATC)
C10 – 2-150 pF 100 mil Chip Caps in Parallel (ATC)
C11 – 1.0-10 pF Johanson (JMC 5201)
C12, C13 – 1000 pF UNELCO Feedthru
C14 – 0.1 μF Erie Redcap

L1 – 0.15 μH Molded Choke with Ferrite Bead (Ferroxcube #56-590-65/4B) on Ground End
L2 – 4 Turns #18 AWG, 1/4" ID
L3 – Ferroxcube VK200-19/4B

Z1 – Microstrip Line 2300 mils L X 210 mils W
Z2 – Microstrip Line 2300 mils L X 280 mils W

Board – Glass Teflon, t = 0.062", ϵ_r = 2.56

FIGURE 2 — OUTPUT POWER versus INPUT POWER

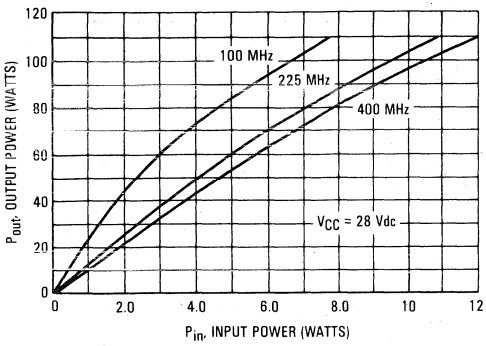


FIGURE 3 — OUTPUT POWER versus FREQUENCY

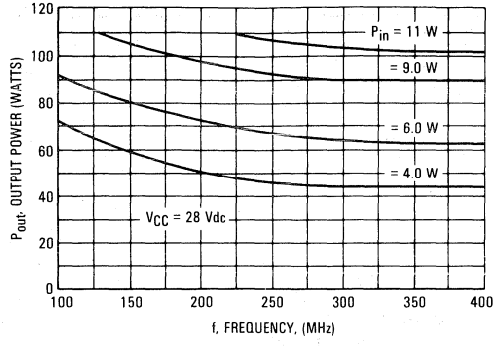


FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE (225 MHz)

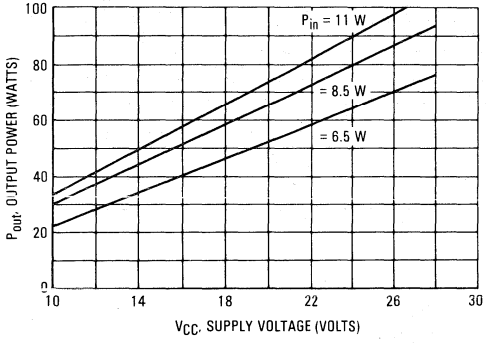


FIGURE 5 — OUTPUT POWER versus SUPPLY VOLTAGE (400 MHz)

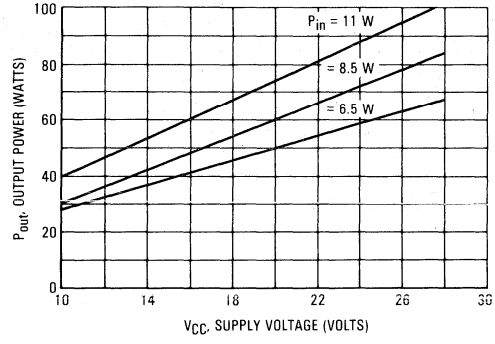


FIGURE 6 — POWER GAIN versus FREQUENCY

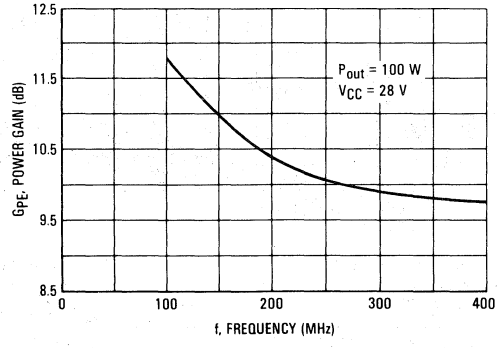
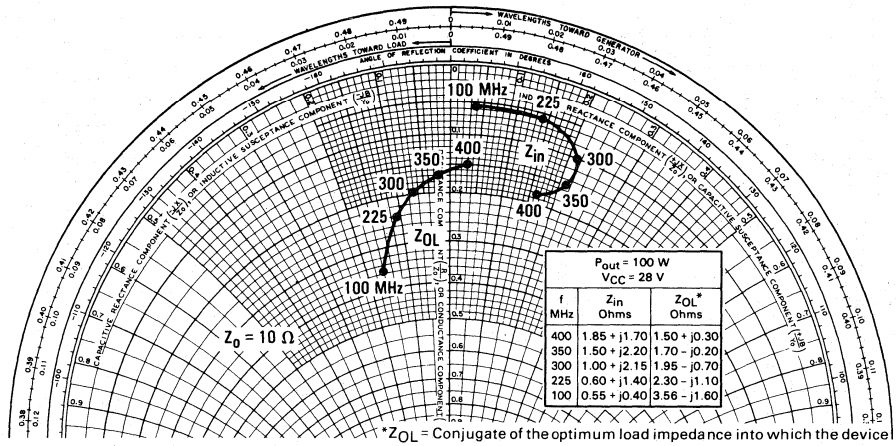


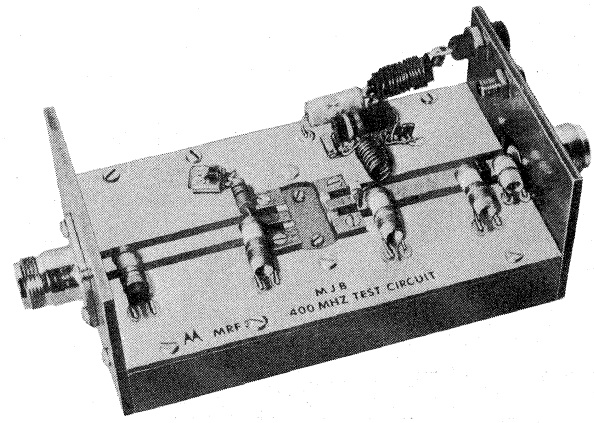
FIGURE 7 — SERIES EQUIVALENT INPUT/
OUTPUT IMPEDANCE



P_{out} = 100 W, V_{CC} = 28 V		
f MHz	Z_{in} Ohms	Z_{OL}^* Ohms
400	1.85 + j1.70	1.50 + j0.30
350	1.50 + j2.20	1.70 - j0.20
300	1.00 + j2.15	1.95 - j0.70
225	0.60 + j1.40	2.30 - j1.10
100	0.55 + j0.40	3.56 - j1.60

*Z_{OL} = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

FIGURE 8 — TEST FIXTURE



3

MRF331

The RF Line

10 W – 400 MHz

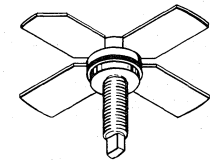
RF POWER
TRANSISTOR

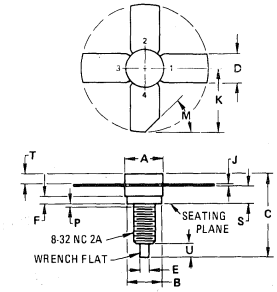
NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed primarily for wideband large-signal driver and predriver amplifier stages in the 100–500 MHz frequency range.

- Guaranteed Performance at 400 MHz and 28 Vdc
  Output Power = 10 Watts
  Minimum Gain = 8 dB
  Efficiency = 55%
- 100% Tested for Load Mismatch at All Phase Angles With 30:1 VSWR
- Broadband Version of MRF321
- Gold Metallization System for High Reliability
- Controlled Wirebonding Gives High Input Impedance
- See EB74 for Broadband Circuit Details





STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.06	7.26	0.278	0.286
B	6.20	6.50	0.244	0.256
C	14.99	16.51	0.590	0.650
D	5.46	5.97	0.215	0.235
E	1.40	1.65	0.055	0.065
F	1.52	–	0.060	–
J	0.08	0.18	0.003	0.007
K	11.05	–	0.435	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
S	3.00	3.25	0.118	0.128
T	1.40	1.78	0.055	0.070
U	2.92	3.68	0.115	0.145

CASE 244-04

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	33	Vdc
Collector-Base Voltage	V_{CBO}	60	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current – Continuous – Peak	I_C	1.1 1.5	Adc
Total Device Dissipation @ T_A = 25°C (1) Derate above 25°C	P_D	27 160	Watts mW/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	6.4	°C/W

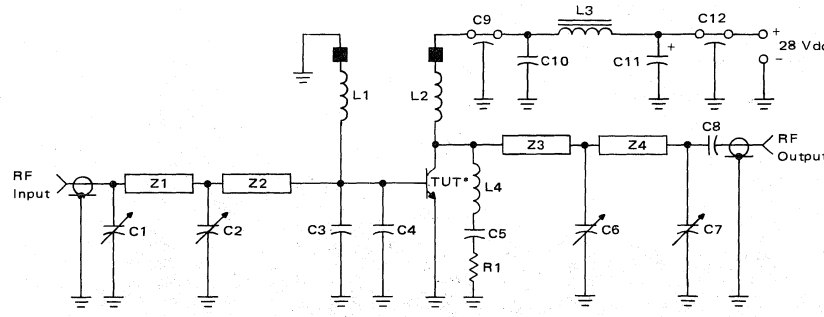
(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	33	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 20 mAdc, I_E = 0)	$V_{(BR)CBO}$	60	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 2.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	20	–	80	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	10	12	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 10 W, f = 400 MHz)	G_{PE}	8.0	10.5	–	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 10 W, f = 400 MHz)	η	55	65	–	%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 10 W, f = 400 MHz, VSWR = 30:1 all phase angles)	ψ	No Degradation in Power Output			

FIGURE 1 – 400 MHz TEST CIRCUIT



C1, C2, C6 – 1.0–20 pF Johanson Trimmer (JMC5501)
C3, C4 – 50 pF Chip Capacitor
C5, C10 – 0.1 μF Erie Redcap
C7 – 0.5–10 pF Johanson Trimmer (JMC5201)
C8 – 270 pF Chip Capacitor
C9, C12 – 680 pF Feedthru
C11 – 1.0 μF 50 V Tantalum

R1 – 5.1 Ω 1/4 Watt

L1, L2 – 0.15 μH Molded Choke with Ferrite Bead (Ferroxcube 56-590-65/4B)

L3 – VK-200-19/4B
L4 – 4 Turns #20 Enamel, 1/8" ID

Z1 – Microstrip 0.1" W X 1.35" L
Z2 – Microstrip 0.1" W X 0.55" L
Z3 – Microstrip 0.1" W X 0.8" L
Z4 – Microstrip 0.1" W X 1.75" L

Board – Glass Teflon ϵ_r = 2.56, t = 0.062"

Input/Output Connectors – Type N

*Transistor Under Test

FIGURE 2 – POWER GAIN versus FREQUENCY

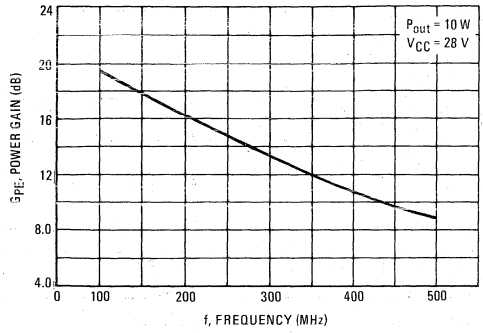


FIGURE 3 – OUTPUT POWER versus INPUT POWER

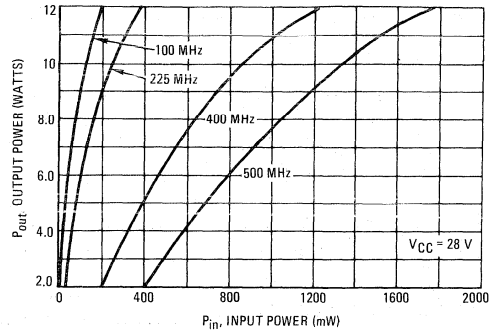


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

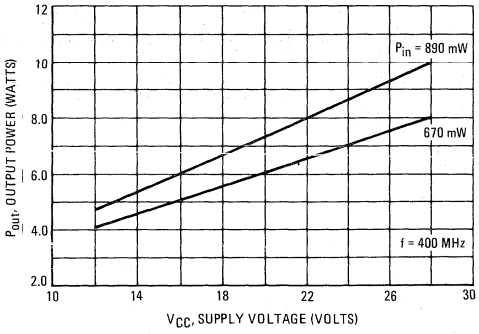


FIGURE 5 – TEST CIRCUIT

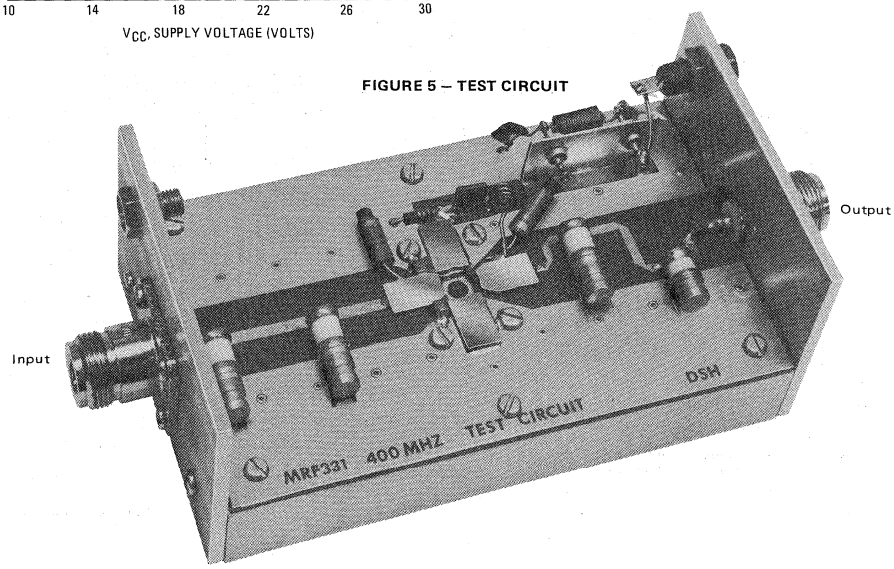
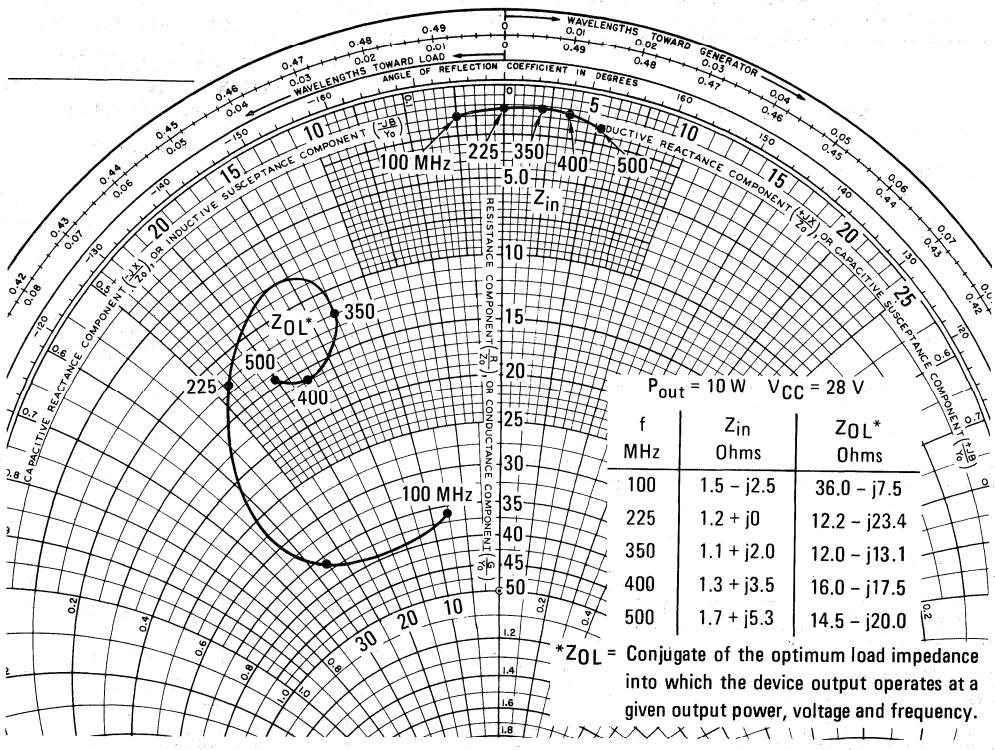


FIGURE 6 – SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCE



P_{out} = 10 W V_{CC} = 28 V

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
100	1.5 – j2.5	36.0 – j7.5
225	1.2 + j0	12.2 – j23.4
350	1.1 + j2.0	12.0 – j13.1
400	1.3 + j3.5	16.0 – j17.5
500	1.7 + j5.3	14.5 – j20.0

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

3

MRF338

The RF Line

NPN SILICON RF POWER TRANSISTOR

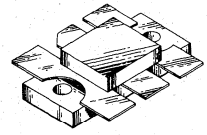
. . . designed primarily for wideband large-signal output and driver amplifier stages in the 400–512 MHz frequency range.

- Specified 28 Volt, 470 MHz Characteristics —
  Output Power = 80 Watts
  Minimum Gain = 7.3 dB
  Efficiency = 50% (Min)
- Built-In Matching Network for Broadband Operation
- 100% Tested for Load Mismatch at All Phase Angles With 30:1 VSWR
- Gold Metallization System for High Reliability Applications

80 W — 400-512 MHz

CONTROLLED "Q" BROADBAND RF POWER TRANSISTOR

NPN SILICON



3

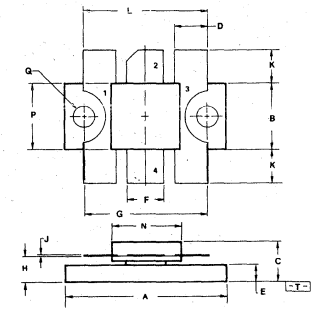
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	60	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous — Peak	I_C	9.0 12.0	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	250 1.43	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	0.7	°C/W

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.
(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.



NOTES:
1. DIMENSIONS -A- AND -B- ARE DATUMS.
2. POSITIONAL TOLERANCE FOR MOUNTING HOLES: ⌖ ø 0.13(0.005)Ⓜ T AⓂ BⓂ
3. -T- IS SEATING PLANE.
4. DIM "D" FOUR PLACES; DIM "F" TWO PLACES.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. EMITTER
4. BASE

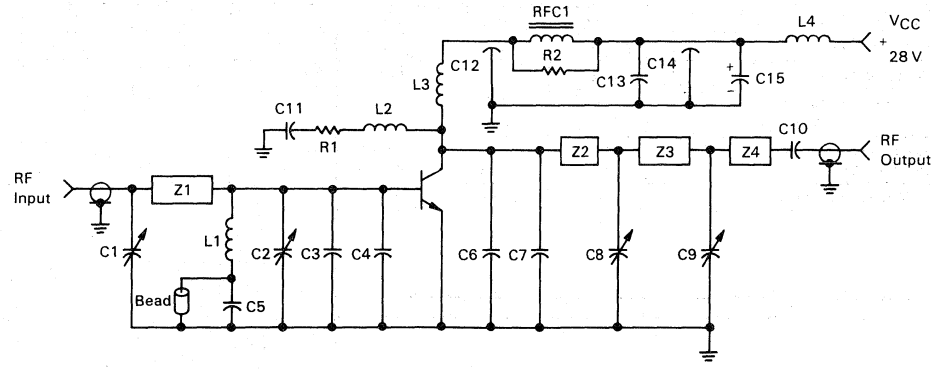
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.51	25.02	0.965	0.985
B	9.91	10.41	0.390	0.410
C	6.73	7.24	0.265	0.285
D	4.83	5.33	0.190	0.210
E	2.42	2.92	0.095	0.115
F	5.47	5.96	0.215	0.235
G	18.42 BSC		0.725 BSC	
H	3.94	4.44	0.155	0.175
J	0.10	0.15	0.004	0.006
K	4.95	5.21	0.195	0.205
L	18.80	19.55	0.740	0.770
N	10.54	10.80	0.415	0.425
P	9.91	10.16	0.390	0.400
Q	3.18	3.42	0.125	0.135

CASE 333-02

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 80 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 80 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 8.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 80 mAdc, I_E = 0)	$V_{(BR)CBO}$	60	—	—	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	—	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	—	80	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	95	125	pF
FUNCTIONAL TESTS (Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 80 W, f = 470 MHz)	G_{PE}	7.3	8.8	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 80 W, f = 470 MHz)	η	50	60		%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 80 W, f = 470 MHz, VSWR = 30:1 all angles)	ψ	No Degradation in Output Power			

FIGURE 1 — 470 MHz TEST CIRCUIT



C1, C2, C8, C9 — 0.8–20 pF Johanson (JMC 5501)
C3, C4, C6, C7 — 25 pF Underwood 100 V
C5, C10 — 100 pF Underwood 100 V
C11, C13 — 0.1 μF Erie Redcap
C12, C14 — 680 pF Feedthru
C15 — 1.0 μF Tantalum
L1 — 0.15 μH Molded Choke
L2 — 5 Turns #20 AWG, 0.185″ ID, Close Wound
L3 — 3 Turns #18 AWG, 0.185″ ID, Close Wound
L4 — 4 Turns #18 AWG, 0.185″ ID, Close Wound

RFC1 — Ferroxcube VK200 19/4B
Bead — Ferroxcube #56-590-65/3B
R1, R2 — 10 Ω 2.0 Watt Carbon
Z1 — Microstrip Line 0.190″ W × 2.5″ L
Z2 — Microstrip Line 0.190″ W × 0.289″ L
Z3 — Microstrip Line 0.190″ W × 0.55″ L
Z4 — Microstrip Line 0.190″ W × 0.325″ L
Board — Glass Teflon, ϵ_r = 2.56, t = 0.062″

FIGURE 2 — POWER OUTPUT versus POWER INPUT

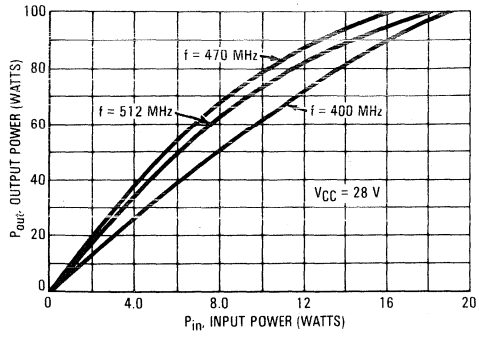


FIGURE 3 — OUTPUT POWER versus SUPPLY VOLTAGE

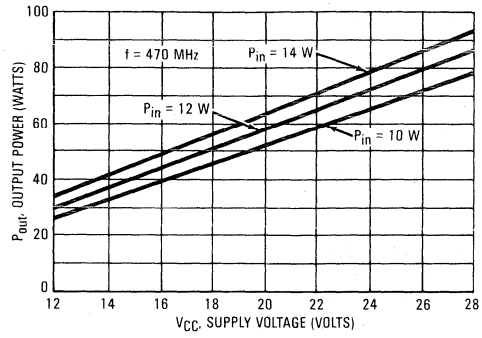


FIGURE 4 — POWER GAIN versus FREQUENCY

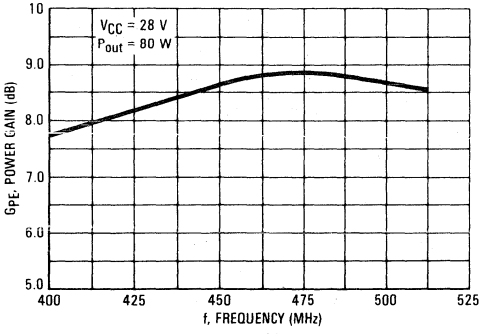


FIGURE 5 — OUTPUT POWER versus FREQUENCY

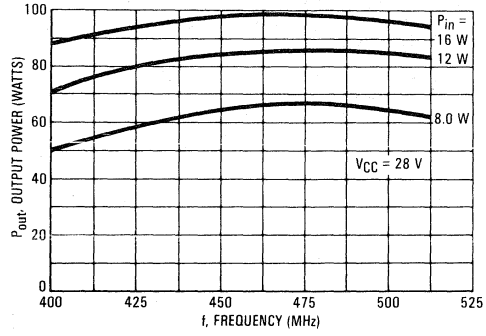
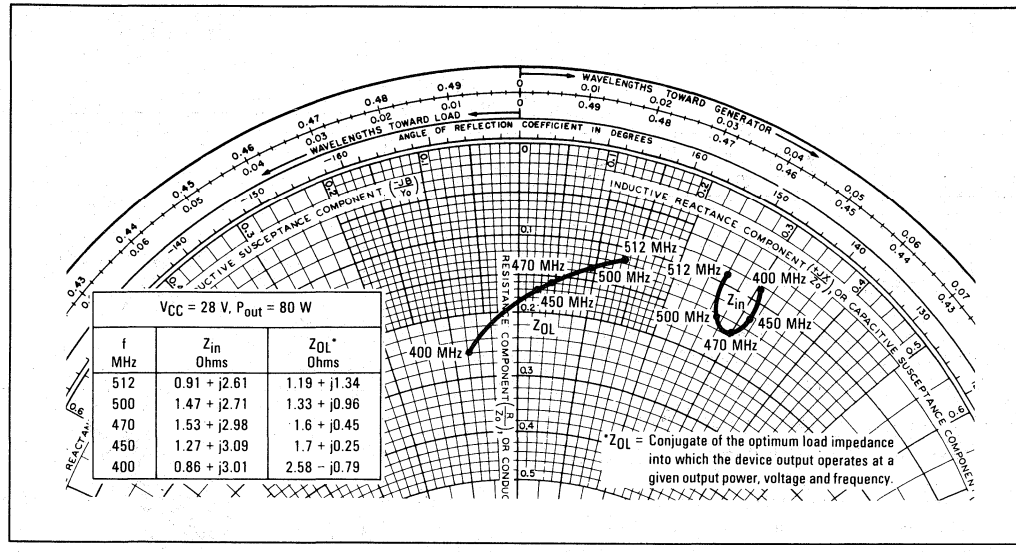


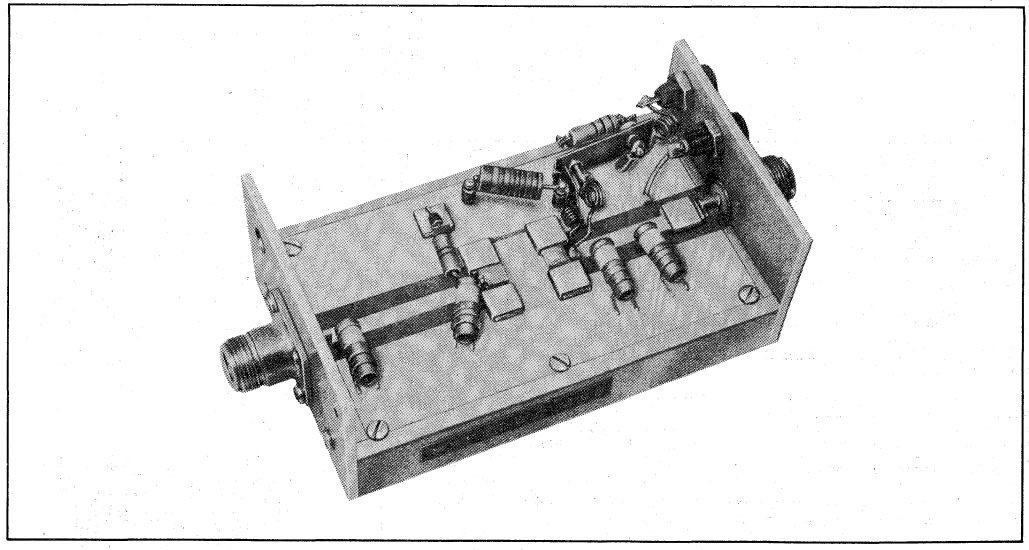
FIGURE 6 — SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCE



V_{CC} = 28 V, P_{out} = 80 W

f MHz	Z_{in} Ohms	Z_{OL}^* Ohms
512	0.91 + j2.61	1.19 + j1.34
500	1.47 + j2.71	1.33 + j0.96
470	1.53 + j2.98	1.6 + j0.45
450	1.27 + j3.09	1.7 + j0.25
400	0.86 + j3.01	2.58 − j0.79

FIGURE 7 — TEST FIXTURE



3

MRF340

The RF Line

NPN SILICON RF POWER TRANSISTOR

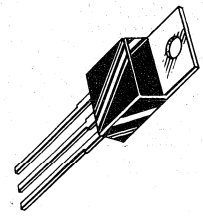
. . . designed primarily for use in VHF amplifiers with amplitude modulation and other communications equipment operating to 150 MHz.

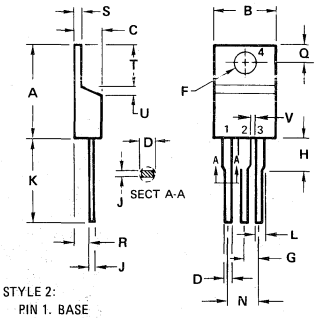
- Low Cost Common Emitter TO-220 Package
- Specified 27 V, 136 MHz Performance:
  Output Power = 8.0 W
  Power Gain = 13 dB Min
  Efficiency = 50% Min
- 20:1 VSWR Load Mismatch Capability at Rated Output Power and Supply Voltage
- Other Devices in the Series:
  MRF342 24 W
  MRF344 60 W

8 W 100–150 MHz

RF POWER TRANSISTOR

NPN SILICON





STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	35	Vdc
Collector-Base Voltage	V_{CBO}	65	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Continuous Peak	I_C	1.0 1.2	Adc
Total Device Dissipation — $T_C = 25^oC$ (1) Derate above 25^oC	P_D	15 86	Watts mW/^oC
Storage Temperature Range	T_{stg}	−65 to +150	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	11.6	$^oC/W$

1. These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

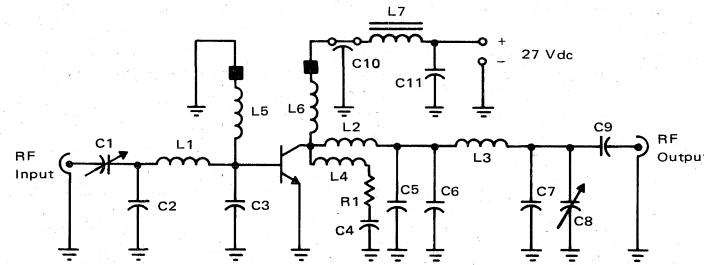
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

CASE 221A-02

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	35	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	65	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 20 mAdc, I_E = 0)	$V_{(BR)CBO}$	65	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 2.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 27 Vdc, V_{BE} = 0)	I_{CES}	–	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CD} = 5.0 Vdc)	h_{FE}	10	–	100	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 27 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	8.0	15	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 13.5 Vdc, P_{out} = 2.0 W, f = 136 MHz)	G_{PE}	9.0	10.5	–	dB
Common Emitter Amplifier Power Gain (V_{CC} = 27 Vdc, P_{out} = 8.0 W, f = 136 MHz)	G_{PE}	13.0	14.9	–	dB
Collector Efficiency (V_{CC} = 27 Vdc, P_{out} = 8.0 W, f = 136 MHz)	η	50	60	–	%
Load Mismatch (V_{CC} = 27 Vdc, P_{out} = 8.0 W (peak), f = 136 MHz. Drive modulated with 1.0 kHz square wave, 50% duty cycle. Load VSWR ≥ 20:1, all phase angles)	ψ	No Degradation in Power Output			

FIGURE 1 – 136 MHz TEST CIRCUIT



C1 – Arco 404 8–60 pF
C2, C5 – 40 pF UNELCO
C3 – 80 pF UNELCO
C4, C11 – 0.1 μF Erie Redcap
C6 – 25 pF UNELCO
C7 – 5.0 pF UNELCO
C8 – Arco 403 3–35 pF
C9 – 510 pF Dipped Mica
C10 – 680 pF Feedthru

L1 – 3 Turns #18 AWG, 1/8" ID
L2, L3 – 4 Turns #18 AWG, 1/8" ID
L4 – 0.33 μH Molded Choke
L5 – 0.15 μH Molded Choke with Ferrite Bead
L6 – 0.47 μH Molded Choke with Ferrite Bead
L7 – VK-200-19/4B

R1 – 100 Ω, 1.0 Watt

FIGURE 2 – POWER GAIN versus FREQUENCY

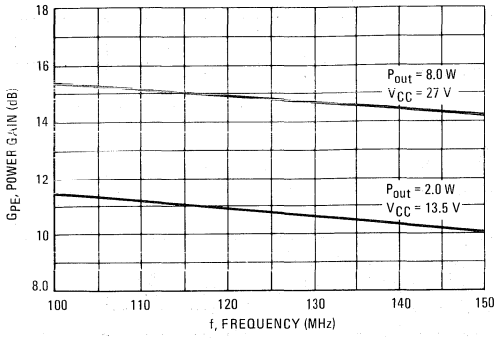


FIGURE 3 – OUTPUT POWER versus SUPPLY VOLTAGE (f = 136 MHz)

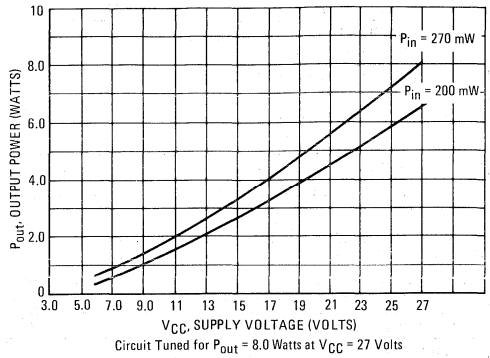


FIGURE 4 – OUTPUT POWER versus INPUT POWER (V_{CC} = 27 V)

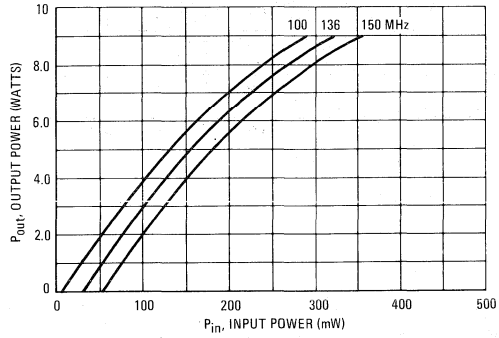


FIGURE 5 – OUTPUT POWER versus INPUT POWER (V_{CC} = 13.5 V)

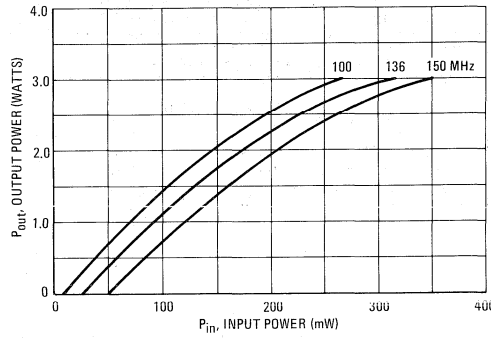
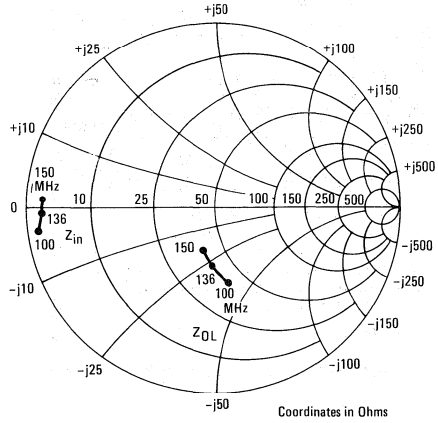


FIGURE 6 – SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCES



V_{CC} = 27 V P_{out} = 8.0 W

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
100	3.40 – j1.70	42.6 – j31.8
136	4.00 – j0.57	39.2 – j26.4
150	3.95 + j0.66	38.3 – j17.0

*Z_{OL} = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

FIGURE 7 – 136 MHz TEST AMPLIFIER

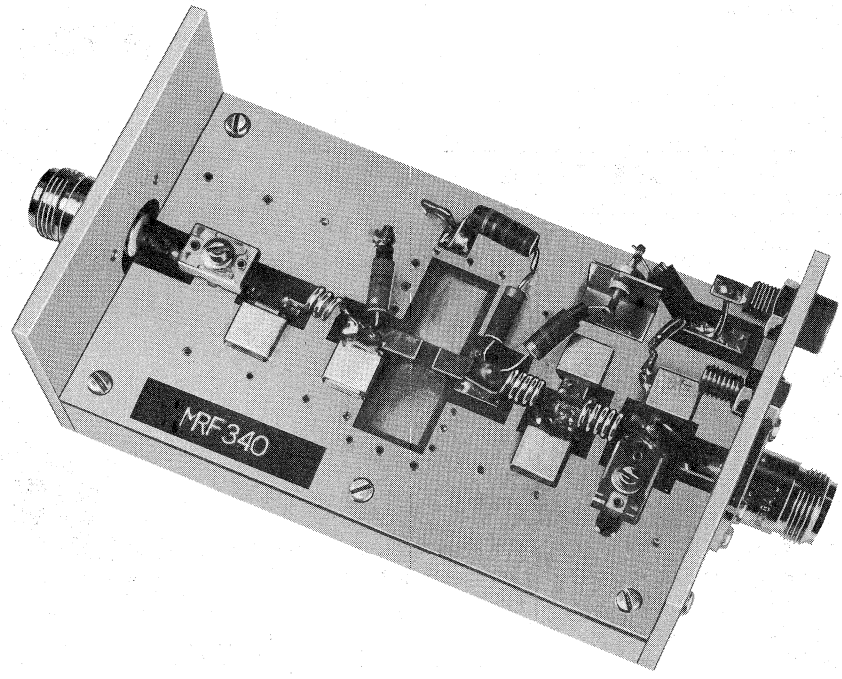
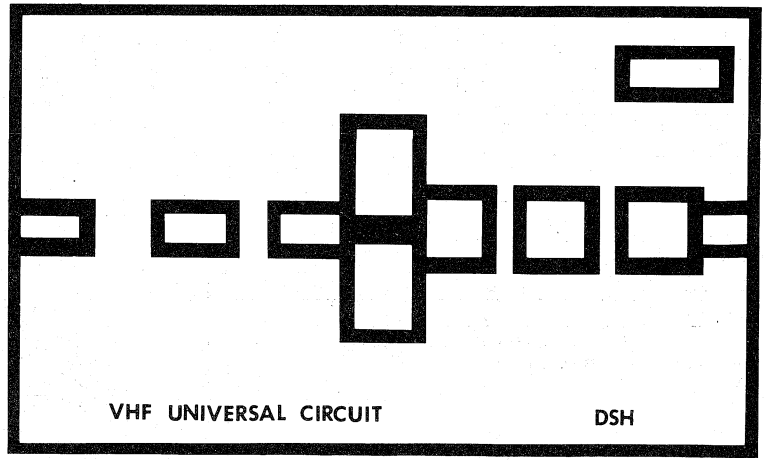


FIGURE 8 – PRINTED CIRCUIT BOARD LAYOUT – 136 MHz TEST CIRCUIT



MRF344

The RF Line

60 W 100–150 MHz

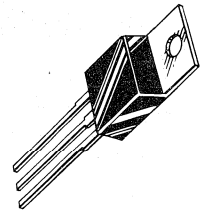
RF POWER TRANSISTOR

NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed primarily for use in VHF amplifiers with amplitude modulation and other communications equipment operating to 150 MHz.

- Low Cost Common Emitter TO-220 Package
- Specified 27 V, 136 MHz Performance:
  Output Power = 60 W
  Power Gain = 6.0 dB Min
  Efficiency = 50% Min
- 20:1 VSWR Load Mismatch Capability at Rated Peak Output Power and Supply Voltage
- Other Devices in the Series:
  MRF340 8 W
  MRF342 24 W



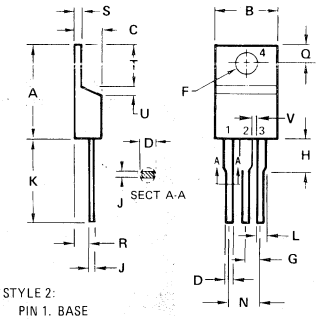
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	35	Vdc
Collector-Base Voltage	V_{CBO}	65	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Continuous Peak	I_C	5.0 6.0	Adc
Total Device Dissipation — T_C = 25°C (1) Derate above 25°C	P_D	87.5 0.5	Watts mW/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	°C/W

1. These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.



STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

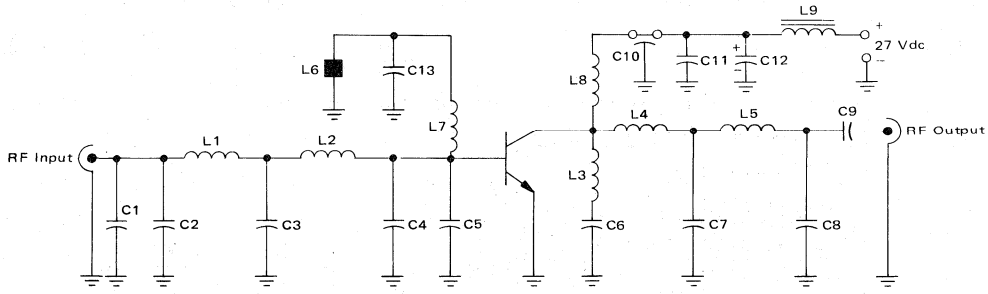
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

CASE 221A-02

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	35	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	65	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 50 mAdc, I_E = 0)	$V_{(BR)CBO}$	65	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 27 Vdc, V_{BE} = 0)	I_{CES}	–	–	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	–	80	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 27 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	130	200	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 13.5 Vdc, P_{out} = 15 W, f = 136 MHz)	G_{PE}	4.0	4.5	–	dB
Common Emitter Amplifier Power Gain (V_{CC} = 27 Vdc, P_{out} = 60 W, f = 136 MHz)	G_{PE}	6.0	6.7	–	dB
Collector Efficiency (V_{CC} = 27 Vdc, P_{out} = 60 W, f = 136 MHz)	η	50	60	–	%
Load Mismatch (V_{CC} = 27 Vdc, P_{out} = 60 W (peak), f = 136 MHz. Drive modulated with 1.0 kHz square wave, 50% duty cycle. Load VSWR ≥ 20:1, all phase angles)	ψ	No Degradation in Power Output			

FIGURE 1 – 136 MHz TEST CIRCUIT



C1, C2 – 10 pF UNELCO
C3, C8 – 25 pF UNELCO
C4, C5, C7 – 100 pF UNELCO
C6, C11 – 0.1 μF Erie Redcap
C9 – 1000 pF UNELCO
C10 – 1000 pF UNELCO Feedthru
C12 – 1.0 μF 50 V Tantalum
C13 – 200 pF UNELCO

L1 – 3/4" of #20 AWG
L2 – 1/2" of #20 AWG
L3 – 2 Turns, 1/8" ID #20 AWG
L4 – Copper Strap 15 mil Thick 3/16" X 1/2" L
L5 – 2 Turns #20 AWG 1/4" ID
L6 – Ferrite Bead on Lead of L7
L7, L8 – 0.15 μH Molded Choke
L9 – VK-200-19/4B

Input/Output Connectors Type N

FIGURE 2 – POWER GAIN versus FREQUENCY

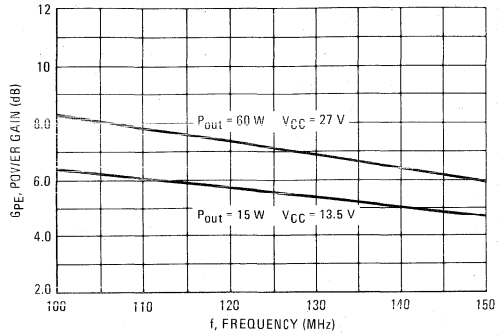


FIGURE 3 – OUTPUT POWER versus SUPPLY VOLTAGE (f = 136 MHz)

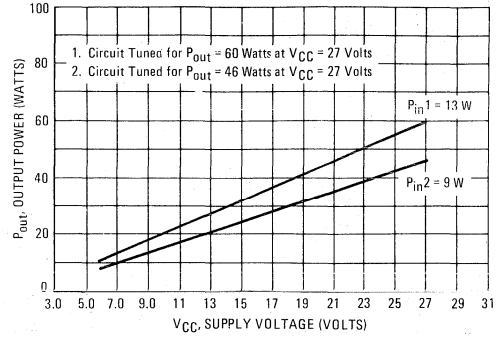


FIGURE 4 – OUTPUT POWER versus INPUT POWER (V_{CC} = 27 V)

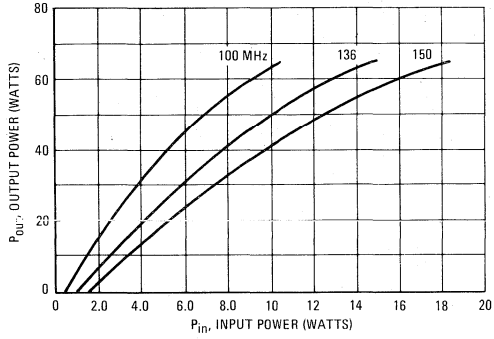


FIGURE 5 – OUTPUT POWER versus INPUT POWER (V_{CC} = 13.5 V)

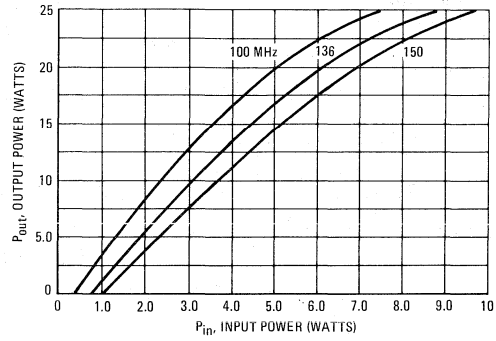
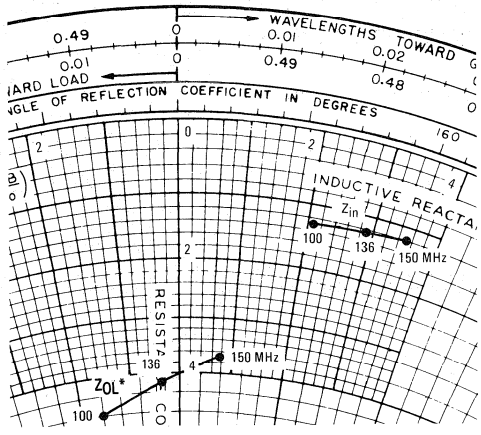


FIGURE 6 – SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCES



V_{CC} = 27 V P_{out} = 60 W

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
100	1.33 + j2.1	4.8 – j1.6
136	1.25 + j2.86	4.2 – j0.32
150	1.2 + J3.5	3.7 + j0.8

*Z_{OL} = Conjugate of the optimum load impedance into which the device operates at a given output power voltage, and frequency.

FIGURE 7 – 136 MHz TEST AMPLIFIER

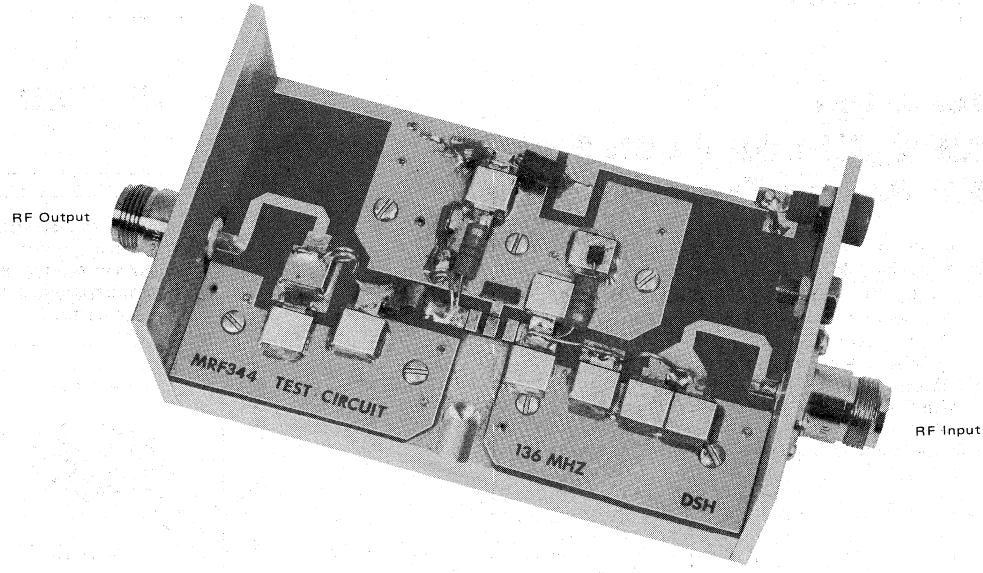
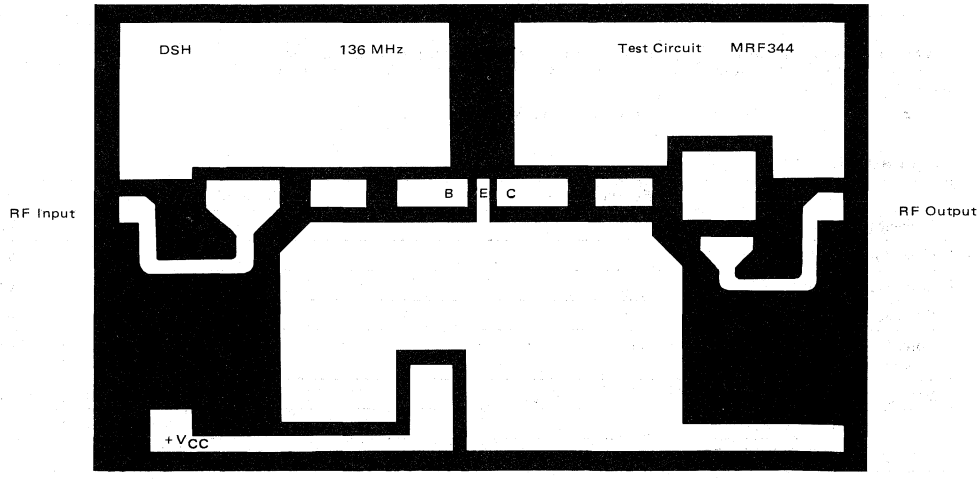


FIGURE 8 – PRINTED CIRCUIT BOARD LAYOUT – 136 MHz TEST CIRCUIT



MRF390

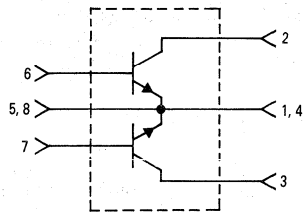
**60 WATTS, 30–500 MHz
CONTROLLED "Q"
BROADBAND PUSH-PULL
RF POWER TRANSISTOR
NPN SILICON**

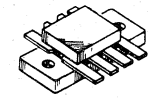
The RF Line

NPN Silicon Push-Pull RF Power Transistor

. . . designed primarily for wideband large-signal output and driver amplifier stages in the 30–500 MHz frequency range.

- Specified 28 Volt, 400 MHz Characteristics —
  Output Power = 60 Watts
  Typical Gain = 9.5 dB
  Efficiency = 55% (Typ)
- Built-In Input Impedance Matching Networks for Broadband Operation
- Push-Pull Configuration Reduces Even Numbered Harmonics
- Gold Metallization System for High Reliability
- 100% Tested for Load Mismatch





CASE 744-02

3

The MRF390 is two transistors in a single package with separate base and collector leads and emitters common. This arrangement provides the designer with a space saving device capable of operation in a push-pull configuration.

PUSH-PULL TRANSISTORS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	60	Vdc
Emitter-Base Voltage	V_{EBO}	4	Vdc
Collector Current — Continuous	I_C	7	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	140 0.80	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W

(1) These devices are designed for RF operation. The total dissipation rating applies only when the devices are operated as RF push-pull amplifiers.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (NOTE 1)					
Collector-Emitter Breakdown Voltage (I_C = 30 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 30 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 3 mAdc, I_C = 0)	$V_{(BR)EBO}$	4	—	—	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	—	3	mAdc
ON CHARACTERISTICS (NOTE 1)					
DC Current Gain (I_C = 1 Adc, V_{CE} = 5 Vdc)	h_{FE}	20	—	100	—
DYNAMIC CHARACTERISTICS (NOTE 1)					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1 MHz)	C_{ob}	—	37	50	pF
FUNCTIONAL TEST (NOTE 2 — See Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 60 W, f = 400 MHz)	G_{pe}	7.5	9.5	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 60 W, f = 400 MHz)	η	50	55	—	%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 60 W, f = 400 MHz VSWR = 30:1, all phase angles)	ψ	No Degradation in Output Power			

NOTES:
1. Each transistor chip measured separately.
2. Both transistor chips operating in push-pull amplifier.

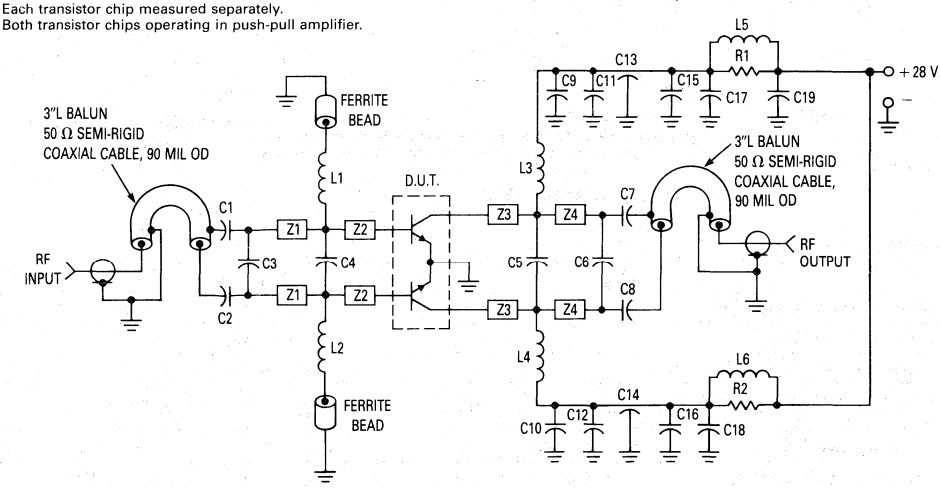


Figure 1. 400 MHz Test Circuit

C1, C2 — 240 pF, 100 Mil Chip
C3 — 12 pF, 100 Mil Chip
C5 — 20 pF, 100 Mil Chip
C4, C6 — 18 pF, 100 Mil Chip
C7, C8 — 270 pF, 100 Mil Chip
C9, C10, C11, C12 — 470 pF, 100 Mil Chip
C13, C14 — 680 pF Feedthru Capacitor
C15, C16, C19 — 0.1 μF Disc Ceramic
C17, C18 — 1 μF, 50 V Tantalum Capacitor
R1, R2 — 910 kΩ, 2 W Carbon Res.

L1, L2 — 10 μH RF Choke With Ferrite Bead
L3, L4 — 5 Turns #20 AWG, 1/4" ID
L5, L6 — 15 Turns #18 AWG Enameled, 0.35" ID Closewound Around R1, R2 Respectively
Z1 — Microstrip Line 850 Mils L x 130 Mils W
Z2, Z3 — Microstrip Line 250 Mils L x 130 Mils W
Z4 — Microstrip Line 830 Mils L x 130 Mils W
Board Material — 0.0625" Teflon Fiberglass ϵ_r = 2.5 ± 0.05, 1 oz. cu. clad, Double Sided

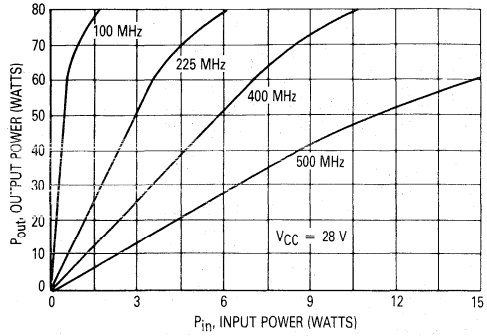


Figure 2. Output Power versus Input Power/Frequency

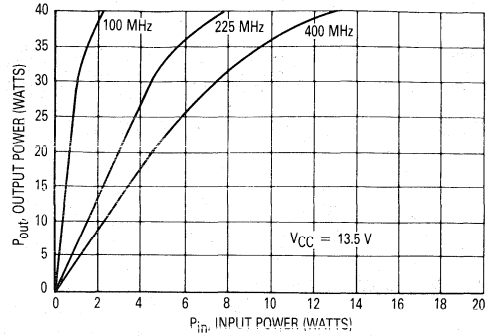


Figure 3. Output Power versus Input Power/Frequency

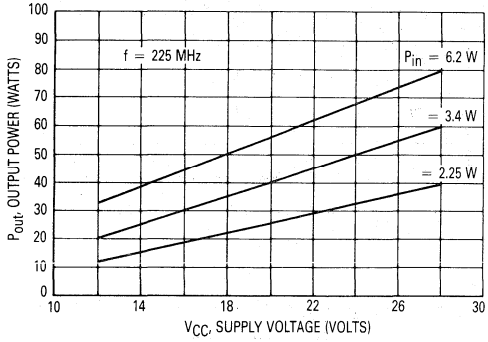


Figure 4. Output Power versus Supply Voltage — 225 MHz

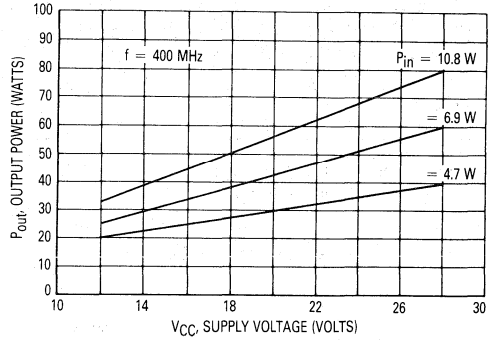


Figure 5. Output Power versus Supply Voltage — 400 MHz

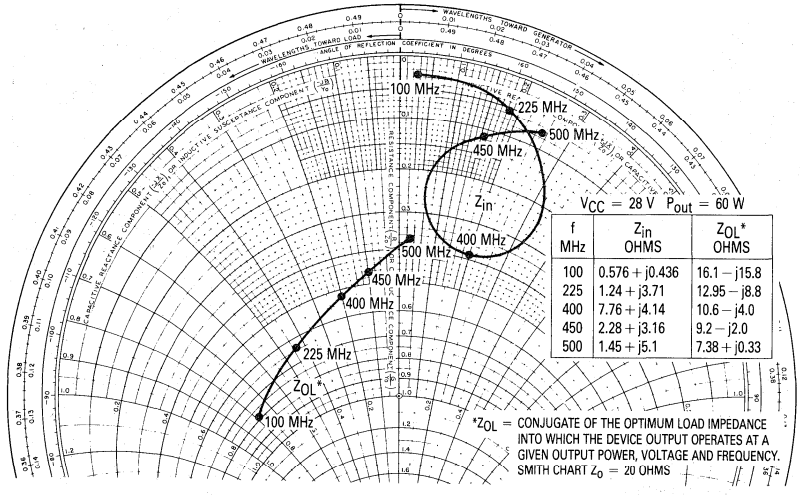
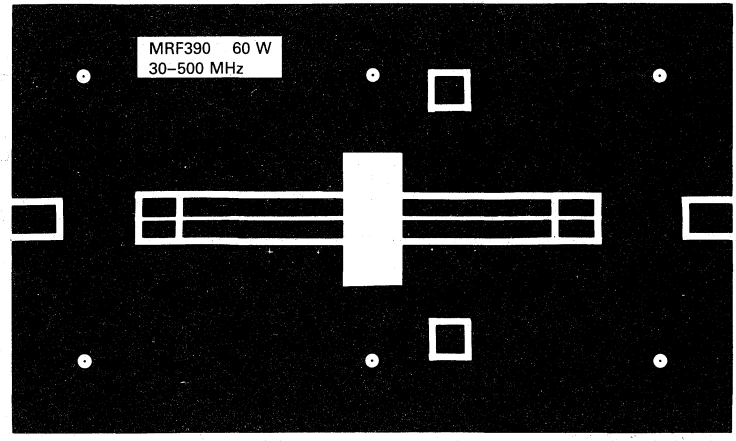


Figure 6. Series Equivalent Input/Output Impedances



NOTE: The Printed Circuit Board shown is 75% of the original.

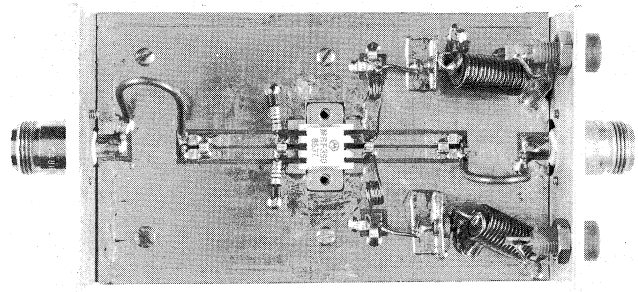
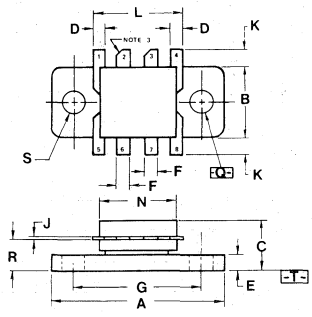


Figure 7. 400 MHz Test Circuit and Photomaster

OUTLINE DIMENSIONS



STYLE 1:
PIN 1. EMITTER (COMMON)
2. COLLECTOR
3. COLLECTOR
4. EMITTER (COMMON)
5. EMITTER (COMMON)
6. BASE
7. BASE
8. EMITTER (COMMON)

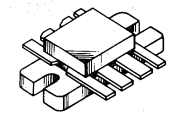
NOTES:
1. DIMENSION Q IS DATUM.
2. POSITIONAL TOLERANCE FOR S:
⌖ ⌀ 0.18 (0.007) Ⓜ T Q Ⓜ
3. IDENTIFICATION NOTCH:
1.0 mm (0.04) MIN X 45°.
4. -T- IS SEATING PLANE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

CASE 744-02

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	24.51	25.15	0.965	0.985
B	9.91	10.41	0.390	0.410
C	6.22	7.24	0.245	0.285
D	1.65	1.90	0.065	0.075
E	2.16	2.41	0.085	0.095
F	1.91	2.16	0.075	0.085
G	18.42 BSC		0.725 BSC	
H	—	—	—	—
J	0.08	0.18	0.003	0.007
K	2.29	2.79	0.090	0.110
L	12.55	12.85	0.494	0.506
N	9.91	10.42	0.415	0.435
P	—	—	—	—
Q	3.18	3.43	0.125	0.135
R	3.94	4.45	0.155	0.175
S	3.18	3.43	0.125	0.135
U	1.02	1.27	0.040	0.050
V	0.64	0.89	0.025	0.035

MRF392

**125 WATTS, 30–500 MHz
CONTROLLED "Q"
BROADBAND PUSH-PULL
RF POWER TRANSISTOR
NPN SILICON**



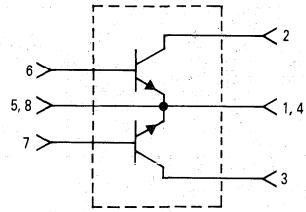
CASE 744A-01

The RF Line

NPN Silicon Push-Pull RF Power Transistor

. . . designed primarily for wideband large-signal output and driver amplifier stages in the 30–500 MHz frequency range.

- Specified 28 Volt, 400 MHz Characteristics —
  Output Power = 125 W
  Typical Gain = 10 dB
  Efficiency = 55% (Typ)
- Built-In Input Impedance Matching Networks for Broadband Operation
- Push-Pull Configuration Reduces Even Numbered Harmonics
- Gold Metallization System for High Reliability
- 100% Tested for Load Mismatch.



The MRF392 is two transistors in a single package with separate base and collector leads and emitters common. This arrangement provides the designer with a space saving device capable of operation in a push-pull configuration.

PUSH-PULL TRANSISTORS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	60	Vdc
Emitter-Base Voltage	V_{EBO}	4	Vdc
Collector Current — Continuous	I_C	16	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	270 1.54	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

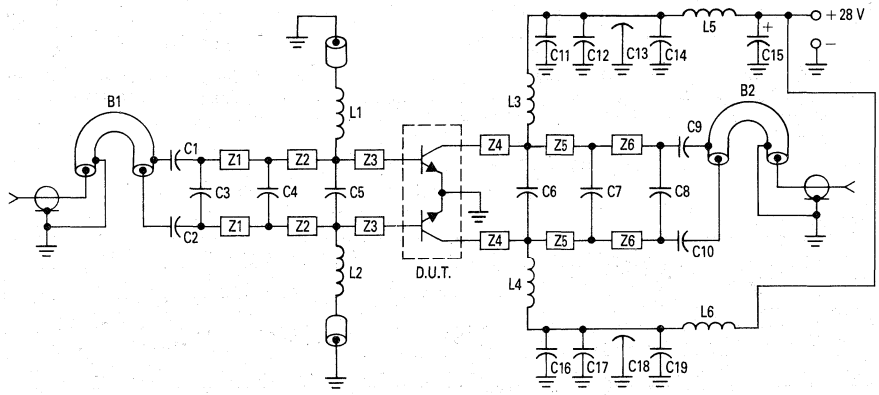
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.65	°C/W

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF push-pull amplifiers.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (NOTE 1)					
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 5 mAdc, I_C = 0)	$V_{(BR)EBO}$	4	—	—	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	—	5	mAdc
ON CHARACTERISTICS (NOTE 1)					
DC Current Gain (I_C = 1 Adc, V_{CE} = 5 Vdc)	h_{FE}	20	—	100	—
DYNAMIC CHARACTERISTICS (NOTE 1)					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1 MHz)	C_{ob}	—	75	115	pF
FUNCTIONAL TEST (NOTE 2 — See Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 125 W, f = 400 MHz)	G_{pe}	8	10	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 125 W, f = 400 MHz)	η	50	55	—	%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 125 W, f = 400 MHz VSWR = 30:1, all phase angles)	ψ	No Degradation in Output Power			

NOTES:
1. Each transistor chip measured separately.
2. Both transistor chips operating in push-pull amplifier.



C1, C2 — 240 pF, 100 Mil Chip Cap (ATC) or Equivalent
C3 — 3.6 pF, 100 Mil Chip Cap (ATC) or Equivalent
C4, C8 — 8.2 pF, 100 Mil Chip Cap (ATC) or Equivalent
C5, C6 — 20 pF, 100 Mil Chip Cap (ATC) or Equivalent
C7 — 18 pF, 100 Mil Chip Cap (ATC) or Equivalent
C9, C10 — 270 pF, 100 Mil Chip Cap (ATC) or Equivalent
C11, C12, C16, C17 — 470 pF 100 Mil Chip Cap (ATC) or Equivalent
C13, C18 — 680 pF Feedthru
C14, C19 — 0.1 μF Erie Redcap or Equivalent
C15 — 20 μF, 50 V

L1, L2 — 0.15 μH Molded Choke With Ferrite Bead
L3, L4 — 2-1/2 Turns #20 AWG, 0.200 ID
L5, L6 — 3-1/2 Turns #18 AWG, 0.200 ID

B1 — Balun, 50 Ω Semi-Rigid Coaxial Cable 86 Mil OD, 2" L
B2 — Balun, 50 Ω Semi-Rigid Coaxial Cable 86 Mil OD, 2" L

Z1 — Microstrip Line 270 Mil L x 125 Mil W
Z2 — Microstrip Line 375 Mil L x 125 Mil W
Z3 — Microstrip Line 280 Mil L x 125 Mil W
Z4 — Microstrip Line 300 Mil L x 125 Mil W
Z5 — Microstrip Line 350 Mil L x 125 Mil W
Z6 — Microstrip Line 365 Mil L x 125 Mil W

Board Material — 0.0625" Teflon Fiberglass ϵ_r = 2.5 ± 0.05 1 oz. Cu. CLAD, Double Sided

Figure 1. 400 MHz Test Fixture

3

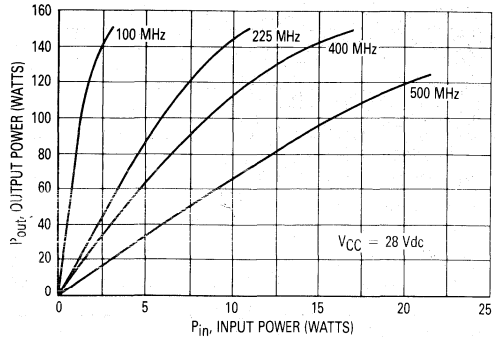


Figure 2. Output Power versus Input Power

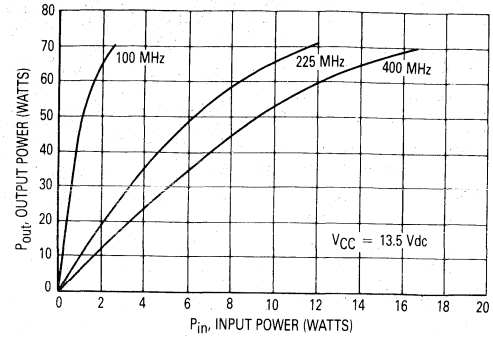


Figure 3. Output Power versus Input Power

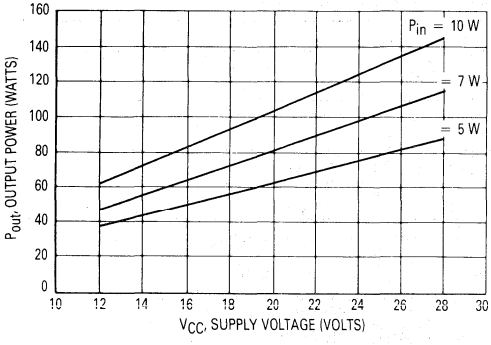


Figure 4. Output Power versus Supply Voltage — 225 MHz

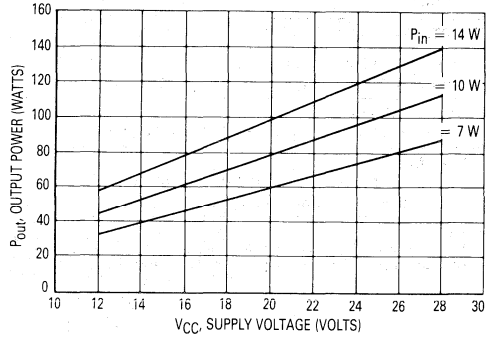
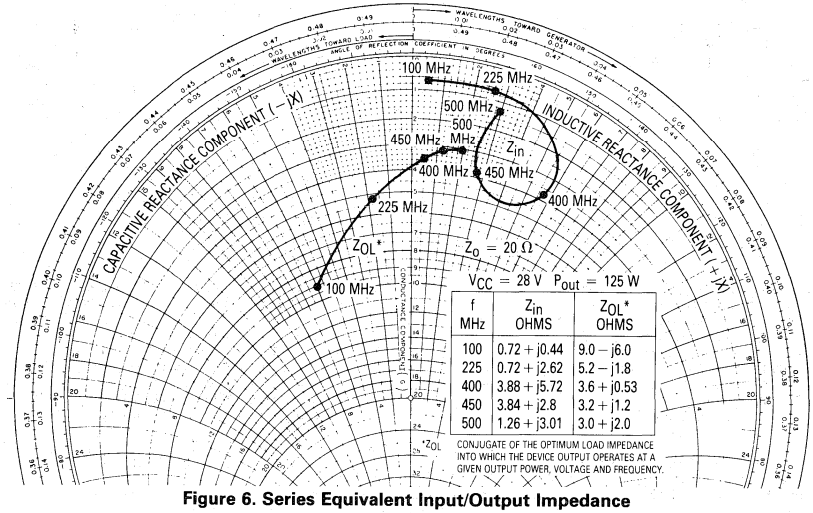
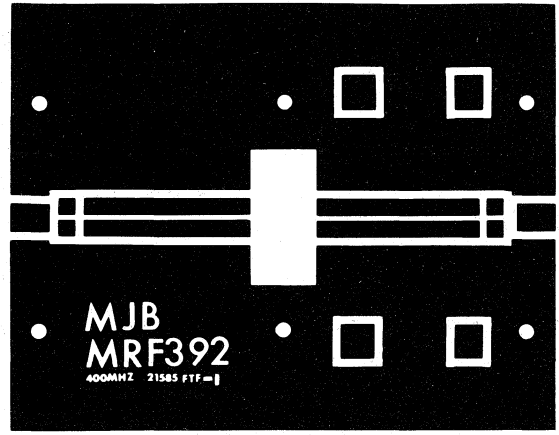


Figure 5. Output Power versus Supply Voltage — 400 MHz



f MHz	Z_{in} OHMS	Z_{OL}* OHMS
100	0.72 + j0.44	9.0 − j6.0
225	0.72 + j2.62	5.2 − j1.8
400	3.88 + j5.72	3.6 + j0.53
450	3.84 + j2.8	3.2 + j1.2
500	1.26 + j3.01	3.0 + j2.0

Figure 6. Series Equivalent Input/Output Impedance



NOTE: The Printed Circuit Board shown is 75% of the original.

Figure 7. Test Circuit Photomaster

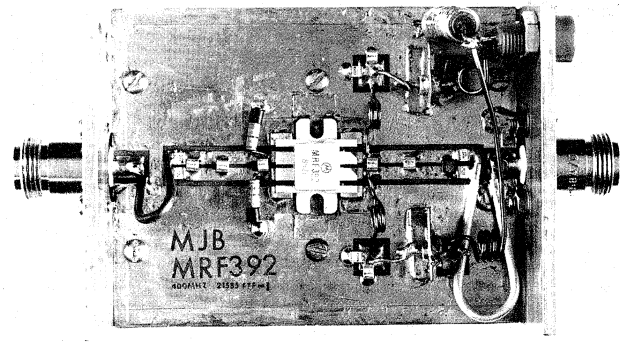
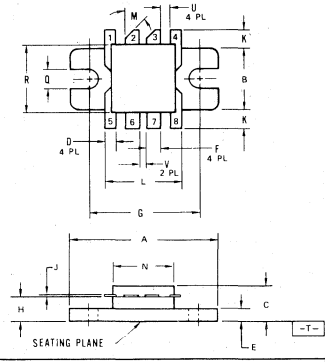


Figure 8. 400 MHz Test Circuit

OUTLINE DIMENSIONS



STYLE 1:
PIN 1. EMITTER (COMMON)
2. COLLECTOR
3. COLLECTOR
4. EMITTER (COMMON)
5. EMITTER (COMMON)
6. BASE
7. BASE
8. EMITTER (COMMON)

NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND -T- IS A DATUM SURFACE.
2. POSITIONAL TOLERANCE FOR SLOTS: ⌖ ø 0.76 (0.030) Ⓜ A Ⓜ B Ⓜ
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

CASE 744A-01

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.60	23.11	0.890	0.910
B	9.52	10.03	0.375	0.395
C	6.65	7.16	0.262	0.282
D	1.60	1.95	0.063	0.077
E	2.94	3.40	0.116	0.134
F	2.87	3.22	0.113	0.127
G	16.51 BSC		0.650 BSC	
H	4.01	4.36	0.158	0.172
J	0.07	0.15	0.003	0.006
K	4.34	4.90	0.171	0.193
L	12.44	12.95	0.490	0.510
M	45° NOM		45° NOM	
N	10.51	11.02	0.414	0.434
Q	3.04	3.35	0.120	0.132
R	9.90	10.41	0.390	0.410
U	1.02	1.27	0.040	0.050
V	0.64	0.89	0.025	0.035

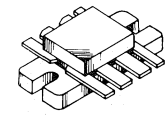
MRF393

The RF Line
NPN Silicon Push-Pull RF Power Transistor

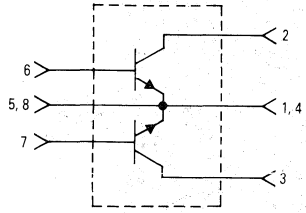
100 WATTS, 30–500 MHz
CONTROLLED "Q"
BROADBAND PUSH-PULL
RF POWER TRANSISTOR
NPN SILICON

. . . designed primarily for wideband large-signal output and driver amplifier stages in the 30–500 MHz frequency range.

- Specified 28 Volt, 500 MHz Characteristics —
  Output Power = 100 W
  Typical Gain = 9.5 dB (Class AB); 8.5 dB (Class C)
  Efficiency = 55% (Typ)
- Built-In Input Impedance Matching Networks for Broadband Operation
- Push-Pull Configuration Reduces Even Numbered Harmonics
- Gold Metallization System for High Reliability
- 100% Tested for Load Mismatch



CASE 744A-01



The MRF393 is two transistors in a single package with separate base and collector leads and emitters common. This arrangement provides the designer with a space saving device capable of operation in a push-pull configuration.

3

PUSH-PULL TRANSISTORS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	60	Vdc
Emitter-Base Voltage	V_{EBO}	4	Vdc
Collector Current — Continuous	I_C	16	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	270 1.54	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

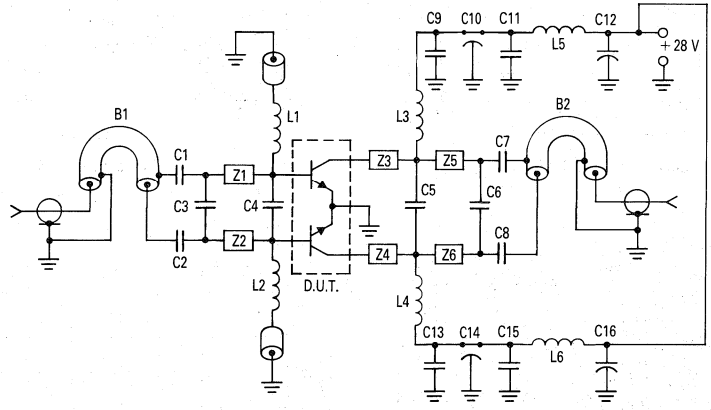
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.65	°C/W

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF push-pull amplifiers.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (NOTE 1)					
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 5 mAdc, I_C = 0)	$V_{(BR)EBO}$	4	—	—	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	—	5	mAdc
ON CHARACTERISTICS (NOTE 1)					
DC Current Gain (I_C = 1 Adc, V_{CE} = 5 Vdc)	h_{FE}	20	—	100	—
DYNAMIC CHARACTERISTICS (NOTE 1)					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1 MHz)	C_{ob}	—	75	115	pF
FUNCTIONAL TEST (NOTE 2 — See Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 100 W, f = 500 MHz)	G_{pe}	7.5	8.5	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 100 W, f = 500 MHz)	η	50	55	—	%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 100 W, f = 500 MHz VSWR = 30:1, all phase angles)	ψ	No Degradation in Output Power			

NOTES:
1. Each transistor chip measured separately.
2. Both transistor chips operating in push-pull amplifier.



C1, C2, C7, C8 — 240 pF 100 mil Chip Cap
C3 — 15 pF 100 mil Chip Cap
C4 — 24 pF 100 mil Chip Cap
C5 — 33 pF 100 mil Chip Cap
C6 — 12 pF 100 mil Chip Cap
C9, C13 — 1000 pF 100 mil Chip Cap
C10, C14 — 680 pF Feedthru Cap
C11, C15 — 0.1 μF Ceramic Disc Cap
C12, C16 — 50 μF 50 V

L1–L2 — 0.15 μH Molded Choke with Ferrite Bead
L3–L4 — 2-1/2 Turns #20 AWG 0.200" ID
L5–L6 — 3-1/2 Turns #18 AWG 0.200" ID

B1, B2 — Balun 50 Ω Semi Rigid Coax, 86 mil OD, 2" Long

Z1, Z2 — 850 mil Long x 125 mil W. Microstrip
Z3, Z4 — 200 mil Long x 125 mil W. Microstrip
Z5, Z6 — 800 mil Long x 125 mil W. Microstrip

Board Material — 0.0325" Teflon-Fiberglass, ϵ_r = 2.56, 1 oz. Copper Clad both sides.

Figure 1. 500 MHz Test Fixture

OUTPUT POWER versus INPUT POWER
CLASS C

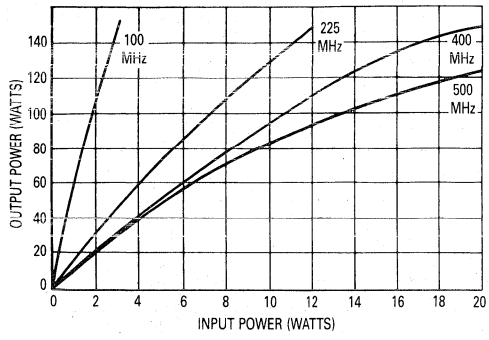


Figure 2. V_{CC} = 28 V

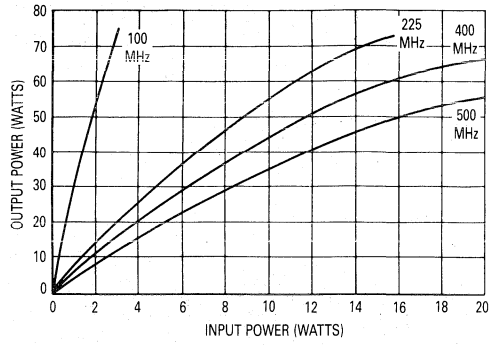


Figure 3. V_{CC} = 13.5 V

OUTPUT POWER versus SUPPLY VOLTAGE
CLASS C

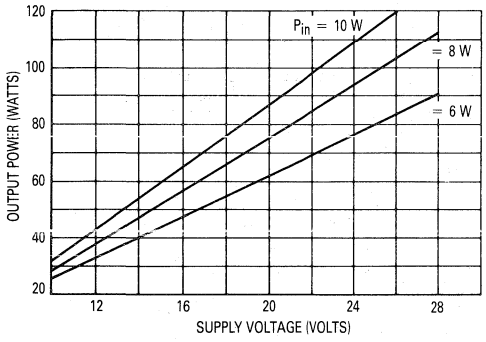


Figure 4. f = 225 MHz

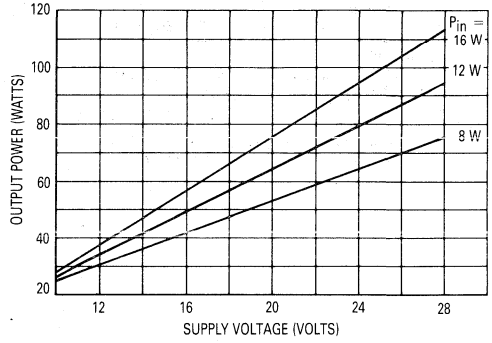
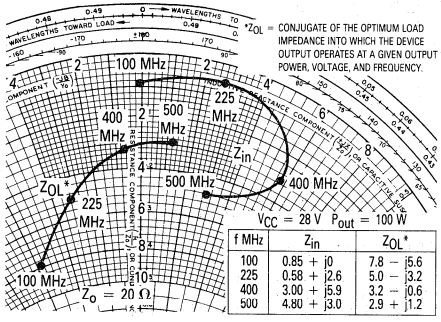


Figure 5. f = 500 MHz



f MHz	Z_{in}	Z_{OL}*
100	0.85 + j0	7.8 − j5.6
225	0.58 + j2.6	5.0 − j3.2
400	3.00 + j5.9	3.2 − j0.6
500	4.80 + j3.0	2.9 + j1.2

Figure 6. Series Equivalent Input/Output Impedance

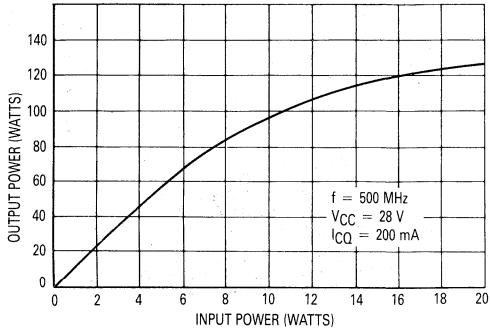
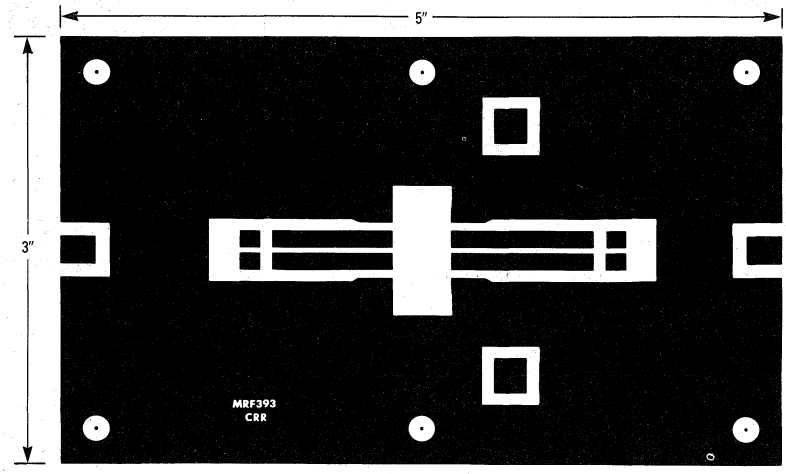


Figure 7. Class AB Output Power versus Input Power



NOTE: The Printed Circuit Board shown is 75% of the original.

Figure 8. Test Circuit Photomaster

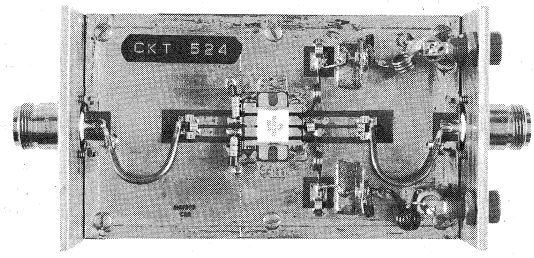
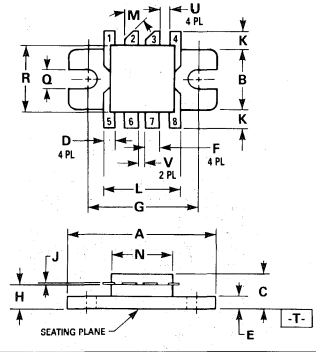


Figure 9. 500 MHz Test Circuit



OUTLINE DIMENSIONS

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. POSITIONAL TOLERANCE FOR SLOTS:
   ⌖ | ⌀ 0.76 (0.030) Ⓜ | A Ⓜ | B Ⓜ
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

CASE 744A-01

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.60	23.11	0.890	0.910
B	9.52	10.03	0.375	0.395
C	6.65	7.16	0.262	0.282
D	1.60	1.95	0.063	0.077
E	2.94	3.40	0.116	0.134
F	2.87	3.22	0.113	0.127
G	16.51 BSC		0.650 BSC	
H	4.01	4.36	0.158	0.172
J	0.07	0.15	0.003	0.006
K	4.34	4.90	0.171	0.193
L	12.44	12.95	0.490	0.510
M	45° NOM		45° NOM	
N	10.51	11.02	0.414	0.434
Q	3.04	3.35	0.120	0.132
R	9.90	10.41	0.390	0.410
U	1.02	1.27	0.040	0.050
V	0.64	0.89	0.025	0.035

MRF401

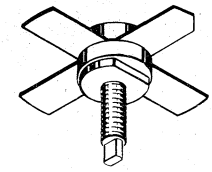
The RF Line

25 W PEP – 30 MHz
RF POWER
TRANSISTOR
NPN SILICON

NPN SILICON RF POWER TRANSISTORS

. . . designed primarily for applications as a high-power linear amplifier from 2.0 to 75 MHz.

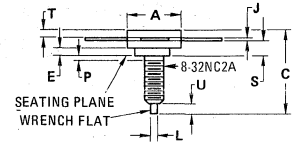
- Specified 28 Volt, 30 MHz Characteristics –
  Output Power = 25 W (PEP)
  Minimum Gain = 13 dB
  Efficiency = 40%
- Intermodulation Distortion at 25 W (PEP)
  IMD = -32 dB (Max)
- Isothermal-Resistor Design Results in Rugged Device

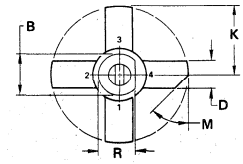


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current – Continuous	I_C	3.3	Adc
Total Device Dissipation @ $T_C = 25^oC$(1) Derate above 25^oC	P_D	50 0.286	Watts $W/^oC$
Storage Temperature Range	T_{stg}	−65 to +150	^oC

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as class B or C RF amplifiers.





STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	17.02	20.07	0.670	0.790
D	5.46	5.97	0.215	0.235
E	1.78	–	0.070	–
J	0.08	0.18	0.003	0.007
K	12.45	–	0.490	–
L	1.40	1.78	0.055	0.070
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.11	2.54	0.083	0.100
U	2.49	3.35	0.098	0.132

Case 145A-09

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	20	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 30 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	65	85	pF
FUNCTIONAL TEST (Figure 1)					
Common-Emitter Amplifier Power Gain (P_{out} = 25 Watts PEP, I_C (max) = 1.12 Adc, V_{CC} = 28 Vdc, f = 30 MHz)	G_{PE}	13	–	–	dB
Collector Efficiency (P_{out} = 25 Watts PEP, I_C (max) = 1.12 Adc, V_{CC} = 28 Vdc, f = 30 MHz)	η	40	–	–	%
Intermodulation Distortion (P_{out} = 25 Watts PEP, I_C = 1.12 Adc, V_{CC} = 28 Vdc, f_1 = 30 MHz, f_2 = 30.001 MHz)	IMD	–	–	-32	dB

3

FIGURE 1 – 30 MHz LINEAR TEST CIRCUIT

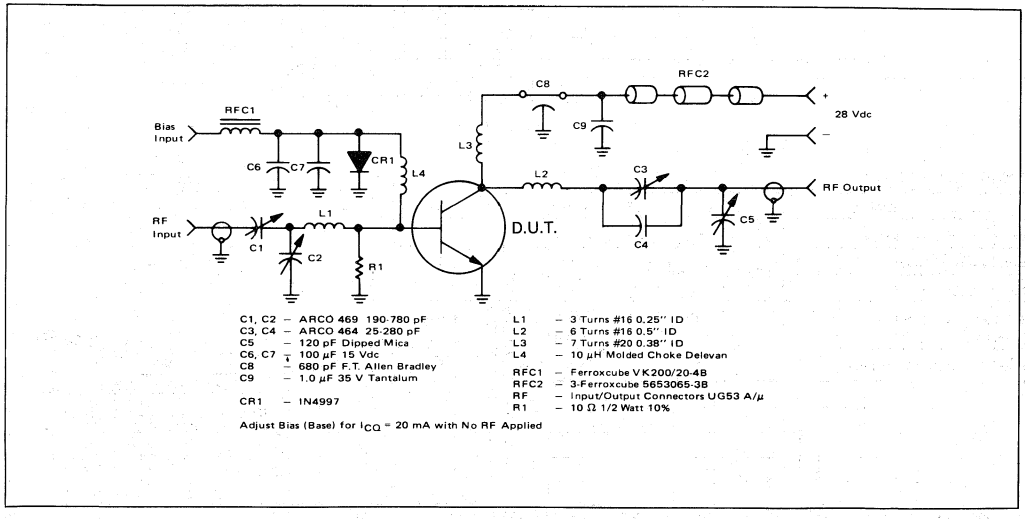


FIGURE 2 – PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

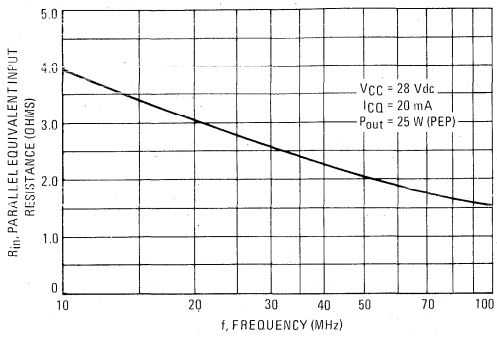


FIGURE 3 – PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

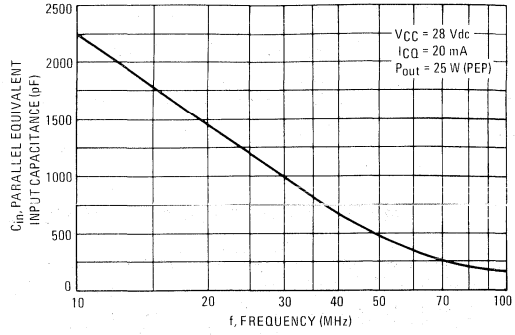


FIGURE 4 – PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY

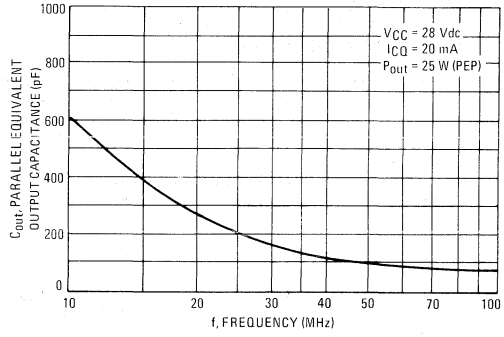


FIGURE 5 – POWER GAIN versus FREQUENCY

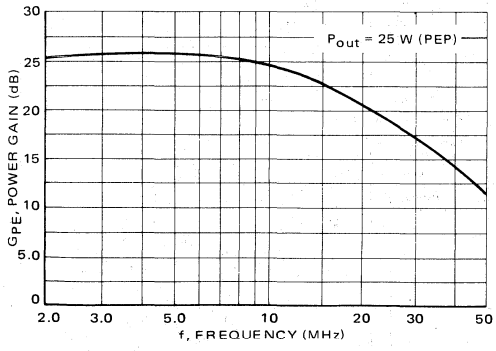
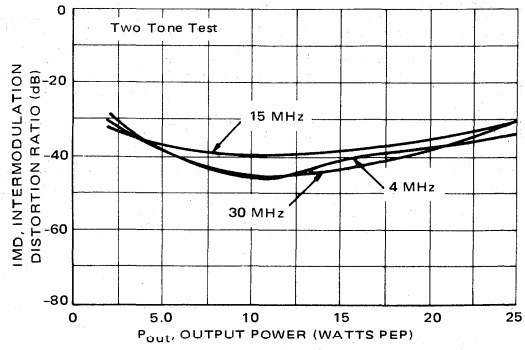


FIGURE 6 – IMD versus POWER OUTPUT



MRF406

The RF Line

20 W(PEP) — 30 MHz

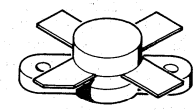
RF POWER TRANSISTOR

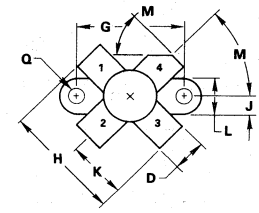
NPN SILICON

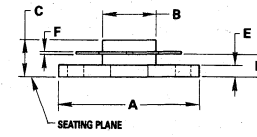
NPN SILICON RF POWER TRANSISTOR

. . . designed primarily for application as a power linear amplifier from 2.0 to 30 MHz.

- Specified 12.5 Volt, 30 MHz Characteristics —
  Output Power = 20 W(PEP)
  Minimum Gain = 12 dB
  Efficiency = 45%
- Intermodulation Distortion @ 20 W(PEP) —
  IMD = -30 dB (Min)
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR







STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CBO}	40	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	4.0	Adc
Withstand Current (t = 5.0 s)	—	12	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	80 0.46	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.2	°C/W

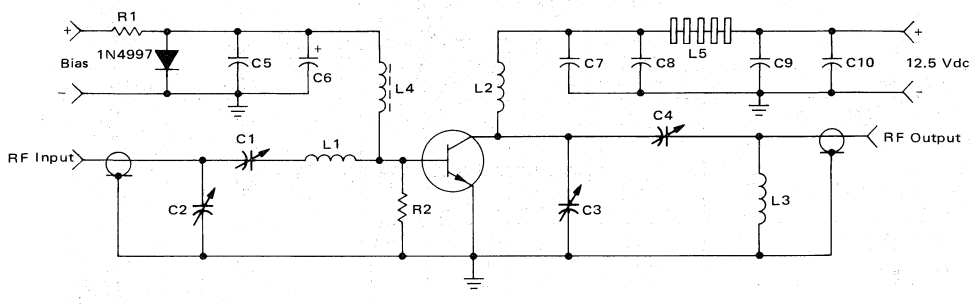
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	9.40	9.91	0.370	0.390
C	5.82	7.14	0.229	0.281
D	5.46	5.97	0.215	0.235
E	2.16	2.67	0.085	0.105
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	20.07	20.57	0.790	0.810
K	10.03	10.29	0.395	0.405
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.81	4.57	0.150	0.180
Q	2.87	3.30	0.113	0.130

CASE 211-07

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	40	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 50 mAdc, I_E = 0)	$V_{(BR)CBO}$	40	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 12.5 Vdc, V_{BE} = 0)	I_{CES}	–	–	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	35	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	150	200	pF
FUNCTIONAL TESTS (Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 20 W(PEP), $I_{C(max)}$ = 1.75 Adc, I_{CQ} = 25 mAdc, f = 30, 30.001 MHz)	G_{PE}	12	15	–	dB
Power Output (V_{CE} = 12.5 Vdc, f = 30 MHz)	P_{out}	20	–	–	Watts (PEP)
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 20 W(PEP), $I_{C(max)}$ = 1.75 Adc, I_{CQ} = 25 mAdc, f = 30, 30.001 MHz)	η	45	–	–	%
Intermodulation Distortion (V_{CE} = 12.5 Vdc, P_{out} = 20 W(PEP), $I_{C(max)}$ = 1.75 Adc, I_{CQ} = 25 Adc, f = 30, 30.001 MHz)	IMD	−30	−35	–	dB
Load Mismatch (V_{CC} = 12.5 Vdc, P_{out} = 20 W(PEP), I_C = 1.75 Adc, I_{CQ} = 25 mAdc, f = 30, 30.001 MHz)	–	> 30:1 All Phase Angles			–

FIGURE 1 – 30 MHz TEST CIRCUIT SCHEMATIC



C1, C2, C4	ARCO 466	L1	0.15 μH, Molded Choke
C3	ARCO 469	L2	15 Turns of #20 AWG Enameled Wire, 1/4" I.D., Close Wound
C5, C8, C9	0.1 μF Disc Ceramic	L3	4 Turns of #18 AWG Wire, 5/16" I.D., 3/8" Long.
C6	1000 μF, 3 V Electrolytic	L4	10 μH, Molded Choke
C7	1000 pF, UNELCO	L5	5 Ferrite Beads, FERROXCUBE #56-590-65/3B
C10	100 μF, 15 V Electrolytic		
R1	100 Ohm, 25 W, Wire Wound		
R2	10 Ohm, ½ W, Carbon		

FIGURE 2 – OUTPUT POWER versus INPUT POWER

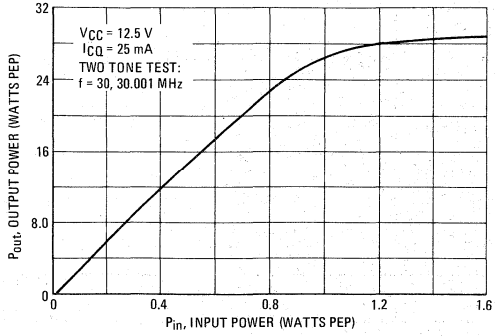


FIGURE 3 – OUTPUT POWER versus SUPPLY VOLTAGE

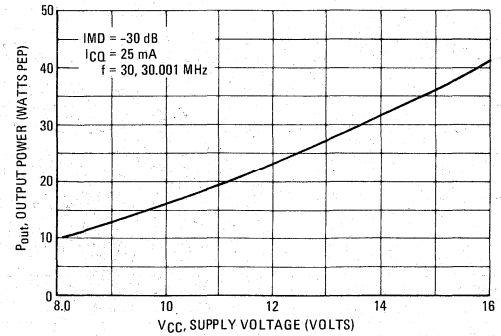


FIGURE 4 – POWER GAIN versus FREQUENCY

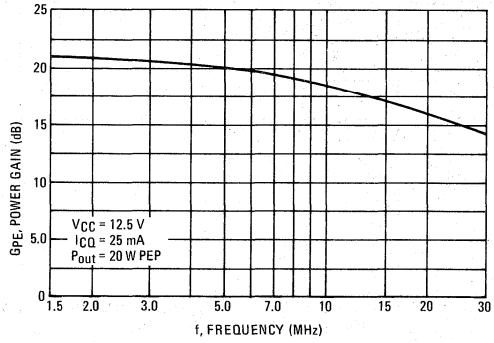


FIGURE 5 – INTERMODULATION DISTORTION versus OUTPUT POWER

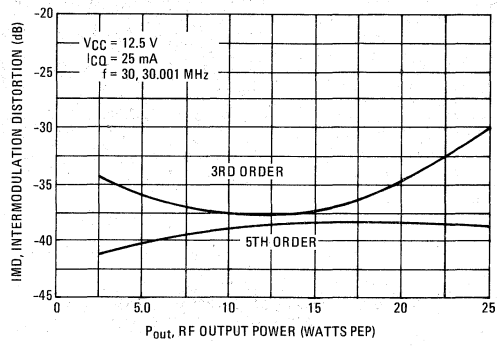


FIGURE 6 – DC SAFE OPERATING AREA

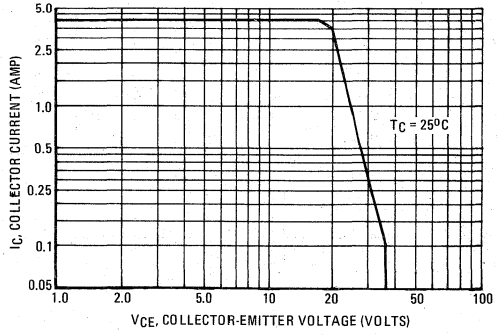


FIGURE 7 – SERIES EQUIVALENT IMPEDANCE

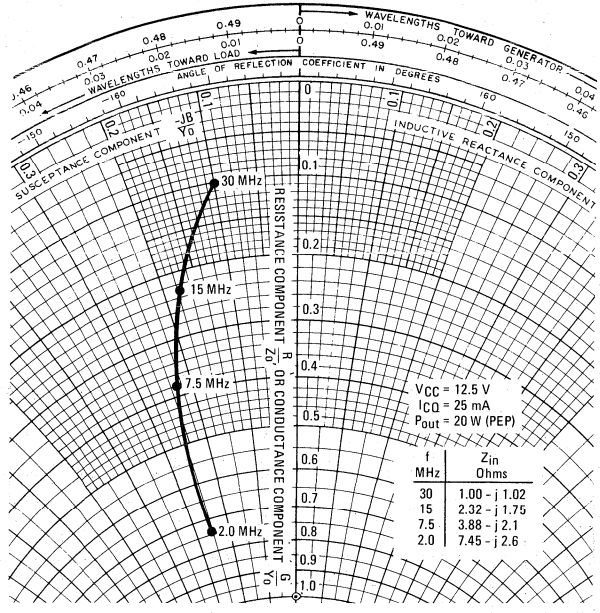


FIGURE 8 – PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY

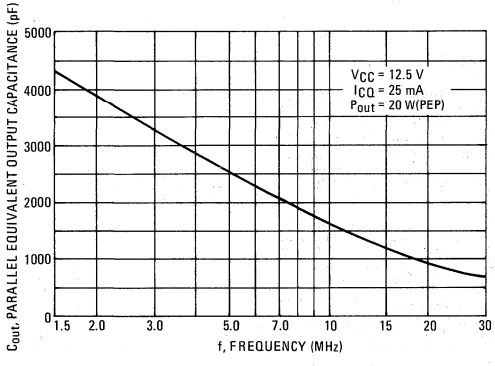
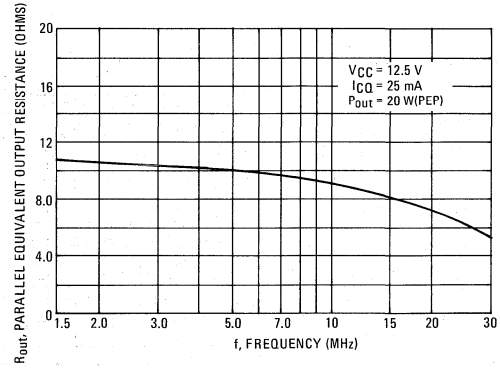


FIGURE 9 – PARALLEL EQUIVALENT OUTPUT RESISTANCE versus FREQUENCY



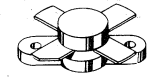
MRF410
MRF410A

The RF Line
NPN Silicon
RF Power Transistors

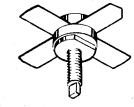
10 W–30 MHz
RF POWER
TRANSISTORS
NPN SILICON

. . . designed for high gain driver and output linear amplifier stages in 1.5 to 30 MHz HF/SSB equipment.

- Specified 28 Volt, 30 MHz Characteristics —
  Output Power = 10 W
  Minimum Gain = 13 dB
  Efficiency = 40%
- Intermodulation Distortion @ 10 W (PEP) —
  IMD = −30 dB (Max)
- 100% Tested for Load Mismatch at All Phase Angles With 30:1 VSWR
- Direct Replacement for 2N6370



MRF410
CASE 211-07



MRF410A
CASE 145A-09

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	35	Vdc
Collector-Base Voltage	V_{CBO}	65	Vdc
Emitter-Base Voltage	V_{EBO}	4	Vdc
Collector Current — Continuous	I_C	1.5	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	40 0.23	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.35	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	35	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 50 mAdc, I_E = 0)	$V_{(BR)CES}$	65	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4	—	—	Vdc
Collector Cutoff Current (V_{CE} = 28 Vdc, V_{BE} = 0)	I_{CES}	—	—	5	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1 Adc, V_{CE} = 5 Vdc)	h_{FE}	10	35	100	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1 MHz)	C_{ob}	—	85	100	pF

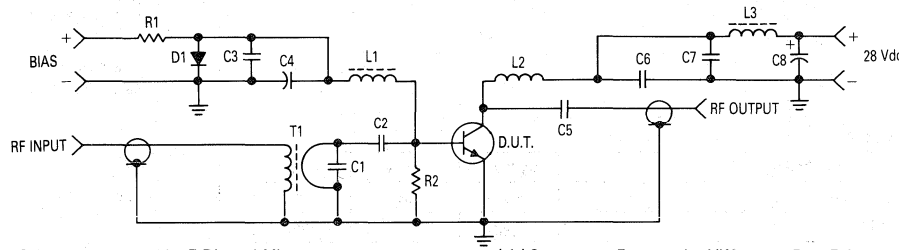
(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (SSB)					
Common-Emitter Amplifier Gain (V_{CC} = 28 Vdc, P_{out} = 10 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 25 mA)	G_{PE}	13	16	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 10 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 25 mA)	η	40	—	—	%
Intermodulation Distortion (1) (V_{CC} = 28 Vdc, P_{out} = 10 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 25 mA)	$IMD_{(d3)}$	—	−35	−30	dB
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 10 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 25 mA, VSWR 30:1 at All Phase Angles)		No Degradation in Output Power			
CLASS A PERFORMANCE					
Power Gain and Intermodulation Distortion (1) (V_{CC} = 28 Vdc, P_{out} = 4 W (PEP), I_{CQ} = 500 mA, f1 = 30 MHz, f2 = 30.001 MHz)	G_{PE} $IMD_{(d3)}$ $IMD_{(d5)}$	— — —	17 40 65	— — —	dB dB dB

(1) To MIL-STD-1311 Version A, Test Method 2204B, Two Tone, Reference each tone.



C1 — 1300 pF Dipped Mica
C2,C3,C5,C6 — 0.1 μF Type 1812 Chip or Equivalent
C4 — 100 μF/16 V Electrolytic
C7 — 0.01 μF Type 1812 Chip or Equivalent
C8 — 10 μF/35 V Electrolytic
R1 — 5 Ohms/5 W
R2 — 10 Ohms/½ W Carbon
D1 — MR820–826 or Equivalent
L1,L3 — Ferroxcube VK200 10/3B or Fair-Rite Products Corporation 2843003102
L2 — 15 Turns #22 AWG Enameled Wire, Close Wound, ¼" ID
T1 — RF Transformer 9:1 Impedance Ratio. See Motorola Application Note AN749, Figure 4 for Details. Ferrite Material: 2 each Fair-Rite Products Corporation 2643006801

Figure 1. 30 MHz Test Circuit

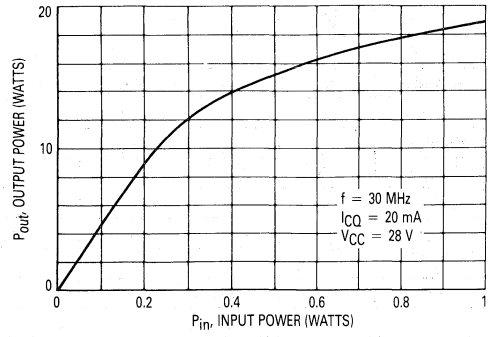


Figure 2. Output Power versus Input Power

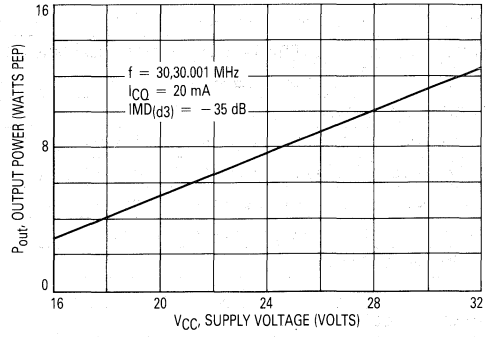


Figure 3. Output Power versus Supply Voltage

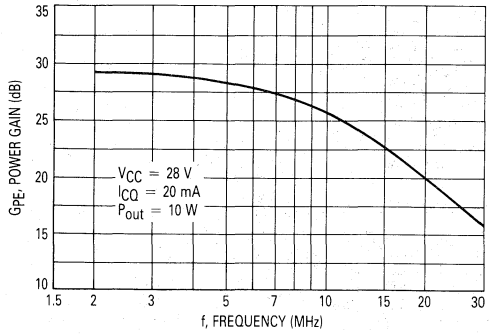


Figure 4. Power Gain versus Frequency

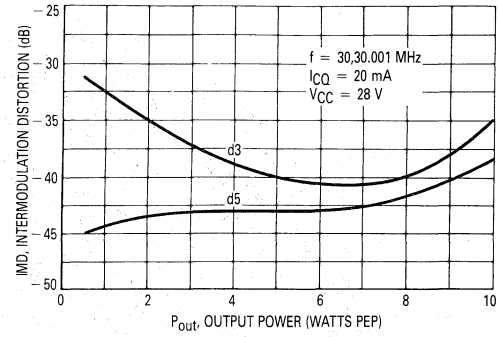


Figure 5. Intermodulation Distortion versus Output Power

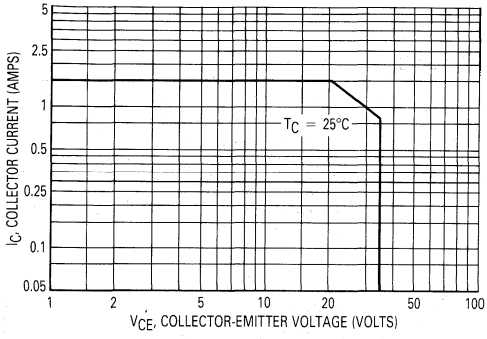


Figure 6. D.C. Safe Operating Area

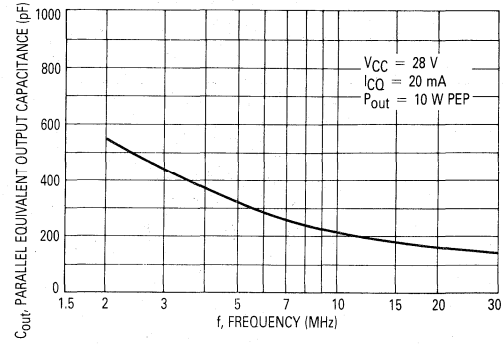


Figure 7. Output Capacitance versus Frequency

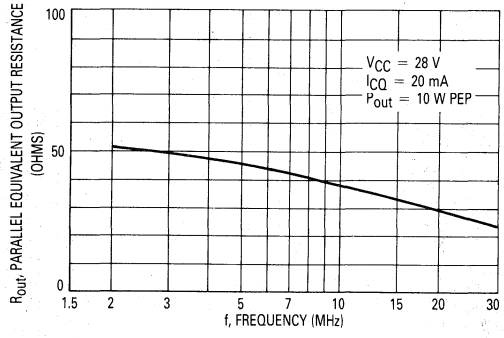


Figure 8. Output Resistance versus Frequency

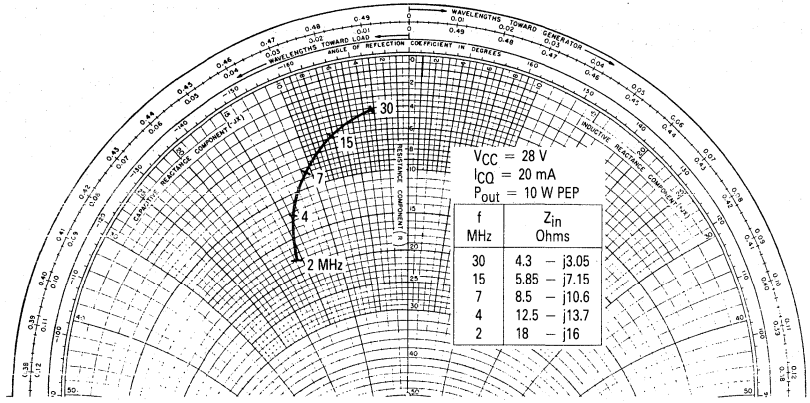
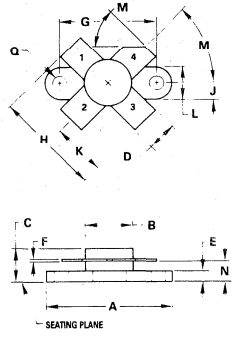


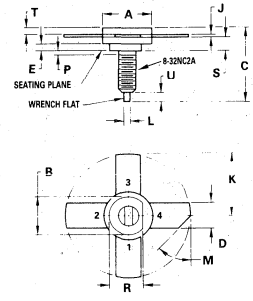
Figure 9. Series Equivalent Input Impedance

OUTLINE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	9.40	9.91	0.370	0.390
C	5.82	7.14	0.229	0.281
D	5.46	5.97	0.215	0.235
E	2.16	2.67	0.085	0.105
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	20.07	20.57	0.790	0.810
K	10.03	10.29	0.395	0.405
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.81	4.57	0.150	0.180
Q	2.87	3.30	0.113	0.130

CASE 211-07



STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	17.02	20.07	0.670	0.790
D	5.46	5.97	0.215	0.235
E	1.78	—	0.070	—
J	0.08	0.18	0.003	0.007
K	12.45	—	0.490	—
L	1.40	1.78	0.055	0.070
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.11	2.54	0.083	0.100
U	2.49	3.35	0.098	0.132

CASE 145A-09

MRF412

The RF Line

70 W (PEP) — 30 MHz

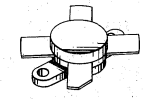
RF POWER TRANSISTOR

NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed primarily for applications as a high-power amplifier from 2.0 to 30 MHz, in single sideband mobile, marine and base station equipment where superior ruggedness is required.

- Specified 13.6 V, 30 MHz Characteristics —
  Output Power = 70 W PEP or CW
  Minimum Gain = 13 dB
  Efficiency = 40%
  Intermodulation Distortion d_3 = -33 dB Typ
- Guaranteed Ruggedness @ 3.0 dB Overdrive and 15.5 V Supply



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Continuous	I_C	20	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	250 1.43	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

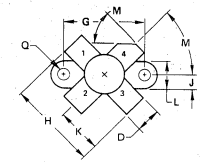
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	0.7	°C/W

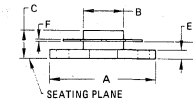
(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.
(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

MATCHING PROCEDURE

In the push-pull circuit configuration it is preferred that the transistors are used as matched pairs to obtain optimum performance.

The matching procedure used by Motorola consists of measuring h_{FE} at the data sheet conditions and color coding the device to predetermined h_{FE} ranges within the normal h_{FE} limits. A color dot is added to the marking on top of the cap. Any two devices with the same color dot can be paired together to form a matched set of units.





STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	9.40	9.91	0.370	0.390
C	5.82	7.14	0.229	0.281
D	5.46	5.97	0.215	0.235
E	2.16	2.67	0.085	0.105
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	20.07	20.57	0.790	0.810
K	10.03	10.28	0.395	0.405
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.81	4.57	0.150	0.180
Q	2.87	3.30	0.113	0.130

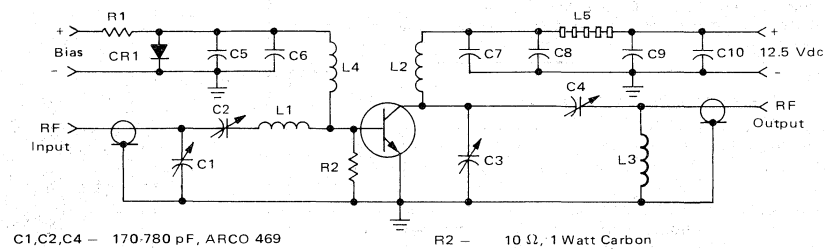
CASE 211-11

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 13.6 Vdc, V_{BE} = 0)	I_{CES}	—	—	20	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	—	150	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	—	450	pF
FUNCTIONAL TESTS (SSB)					
Common-Emitter Amplifier Power Gain (V_{CC} = 13.6 Vdc, P_{out} = 70 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 100 mA)	G_{PE}	13	16	—	dB
Collector Efficiency (V_{CC} = 13.6 Vdc, P_{out} = 70 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 100 mA)	η	40	—	—	%
Intermodulation Distortion (1) (PEP) (V_{CC} = 13.6 Vdc, P_{out} = 70 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 100 mA)	$IMD_{(d3)}$	—	-33	-28	dB
Load Mismatch (V_{CC} = 15.5 Vdc, P_{in} = 7.0 W (CW), f = 30 MHz, VSWR = 30:1 All Angles)	ψ	No Degradation in Output Power			

(1) To MIL-STD-1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.

FIGURE 1 — 30-MHz TEST CIRCUIT



C1,C2,C4 — 170-780 pF, ARCO 469
C3 — 80-480 pF, ARCO 466
C5,C7,C10 — ERIE 0.1 μF, 100 V
C6 — MALLORY 500 μF @ 15 V Electrolytic
C9 — 100 μF, 15 V Electrolytic
C8 — 1000 pF, 350 V UNDERWOOD
R1 — 10 Ω, 25 Watt Wirewound
R2 — 10 Ω, 1 Watt Carbon
CR1 — IN4997
L1 — 3 Turns, #16 Wire, 5/16" I.D., 5/16" Long
L2 — 12 Turns, #16 Enamaled Wire Closewound, 1/4" I.D.
L3 — 1 3/4 Turns, 1/8" Tubing, 3/8" I.D., 3/8" Long
L4 — 10 μH Molded Choke
L5 — 10 Ferrite Beads - FERROXCUBE #56-590-65/3B

FIGURE 2 – OUTPUT POWER versus INPUT POWER

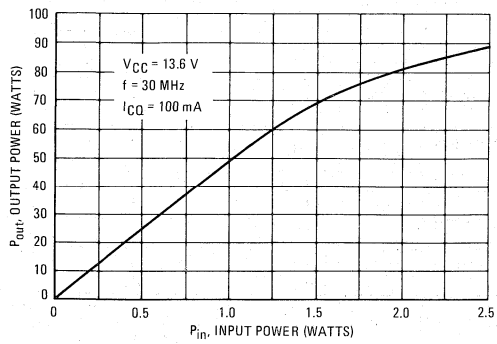


FIGURE 3 – POWER GAIN versus FREQUENCY

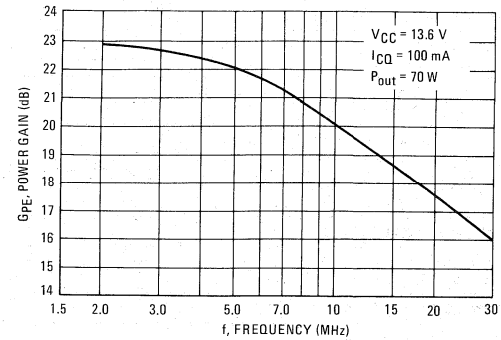


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

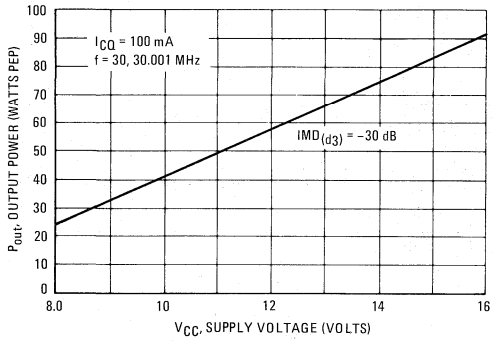


FIGURE 5 – INTERMODULATION DISTORTION versus OUTPUT POWER

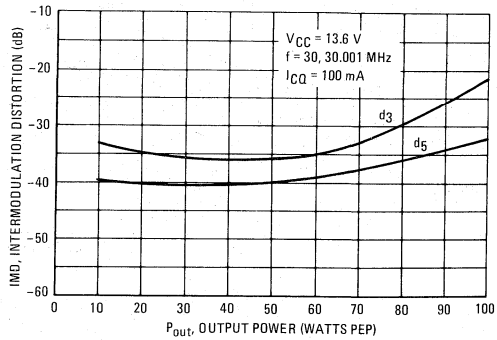


FIGURE 6 – OUTPUT CAPACITANCE versus FREQUENCY

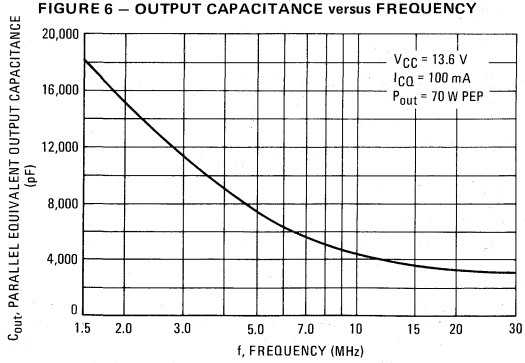


FIGURE 7 – OUTPUT RESISTANCE versus FREQUENCY

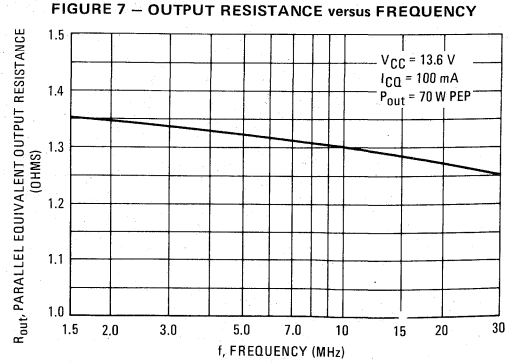


FIGURE 8 – SAFE OPERATING AREA

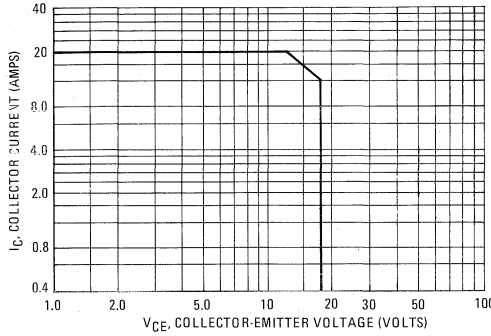
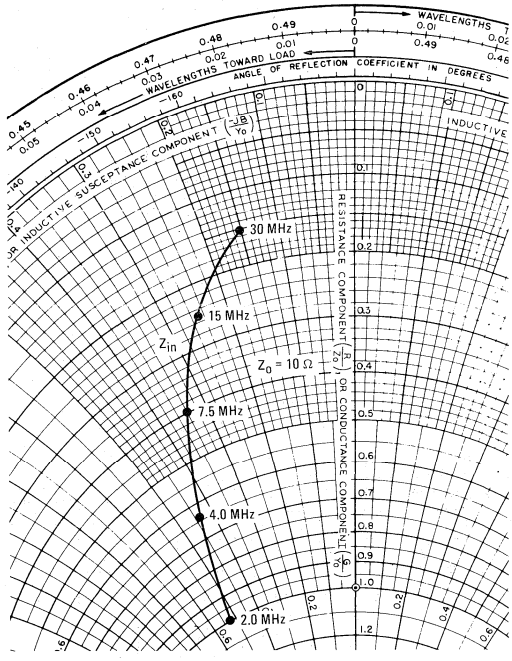


FIGURE 9 – SERIES INPUT IMPEDANCE



V_{CC} = 13.6 V
I_{CQ} = 100 mA
P_{out} = 70 W PEP

f MHz	Z_{in} Ohms
30	1.5 – j1.5
15	2.4 – j2.6
7.5	4.0 – j3.4
4.0	6.3 – j4.6
2.0	9.9 – j5.3

MRF421
MRF421MP

The RF Line

100 W(PEP) — 30 MHz

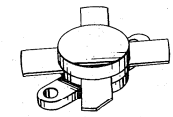
RF POWER TRANSISTORS

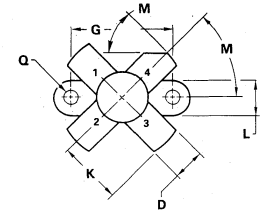
NPN SILICON

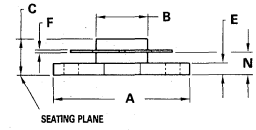
NPN SILICON RF POWER TRANSISTOR

. . . designed primarily for application as a high-power linear amplifier from 2.0 to 30 MHz.

- Specified 12.5 Volt, 30 MHz Characteristics —
  Output Power = 100 W(PEP)
  Minimum Gain = 10 dB
  Efficiency = 40%
- Intermodulation Distortion @ 100 W (PEP) —
  IMD = -30 dB (Min)
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR







STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	11.81	12.95	0.465	0.510
C	5.82	6.98	0.229	0.275
D	5.46	5.97	0.216	0.235
E	2.13	2.79	0.084	0.110
F	0.08	0.18	0.003	0.007
G	18.29	18.54	0.720	0.730
K	11.05	—	0.435	—
L	6.22	6.48	0.246	0.255
M	45° NOM		45° NOM	
N	3.66	4.52	0.144	0.178
Q	2.92	3.30	0.115	0.130

CASE 211-11

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CBO}	45	Vdc
Emitter-Base Voltage	V_{EBO}	3.0	Vdc
Collector Current — Continuous	I_C	20	Adc
Withstand Current — 10 s	—	30	Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	290 1.66	Watts $W/^oC$
Storage Temperature Range	T_{stg}	−65 to +150	^oC

MRF421MP is for ordering an h_{FE} matched pair.

THERMAL CHARACTERISTICS

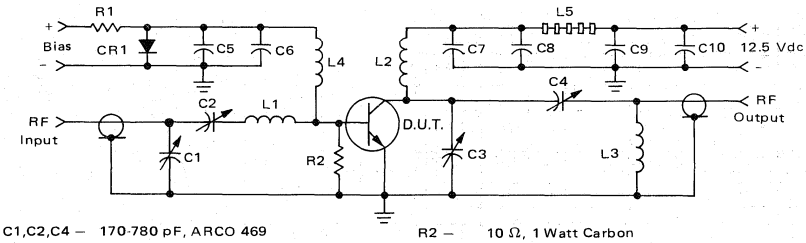
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.6	$^oC/W$

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 200 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	45	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 200 mAdc, I_E = 0)	$V_{(BR)CBO}$	45	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 16 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	–	–	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	30	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	650	800	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 100 W, $I_{C(max)}$ = 10 Adc, I_{CQ} = 150 mAdc, f = 30, 30.001 MHz)	G_{PE}	10	12	–	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 100 W, $I_{C(max)}$ = 10 Adc, I_{CQ} = 150 mA, f = 30, 30.001 MHz)	η	40	–	–	%
Intermodulation Distortion (1) (V_{CE} = 12.5 Vdc, P_{out} = 100 Watts, I_C = 10 Adc, I_{CQ} = 150 mA, f = 30, 30.001 MHz)	IMD	–	-33	-30	dB

(1) To proposed EIA measurement technique.

FIGURE 1 – 30 MHz TEST CIRCUIT SCHEMATIC



C1,C2,C4 – 170-780 pF, ARCO 469
C3 – 80-480 pF, ARCO 466
C5,C7,C10 – ERIE 0.1 μF, 100 V
C6 – MALLORY 500 μF @ 15 V Electrolytic
C9 – 100 μF, 15 V Electrolytic
C8 – 1000 pF, 350 V UNDERWOOD
R1 – 10 Ω, 25 Watt Wirewound
R2 – 10 Ω, 1 Watt Carbon
CR1 – IN4997
L1 – 3 Turns, #16 Wire, 5/16" I.D., 5/16" Long
L2 – 12 Turns, #16 Enamaled Wire Closewound, 1/4" I.D.
L3 – 1 3/4 Turns, 1/8" Tubing, 3/8" I.D., 3/8" Long
L4 – 10 μH Molded Choke
L5 – 10 Ferrite Beads - FERROXCUBE #56-590-65/3B

FIGURE 2 – OUTPUT POWER versus INPUT POWER

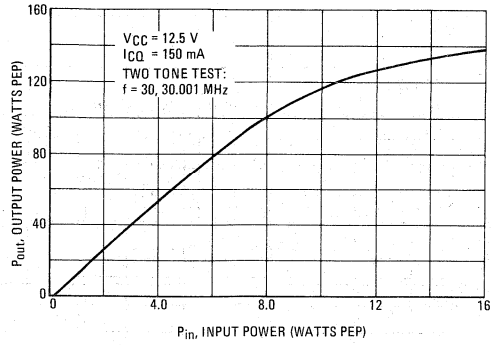


FIGURE 3 – OUTPUT POWER versus SUPPLY VOLTAGE

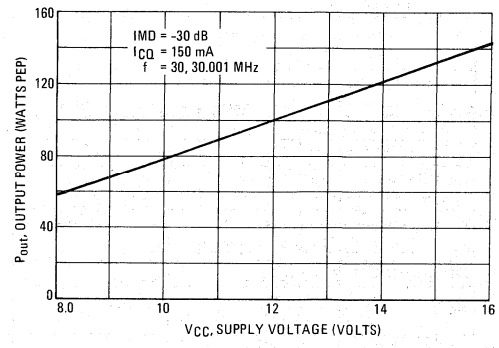


FIGURE 4 – POWER GAIN versus FREQUENCY

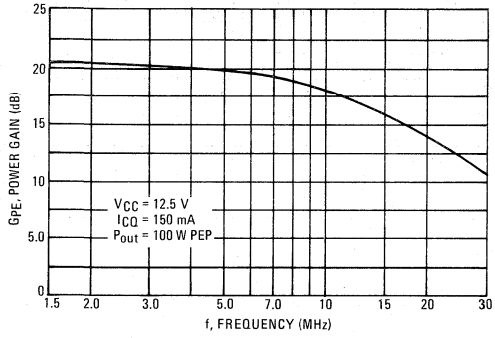


FIGURE 5 – INTERMODULATION DISTORTION versus OUTPUT POWER

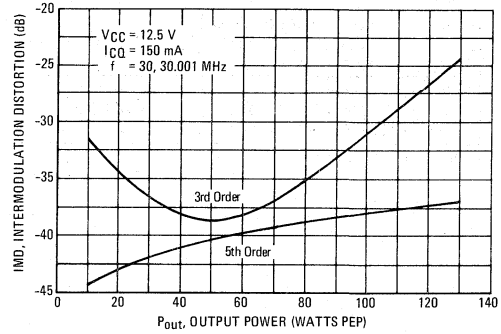


FIGURE 6 – DC SAFE OPERATING AREA

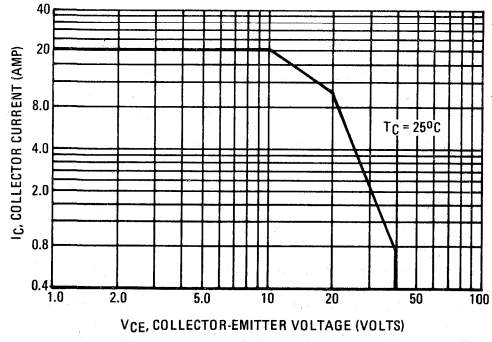
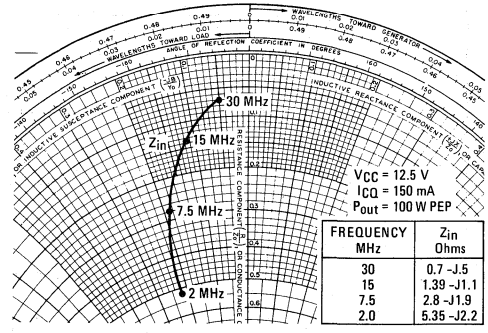


FIGURE 7 – SERIES EQUIVALENT IMPEDANCE



FREQUENCY MHz	Zin Ohms
30	0.7 -J.5
15	1.39 -J1.1
7.5	2.8 -J1.9
2.0	5.35 -J2.2

FIGURE 8 – OUTPUT CAPACITANCE versus FREQUENCY

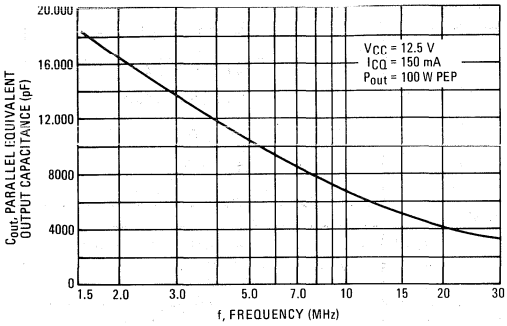
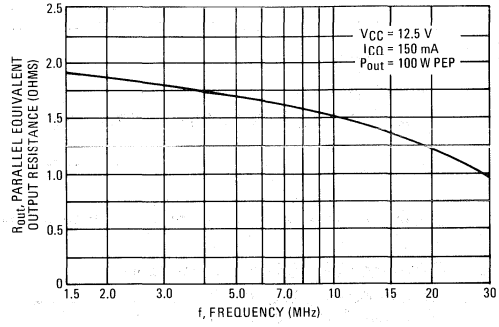


FIGURE 9 – OUTPUT RESISTANCE versus FREQUENCY



MRF422
MRF422MP

The RF Line

NPN SILICON RF POWER TRANSISTOR

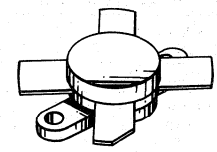
. . . designed primarily for applications as a high-power linear amplifier from 2.0 to 30 MHz.

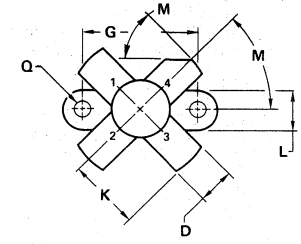
- Specified 28 Volt, 30 MHz Characteristics –
  Output Power = 150 W(PEP)
  Minimum Gain = 10 dB
  Efficiency = 40%
- Intermodulation Distortion @ 150 W(PEP) –
  IMD = -30 dB (Min)
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR

150 W(PEP) – 30 MHz

RF POWER TRANSISTOR

NPN SILICON





STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	11.81	12.95	0.465	0.510
C	5.82	6.98	0.229	0.275
D	5.46	5.97	0.216	0.235
E	2.13	2.79	0.084	0.110
F	0.08	0.18	0.003	0.007
G	18.29	18.54	0.720	0.730
K	11.05	–	0.435	–
L	6.22	6.48	0.246	0.255
M	45° NOM		45° NOM	
N	3.66	4.52	0.144	0.178
Q	2.92	3.30	0.115	0.130

CASE 211-11

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CBO}	85	Vdc
Emitter-Base Voltage	V_{EBO}	3.0	Vdc
Collector Current – Continuous	I_C	20	Adc
Withstanding Current – 10 s	–	30	Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	290 1.66	Watts $W/^oC$
Storage Temperature Range	T_{stg}	−65 to +150	^oC

MRF422MP is for ordering a HFE matched pair.

THERMAL CHARACTERISTICS

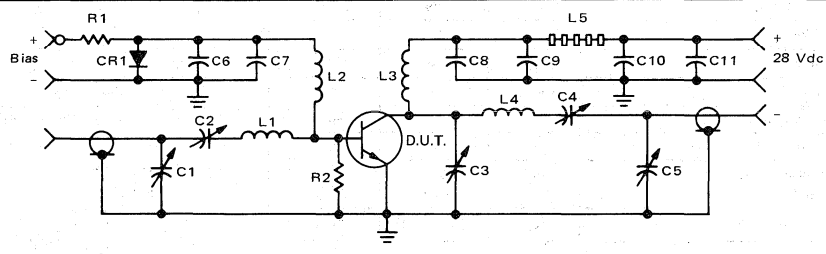
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.6	$^oC/W$

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 200 mAdc, I_B = 0)	$V_{(BR)CEO}$	35	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	85	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 mAdc, I_E = 0)	$V_{(BR)CBO}$	85	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 28 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	–	–	20	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	30	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	420	–	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 150 W(PEP), $I_{C(max)}$ = 6.7 Adc, I_{CQ} = 150 mAdc, f = 30, 30.001 MHz)	G_{PE}	10	13	–	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 150 W(PEP), $I_{C(max)}$ = 6.7 Adc, I_{CQ} = 150 mAdc, f = 30, 30.001 MHz)	η	–	45	–	%
Intermodulation Distortion * (V_{CE} = 28 Vdc, P_{out} = 150 Watts(PEP), I_C = 6.7 Adc, I_{CQ} = 150 mAdc, f = 30, 30.001 MHz)	IMD	—	-33	-30	dB
Output Power (V_{CE} = 28 Vdc, f = 30 MHz)	P_{out}	150	–	–	Watts PEP

*To Mil Std 1311 Version A, Test Method 2204, Two Tone, Reference each Tone.

FIGURE 1 – 30 MHz TEST CIRCUIT SCHEMATIC



C1,2,3,5 — 170-680 pF, ARCO 469
C4 — 80-480 pF, ARCO 466
C6,8,11 — ERIE 0.1 μF, 100 V
C7 — MALLORY 500 μF, 15 V Electrolytic
C9 — UNDERWOOD 1000 pF, 350 V
C10 — 10 μF, 50 V Electrolytic
R1 — 10 Ω, 25 Watt Wire Wound
R2 — 10 Ω, 1 Watt Carbon
CR1 — 1N4997

L1 — 3 Turns, #16 Wire, 5/16" I.D., 5/16" Long
L2 — 10 μH Molded Choke
L3 — 12 Turns, #16 Enamaled Wire, Close Wound, 1/4" Dia.
L4 — 5 turns, 1/8" Copper Tubing
L5 — 10 Ferrite Beads — FERROXCUBE #56-590-65/3B

FIGURE 2 – OUTPUT POWER versus INPUT POWER

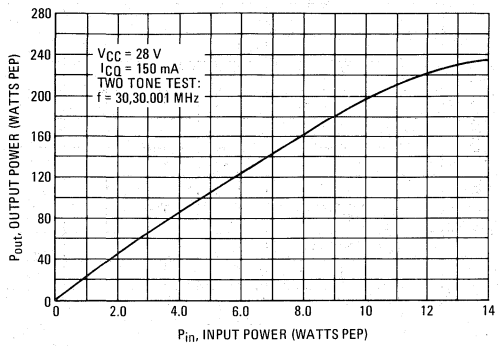


FIGURE 3 – POWER GAIN versus FREQUENCY

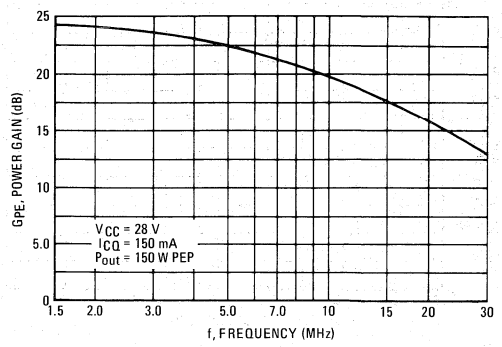


FIGURE 4 – LINEAR OUTPUT POWER versus SUPPLY VOLTAGE

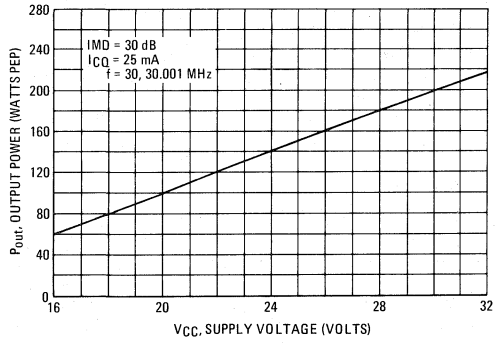


FIGURE 5 – INTERMODULATION DISTORTION versus OUTPUT POWER

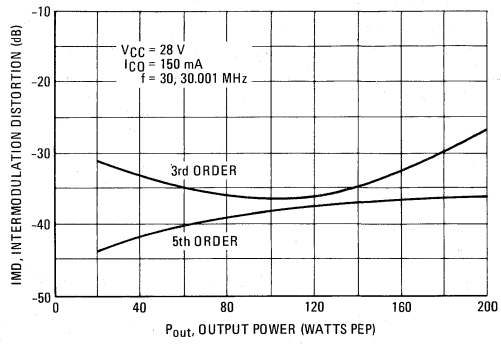


FIGURE 6 – DC SAFE OPERATING AREA

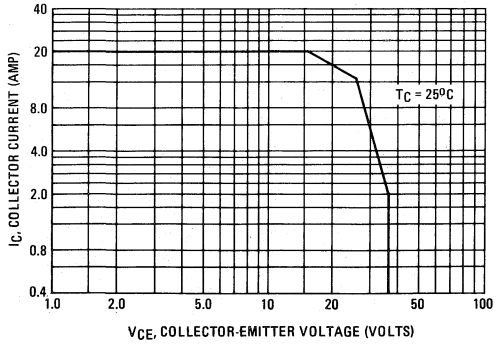
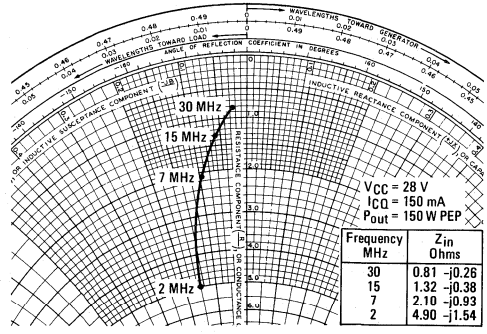


FIGURE 7 – SERIES INPUT IMPEDANCE



Frequency MHz	Z_{in} Ohms
30	0.81 –j0.26
15	1.32 –j0.38
7	2.10 –j0.93
2	4.90 –j1.54

3

FIGURE 8 – OUTPUT RESISTANCE versus FREQUENCY

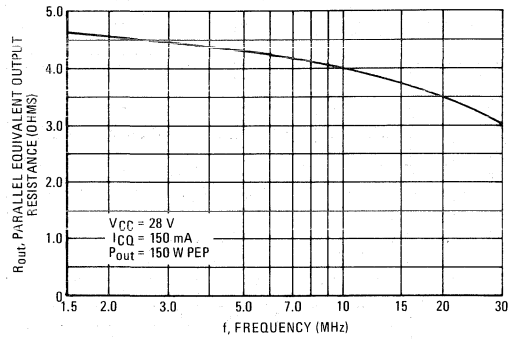
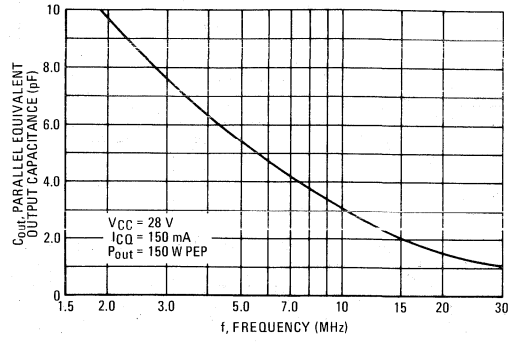


FIGURE 9 – OUTPUT CAPACITANCE versus FREQUENCY



MRF426
MRF426A

The RF Line

25 W (PEP) — 30 MHz

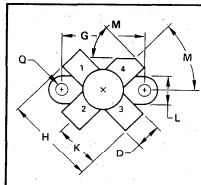
RF POWER
TRANSISTOR

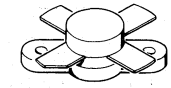
NPN SILICON

NPN SILICON RF POWER TRANSISTOR

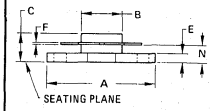
. . . designed for high gain driver and output linear amplifier stages in 1.5 to 30 MHz HF/SSB equipment.

- Specified 28 Volt, 30 MHz Characteristics —
  Output Power = 25 W (PEP)
  Minimum Gain = 22 dB
  Efficiency = 35%
- Intermodulation Distortion @ 25 W (PEP) —
  IMD = −30 dB (Max)
- 100% Tested for Load Mismatch at All Phase Angles With 30:1 VSWR
- Class A and AB Characterization
- BLX 13 Equivalent





MRF426



STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	24.64	24.89	0.970	0.980
B	9.40	9.91	0.370	0.390
C	5.82	7.14	0.229	0.281
D	5.46	5.97	0.215	0.235
E	2.16	2.67	0.085	0.105
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	20.07	20.57	0.790	0.810
K	10.03	10.29	0.395	0.405
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.81	4.57	0.150	0.180
Q	2.87	3.30	0.113	0.130

CASE 211-07

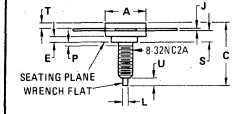
MAXIMUM RATINGS

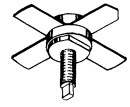
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	35	Vdc
Collector-Base Voltage	V_{CBO}	65	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	3.0	Adc
Withstand Current — 5 s	—	6.0	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	70 0.4	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

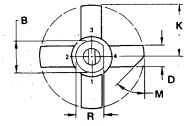
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.





MRF426A



STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	17.02	20.07	0.670	0.790
D	5.46	5.97	0.215	0.235
E	1.78	—	0.070	—
J	0.08	0.18	0.003	0.007
K	12.45	—	0.490	—
L	1.40	1.78	0.055	0.070
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.11	2.54	0.083	0.100
U	2.49	3.35	0.098	0.132

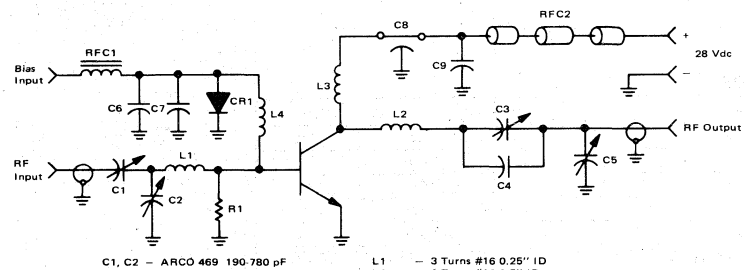
CASE 145A-09

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	35	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 50 mAdc, I_E = 0)	$V_{(BR)CBO}$	65	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 28 Vdc, V_{BE} = 0)	I_{CES}	–	–	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc	h_{FE}	10	35	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 30 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	60	80	pF
FUNCTIONAL TESTS (SSB)					
Common-Emitter Amplifier Gain (V_{CC} = 28 Vdc, P_{out} = 25 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 25 mA)	G_{PE}	22	25	–	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 25 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 25 mA)	η	35	–	–	%
Intermodulation Distortion (1) (V_{CC} = 28 Vdc, P_{out} = 25 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 25 mA)	IMD(d3)	–	–35	–30	dB
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 25 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 25 mA, VSWR 30:1 at All Phase Angles	ψ	No Degradation in Output Power			
CLASS A PERFORMANCE					
Intermodulation Distortion (1) and Power Gain (V_{CC} = 28 Vdc, P_{out} = 8 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 1.2 Adc)	G_{PE} IMD(d3) IMD(d5)	– – –	23.5 –40 –55	– – –	dB

(1) To MIL-STD-1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.

FIGURE 1 – 30 MHz LINEAR TEST CIRCUIT



C1, C2 – ARCO 469 190-780 pF
C3, C4 – ARCO 464 25-280 pF
C5 – 120 pF Dipped Mica
C6, C7 – 100 µF 15 Vdc
C8 – 680 pF F.T. Allen Bradley
C9 – 1.0 µF 35 V Tantalum

CR1 – IN4997

L1 – 3 Turns #16 0.25" ID
L2 – 6 Turns #16 0.5" ID
L3 – 7 Turns #20 0.38" ID
L4 – 10 µH Molded Choke Delevan

RFC1 – Ferroxcube VK200/20-4B
RFC2 – 3-Ferroxcube 5653065-3B
RF – Input/Output Connectors UG53 A/µ
R1 – 10 Ω 1/2 Watt 10%

Adjust Bias (Base) for I_{CQ} = 20 mA with No RF Applied

FIGURE 2 – OUTPUT POWER versus INPUT POWER

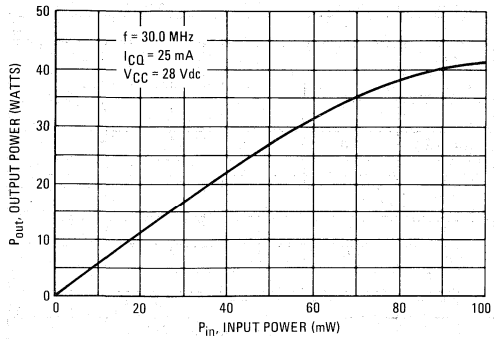


FIGURE 3 – OUTPUT POWER versus SUPPLY VOLTAGE

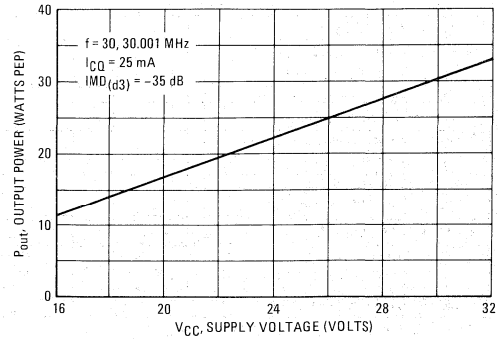


FIGURE 4 – POWER GAIN versus FREQUENCY

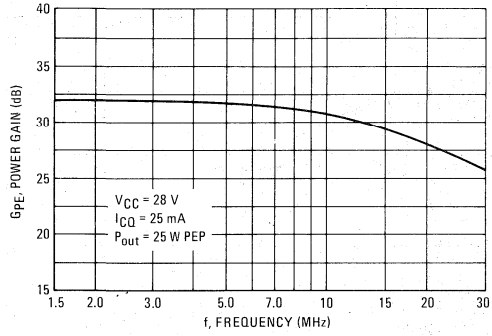


FIGURE 5 – INTERMODULATION DISTORTION versus OUTPUT POWER

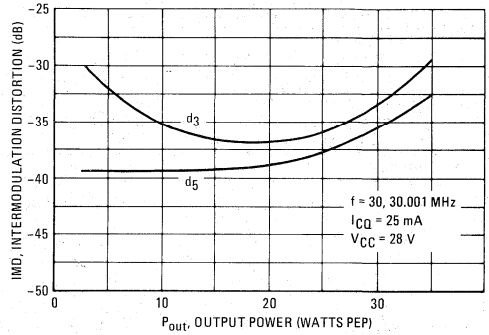


FIGURE 6 – DC SAFE OPERATING AREA

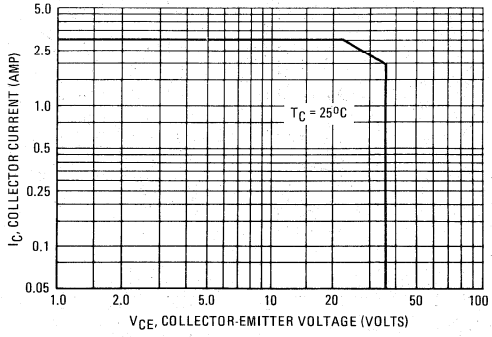


FIGURE 7 – OUTPUT CAPACITANCE versus FREQUENCY

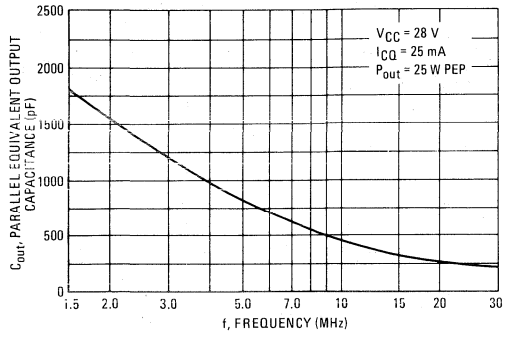


FIGURE 8 – OUTPUT RESISTANCE versus FREQUENCY

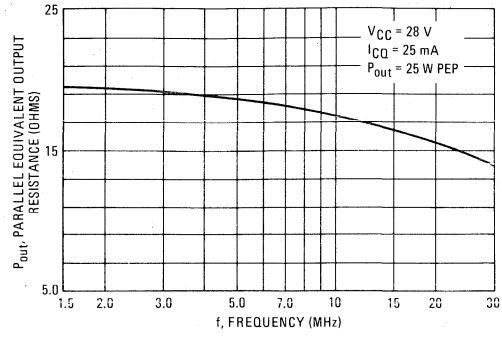
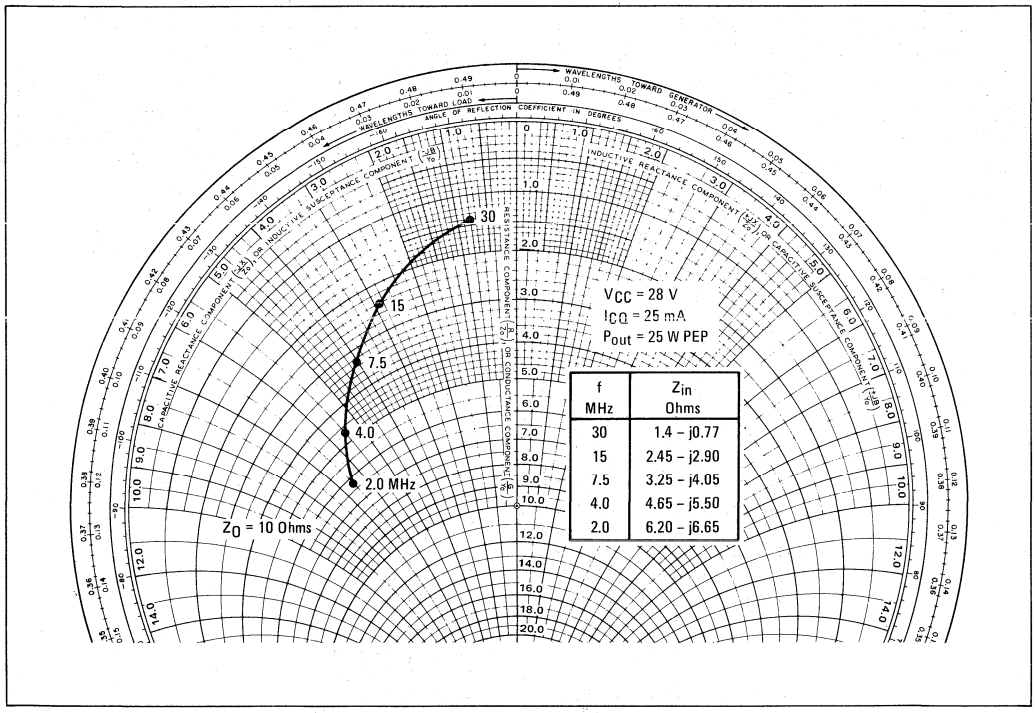


FIGURE 9 – SERIES EQUIVALENT INPUT IMPEDANCE



f MHz	Z_{in} Ohms
30	1.4 – j0.77
15	2.45 – j2.90
7.5	3.25 – j4.05
4.0	4.65 – j5.50
2.0	6.20 – j6.65

MRF427
MRF427A

The RF Line

25 W (PEP) — 30 MHz

RF POWER TRANSISTOR

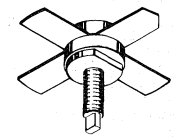
NPN SILICON

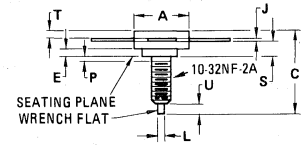
NPN SILICON RF POWER TRANSISTOR

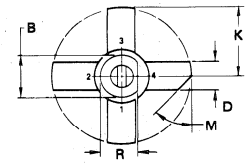
. . . designed primarily for high-voltage applications as a high-power linear amplifier from 2.0 to 30 MHz. Ideal for marine and base station equipment.

- Specified 50 Volt, 30 MHz Characteristics —
  Output Power = 25 W(PEP)
  Minimum Gain = 18 dB
- Intermodulation Distortion @ 25 W(PEP) —
  IMD = -34 dB (Min)
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR

MRF427A







STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.45	12.95	0.490	0.510
B	10.54	10.80	0.415	0.425
C	19.68	22.73	0.775	0.895
D	5.46	5.97	0.215	0.235
E	1.83	—	0.072	—
J	0.08	0.18	0.003	0.007
K	12.45	—	0.490	—
L	1.65	1.90	0.065	0.075
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
R	9.73	10.06	0.383	0.396
S	3.84	4.50	0.151	0.177
T	2.11	2.54	0.083	0.100
U	2.49	3.35	0.098	0.132

NOTE:
1. 145A-10, USE 10-32NF-2A STUD.

CASE 145A-10

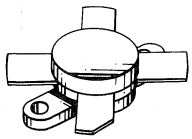
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	65	Vdc
Collector-Base Voltage	V_{CBO}	110	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	6.0	Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	80 0.457	Watts $W/^oC$
Storage Temperature Range	T_{stg}	−65 to +150	^oC

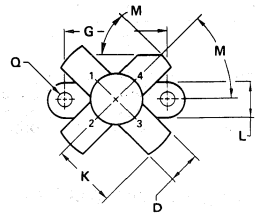
THERMAL CHARACTERISTICS

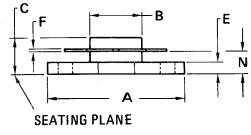
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.19	$^oC/W$

MRF427



STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	11.81	12.95	0.465	0.510
C	5.82	6.98	0.229	0.275
D	5.46	5.97	0.216	0.235
E	2.13	2.79	0.084	0.110
F	0.08	0.18	0.003	0.007
G	18.29	18.54	0.720	0.730
K	11.05	—	0.435	—
L	6.22	6.48	0.246	0.255
M	45° NOM		45° NOM	
N	3.66	4.52	0.144	0.178
Q	2.92	3.30	0.115	0.130

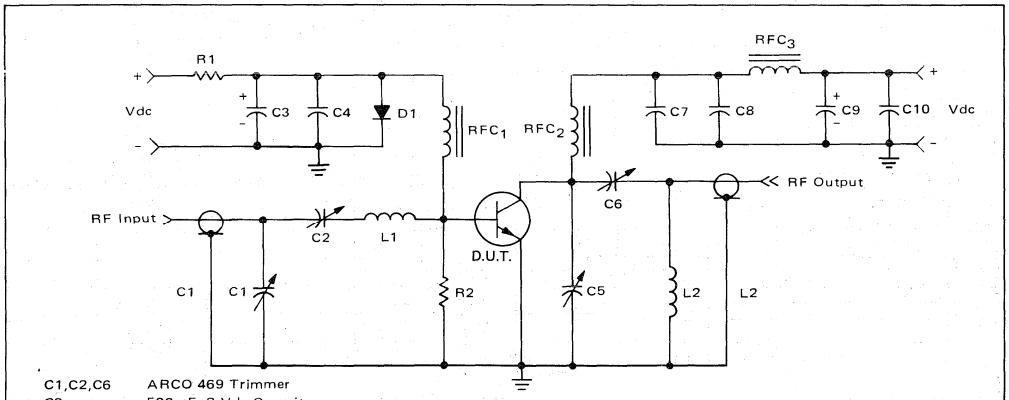
CASE 211-11

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 200 mAdc, I_B = 0)	$V_{(BR)CEO}$	65	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	110	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 mAdc, I_E = 0)	$V_{(BR)CBO}$	110	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0			Vdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	15	–	90	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 50 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	–	60	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 50 Vdc, P_{out} = 25 W(PEP), f = 30 MHz)	G_{pe}	18	20	–	dB
Intermodulation Distortion (V_{CC} = 50 Vdc, P_{out} = 25 W(PEP))	IMD	-34	-37	–	dB
Electrical Ruggedness (V_{CC} = 50 Vdc, P_{out} = 25 W(PEP), f = 30 MHz, VSWR 30:1) All Phase Angles	–	No Degradation in Output Power			

3

FIGURE 1 – 30 MHz TEST CIRCUIT SCHEMATIC



C1,C2,C6	ARCO 469 Trimmer	RFC1	1 μH Molded Choke
C3	500 μF, 3 Vdc Capacitor	RFC2	20 Turns, #20 AWG, Enameled Wire
C4,C7,C10	0.1 μF ERIE REDCAP		on 390 Ω, 1 Watt Resistor
C5	ARCO 463 Trimmer	RFC3	VK 200-4B FERROXCUBE Choke
C8	1000 pF, UNELCO Capacitor		
C9	47 μF, 50 Vdc Capacitor		
R1	20 Ω, 5 Watt Resistor		
R2	10 Ω, ½ Watt Resistor		
L1	0.15 μH Inductor		
L2	0.3 μH Inductor		
D1	1N4997		

FIGURE 2 – OUTPUT POWER versus INPUT POWER

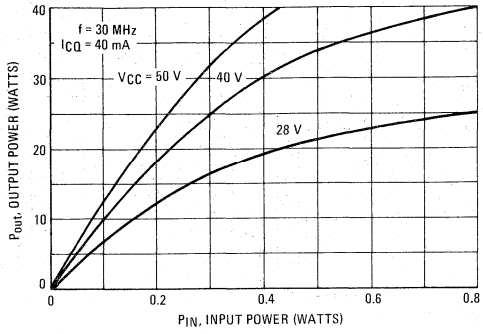


FIGURE 3 – POWER GAIN versus FREQUENCY

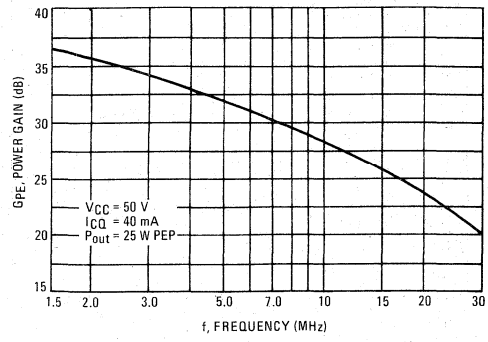


FIGURE 4 – INTERMODULATION DISTORTION versus OUTPUT POWER
V_{CC} = 50 Vdc

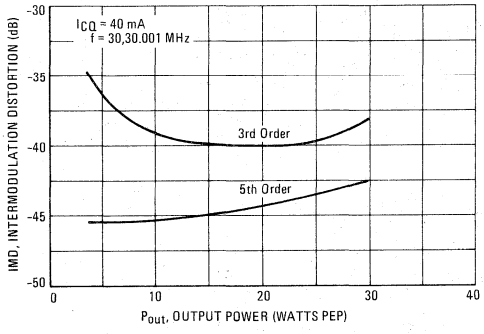


FIGURE 5 – INTERMODULATION DISTORTION versus OUTPUT POWER
V_{CC} = 40 Vdc

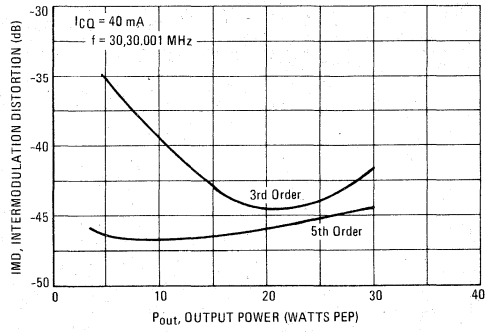


FIGURE 6 – OUTPUT RESISTANCE versus FREQUENCY

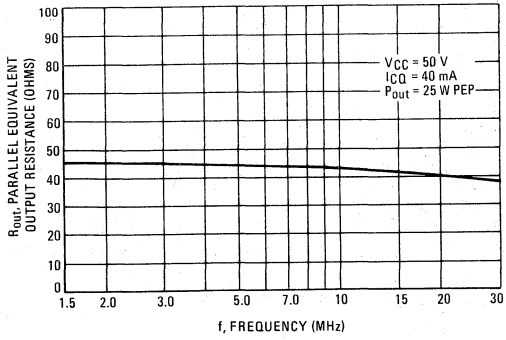


FIGURE 7 – OUTPUT CAPACITANCE versus FREQUENCY

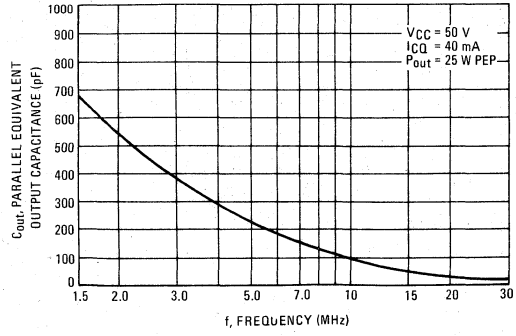


FIGURE 8 – OUTPUT POWER versus SUPPLY VOLTAGE

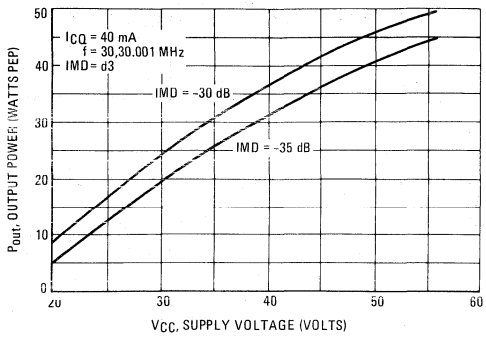


FIGURE 9 – DC SAFE OPERATING AREA

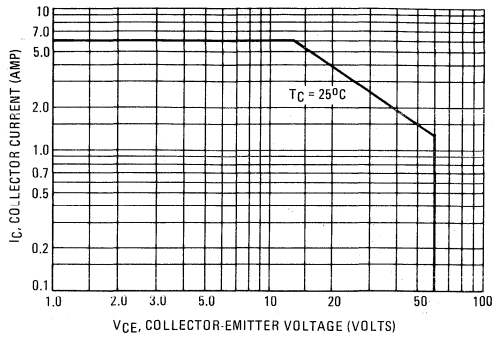
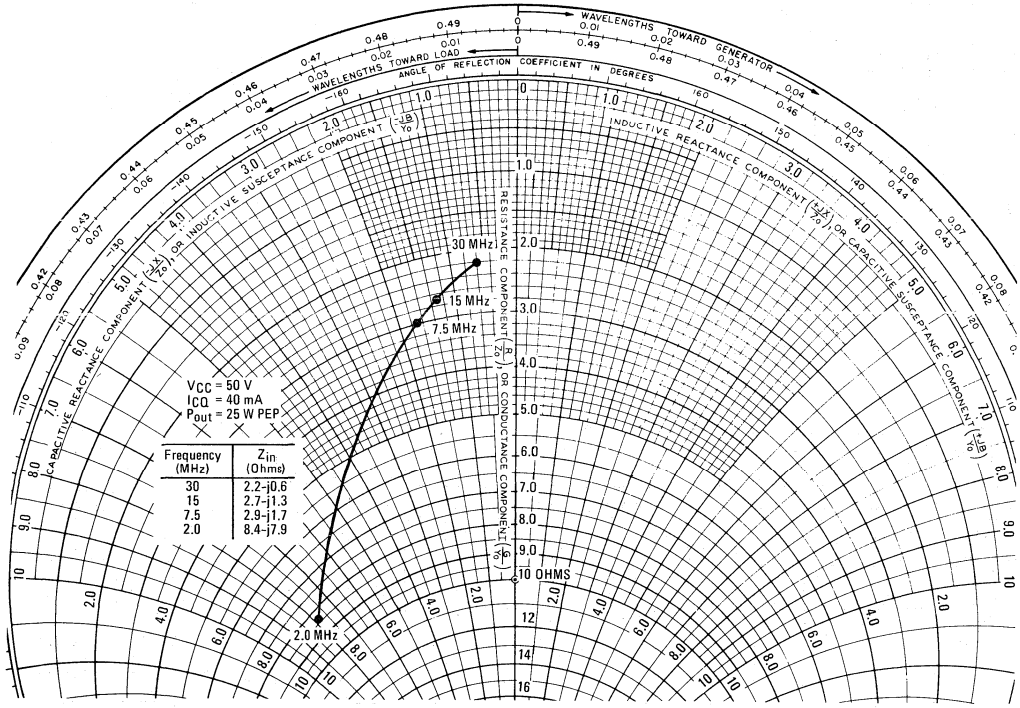


FIGURE 10 – SERIES EQUIVALENT IMPEDANCE



Frequency (MHz)	Zin (Ohms)
30	2.2-j0.6
15	2.7-j1.3
7.5	2.9-j1.7
2.0	8.4-j7.9

MRF428

The RF Line

150 W (PEP) – 30 MHz

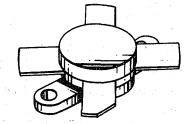
RF POWER TRANSISTOR

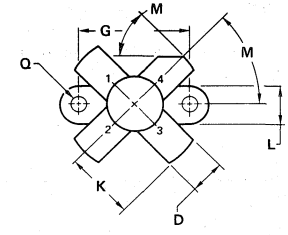
NPN SILICON

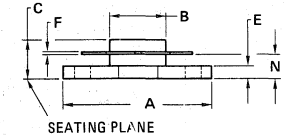
NPN SILICON RF POWER TRANSISTOR

. . . designed primarily for high-voltage applications as a high-power linear amplifier from 2.0 to 30 MHz. Ideal for marine and base station equipment.

- Specified 50 Volt, 30 MHz Characteristics –
  Output Power = 150 W(PEP)
  Minimum Gain = 13 dB
  Efficiency = 45%
- Intermodulation Distortion @ 150 W (PEP) –
  IMD = -30 dB (Max)
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR







STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	24.38	25.15	0.960	0.990
B	11.81	12.95	0.465	0.510
C	5.82	6.98	0.229	0.275
D	5.46	5.97	0.216	0.235
E	2.13	2.79	0.084	0.110
F	0.08	0.18	0.003	0.007
G	18.29	18.54	0.720	0.730
K	11.05	–	0.435	–
L	6.22	6.48	0.246	0.255
M	45° NOM		45° NOM	
N	3.66	4.52	0.144	0.178
Q	2.92	3.30	0.115	0.130

CASE 211-11

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	55	Vdc
Collector-Base Voltage	V_{CBO}	110	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current – Continuous	I_C	20	Adc
Withstand Current – 10 s	–	30	Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	320 1.83	Watts $W/^oC$
Storage Temperature Range	T_{stg}	−65 to +150	^oC

THERMAL CHARACTERISTICS

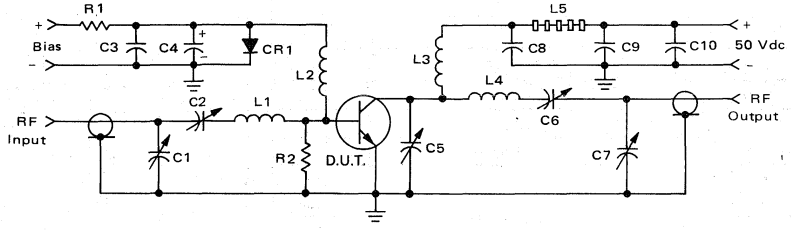
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.5	$^oC/W$

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 200 mAdc, I_B = 0)	$V_{(BR)CEO}$	55	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	110	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 mAdc, I_E = 0)	$V_{(BR)CBO}$	110	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	30	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 50 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	200	250	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Gain (V_{CC} = 50 Vdc, P_{out} = 150 W (PEP) I_C(max) = 3.32 Adc, f = 30 MHz)	G_{PE}	13	15	–	dB
Output Power (V_{CE} = 50 Vdc, f = 30 MHz)	P_{out}	150	–	–	W PEP
Collector Efficiency (V_{CC} = 50 Vdc, P_{out} = 150 W (PEP), I_C(max) = 3.32 Adc, f = 30 MHz)	η	45	–	–	%
Intermodulation Distortion (1) (V_{CE} = 50 Vdc, P_{out} = 150 W (PEP), I_C = 3.32 Adc)	IMD	–	-33	-30	dB
Electrical Ruggedness (V_{CC} = 50 Vdc, P_{out} = 150 W (PEP), I_C(max) = 3.32 Adc, f = 30 MHz) VSWR 30:1 at all Phase Angles	No Degradation in Output Power				

(1) To Mil Std 1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.

FIGURE 1 – 30 MHz TEST CIRCUIT SCHEMATIC



C1,C2,C7	170-780 pF, ARCO 465	R2	10 Ω, 1 Watt
C3,C8,C9	0.1 μF, 100 V ERIE	CR1	1N4997
C4	500 μF @ 6 V	L1	3 Turns, #16 Wire, 5/16" I.D., 5/16" Long
C5	9.0-180 pF, ARCO 463	L2	10 μH Molded Choke
C6	80-480 pF, ARCO 466	L3	12 Turns, #16 Enamaled Wire Closewound, 1/4" I.D.
C10	30 μF, 100 V	L4	5 Turns, 1/8" Copper Tubing, 9/16" I.D., 3/4" Long
R1	10 Ω, 10 Watt	L5	10 Ferrite Beads – FERROXCUBE #56-590-65/3B

FIGURE 2 – OUTPUT POWER versus INPUT POWER

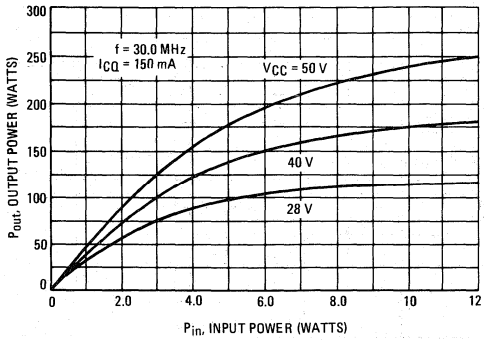


FIGURE 3 – OUTPUT POWER versus SUPPLY VOLTAGE

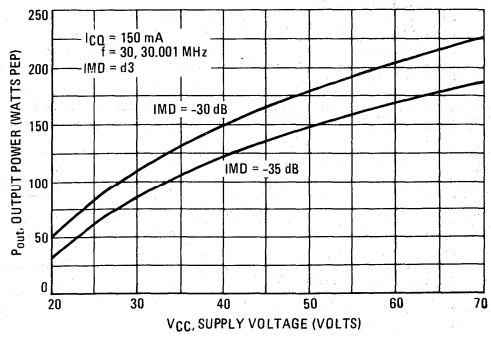


FIGURE 4 – POWER GAIN versus FREQUENCY

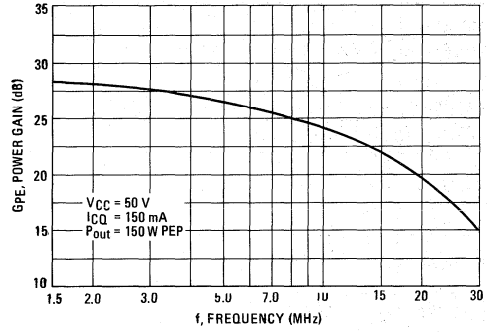
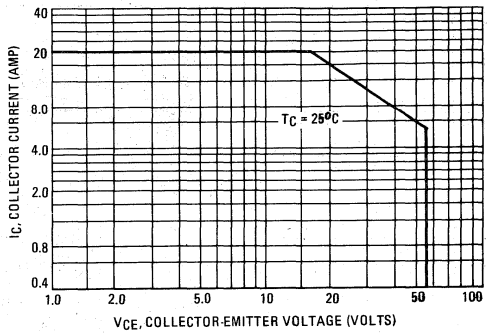


FIGURE 5 – DC SAFE OPERATING AREA



INTERMODULATION DISTORTION versus OUTPUT POWER

FIGURE 6 – V_{CC} = 40 Vdc

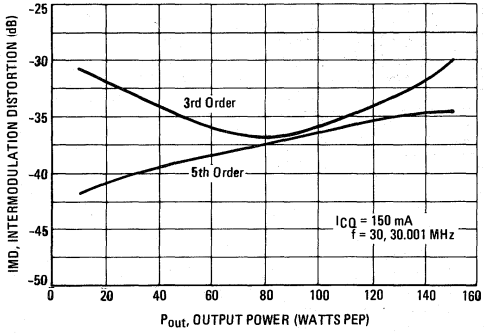
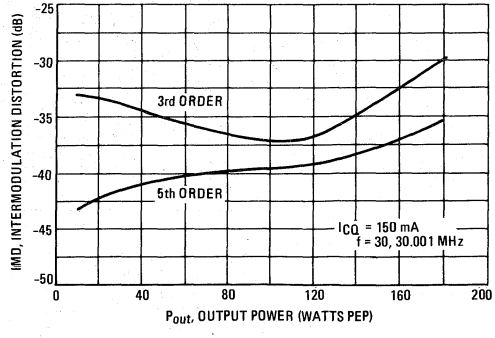


FIGURE 7 – V_{CC} = 50 Vdc



3

FIGURE 8 – OUTPUT CAPACITANCE versus FREQUENCY

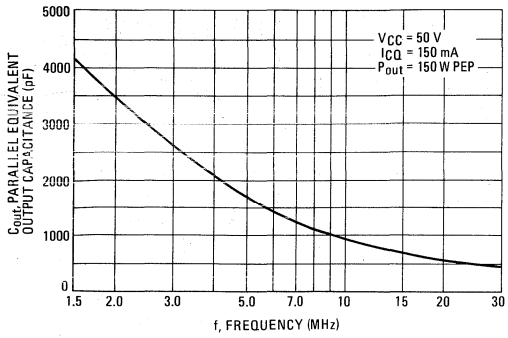


FIGURE 9 – OUTPUT RESISTANCE versus FREQUENCY

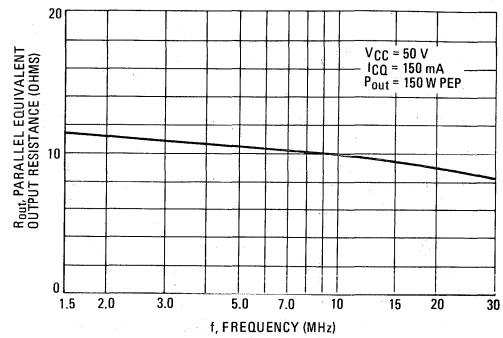
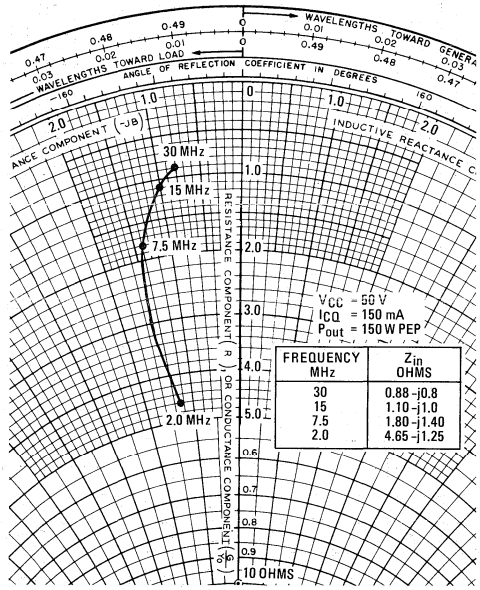


FIGURE 10 – SERIES EQUIVALENT IMPEDANCE



FREQUENCY MHz	Z_{in} OHMS
30	0.88 -j0.8
15	1.10 -j1.0
7.5	1.80 -j1.40
2.0	4.65 -j1.25

MRF429
MRF429MP

The RF Line

150 W (LINEAR) 30 MHz

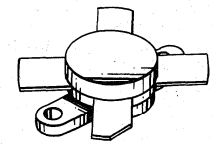
RF POWER TRANSISTOR

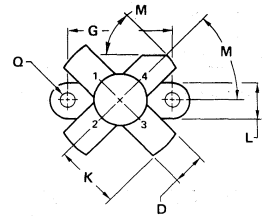
NPN SILICON

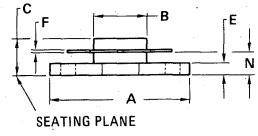
NPN SILICON RF POWER TRANSISTOR

. . . designed primarily for high-voltage applications as a high-power linear amplifier from 2.0 to 30 MHz. Ideal for marine and base station equipment.

- Specified 50 Volt, 30 MHz Characteristics —
  Output Power = 150 W(PEP)
  Minimum Gain = 13 dB
  Efficiency = 45%
- Intermodulation Distortion @ 150 W(PEP) —
  IMD = −32 dB (Max)
- Diffused Emitter Resistors for Superior Ruggedness
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR @ 150 W CW







STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	24.38	25.15	0.960	0.990
B	11.81	12.95	0.465	0.510
C	5.82	6.98	0.229	0.275
D	5.46	5.97	0.216	0.235
E	2.13	2.79	0.084	0.110
F	0.08	0.18	0.003	0.007
G	18.29	18.54	0.720	0.730
K	11.05	–	0.435	–
L	6.22	6.48	0.246	0.255
M	45° NOM		45° NOM	
N	3.66	4.52	0.144	0.178
Q	2.92	3.30	0.115	0.130

CASE 211-11

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector-Base Voltage	V_{CBO}	100	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	16	Adc
Withstand Current — 10 s	—	20	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	320 1.33	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

MRF429MP is for ordering an h_{FE} matched pair.

THERMAL CHARACTERISTICS

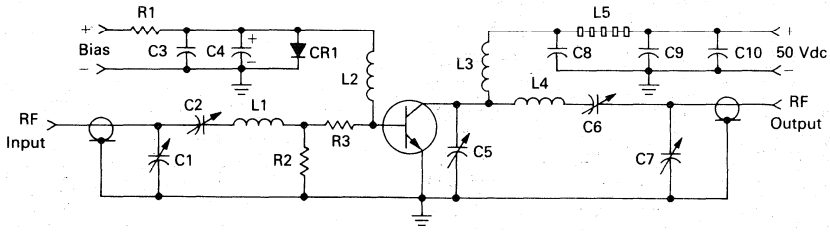
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.75	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 200 mAdc, I_B = 0)	$V_{(BR)CEO}$	50	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	100	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 100 mAdc, I_E = 0)	$V_{(BR)CBO}$	100	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	30	80	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 50 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	220	300	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Gain (V_{CC} = 50 Vdc, P_{out} = 150 W (PEP) I_C(max) = 3.32 Adc, f = 30; 30.001 MHz)	G_{PE}	13	15	—	dB
Output Power (V_{CE} = 50 Vdc, f = 30; 30.001 MHz)	P_{out}	150	—	—	W (PEP)
Collector Efficiency (V_{CC} = 50 Vdc, P_{out} = 150 W (PEP), I_C(max) = 3.32 Adc, f = 30; 30.001 MHz)	η	45	—	—	%
Intermodulation Distortion (1) (V_{CE} = 50 Vdc, P_{out} = 150 W (PEP), I_C = 3.32 Adc)	IMD	—	−35	−32	dB
Electrical Ruggedness (V_{CC} = 50 Vdc, P_{out} = 150 W CW, f = 30 MHz, VSWR 30:1 at all Phase Angles)	No Degradation in Output Power				

(1) To Mil Std 1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.

FIGURE 1 — 30 MHz TEST CIRCUIT SCHEMATIC



C1,C2,C7	170-780 pF, Arco 469	R2	10 Ω, 1 Watt
C3,C8,C9	0.1 μF, 100 V Erie	R3	5-3.3 Ω 1/2 Watt Carbon Resistors in Parallel
C4	500 μF @ 6 V	CR1	1N4997
C5	9.0-180 pF, Arco 463	L1	3 Turns, #16 Wire, 5/16" I.D., 5/16" Long
C6	80-480 pF, Arco 466	L2	10 μH Molded Choke
C10	30 μF, 100 V	L3	12 Turns, #16 Enameled Wire Closewound, 1/4" I.D.
R1	10 Ω, 10 Watt	L4	5 Turns, 1/8" Copper Tubing, 9/16" I.D., 3/4" Long
		L5	10 Ferrite Beads — Ferroxcube #56-590-65/3B

FIGURE 2 — OUTPUT POWER versus INPUT POWER

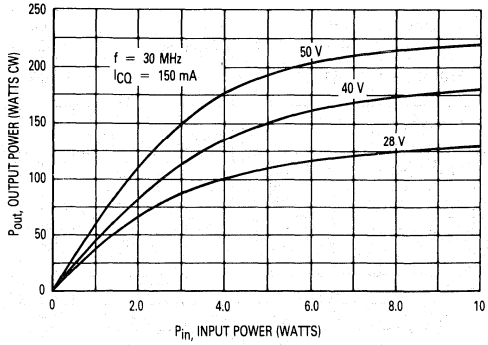


FIGURE 3 — OUTPUT POWER versus SUPPLY VOLTAGE

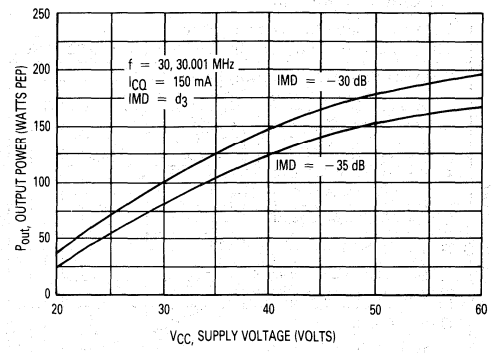


FIGURE 4 — POWER GAIN versus FREQUENCY

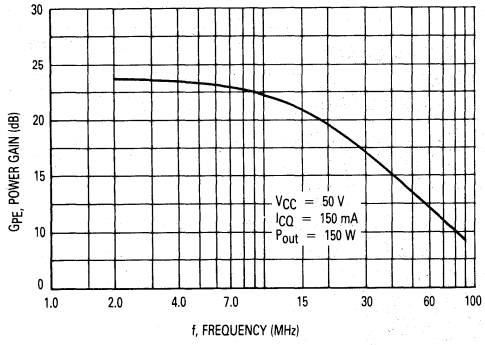


FIGURE 5 — RF SAFE OPERATING AREA (SOAR)

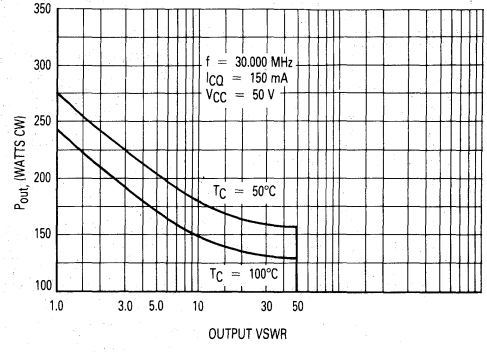


FIGURE 6 — f_T versus COLLECTOR CURRENT

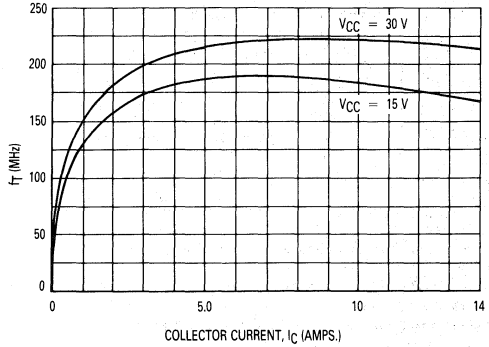


FIGURE 7 — IMD versus P_{out}

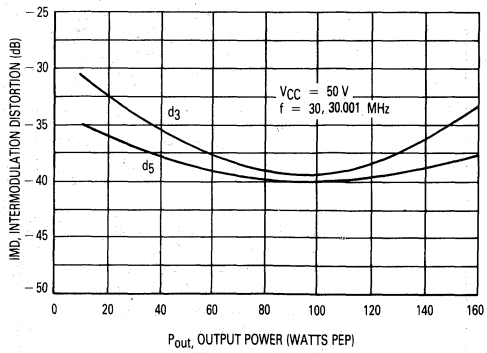


FIGURE 8 — OUTPUT CAPACITANCE versus FREQUENCY

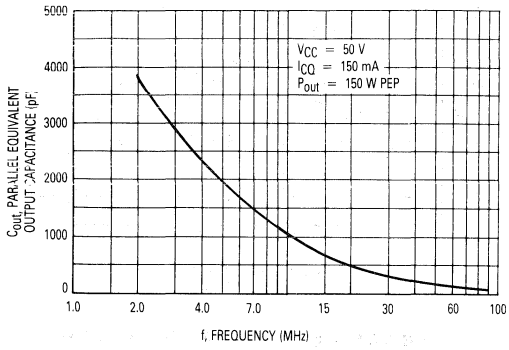


FIGURE 9 — OUTPUT RESISTANCE versus FREQUENCY

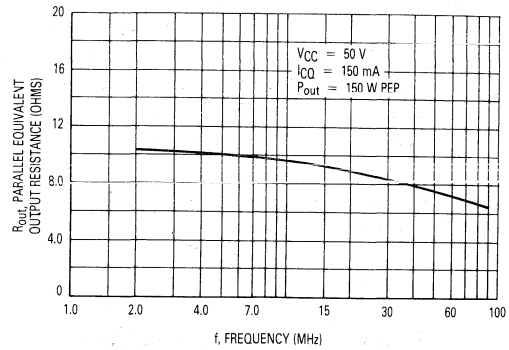
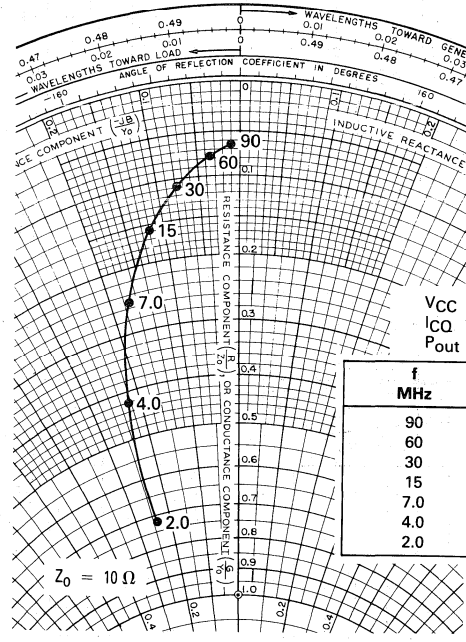


FIGURE 10 — SERIES EQUIVALENT IMPEDANCE



V_{CC} = 50 V
I_{CQ} = 150 mA
P_{out} = 150 W PEP

f MHz	Z_{in} Ohms
90	0.67 − J0.10
60	0.78 − J0.30
30	1.10 − J0.70
15	1.60 − J1.15
7.0	2.55 − J1.75
4.0	4.20 − J2.25
2.0	7.15 − J2.40

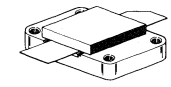
MRF430

The RF Line
NPN Silicon RF Power Transistor

600 WATTS (LINEAR)
30 MHz
RF POWER TRANSISTOR
NPN SILICON

. . . designed primarily for high-voltage applications as a high-power linear amplifier from 2 to 30 MHz. Ideal for marine and base station equipment.

- Specified 50 Volt, 30 MHz Characteristics
  - Output Power = 600 W
  - Minimum Gain = 10 dB
  - Efficiency = 40%
- Intermodulation Distortion @ 600 W(PEP) — IMD = −30 dB
- Diffused Emitter Resistors for Superior Ruggedness
- Low Thermal Resistance



CASE 368-01

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector-Base Voltage	V_{CBO}	110	Vdc
Emitter-Base Voltage	V_{EBO}	4	Vdc
Collector Current — Continuous	I_C	60	Adc
Operating Junction Temperature	T_J	200	°C
Total Device Dissipation @ T_C = 25°C Derate Above 25°C	P_D	875 5	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.20	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

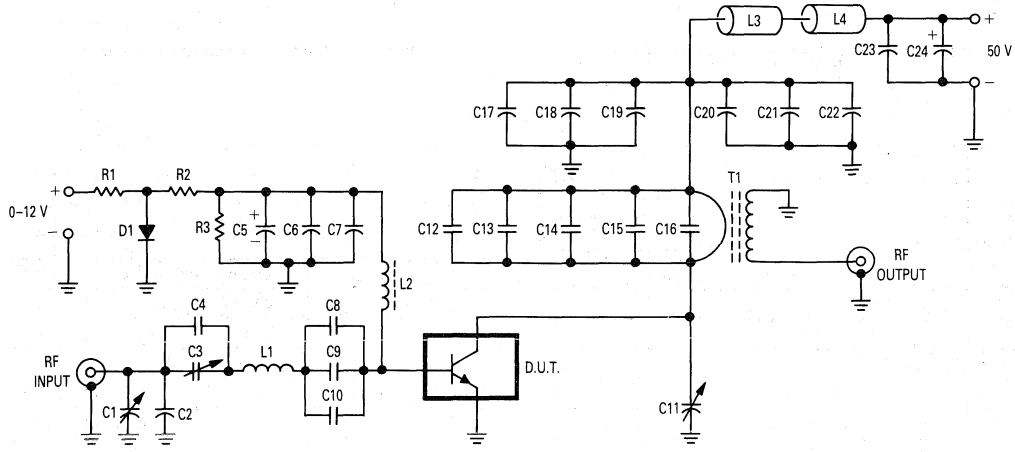
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 500 mAdc, I_B = 0)	$V_{(BR)CEO}$	50	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 200 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	110	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 20 mAdc, I_C = 0)	$V_{(BR)EBO}$	4	—	—	Vdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 20 Adc, V_{CE} = 10 Vdc)	h_{FE}	10	30	80	—

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 50 Vdc, I_E = 0, f = 1 MHz)		C_{ob}	—	900	1200	pF
FUNCTIONAL TEST						
Common-Emitter Amplifier Power Gain (V_{CC} = 50 Vdc, P_{out} = 600 W (CW), f = 30 MHz, I_{CQ} = 600 mA)		G_{PE}	10	13	—	dB
Collector Efficiency (V_{CC} = 50 Vdc, P_{out} = 600 W, f = 30 MHz, I_{CQ} = 600 mA)	(PEP)	η	—	40	—	%
	(CW)		—	60	—	%
Intermodulation Distortion (1) (V_{CE} = 50 Vdc, P_{out} = 600 W (PEP), I_{CQ} = 600 mA, f = 30 MHz)		IMD	—	−30	—	dB

(1) To Mil Std 1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.



C1, C3, C11 — Arco 469 or equivalent
C2 — 820 pF
C4 — 330 pF
C5 — 1000 μF/3 V Electrolytic
C6, C8, C9, C10, C17, C18, C19 — 0.1 μF
C7, C22, C23 — 0.47 μF, RMC Type 2225C or equivalent
C12, C13, C14 — 470 pF
C15 — 1000 pF
C16 — Two Unencapsulated 1000 pF Mica in Series
C20, C21 — 0.039 μF
C24 — 10 μF/100 V Electrolytic
D1 — 1N4997 or equivalent
R1 — 10 Ohms/10 W
R2 — 0.1 Ohm/½ W
R3 — 2.7 Ohms/2 W

L1 — 2 Turns #14 AWG, ½" ID, ½" Long
L2 — Ohmite Z-235 or equivalent
L3, L4 — Ferrite Beads, Fair-Rite Products Corp. #2673000801 or equivalent
T1 — RF Transformer, 1:25 Impedance Ratio. See Motorola Application Note AN749, Figure 4 for details. Ferrite Material: 2 Each, Fair-Rite Product Corp. #2667540001 or equivalent

All capacitors ATC type 100/200 chips or equivalent, unless otherwise noted.

Figure 1. 30 MHz Test Circuit Schematic

TYPICAL CHARACTERISTICS

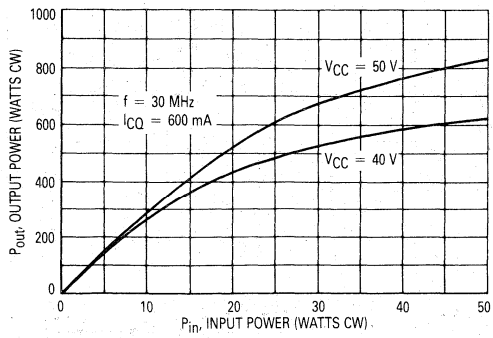


Figure 2. Output Power versus Input Power

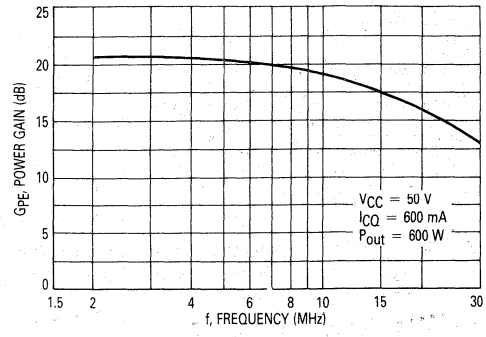


Figure 3. Power Gain versus Frequency

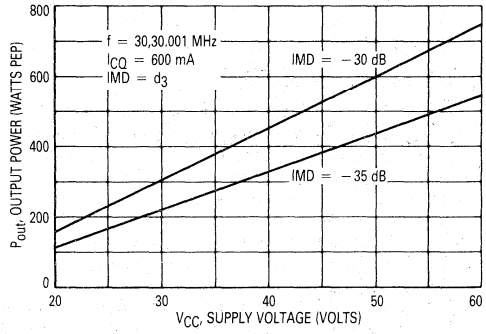


Figure 4. Output Power versus Supply Voltage

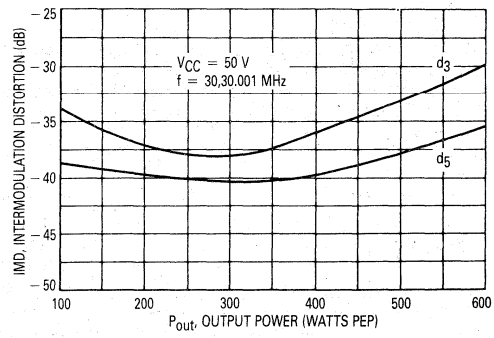


Figure 5. IMD versus Output Power

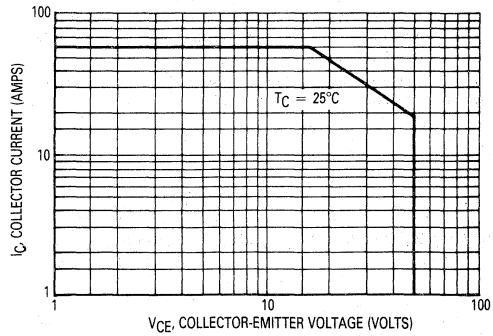


Figure 6. DC Safe Operating Area

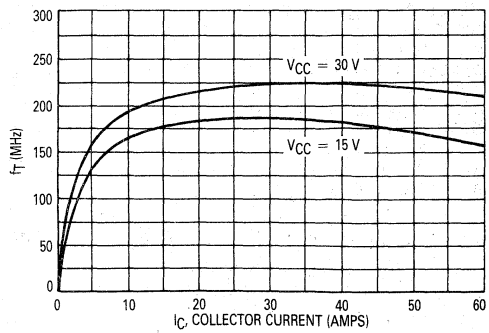


Figure 7. f_T versus Collector Current

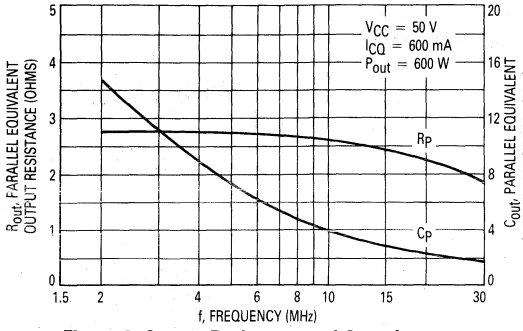
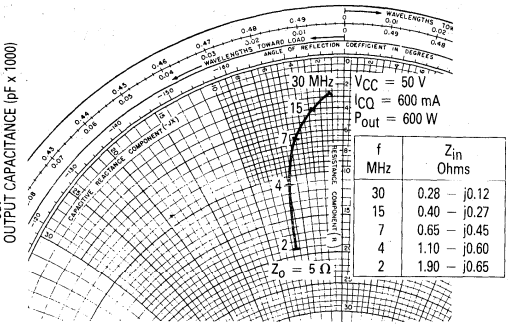


Figure 8. Output Resistance and Capacitance versus Frequency



f MHz	Z_{in} Ohms
30	0.28 – j0.12
15	0.40 – j0.27
7	0.65 – j0.45
4	1.10 – j0.60
2	1.90 – j0.65

Figure 9. Series Equivalent Input Impedance

MOUNTING OF HIGH POWER RF POWER TRANSISTORS

The package of this device is designed for conduction cooling. It is extremely important to minimize the thermal resistance between the device flange and the heat dissipator.

Since the device mounting flange is made of soft copper, it may be deformed during various stages of handling or during transportation. It is recommended that the user makes a final inspection on this before the device installation. ±0.0005″ is considered sufficient for the flange bottom.

The same applies to the heat dissipator in the device mounting area. If copper heatsink is not used, a copper head spreader is strongly recommended between the device mounting surfaces and the main heatsink. It should be at least 1/4″ thick and extend at least one inch from the flange edges. A thin layer of thermal compound in all interfaces is, of course, essential. The recommended torque on the 4-40 mounting screws should be in the area of 4–5 lbs.-inch, and spring type lock washers along with flat washers are recommended.

For die temperature calculations, the Δ temperature from a corner mounting screw area to the bottom center of the flange is approximately 5°C and 10°C under normal operating conditions (dissipation 150 W and 300 W respectively).

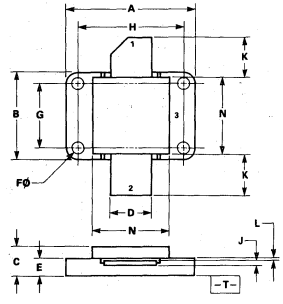
The main heat dissipator must be sufficiently large and have low R_θ for moderate air velocity, unless liquid cooling is employed.

CIRCUIT CONSIDERATIONS

At high power levels (500 W and up), the circuit layout becomes critical due to the low impedance levels and high RF currents associated with the output matching. Some of the components, such as capacitors and inductors must also withstand these currents. The component losses are directly proportional to the operating frequency. The manufacturers specifications on capacitor ratings should be consulted on these aspects prior to design.

Push-pull circuits are less critical in general, since the ground referenced RF loops are practically eliminated, and the impedance levels are higher for a given power output. High power broadband transformers are also easier to design than comparable LC matching networks.

OUTLINE DIMENSIONS



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS BOTH A DATUM AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR F DIAMETER. ⌖ ϕ 0.25 (.010) Ⓜ | T | A Ⓜ | B Ⓜ |
3. DIMENSIONING AND TOLERANCING PER Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

CASE 368-01

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	37.85	38.35	1.490	1.510
B	25.15	25.65	0.990	1.010
C	8.38	8.89	0.330	0.350
D	12.45	12.95	0.490	0.510
E	4.95	5.21	0.195	0.205
F	3.05	3.30	0.120	0.130
G	19.05 BSC		0.750 BSC	
H	31.75 BSC		1.250 BSC	
J	1.14	1.39	0.045	0.055
K	10.54	11.05	0.415	0.435
L	0.10	0.15	0.004	0.006
N	22.87	23.11	0.890	0.910

MRF433

The RF Line

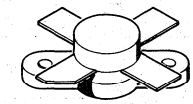
12.5 W (PEP) – 30 MHz
RF POWER TRANSISTOR

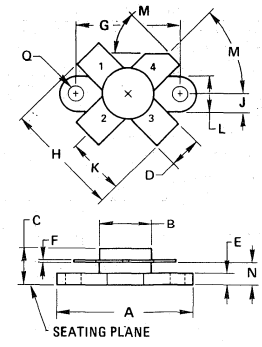
MRF433 – NPN SILICON

SILICON RF POWER TRANSISTORS

. . . designed primarily for application as complementary symmetry amplifiers in linear amplifiers from 2.0 to 30 MHz.

- Specified 12.5 Volt, 30 MHz Characterisitcs –
  Output Power = 12.5 W (PEP)
  Minimum Gain = 20 dB
  Efficiency = 50%
- Intermodulation Distortion @ 12.5 W (PEP) –
  IMD = -30 dB (Max)





STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current – Continuous	I_C	2.5	Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	20 114	Watts $W/^oC$
Storage Temperature Range	T_{stg}	–65 to +150	^oC

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.64	24.89	0.970	0.980
B	9.40	9.91	0.370	0.390
C	5.82	7.14	0.229	0.281
D	5.46	5.97	0.215	0.235
E	2.16	2.67	0.085	0.105
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	20.07	20.57	0.790	0.810
K	10.03	10.29	0.395	0.405
L	6.22	6.48	0.245	0.255
M	40^0	50^0	40^0	50^0
N	3.81	4.57	0.150	0.180
Q	2.87	3.30	0.113	0.130

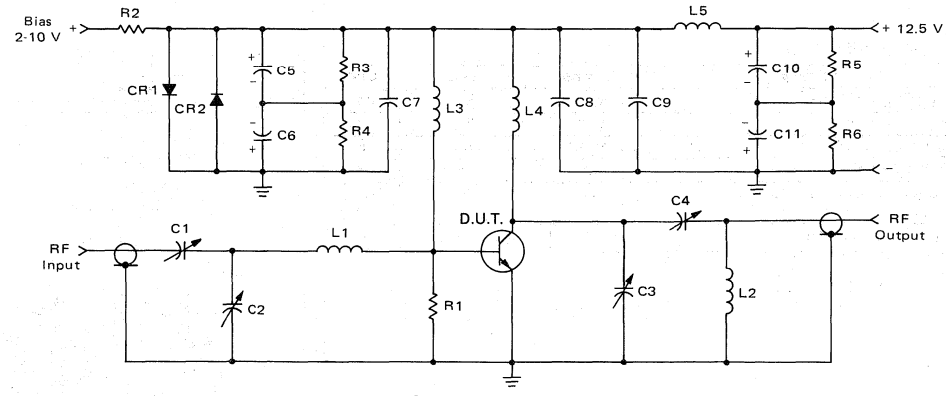
CASE 211-07

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 2.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 55°C)	I_{CES}	–	–	8.0	mAdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	0.5	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	15	–	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	70	120	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain(1) (V_{CC} = 12.5 Vdc, P_{out} = 12.5 W (PEP), I_{CQ} = 100 mAdc, f = 30,30.001 MHz)	G_{pe}	20	–	–	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 12.5 W (PEP) (f = 30,30.001 MHz)	η(1) η(2)	45 40	50 45	–	%
Intermodulation Distortion (V_{CC} = 12.5 Vdc, P_{out} = 12.5 W (PEP), I_{CQ} = 100 mAdc, f = 30, 30.001 MHz)	IMD	–	–	-30	dB
Series Equivalent Input Impedance (V_{CC} = 12.5 Vdc, P_{out} = 12.5 W (PEP), I_{CQ} = 100 mAdc, f = 30,30.001 MHz)	Z_{in}	–	2.50-j2.20	–	Ohms
Series Equivalent Output Impedance (V_{CC} = 12.5 Vdc, P_{out} = 12.5 W (PEP), I_{CQ} = 100 mAdc, f = 30, 30.001 MHz)	Z_{out}	–	4.80-j3.00	–	Ohms

(1) Class AB
(2) Class A

FIGURE 1 – 30 MHz TEST CIRCUIT SCHEMATIC



C1,C2,C4	170–780 pF, ARCO 469	R2	10 Ω, 5 Watt	L3	10 μH Molded Choke
C3	25–280 pF, ARCO 464	R3,R4	1 kΩ, 1/4 Watt	L4	15 Turns, #24 AWG Enamaled Wire, Closewound on a 100 Ω, 1 Watt Carbon Resistor.
C5,C6	500 μF, 3 V, ELECTROLYTIC	R5,R6	10 kΩ, 1/4 Watt		
C7,C9	0.1 μF, Disc Ceramic	CR1,CR2	1N4001		
C8	1000 pF Disc Ceramic	L1	3 Turns, #18 AWG, 1/4" I.D., 3/16" Long	L5	FERROXCUBE VK200 – 20/4B
C10,C11	100 μF, 15 V, ELECTROLYTIC	L2	3 Turns, #16 AWG, 3/8" I.D., 1/4" Long		
R1	10 Ω, 1/2 Watt				

MRF448

The RF Line

250 W — 30 MHz

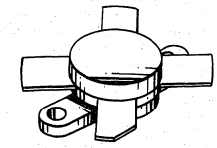
RF POWER TRANSISTOR

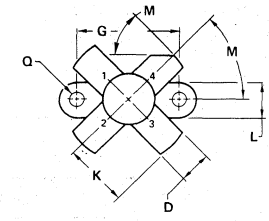
NPN SILICON

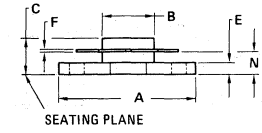
NPN SILICON RF POWER TRANSISTOR

. . . designed primarily for high-voltage applications as a high-power linear amplifier from 2.0 to 30 MHz. Ideal for marine and base station equipment.

- Specified 50 Volt, 30 MHz Characteristics
  - Output Power = 250 W
  - Minimum Gain = 12 dB
  - Efficiency = 45%
- Intermodulation Distortion @ 250 W (PEP) — IMD = −30 dB (Max)
- 100% Tested for Load Mismatch at all Phase Angles with 3:1 VSWR







STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	11.81	12.95	0.465	0.510
C	5.82	6.98	0.229	0.275
D	5.46	5.97	0.216	0.235
E	2.13	2.79	0.084	0.110
F	0.08	0.18	0.003	0.007
G	18.29	18.54	0.720	0.730
K	11.05	–	0.435	–
L	6.22	6.48	0.246	0.255
M	45° NOM		45° NOM	
N	3.66	4.52	0.144	0.178
Q	2.92	3.30	0.115	0.130

CASE 211-11

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector-Base Voltage	V_{CBO}	100	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	16	Adc
Withstand Current — 10 s	—	20	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate Above 25°C	P_D	400 1.67	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.6	°C/W

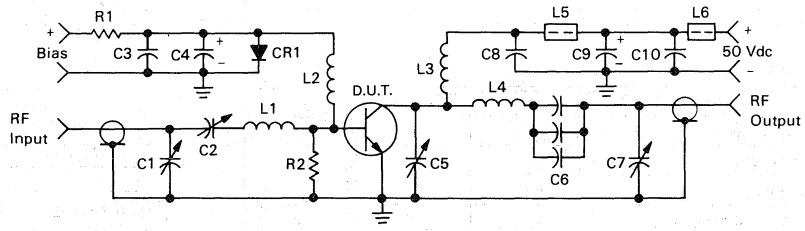
(1) P_D is a measurement reflecting short term maximum condition. See SOAR curve for operating conditions.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 200 mAdc, I_B = 0)	$V_{(BR)CEO}$	50	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	100	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 100 mAdc, I_E = 0)	$V_{(BR)CBO}$	100	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	30	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 50 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	350	450	pF
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (V_{CC} = 50 Vdc, P_{out} = 250 W CW, f = 30 MHz, I_{CQ} = 250 mA)	G_{PE}	12	14	—	dB
Collector Efficiency (V_{CC} = 50 Vdc, P_{out} = 250 W, f = 30 MHz, I_{CQ} = 250 mA)	η	— —	45 65	— —	% (PEP) % (CW)
Intermodulation Distortion (1) (V_{CE} = 50 Vdc, P_{out} = 250 W (PEP), I_{CQ} = 250 mA, f = 30 MHz)	IMD	—	-33	-30	dB
Electrical Ruggedness (V_{CC} = 50 Vdc, P_{out} = 250 W CW, f = 30 MHz, VSWR 3:1 at all Phase Angles)	No Degradation in Output Power				

(1) To Mil Std 1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.

FIGURE 1 — 30 MHz TEST CIRCUIT SCHEMATIC



C1, C2, C5, C7 — 170–780 pF, Arco 469
C3, C8, C9 — 0.1 μF, 100 V Erie
C4 — 500 μF @ 6.0 V
C6 — 360 pF, 3 × 120 pF 3.0 kV in parallel
C10 — 10 μF, 100 V
R1 — 10 Ω, 10 Watt
R2 — 10 Ω, 1 Watt

CR1 — 1N4997 or equivalent
L1 — 3 Turns, #16 Wire, 0.4 ″ I.D., 0.3 ″ Long
L2 — 0.8 μH, Ohmite Z-235 or equivalent
L3 — 12 Turns, #16 Enameled Wire Closewound 0.25″ I.D.
L4 — 4 Turns, 1/8″ Copper Tubing, 0.6″ I.D., 1.0″ Long
L5, L6 — 2.0 μH, Fair-Rite 2643021801 Ferrite bead each or equivalent.

FIGURE 2 — OUTPUT POWER versus INPUT POWER

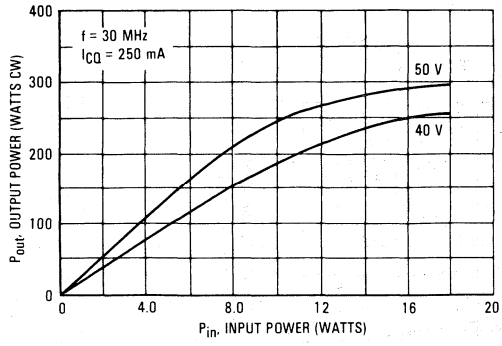


FIGURE 3 — OUTPUT POWER versus SUPPLY VOLTAGE

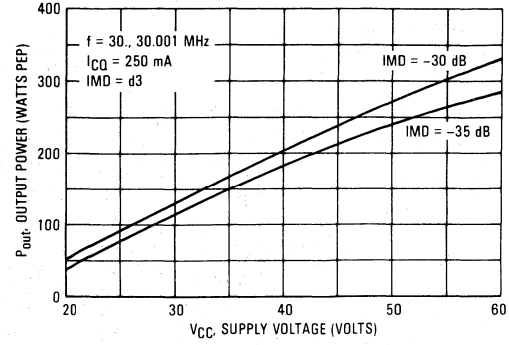


FIGURE 4 — POWER GAIN versus FREQUENCY

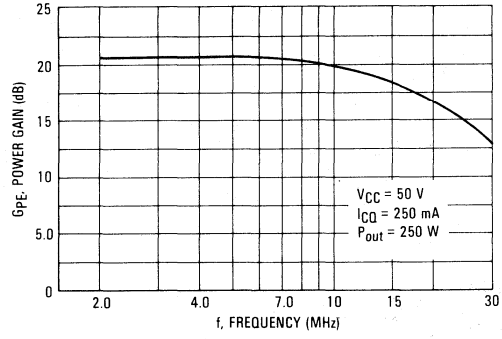


FIGURE 5 — RF SOAR (CLASS AB)
P_{out} versus OUTPUT VSWR

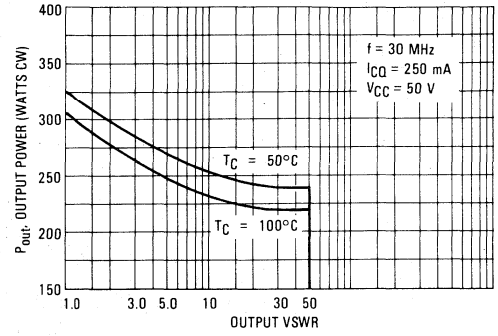


FIGURE 6 — f_T versus COLLECTOR CURRENT

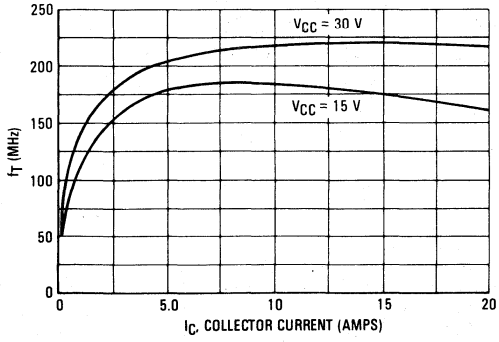


FIGURE 7 — IMD versus P_{out}

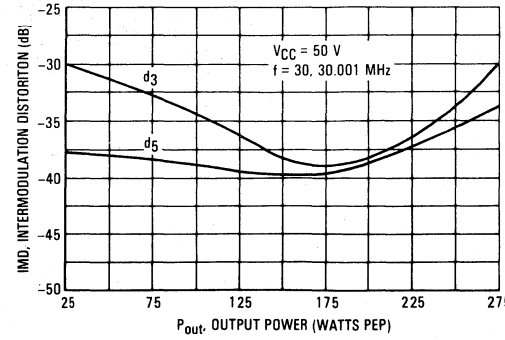


FIGURE 8 — OUTPUT RESISTANCE AND CAPACITANCE versus FREQUENCY

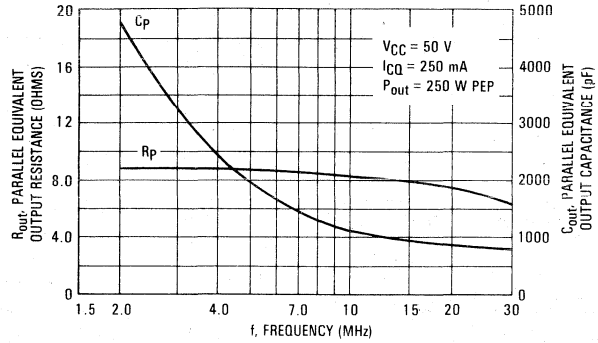
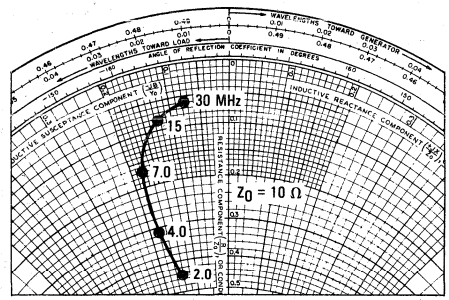


FIGURE 9—SERIES EQUIVALENT IMPEDANCE



V_{CC} = 50 V
I_{CQ} = 150 mA
P_{out} = 250 W PEP

f MHz	Z_{in} Ohms
30	0.60 –J0.75
15	0.80 –J1.25
7.0	1.70 –J1.75
4.0	3.10 –J1.80
2.0	4.50 –J1.40

MRF449
MRF449A

The RF Line

30 W — 30 MHz

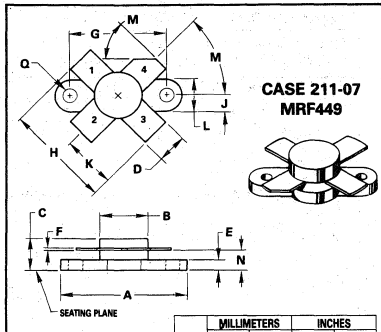
RF POWER TRANSISTORS

NPN SILICON

NPN SILICON RF POWER TRANSISTORS

. . . designed for power amplifier application in industrial, commercial and amateur radio equipment to 30 MHz.

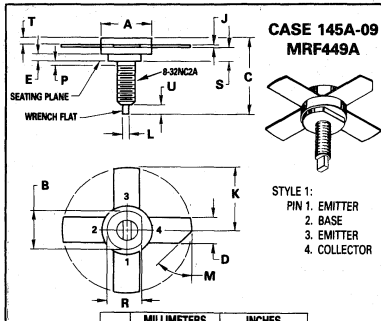
- Specified 12.5 Volt, 30 MHz Characteristics —
  Output Power = 30 Watts
  Minimum Gain = 12 dB
  Efficiency = 50%



CASE 211-07
MRF449

STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	24.38	25.15	0.960	0.990
B	9.40	9.91	0.370	0.390
C	5.82	7.14	0.229	0.281
D	5.46	5.97	0.215	0.235
E	2.16	2.67	0.085	0.105
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	20.07	20.57	0.790	0.810
K	10.03	10.29	0.395	0.405
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.81	4.57	0.150	0.180
Q	2.87	3.30	0.113	0.130



CASE 145A-09
MRF449A

STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	17.02	20.07	0.670	0.790
D	5.46	5.97	0.215	0.235
E	1.78	—	0.070	—
J	0.08	0.18	0.003	0.007
K	12.45	—	0.490	—
L	1.40	1.78	0.055	0.070
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.11	2.54	0.083	0.100
U	2.49	3.35	0.098	0.132

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CBO}	40	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	60 343	Watts mW/^oC
Storage Temperature Range	T_{stg}	−65 to +150	^oC

THERMAL CHARACTERISTICS

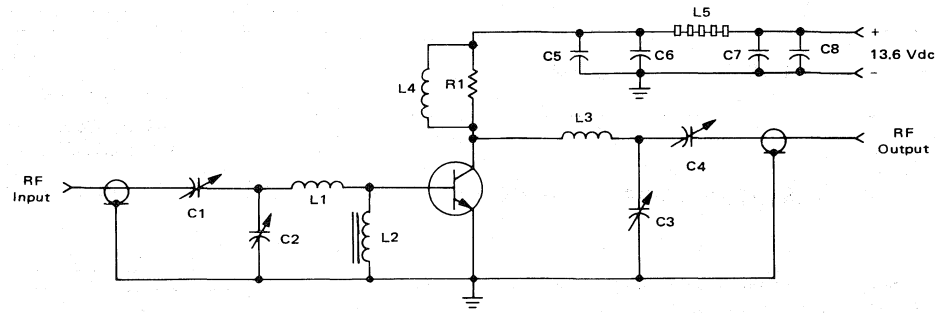
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.9	$^oC/W$

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	–	–	Vdc
Collector-Emitter Breakdown Voltage (i_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	40	50	–	Vdc
Collector-Base Breakdown Voltage (i_C = 20 mAdc, I_E = 0)	$V_{(BR)CBO}$	40	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
ON CHARACTERISTICS					
DC Current Gain (i_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	–	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	–	140	pF
FUNCTIONAL TESTS (Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 13.6 Vdc, P_{out} = 30 W, I_C(max) = 4.0 Adc, f = 30 MHz)	G_{PE}	12	14	–	dB
Collector Efficiency (V_{CC} = 13.6 Vdc, P_{out} = 30 W, I_C(max) = 4.0 Adc, f = 30 MHz)	η	50	–	–	%
Series Equivalent Input Impedance (V_{CC} = 12.5 Vdc, P_{out} = 30 W, f = 30 MHz)	Z_{in}	–	2.13-j1.15	–	Ohms
Series Equivalent Output Impedance (V_{CC} = 12.5 Vdc, P_{out} = 30 W, f = 30 MHz)	Z_{out}	–	2.47-j0.37	–	Ohms

FIGURE 1 – 30 MHz TEST CIRCUIT SCHEMATIC



C1 –	14-150 pF, ARCO 424
C2,C3,C4 –	170-780 pF, ARCO 469
C5,C8 –	ERIE 0.1 μF @ 100 V RED CAPS
C6 –	1000 pF UNELCO, 350 Vdc
C7 –	10 μF, 35 Vdc
R1 –	100 Ω, 2 W Carbon
L1 –	0.15 μH Molded Choke MILLER
L2 –	FERROXCUBE, VK200-20-4B
L3 –	3 Turns, #14 Bare Tinned Wire, 0.3" (0.79) I.D. x 0.38" (0.97) Long
L4 –	9 Turns, #20 Enamal Wire, Close Wound on R1
L5 –	FERROXCUBE #56-570-65/3B, 5 Ferrite Beads, on 1" Long #20 Wire

Input/Output Connectors – Type N

Board – Glass Teflon Mounted on a 4" x 4" x 2" SEEZAK Box

FIGURE 2 – POWER OUTPUT versus POWER INPUT

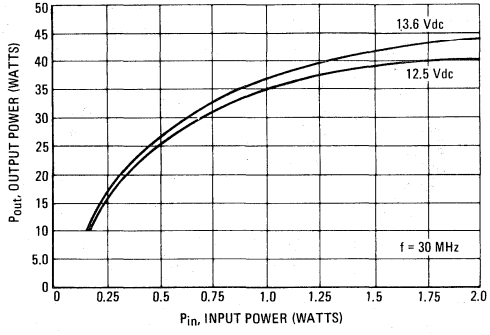
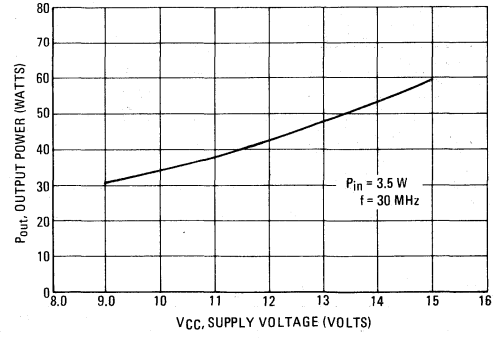


FIGURE 3 – OUTPUT POWER versus SUPPLY VOLTAGE



MRF450
MRF450A

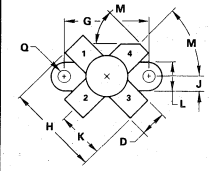
The RF Line

50 W – 30 MHz
RF POWER
TRANSISTORS
NPN SILICON

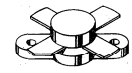
NPN SILICON RF POWER TRANSISTORS

. . . designed for power amplifier applications in industrial, commercial and amateur radio equipment to 30 MHz.

- Specified 12.5 Volt, 30 MHz Characteristics –
  Output Power = 50 Watts
  Minimum Gain = 11 dB
  Efficiency = 50%

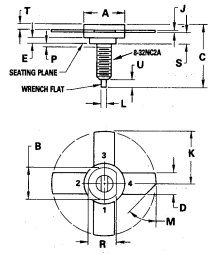


CASE 211-07
MRF450

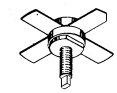


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	9.40	9.91	0.370	0.390
C	5.82	7.14	0.229	0.281
D	5.46	5.97	0.215	0.235
E	2.16	2.67	0.085	0.105
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	20.07	20.57	0.790	0.810
K	10.03	10.29	0.395	0.405
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.81	4.57	0.150	0.180
Q	2.87	3.30	0.113	0.130

STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR



CASE 145A-09
MRF450A



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.39	0.320	0.330
C	17.02	20.07	0.670	0.790
D	5.46	5.97	0.215	0.235
E	1.78	—	0.070	—
J	0.08	0.18	0.003	0.007
K	12.45	—	0.490	—
L	1.40	1.78	0.055	0.070
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.11	2.54	0.083	0.100
U	2.49	3.35	0.098	0.132

STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CBO}	40	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	— Vdc
Collector Current — Continuous	I_C	7.5	Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	115 0.66	Watts $W/^oC$
Storage Temperature Range	T_{stg}	−65 to +150	^oC

THERMAL CHARACTERISTICS

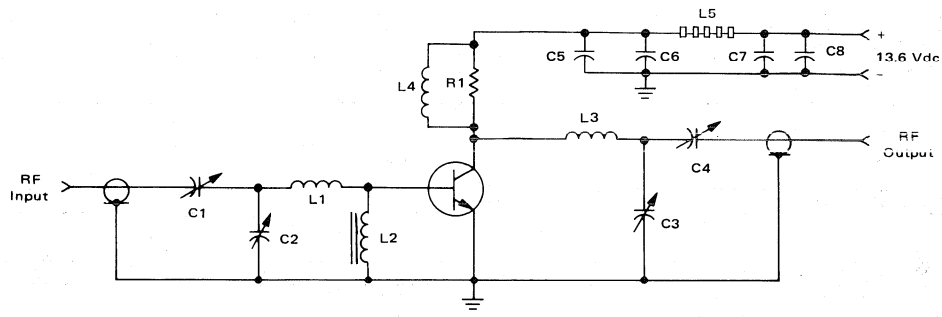
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.53	$^oC/W$

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	40	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 20 mAdc, I_E = 0)	$V_{(BR)CBO}$	40	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	–	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	–	200	pF
FUNCTIONAL TESTS (Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 13.6 Vdc, P_{out} = 50 W, I_C(max) = 6.13 Adc, f = 30 MHz)	G_{PE}	11	15	–	dB
Collector Efficiency (V_{CC} = 13.6 Vdc, P_{out} = 50 W, I_C(max) = 6.13 Adc, f = 30 MHz)	η	50	–	–	%
Series Equivalent Input Impedance (V_{CC} = 13.6 Vdc, P_{out} = 50 W; f = 30 MHz)	Z_{in}	–	1.56-j.89	–	Ohms
Series Equivalent Output Impedance (V_{CC} = 13.6 Vdc, P_{out} = 50 W, f = 30 MHz)	Z_{out}	–	174-j.50	–	Ohms

FIGURE 1 – 30 MHz TEST CIRCUIT SCHEMATIC



C1 –	14-150 pF, ARCO 424
C2,C3,C4 –	170-780 pF, ARCO 469
C5,C8 –	ERIE 0.1 μF @ 100 V RED CAPS
C6 –	1000 pF UNELCO, 350 Vdc
C7 –	10 μF, 35 Vdc
R1 –	100 Ω, 2 W Carbon
L1 –	0.15 μH Molded Choke MILLER
L2 –	FERROXCUBE, VK200-20-4B
L3 –	3 Turns, #14 Bare Tinned Wire, 0.3" (0.79) I.D. x 0.38" (0.97) Long
L4 –	9 Turns, #20 Enamal Wire, Close Wound on R1
L5 –	FERROXCUBE #56-570-65/3B, 5 Ferrite Beads, on 1" Long #20 Wire
Input/Output Connectors –	Type N
Board –	Glass Teflon Mounted on a 4" x 4" x 2" SEEZAK Box

FIGURE 2 – INPUT POWER versus OUTPUT POWER

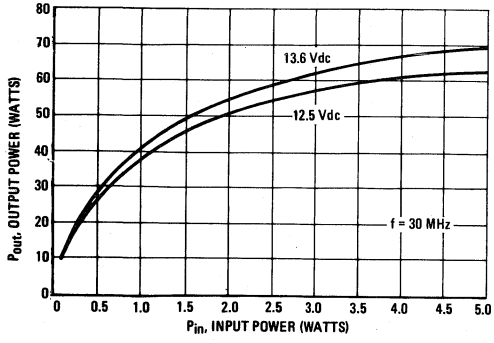
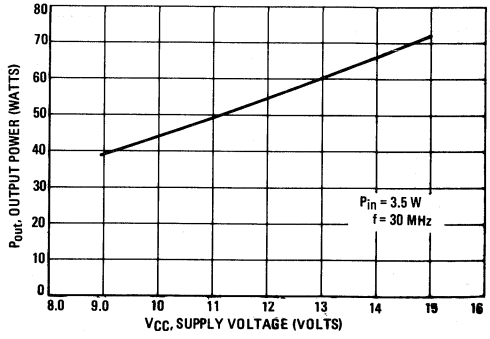


FIGURE 3 – OUTPUT POWER versus SUPPLY VOLTAGE



MRF453
MRF453A

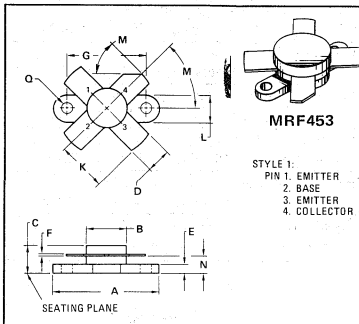
The RF Line

60 W – 30 MHz
RF POWER
TRANSISTORS
NPN SILICON

NPN SILICON RF POWER TRANSISTORS

. . . designed for power amplifier applications in industrial, commercial and amateur radio equipment to 30 MHz.

- Specified 12.5 Volt, 30 MHz Characteristics –
  Output Power = 60 Watts
  Minimum Gain = 13 dB
  Efficiency = 55%

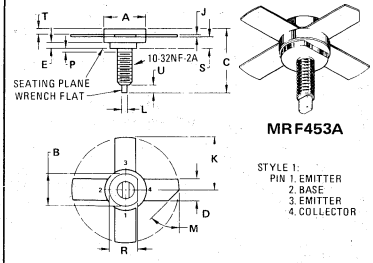


MRF453

STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.64	24.89	0.970	0.980
B	11.81	12.95	0.465	0.510
C	5.82	6.98	0.229	0.275
D	5.46	5.97	0.216	0.235
E	2.13	2.79	0.084	0.110
F	0.08	0.18	0.003	0.007
G	18.29	18.54	0.720	0.730
K	11.05	–	0.435	–
L	6.22	6.48	0.246	0.255
M	45° NOM		45° NOM	
N	3.66	4.52	0.144	0.178
Q	2.92	3.30	0.115	0.130

CASE 211-11



MRF453A

STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

NOTE:
1. 145A-10, USE 10-32NF-2A STUD.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.45	12.95	0.490	0.510
B	10.54	10.80	0.415	0.425
C	19.68	22.73	0.775	0.895
D	5.46	5.97	0.215	0.235
E	1.83	–	0.072	–
J	0.08	0.18	0.003	0.007
K	12.45	–	0.490	–
L	1.65	1.90	0.065	0.075
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
R	9.73	10.06	0.383	0.396
S	3.84	4.50	0.151	0.177
T	2.11	2.54	0.083	0.100
U	2.49	3.35	0.098	0.132

CASE 145A-10

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Emitter Voltage	V_{CES}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current – Continuous	I_C	15	Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	175 1.0	Watts $W/^oC$
Storage Temperature Range	T_{stg}	-65 to +150	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	$^oC/W$

MATCHING PROCEDURE

In the push-pull circuit configuration, it is preferred that the transistors are used as matched pairs to obtain optimum performance.

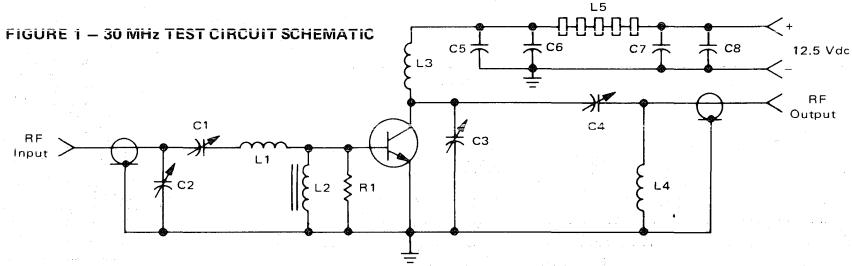
The matching procedure used by Motorola consists of measuring h_{FE} at the data sheet conditions and color coding the device to predetermined h_{FE} ranges within the normal h_{FE} limits. A color dot is added to the marking on top of the cap. Any two devices with the same color dot can be paired together to form a matched set of units.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	–	150	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	–	250	pF
FUNCTIONAL TESTS (Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 60 W, f = 30 MHz)	G_{pe}	13	–	–	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 60 W, f = 30 MHz)	η	55	–	–	%
Series Equivalent Input Impedance (V_{CC} = 12.5 Vdc, P_{out} = 60 W, f = 30 MHz)	Z_{in}	–	1.66-j.844	–	Ohms
Series Equivalent Output Impedance (V_{CC} = 12.5 Vdc, P_{out} = 60 W, f = 30 MHz)	Z_{out}	–	1.73-j.188	–	Ohms
Parallel Equivalent Input Impedance (V_{CC} = 12.5 Vdc, P_{out} = 60 W, f = 30 MHz)	Z_{in}	–	2.09/1030	–	Ω/pF
Parallel Equivalent Output Impedance (V_{CC} = 12.5 Vdc, P_{out} = 60 W, f = 30 MHz)	Z_{out}	–	1.75/330	–	Ω/pF

FIGURE 1 – 30 MHz TEST CIRCUIT SCHEMATIC



C1, C2, C4	ARCO 469	L1	3 Turns, #18 AWG, 5/16" I.D., 5/16" Long
C3	ARCO 466	L2	VK200 – 20/4B, FERROXCUBE
C5	1000 pF, UNELCO	L3	12 Turns, #18 AWG Enameled Wire, 1/4" I.D., Close Wound
C6, C7	0.1 μF Disk Ceramic	L4	3 Turns 1/8" O.D. Copper Tubing, 3/8" I.D., 3/4" Long
C8	1000 μF/15 V Electrolytic	L5	7 FERRITE Beads, FERROXCUBE #56-590-65/3B
R1	10 Ohm/1 Watt, Carbon		

FIGURE 2 – OUTPUT POWER versus INPUT POWER

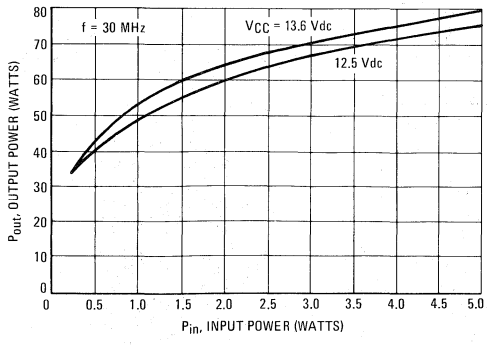
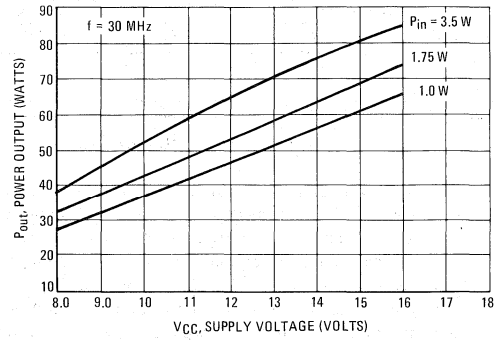


FIGURE 3 – OUTPUT POWER versus SUPPLY VOLTAGE



MRF454
MRF454A

The RF Line

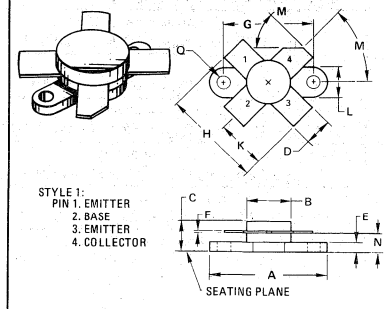
80 W – 30 MHz
RF POWER
TRANSISTORS

NPN SILICON

NPN SILICON RF POWER TRANSISTORS

. . . designed for power amplifier applications in industrial, commercial and amateur radio equipment to 30 MHz.

- Specified 12.5 Volt, 30 MHz Characteristics –
  Output Power = 80 Watts
  Minimum Gain = 12 dB
  Efficiency = 50%



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.64	24.89	0.970	0.980
B	11.81	12.95	0.465	0.510
C	5.82	6.98	0.229	0.275
D	5.46	5.97	0.216	0.235
E	2.13	2.79	0.084	0.110
F	0.08	0.18	0.003	0.007
G	18.29	18.54	0.720	0.730
K	11.05	–	0.435	–
L	6.22	6.48	0.246	0.255
M	45° NOM		45° NOM	
N	3.66	4.52	0.144	0.178
Q	2.92	3.30	0.115	0.130

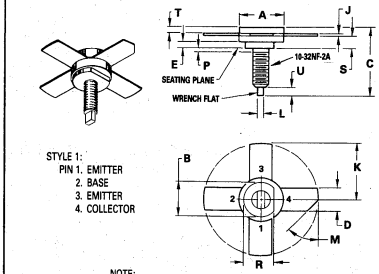
MRF454 **CASE 211-11**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	25	Vdc
Collector-Base Voltage	V_{CBO}	45	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	20	Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	250 1.43	Watts $W/^oC$
Storage Temperature Range	T_{stg}	−65 to +150	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	$^oC/W$



NOTE:
1. 145A-10, USE 10-32NF-2A STUD.

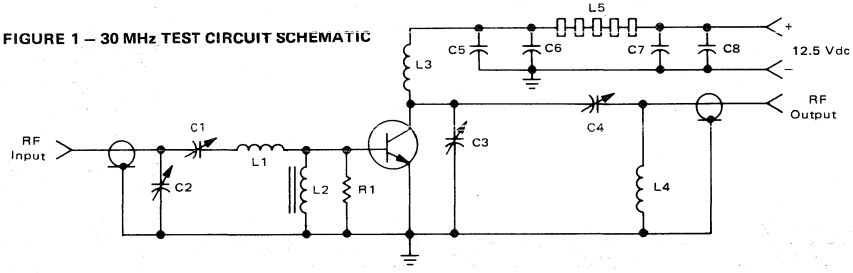
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.45	12.95	0.490	0.510
B	10.54	10.80	0.415	0.425
C	19.68	22.73	0.775	0.895
D	5.46	5.97	0.215	0.235
E	1.83	–	0.072	–
J	0.08	0.18	0.003	0.007
K	12.45	–	0.490	–
L	1.65	1.90	0.065	0.075
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
R	9.73	10.06	0.383	0.396
S	3.84	4.50	0.151	0.177
T	2.11	2.54	0.083	0.100
U	2.49	3.35	0.098	0.132

MRF454A **CASE 145A-10**

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	–	150	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	–	250	pF
FUNCTIONAL TESTS (Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 80 W, f = 30 MHz)	G_{pe}	12	–	–	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 80 W, f = 30 MHz)	η	50	–	–	%
Series Equivalent Input Impedance (V_{CC} = 12.5 Vdc, P_{out} = 80 W, f = 30 MHz)	Z_{in}	–	.938–j.341	–	Ohms
Series Equivalent Output Impedance (V_{CC} = 12.5 Vdc, P_{out} = 80 W, f = 30 MHz)	Z_{out}	–	1.16–j.201	–	Ohms
Parallel Equivalent Input Impedance (V_{CC} = 12.5 Vdc, P_{out} = 80 W, f = 30 MHz)	–	–	1.06 Ω 1817 pF	–	–
Parallel Equivalent Output Impedance (V_{CC} = 12.5 Vdc, P_{out} = 80 W, f = 30 MHz)	–	–	1.19 Ω 777 pF	–	–

FIGURE 1 – 30 MHz TEST CIRCUIT SCHEMATIC



C1, C2, C4 ARCO 469
C3 ARCO 466
C5 1000 pF, UNELCO
C6, C7 0.1 μF Disk Ceramic
C8 1000 μF/15 V Electrolytic
R1 10 Ohm/1 Watt, Carbon

L1 3 Turns, #18 AWG, 5/16" I.D., 5/16" Long
L2 VK200 – 20/4B, FERROXCUBE
L3 12 Turns, #18 AWG Enameled Wire, 1/4" I.D., Close Wound
L4 3 Turns 1/8" O.D. Copper Tubing, 3/8" I.D., 3/4" Long
L5 7 FERRITE Beads, FERROXCUBE #56-590-65/3B

FIGURE 2 – OUTPUT POWER versus INPUT POWER

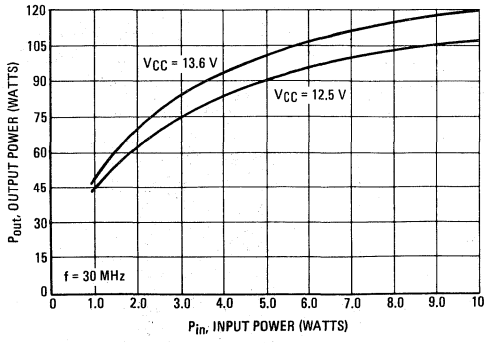
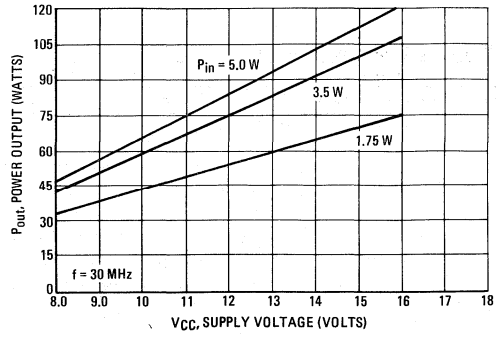


FIGURE 3 – OUTPUT POWER versus SUPPLY VOLTAGE



MRF455
MRF455A

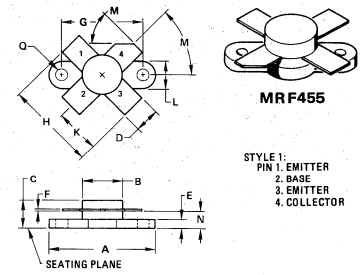
The RF Line

NPN SILICON RF POWER TRANSISTORS

. . . designed for power amplifier applications in industrial, commercial and amateur radio equipment to 30 MHz.

- Specified 12.5 Volt, 30 MHz Characteristics –
  Output Power = 60 Watts
  Minimum Gain = 13 dB
  Efficiency = 55%

60 W – 30 MHz
RF POWER
TRANSISTORS
NPN SILICON



MRF455

STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	24.64	24.89	0.970	0.980
B	9.40	9.91	0.370	0.390
C	5.82	7.14	0.229	0.281
D	5.46	5.97	0.215	0.235
E	2.16	2.67	0.085	0.105
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	20.07	20.57	0.790	0.810
K	10.03	10.29	0.395	0.405
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.81	4.57	0.150	0.180
Q	2.87	3.30	0.113	0.130

CASE 211-07

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Emitter Voltage	V_{CES}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	15	Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	175 1.0	Watts $W/^oC$
Storage Temperature Range	T_{stg}	−65 to +150	^oC

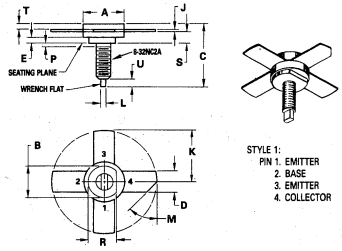
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	$^oC/W$

MATCHING PROCEDURE

In the push-pull circuit configuration it is preferred that the transistors are used as matched pairs to obtain optimum performance.

The matching procedure used by Motorola consists of measuring h_{FE} at the data sheet conditions and color coding the device to predetermined h_{FE} ranges within the normal h_{FE} limits. A color dot is added to the marking on top of the cap. Any two devices with the same color dot can be paired together to form a matched set of units.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	17.02	20.07	0.670	0.790
D	5.46	5.97	0.215	0.235
E	1.78	—	0.070	—
J	0.08	0.18	0.003	0.007
K	12.45	—	0.490	—
L	1.40	1.78	0.055	0.070
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.11	2.54	0.083	0.100
U	2.49	3.35	0.098	0.132

CASE 145A-09

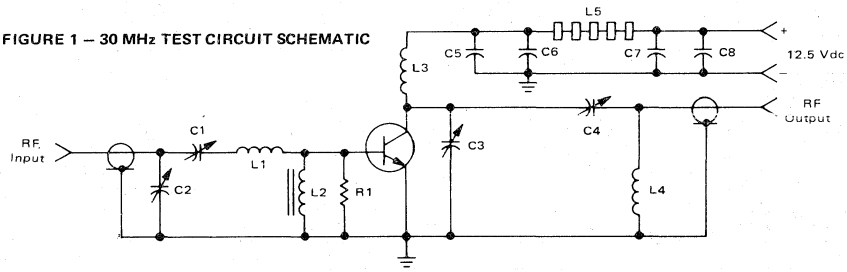
3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	–	150	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	–	250	pF
FUNCTIONAL TESTS (Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 60 W, f = 30 MHz)	G_{pe}	13	–	–	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 60 W, f = 30 MHz)	η	55	–	–	%
Series Equivalent Input Impedance (V_{CC} = 12.5 Vdc, P_{out} = 60 W, f = 30 MHz)	Z_{in}	–	1.66-j.844	–	Ohms
Series Equivalent Output Impedance (V_{CC} = 12.5 Vdc, P_{out} = 60 W, f = 30 MHz)	Z_{out}	–	1.73-j.188	–	Ohms
Parallel Equivalent Input Impedance (V_{CC} = 12.5 Vdc, P_{out} = 60 W, f = 30 MHz)	Z_{in}	–	2.09/1030	–	Ω/pF
Parallel Equivalent Output Impedance (V_{CC} = 12.5 Vdc, P_{out} = 60 W, f = 30 MHz)	Z_{out}	–	1.75/330	–	Ω/pF

3

FIGURE 1 – 30 MHz TEST CIRCUIT SCHEMATIC



C1, C2, C4	ARCO 469	L1	3 Turns, #18 AWG, 5/16" I.D., 5/16" Long
C3	ARCO 466	L2	VK200 – 20/4B, FERROXCUBE
C5	1000 pF, UNELCO	L3	12 Turns, #18 AWG Enameled Wire, 1/4" I.D., Close Wound
C6, C7	0.1 μF Disk Ceramic	L4	3 Turns 1/8" O.D. Copper Tubing, 3/8" I.D., 3/4" Long
C8	1000 μF/15 V Electrolytic	L5	7 FERRITE Beads, FERROXCUBE #56-590-65/3B
R1	10 Ohm/1 Watt, Carbon		

FIGURE 2 – OUTPUT POWER versus INPUT POWER

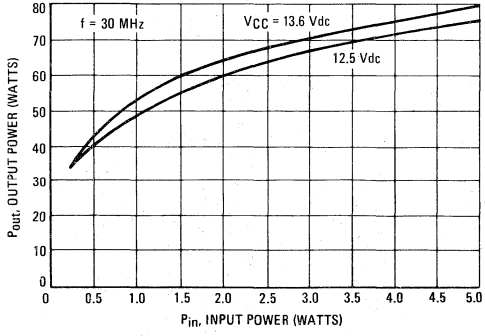
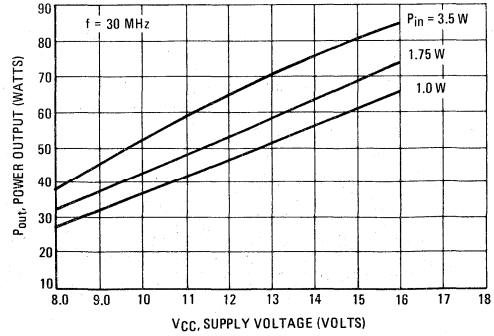


FIGURE 3 – OUTPUT POWER versus SUPPLY VOLTAGE



MRF458
MRF458A

The RF Line

NPN SILICON RF POWER TRANSISTOR

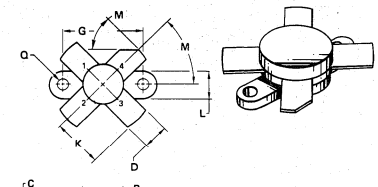
. . . designed for power amplifier applications in industrial, commerical and amateur radio equipment to 30 MHz.

- Specified 12.5 Volt, 30 MHz Characteristics —
  Output Power = 80 Watts
  Minimum Gain = 12 dB
  Efficiency = 50%
- Capable of Withstanding 30:1 Load VSWR @ Rated P_{out} and V_{CC}

80 W — 30 MHz

RF POWER TRANSISTOR

NPN SILICON



STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	24.64	24.89	0.970	0.980
B	11.81	12.95	0.465	0.510
C	5.82	6.98	0.229	0.275
D	5.46	5.97	0.216	0.235
E	2.13	2.79	0.084	0.110
F	0.08	0.18	0.003	0.007
G	18.29	18.54	0.720	0.730
K	11.05	–	0.435	–
L	6.22	6.48	0.246	0.255
M	45° NOM		45° NOM	
N	3.66	4.52	0.144	0.178
Q	2.92	3.30	0.115	0.130

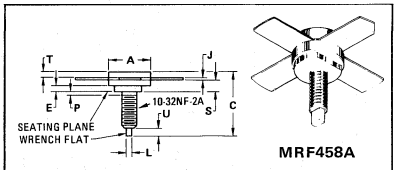
CASE 211-11

MAXIMUM RATINGS

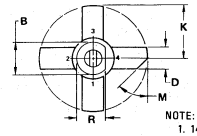
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	10	Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	175 1.0	Watts $W/^oC$
Storage Temperature Range	T_{stg}	−65 to +150	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	$^oC/W$



MRF458A



NOTE:
1. 145A-10, USE 10-32NF-2A STUD.

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	12.45	12.95	0.490	0.510
B	10.54	10.80	0.415	0.425
C	19.68	22.73	0.775	0.895
D	5.46	5.97	0.215	0.235
E	1.83	–	0.072	–
J	0.08	0.18	0.003	0.007
K	12.45	–	0.490	–
L	1.65	1.90	0.065	0.075
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
R	9.73	10.06	0.383	0.396
S	3.84	4.50	0.151	0.177
T	2.11	2.54	0.083	0.100
U	2.49	3.35	0.098	0.132

STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

CASE 145A-10

MATCHING PROCEDURE

In the push-pull circuit configuration, it is preferred that the transistors are used as matched pairs to obtain optimum performance.

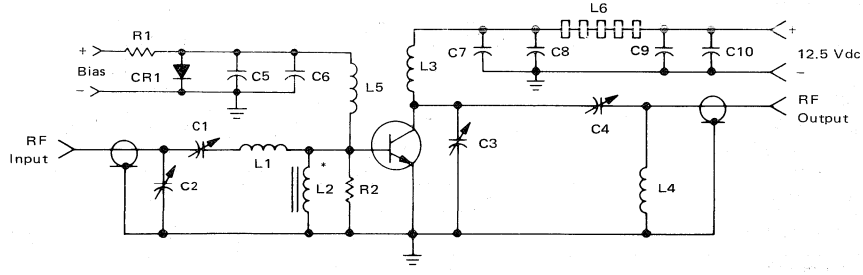
The matching procedure used by Motorola consists of measuring h_{FE} at the data sheet conditions and color coding the device to predetermined h_{FE} ranges within the normal h_{FE} limits. A color dot is added to the marking on top of the cap. Any two devices with the same color dot can be paired together to form a matched set of units.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 50 mAdc, I_E = 0)	$V_{(BR)CBO}$	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	–	150	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	–	300	pF
FUNCTIONAL TESTS (Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 80 W, f = 30 MHz)	G_{PE}	12	–	–	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 80 W, f = 30 MHz)	η	50	–	–	%
Intermodulation Distortion (V_{CC} = 12.5 Vdc, P_{out} = 70 W PEP, f = 30, 30.001 MHz	IMD_3 IMD_5	– –	–32 –35	– –	dB

3

FIGURE 1 – 30 MHz TEST CIRCUIT SCHEMATIC



C1, C2, C4 – ARCO 469
C3 – ARCO 466
C5 – ERIE 0.1 μF, 100 V
C6 – 500 μF, 15 V Electrolytic
C7 – 1000 pF, UNELCO
C8, C9 – 0.1 μF Disk Ceramic
C10 – 100 μF, 15 V Electrolytic
CR1 – 1N4997
R1 – 10 Ω, 25 Watt Wirewound
R2 – 10 Ohm, 1 Watt, Carbon

L1 – 3 Turns #18 AWG, 5/16" I.D., 5/16" Long
L2, L5 – VK200 – 20/4B, FERROXCUBE
L3 – 12 Turns, #18 AWG Enameled Wire, 1/4" I.D., Close Wound
L4 – 3 Turns 1/8" O.D. Copper Tubing, 3/8" I.D., 3/4" Long
L6 – 7 FERRITE Beads, FERROXCUBE #56-590-65/3B

*NOTE: For Class C operation bias network (R1, R2, CR1, C5, C6, L5) is not used.
For Class AB operation L2 is not used.

TYPICAL PERFORMANCE CURVES

FIGURE 2 – POWER GAIN versus FREQUENCY

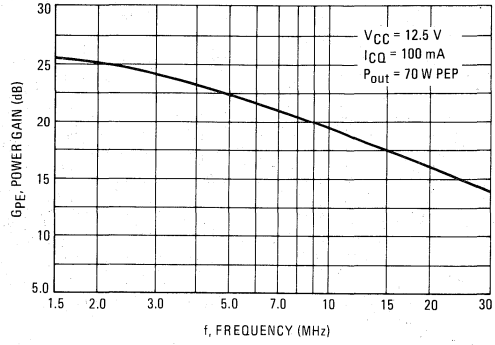


FIGURE 3 – OUTPUT RESISTANCE versus FREQUENCY

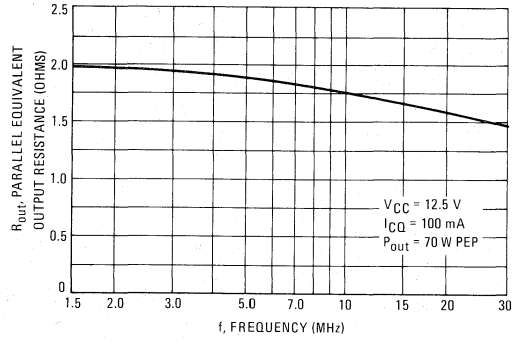
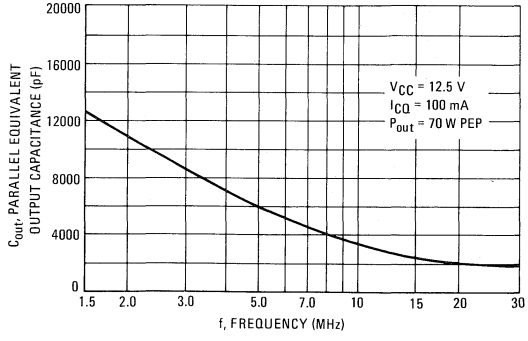
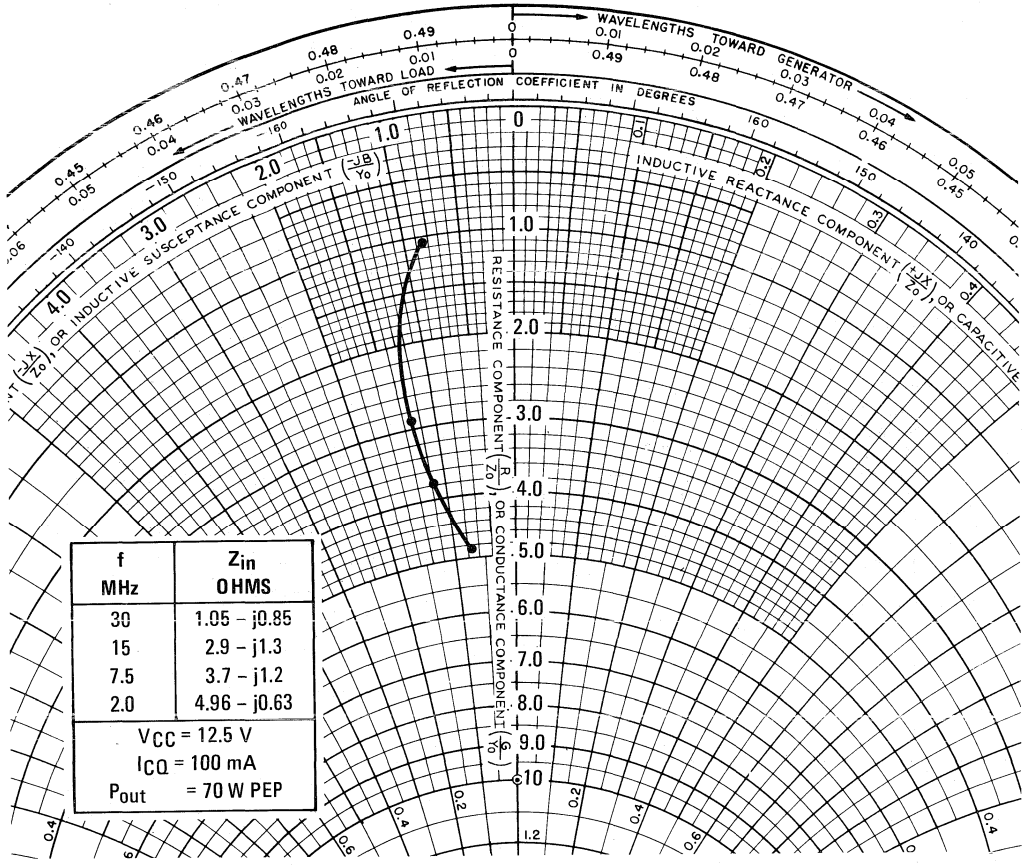


FIGURE 4 – OUTPUT CAPACITANCE versus FREQUENCY



3

FIGURE 5 – SERIES EQUIVALENT INPUT-OUTPUT IMPEDANCE



MRF460

The RF Line

40 W (PEP) – 30 MHz

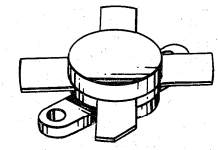
RF POWER
TRANSISTOR

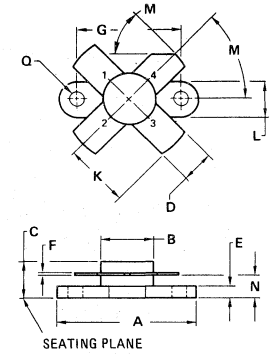
NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed primarily for applications as a high-power linear amplifier from 2.0 to 30 MHz.

- Specified 12.5 Volt, 30 MHz Characteristics –
  Output Power = 40 W (PEP)
  Minimum Gain = 12 dB
  Efficiency = 40%
- Intermodulation Distortion at Rated Power Output –
  IMD = -30 dB (Max)
- Isothermal-Resistor Design Results in Rugged Device
- Replacement for 2N6368





STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.64	24.89	0.970	0.980
B	11.81	12.95	0.465	0.510
C	5.82	6.98	0.229	0.275
D	5.46	5.97	0.216	0.235
E	2.13	2.79	0.084	0.110
F	0.08	0.18	0.003	0.007
G	18.29	18.54	0.720	0.730
K	11.05	–	0.435	–
L	6.22	6.48	0.246	0.255
M	45° NOM		45° NOM	
N	3.66	4.52	0.144	0.178
Q	2.92	3.30	0.115	0.130

CASE 211-11

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CBO}	40	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current – Continuous	I_C	15	Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	175 1.0	Watts $W/^oC$
Storage Temperature Range	T_{stg}	−65 to +150	^oC

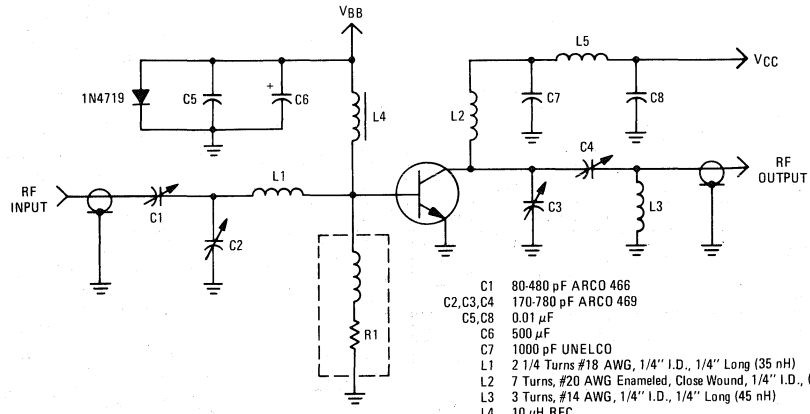
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	40	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 12.5 Vdc, V_{BE} = 0, T_C = +55°C)	I_{CES}	–	–	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	40	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	300	350	pF
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (Figure 1) (P_{out} = 40 W (PEP), I_C = 4.7 Adc Max, V_{CC} = 12.5 Vdc, I_{CQ} = 50 mAdc, f_1 = 30 MHz, f_2 = 30.001 MHz)	G_{PE}	12	15	–	dB
Intermodulation Distortion Ratio (Figure 1) (P_{out} = 40 W (PEP), I_C = 4.7 Adc Max, V_{CC} = 12.5 Vdc, I_{CQ} = 50 mAdc, f_1 = 30 MHz, f_2 = 30.001 MHz)	IMD	–	-35	-30	dB
Collector Efficiency (Figure 1) (P_{out} = 40 W (PEP), I_C = 4.7 Adc Max, V_{CC} = 12.5 Vdc, I_{CQ} = 50 mAdc, f_1 = 30 MHz, f_2 = 30.001 MHz)	η	40	45	–	%

3

*Indicates JEDEC Registered Data.

FIGURE 1 – 30 MHz TEST CIRCUIT



C1	80-480 pF ARCO 466
C2,C3,C4	170-780 pF ARCO 469
C5,C8	0.01 μF
C6	500 μF
C7	1000 pF UNELCO
L1	2 1/4 Turns #18 AWG, 1/4" I.D., 1/4" Long (35 nH)
L2	7 Turns, #20 AWG Enameled, Close Wound, 1/4" I.D., (0.2 μH)
L3	3 Turns, #14 AWG, 1/4" I.D., 1/4" Long (45 nH)
L4	10 μH RFC
L5	RF Choke Ferroxcube VK200-20-4B
R1	10 Ohms, Wirewound, 1 W (0.25 μH Inductance)

FIGURE 2 – OUTPUT POWER versus INPUT POWER

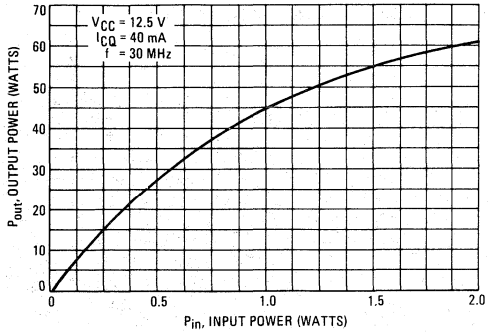


FIGURE 3 – POWER GAIN versus FREQUENCY

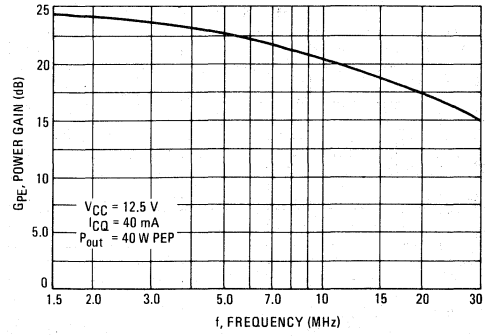


FIGURE 4 – INTERMODULATION DISTORTION versus OUTPUT POWER

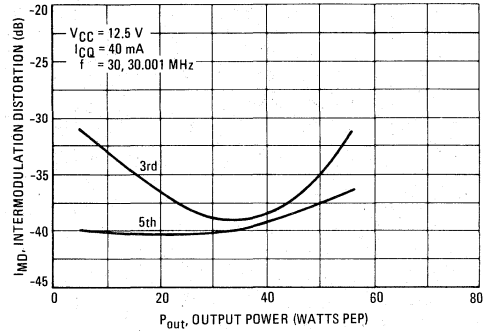


FIGURE 5 – OUTPUT POWER versus SUPPLY VOLTAGE

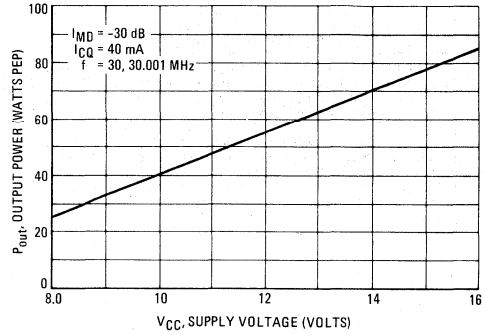


FIGURE 6 – OUTPUT RESISTANCE versus FREQUENCY

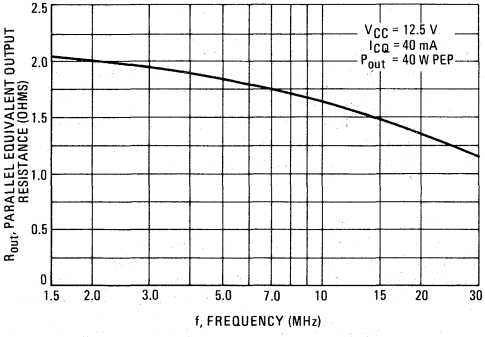
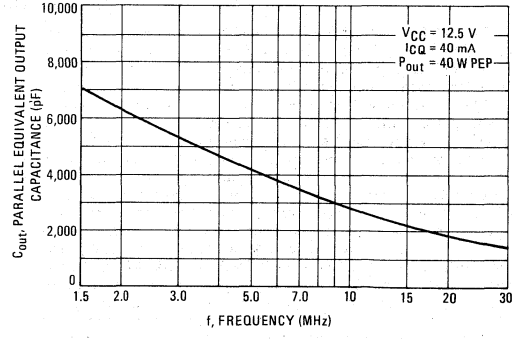


FIGURE 7 – OUTPUT CAPACITANCE versus FREQUENCY



3

FIGURE 8 – DC SAFE OPERATING AREA

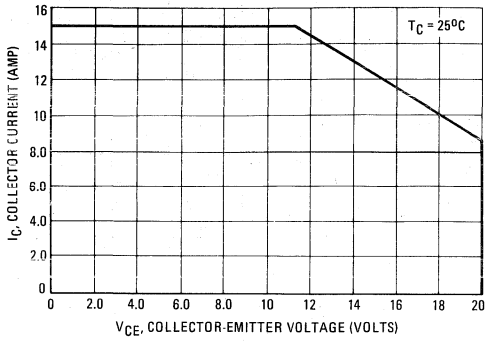
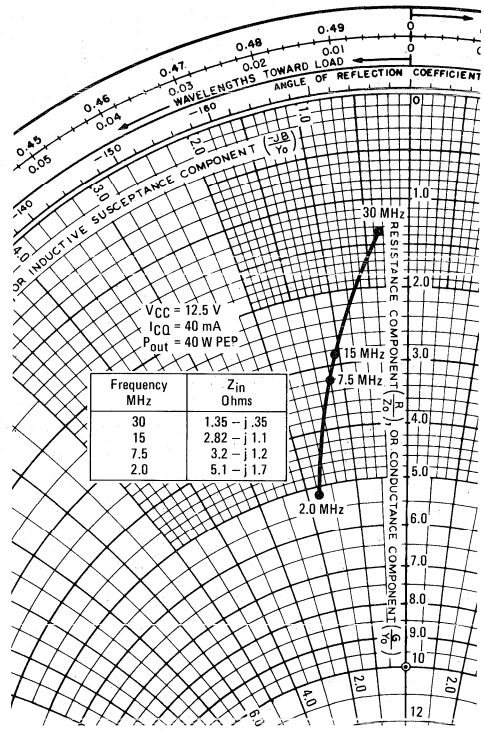


FIGURE 9 – SERIES EQUIVALENT IMPEDANCE



Frequency MHz	Z_{in} Ohms
30	1.35 – j .35
15	2.82 – j 1.1
7.5	3.2 – j 1.2
2.0	5.1 – j 1.7

MATCHING PROCEDURE

In the push-pull circuit configuration two device parameters are critical for optimum circuit performance. These parameters are $V_{BE(on)}$ and h_{FE}. Both parameters can be guaranteed by measuring I_{CQ} of the devices and selecting pairs with a $\Delta I_{CQ} \leq 10$ mAdc.

Actual I_{CQ} matching is performed in the MRF460 test circuit with a V_{CE} equal to 28 Volts. The base bias supply is adjusted to set I_{CQ} equal to 40 mAdc using a reference standard MRF460. The production MRF460s are tested and categorized in ranges of 10 mAdc. Finally, the devices are stocked as pairs with a guaranteed $\Delta I_{CQ} \leq 10$ mAdc.

APPLICATIONS INFORMATION

The MRF460 transistor is designed for linear power amplifier operation in the HF region (2 to 30 MHz). It features guaranteed linear amplifier performance rather than the conventional performance demonstrated in a class C* amplifier.

Class C operation is inherently non-linear, but in many power amplifier applications non-linear operation does not present major problems. With a single frequency driving signal, the only spurious signals generated are harmonics and these can be supressed in the amplifier tuned networks and output filter.

For single sideband (SSB), low level amplitude modulation (AM), and other types of complex signals, class C operation is generally not satisfactory. For instance, when a signal contains multiple frequencies at close spacings, odd-order non-linearities will generate spurious outputs which are within the passband of the tuned circuits and filters; therefore, the spurious outputs are not suppressed before they reach the antenna or other load. As a result, such complex signals require linear amplification if the amplified signal is to be free of spurious outputs.

A detailed analysis of spurious signals generated by non-linearities and linearity requirements of various applications is described in Chapter 12 of Reference 1.

The following discussion concerns itself with a detailed description of the MRF460 characterization curves and general information on solid-state linear power amplifier design.

*"Class C", as used here refers to operation with the no signal conditions $I_C = 0$, and $V_{BE} = 0$, and a theoretical conduction angle of less than 180°, even though the actual conduction angle may be more than 180°.

The Two-Tone Test

The MRF460 functional test specifications consist of a linear power amplifier test with guaranteed limits on power output, gain, efficiency, and intermodulation distortion (IMD) output levels. A two-tone test signal is used with the test amplifier as shown in Figure 1.

The two-tone test is one of many methods commonly used for testing linear amplifier performance. This test involves driving the amplifier with two RF signals, of equal amplitude, separated in frequency from each other by approximately 1 kHz.

APPLICATIONS INFORMATION (continued)

When a two-tone test signal consisting of frequencies f_1 and f_2 is passed through a non-linear amplifier, odd order non-linearities generate spurious signals near the desired carrier. The level of these spurious signals provides a measure of the degree of non-linearity of the amplifier. This type of non-linearity is called intermodulation distortion (IMD). The spurious signals generated by IMD are further classified according to the exponential order of the amplifier non-linearity, i.e., 3rd order IMD products, 5th order IMD products, etc. The 3rd and 5th order IMD products are usually the most significant encountered with linear power amplifiers. Data on both 3rd and 5th order IMD are included in the MRF460 characterization.

Third order IMD generates spurious signals near the operating frequency at frequencies $2f_1 - f_2$ and $2f_2 - f_1$; and 5th order IMD spurious are at frequencies $3f_1 - 2f_2$ and $3f_2 - 2f_1$.

Specifications and Characterization

The two-tone functional amplifier test is performed in a manner identical to the conventional class C functional test with two exceptions: a two-frequency signal is used in place of a single frequency, and amplifier linearity is added to the items tested and specified.

The functional test procedure for the MRF460 requires driving the test amplifier with a two-frequency signal and measuring power output, gain, efficiency, and linearity.

Power output, gain and efficiency measurement methods are the same for both linear and class C amplifier.

Since a multiple frequency test signal has an instantaneous power level which varies with time, power levels are normally expressed in peak envelope power (PEP). This is the average power level of the envelope at its greatest amplitude point.

When the test signal consists of multiple signals with equal amplitudes and different frequencies, the relationship of average power and PEP is given by the following expression:

$$\text{Average power} = \frac{\text{PEP}}{N}$$

where N = the number of input frequencies.

Therefore, when measuring the power level of a standard two-tone test signal, a true average reading power meter will indicate 1/2 the PEP of the signal.

Linearity is tested by measuring the amplitudes of the 3rd and 5th order IMD products. The ratio of one of the 3rd order products to one of the two desired frequencies is then expressed as a power ratio in decibels (dB). This is repeated for the 5th order products. The smaller of these two ratios (usually the 3rd order) is then included in the electrical characteristics specifications as intermodulation distortion ratio (IMD).

MRF460 Performance Curves

Figures 2 and 3 show typical power output and gain characteristics versus frequency and/or input power. These curves are similar to those found on other RF power transistor data sheets with one exception, a two-frequency test signal was used rather than a single frequency signal.

The curves shown in Figure 4 are unique to transistors characterized for linear power amplifier service and show the typical IMD levels versus power output.

The MRF460 features guaranteed IMD performance at the -30 dB level. However, the designer may desire IMD greater or less than -30 dB for a particular application. Figure 4 provides data on IMD levels that can be expected as a function of output power.

Figure 5 reflects the power output that can be obtained at a fixed IMD ratio for operation with dc supply voltages other than 12.5 Vdc.

Figures 6 and 7 show the large signal impedance characteristics of the MRF460. These are similar to curves shown on other Motorola data sheets except a two-frequency test signal was used rather than a single frequency signal.

It must be stressed that the data shown in Figures 6 and 7 do not represent y, z, h, s, or any standard two-port parameter set. The actual transistor impedance levels during normal operation in a power amplifier are given. For a detailed discussion of RF power transistor large signal impedance, see Reference 2.

Linear Amplifier Design

The following is a discussion of some general design considerations for solid-state linear power amplifiers. While this is not a detailed analysis of linear amplifier design, some general guidelines are provided.

The major difference between linear power amplifiers and class C power amplifiers is in the dc bias circuitry. As stated in the introduction, class C operation usually involves a collector dc supply as the only bias voltage with $V_E = V_B = 0$. The collector current is zero until the input RF signal turns the transistor "on."

In contrast, a linear amplifier is normally operated with forward bias and some collector current flowing when no signal is present.

The magnitude of no-signal collector current and the bias circuitry may vary with the application. Optimum no-signal collector current for the MRF460 was found to be approximately 50 mA.

The key to bias circuitry for good linearity lies in maintaining the base-emitter dc voltage relatively constant as the RF signal amplitude varies. The inherent nature of a forward-biased RF power transistor is to bias itself "off" with increasing RF drive signal. Therefore, a constant voltage source is required for base voltage.

Temperature effects also complicate the situation, since V_{BE} decreases with increasing temperature.

A simple solution to the bias problem involves the use of a forward-biased diode mounted on the transistor heat sink for thermal coupling to the transistor. A sample of this technique is shown in the test circuit of Figure 1. The reader is referred to reference 3 for a detailed description of the operation of this bias circuit. It is also possible to use complex active circuitry for biasing, and some rather exotic schemes have been developed to provide the same results.

Another important consideration is the collector-output network. Normally, a network with low impedance to ground for harmonics provides better linearity than a network with high harmonic impedances; therefore, some experimentation with network configuration is in order. Proper impedance matching remains the primary factor in both input and output network design. Further, it must also be stressed that the collector load impedance should be designed for the PEP, not the average power output. See Chapter 13 of Reference 1 for a detailed discussion of network design considerations.

Feedback may also be employed to improve linearity and may take the form of either neutralization or negative RF feedback. The possibilities here are limited only by the designer's imagination. Of course, negative RF feedback involves a decrease in gain to improve linearity.

REFERENCES

1. Pappenfus, Bruene, Schoenike, "Single Sideband Principles and Circuits", McGraw-Hill.
2. Hejhall, "Systemizing RF Power Amplifier Design", Motorola Semiconductor Products Inc., Application Note AN-282A.
3. Hejhall, "Solid-State Linear Power Amplifier Design," Motorola Semiconductor Products Inc., Application Note AN-546.

MRF464
MRF464A

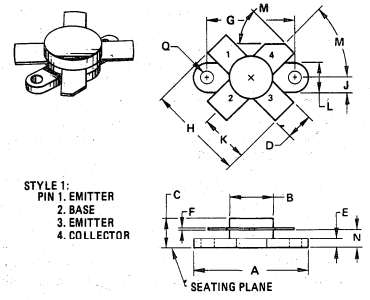
The RF Line

NPN SILICON RF POWER TRANSISTORS

. . . designed primarily for applications as a high-power linear amplifier from 2.0 to 30 MHz, in single sideband mobile, marine and base station equipment.

- Specified 28 Volt, 30 MHz Characteristics –
  Output Power = 80 W (PEP)
  Minimum Gain = 15 dB
  Efficiency = 40%
  Intermodulation Distortion = -32 dB (Max)

80 W (PEP) – 30 MHz
RF POWER
TRANSISTOR
NPN SILICON



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	24.38	25.15	0.960	0.990
B	9.40	9.91	0.370	0.390
C	5.82	7.14	0.229	0.281
D	5.46	5.97	0.215	0.235
E	2.16	2.67	0.085	0.105
F	0.10	0.15	0.004	0.006
G	18.28	18.54	0.720	0.730
H	20.07	20.57	0.790	0.810
K	10.03	10.28	0.395	0.405
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.81	4.57	0.150	0.180
Q	2.87	3.30	0.113	0.130

MRF464 CASE 211-11

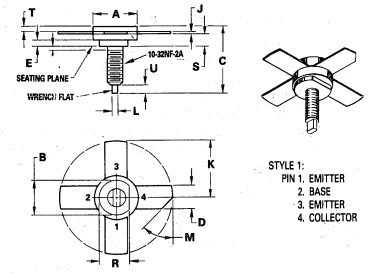
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	35	Vdc
Collector-Base Voltage	V_{CBO}	65	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current – Continuous	I_C	10	Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	250 1.4	Watts $W/^oC$
Storage Temperature Range	T_{stg}	−65 to +150	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	$^oC/W$
Stud Torque (1)	–	8.5	In. Lb

(1) Case 145A-08 – For Repeated Assembly Use 11 In. Lb.



NOTE:
1. 145A-10, USE 10-32NF-2A STUD.

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	12.45	12.95	0.490	0.510
B	10.54	10.80	0.415	0.425
C	19.68	22.73	0.775	0.895
D	5.46	5.97	0.215	0.235
E	1.83	—	0.072	—
J	0.08	0.18	0.003	0.007
K	12.45	—	0.490	—
L	1.65	1.90	0.065	0.075
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
R	9.73	10.06	0.383	0.396
S	3.84	4.50	.0.151	0.177
T	2.11	2.54	0.083	0.100
U	2.49	3.35	0.098	0.132

MRF464A CASE 145A-10

MATCHING PROCEDURE

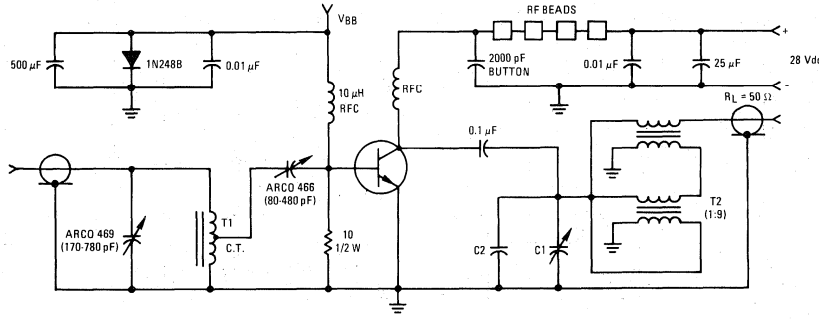
In the push-pull circuit configuration it is preferred that the transistors are used as matched pairs to obtain optimum performance.

The matching procedure used by Motorola consists of measuring h_{FE} at the data sheet conditions and color coding the device to predetermined h_{FE} ranges within the normal h_{FE} limits. A color dot is added to the marking on top of the cap. Any two devices with the same color dot can be paired together to form a matched set of units.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, I_B = 0)	$V_{(BR)CEO}$	35	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	65	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	Vdc
Collector Cutoff Current (V_{CE} = 28 Vdc, V_{BE} = 0, T_C = +55°C)	I_{CES}	–	10	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	–	–
DYNAMIC CHARACTERISTICS				
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	200	pF
FUNCTIONAL TEST				
Common-Emitter Amplifier Power Gain (Figure 1) (P_{out} = 80 W (PEP), I_C = 3.6 Adc (Max), V_{CC} = 28 Vdc, f_1 = 30 MHz, f_2 = 30.001 MHz)	G_{PE}	15	–	dB
Intermodulation Distortion Ratio (Figure 1) (P_{out} = 80 W (PEP), I_C = 3.6 Adc (Max), V_{CC} = 28 Vdc, f_1 = 30 MHz, f_2 = 30.001 MHz)	IMD	–	-32	dB
Collector Efficiency (P_{out} = 80 W (PEP), I_C = 3.6 Adc (Max), V_{CC} = 28 Vdc, f_1 = 30 MHz, f_2 = 30.001 MHz)	η	40	–	%

FIGURE 1–30 MHz TEST CIRCUIT



RFC: 20 TURNS #12 AWG ENAMELED WIRE CLOSE WOUND IN 2 LAYERS, 1/4" I.D.
T1: 20 TURNS #24 AWG WIRE WOUND ON MICRO-METALS T37-7 TOROID CORE CENTER TAPPED.
T2: 1:9 XFMR; 6 TURNS OF 2 TWISTED PAIRS OF #28 AWG ENAMELED WIRE. (8 CRESTS PER INCH) BIFILAR WOUND ON EACH OF 2 SEPARATE BALUN CORES. (Stackpole #57-1503, No. 14 Material) Interconnected as shown
RF BEADS: FERROXCUBE #56-590-65/3B

V_{BB} adjusted for I_{CQ}: 40 mAdc (I_{CQ} = Quiescent Collector Current)

C1 – 170-180 pF ARCO 469 or Equiv.

C2 – 330 pF

3

FIGURE 2 – OUTPUT POWER versus INPUT POWER

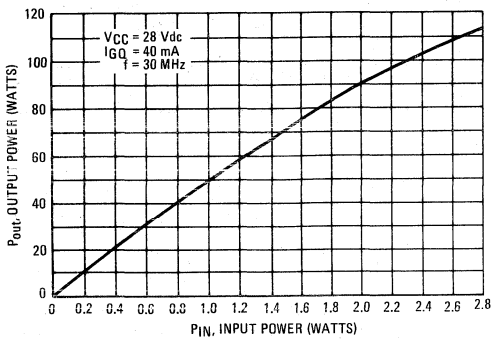


FIGURE 3 – POWER GAIN versus FREQUENCY

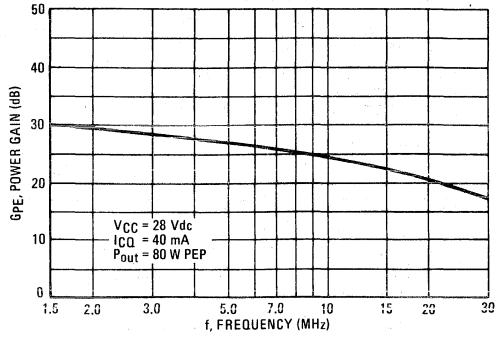


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

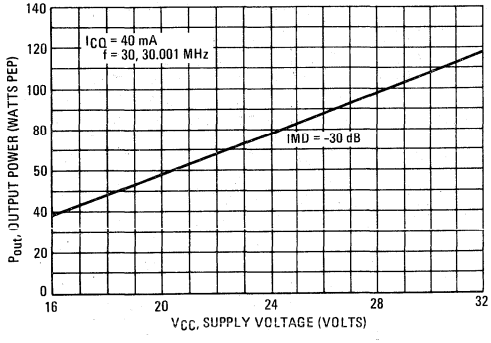


FIGURE 5 – INTERMODULATION DISTORTION versus OUTPUT POWER

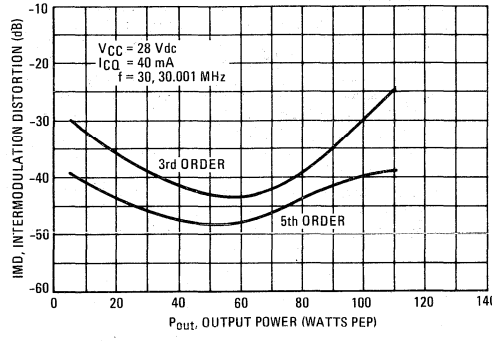


FIGURE 6 – OUTPUT CAPACITANCE versus FREQUENCY

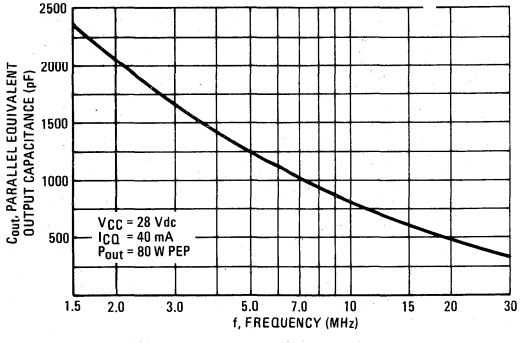


FIGURE 7 – OUTPUT RESISTANCE versus FREQUENCY

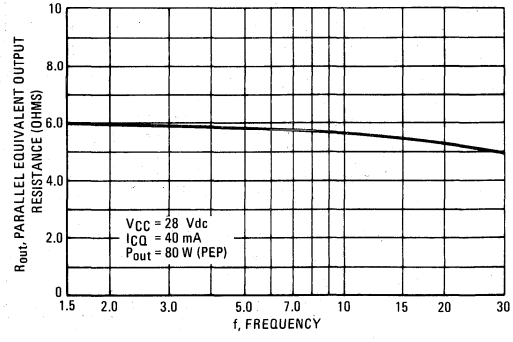


FIGURE 8 – DC SAFE OPERATING AREA

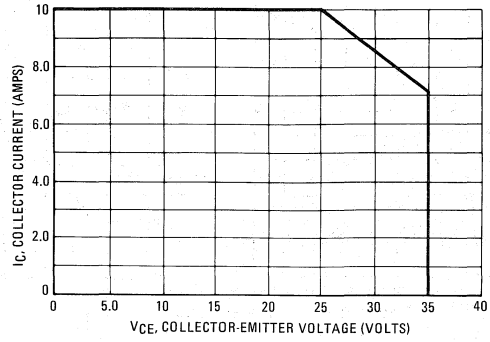
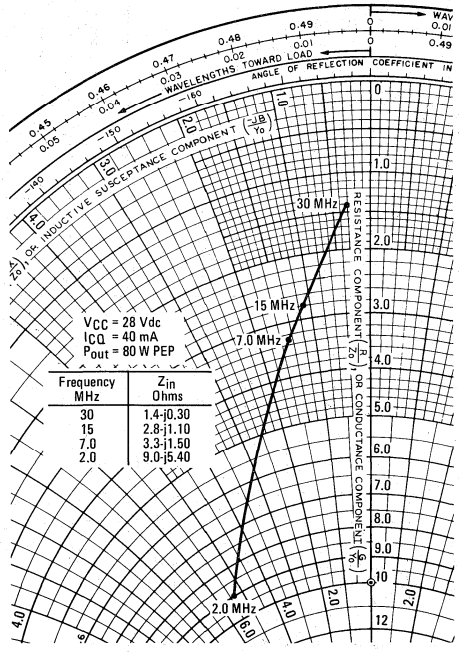


FIGURE 9 – SERIES INPUT IMPEDANCE



Frequency MHz	Z_{in} Ohms
30	1.4-j0.30
15	2.8-j1.10
7.0	3.3-j1.50
2.0	9.0-j5.40

MRF466

The RF Line

NPN SILICON RF POWER TRANSISTOR

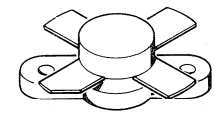
. . . designed primarily for applications as a high-power amplifier from 2.0 to 30 MHz, in single sideband mobile, marine and base station equipment.

- Specified 28 V, 30 MHz Characteristics —
  Output Power = 40 W PEP or CW
  Minimum Gain = 15 dB
  Efficiency = 40%
  Intermodulation Distortion d_3 = -30 dB Max
- Guaranteed Ruggedness
- 2N5941 Replacement

40 W (PEP) 30 MHz

RF POWER TRANSISTOR

NPN SILICON



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	35	Vdc
Collector-Base Voltage	V_{CBO}	65	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Continuous	I_C	6.0	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	175 1.0	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

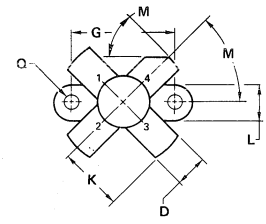
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	1.0	°C/W

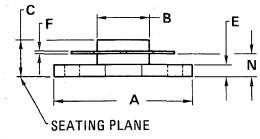
(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.
(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

MATCHING PROCEDURE

In the push-pull circuit configuration it is preferred that the transistors are used as matched pairs to obtain optimum performance.

The matching procedure used by Motorola consists of measuring h_{FE} at the data sheet conditions and color coding the device to predetermined h_{FE} ranges within the normal h_{FE} limits. A color dot is added to the marking on top of the cap. Any two devices with the same color dot can be paired together to form a matched set of units.





STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.64	24.89	0.970	0.980
B	9.40	9.91	0.370	0.390
C	5.82	7.14	0.229	0.281
D	5.46	5.97	0.215	0.235
E	2.29	2.79	0.090	0.110
F	0.08	0.18	0.003	0.007
G	18.29	18.54	0.720	0.730
K	11.05	–	0.435	–
L	6.22	6.48	0.245	0.255
M	45° NOM		45° NOM	
N	3.81	4.57	0.150	0.180
Q	2.87	3.30	0.113	0.130

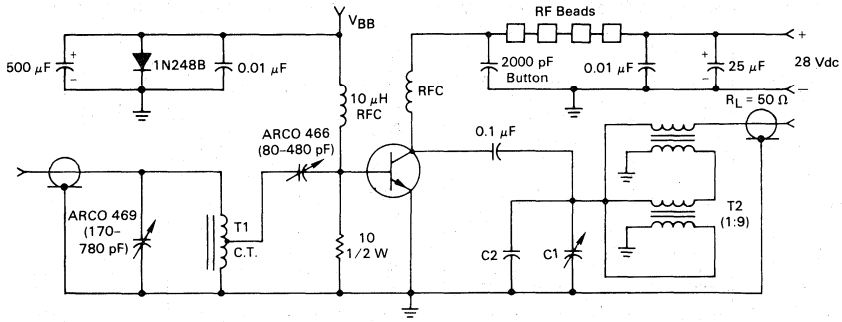
CASE 211-09

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, I_B = 0)	$V_{(BR)CEO}$	35	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	65	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mADC, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 28 Vdc, V_{BE} = 0)	I_{CES}	—	—	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	40	80	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	125	200	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 40 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 20 mA)	G_{PE}	15	19	—	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 40 W (PEP), f1 = 30 MHz f2 = 30.001 MHz, I_{CQ} = 20 mA)	η	40	—	—	%
Intermodulation Distortion (1) (V_{CC} = 28 Vdc, P_{out} = 40 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 20 mA)	$IMD_{(d3)}$	—	-40	-30	dB
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 40 W (PEP), f = 30 MHz, VSWR = 30:1 All Angles)	—	No Degradation in Poutput Power			

(1) To MIL-STD-1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.

FIGURE 1 – 30 MHz TEST CIRCUIT



RFC: 20 Turns #18 AWG Enameled Wire Close Wound in 2 Layers, 1/4" I.D.

T1: 20 Turns #24 AWG Wire Wound on Micro Metals T37-7 Toroid Core Center Tapped.

T2: 1:9 XFMR; 6 Turns of 2 Twisted Pairs of #28 AWG Enameled Wire (8 Crests per Inch) Bifilar Wound on each of 2 Separate Balun Cores. (Stackpole #57-1503 No. 14 Material) Interconnected as shown.

RF BEADS: Ferroxcube #56-590-65/3B

V_{BB} adjusted for I_{CQ}: 20 mAdc (I_{CQ} = Quiescent Collector Current)

C1 — 80-480 pF, ARCO 466 or Equiv

C2 — 220 pF

FIGURE 2 — OUTPUT POWER versus INPUT POWER

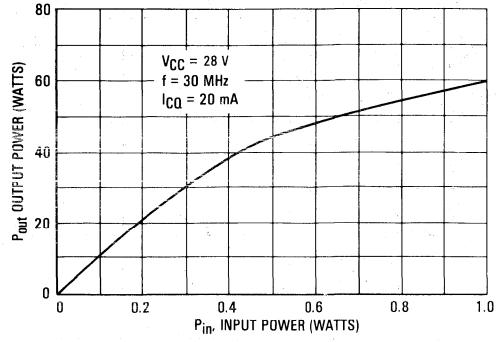


FIGURE 3 — POWER GAIN versus FREQUENCY

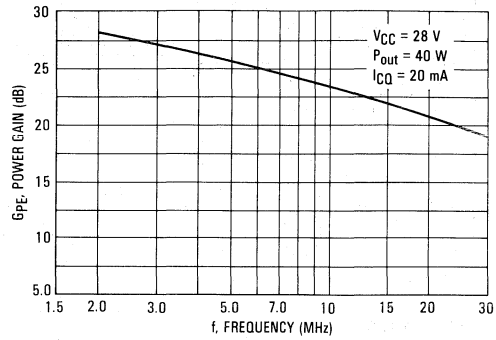


FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE

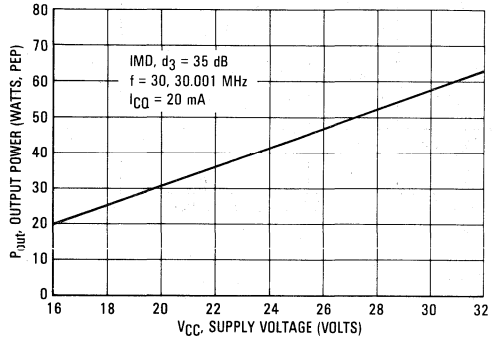


FIGURE 5 — INTERMODULATION DISTORTION versus OUTPUT POWER

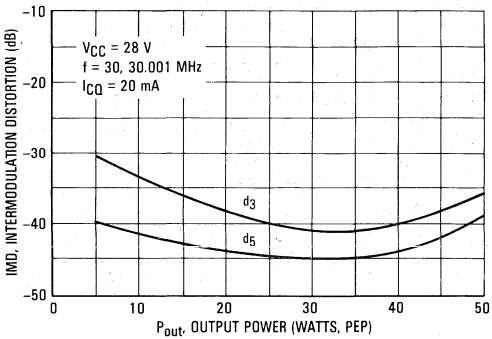


FIGURE 6 — OUTPUT CAPACITANCE versus FREQUENCY

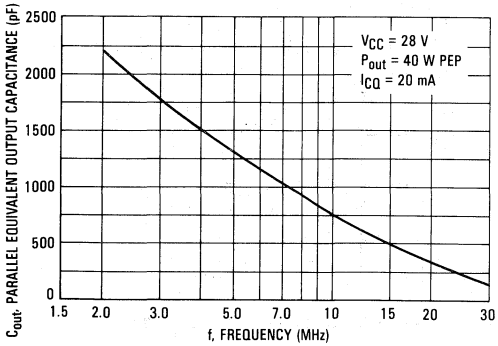


FIGURE 7 — OUTPUT RESISTANCE versus FREQUENCY

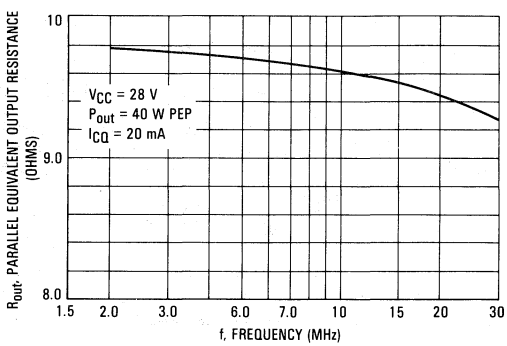


FIGURE 8 — SAFE OPERATING AREA

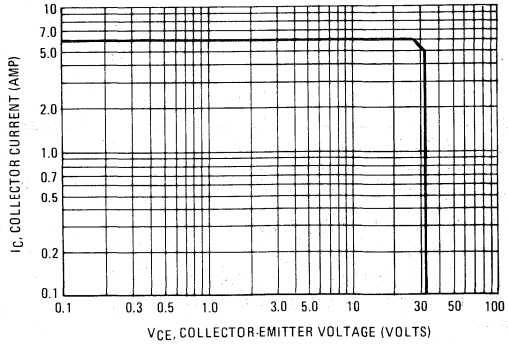
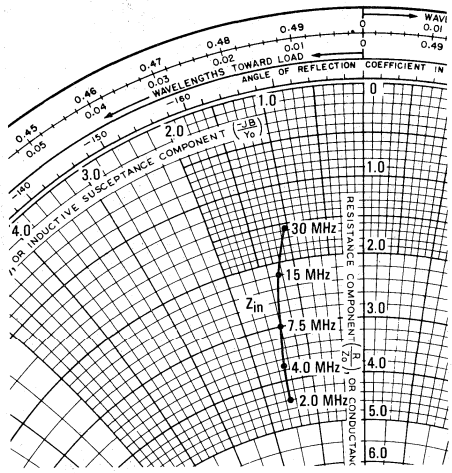


FIGURE 9 — SERIES INPUT IMPEDANCE



V_{CC} = 28 V
I_{CQ} = 20 mA
P_{out} = 40 W (PEP)

f MHz	Z_{in} Ohms
30	1.58 – j1.04
15	2.20 – j1.24
7.5	3.00 – j1.38
4.0	3.70 – j1.45
2.0	4.40 – j1.51

MRF475

The RF Line

12 W (PEP) — 12 W (CW) — 30 MHz

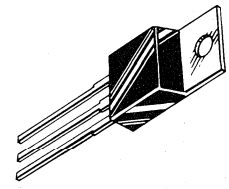
RF POWER TRANSISTOR

NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed primarily for use in single sideband linear amplifier output applications in citizens band and other communications equipment operating to 30 MHz.

- Characterized for Single Sideband and Large-Signal Amplifier Applications Utilizing Low-Level Modulation.
- Specified 13.6 V, 30 MHz Characteristics —
  Output Power = 12 W (PEP)
  Minimum Efficiency = 40% (SSB)
  Output Power = 4.0 W (CW)
  Minimum Efficiency = 50% (CW)
  Minimum Power Gain = 10 dB (PEP & CW)
- Common Collector Characterization

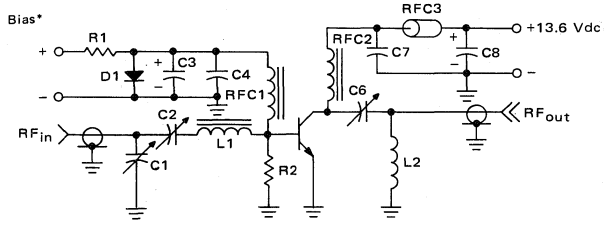


3

MAXIMUM RATINGS

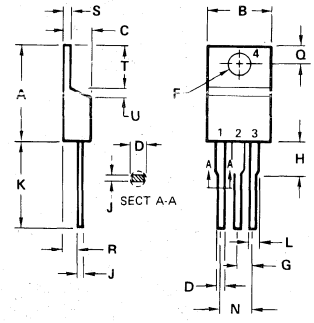
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	48	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	4.0	Adc
Total Device Dissipation @ $T_C = 50^oC$ Derate above 50^oC	P_D	10 0.1	Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	^oC

FIGURE 1 — COMMON-EMITTER TEST CIRCUIT



Adjust for ICQ = 20 mA

C1, 2, 6 — ARCO 466 Trimmer Capacitors
C3 — 1000 μF, 3.0 Vdc Electrolytic
C4, 7 — 0.1 μF Disc Ceramics
C8 — 100 μF, 15 Vdc Electrolytic
R1 — 10 Ω, 5.0 Watt Resistor
R2 — 10 Ω, 1.0 Watt Resistor
L1 — 2.2 μH Molded Choke
L2 — 4 Turns #18 AWG Wire, 1/2" I.D., 5/16" Long
RFC1 — 10 μH Molded Choke
RFC2 — 15 Turns #20 AWG Wire on 5.6 kΩ, 1.0 Watt Carbon Resistor
RFC3 — 5 Ferroxcube, #56-590-65/3B, Beads on #18 AWG Wire
D1 — 1N4997



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTE:
1. DIM. L & H APPLIES TO ALL LEADS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	48	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 25 Vdc, I_E = 0)	I_{CBO}	–	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	30	60	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 13.6 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	125	145	pF
FUNCTIONAL TESTS (SSB)					
Common-Emitter Amplifier Power Gain (V_{CC} = 13.6 Vdc, *P_{out} = 12 W, f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 20 mA)	G_{PE}	10	12	–	dB
Collector Efficiency (V_{CC} = 13.6 Vdc, *P_{out} = 12 W, f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 20 mA)	η	40	–	–	%
Intermodulation Distortion (V_{CC} = 13.6 Vdc, *P_{out} = 12 W, f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 20 mA)	IMD	-30	–	–	%
FUNCTIONAL TESTS (CW)					
Common-Emitter Amplifier Power Gain (V_{CC} = 13.6 Vdc, P_{out} = 4.0 W, f = 30 MHz)	G_{PE}	10	12	–	dB
Collector Efficiency (V_{CC} = 13.6 Vdc, P_{out} = 4.0 W, f = 30 MHz)	η	50	–	–	%
Percentage Up-Modulation (1) (4.0 W Carrier)	–	–	100	–	%
IMPEDANCE CHARACTERISTICS					
Series Equivalent Input	V_{CC} = 13.6 Vdc, P_o = 12 W (PEP), f = 30 MHz, I_{CQ} = 20 mA	Z_{in}	–	4.5–j2.4	–	Ohms
Series Equivalent Output		Z_{out}	–	5.1–j3.2	–	Ohms
Parallel Equivalent Input		Z_{in}	–	5.8/10.9	–	Ω/pF
Parallel Equivalent Output		Z_{out}	–	7.1/11.3	–	Ω/pF

*PEP

(1) Percentage Up-Modulation is measured in the test circuit (Figure 1) by setting the Carrier Power (P_c) to 4.0 Watts with V_{CC} = 13.6 Vdc and noting the power input. Then the Peak Envelope Power (PEP) is noted after doubling the original power input to simulate driver modulation.

$$\text{Percentage Up-Modulation} = \left[\left(\frac{PEP}{P_c}\right) - 1\right] \bullet 100$$

FIGURE 2 – OUTPUT POWER versus INPUT POWER

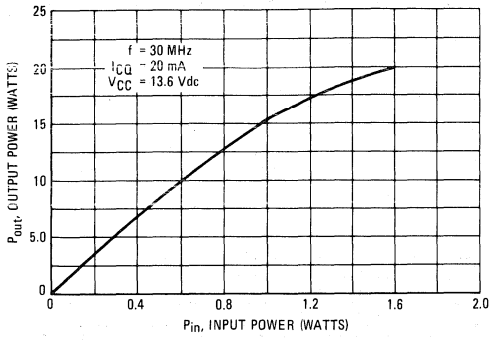


FIGURE 3 – INTERMODULATION DISTORTION versus OUTPUT POWER

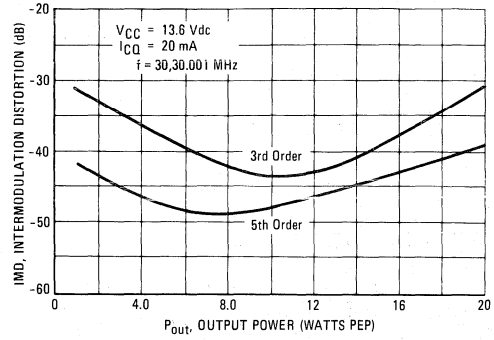


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

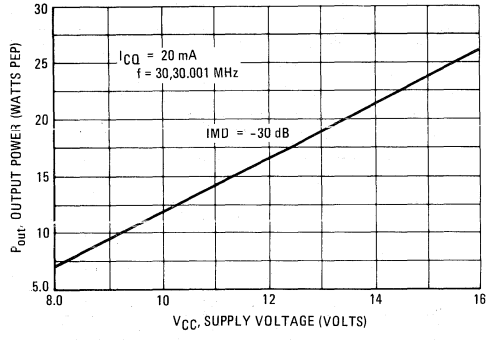


FIGURE 5 – OUTPUT CAPACITANCE versus FREQUENCY

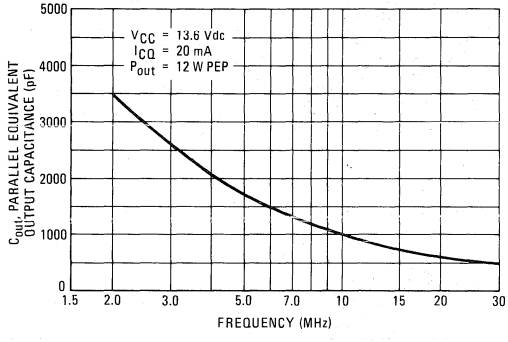


FIGURE 6 – OUTPUT RESISTANCE versus FREQUENCY

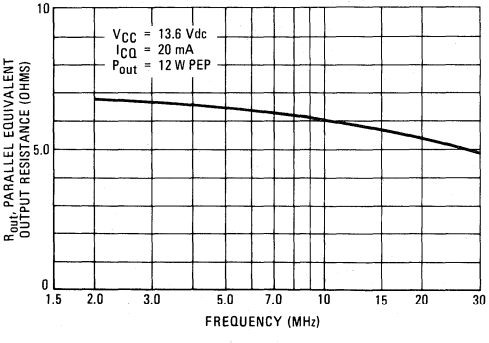


FIGURE 7 – POWER GAIN versus FREQUENCY

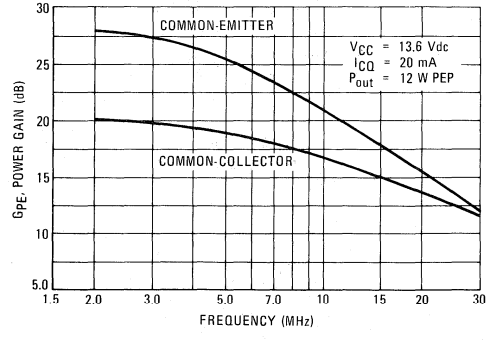
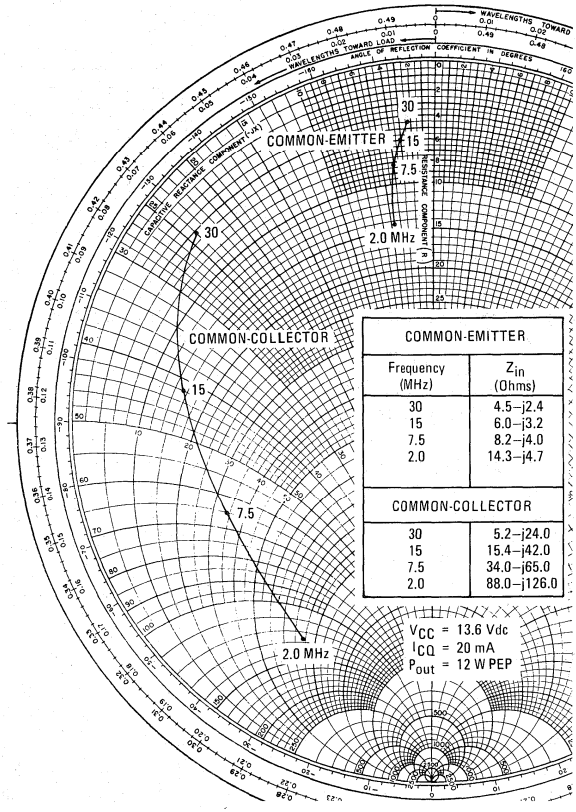
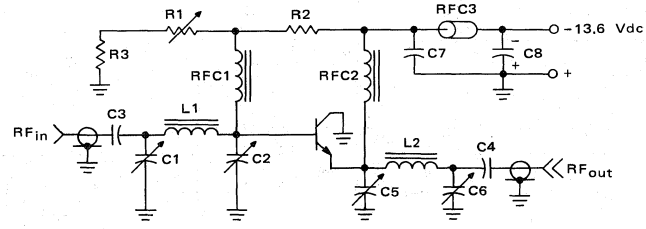


FIGURE 8 – IMPEDANCE COORDINATES – 50-OHM CHARACTERISTICS IMPEDANCE



COMMON-EMITTER	
Frequency (MHz)	Z_{in} (Ohms)
30	4.5–j2.4
15	6.0–j3.2
7.5	8.2–j4.0
2.0	14.3–j4.7
COMMON-COLLECTOR	
30	5.2–j24.0
15	15.4–j42.0
7.5	34.0–j65.0
2.0	88.0–j126.0

FIGURE 9 – COMMON-COLLECTOR TEST CIRCUIT



C1, 5 – ARCO 466 Trimmer Capacitors
C2 – ARCO 463 Trimmer Capacitor
C3, 4, 7 – 0.1 μF Ceramic Disc
C6 – ARCO 469 Trimmer Capacitor
C8 – 100 μF 15 Vdc Electrolytic
R1 – 250 Ω, 2.0 W Potentiometer
R2 – 5.1 Ω, 1/2 W Resistor
R3 – 51 Ω, 2.0 W Resistor

L1 – 0.33 μH Molded Choke
L2 – 4 Turns #18 AWG Wire, 1/8" I.D., 5/16" Long
RFC1 – 18 μH Molded Choke
RFC2 – 15 Turns #20 AWG Wire on 100 Ω, 1.0 W Carbon Resistor
RFC3 – Ferroxcube, #56-590-65/3B, Beads on #18 AWG Wire

MRF476

The RF Line

NPN SILICON RF POWER TRANSISTOR

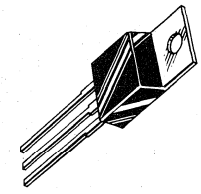
. . . designed primarily for use in single sideband linear amplifier output applications in citizens band and other communications equipment operating to 50 MHz.

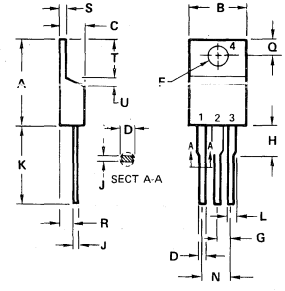
- Characterized for Single Sideband and Large-Signal Amplifier Applications Utilizing Low-Level Modulation
- Specified 12.5 V, 30 MHz Characteristics –
  - Output Power = 3.0 W (PEP)
  - Minimum Efficiency = 40% (SSB)
  - Output Power = 3.0 W (CW)
  - Minimum Power Gain = 15 dB (PEP)
- Common-Emitter Characterization

3.0 W (PEP)–3.0 W (CW) – 30 MHz

RF POWER TRANSISTOR

NPN SILICON





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTE:
1. DIM. L & H APPLIES TO ALL LEADS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	1.0	Adc
Total Device Dissipation @ $T_A = 25^oC$ (1) Derate above 25^oC	P_D	10 57.2	Watts $mW/^oC$
Storage Temperature Range	T_{stg}	-65 to + 150	^oC

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

THERMAL CHARACTERISTICS

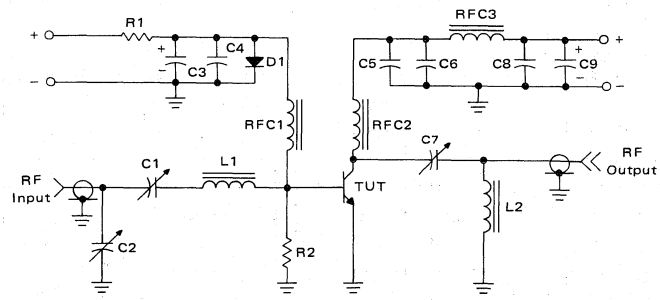
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	17.5	$^oC/W$

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 25 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	0.5	mAdc
ON CHARACTERISITCS					
DC Current Gain (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	50	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	25	35	pF
FUNCTIONAL TESTS (SSB)					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 3.0 W (PEP) f1 = 30 MHz, f2 = 30.001 MHz, ICQ = 20 mA)	G_{PE}	15	18	–	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 3.0 W (PEP) f1 = 30 MHz, f2 = 30.001 MHz, ICQ = 20 mA)	η	40	–	–	%
Intermodulation Distortion (V_{CC} = 12.5 Vdc, P_{out} = 3.0 W (PEP) f1 = 30 MHz, f2 = 30.001 MHz, ICQ = 20 mA	IMD	-30	-35	–	dB
50 MHz PERFORMANCE					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 3.0 W, f = 50 MHz)	G_{PE}	–	15	–	dB

3

FIGURE 1 – 30 MHz TEST CIRCUIT SCHEMATIC



C2 – Arco 466 Trimmer
C1, C7 – Arco 469 Trimmer
C3 – 500 μF, 3.0 V Electrolytic
C4, C5, C8 – 0.1 μF Erie Redcap
C6 – 1000 pF UNELCO
C9 – 100 μF, 15 V Electrolytic

R1 – 33 Ω 5 W Wire Wound
R2 – 50 Ω 1/2 W Carbon

L1 – 0.22 μH Molded Choke
L2 – 5 Turns #18 Enameled Wire, 1/4" ID

RFC1 – 10 μH Molded Choke
RFC2 – 1.9 μH Molded Choke (Ohmite Z-144)
RFC3 – 6 Ferroxcube Beads on #18 AWG Wire

D1 – MR751

Board – G10, 2-sided 2 oz. Copper Clad

Connectors – Type N

FIGURE 2 – POWER GAIN versus FREQUENCY

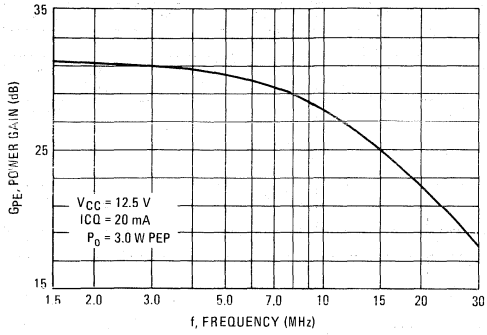


FIGURE 3 – OUTPUT POWER versus INPUT POWER

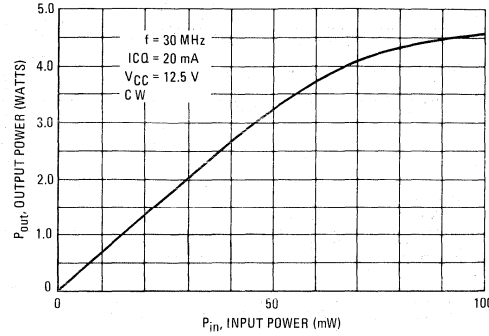


FIGURE 4 – OUTPUT POWER versus INPUT POWER

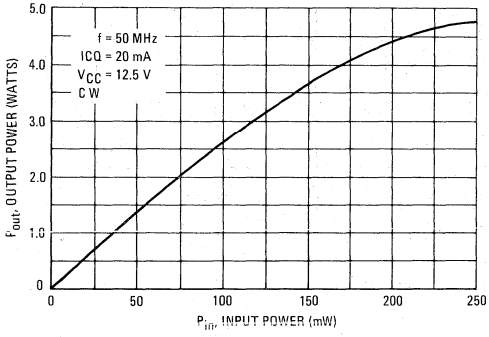


FIGURE 5 – OUTPUT POWER versus SUPPLY VOLTAGE

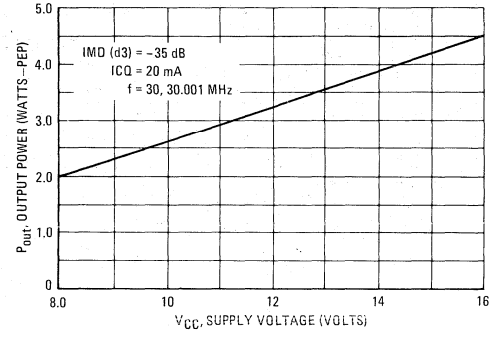


FIGURE 6 – INTERMODULATION DISTORTION versus OUTPUT POWER

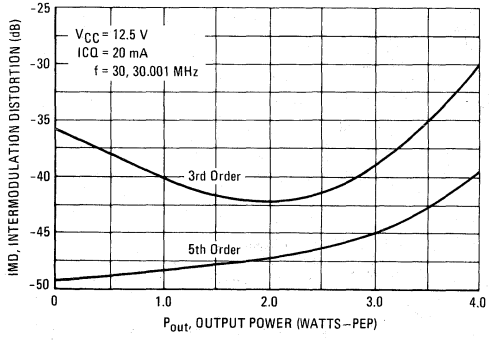
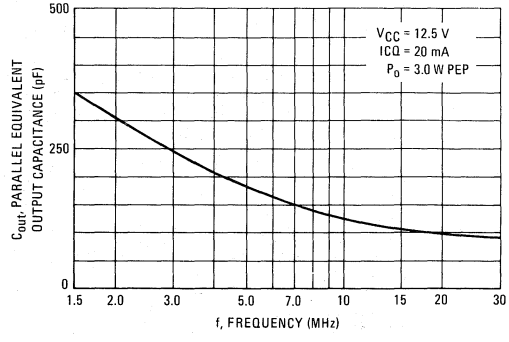


FIGURE 7 – OUTPUT CAPACITANCE versus FREQUENCY



3

FIGURE 8 – OUTPUT RESISTANCE versus FREQUENCY

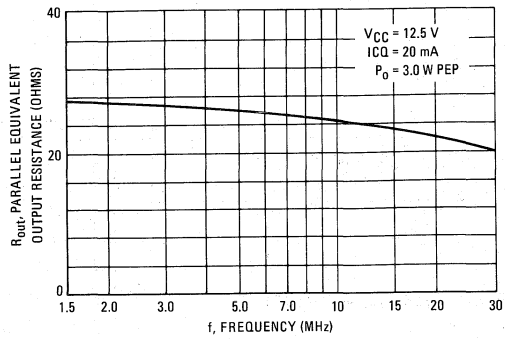
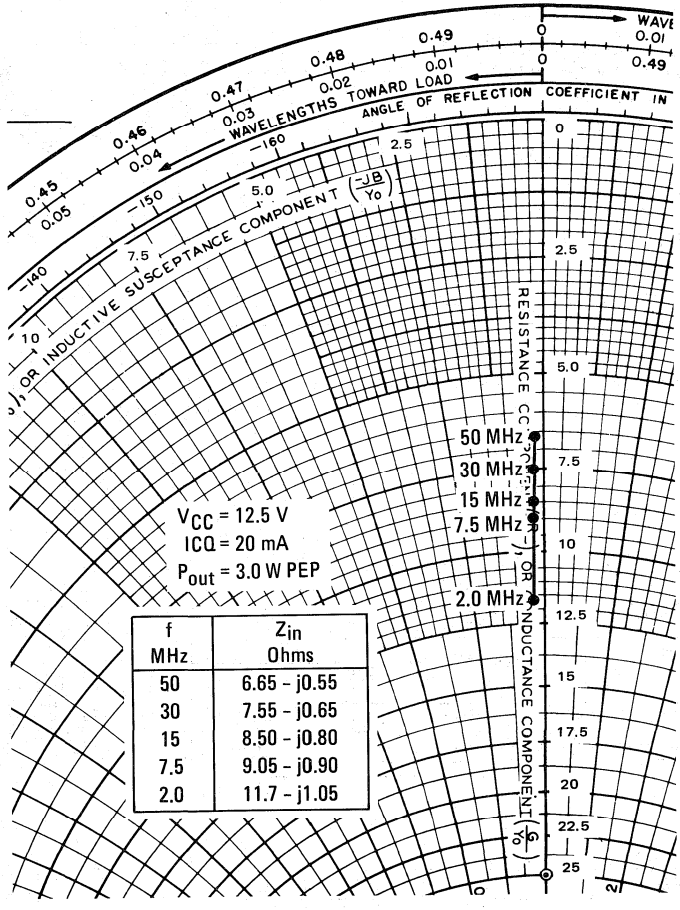


FIGURE 9 – SERIES EQUIVALENT INPUT IMPEDANCE



f MHz	Z_{in} Ohms
50	6.65 - j0.55
30	7.55 - j0.65
15	8.50 - j0.80
7.5	9.05 - j0.90
2.0	11.7 - j1.05

MRF477

The RF Line

40 W (PEP) – 30 MHz

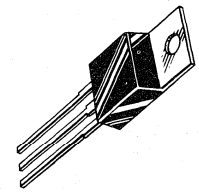
RF POWER TRANSISTOR

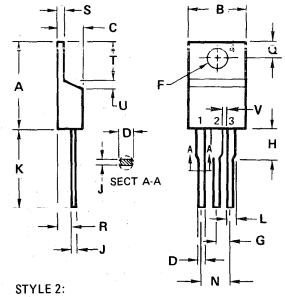
NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed primarily for application as a high-power linear amplifier from 1.5 to 30 MHz, in single sideband mobile, marine and base station equipment.

- Low-Cost, Common-Emitter TO-220 Package
- Specified 12.5 Volt, 30 MHz Performance –
  Output Power = 40 W CW or PEP
  Power Gain = 15 dB Min
  Efficiency = 40% Min (PEP)
- Intermodulation Distortion @ 40 W (PEP) –
  IMD = –30 dB (Max)
- 30:1 VSWR Load Mismatch Capability at Rated Output Power and Supply Voltage





STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current – Continuous	I_C	5.0	Adc
Withstand Current (t = 5.0 s)	–	8.0	Adc
Total Device Dissipation @ $T_C = 25^oC$ (1) Derate above 25^oC	P_D	87.5 0.5	Watts $W/^oC$
Storage Temperature Range	T_{stg}	–65 to +150	^oC

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	$^oC/W$

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

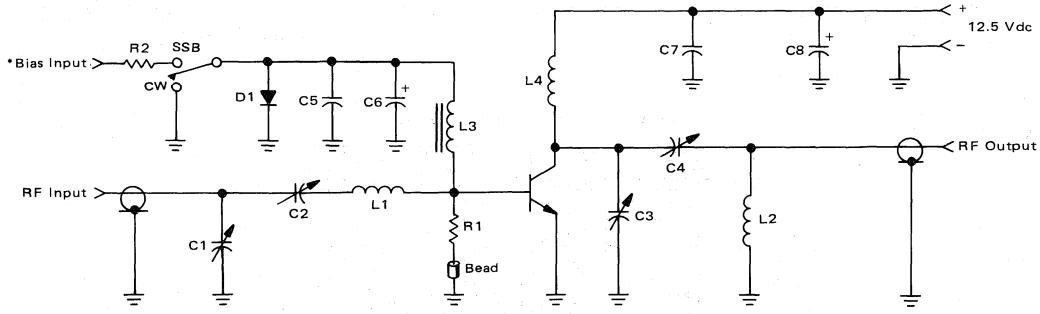
CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 mAdc, I_E = 0)	$V_{(BR)CBO}$	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 12.5 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	–	–	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	70	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	175	250	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 40 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 40 mAdc)	G_{PE}	15	17	–	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 40 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 40 mAdc)	η	40	45	–	%
Intermodulation Distortion (1) (V_{CC} = 12.5 Vdc, P_{out} = 40 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 40 mAdc)	IMD (d_3)	–	-35	-30	dB

(1) To MIL-STD-1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.

FIGURE 1 – 30 MHz TEST CIRCUIT



C1, C2, C4 – Arco 469, 190-780 pF
C3 – Arco 429, 90-400 pF
C5, C7 – 0.001 μF Disk Ceramics
C6 – 500 μF 3.0 Vdc Electrolytic
C8 – 100 μF 16 Vdc Electrolytic

R1 – 10 Ω 1.0 Watt Resistor
R2 – 5 Ω 5.0 Watt Resistor

L1 – 4 Turns #16 AWG 1/3" ID, 1/3" Long
L2 – 3 Turns #16 AWG 1/3" ID, 1/2" Long
L3 – 10 μH Molded Choke
L4 – 12 Turns #18 AWG 1/4" ID

Bead – Ferroxcube #56-590-65/3B

D1 – 1N4719

*Adjust Bias (Base) Voltage for I_{CQ} = 40 mA with no RF applied.

FIGURE 2 – OUTPUT POWER versus INPUT POWER

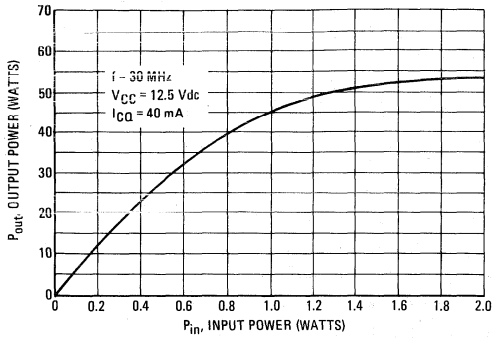


FIGURE 3 – OUTPUT POWER versus SUPPLY VOLTAGE

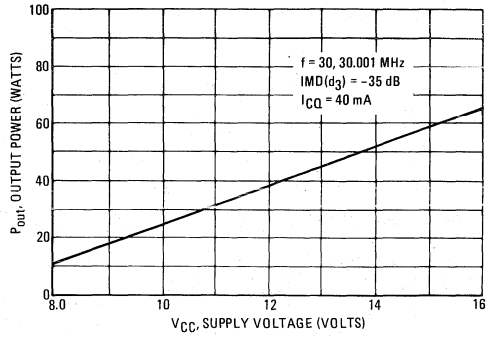


FIGURE 4 – POWER GAIN versus FREQUENCY

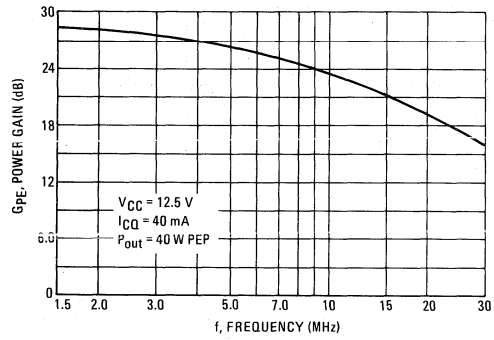


FIGURE 5 – INTERMODULATION DISTORTION versus OUTPUT POWER

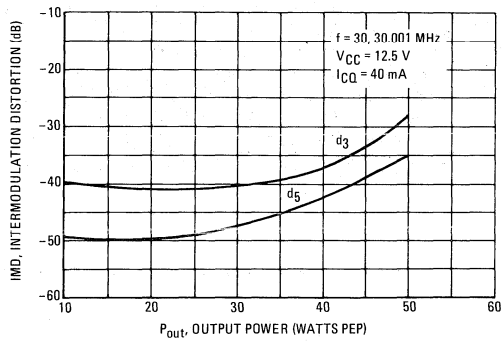


FIGURE 6 – SAFE OPERATING AREA

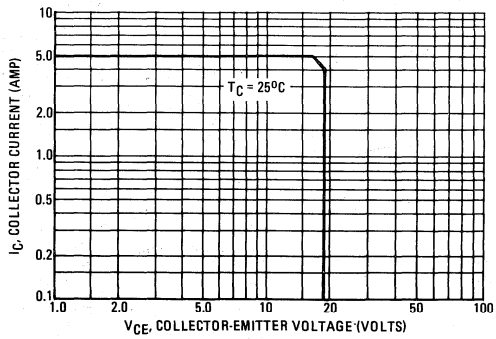


FIGURE 7 – SERIES EQUIVALENT INPUT IMPEDANCE

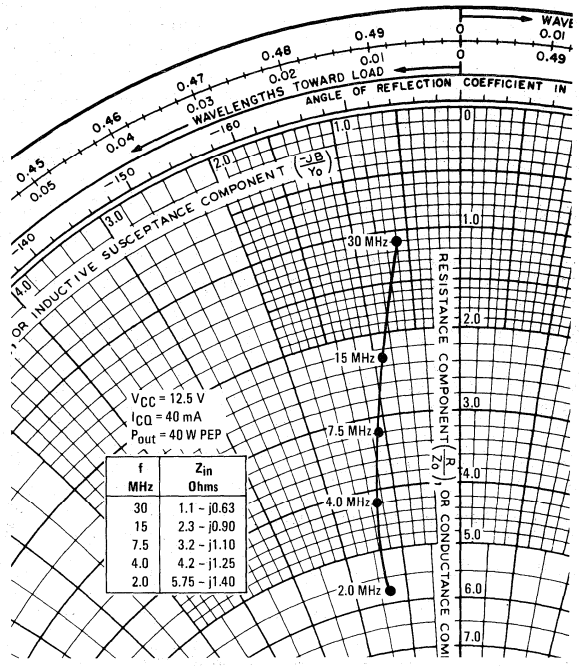


FIGURE 8 – OUTPUT CAPACITANCE versus FREQUENCY

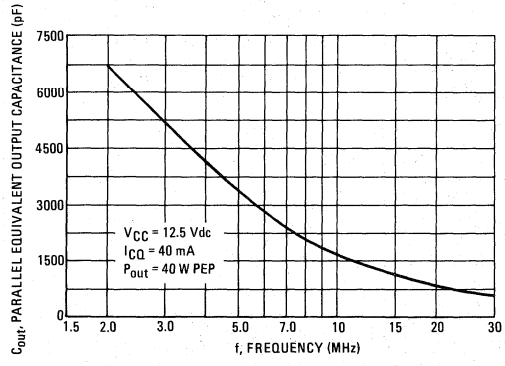
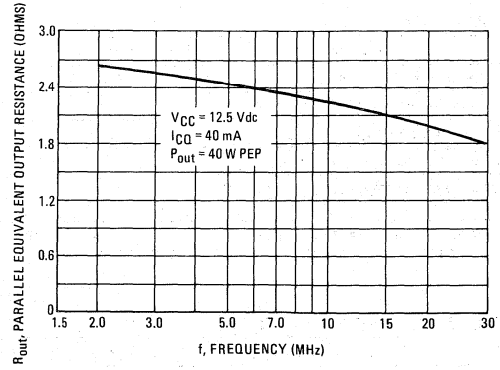


FIGURE 9 – OUTPUT RESISTANCE versus FREQUENCY



3

MRF479

The RF Line

15 W (PEP), 15 W (CW)—30 MHz

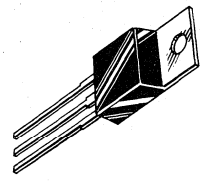
RF POWER TRANSISTOR

NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed primarily for use in single sideband linear amplifier output applications and other communications equipment operating to 50 MHz.

- Low-Cost, Common-Emitter TO-220 Package
- Specified 12.5 V, 30 MHz Performance —
  Output Power = 15 W (PEP) or (CW)
  Power Gain = 12 dB Min
  Efficiency = 40% Min
- Intermodulation Distortion @ 15 W (PEP) —
  IMD = -30 dB (Max)
- 30:1 VSWR Load Mismatch Capability at Rated Output Power and Supply Voltage
- Characterized from 2.0 to 50 MHz



MAXIMUM RATINGS

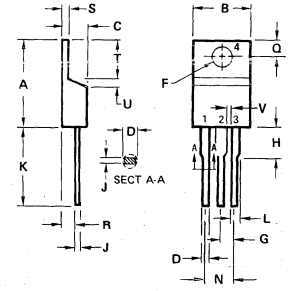
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Continuous	I_C	2.0	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	30 0.17	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	5.85	°C/W

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.



STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

NOTE:
1. DIM. L & H APPLIES TO ALL LEADS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

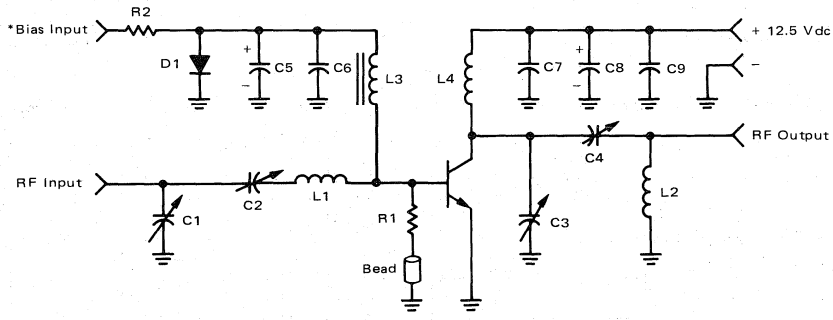
CASE 221A-02

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CBO}$	36	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CES}	—	—	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	30	60	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	125	155	pF
FUNCTIONAL TESTS (SSB)					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 15 W (PEP), f_1 = 30 MHz, f_2 = 30.001 MHz, I_{CQ} = 20 mA)	G_{PE}	12	14	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 15 W (PEP), f_1 = 30 MHz, f_2 = 30.001 MHz, I_{CQ} = 20 mA)	η	40	—	—	%
Intermodulation Distortion (1) (PEP) (V_{CC} = 12.5 Vdc, P_{out} = 15 W (PEP), f_1 = 30 MHz, f_2 = 30.001 MHz, I_{CQ} = 20 mA)	d_3	—	—	-30	dB

(1) To MIL-STD-1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.

FIGURE 1 — 30-MHz COMMON EMITTER TEST CIRCUIT



C1, C2, C4 — 469 Arco 170–780 pF
C3 — 426 Arco 37–250 pF
C5 — 500 μF, 3.0 V
C6, C7 — 0.1 μF Erie Redcap
C8 — 0.01 μF Erie Redcap
C9 — 100 μF, 16 V

L1 — 4 Turns #18 AWG 0.3" ID X 0.25"
L2 — 5 Turns #16 AWG 0.35" ID X 0.9"

L3 — 10 μH Molded Choke
L4 — 12 Turns #18 AWG 0.25" ID X 0.75"

R1 — 10 Ω, 1.0 W
R2 — 5.0 Ω, 5.0 W

Bead — Ferroxcube Bead #56-590-65/3B

D1 — 1N4997

*Adjust Bias (Base) Voltage for I_{CQ} = 20 mA with no RF applied.

FIGURE 2 – OUTPUT POWER versus INPUT POWER

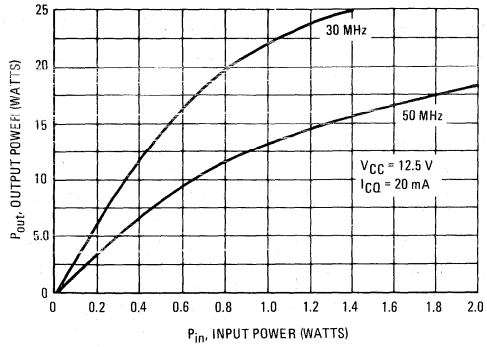


FIGURE 3 – POWER GAIN versus FREQUENCY

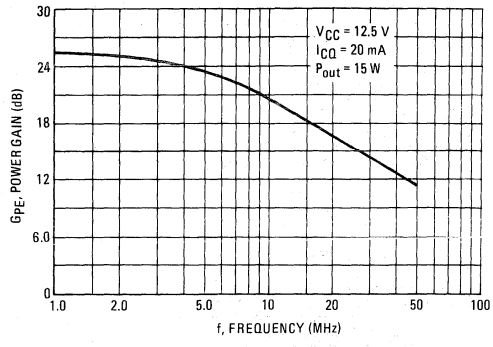


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

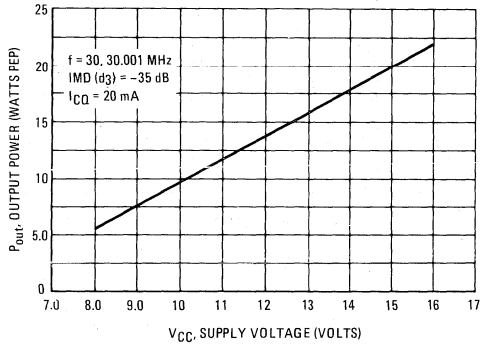


FIGURE 5 – INTERMODULATION DISTORTION versus OUTPUT POWER

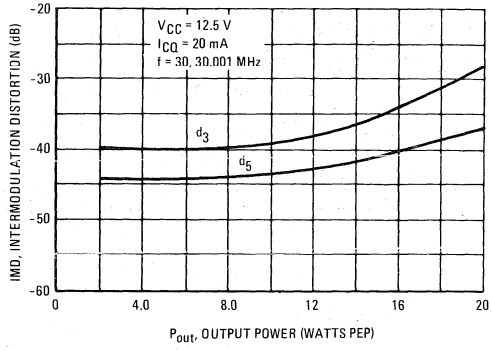


FIGURE 6 – OUTPUT CAPACITANCE versus FREQUENCY

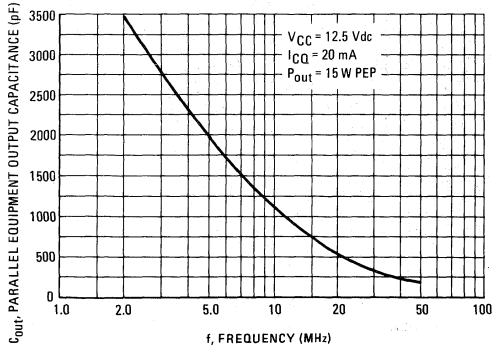


FIGURE 7 – OUTPUT RESISTANCE versus FREQUENCY

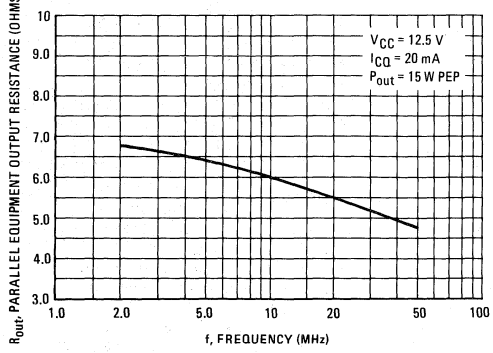
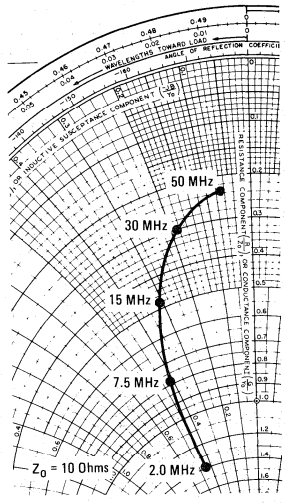


FIGURE 8 – SERIES EQUIVALENT INPUT IMPEDANCE



V_{CC} = 12.5 Vdc
I_{CQ} = 20 mA
P_{out} = 15 W PEP

f MHz	Z_{in} Ohms
50	2.35 – j0.7
30	3.0 – j1.9
15	4.8 – j3.1
7.5	7.9 – j4.1
2.0	14 – j4.7

FIGURE 9 – 30 MHz TEST AMPLIFIER

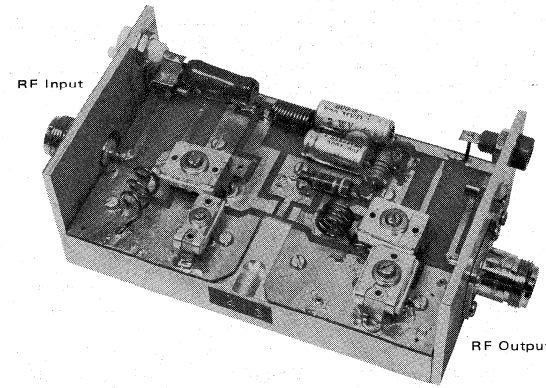
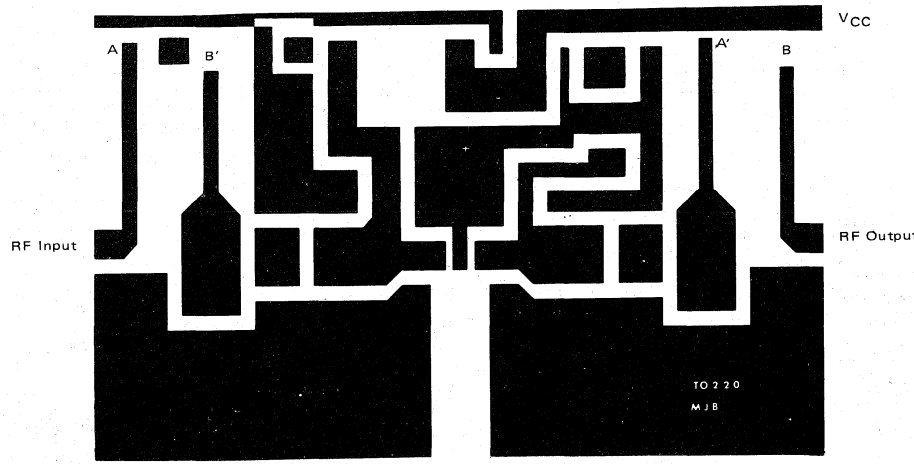


FIGURE 10 – TEST AMPLIFIER PCB PHOTOMASTER



NOTE: Points A, A′ and B, B′ are connected via 50 Ω coaxial cable under the PCB.
The Printed Circuit Board shown is 75% of the original.

MRF485

The RF Line

15 W (PEP) — 15 W (CW) — 30 MHz

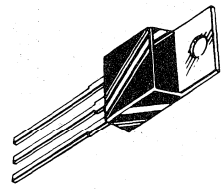
RF POWER
TRANSISTOR

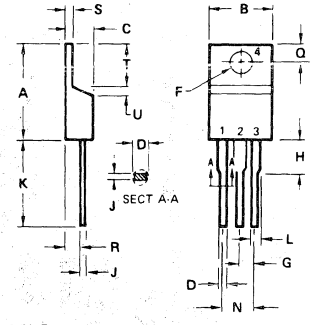
NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed primarily for use in single sideband linear amplifier output applications and other communications equipment operating to 30 MHz.

- Characterized for Single Sideband and Large-Signal Amplifier Applications Utilizing Low-Level Modulation
- Specified 28 V, 30 MHz Characteristics —
  Output Power = 15 W (PEP)
  Minimum Efficiency = 40% (SSB)
  Minimum Power Gain = 10 dB (PEP & CW)





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTE:
1. DIM. L & H APPLIES TO ALL LEADS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	35	Vdc
Collector-Base Voltage	V_{CBO}	65	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	1.0	Adc
Total Device Dissipation @ $T_C = 50^oC$ (1) Derate above 50^oC	P_D	30 0.3	Watts $W/^oC$
Storage Temperature Range	T_{stg}	−65 to +150	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.33	$^oC/W$

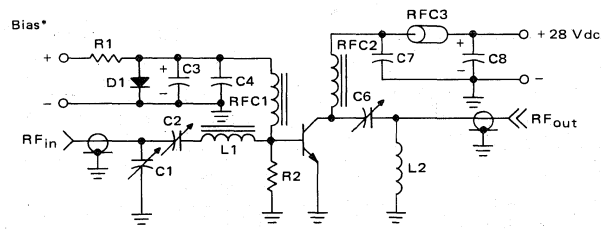
(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	35	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 25 Vdc, I_E = 0)	I_{CBO}	–	–	1.0	mAdc
Collector-Cutoff Current (V_{CE} = 28 Vdc, V_{BE} = 0)	I_{CES}	–	–	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	30	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	85	100	pF
FUNCTIONAL TESTS (SSB)					
Common-Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 15 W (PEP, f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 20 mA)	G_{PE}	10	13	–	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 15 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 20 mA)	η	40	–	–	%
Intermodulation Distortion (1) (V_{CC} = 28 Vdc, P_{out} = 15 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 20 mA)	$IMD_{(d3)}$	–	–35	–30	dB
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 15 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, VSWR = 30:1 All Angles)	ψ	No Degradation in Output Power			

(1) To MIL-STD-1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.

FIGURE 1 – COMMON-EMITTER TEST CIRCUIT



*Adjust for I_{CQ} = 20 mA

C1, 2, 6 – ARCO 466 Trimmer Capacitors.
C3 – 1000 μF, 3.0 Vdc Electrolytic
C4, 7 – 0.1 μF, Disc Ceramics
C8 – 100 μF, 15 Vdc Electrolytic

R1 – 10 Ω, 5.0 Watt Resistor
R2 – 10 Ω, 1.0 Watt Resistor

L1 – 2.2 μH Molded Choke
L2 – 7 Turns #18 AWG Wire, 3/8" I.D.

RFC1 – 10 μH Molded Choke
RFC2 – 0.84 μH Molded Choke
RFC3 – 2 Ferroxcube, #56-590-65/3B, Beads on #18 AWG Wire

D1 – 1N4997

FIGURE 2 – OUTPUT POWER versus INPUT POWER

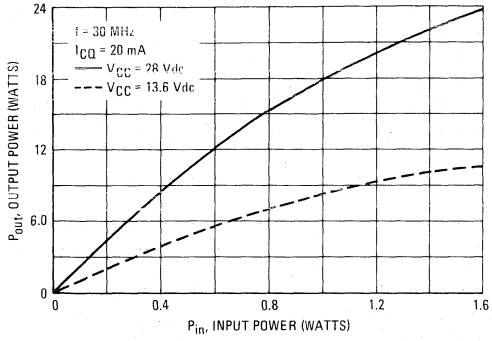


FIGURE 3 – INTERMODULATION DISTORTION versus OUTPUT POWER

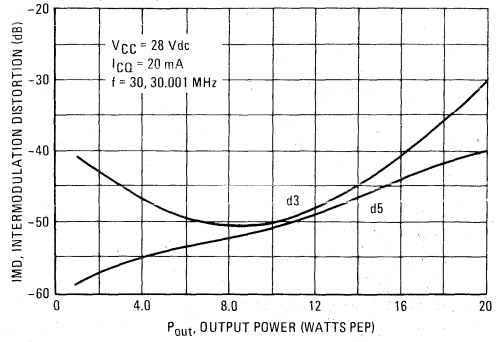


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

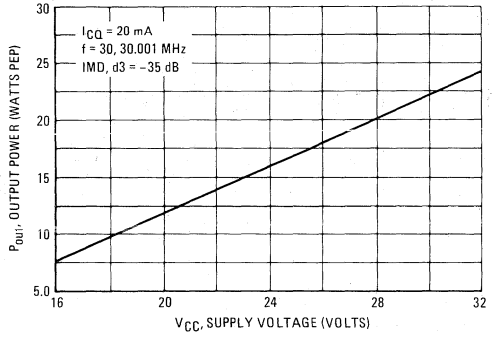


FIGURE 5 – OUTPUT CAPACITANCE versus FREQUENCY

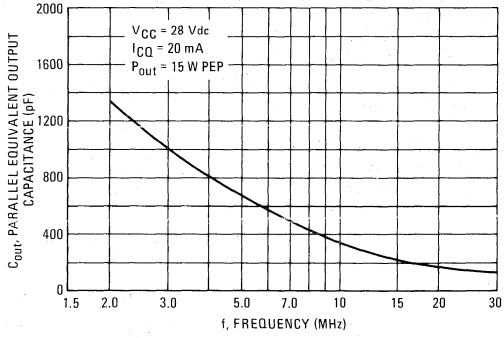


FIGURE 6 – OUTPUT RESISTANCE versus FREQUENCY

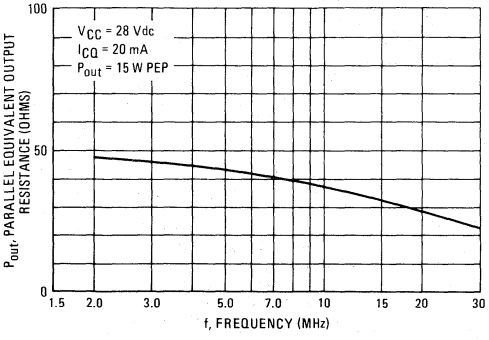


FIGURE 7 – POWER GAIN versus FREQUENCY

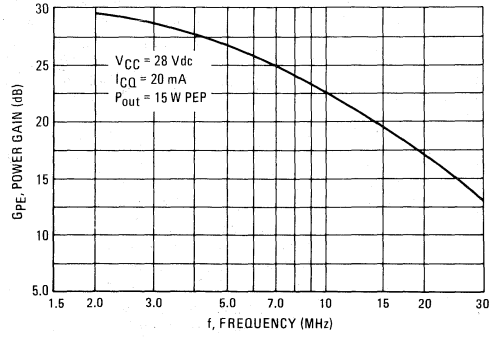
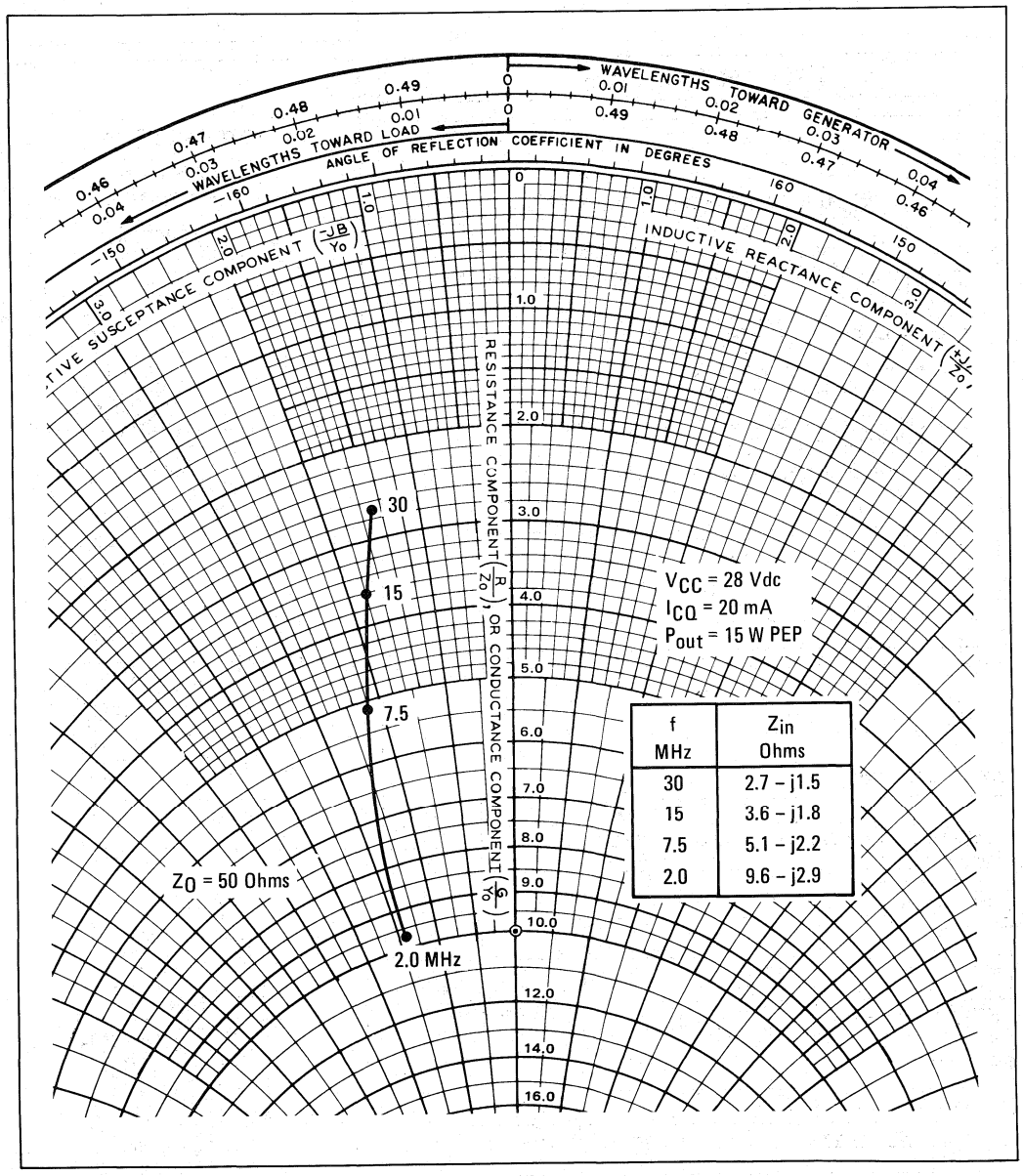


FIGURE 8 – SERIES EQUIVALENT INPUT IMPEDANCE



MRF486

The RF Line

40 W (PEP) – 30 MHz

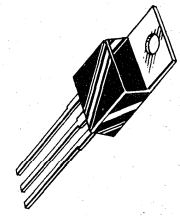
RF POWER TRANSISTOR

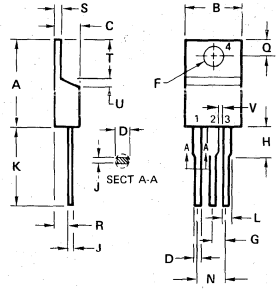
NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed primarily for application as a high-power linear amplifier from 1.5 to 30 MHz, in single sideband mobile, marine and base station equipment.

- Low-Cost, Common-Emitter TO-220 Package
- Specified 28 Volt, 30 MHz Performance –
  Output Power = 40 W (PEP)
  Power Gain = 15 dB Min
  Efficiency = 40% Min
- Intermodulation Distortion @ 40 W (PEP) –
  IMD = –30 dB (Max)
- 30:1 VSWR Load Mismatch Capability at Rated Output Power and Supply Voltage





STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	35	Vdc
Collector-Base Voltage	V_{CBO}	65	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current – Continuous	I_C	3.0	Adc
Withstand Current (t = 5.0 s)	–	6.0	Adc
Total Device Dissipation @ $T_C = 25^oC$ (1) Derate above 25^oC	P_D	87.5 0.5	Watts $W/^oC$
Storage Temperature Range	T_{stg}	–65 to +150	^oC

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	$^oC/W$

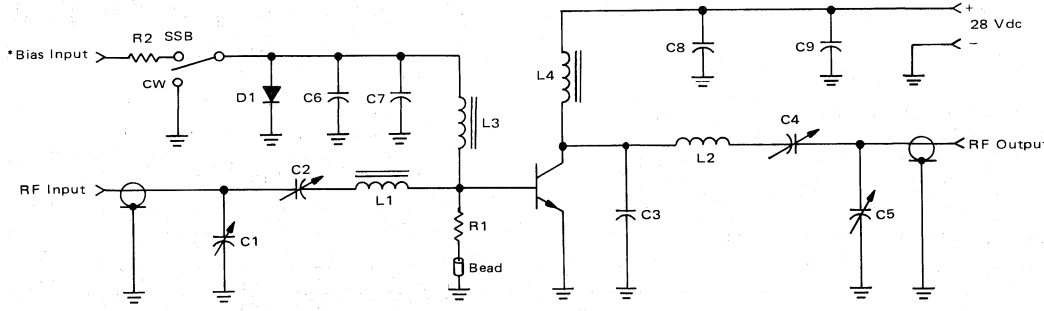
(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	35	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	65	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 50 mAdc, I_E = 0)	$V_{(BR)CBO}$	65	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 28 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	–	–	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	40	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 27 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	130	200	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 40 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 40 mAdc)	G_{PE}	15	17.5	–	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 40 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 40 mAdc)	η	40	45	–	%
Intermodulation Distortion (1) (V_{CC} = 28 Vdc, P_{out} = 40 W (PEP), f1 = 30 MHz, f2 = 30.001 MHz, I_{CQ} = 40 mAdc)	$IMD(d_3)$	–	–35	–30	dB

(1) To MIL-STD-1311 Version A, Test Method 2204B, Two Tone, Reference Each Tone.

FIGURE 1 – 30 MHz TEST CIRCUIT



C1, C2 – Arco 469, 190–780 pF
C3 – 150 pF ELMENCO**
C4, C5 – Arco 429, 90–400 pF
C6, C9 – 0.001 μF Disc Ceramics
C7 – 500 μF, 3 Vdc Electrolytic
C8 – 50 μF, 50 Vdc Electrolytic

R1 – 10 Ω, 1.0 Watt Resistor
R2 – 5 Ω, 5.0 Watt Resistor

L1 – 0.15 μH Molded Choke
L2 – 7 Turns, #16 AWG Enameled Close-Wound, 1/2" ID
L3 – 10 μH Molded Choke
L4 – 1.9 μH Molded Choke

One Bead – #56-590-65/3B (Ferroxcube or equiv.)

D1 – 1N4997

*Adjust Bias (Base) Voltage for I_{CQ} = 40 mA with no RF applied.
**Type MCM01/010 or UNELCO 3 HS 0006.

FIGURE 2 – OUTPUT POWER versus INPUT POWER

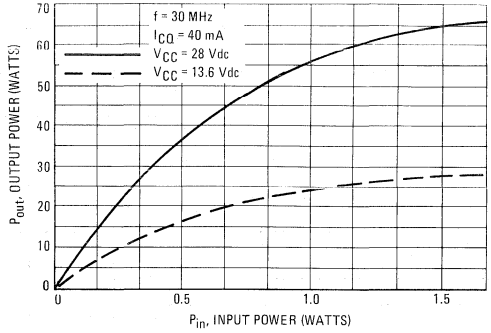


FIGURE 3 – OUTPUT POWER versus SUPPLY VOLTAGE

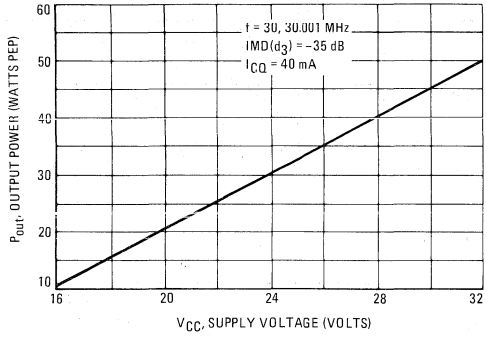


FIGURE 4 – POWER GAIN versus FREQUENCY

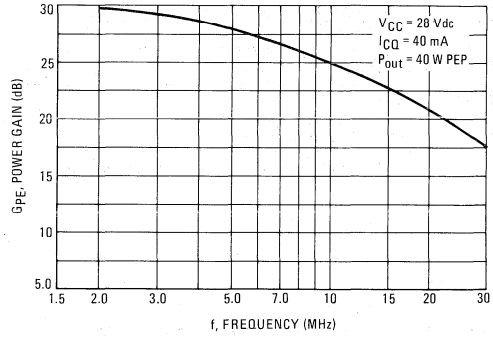


FIGURE 5 – INTERMODULATION DISTORTION versus OUTPUT POWER

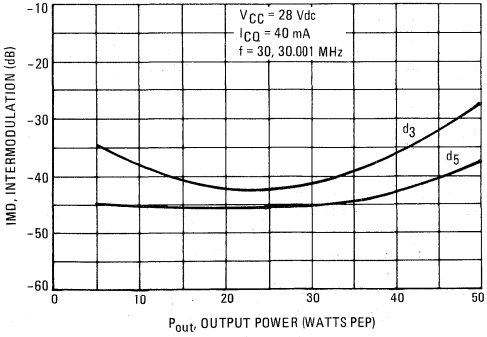


FIGURE 6 – SAFE OPERATING AREA

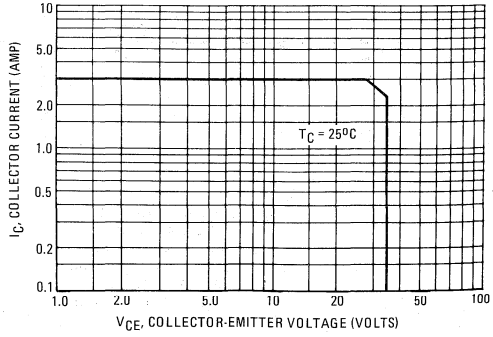
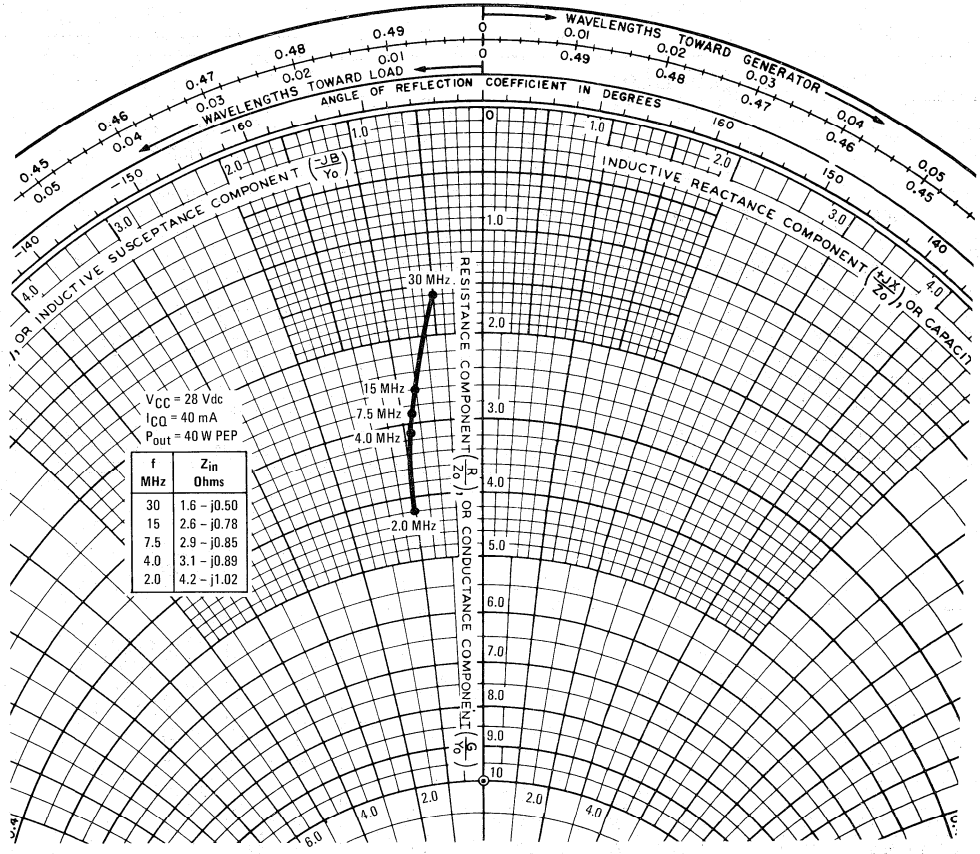


FIGURE 7 – SERIES EQUIVALENT INPUT IMPEDANCE



f MHz	Zin Ohms
30	1.6 – j0.50
15	2.6 – j0.78
7.5	2.9 – j0.85
4.0	3.1 – j0.89
2.0	4.2 – j1.02

FIGURE 8 – OUTPUT CAPACITANCE versus FREQUENCY

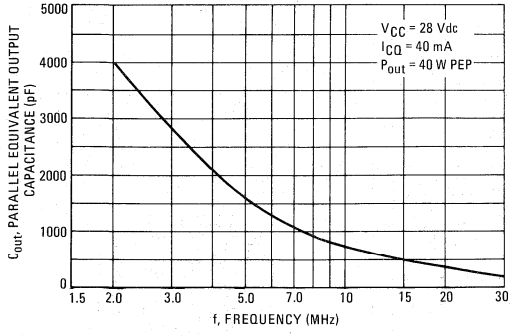
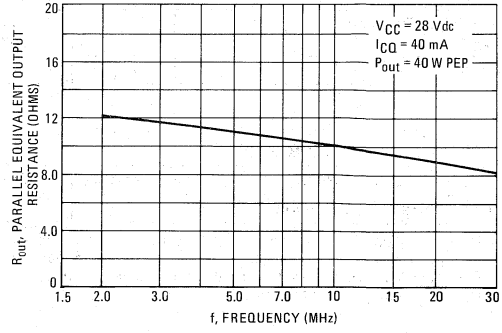


FIGURE 9 – OUTPUT RESISTANCE versus FREQUENCY



MRF492
MRF492A

The RF Line

70 W 50 MHz

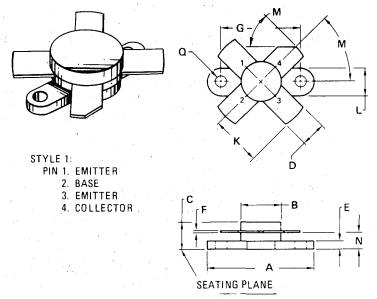
RF POWER TRANSISTOR

NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed for 12.5 volt low band VHF large-signal power amplifier applications in commercial and industrial FM equipment.

- Specified 12.5 V, 50 MHz Characteristics —
  Output Power = 70 W
  Minimum Gain = 11 dB
  Efficiency = 50%
- Load Mismatch Capability at High Line and RF Overdrive



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	24.64	24.89	0.970	0.980
B	11.81	12.95	0.465	0.510
C	5.82	6.98	0.229	0.275
D	5.46	5.97	0.216	0.235
E	2.13	2.79	0.084	0.110
F	0.08	0.18	0.003	0.007
G	18.29	18.54	0.720	0.730
K	11.05	–	0.435	–
L	6.22	6.48	0.245	0.255
M	45° NOM		45° NOM	
N	3.66	4.52	0.144	0.178
Q	2.92	3.30	0.115	0.130

MRF492 **CASE 211-11**

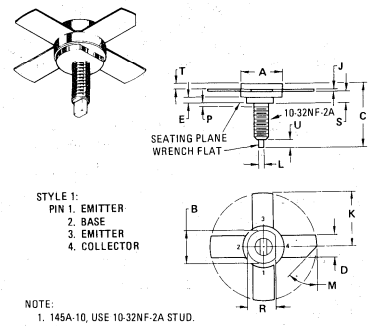
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Continuous	I_C	20	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	250 1.43	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	0.7	°C/W

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.
(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	12.45	12.95	0.490	0.510
B	10.54	10.80	0.415	0.425
C	19.68	22.73	0.775	0.895
D	5.46	5.97	0.215	0.235
E	1.83	–	0.072	–
J	0.08	0.18	0.003	0.007
K	12.45	–	0.490	–
L	1.65	1.90	0.065	0.075
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
R	9.73	10.06	0.383	0.396
S	3.84	4.50	0.151	0.177
T	2.11	2.54	0.083	0.100
U	2.49	3.35	0.098	0.132

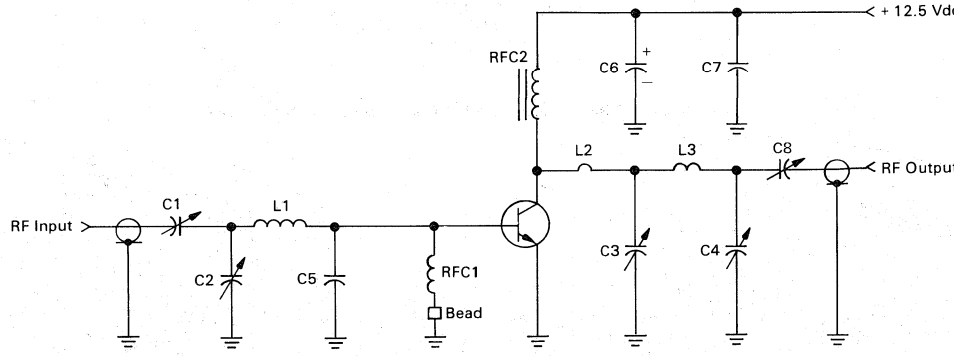
MRF492A **CASE 145A-10**

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter-Base Breakdown Voltage I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 13.6 Vdc, V_{BE} = 0)	I_{CES}	—	—	20	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	—	150	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	275	450	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 70 W, f = 50 MHz)	G_{PE}	11	13	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 70 W, f = 50 MHz)	η	50	—	—	%

3

FIGURE 1 — 50 MHz TEST CIRCUIT



C1, C8 — 9.0-180 pF, Arco 463
C2, C3, C4 — 80-480 pF, Arco 466
C5 — 1000 pF, 350 V, Unelco
C6 — 10 μF, 25 Vdc
C7 — 0.01 μF, Ceramic
RFC1 — 10 μH Molded Choke

RFC2 — 12 Turns, #16 AWG, Enameled Wire Closewound on a 2 W Carbon Resistor
L1 — 2 Turns, #18 AWG Enameled Wire, 0.4″ ID, 0.15″ Long
L2 — Loop, #12 AWG Wire, 0.6″ High, 0.4″ Wide
L3 — 2 Turns, #12 AWG Wire, ID 0.4″, 0.25″ Long
Bead — Ferrite Bead Ferroxcube #56-590-65/3B

FIGURE 2 — OUTPUT POWER versus INPUT POWER

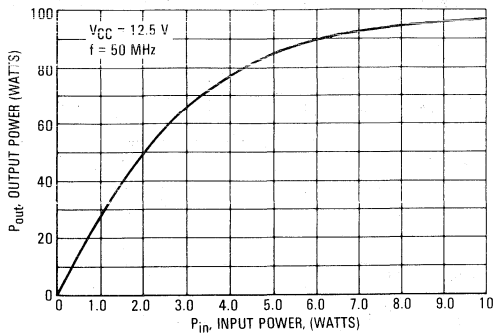


FIGURE 3 — POWER GAIN versus FREQUENCY

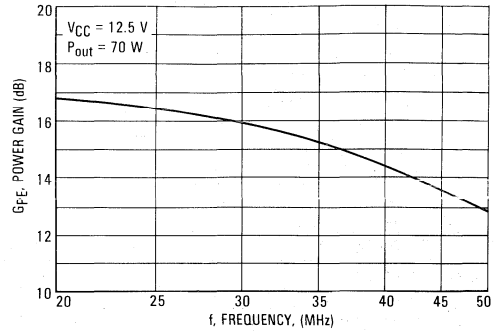
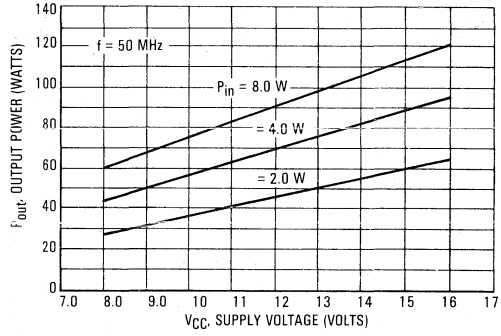
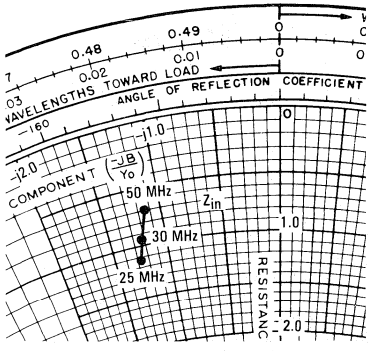


FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE



3

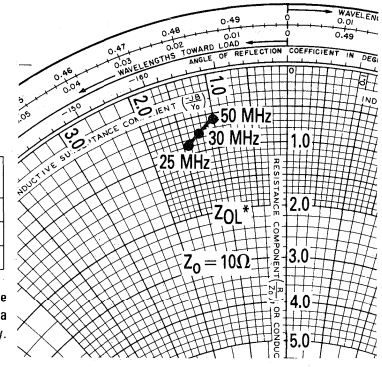
FIGURE 5 — SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCES



V_{CC} = 12.5 V, P_{out} = 70 W

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
50	0.7 – j1.17	0.58 – j1.0
30	0.93 – j1.24	0.76 – j1.3
25	1.12 – j1.28	0.85 – j1.46

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.



MRF497

The RF Line

40 W 50 MHz

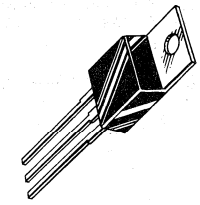
RF POWER TRANSISTOR

NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed for 12.5-volt VHF large-signal power amplifier applications in commercial and industrial equipment, operating in the 25 to 50 MHz frequency range.

- Low-Cost, Common-Emitter TO-220 Package
- Specified 12.5 V, 50 MHz Performance —
  Output Power = 40 Watts
  Power Gain = 10 dB Min
  Efficiency = 60% Min
- Load Mismatch Capability at Rated Voltage and RF Drive



3

MAXIMUM RATINGS

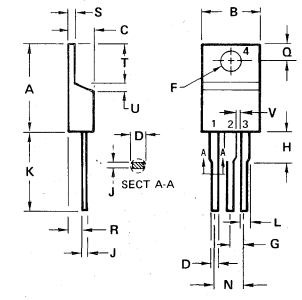
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Continuous	I_C	6.0	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	87.5 0.5	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	2.0	°C/W

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.



STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

NOTE:
1. DIM. L & H APPLIES TO ALL LEADS.

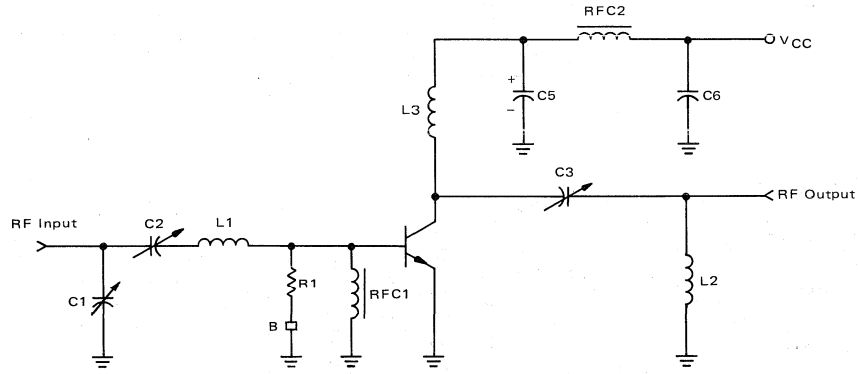
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

CASE 221A-02

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	—	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	—	250	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 40 W, f = 50 MHz)	G_{PE}	10	11.2	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 40 W, f = 50 MHz)	η	60	—	—	%

FIGURE 1 — 50 MHz TEST CIRCUIT



C1 — Arco 469
C2, C3 — Arco 466
C5 — 100 μF, 16 Vdc Electrolytic
C6 — 0.001 μF Disc Ceramic

R1 — 10 Ω, 1.0 Watt Resistor

L1 — 3 Turns #14 AWG Wire, 1/3" ID
L2 — 1-1/2 Turns #14 AWG Wire, 1/2" ID
L3 — 14 Turns #18 AWG Wire 1/4" ID

RFC1 — RF Choke Ferroxcube VK200-20/4B
RFC2 — 3 Ferroxcube, #56-590-65/3B, Beads on #18 AWG Wire

B — Ferroxcube #56-490-65/3B

Board Material — Epoxy Fiberglass, 0.062" thick

FIGURE 2 – POWER GAIN versus FREQUENCY

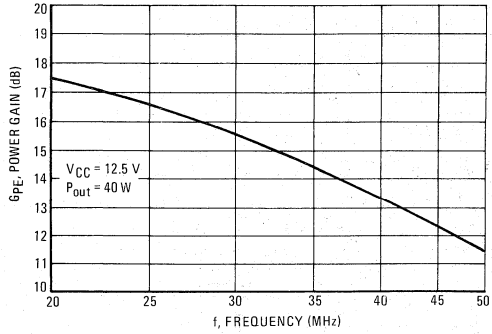


FIGURE 3 – OUTPUT POWER versus INPUT POWER

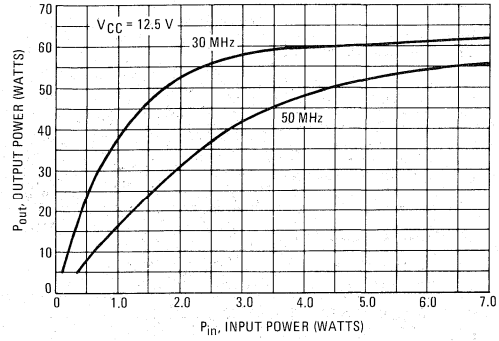
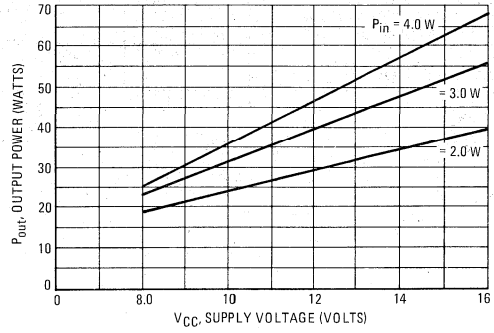


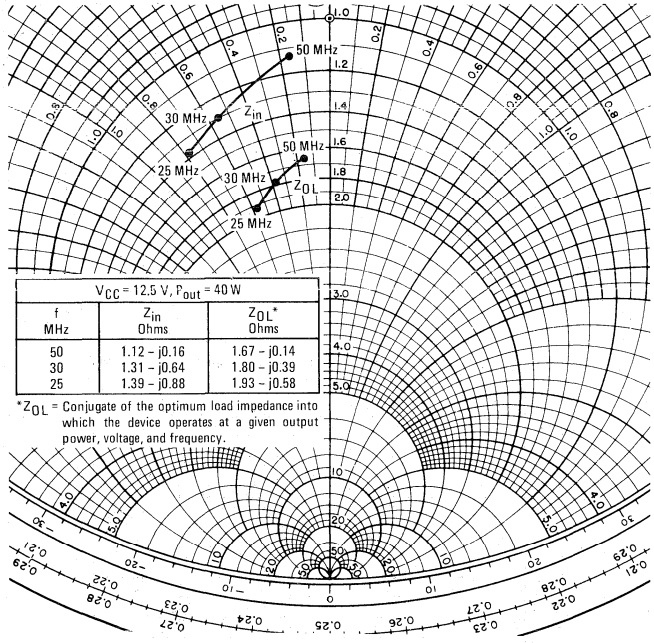
FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

50 MHz



3

FIGURE 5 — SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCES

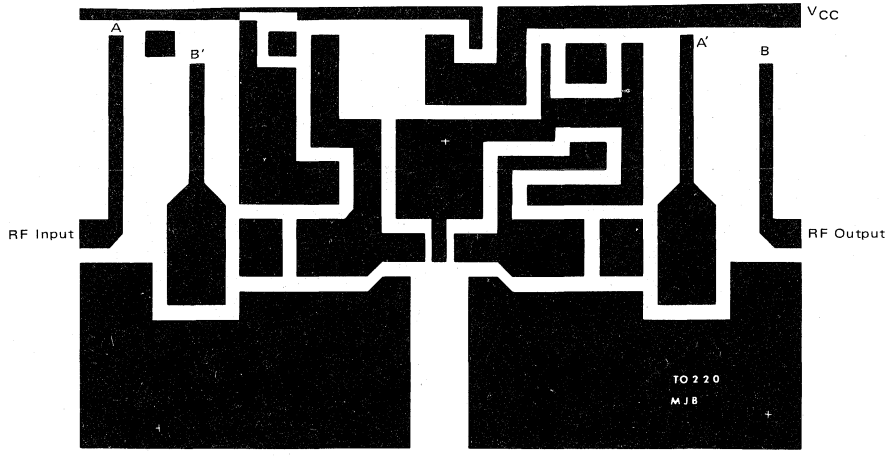


V_{CC} = 12.5 V, P_{out} = 40 W		
f MHz	Z_{in} Ohms	Z_{OL}^* Ohms
50	1.12 – j0.16	1.67 – j0.14
30	1.31 – j0.64	1.80 – j0.39
25	1.39 – j0.88	1.93 – j0.58

*Z_{OL} = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

3

FIGURE 6 — TEST AMPLIFIER PCB PHOTOMASTER



NOTE: Points A, A′ and B, B′ are connected via 50 Ω coaxial cable under the PCB.
The Printed Circuit Board shown is 75% of the original.

MRF501
MRF502

The RF Line

NPN SILICON HIGH-FREQUENCY TRANSISTORS

. . . designed primarily for use in high-gain, low-noise amplifier, oscillator, and mixer applications. Can also be used in UHF converter applications.

- High Current-Gain — Bandwidth Product —
  f_T = 1.2 GHz (Typ) @ I_C = 5.0 mAdc
- Low Noise Figure —
  NF = 4.0 dB (Typ) @ f = 200 MHz

HIGH FREQUENCY
TRANSISTORS

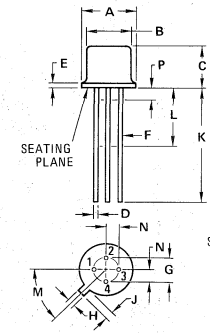
NPN SILICON



3

MAXIMUM RATINGS

Rating	Symbol	MRF501	MRF502	Unit
Collector-Emitter Voltage	V_{CEO}	15		Vdc
Collector-Base Voltage	V_{CBO}	25	35	Vdc
Emitter-Base Voltage	V_{EBO}	3.5		Vdc
Collector Current	I_C	50		mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	200 1.14		mW mW/°C
Storage Temperature Range	T_{stg}	-65 to +200		°C



STYLE 10
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. CASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

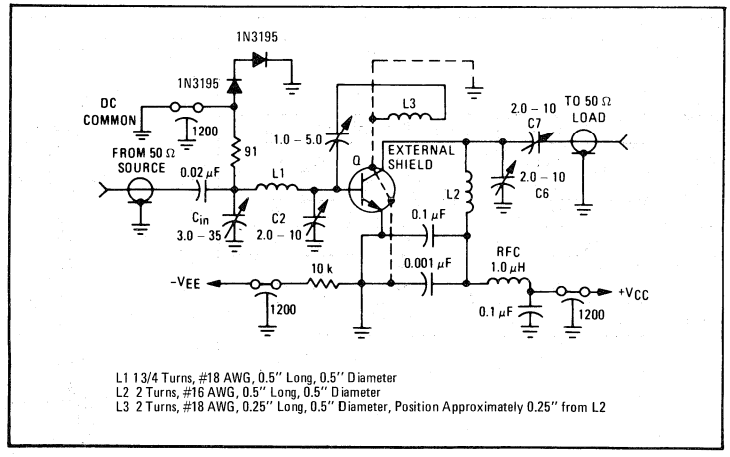
ALL JEDEC dimensions and notes apply
CASE 20-03
TO-72

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 3.0 mAdc, I_B = 0)		$V_{(BR)CEO}$	15	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 1.0 μAdc, I_E = 0)	MRF501 MRF502	$V_{(BR)CBO}$	25 35	– –	– –	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 μAdc, I_C = 0)		$V_{(BR)EBO}$	3.5	–	–	Vdc
Collector Cutoff Current (V_{CB} = 1.0 Vdc, I_E = 0)	MRF501 MRF502	I_{CBO}	– –	– –	50 20	nAdc
ON CHARACTERISTICS						
DC Current Gain (I_C = 1.0 mAdc, V_{CE} = 6.0 Vdc)	MRF501 MRF502	h_{FE}	30 40	– –	250 170	–
DYNAMIC CHARACTERISTICS						
Current Gain – Bandwdith Product (I_C = 5.0 mAdc, V_{CE} = 6.0 Vdc, f = 100 MHz)	MRF501 MRF502	f_T	600 800	1000 1200	– –	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 to 1.0 MHz)		C_{cb}	–	0.6	–	pF
Collector-Base Time Constant (I_E = 2.0 mAdc, V_{CB} = 6.0 Vdc, f = 31.8 MHz)		$r_b'C_c$	–	8.0	–	ps
Noise Figure (Figure 1) (I_C = 1.5 mAdc, V_{CE} = 6.0 Vdc, R_S = 50 ohms, f = 200 MHz)	MRF501 MRF502	NF	– –	4.5 4.0	– –	dB
FUNCTIONAL TEST						
Common-Emitter Amplifier Power Gain (Figure 1) (V_{CC} = 6.0 Vdc, I_C = 5.0 mAdc, f = 200 MHz)	MRF501 MRF502	G_{pe}	– –	15 17	– –	dB

3

FIGURE 1 – 200 MHz AMPLIFIER POWER GAIN AND NOISE FIGURE CIRCUIT



L1 13/4 Turns, #18 AWG, 0.5" Long, 0.5" Diameter
L2 2 Turns, #16 AWG, 0.5" Long, 0.5" Diameter
L3 2 Turns, #18 AWG, 0.25" Long, 0.5" Diameter, Position Approximately 0.25" from L2

MRF511

The RF Line

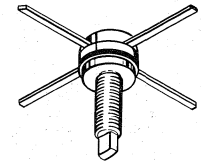
NPN SILICON HIGH FREQUENCY TRANSISTOR

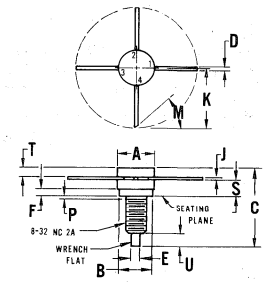
. . . designed specifically for broadband applications requiring low distortion characteristics and noise figure. Specified for use in CATV applications.

- Specified +50 dBmV Output, 80 mAdc Distortion Characteristics –
  Triple Beat = -65 dB (Max)
  Cross Modulation = -57 dB (Max)
  Second Order = -50 dB (Max)
- High Broadband Power Gain –
  G_{pe} = 10 dB (Min) @ f = 250 MHz
- Low Broadband Noise Figure –
  NF = 10 dB (Max) @ f = 200 MHz

HIGH FREQUENCY TRANSISTOR

NPN SILICON





STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.06	7.26	0.278	0.286
B	6.20	6.50	0.244	0.256
C	15.24	16.51	0.600	0.650
D	0.66	0.86	0.026	0.034
E	1.40	1.65	0.055	0.065
F	1.52	–	0.060	–
J	0.10	0.15	0.004	0.006
K	11.17	–	0.440	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
S	2.74	3.35	0.108	0.132
T	1.40	1.78	0.055	0.070
U	2.92	3.68	0.115	0.145

CASE 244A-01

MAXIMUM RATINGS

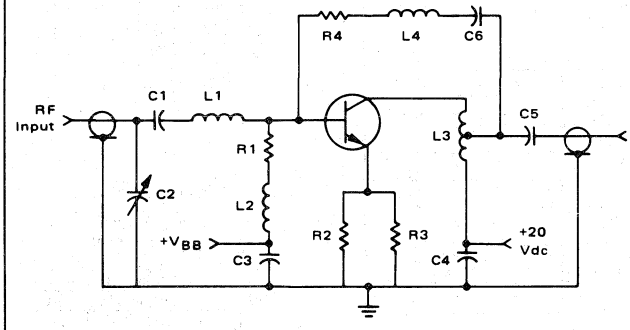
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	25	Vdc
Collector-Base Voltage	V_{CBO}	35	Vdc
Emitter-Base Voltage	V_{EBO}	3.5	Vdc
Collector Current – Continuous	I_C	250	mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	5.0 28.6	Watts mW/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Stud Torque(1)	–	6.5	In. Lb.

(1) For Repeated Assembly use 5 In. Lb.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	$V_{(BR)CBO}$	35	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	–	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, I_B = 0)	I_{CEO}	–	–	100	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 80 mAdc, V_{CE} = 10 Vdc)	h_{FE}	25	50	200	–
Collector-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)	$V_{CE(sat)}$	–	0.2	0.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 80 mAdc, V_{CE} = 20 Vdc, f = 200 MHz)	f_T	1.5	2.1	–	GHz
Output Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	3.2	4.5	pF
Noise Figure (I_C = 50 mAdc, V_{CE} = 20 Vdc, f = 200 MHz)	NF	–	7.3	10	dB
FUNCTIONAL TESTS (Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CE} = 20 Vdc, I_C = 80 mAdc, f = 250 MHz)	G_{pe}	10	11	–	dB
2nd Order Intermodulation Distortion (V_{CE} = 20 Vdc, I_C = 80 mAdc, V_{out} = +50 dBmV, Chn 2 + Chn 13 = 266.5 MHz)	IMD	–	-55	-50	dB
Cross-Modulation Distortion (V_{CE} = 20 Vdc, V_{out} = +50 dBmV, I_C = 80 mAdc) Chn 13 / Chn R	12 Chn XMD / 30 Chn XMD	– / –	-59 / -46	-57 / –	dB
Triple Beat (V_{CE} = 20 Vdc, I_C = 80 mAdc, V_{out} = +50 dBmV, Chn 2 + Chn 3 + Chn E = 261.75 MHz)	TB	–	-68	-65	dB

FIGURE 1 – 40 to 330 MHz BROADBAND TEST CIRCUIT SCHEMATIC



CIRCUIT PERFORMANCE	Min	Typ
Input/Output Return Loss	–	18 dB
Flatness	–	+0.3 dB
Gain	10 dB	
Bandwidth	–	40-300 MHz

C1,C3,C4,C5,C6	0.002 μF Ceramic Disc
C2	0.35-3.5 pF JOHANSON 4702
L1	2 Turns, #20 AWG, 1/8" I.D., 0.2 " Long
L2	5 μH, Ferrite Choke, MILLER
L3	18 Turns, #24 AWG Enamelled, on Ferrite Torrid Core FERROXCUBE 1041T060-4C7
L4	5 Turns, #20 AWG, 3/16" I.D., 0.35" Long

R1	4.7 kΩ, 1/4W, 10%
R2	27 Ω, 1W, 10%
R3	27 Ω, 1W,10%
R4	300 Ω, 1/4W, 10%.

Input/Output Connectors – Type F

Z_o – 75 Ohms

FIGURE 2 – CURRENT-GAIN–BANDWIDTH PRODUCT

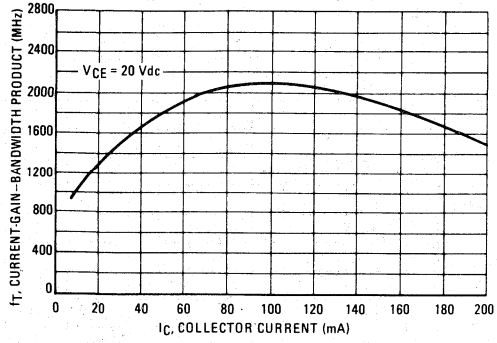


FIGURE 3 – OUTPUT CAPACITANCE

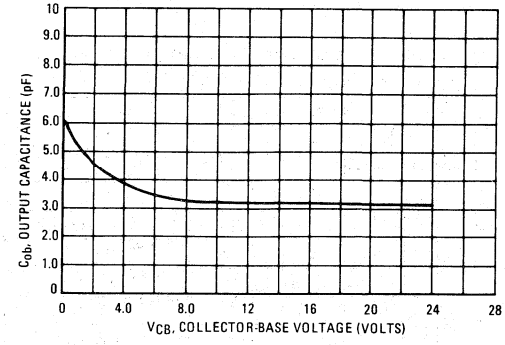


FIGURE 4 – INPUT CAPACITANCE

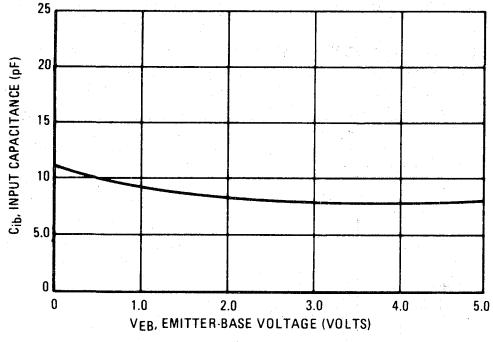


FIGURE 5 – BROADBAND NOISE FIGURE

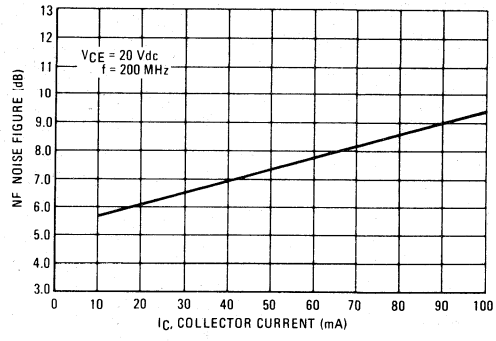


FIGURE 6 – 12 CHANNEL CROSS-MODULATION versus COLLECTOR-EMITTER VOLTAGE

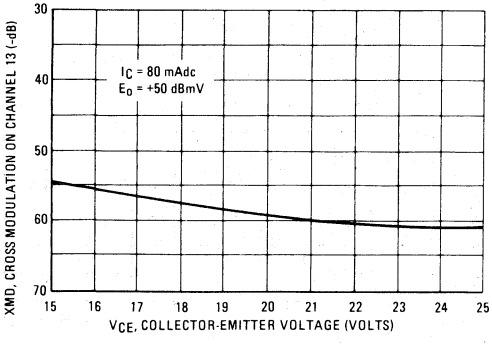
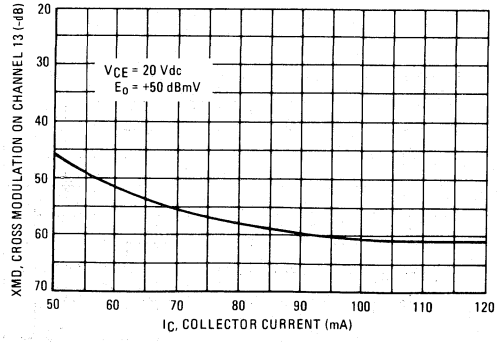


FIGURE 7 – 12 CHANNEL CROSS-MODULATION versus COLLECTOR CURRENT



3

FIGURE 8 – 30 CHANNEL CROSS-MODULATION ON CHANNEL R

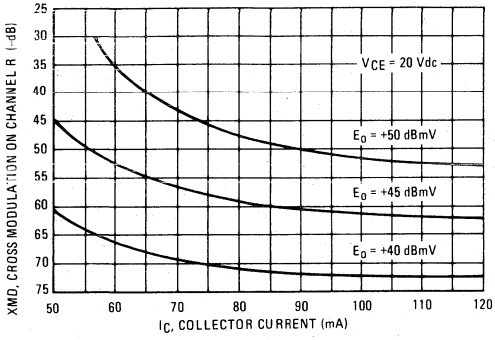


FIGURE 9 – 30 CHANNEL CROSS-MODULATION ON CHANNEL 2,13,R

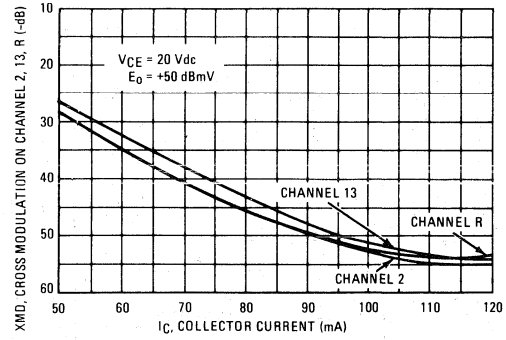


FIGURE 10 – 30-CHANNEL CROSS-MODULATION versus COLLECTOR-EMITTER VOLTAGE

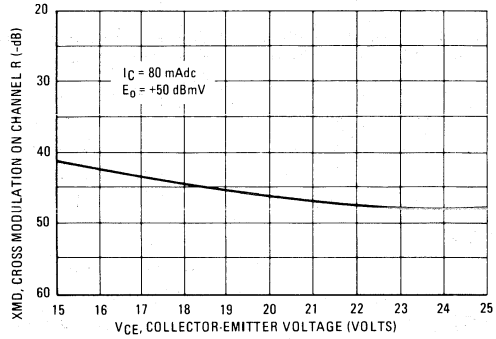


FIGURE 11 – TRIPLE BEAT versus COLLECTOR CURRENT

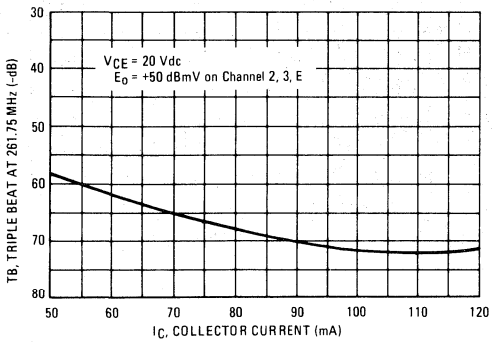


FIGURE 12 – TRIPLE BEAT versus COLLECTOR-EMITTER VOLTAGE

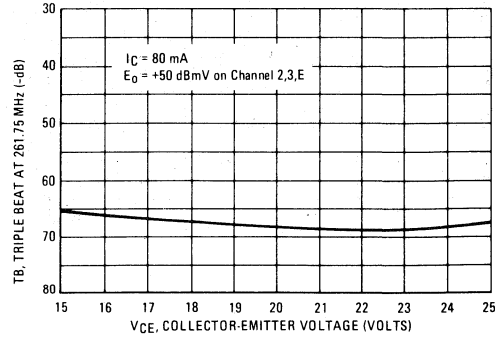


FIGURE 13 – SECOND ORDER IMD versus COLLECTOR CURRENT

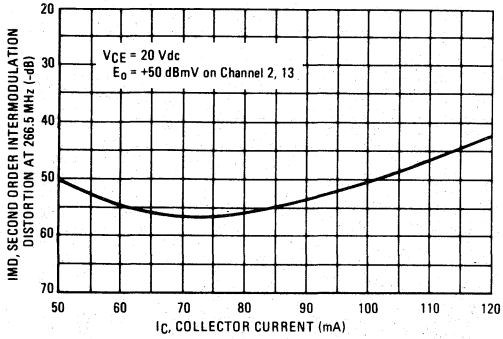


FIGURE 14 – SECOND ORDER IMD versus COLLECTOR-EMITTER VOLTAGE

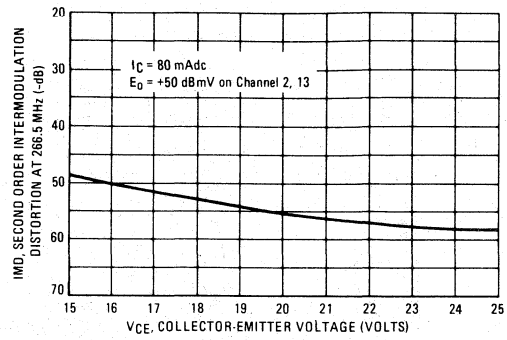
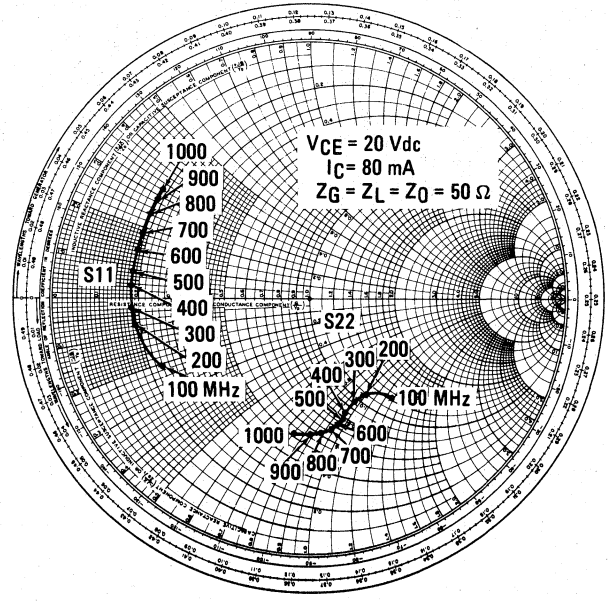


FIGURE 15 – INPUT REFLECTION COEFFICIENT (S11) AND OUTPUT REFLECTION COEFFICIENT (S22) versus FREQUENCY



3

FIGURE 16 – FORWARD TRANSMISSION COEFFICIENT (S12) versus FREQUENCY

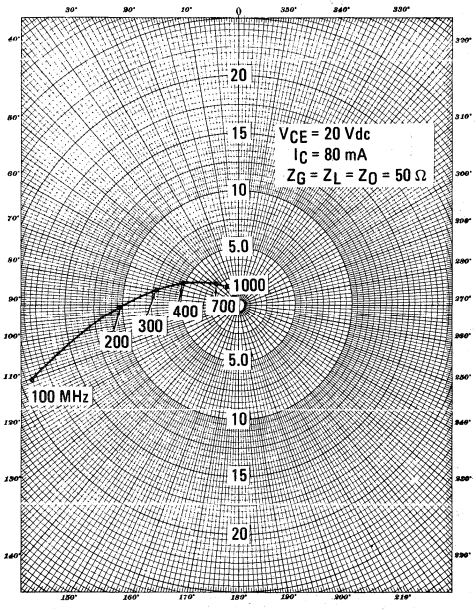
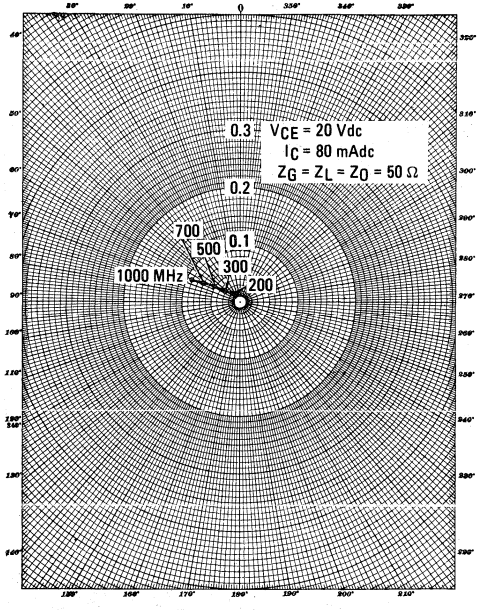


FIGURE 17 – REVERSE TRANSMISSION COEFFICIENT (S21) versus FREQUENCY



3

MRF515

The RF Line

0.75 W — 470 MHz

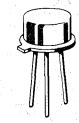
HIGH FREQUENCY TRANSISTOR

NPN SILICON

NPN SILICON HIGH FREQUENCY TRANSISTOR

. . . designed for 12.5 Volt UHF large-signal amplifier applications required in industrial equipment

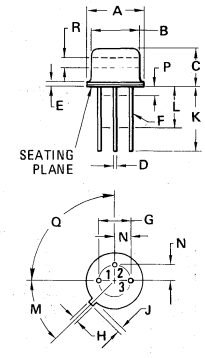
- Specified 12.5 Volt, 470 MHz Characteristics —
  Output Power = 0.75 Watts
  Minimum Gain = 8.0 dB
  Efficiency = 50%
- S Parameter Data From 100 MHz to 1.0 GHz



3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CBO}	35	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	150	mAdc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	2.5 14.3	Watts mW/^{o}C
Storage Temperature Range	T_{stg}	-65 to +200	^{o}C



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	—	0.500	—
L	6.35	—	0.250	—
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
Q	90° NOM		90° NOM	
R	2.54	—	0.100	—

All JEDEC dimensions arid notes apply.

STYLE 1
PIN 1. EMITTER
2. BASE
3. COLLECTOR

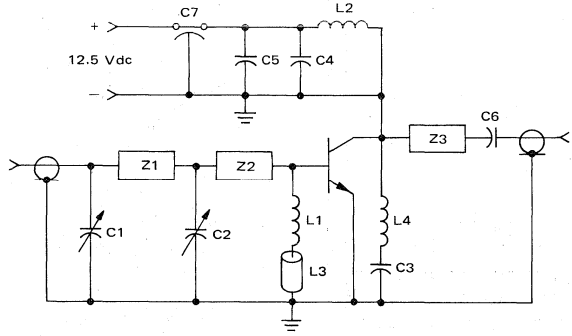
CASE 79-02
TO-39

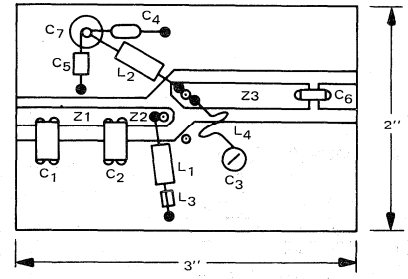
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	$V_{(BR)CBO}$	35	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, I_B = 0)	I_{CEO}	–	–	10	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	20	60	150	–
Collector-Emitter Saturation Voltage (I_C = 50 mAdc, I_B = 5.0 mAdc)	$V_{CE(sat)}$	–	–	0.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 200 MHz)	f_T	1800	2000	–	MHz
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	3.5	4.0	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 0.75 W, f = 470 MHz)	G_{PE}	8.0	8.5	–	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 0.75 W, f = 470 MHz)	η	50	70	–	%
Series Equivalent Input Impedance (V_{CC} = 12.5 Vdc, P_{out} = 0.75 W, f = 470 MHz)	Z_{in}	–	14+j4.0	–	Ohms
Series Equivalent Output Impedance (V_{CC} = 12.5 Vdc, P_{out} = 0.75 W, f = 470 MHz)	Z_{out}	–	28-j38	–	Ohms

3

FIGURE 1 – 470 MHz TEST CIRCUIT





C1,C2,C3 - 1.0-10 pF JOHANSON
C4 - 0.1 μF disc
C5 - 1.0 μF TANTULAM
C6 - 0.018 μF chip
C7 - 1000 pF Feedthru
L1,L2 - 0.15 μF Choke
L3 - Bead Ferrite
Z1,Z2 - 0.09" x 0.5" LINE, Z_o = 100 Ω
Z3 - 0.18" x 1.0" LINE, Z_o = 50 Ω

BOARD = 0.032" TEFLONGLASS, ϵ_R = 2.5

FIGURE 2 – OUTPUT POWER versus INPUT POWER

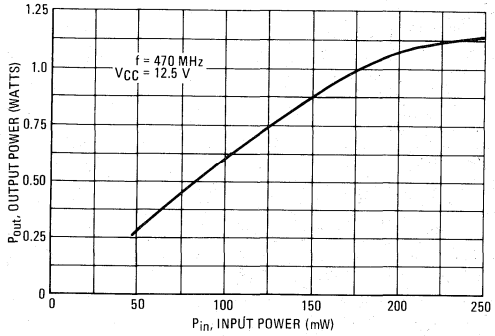


FIGURE 3 – CURRENT-GAIN – BANDWIDTH PRODUCT versus COLLECTOR CURRENT

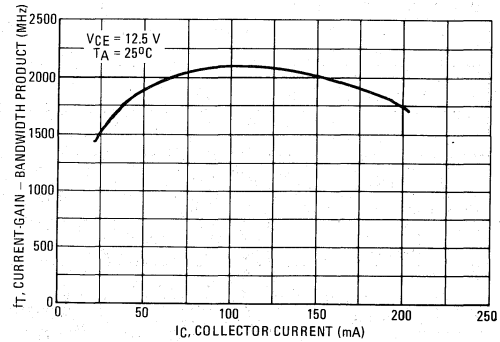
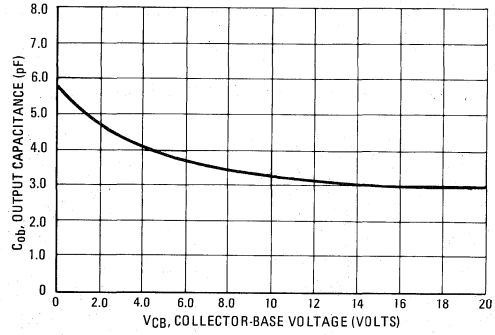
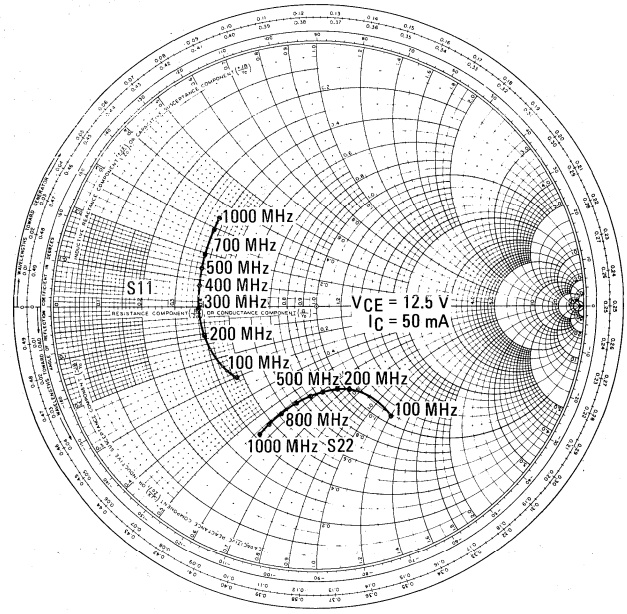


FIGURE 4 – OUTPUT CAPACITANCE versus COLLECTOR BASE VOLTAGE



3

FIGURE 5 – S_{11} and S_{22} versus FREQUENCY



3

FIGURE 6 – S_{12} versus FREQUENCY

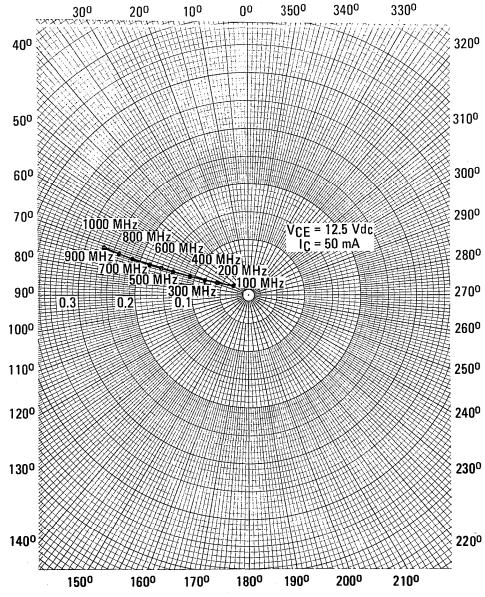
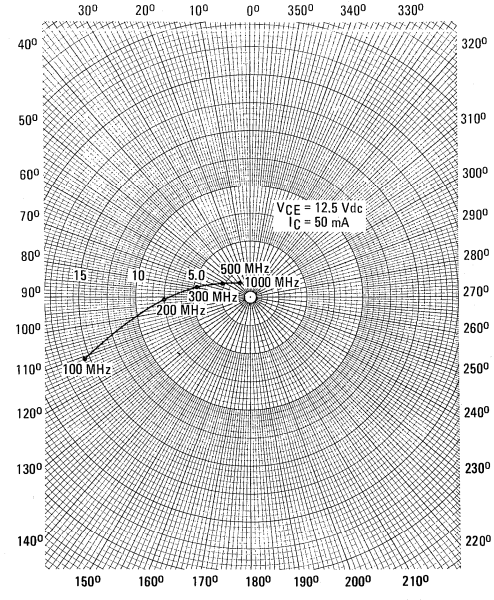


FIGURE 7 – S_{21} versus FREQUENCY



MRF517

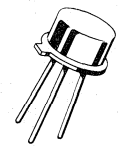
The RF Line

NPN SILICON HIGH FREQUENCY TRANSISTOR

. . . designed specifically for broadband applications requiring low distortion characteristics. Specified for use in CATV distribution equipment.

- Specified +45 dBmV Output, 60 mA Distortion Characteristics –
  Triple Beat = -72 dB (Max)
  12 Channel Cross Modulation = -57 dB (Max)
  Second Order = -60 dB (Max)
- Broadband Power Gain –
  G_{PE} = 10 dB (Typ)
- Broadband Noise Figure –
  NF = 7.5 dB (Max) @ f = 300 MHz

HIGH FREQUENCY
TRANSISTOR
NPN SILICON



3

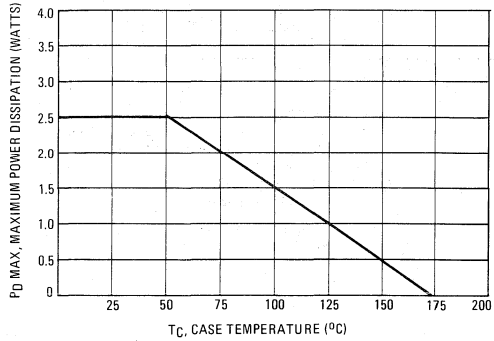
MAXIMUM RATINGS

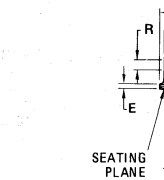
Rating	Symbol	Value	Unit
Collector-Emitter Voltage (R_{BE} = 330 Ω)	V_{CER}	25	Vdc
Collector-Base Voltage	V_{CBO}	35	Vdc
Emitter-Base Voltage	V_{EBO}	3.5	Vdc
Collector Current – Continuous	I_C	150	mAdc
Total Power Dissipation @ T_C = 50°C Derate above 50°C	P_D	2.5 0.02	Watts W/°C
Operating Junction Temperature	T_J	+175	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

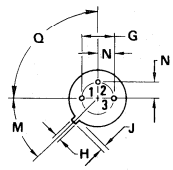
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	50	°C/W

FIGURE 1 – POWER DISSIPATION







STYLE 1
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

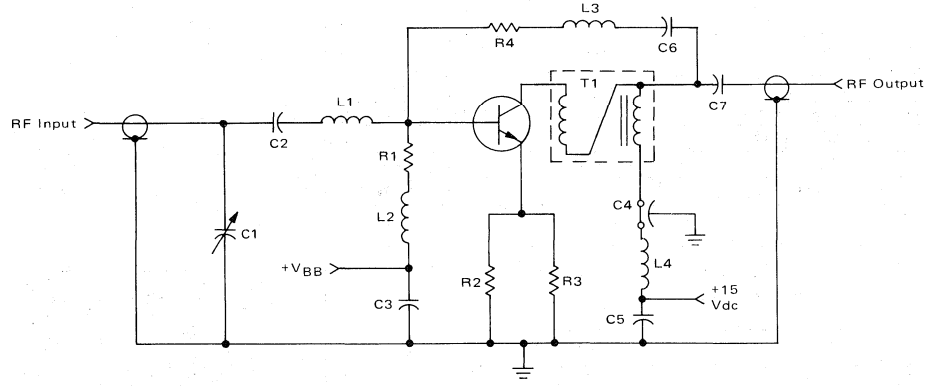
All JEDEC dimensions and notes apply.

CASE 79-02
TO-39

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, R_{BE} = 330 Ohms)	$V_{(BR)CER}$	25	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	$V_{(BR)CBO}$	35	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	–	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, I_B = 0)	I_{CEO}	–	–	100	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 60 mAdc, V_{CE} = 10 Vdc)	h_{FE}	40	–	200	–
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 60 mAdc, V_{CE} = 15 Vdc, f = 200 MHz)	f_T	2200	2700	–	MHz
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	3.0	4.5	pF
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (V_{CE} = 15 Vdc, I_C = 60 mAdc, f = 300 MHz)	G_{pe}	–	10	–	dB
Broadband Noise Figure (V_{CE} = 15 Vdc, I_C = 50 mAdc, f = 300 MHz)	NF	–	–	7.5	dB
2nd Order Distortion (V_{CE} = 15 Vdc, I_C = 60 mAdc, E_{out} = +45 dBmV, Ch 2 + Ch G = 212.5 MHz)	IMD_2	–	–	-57	dB
NCTA Cross Modulation Distortion, 12 Ch's (2-13) (V_{CE} = 15 Vdc, I_C = 60 mAdc, E_{out} = +45 dBmV, Measured at Ch's 2 and 13)	XMD_{12}	–	–	-57	dB
Triple Beat Distortion, 3 Ch's (V_{CE} = 15 Vdc, I_C = 60 mAdc, E_{out} = +45 dBmV, Ch's (4 + 5 + A) = 265 MHz)	TB_3	–	–	-72	dB

FIGURE 2 – 40 to 330 MHz BROADBAND TEST CIRCUIT SCHEMATIC



C1	1.0 – 10 pF JOHANSON
C2,C6,C7	0.002 μF Ceramic Disk
C3,C5	0.1 μF, 50 Vdc Tantalum
C4	1000 pF Button
L1	1 Turn, #20 AWG
L2	5.6 μH Molded Choke
L3	4 Turns, #20 AWG, 1/4" I.D.
L4	VK200
T1	16:1 Bifilar Wound, #20 AWG Enameled Wire, Wound on a FERROXCUBE 1041T060-4C4 Core
R1	4.7 kΩ, 1/4 Watt, 10%
R2,R3	27 Ω , 1/4 Watt, 5%
R4	270 Ω, 1/4 Watt, 5%

Input/Output Connectors – Type F
Z_o = 75 Ohms

FIGURE 3 – TYPICAL RESPONSE CURVE
(See Figure 2)

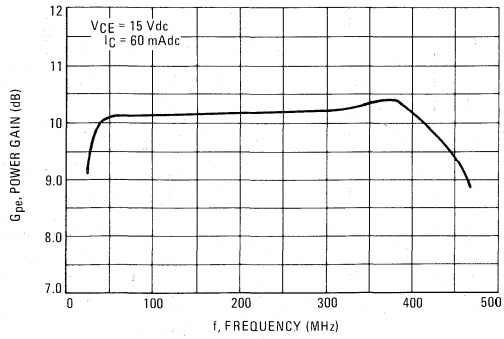


FIGURE 4 – COMMON-EMITTER POWER GAIN versus FREQUENCY

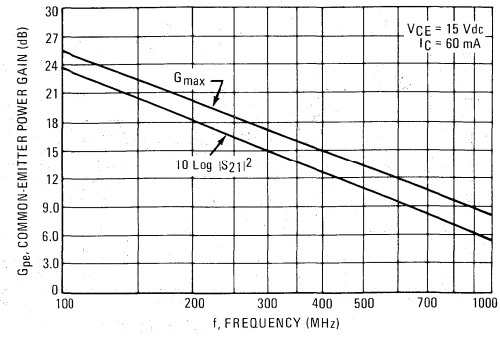


FIGURE 5 – CURRENT GAIN BANDWIDTH PRODUCT versus COLLECTOR CURRENT

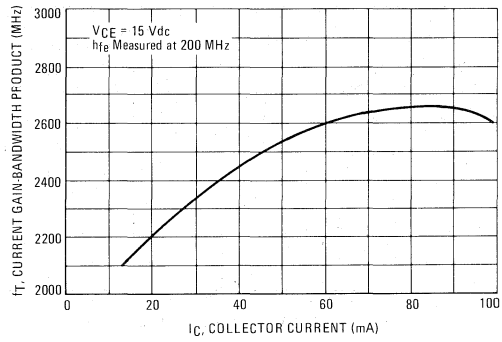


FIGURE 6 – INPUT CAPACITANCE versus EMITTER-BASE VOLTAGE

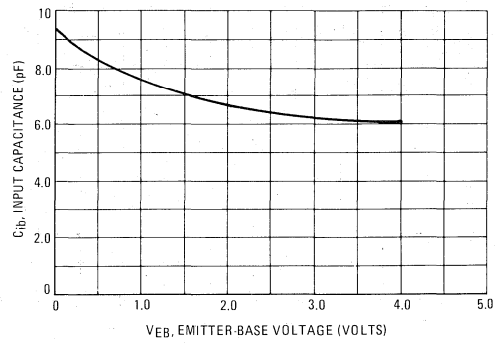


FIGURE 7 – OUTPUT CAPACITANCE versus COLLECTOR-BASE VOLTAGE

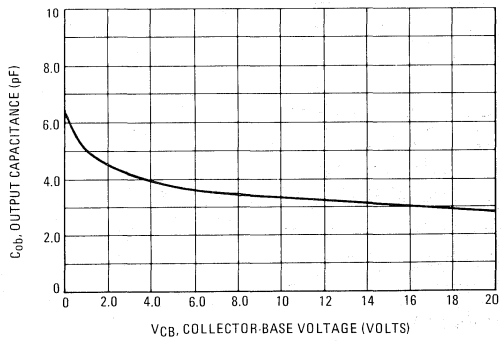


FIGURE 8 – BROADBAND NOISE FIGURE versus COLLECTOR CURRENT

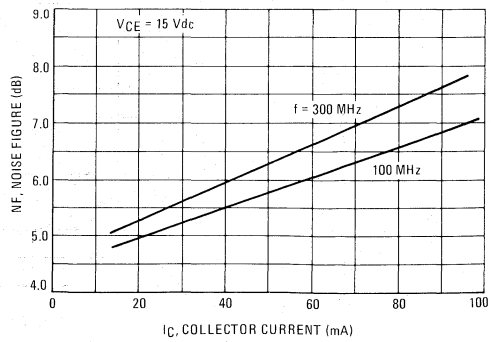


FIGURE 9 – 2nd ORDER DISTORTION ($f_1 \pm f_2$) versus COLLECTOR CURRENT

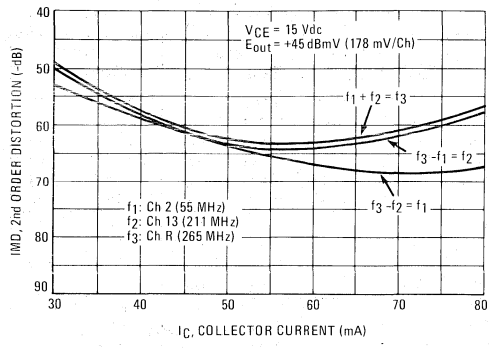


FIGURE 10 – 12-CHANNEL CROSS MODULATION DISTORTION versus COLLECTOR CURRENT

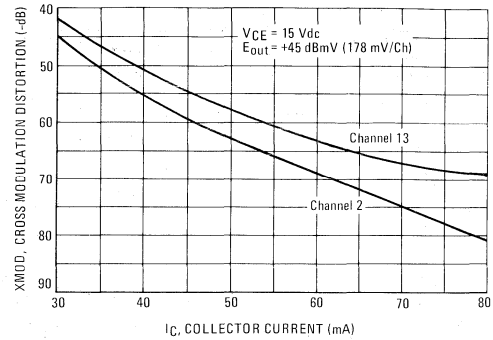


FIGURE 11 – DIN 45004 CROSS-MODULATION DISTORTION

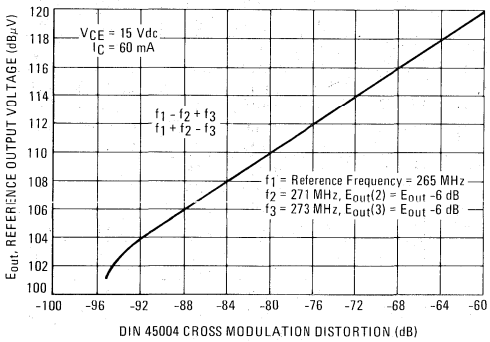


FIGURE 12 – TRIPLE BEAT DISTORTION ($f_1 + f_2 + f_3$) versus COLLECTOR CURRENT

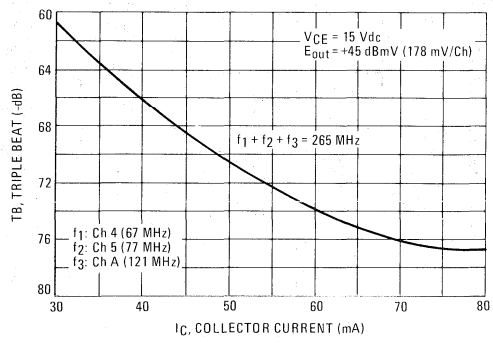
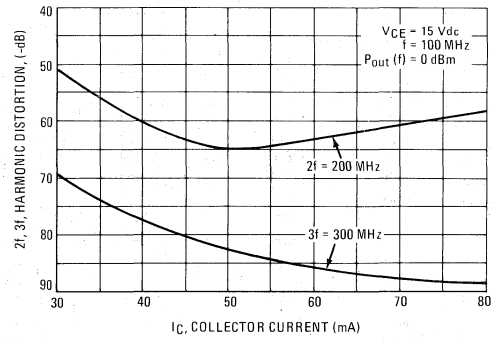


FIGURE 13 – HARMONIC DISTORTION (2f, 3f) versus COLLECTOR CURRENT



V_{CE} (Volts)	I_C (mA)	Frequency (MHz)	S11		S21		S12		S22	
			|S11|	∠φ	|S21|	∠φ	|S12|	∠φ	|S22|	∠φ
5	30	100	0.538	-152	12.821	100	0.043	49	0.381	-102
		200	0.546	-173	6.612	86	0.064	55	0.314	-121
		400	0.557	163	3.440	71	0.105	60	0.315	-132
		600	0.602	147	2.357	59	0.144	61	0.360	-140
		800	0.625	136	1.872	46	0.181	59	0.437	-143
		1000	0.626	120	1.614	34	0.211	57	0.482	-144
	60	100	0.532	-160	13.475	98	0.040	54	0.362	-111
		200	0.542	-178	6.850	86	0.063	60	0.314	-130
		400	0.558	160	3.586	72	0.109	63	0.313	-140
		600	0.602	145	2.475	60	0.151	62	0.353	-146
		800	0.619	134	1.962	48	0.190	59	0.423	-147
		1000	0.616	118	1.706	35	0.221	57	0.464	-147
	90	100	0.532	-163	13.530	98	0.038	57	0.354	-115
		200	0.545	179	6.908	85	0.063	62	0.313	-133
		400	0.558	159	3.607	72	0.111	64	0.312	-143
		600	0.604	145	2.489	61	0.153	63	0.352	-148
		800	0.620	133	1.982	48	0.193	59	0.419	-149
		1000	0.614	117	1.721	35	0.224	57	0.455	-148
10	30	100	0.500	-145	14.176	102	0.040	50	0.386	-87
		200	0.502	-170	7.358	87	0.059	55	0.304	-105
		400	0.512	164	3.819	71	0.097	61	0.304	-118
		600	0.559	149	2.593	59	0.133	62	0.356	-128
		800	0.583	137	2.033	46	0.166	60	0.442	-134
		1000	0.584	122	1.724	34	0.194	59	0.497	-137
	60	100	0.487	-154	14.977	100	0.037	55	0.353	-96
		200	0.498	-174	7.715	86	0.059	60	0.287	-114
		400	0.506	161	4.009	72	0.101	63	0.294	-125
		600	0.553	146	2.731	60	0.139	63	0.341	-133
		800	0.572	135	2.158	47	0.174	60	0.422	-137
		1000	0.569	119	1.835	35	0.202	58	0.475	-139
	90	100	0.486	-157	15.192	99	0.036	57	0.337	-98
		200	0.493	-176	7.764	86	0.058	61	0.280	-116
		400	0.508	160	4.043	72	0.101	64	0.287	-126
		600	0.555	145	2.761	60	0.141	63	0.336	-134
		800	0.574	134	2.184	47	0.176	60	0.417	-138
		1000	0.568	118	1.861	35	0.204	58	0.469	-139
15	30	100	0.465	-153	15.774	100	0.035	56	0.337	-88
		200	0.475	-174	8.091	86	0.056	61	0.274	-105
		400	0.487	161	4.209	71	0.097	64	0.284	-116
		600	0.532	146	2.863	59	0.133	63	0.337	-126
		800	0.551	135	2.249	47	0.167	60	0.425	-132
		1000	0.547	119	1.909	34	0.193	58	0.482	-135
	60	100	0.468	-150	15.650	101	0.036	54	0.354	-87
		200	0.475	-172	8.088	87	0.057	60	0.282	-104
		400	0.486	163	4.178	72	0.096	63	0.290	-116
		600	0.530	147	2.846	60	0.133	63	0.341	-126
		800	0.549	136	2.228	47	0.166	60	0.429	-132
		1000	0.547	120	1.887	34	0.192	59	0.487	-135
	90	100	0.487	-141	14.773	103	0.039	50	0.391	-80
		200	0.486	-167	7.724	87	0.057	55	0.303	-97
		400	0.491	166	3.986	71	0.093	61	0.306	-110
		600	0.537	150	2.694	59	0.127	62	0.359	-122
		800	0.565	138	2.108	45	0.159	60	0.448	-129
		1000	0.566	123	1.779	33	0.185	60	0.507	-134

MRF521
MRFC521
MRF522
MRF524
MRF5211,L

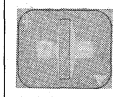
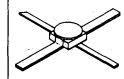
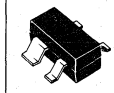
HIGH FREQUENCY TRANSISTORS PNP SILICON

The RF Line
PNP Silicon
High-Frequency Transistors

. . . designed primarily for use in the high-gain, low-noise small-signal amplifiers for operation up to 3.5 GHz. Also usable in applications requiring fast switching times.

- High Current Gain-Bandwidth Product — f_T = 4.2 GHz (Typ) @ I_C = 50 mAdc
- Low Noise Figure @ f = 1 GHz — $NF_{(matched)}$ = 2.8 dB (Typ)
- High Power Gain — $G_{pe\ (matched)}$ = 11 dB (Typ)
- Guaranteed RF Parameters
- Surface Mounted SOT-143 Offers Improved RF Performance
  - Lower Package Parasitics
  - Higher Gain
- Available In Both Standard Profile (MRF5211) and Low Profile (MRF5211L)
- Tape and Reel Packaging Options

3

MAXIMUM RATINGS		MRFC521  Chip	MRF521  Macro-X Case 317-01	MRF522  Case 303-01	MRF524  Case 20-03 (TO-72)	MRF5211,L  Case 318B-01 (SOT-143)	
Ratings	**Symbol**	**Values**					**Unit**
Collector-Emitter Voltage	V_{CEO}	10	10	10	10	10	Vdc
Collector-Base Voltage	V_{CBO}	20	20	20	20	20	Vdc
Emitter-Base Voltage	V_{EBO}	2.5	2.5	2.5	2.5	2.5	Vdc
Maximum Junction Temperature	T_{Jmax}	200	150	200	200	150	°C
Collector Current — Continuous	I_C	50	70	50	50	70	mA
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	— —	— —	— —	0.2 1.14	0.58 4.64	Watts mW/°C
Total Device Dissipation @ T_C = 75°C Derate above 75°C	P_D	0.75 —	0.75 10	0.62 5	— —	0.58 7.7	Watts mW/°C
Storage Temperature	T_{stg}	−65 to +200	−65 to +150	−65 to +200	−65 to +200	−65 to +150	°C
THERMAL CHARACTERISTICS							
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	—	—	—	870	216	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	—	100	200	—	130	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1 mAdc, I_B = 0)	$V_{(BR)CEO}$	10	12	—	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	20	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 50 μAdc, I_C = 0)	$V_{(BR)EBO}$	2.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 8 Vdc, I_E = 0)	I_{CBO}	—	—	10	μAdc

Note 1. Case Temperature is measured on the collector lead where it first contacts the printed circuit board closest to the package.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS						
DC Current Gain (I_C = 30 mAdc, V_{CE} = 5 Vdc)		h_{FE}	25	—	125	—
DYNAMIC CHARACTERISTICS						
Collector-Base Capacitance (V_{CB} = 6 Vdc, I_E = 0, f = 1 MHz)	Figure 1	C_{cb}	—	1	1.5	pF
Current Gain — Bandwidth Product (V_{CE} = 8 Vdc, I_C = 50 mA, f = 1 GHz)	Figure 7	f_T	—	4.2	—	GHz
FUNCTIONAL TESTS						
Power Gain at Minimum Noise Figure	Figure 6	G_{NFmin}				dB
(V_{CE} = 6 V, I_C = 5 mA, f = 500 MHz)	MRF524		9	—	—	
(V_{CE} = 6 V, I_C = 5 mA, f = 1 GHz)	MRF521/522/5211,L		10	11	—	
Noise Figure	Figure 6	NF_{min}				dB
(V_{CE} = 6 V, I_C = 5 mA, f = 500 MHz)	MRF524		—	—	2.5	
(V_{CE} = 6 V, I_C = 5 mA, f = 1 GHz)	MRF521/522/5211,L		—	2.8	3.5	

TYPICAL CHARACTERISTICS

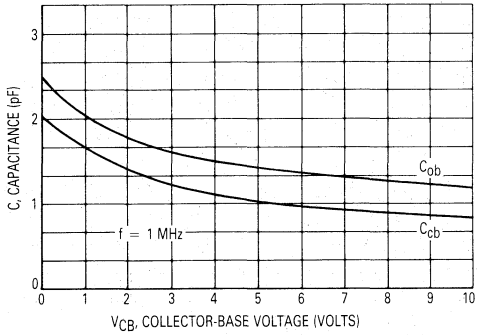


Figure 1. Junction Capacitance versus Voltage

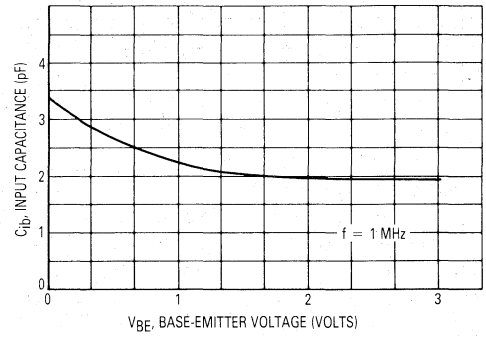


Figure 2. Input Capacitance versus Voltage

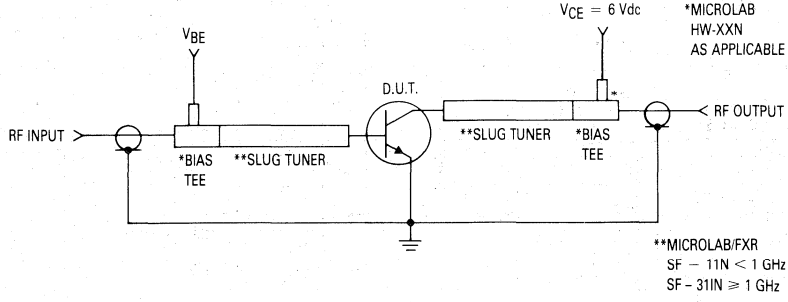


Figure 3. Functional Circuit Schematic

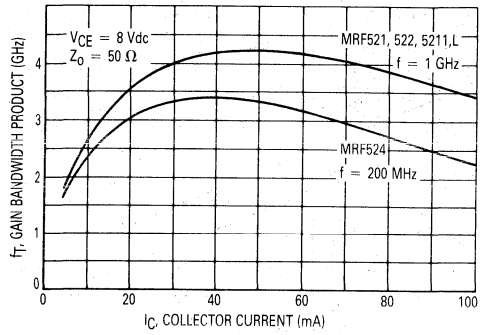


Figure 4. Gain-Bandwidth Product versus Current

GAIN AND NOISE FIGURE VERSUS FREQUENCY

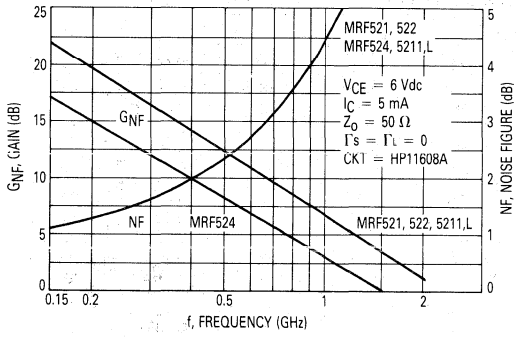


Figure 5. 50 Ohm System

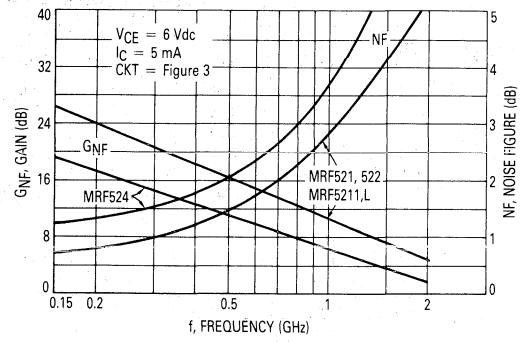


Figure 6. Tuned Circuit

GAIN AND NOISE FIGURE VERSUS CURRENT

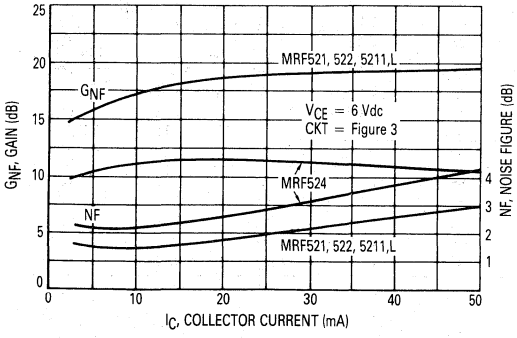


Figure 7. Tuned Circuit — Frequency 500 MHz

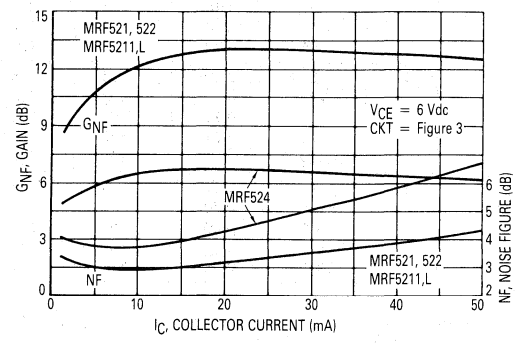


Figure 8. Tuned Circuit — Frequency 1 GHz

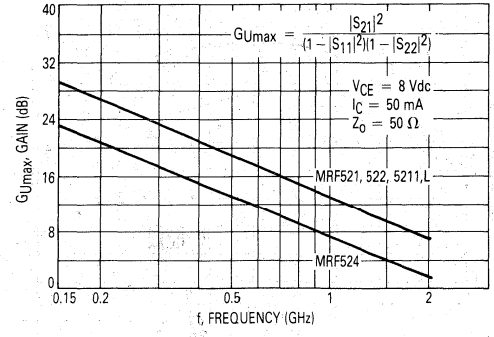


Figure 9. G_{Umax} versus Current

MRF521 COMMON EMITTER S-PARAMETERS

V_{CE} (Vdc)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
6	5	200	0.75	−116	7.6	117	0.06	36	0.59	−42
		500	0.75	−164	3.9	86	0.07	28	0.42	−51
		1000	0.74	165	2	63	0.08	37	0.37	−64
		1500	0.75	144	1.3	45	0.09	53	0.39	−85
		2000	0.74	124	1	32	0.14	61	0.43	−101
	10	200	0.71	−138	10.7	109	0.04	37	0.45	−54
		500	0.72	−175	4.7	82	0.06	40	0.29	−61
		1000	0.72	148	2.4	63	0.08	55	0.20	−73
		1500	0.72	140	1.6	47	0.11	63	0.28	−94
		2000	0.71	122	1.2	34	0.16	61	0.31	−108
	50	200	0.71	−172	12.9	100	0.02	59	0.26	−77
		500	0.72	170	5.3	78	0.05	68	0.15	−88
		1000	0.72	152	2.7	62	0.09	71	0.13	−99
		1500	0.72	136	1.8	46	0.13	70	0.17	−116
		2000	0.71	118	1.4	63	0.18	63	0.20	−123
8	5	200	0.77	−107	8.3	119	0.06	40	0.64	−38
		500	0.74	−163	4.1	88	0.07	28	0.45	−46
		1000	0.74	167	2.2	64	0.07	39	0.40	−58
		1500	0.74	146	1.4	47	0.08	54	0.42	−79
		2000	0.73	126	1.1	33	0.13	62	0.45	−95
	10	200	0.69	−133	11.5	111	0.04	39	0.49	−49
		500	0.71	−172	5.1	83	0.05	41	0.32	−55
		1000	0.71	161	2.6	64	0.07	56	0.28	−64
		1500	0.71	142	1.7	48	0.10	64	0.30	−85
		2000	0.70	123	1.3	34	0.15	63	0.33	−98
	50	200	0.67	−171	13.2	99	0.02	59	0.25	−70
		500	0.70	171	5.8	81	0.04	67	0.17	−74
		1000	0.69	151	2.9	62	0.08	72	0.15	−82
		1500	0.70	136	2	38	0.12	70	0.17	−100
		2000	0.68	117	1.5	33	0.17	63	0.20	−109

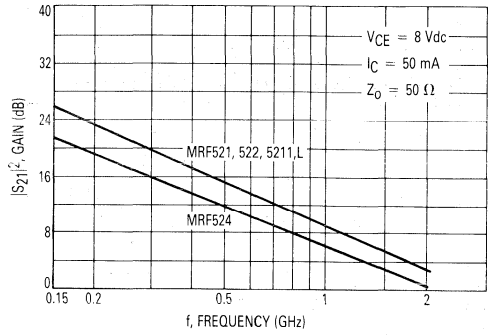


Figure 10. Insertion Gain versus Frequency

MRF522 COMMON EMITTER S-PARAMETERS

V_{CE} (Vdc)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
6	5	200	0.77	−113	7.5	120	0.06	34	0.60	−40
		500	0.80	−157	3.9	90	0.07	18	0.42	−51
		1000	0.83	177	2	70	0.07	14	0.36	−63
		1500	0.84	164	1.3	52	0.06	17	0.37	−88
		2000	0.88	153	1	39	0.06	27	0.41	−106
	10	200	0.77	−138	10.4	112	0.04	32	0.47	−56
		500	0.82	−168	4.9	88	0.05	25	0.28	−65
		1000	0.85	173	2.5	71	0.05	31	0.23	−77
		1500	0.86	163	1.7	56	0.06	39	0.26	−100
		2000	0.88	153	1.3	45	0.07	47	0.30	−112
	50	200	0.81	−169	13.2	104	0.02	43	0.30	−88
		500	0.84	177	5.8	85	0.03	53	0.17	−112
		1000	0.87	166	3	71	0.04	63	0.13	−130
		1500	0.87	158	2	57	0.06	65	0.19	−138
		2000	0.90	149	1.5	47	0.08	66	0.21	−142
8	5	200	0.80	−109	8	121	0.06	36	0.64	−39
		500	0.81	−153	4.1	92	0.07	20	0.43	−46
		1000	0.83	−179	2.1	72	0.07	15	0.38	−58
		1500	0.85	168	1.4	55	0.06	18	0.39	−80
		2000	0.87	157	1.1	43	0.06	28	0.42	−95
	10	200	0.76	−133	11.1	113	0.04	33	0.49	−52
		500	0.80	−167	5.3	89	0.05	25	0.28	−60
		1000	0.83	174	2.7	71	0.05	31	0.23	−69
		1500	0.85	163	1.8	57	0.06	38	0.27	−91
		2000	0.87	153	1.4	46	0.07	46	0.30	−105
	50	200	0.76	−160	14.4	105	0.02	44	0.30	−86
		500	0.80	178	6.4	85	0.03	52	0.16	−110
		1000	0.84	164	3.2	70	0.04	62	0.16	−125
		1500	0.85	154	2.1	55	0.06	64	0.16	−140
		2000	0.88	145	1.7	45	0.08	62	0.19	−141

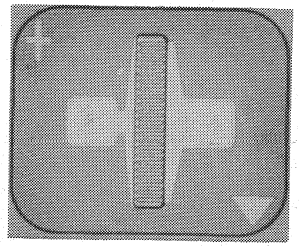
MRF524 COMMON EMITTER S-PARAMETERS

V_{CE} (Vdc)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
6	5	200	0.42	−98	5.8	109	0.07	57	0.65	−26
		400	0.29	−143	3.5	84	0.10	58	0.54	−29
		600	0.27	−175	2.5	71	0.13	60	0.50	−33
		800	0.27	166	2	60	0.17	61	0.47	−42
		1000	0.25	147	1.7	49	0.21	61	0.47	−49
	10	200	0.28	−111	7.3	100	0.06	64	0.54	−28
		400	0.21	−152	4.1	81	0.10	64	0.46	−28
		600	0.20	−179	2.9	69	0.14	63	0.41	−32
		800	0.20	167	2.3	59	0.19	61	0.39	−41
		1000	0.18	149	1.9	49	0.22	58	0.41	−47
	50	200	0.15	−136	8.1	92	0.06	73	0.42	−26
		400	0.13	−172	4.4	77	0.12	70	0.36	−25
		600	0.15	166	3.1	66	0.17	65	0.33	−28
		800	0.15	159	2.4	56	0.21	60	0.32	−38
		1000	0.13	143	2	47	0.25	55	0.32	−45
8	5	200	0.45	−93	6.1	109	0.06	57	0.67	−25
		400	0.30	−137	3.7	86	0.09	58	0.57	−27
		600	0.27	−167	2.6	72	0.12	60	0.51	−32
		800	0.26	174	2.1	61	0.15	60	0.49	−40
		1000	0.23	155	1.8	51	0.19	60	0.50	−47
	10	200	0.28	−100	7.5	101	0.06	65	0.57	−25
		400	0.18	−139	4.3	82	0.10	65	0.49	−26
		600	0.17	−171	3	70	0.13	64	0.45	−30
		800	0.16	174	2.3	60	0.18	61	0.43	−39
		1000	0.13	153	2	50	0.21	58	0.44	−45
	50	200	0.14	−107	8.3	94	0.06	72	0.47	−23
		400	0.10	−155	4.6	78	0.11	70	0.42	−23
		600	0.10	172	3.2	67	0.16	66	0.39	−26
		800	0.10	163	2.5	57	0.20	61	0.37	−36
		1000	0.09	144	2	47	0.24	57	0.37	−42

MRF5211,L COMMON EMITTER S-PARAMETERS

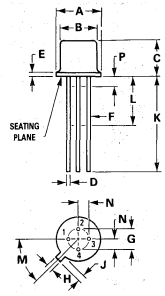
V_{CE} (Vdc)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
6	5	200	0.82	−114	7.9	118	0.07	35	0.59	−46
		500	0.81	−158	4	88	0.08	21	0.40	−54
		1000	0.79	175	2	67	0.08	21	0.37	−68
		1500	0.76	158	1.3	50	0.07	30	0.43	−82
		2000	0.74	143	1	38	0.08	47	0.47	−95
	10	200	0.78	−137	10.6	109	0.05	32	0.43	−63
		500	0.79	−168	4.9	84	0.06	28	0.26	−75
		1000	0.77	169	2.5	66	0.06	39	0.24	−87
		1500	0.74	155	1.6	50	0.08	49	0.29	−97
		2000	0.71	140	1.2	39	0.10	55	0.32	−106
	50	200	0.77	−167	13.1	99	0.02	45	0.26	−108
		500	0.77	176	5.7	80	0.04	57	0.18	−132
		1000	0.76	161	2.8	65	0.06	65	0.17	−142
		1500	0.73	149	1.9	51	0.08	67	0.19	−137
		2000	0.70	136	1.4	40	0.12	65	0.20	−137
8	5	200	0.82	−109	8.1	119	0.07	36	0.62	−43
		500	0.80	−154	4.2	90	0.08	22	0.42	−52
		1000	0.78	175	2.2	67	0.08	22	0.38	−65
		1500	0.75	159	1.4	50	0.07	31	0.43	−78
		2000	0.72	143	1	37	0.09	43	0.46	−89
	10	200	0.77	−132	11.2	110	0.05	33	0.45	−61
		500	0.77	−167	5.2	86	0.06	29	0.27	−70
		1000	0.76	169	2.6	67	0.06	39	0.25	−81
		1500	0.73	155	1.7	51	0.07	49	0.29	−90
		2000	0.70	140	1.3	39	0.10	54	0.31	−98
	50	200	0.75	−164	14.2	100	0.02	43	0.26	−101
		500	0.76	178	6.1	82	0.04	55	0.17	−121
		1000	0.75	163	3.1	67	0.06	64	0.15	−131
		1500	0.72	151	2	53	0.08	67	0.18	−126
		2000	0.70	139	1.5	42	0.11	68	0.19	−127

CHIP TOPOGRAPHY



Nominal Chip Size: 0.015″ x 0.016″ x 0.005″
Front Metallization: Gold
Back Metallization: Gold
Emitter Base Bond Pad: 2.2 x 2.2 mil
#Emitter Fingers: 22
#Base Fingers: 23
Emitter Diffusion: Ion-Implanted Arsenic

OUTLINE DIMENSIONS

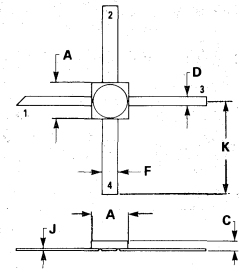


STYLE 10:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. CASE

NOTE: ALL RULES AND NOTES ASSOCIATED WITH TO-72 OUTLINE SHALL APPLY.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	—	0.76	—	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	—	0.500	—
L	6.35	—	0.250	—
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	—	1.27	—	0.050

CASE 20-03
TO-206 AF
(TO-72)

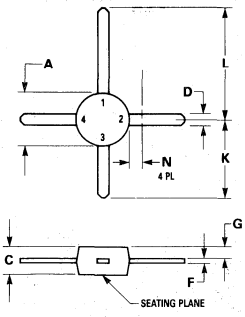


STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. BASE
4. EMITTER

NOTE:
1. DIMENSION K APPLIES TO ALL LEADS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.29	2.67	0.090	0.105
C	0.89	1.40	0.035	0.055
D	0.41	0.61	0.016	0.024
F	0.89	1.09	0.035	0.043
J	0.08	0.15	0.003	0.006
K	4.45	5.84	0.175	0.230

CASE 303-01

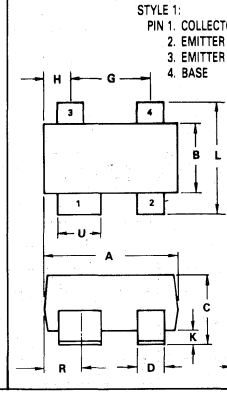


NOTE:
DIMENSION D NOT APPLICABLE IN ZONE N.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.44	5.21	0.175	0.205
C	1.90	2.54	0.075	0.100
D	0.84	0.99	0.033	0.039
F	0.20	0.30	0.008	0.012
G	0.76	1.14	0.030	0.045
K	7.24	8.13	0.285	0.320
L	10.54	11.43	0.415	0.450
N	—	1.65	—	0.065

STYLE 2:
PIN 1. COLLECTOR
2. EMITTER
3. BASE
4. EMITTER

CASE 317-01



STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. EMITTER
4. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.110	0.120
B	1.20	1.39	0.047	0.055
C	0.85	1.14	0.033	0.045
D	0.38	0.45	0.015	0.018
F	0.08	0.15	0.003	0.006
G	1.78	2.03	0.070	0.080
H	0.51	0.60	0.020	0.024
K	0.10	0.25	0.004	0.010
L	2.11	2.48	0.083	0.098
M	0.46	0.60	0.018	0.024
R	0.71	0.83	0.028	0.033
U	0.78	0.88	0.031	0.035
* K	0.013	0.102	0.0005	0.0040

***Low Profile** = Case 318A-02

CASE 318B-01
(SOT-143)

MRF525

The RF Line

100–500 MHz BROADBAND

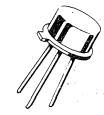
HIGH FREQUENCY TRANSISTOR

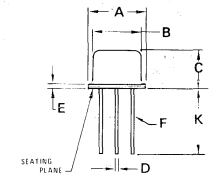
NPN SILICON

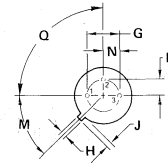
NPN SILICON HIGH FREQUENCY TRANSISTOR

. . . designed specifically for broadband linear amplifier stages in the 100–500 MHz frequency range.

- Guaranteed Performance at 225–400 MHz, 26 Vdc
  Minimum Gain = 13 dB
  Maximum NF = 4.0 dB
- Third Order Intercept +35 dBm (Typ)
- Common Emitter TO-39 Package
- S-Parameter Characterization







STYLE 5
PIN 1. COLLECTOR
PIN 2. BASE
PIN 3. EMITTER

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage (R_{BE} = 330 Ω)	V_{CER}	25	Vdc
Collector-Base Voltage	V_{CBO}	35	Vdc
Emitter-Base Voltage	V_{EBO}	3.5	Vdc
Collector Current — Continuous	I_C	150	mAdc
Total Power Dissipation @ T_A = 50°C Derate above 50°C	P_D	2.5 0.017	Watts W/°C
Operating Junction Temperature	T_J	+175	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	60	°C/W

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.02	9.30	0.355	0.366
B	8.00	8.51	0.315	0.335
C	4.19	4.57	0.165	0.180
D	0.43	0.53	0.017	0.021
E	0.43	0.89	0.017	0.035
F	0.41	0.48	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.71	0.86	0.028	0.034
J	0.74	1.02	0.029	0.040
K	12.70	–	0.500	–
M	45° NOM		45° NOM	
N	2.54 TYP		0.100 TYP	
Q	90° NOM		90° NOM	

NOTE: The pin configuration of this version of the TO-39 package differs from the common isolated emitter type.

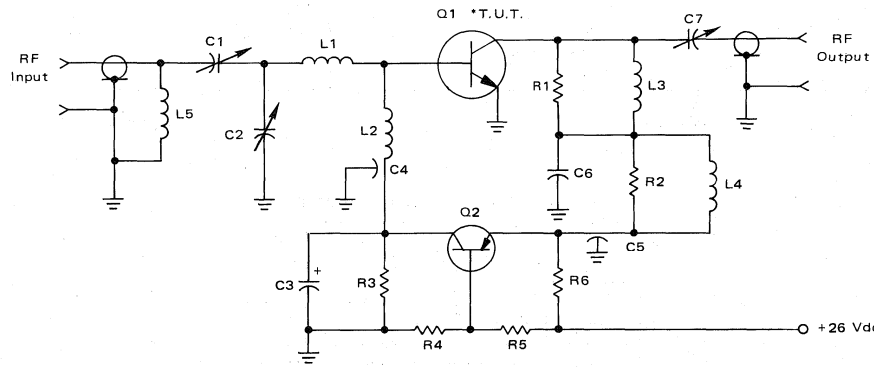
All JEDEC dimensions and notes apply.

CASE 79-03
TO-39

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, R_{BE} = 330 Ohms)	$V_{(BR)CER}$	25	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mA, I_E = 0)	$V_{(BR)CBO}$	35	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mA, I_C = 0)	$V_{(BR)EBO}$	3.5	–	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, I_B = 0)	I_{CEO}	–	–	100	μA
ON CHARACTERISTICS					
DC Current Gain (I_C = 80 mAdc, V_{CE} = 10 Vdc)	h_{FE}	60	–	175	–
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 50 mAdc, V_{CE} = 20 Vdc, f = 200 MHz)	f_T	2.2	2.5	–	GHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	3.0	4.0	pF
FUNCTIONAL TEST – BROADBAND (Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 26 Vdc, P_{in} = 0 dBm, f = 400 MHz)	G_{PE}	13	14	–	dB
Broadband Noise Figure (V_{CE} = 26 Vdc, f = 400 MHz)	NF	–	–	4.0	dB

FIGURE 1 – 225 to 400 MHz BROADBAND TEST CIRCUIT SCHEMATIC



C1, C2 – 2.5-11 pF Erie Ceramic Variable
C3 – 47 μF 6.0 Volt Electrolytic
C4, C5 – 1000 pF Feedthru
C6 – 470 pF Ceramic Chip
C7 – 5.5-18 pF Erie Ceramic Variable

R1 – 150 Ω 1/8 Watt Carbon
R2 – 100 Ω 1/8 Watt Carbon
R3, R4 – 10 kΩ 1/8 Watt Carbon
R5 – 3.3 kΩ 1/8 Watt Carbon
R6 – 120 Ω 1/2 Watt Carbon

L1 – 1 Turn #24, 0.125 mil ID
L2, L4 – 0.47 μH Molded Choke
L3 – 2 Turns #24, 0.125 mil ID
L5 – 4 Turns #24, 0.125 mil ID

Q2 – 2N2907A

*Transistor Under Test
I_E = 47 mAdc (Nominal)

FIGURE 2 – COMMON-EMITTER POWER GAIN (G_{max}) versus FREQUENCY

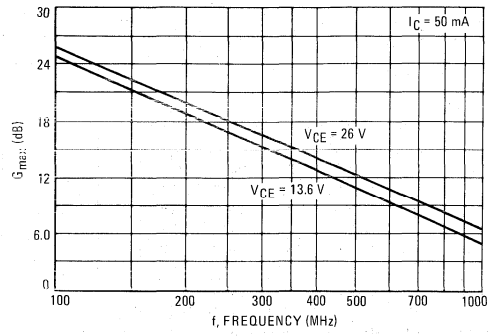


FIGURE 3 – CURRENT GAIN BANDWIDTH PRODUCT versus COLLECTOR CURRENT

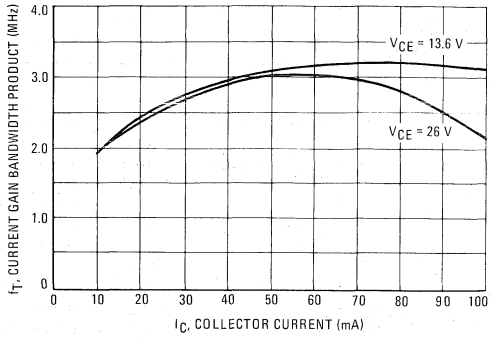


FIGURE 4 – BROADBAND AMPLIFIER RESPONSE

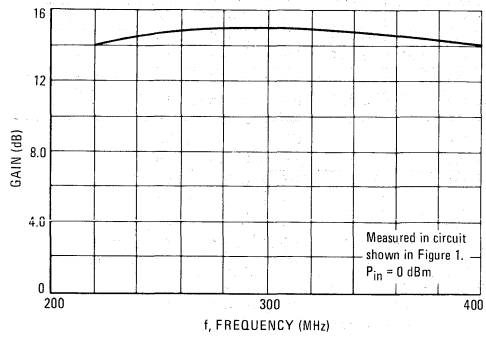


FIGURE 5 – 1.0 dB GAIN COMPRESSION OUTPUT versus FREQUENCY

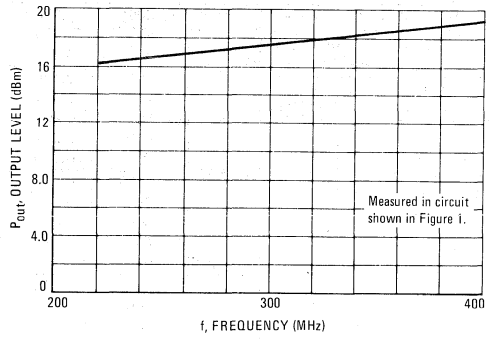
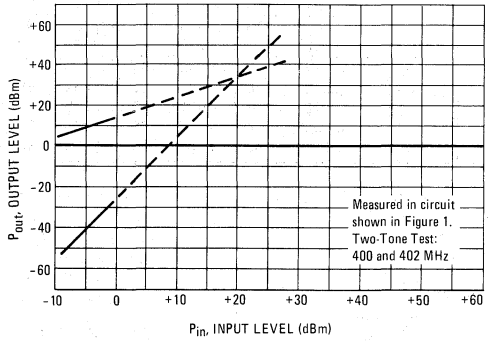


FIGURE 6 – THIRD ORDER INTERCEPT



S–PARAMETERS

V_{CE} (Volts)	I_C (mA)	Frequency (MHz)	S11		S21		S12		S22	
			|S11|	∠φ	|S21|	∠φ	|S12|	∠φ	|S22|	∠φ
13.6	10	100	0.388	-111	12.318	107	0.032	61	0.597	-24
		200	0.331	-151	6.768	88	0.049	68	0.480	-25
		300	0.337	-171	4.650	77	0.072	73	0.443	-31
		400	0.344	176	3.580	68	0.096	78	0.442	-40
		500	0.349	166	2.889	59	0.125	80	0.459	-47
	20	100	0.287	-125	14.160	103	0.030	67	0.516	-24
		200	0.263	-160	7.585	86	0.053	73	0.414	-23
		300	0.275	-177	5.167	76	0.078	76	0.378	-30
		400	0.288	172	3.968	68	0.104	77	0.378	-38
		500	0.293	164	3.214	60	0.135	78	0.396	-45
	50	100	0.206	-140	15.745	99	0.029	74	0.446	-24
		200	0.208	-171	8.299	84	0.056	76	0.358	-21
		300	0.226	176	5.612	75	0.084	76	0.324	-27
		400	0.235	169	4.307	68	0.113	77	0.326	-36
		500	0.243	161	3.488	60	0.114	76	0.345	-42
	100	100	0.179	-151	15.931	98	0.029	77	0.430	-22
		200	0.187	-177	8.293	85	0.058	80	0.358	-19
		300	0.203	171	5.626	77	0.087	80	0.330	-25
		400	0.212	164	4.276	70	0.115	80	0.338	-33
		500	0.213	157	3.456	63	0.147	79	0.364	-39
26	10	100	0.454	-100	13.580	105	0.027	58	0.625	-15
		200	0.313	-138	7.339	88	0.040	67	0.552	-17
		300	0.291	-161	4.989	78	0.060	76	0.532	-23
		400	0.287	-175	3.826	70	0.080	84	0.544	-30
		500	0.287	173	3.096	63	0.106	89	0.570	-36
	20	100	0.313	-105	15.191	102	0.025	62	0.566	-14
		200	0.220	-144	8.086	87	0.044	73	0.509	-15
		300	0.213	-166	5.487	77	0.067	78	0.489	-20
		400	0.215	-178	4.204	71	0.092	83	0.498	-28
		500	0.214	170	3.404	64	0.116	86	0.523	-34
	50	100	0.165	-117	16.375	102	0.026	71	0.529	-14
		200	0.139	-157	8.695	87	0.048	78	0.471	-14
		300	0.151	-176	5.882	78	0.073	80	0.449	-20
		400	0.157	173	4.494	71	0.098	82	0.458	-27
		500	0.158	164	3.659	65	0.124	84	0.485	-32
	100	100	0.215	-147	13.156	103	0.023	72	0.602	-14
		200	0.212	-176	7.220	88	0.044	82	0.536	-17
		300	0.222	171	4.951	79	0.069	84	0.507	-24
		400	0.230	164	3.851	72	0.093	87	0.513	-31
		500	0.233	156	3.123	64	0.123	89	0.534	-36

MRF531

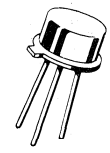
The RF Line

NPN SILICON HIGH FREQUENCY TRANSISTOR

. . . designed for high voltage and high current f_T switching applications. These devices are also ideal for CRT drivers.

- High Collector-Emitter Breakdown Voltage — BV_{CEO} = 100 Vdc (Min) @ I_C = 10 mAdc
- High Current-Gain — Bandwidth Product — f_T = 800 MHz (Typ) @ I_C = 50 mAdc
- Characterized with Safe Operating Area (SOA) Curves

HIGH FREQUENCY
TRANSISTOR
NPN SILICON



3

MAXIMUM RATINGS

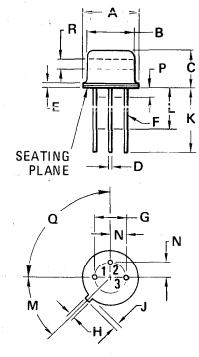
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	100	Vdc
Collector-Base Voltage	V_{CBO}	100	Vdc
Emitter-Base Voltage	V_{EBO}	3.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	2.5 14	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	25	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	$V_{(BR)CEO}$	100	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	100	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	–	–	Vdc
Collector Cutoff Current (V_{CE} = 75 Vdc, V_{BE} = 0)	I_{CES}	–	–	10	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 mAdc, V_{CE} = 10 Vdc)	h_{FE}	25	–	–	–
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{CE(sat)}$	–	–	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 50 mAdc, V_{CE} = 25 Vdc, f = 100 MHz)	f_T	500	800	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	–	4.0	pF
Input Capacitance (V_{BE} = 3.0 Vdc, I_C = 0, f = 1.0 MHz)	C_{ib}	–	9.0	–	pF



STYLE 1
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO-39

FIGURE 1 – CURRENT-GAIN – BANDWIDTH PRODUCT

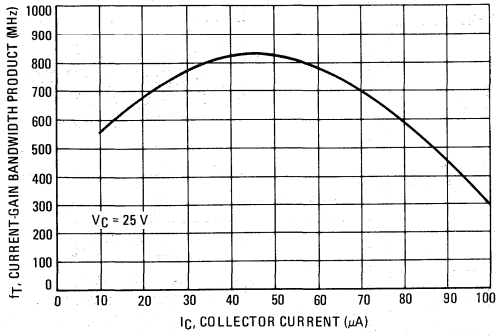


FIGURE 2 – INPUT CAPACITANCE

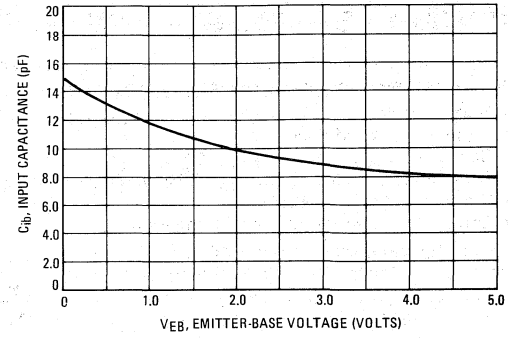


FIGURE 3 – OUTPUT CAPACITANCE

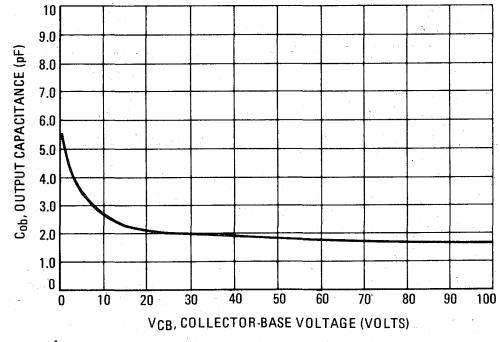
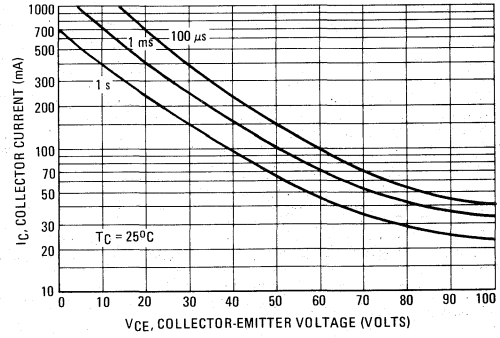


FIGURE 4 – DC SAFE OPERATING AREA



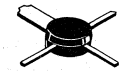
MRF542
MRF548

The RF Line
NPN Silicon
High Frequency Transistors

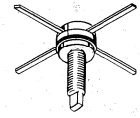
. . . designed primarily for high frequency common base amplifiers used in medium and high resolution color video display monitors.

- High Collector-Base Breakdown Voltage $V_{(BR)CBO}$ = 120 V (Min)
- Stripline Opposed Base Construction
- Common Base Insertion Gain = 5.5 dB (Typ)
- Package Options for Low Cost (MRF542), High Power Dissipation (MRF548)
- **Die Source Same as MRF544**
- Emitter Ballasted for Improved Ruggedness

HIGH FREQUENCY TRANSISTORS NPN SILICON



MRF542
CASE 317D-01
PLASTIC



MRF548
CASE 244A-01
(TO-117)
CERAMIC

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector-Emitter Voltage		V_{CEO}	70	Vdc
Collector-Base Voltage		V_{CBO}	120	Vdc
Emitter-Base Voltage		V_{EBO}	3	Vdc
Collector-Current — Continuous		I_C	400	mAdc
Operating Junction Temperature	MRF542 MRF548	T_J	150 200	°C °C
Total Device Dissipation @ T_C = 75°C (1,2)	MRF542 MRF548	P_D	3 5	Watts
Derate above 75°C	MRF542/548		40	mW/°C
Storage Temperature Range		T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	25	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1 mAdc, I_B = 0)	$V_{(BR)CEO}$	70	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	120	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	3	—	—	Vdc
Collector Cutoff Current (V_{CE} = 80 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	100	μAdc
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	—	—	20	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	15	—	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)	C_{ob}	—	2.9	—	pF
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)	C_{cb}	—	2	2.5	pF
Input Capacitance (V_{EB} = 3 Vdc, f = 1 MHz)	C_{ib}	—	12.5	—	pF
FUNCTIONAL TESTS					
Common Base Gain (V_{CB} = 10 V, I_C = 100 mA, f = 250 MHz)	$\|S_{21}\|^2$	4.5	5.5	—	dB

(1) T_C, Case temperature measured on collector lead immediately adjacent to body of package.
(2) The MRF542 PowerMacro must be properly mounted for reliable operation. AN938, "Mounting Techniques in PowerMacro Transistor," discusses methods of mounting and heatsinking.

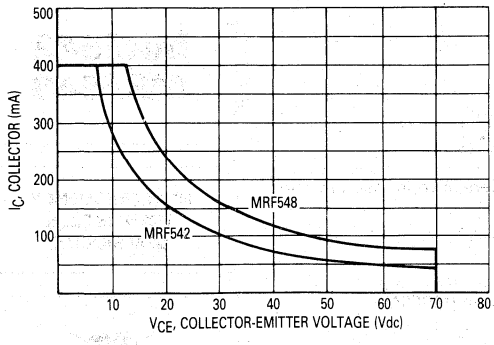


Figure 1. Safe Operating Area

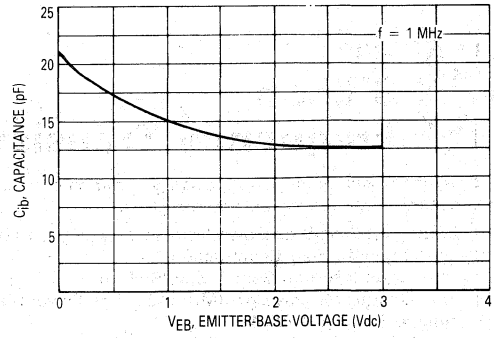


Figure 2. Input Capacitance versus Voltage

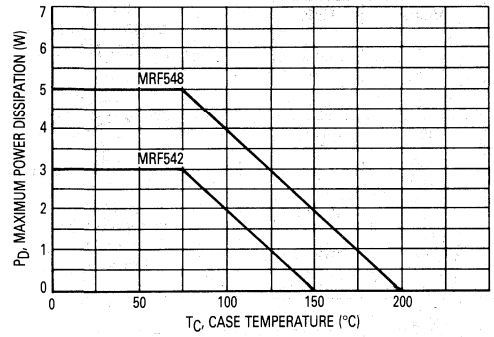


Figure 3. Power Dissipation versus Temperature

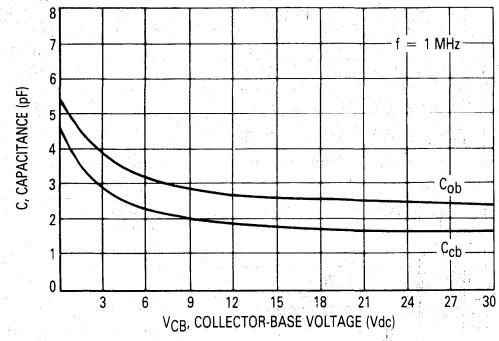
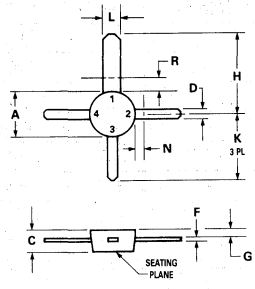


Figure 4. Junction Capacitance versus Voltage

OUTLINE DIMENSIONS

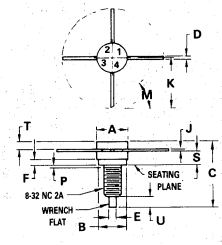


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.44	5.21	0.175	0.205
C	1.90	2.54	0.075	0.100
D	0.84	0.99	0.033	0.039
F	0.20	0.30	0.008	0.012
G	0.63	1.01	0.025	0.040
H	8.84	9.72	0.348	0.383
K	7.24	8.13	0.285	0.320
L	2.46	2.64	0.097	0.104
N	—	1.65	—	0.065
R	—	3.25	—	0.128

STYLE 3:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. BASE

NOTE:
DIMENSION D NOT APPLICABLE IN ZONES N AND R.

CASE 317D-01
PLASTIC



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.06	7.26	0.278	0.286
B	6.20	6.50	0.244	0.256
C	15.24	16.51	0.600	0.650
D	0.66	0.86	0.026	0.034
E	1.40	1.65	0.055	0.065
F	1.52	—	0.060	—
J	0.10	0.15	0.004	0.006
K	11.17	—	0.440	—
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
S	2.74	3.35	0.108	0.132
T	1.40	1.78	0.055	0.070
U	2.92	3.68	0.115	0.145

STYLE 3:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR

CASE 244A-01
CERAMIC
(TO-117)

MRF543
MRF549

The RF Line
PNP Silicon
High Frequency Transistors

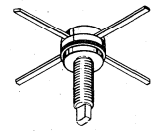
. . . designed primarily for high frequency common base amplifiers used in medium and high resolution color video display monitors.

- High Collector-Base Breakdown Voltage $V_{(BR)CBO}$ = 100 V (Min)
- Stripline Opposed Base Construction
- Common Base Insertion Gain = 5.5 dB (Typ)
- Package Options for Low Cost (MRF543), High Power Dissipation (MRF549)
- **Die Source Same As MRF545**
- Emitter Ballasted for Improved Ruggedness

HIGH FREQUENCY TRANSISTORS PNP SILICON



MRF543
CASE 317D-01
PLASTIC



MRF549
CASE 244A-01
(TO-117)
CERAMIC

MAXIMUM RATINGS (Note 1)

Rating		Symbol	Value	Unit
Collector-Emitter Voltage		V_{CEO}	70	Vdc
Collector-Base Voltage		V_{CBO}	100	Vdc
Emitter-Base Voltage		V_{EBO}	3	Vdc
Collector-Current — Continuous		I_C	400	mAdc
Operating Junction Temperature	MRF543 MRF549	T_J	150 200	°C °C
Total Device Dissipation @ T_C = 75°C (2,3)	MRF543 MRF549	P_D	3 5	Watts
Derate above 75°C	MRF543/549		40	mW/°C
Storage Temperature Range		T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	25	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted. Note 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1 mAdc, I_B = 0)	$V_{(BR)CEO}$	70	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	100	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	3	—	—	Vdc
Collector Cutoff Current (V_{CE} = 80 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	100	μAdc
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	—	—	20	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	15	—	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)	C_{ob}	—	2.8	—	pF
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)	C_{cb}	—	2	2.5	pF
Input Capacitance (V_{EB} = 3 Vdc, f = 1 MHz)	C_{ib}	—	10.5	—	pF
FUNCTIONAL TESTS					
Common Base Gain (V_{CB} = 10 V, I_C = 100 mA, f = 250 MHz)	$\|S_{21}\|^2$	4.5	5.5	—	dB

Notes 1. Voltages and currents for PNP transistors are given for magnitude information only. Polarity is assumed to be opposite that of an NPN transistor.
2. T_C, Case temperature for MRF543 measured on collector lead immediately adjacent to body of package.
3. The MRF543 PowerMacro must be properly mounted for reliable operation. AN938, "Mounting Techniques in PowerMacro Transistor," discusses methods of mounting and heatsinking.

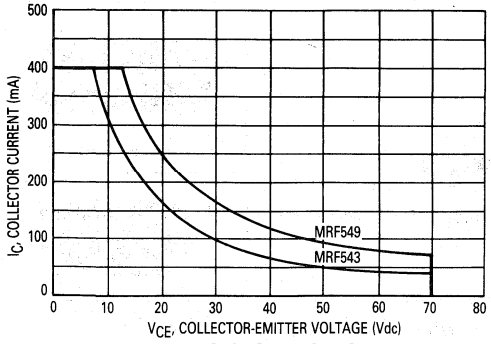


Figure 1. Safe Operating Area

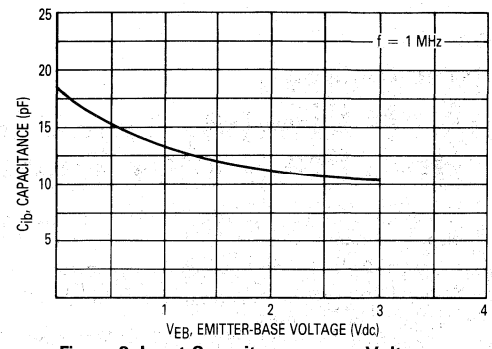


Figure 2. Input Capacitance versus Voltage

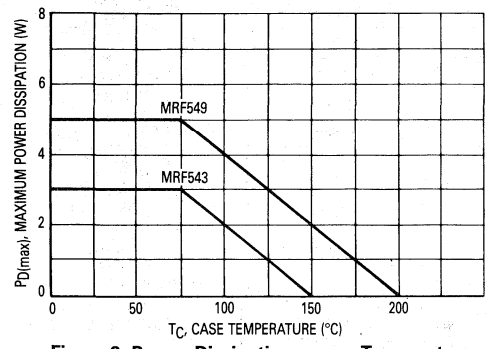


Figure 3. Power Dissipation versus Temperature

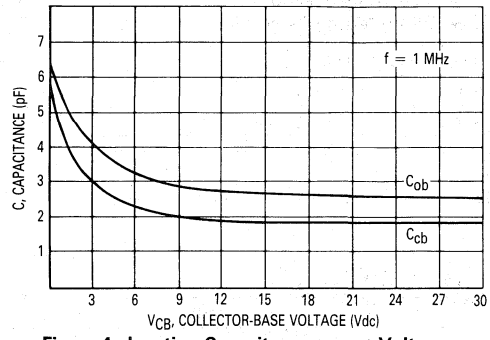
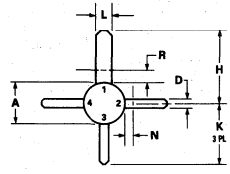


Figure 4. Junction Capacitance versus Voltage

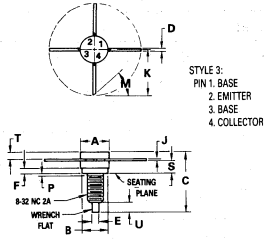
OUTLINE DIMENSIONS



CASE 317D-01
PLASTIC

STYLE 3:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.44	5.21	0.175	0.205
C	1.90	2.54	0.075	0.100
D	0.84	0.99	0.033	0.039
F	0.20	0.30	0.008	0.012
G	0.63	1.01	0.025	0.040
H	8.84	9.72	0.348	0.383
K	7.24	8.13	0.285	0.320
L	2.46	2.64	0.097	0.104
N	—	1.65	—	0.065
R	—	3.25	—	0.128



STYLE 3:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR

CASE 244A-01
CERAMIC
(TO-117)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.06	7.26	0.278	0.286
B	6.20	6.50	0.244	0.256
C	15.24	16.51	0.600	0.650
D	0.66	0.86	0.026	0.034
E	1.40	1.65	0.055	0.065
F	1.52	—	0.060	—
J	0.10	0.15	0.004	0.006
K	11.17	—	0.440	—
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
S	2.74	3.35	0.108	0.132
T	1.40	1.78	0.055	0.070
U	2.92	3.68	0.115	0.145

MRF544
MRFC544

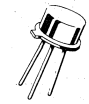
The RF Line

NPN Silicon High Frequency Transistors

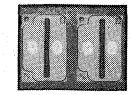
. . . designed for high-frequency and medium and high resolution color video display monitors.

- Emitter Ballasting for Improved Ruggedness
- High Power Gain — $G_{U(max)}$ = 16.5 dB (Typ) @ f = 500 MHz
- Ion Implanted
- High Collector Base Breakdown Voltage — $V_{(BR)CBO}$, 120 V (Min)
- High f_T — 1400 MHz
- State-of-the-Art Technology Fine Line Geometry
- Gold Top Metallization
- Silicon Nitride Passivation

f_T = 1400 MHz (Typ)
@ 50 mA
HIGH FREQUENCY TRANSISTORS



MRF544
CASE 79-02
TO-205AD
(TO-39)



CHIP
MRFC544

3

MAXIMUM RATINGS

Rating	Symbol	MRFC544	MRF544	Unit
Collector-Emitter Voltage	V_{CEO}	70	70	Vdc
Collector-Base Voltage	V_{CBO}	120	120	Vdc
Emitter-Base Voltage	V_{EBO}	3	3	Vdc
Collector-Current — Continuous	I_C	400	400	mAdc
Total Device Dissipation @ T_C = 75°C Derate above 75°C	P_D	5 T_{Jmax} = 200°C	3.5 28	Watts mW/°C
Storage Temperature Range	T_{stg}	−65 to +200	−65 to +200	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1 mAdc, I_B = 0)	$V_{(BR)CEO}$	70	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	$V_{(BR)CBO}$	120	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	$V_{(BR)EBO}$	3	—	—	Vdc
Collector Cutoff Current (V_{CE} = 80 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	100	μAdc
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	—	—	20	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 50 mA, V_{CE} = 5 Vdc)	h_{FE}	15	—	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)	C_{ob}	—	3	—	pF
Junction Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)	C_{cb}	—	1.8	2.5	pF
Input Capacitance (V_{EB} = 3 Vdc, I_C = 0, f = 1 MHz)	C_{ib}	—	9	—	pF
Current Gain-Bandwidth Product (I_C = 50 mA, V_{CE} = 10 V, f = 250 MHz)	f_T	1000	1400	—	MHz
FUNCTIONAL TESTS					
Maximum Available Gain (I_C = 50 mA, V_{CE} = 10 V, f = 250 MHz)	G_{max}	—	16.5	—	dB
Insertion Gain (I_C = 50 mA, V_{CE} = 10 V, f = 250 MHz)	$\|S_{21}\|^2$	—	13	—	dB

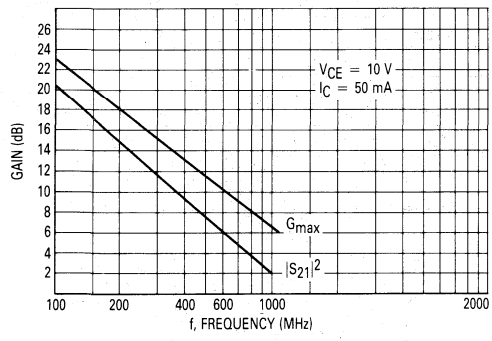


Figure 1. Power Gain versus Frequency

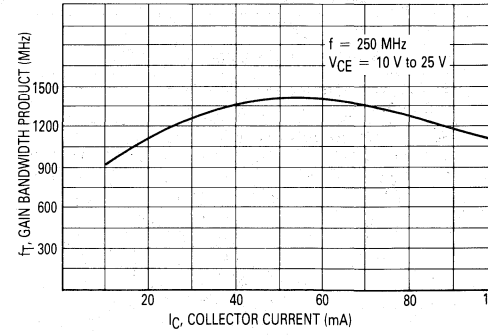


Figure 2. Gain-Bandwidth Product versus Collector Current

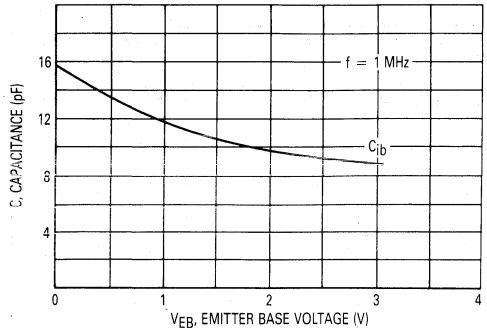


Figure 3. C_{ib} Input Capacitance versus Voltage

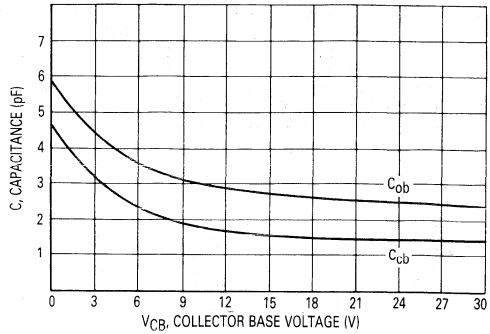


Figure 4. Junction Capacitance versus Voltage

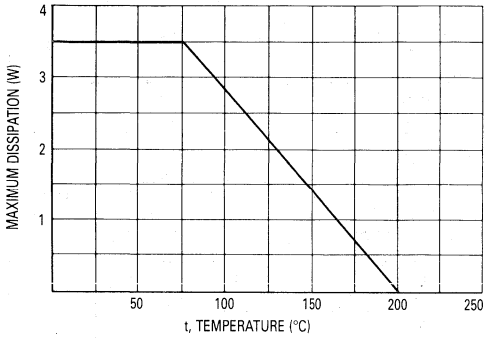


Figure 5. Dissipation versus Temperature

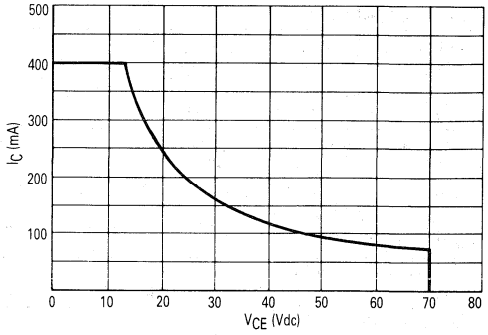


Figure 6. Safe Operating Area

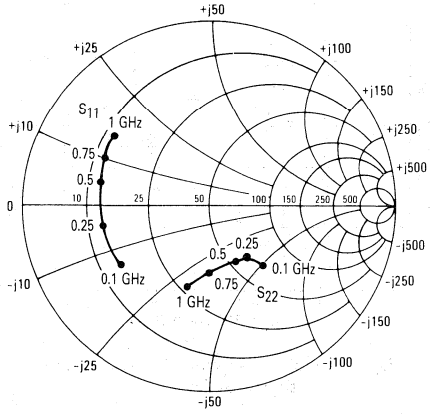


Figure 7. Input/Output Reflection Coefficient versus Frequency (GHz)
V_{CE} = 10 V I_C = 50 mA

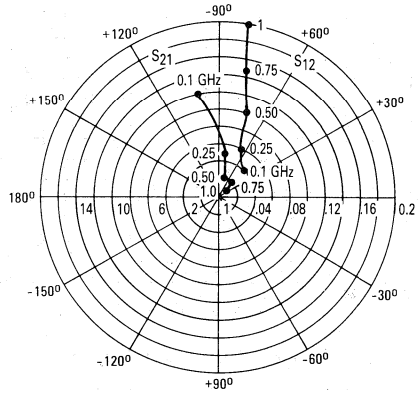


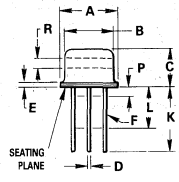
Figure 8. Forward/Reverse Transmission Coefficients versus Frequency (GHz)
V_{CE} = 10 V I_C = 50 mA

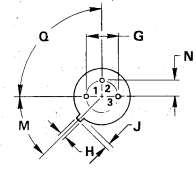
COMMON EMITTER S-PARAMETERS

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
10	25	100	0.59	−138	11.71	106	0.04	50	0.48	−43
		250	0.59	−167	4.64	85	0.06	61	0.38	−50
		500	0.61	174	2.30	67	0.10	75	0.37	−66
		750	0.66	166	1.52	53	0.15	80	0.42	−89
		1000	0.66	157	1.17	43	0.20	82	0.50	−104
	50	100	0.58	−147	12.38	102	0.04	50	0.43	−48
		250	0.58	−171	4.85	83	0.06	63	0.34	−52
		500	0.60	170	2.43	66	0.10	74	0.33	−67
		750	0.64	163	1.61	52	0.15	78	0.39	−91
		1000	0.64	155	1.24	43	0.21	79	0.46	−105
	80	100	0.60	−151	12.15	101	0.03	49	0.39	−47
		250	0.60	−173	4.76	81	0.05	64	0.34	−55
		500	0.62	170	2.35	65	0.10	74	0.35	−72
		750	0.66	162	1.53	50	0.14	78	0.43	−96
		1000	0.65	154	1.16	40	0.20	78	0.51	−108
25	25	100	0.59	−133	12.77	110	0.03	44	0.53	−34
		250	0.59	−164	5.06	86	0.05	62	0.46	−42
		500	0.60	177	2.48	67	0.08	78	0.45	−60
		750	0.64	168	1.59	52	0.12	84	0.50	−83
		1000	0.66	159	1.20	43	0.17	87	0.57	−99
	50	100	0.56	−142	13.25	103	0.03	49	0.50	−35
		250	0.56	−169	5.21	82	0.05	64	0.44	−42
		500	0.58	172	2.60	64	0.09	76	0.43	−59
		750	0.62	163	1.68	50	0.13	82	0.48	−82
		1000	0.63	155	1.28	40	0.18	83	0.55	−97
	80	100	0.58	−143	13.87	102	0.03	52	0.54	−33
		250	0.57	−172	5.19	80	0.05	63	0.47	−39
		500	0.59	170	2.55	62	0.08	77	0.46	−58
		750	0.64	162	1.65	48	0.13	82	0.50	−81
		1000	0.64	154	1.24	37	0.18	83	0.57	−97

OUTLINE DIMENSIONS

TO-39
CASE 79-02





STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

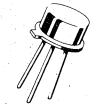
DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	—	0.500	—
L	6.35	—	0.250	—
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
Q	90° NOM		90° NOM	
R	2.54	—	0.100	—

All JEDEC Dimensions and Notes Apply.

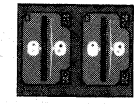
3

MRF545
MRFC545

f_T = 1250 MHz (TYP.)
@ 50 mA
HIGH FREQUENCY
TRANSISTORS
PNP SILICON



MRF545
CASE 79-02
TO-205AD
(TO-39)



CHIP
MRFC545

The RF Line

PNP Silicon
High Frequency Transistors

. . . designed for high-frequency and medium and high resolution color video display monitors.

- Emitter Ballasting for Improved Ruggedness
- High Power Gain — $G_{U(max)}$ = 15.5 dB (Typ) @ f = 250 MHz
- Ion Implanted
- High Collector Base Breakdown Voltage — $V_{(BR)CBO}$, 100 V (Min)
- High f_T — 1250 MHz (Typ)
- State-of-the-Art Technology
  - Fine Line Geometry
  - Gold Top Metallization
  - Silicon Nitride Passivation

3

MAXIMUM RATINGS (Note 1)

Rating	Symbol	MRFC545	MRF545	Unit
Collector-Emitter Voltage	V_{CEO}	70	70	Vdc
Collector-Base Voltage	V_{CBO}	100	100	Vdc
Emitter-Base Voltage	V_{EBO}	3	3	Vdc
Collector-Current — Continuous	I_C	400	400	mAdc
Operating Junction Temperature	T_J	200	200	°C
Total Device Dissipation @ T_C = 75°C Derate above 75°C	P_D	5 T_{Jmax} = 200°C	3.5 28	Watts mW/°C
Storage Temperature Range	T_{stg}	−65 to +200	−65 to +200	°C

Note 1. Voltages and currents for PNP transistors are given for magnitude information only. Polarity is assumed to be opposite that of an NPN transistor.

ELECTRICAL CHARACTERISTICS (Note 1, T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1 mAdc, I_B = 0)	$V_{(BR)CEO}$	70	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	100	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	3	—	—	Vdc
Collector Cutoff Current (V_{CE} = 80 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	100	μAdc
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	—	—	20	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	15	—	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)	C_{ob}	—	3.2	—	pF
Junction Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)	C_{cb}	—	2	2.5	pF
Input Capacitance (V_{EB} = 3 Vdc, I_C = 0, f = 1 MHz)	C_{ib}	—	10	—	pF
Current Gain-Bandwidth Product (I_C = 50 mA, V_{CE} = 25 V, f = 250 MHz)	f_T	1000	1250	—	MHz
FUNCTIONAL TESTS					
Maximum Available Gain (I_C = 50 mA, V_{CE} = 25 V, f = 250 MHz)	G_{max}	—	15.5	—	dB
Insertion Gain (I_C = 50 mA, V_{CE} = 25 V, f = 250 MHz)	$\|S_{21}\|^2$	—	12.7	—	dB

Note 1. Voltages and currents for PNP transistors are given for magnitude information only. Polarity is assumed to be opposite that of an NPN transistor.

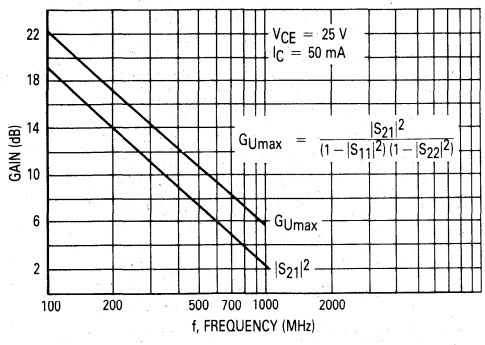


Figure 1. Power Gain versus Frequency

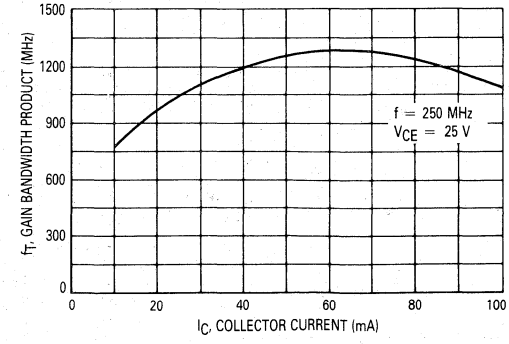


Figure 2. Gain-Bandwidth Product versus Collector Current

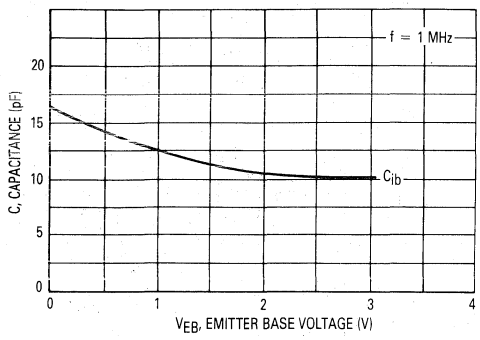


Figure 3. Input Capacitance versus Voltage

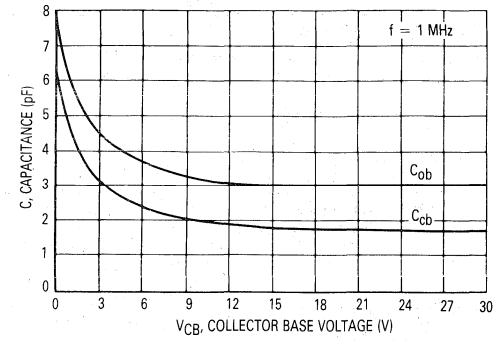


Figure 4. Junction Capacitance versus Voltage

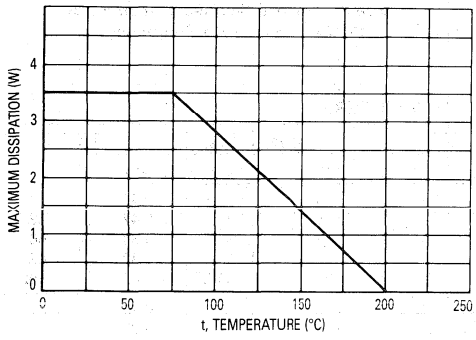


Figure 5. Dissipation versus Temperature

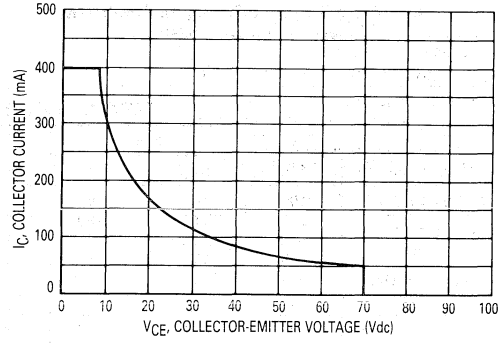
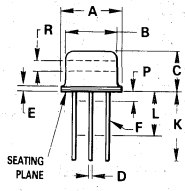
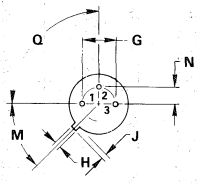


Figure 6. Safe Operating Area

OUTLINE DIMENSIONS





STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

CASE 79-02
TO-205AD
(TO-39)

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	—	0.500	—
L	6.35	—	0.250	—
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
Q	90° NOM		90° NOM	
R	2.54	—	0.100	—

All JEDEC Dimensions and Notes Apply.

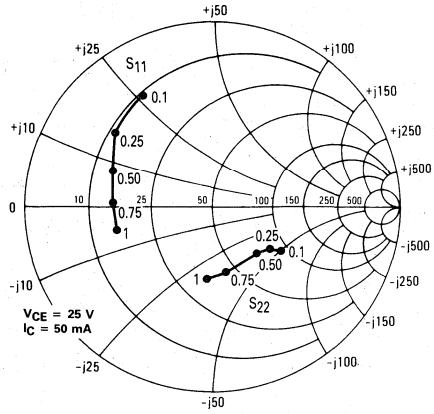


Figure 7. Input/Output Reflection Coefficient versus Frequency (GHz)

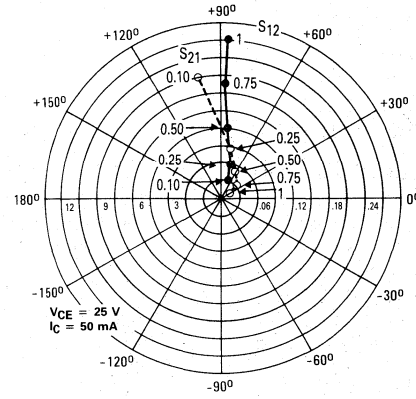


Figure 8. Forward/Reverse Transmission Coefficients versus Frequency

COMMON EMITTER S-PARAMETERS

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
10	25	100	0.60	−161	8.7	101	0.03	57	0.47	−34
		250	0.61	−180	3.6	81	0.06	74	0.42	−39
		500	0.66	163	1.9	62	0.12	88	0.38	−56
		750	0.72	154	1.3	50	0.19	91	0.40	−87
		1000	0.75	143	1.0	41	0.29	89	0.46	−102
	50	100	0.61	−169	8.8	99	0.03	64	0.43	−36
		250	0.62	177	3.7	80	0.06	79	0.38	−40
		500	0.66	161	1.9	63	0.13	88	0.35	−56
		750	0.72	153	1.3	50	0.20	89	0.36	−86
		1000	0.74	142	1.0	41	0.29	87	0.42	−102
	100	100	0.67	−178	5.6	94	0.03	68	0.40	−26
		250	0.70	170	2.3	74	0.07	81	0.36	−37
		500	0.71	155	1.2	54	0.16	89	0.39	−61
		750	0.76	142	0.9	42	0.27	87	0.40	−92
		1000	0.82	128	0.7	37	0.39	81	0.43	−117
25	25	100	0.55	−155	9.9	102	0.03	58	0.49	−32
		250	0.57	−176	4.2	82	0.06	72	0.43	−36
		500	0.61	165	2.1	64	0.11	87	0.38	−50
		750	0.68	156	1.4	51	0.18	90	0.41	−79
		1000	0.70	144	1.1	43	0.27	89	0.45	−96
	50	100	0.53	−162	10.6	101	0.03	62	0.44	−35
		250	0.55	−180	4.4	82	0.06	75	0.39	−38
		500	0.59	162	2.3	65	0.12	85	0.34	−50
		750	0.65	154	1.5	51	0.19	88	0.36	−78
		1000	0.67	143	1.2	43	0.27	86	0.40	−95
	100	100	0.48	−169	9.3	98	0.03	68	0.43	−27
		250	0.53	174	3.9	79	0.07	79	0.37	−33
		500	0.54	159	2.1	61	0.15	85	0.40	−52
		750	0.60	146	1.5	47	0.24	85	0.39	−77
		1000	0.65	132	1.1	37	0.34	81	0.41	−99

MRF546

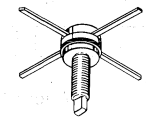
HIGH FREQUENCY
TRANSISTOR
NPN SILICON

The RF Line

NPN Silicon
High Frequency Transistor

. . . designed for high current, high frequency common base amplifiers used in medium and high resolution color video display monitors.

- Stripline Opposed Base Construction
- **Die Source 2X Common Base MRF548**
- Common Base Insertion Gain = 6 dB (Typ)
- High Collector-Base Breakdown Voltage $V_{(BR)CBO}$ = 120 Vdc (Min)
- Emitter Ballasted For Improved Ruggedness
- Gold Top Metallization
- Silicon Nitride Passivation



CASE 244A-01

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	70	Vdc
Collector-Base Voltage	V_{CBO}	120	Vdc
Emitter-Base Voltage	V_{EBO}	3	Vdc
Collector-Current — Continuous	I_C	600	mAdc
Operating Junction Temperature	T_J	200	°C
Total Device Dissipation @ T_C = 75°C Derate above 75°C	P_D	9 72	Watts mW/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	13.9	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 2 mAdc, I_B = 0)	$V_{(BR)CEO}$	70	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 0.2 mAdc, I_E = 0)	$V_{(BR)CBO}$	120	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.2 mAdc, I_C = 0)	$V_{(BR)EBO}$	3	—	—	Vdc
Collector Cutoff Current (V_{CE} = 80 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	200	μAdc
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	—	—	40	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 10 Vdc)	h_{FE}	15	—	200	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)	C_{ob}	—	5	—	pF
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)	C_{cb}	—	3.6	4.5	pF
Input Capacitance (V_{EB} = 3 Vdc, f = 1 MHz)	C_{ib}	—	26	—	pF
FUNCTIONAL TESTS					
Common Base Gain (V_{CB} = 10 V, I_C = 200 mA, f = 250 MHz)	$\|S_{21}\|^2$	4.5	6	—	dB

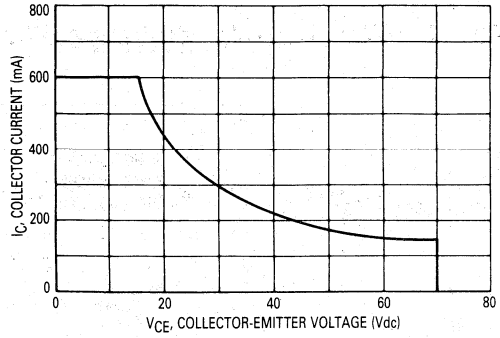


Figure 1. Safe Operating Area

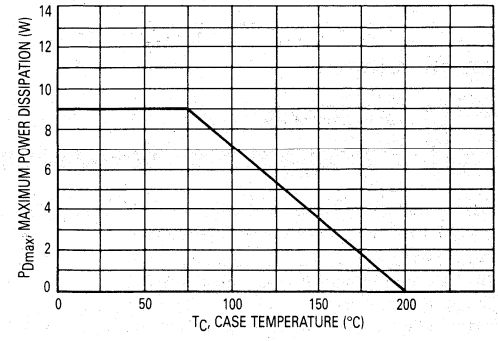


Figure 2. Power Dissipation versus Temperature

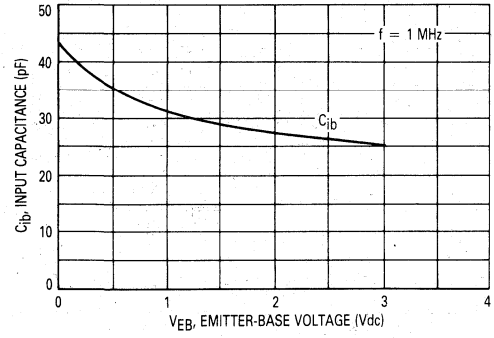


Figure 3. Input Capacitance versus Voltage

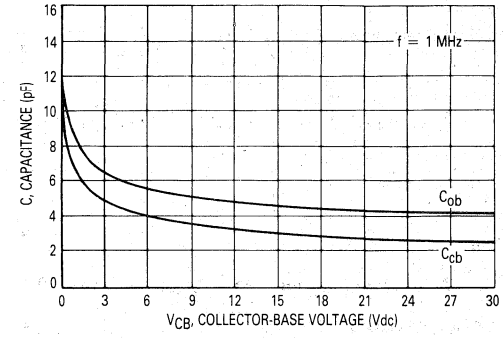
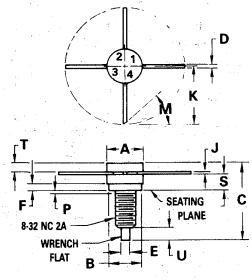


Figure 4. Junction Capacitance versus Voltage

OUTLINE DIMENSIONS



STYLE 3:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR

CASE 244A-01

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.06	7.26	0.278	0.286
B	6.20	6.50	0.244	0.256
C	15.24	16.51	0.600	0.650
D	0.66	0.86	0.026	0.034
E	1.40	1.65	0.055	0.065
F	1.52	—	0.060	—
J	0.10	0.15	0.004	0.006
K	11.17	—	0.440	—
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
S	2.74	3.35	0.108	0.132
T	1.40	1.78	0.055	0.070
U	2.92	3.68	0.115	0.145

MRF547

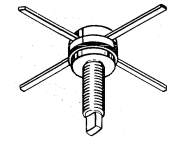
HIGH FREQUENCY
TRANSISTOR
PNP SILICON

The RF Line

PNP Silicon
High Frequency Transistor

. . . designed for high-current, high-frequency common base amplifiers used in medium and high resolution color video display monitors.

- Stripline Opposed Base Construction
- **Die Source 2X Common Base MRF549**
- Common Base Insertion Gain = 5.5 dB (Typ)
- High Collector-Base Breakdown Voltage $V_{(BR)CBO}$ = 100 Vdc (Min)
- Emitter Ballasted For Improved Ruggedness
- Gold Top Metallization
- Silicon Nitride Passivation



CASE 244A-01

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	70	Vdc
Collector-Base Voltage	V_{CBO}	100	Vdc
Emitter-Base Voltage	V_{EBO}	3	Vdc
Collector Current — Continuous	I_C	600	mAdc
Operating Junction Temperature	T_J	200	°C
Total Device Dissipation @ T_C = 75°C Derate above 75°C	P_D	9 72	Watts mW/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	13.9	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted. Note 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 2 mAdc, I_B = 0)	$V_{(BR)CEO}$	70	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 0.2 mAdc, I_E = 0)	$V_{(BR)CBO}$	100	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.2 mAdc, I_C = 0)	$V_{(BR)EBO}$	3	—	—	Vdc
Collector Cutoff Current (V_{CE} = 80 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	200	μAdc
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	—	—	40	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 10 Vdc)	h_{FE}	15	—	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)	C_{ob}	—	5.1	—	pF
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)	C_{cb}	—	3.6	4.5	pF
Input Capacitance (V_{EB} = 3 Vdc, f = 1 MHz)	C_{ib}	—	20	—	pF
FUNCTIONAL TESTS					
Common Base Gain (V_{CB} = 10 V, I_C = 200 mA, f = 250 MHz)	$\|S_{21}\|^2$	4.5	5.5	—	dB

Note 1. Voltages and currents for PNP transistors are given for magnitude information only. Polarity is assumed to be opposite that of an NPN transistor.

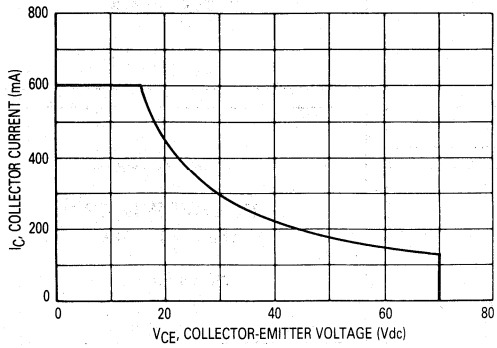


Figure 1. Safe Operating Area

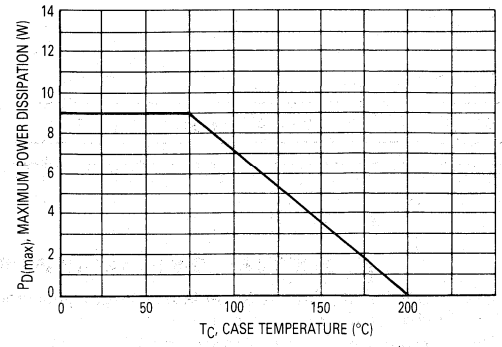


Figure 2. Power Dissipation versus Temperature

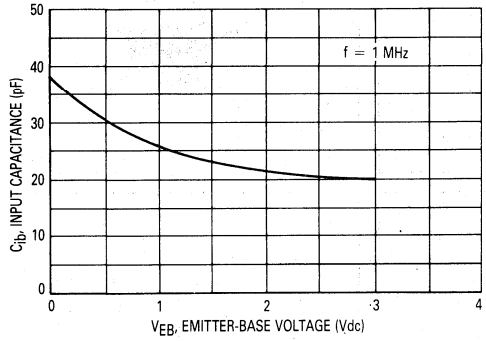


Figure 3. Input Capacitance versus Voltage

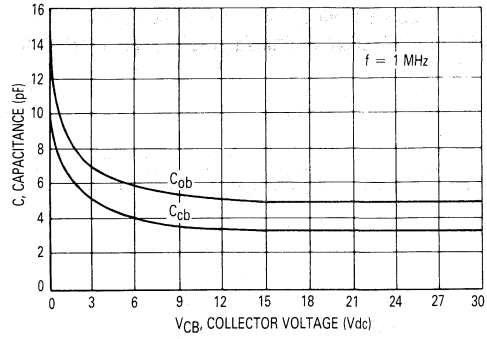
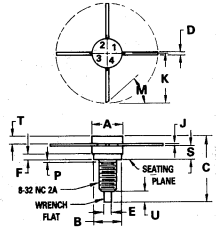


Figure 4. Junction Capacitance versus Voltage

OUTLINE DIMENSIONS



STYLE 3:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR

CASE 244A-01
CERAMIC

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.06	7.26	0.278	0.286
B	6.20	6.50	0.244	0.256
C	15.24	16.51	0.600	0.650
D	0.66	0.86	0.026	0.034
E	1.40	1.65	0.055	0.065
F	1.52	—	0.060	—
J	0.10	0.15	0.004	0.006
K	11.17	—	0.440	—
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
S	2.74	3.35	0.108	0.132
T	1.40	1.78	0.055	0.070
U	2.92	3.68	0.115	0.145

MRF553

The RF Line

1.5 W 175 MHz

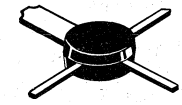
RF LOW POWER TRANSISTOR

NPN SILICON

NPN SILICON RF LOW POWER TRANSISTOR

. . . designed primarily for wideband large signal predriver stages in the VHF frequency range.

- Specified @ 12.5 V, 175 MHz Characteristics
  Output Power = 1.5 W
  Minimum Gain = 11.5 dB
  Efficiency 60% (Typ)
- Cost Effective PowerMacro Package
- Electroless Tin Plated Leads for Improved Solderability



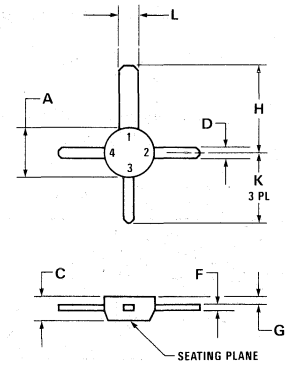
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Continuous	I_C	500	mAdc
Total Device Dissipation @ T_C = 75°C (1,2) Derate above 75°C	P_D	3.0 40	Watts mW/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	25	°C/W

(1) T_C, Case temperature measured on collector lead immediately adjacent to body of package.
(2) The MRF553 PowerMacro must be properly mounted for reliable operation. AN938, "Mounting Techniques for PowerMacro Transistor," discusses methods of mounting and heatsinking.



STYLE 2:
PIN 1. COLLECTOR
2. EMITTER
3. BASE
4. EMITTER

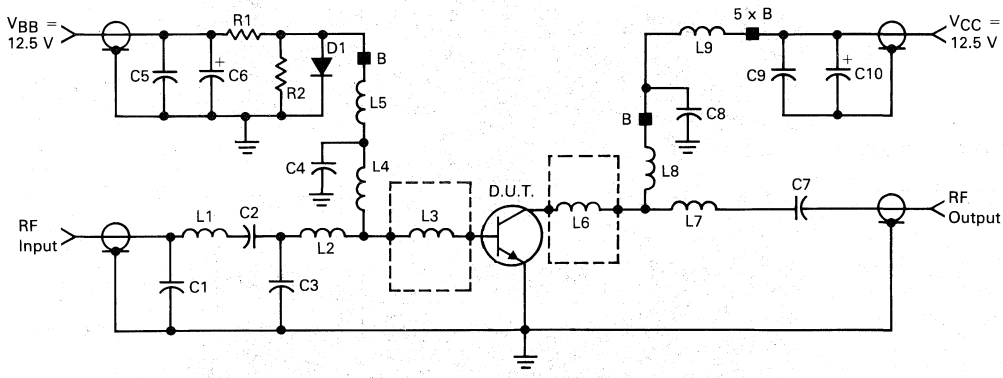
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.44	5.21	0.175	0.205
C	1.90	2.54	0.075	0.100
D	0.84	0.99	0.033	0.039
F	0.20	0.30	0.008	0.012
G	0.63	1.01	0.025	0.040
H	8.84	9.72	0.348	0.383
K	7.24	8.13	0.285	0.320
L	2.46	2.64	0.097	0.104

CASE 317D-01

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)		$V_{(BR)CEO}$	16	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, V_{BE} = 0)		$V_{(BR)CES}$	36	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 5.0 mAdc, I_E = 0)		$V_{(BR)CBO}$	36	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)		$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector-Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)		I_{CES}	—	—	5.0	mAdc
ON CHARACTERISTICS						
DC Current Gain (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)		h_{FE}	30	—	200	—
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	—	12	20	pF
FUNCTIONAL TESTS						
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 1.5 W, f = 175 MHz)	Figure 1,2	G_{pe}	11.5	13	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 1.5 W, f = 175 MHz)	Figure 1,2	η	50	60	—	%
Load Mismatch Stress (V_{CC} = 12.5 Vdc, P_{out} = 1.5 W, f = 175 MHz, VSWR ≥ 10:1 All Phase Angles)		ψ	No Degradation in Output Power			—

FIGURE 1 — 140–175 MHz BROADBAND CIRCUIT SCHEMATIC



C1 — 36 pF Mini Underwood
C2 — 47 pF Mini Underwood
C3 — 91 pF Mini Underwood
C4 — 68 pF Mini Underwood
C5, C9 — 1.0 μF Erie Red Cap Capacitor
C6, C10 — 0.1 μF, 35 V Tantulum
C7 — 470 pF Chip Capacitor
C8 — 2200 pF Chip Capacitor
R1 — 4.7 kΩ, 1/4 W
R2 — 100 Ω, 1/4 W
D1 — 1N4148 Diode

L1 — 3 Turns, #18 AWG, 0.210″ ID, 3/16″ Length
L2, L4, L7 — 0.62″, #18 AWG Wire Bent into "V"
L3, L6 — 60 x 125 x 250 Mils Copper Pad on 27 Mils Thick Alumina Substrate
L5 — 12 μH Molded Choke
L8 — 7 Turns, #18 AWG, 0.170″ ID, 7/16″ Length
L9 — 1.0″, #18 AWG Wire with 5 Ferrite Beads
B — Ferrite Bead
Board Material — Glass Teflon, ϵ_r = 2.56, t = 0.0625″ (See Photomaster, Figure 3)

FIGURE 2 — 140–175 MHZ BROADBAND CIRCUIT

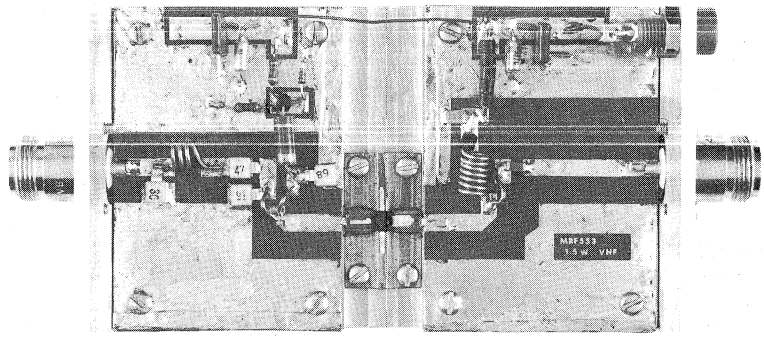
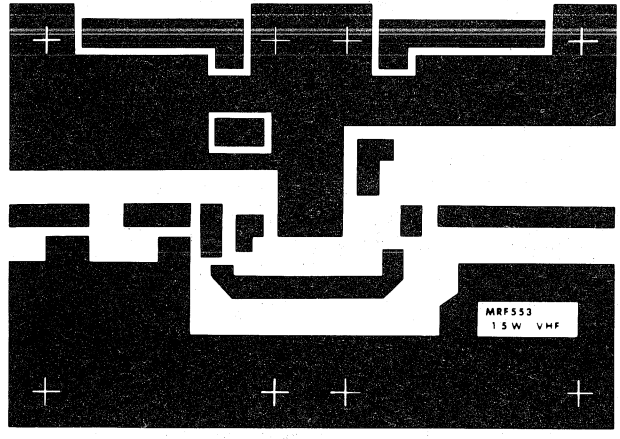


FIGURE 3 — 140–175 MHz TEST CIRCUIT PHOTOMASTER



NOTE: The Printed Circuit Board shown is 75% of the original.

FIGURE 4 — TYPICAL PERFORMANCE IN BROADBAND CIRCUIT

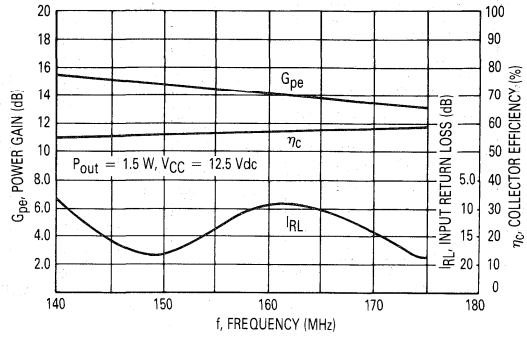


FIGURE 5 — Z_{in} AND Z_{OL} versus COLLECTOR VOLTAGE, INPUT POWER, AND OUTPUT POWER

f Frequency MHz	Z_{in} Ohms						Z_{OL}* Ohms					
	V_{CC} = 7.5 V; P_{in}			V_{CC} = 12.5 V; P_{in}			V_{CC} = 7.5 V; P_{out}			V_{CC} = 12.5 V; P_{out}		
	100 mW	200 mW	300 mW	50 mW	100 mW	150 mW	1.0 W	1.6 W	2.2 W	1.1 W	2.0 W	2.6 W
140	1.65–j3.6	2.0–j2.6	2.3–j1.2	1.7–j4.1	1.8–j3.1	1.9–j2.7	9.9–j11.1	10.6–j5.1	10–j4.9	28.3–j21.5	16–j20.5	16.3–j16.5
175	2.5–j5.6	2.3–j5.9	2.8–j4.0	2.3–j4.6	2.4–j1.2	2.4–j5.7	12.1–j14.9	7.2–j9.8	8.1–j5.4	30.8–j23.3	11.4–j20.9	11.1–j14.3

f Frequency MHz	Z_{in} Ohms						Z_{OL}* Ohms					
	V_{CC} = 7.5 V; P_{in}			V_{CC} = 12.5 V; P_{in}			V_{CC} = 7.5 V; P_{out}			V_{CC} = 12.5 V; P_{out}		
	50 mW	100 mW	200 mW	25 mW	50 mW	100 mW	1.25 W	1.5 W	2.0 W	1.5 W	2.25 W	3.0 W
90	2.5–j9.3	2.5–j6.4	2.5–j4.4	1.6–j10.7	2.5–j7.1	2.2–j1.3	31.8–j9.2	32–j8.9	30.2–j10.7	45.8–j7.2	45.2–j3.9	40–j4.5

*Z_{OL} = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage and frequency.

FIGURE 6 — POWER OUTPUT versus POWER INPUT

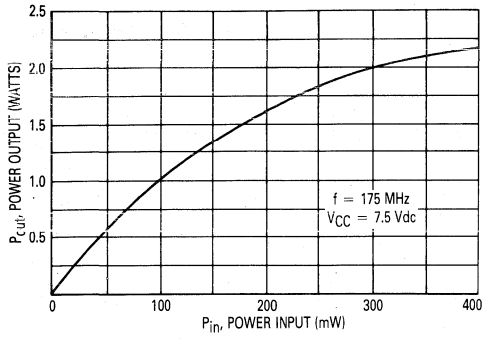


FIGURE 7 — POWER OUTPUT versus POWER INPUT

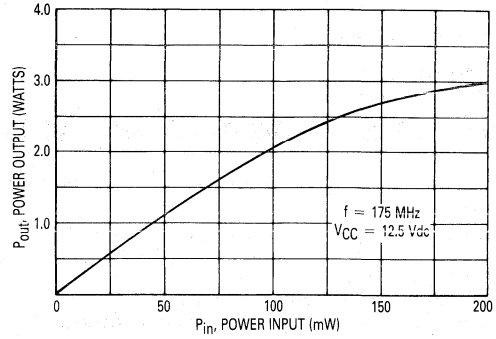


FIGURE 8 — POWER OUTPUT versus FREQUENCY

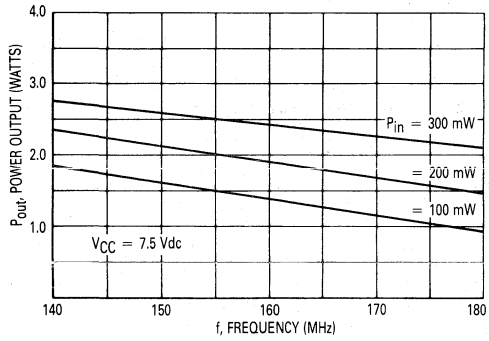


FIGURE 9 — POWER OUTPUT versus FREQUENCY

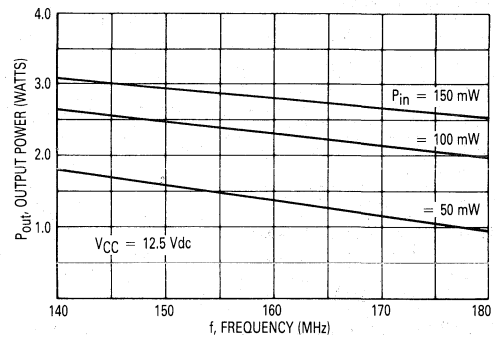


FIGURE 10 — POWER OUTPUT versus COLLECTOR VOLTAGE

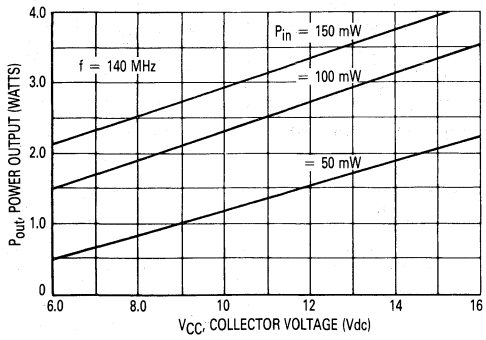
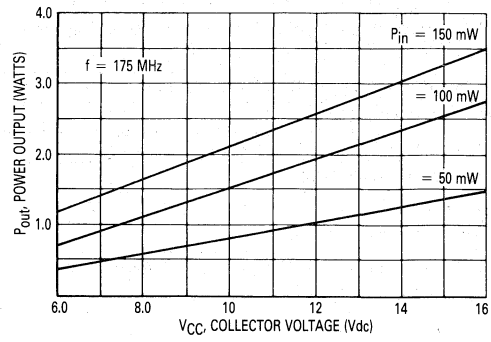
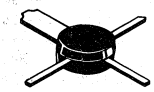


FIGURE 11 — POWER OUTPUT versus COLLECTOR VOLTAGE



MRF555

**1.5 W 470 MHz
RF LOW POWER
TRANSISTOR
NPN SILICON**



CASE 317D-01

3

The RF Line

NPN Silicon RF Low Power Transistor

. . . designed primarily for wideband large signal predriver stages in the UHF frequency range.

- Specified @ 12.5 V, 470 MHz Characteristics @ P_{out} = 1.5 W
  Common Emitter Power Gain = 12.5 dB (Typ)
  Efficiency 60% (Typ)
- Cost Effective PowerMacro Package
- Electroless Tin Plated Leads for Improved Solderability

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4	Vdc
Collector-Current — Continuous	I_C	400	mAdc
Operating Junction Temperature	T_J	150	°C
Total Device Dissipation @ T_C = 75°C (1,2) Derate above 75°C	P_D	3 40	Watts mW/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

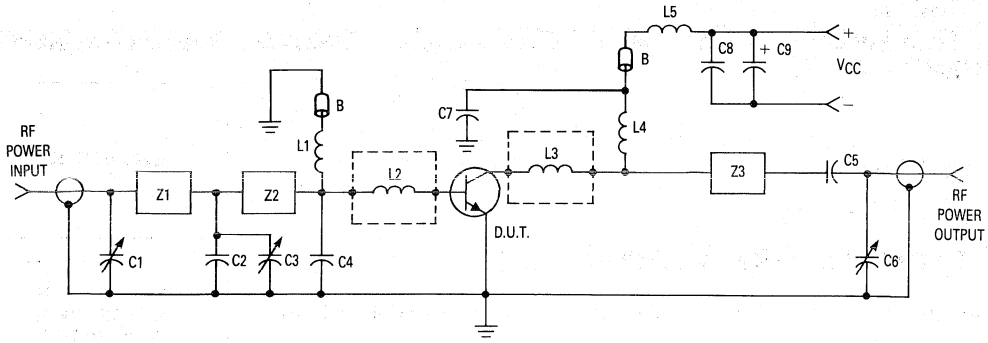
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	25	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 5 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	4	—	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	0.1	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5 Vdc)	h_{FE}	50	90	200	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1 MHz)	C_{ob}	—	3.5	5	pF
FUNCTIONAL TESTS (f = 470 MHz)					
Common-Emitter Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 1.5 W)	G_{pe}	11	12.5	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 1.5 W)	η_c	50	60	—	%
Load Mismatch Stress (V_{CC} = 15.5 Vdc, P_{in} = 125 mW, VSWR ≥ 10:1 all phase angles)	ψ	No Degradation in Output Power			

(1) T_C, Case temperature, measured on collector lead immediately adjacent to body of package.
(2) The MRF555 PowerMacro must be properly mounted for reliable operation. AN938, "Mounting Techniques in PowerMacro Transistor," discusses methods of mounting and heatsinking.



*C1, C3, C6 — 0.8–11 pF Johanson
C2 — 15 pF Clamped Mica, Mini-Underwood
C4 — 36 pF Clamped Mica, Mini-Underwood
C5 — 470 pF Ceramic Chip Capacitor
C7 — 91 pF Clamped Mica, Mini-Underwood
C8 — 68 pF Clamped Mica, Mini-Underwood
C9 — 1 μF, 25 V Tantalum
B — Bead, Ferroxcube 56-590-65/3B

*Fixed tuned for broadband response.

L1 — 5 Turns #21 AWG, 5/32" I.D.
L2, L3 — 60 x 125 x 250 Mils Copper Pad on 27 Mil Thick Alumina Substrate
L4, L5 — 7 Turns #21 AWG 5/32" I.D
Z1 — 1.29" x 0.16" Microstrip
Z2 — 0.70" x 0.16" Microstrip
Z3 — 2.18" x 016" Microstrip
PCB — 1/16" Glass Teflon, 1 oz. cu. clad, double sided, ϵ_r = 2.5
(See Figure 5 — Photomaster)

Figure 1. 400–512 MHz Broadband Circuit

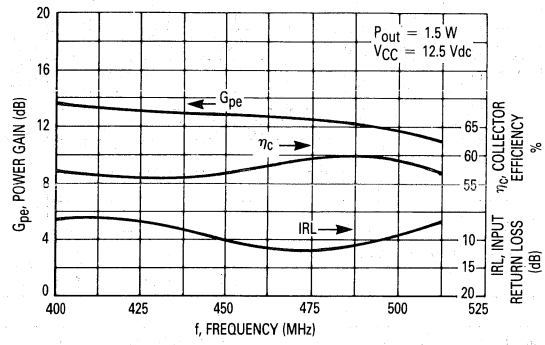


Figure 2. Performance in Broadband Circuit

f Frequency MHz	Z_{in} Ohms		Z_{OL}* Ohms	
	V_{CC} = 7.5 V	V_{CC} = 12.5 V	V_{CC} = 7.5 V	V_{CC} = 12.5 V
	P_{in} = 100 mW	P_{in} = 50 mW	P_{out} 400 MHz = 1.5 W P_{out} 450 MHz = 1.35 W P_{out} 512 MHz = 1.05 W	P_{out} 400 MHz = 1.9 W P_{out} 450 MHz = 1.45 W P_{out} 512 MHz = 0.9 W
400	2.9 – j2.7	1.9 – j3.1	18.0 – j13.4	12.2 – j19.7
450	2.2 – j0.8	2.6 – j4.0	21.6 – j9.9	20.2 – j18.6
512	3.5 – j1.2	2.6 – j2.6	20.1 – j1.0	23.4 – j23.0

*Z_{OL} = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage and frequency.

Figure 3. Z_{in} and Z_{OL} versus Collector Voltage, Input Power and Output Power

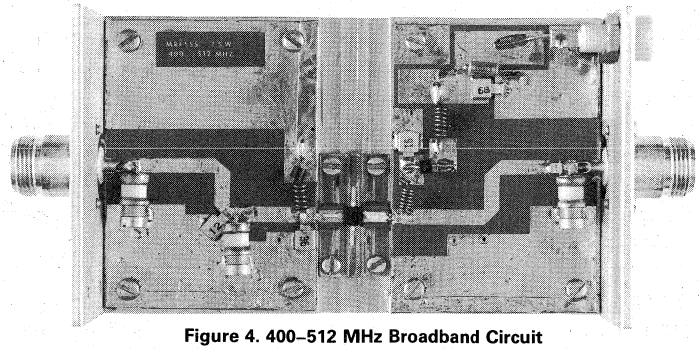
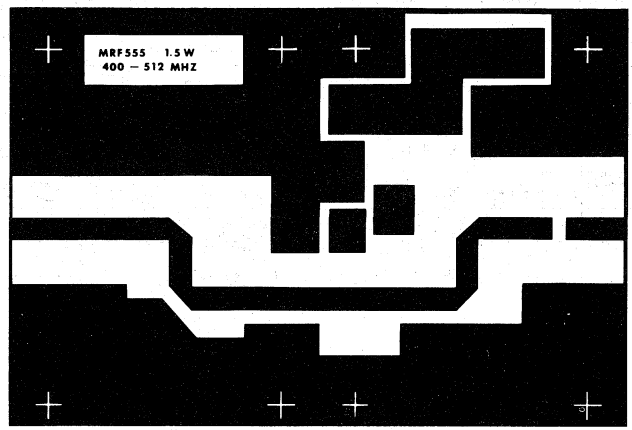


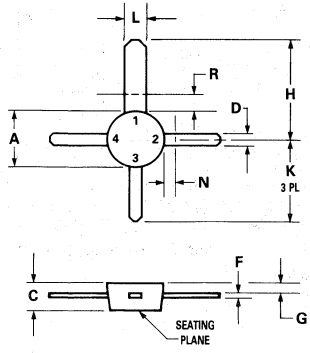
Figure 4. 400–512 MHz Broadband Circuit



NOTE: The Printed Circuit Board shown is 75% of the original.

Figure 5. 400–512 MHz Broadband Circuit Photomaster

OUTLINE DIMENSIONS



CASE 317D-01

STYLE 2:
PIN 1. COLLECTOR
2. EMITTER
3. BASE
4. EMITTER

NOTE:
DIMENSION D NOT APPLICABLE IN ZONES N AND R.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.44	5.21	0.175	0.205
C	1.90	2.54	0.075	0.100
D	0.84	0.99	0.033	0.039
F	0.20	0.30	0.008	0.012
G	0.63	1.01	0.025	0.040
H	8.84	9.72	0.348	0.383
K	7.24	8.13	0.285	0.320
L	2.46	2.64	0.097	0.104
N	—	1.65	—	0.065
R	—	3.25	—	0.128

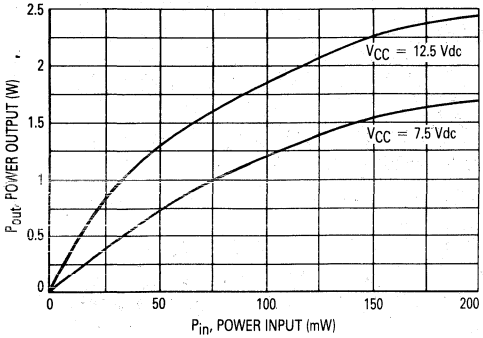


Figure 6. Power Output versus Power Input

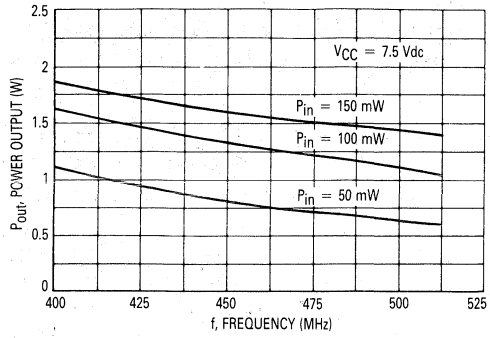


Figure 7. Power Output versus Frequency

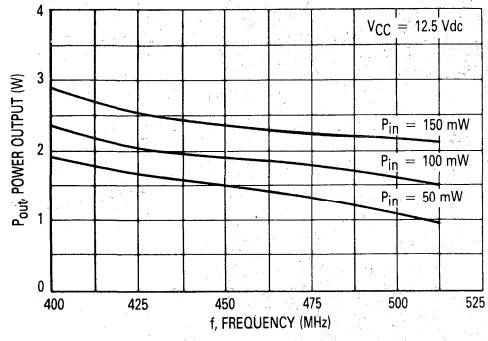


Figure 8. Power Output versus Frequency

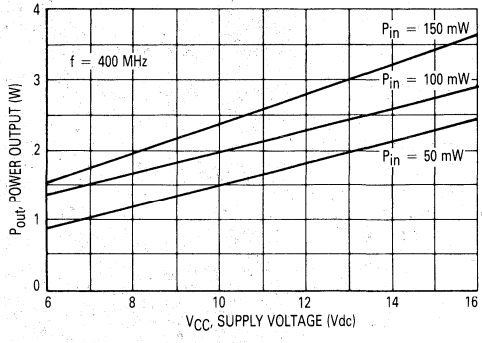


Figure 9. Power Output versus Supply Voltage

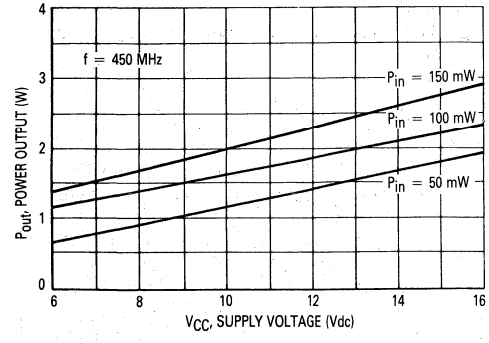


Figure 10. Power Output versus Supply Voltage

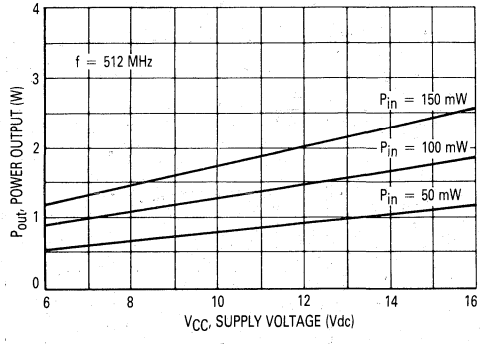


Figure 11. Power Output versus Supply Voltage

MRF557

The RF Line

1.5 W 870 MHz

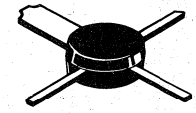
RF LOW POWER TRANSISTOR

NPN SILICON

NPN SILICON RF LOW POWER TRANSISTOR

. . . designed primarily for wideband large signal predriver stages in the 800 MHz frequency range.

- Specified @ 12.5 V, 870 MHz Characteristics
  Output Power = 1.5 W
  Minimum Gain = 8.0 dB
  Efficiency 60% (Typ)
- Cost Effective PowerMacro Package
- Electroless Tin Plated Leads for Improved Solderability



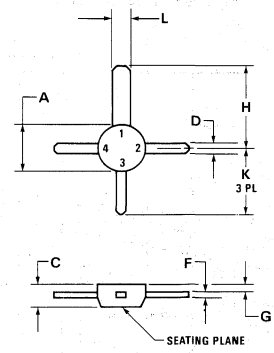
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Continuous	I_C	400	mAdc
Total Device Dissipation @ T_C = 75°C (1,2) Derate above 75°C	P_D	3.0 40	Watts mW/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	25	°C/W

(1) T_C, Case temperature measured on collector lead immediately adjacent to body of package.
(2) The MRF557 PowerMacro must be properly mounted for reliable operation. AN938, "Mounting Techniques in PowerMacro Transistor," discusses methods of mounting and heatsinking.



STYLE 2:
PIN 1. COLLECTOR
2. EMITTER
3. BASE
4. EMITTER

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.44	5.21	0.175	0.205
C	1.90	2.54	0.075	0.100
D	0.84	0.99	0.033	0.039
F	0.20	0.30	0.008	0.012
G	0.63	1.01	0.025	0.040
H	8.84	9.72	0.348	0.383
K	7.24	8.13	0.285	0.320
L	2.46	2.64	0.097	0.104

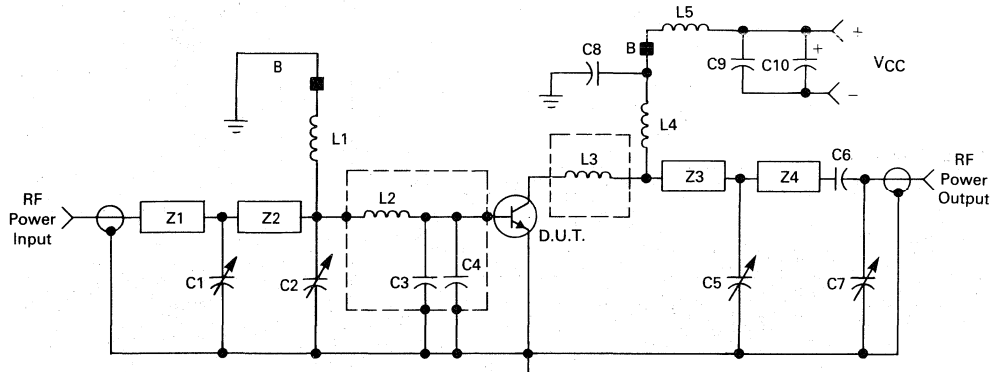
CASE 317D-01

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, i_B = 0)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	0.1	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	50	90	200	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	3.5	5.0	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain Figures 1, 2 (V_{CC} = 12.5 Vdc, P_{out} = 1.5 W, f = 870 MHz)	G_{pe}	8.0	9.0	—	dB
Collector Efficiency Figures 1, 2 (V_{CC} = 12.5 Vdc, P_{out} = 1.5 W, f = 870 MHz)	η_C	55	60	—	%
Load Mismatch Stress Figures 1, 2 (V_{CC} = 15.5 Vdc, P_{in} = 225 mW, f = 870 MHz, VSWR ≥ 10:1 all phase angles)	ψ	No Degradation in Output Power			

3

FIGURE 1 — 800–880 MHz BROADBAND CIRCUIT



C1, C2, C5, C7 — 0.8–8.0 pF Johanson Gigatrim*
C3, C4 — 15 pF Clamped Mica, Mini-Underwood
C6 — 27 pF Clamped Mica, Mini-Underwood
C8 — 91 pF Clamped Mica, Mini-Underwood
C9 — 68 pF Clamped Mica, Mini-Underwood
C10 — 1.0 μF, 25 V Tantalum
B — Bead, Ferroxcube 56-590-65/3B
PCB — 1/16" Glass Teflon, ϵ_r = 2.56
(See Photomaster Figure 3)

L1, L4 — 5 Turns #21 AWG, 5/32" ID
L2, L3 — 60 x 125 x 250 Mils Copper Tab on 27 Mil Thick Alumina Substrate
L5 — 7 Turns #21 AWG, 5/32" ID
Z1 — 1.65 x 0.163" Microstrip, Z_O = 50 Ω
Z2 — 0.85 x 0.163" Microstrip, Z_O = 50 Ω
Z3 — 0.625 x 0.163" Microstrip, Z_O = 50 Ω
Z4 — 1.35 x 0.163" Microstrip, Z_O = 50 Ω

*Fixed tuned for broadband response.

FIGURE 2 — 800–880 MHz BROADBAND CIRCUIT

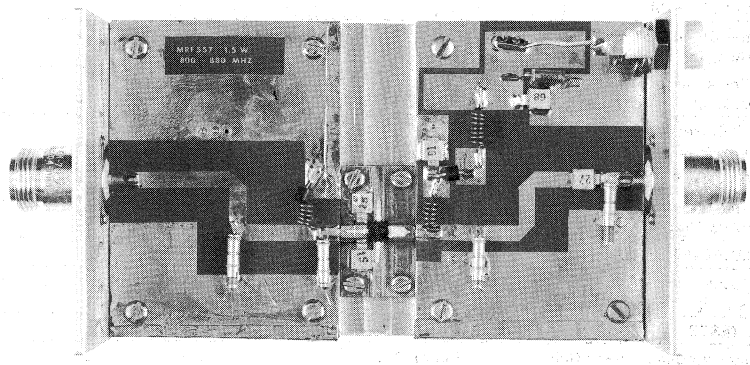
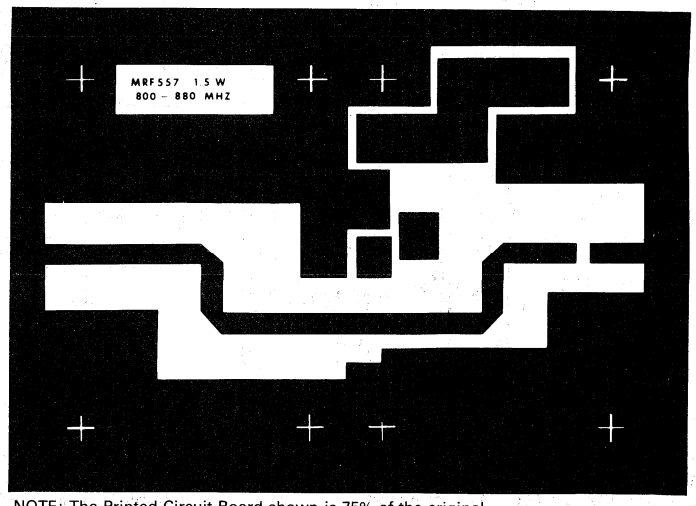


FIGURE 3 — 800–880 MHz TEST CIRCUIT PHOTOMASTER



NOTE: The Printed Circuit Board shown is 75% of the original.

FIGURE 4 — PERFORMANCE IN BROADBAND CIRCUIT

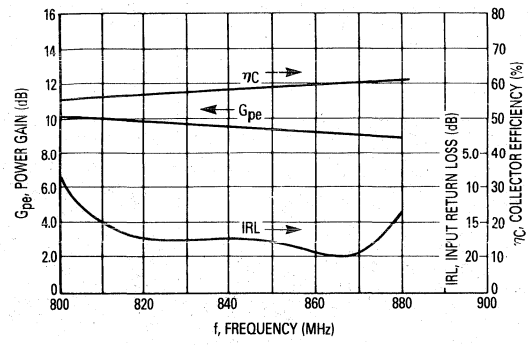


FIGURE 5 — Z_{in} and Z_{ol} versus COLLECTOR VOLTAGE, INPUT POWER AND OUTPUT POWER

f FREQUENCY MHz	Z_{in} Ohms		Z_{OL}* Ohms	
	V_{CC} = 7.5 V	V_{CC} = 12.5 V	V_{CC} = 7.5 V	V_{CC} = 12.5 V
	P_{in} = 300 mW	P_{in} = 200 mW	P_{out} 806 MHz = 1.7 W P_{out} 870 MHz = 1.4 W P_{out} 960 MHz = 1.0 W	P_{out} 806 MHz = 2.1 W P_{out} 870 MHz = 1.8 W P_{out} 960 MHz = 1.1 W
806	2.4 + j3.9	2.4 + j3.1	14.7 − j4.4	13.6 − j12.8
870	2.5 + j4.6	2.7 + j3.7	17.2 − j8.6	16 − j13.2
960	6.1 + j7.4	6.8 + j8.3	40 − j8.3	38 − j10.5

*Z_{OL} = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage and frequency.

FIGURE 6 — POWER OUTPUT versus POWER INPUT

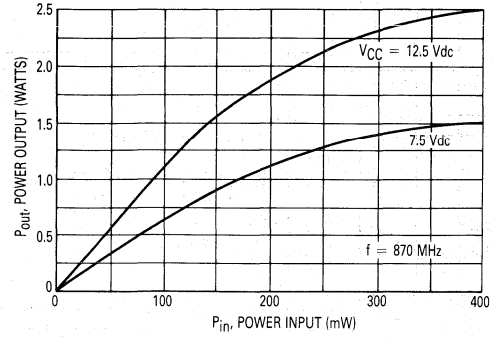


FIGURE 7 — POWER OUTPUT versus FREQUENCY

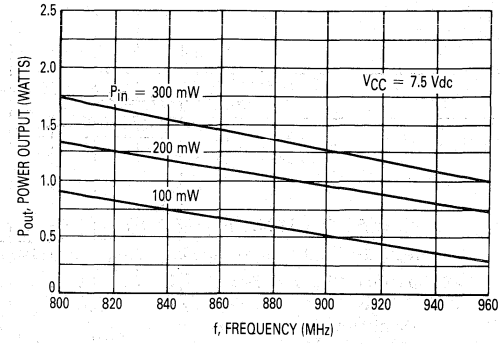


FIGURE 8 — POWER OUTPUT versus FREQUENCY

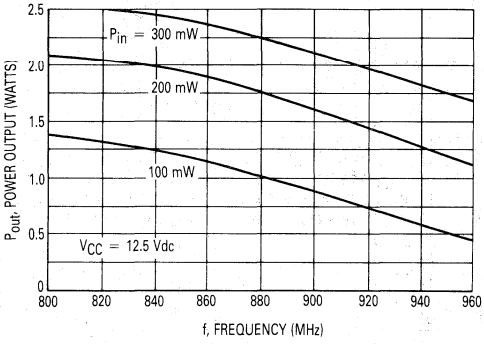


FIGURE 9 — POWER OUTPUT versus SUPPLY VOLTAGE

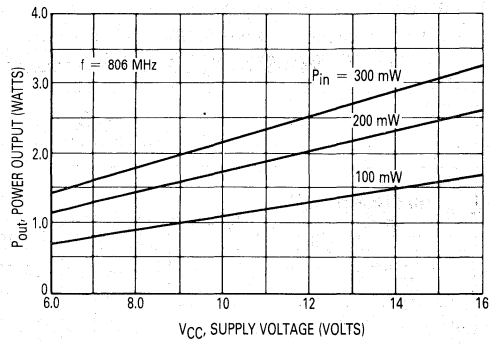


FIGURE 10 — POWER OUTPUT versus SUPPLY VOLTAGE

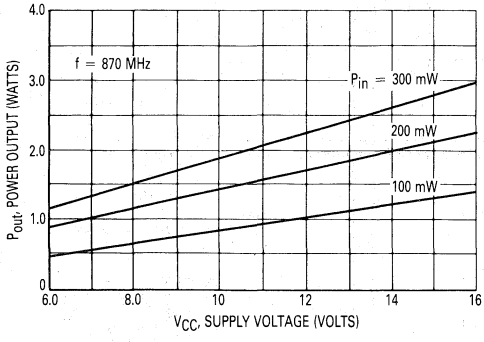
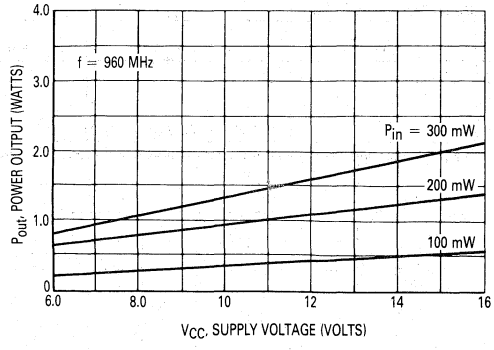


FIGURE 11 — POWER OUTPUT versus SUPPLY VOLTAGE



MRF559

The RF Line

0.5 W — 870 MHz

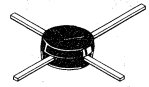
HIGH FREQUENCY TRANSISTOR

NPN SILICON

NPN SILICON HIGH FREQUENCY TRANSISTOR

. . . designed for UHF linear and large-signal amplifier applications.

- Specified 12.5 Volt, 870 MHz Characteristics —
  Output Power = 0.5 Watts
  Minimum Gain = 8.0 dB
  Efficiency = 50%
- S Parameter Data From 250 MHz to 1.5 GHz
- 1.0 dB Compression > +20 dBm Typ
- Ideally Suited for Broadband, Class A, Low-Noise Applications
- Recommended As Driver for MHW808 and MHW820, 806–870 MHz Power Modules

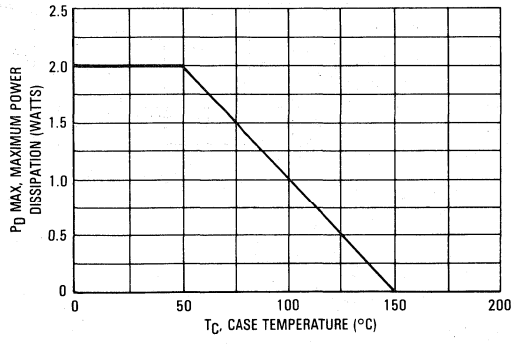


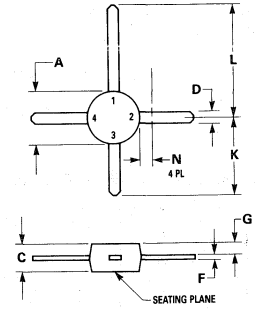
3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	3.0	Vdc
Collector-Current — Continuous	I_C	150	mAdc
Total Device Dissipation @ T_C = 50°C Derate above 50°C	P_D	2.0 20	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

POWER DISSIPATION





STYLE 2:
PIN 1. COLLECTOR
2. EMITTER
3. BASE
4. EMITTER

NOTE:
DIMENSION D NOT APPLICABLE IN ZONE N.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.44	5.21	0.175	0.205
C	1.90	2.54	0.075	0.100
D	0.84	0.99	0.033	0.039
F	0.20	0.30	0.008	0.012
G	0.76	1.14	0.030	0.045
K	7.24	8.13	0.285	0.320
L	10.54	11.43	0.415	0.450
N	—	1.65	—	0.065

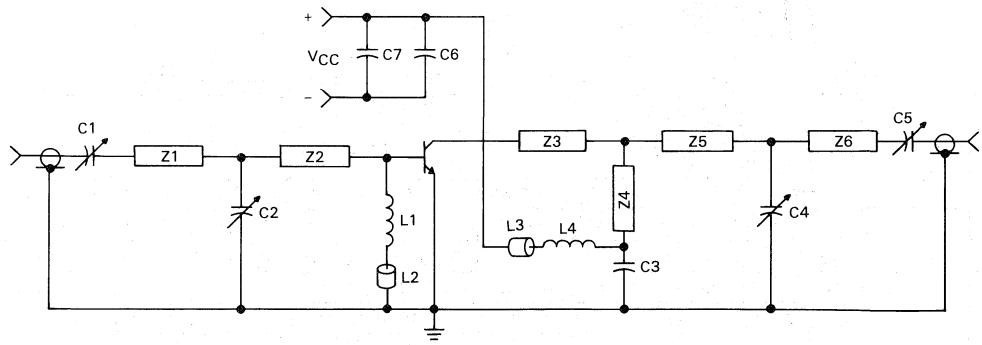
CASE 317-01

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)		$V_{(BR)CEO}$	18	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)		$V_{(BR)CBO}$	36	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		$V_{(BR)EBO}$	3.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0)		I_{CES}	—	—	1.0	mAdc
ON CHARACTERISTICS						
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)		h_{FE}	30	90	200	—
DYNAMIC CHARACTERISTICS						
Current-Gain — Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 200 MHz)		f_T	—	3000	—	MHz
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	—	2.0	2.5	pF
FUNCTIONAL TESTS						
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 0.5 W)	f = 870 MHz f = 512 MHz	G_{PE}	8.0 —	9.5 13	— —	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 0.5 W)	f = 870 MHz f = 512 MHz	η	50 —	65 60	— —	%
TYPICAL PERFORMANCE @ V_{CC} = 7.5 V						
Common-Emitter Amplifier Power Gain (V_{CC} = 7.5 Vdc, P_{out} = 0.5 W)	f = 870 MHz f = 512 MHz	G_{PE}	— —	6.5 10	— —	dB
Collector Efficiency (V_{CC} = 7.5 Vdc, P_{out} = 0.5 W)	f = 870 MHz f = 512 MHz	η	— —	70 65	— —	%

3

FIGURE 1 — 870 MHz TEST FIXTURE



C1, C2, C4, C5 — 1.0–10 pF Johanson
C3, C6 — 0.001 μF Chip Capacitor
C7 — 1.0 μF Tantulam
L1, L4 — 4 Turns #26 AWG, 0.3 cm ID, 0.4 cm Long
L2, L3 — Ferrite Bead
Microstrip Elements — ϵ_r = 1.0

Z1 — 50 Ω 1.5 cm
Z2 — 30 Ω 2.5 cm
Z3 — 50 Ω 2.0 cm
Z4 — 50 Ω 1.2 cm
Z5, Z6 — 50 Ω 1.25 cm

FIGURE 2 — OUTPUT POWER versus INPUT POWER
f = 512 MHz

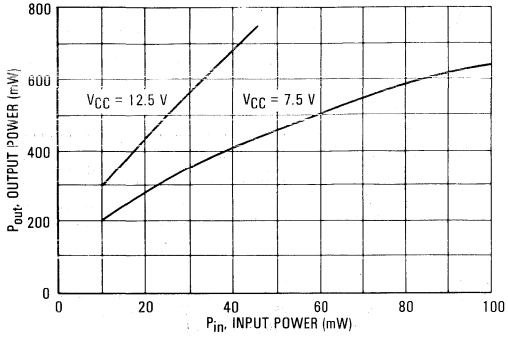


FIGURE 3 — OUTPUT POWER versus FREQUENCY
V_{CC} = 7.5 V

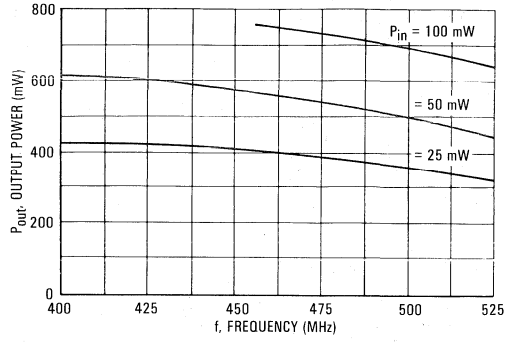


FIGURE 4 — OUTPUT POWER versus COLLECTOR VOLTAGE
f = 512 MHz

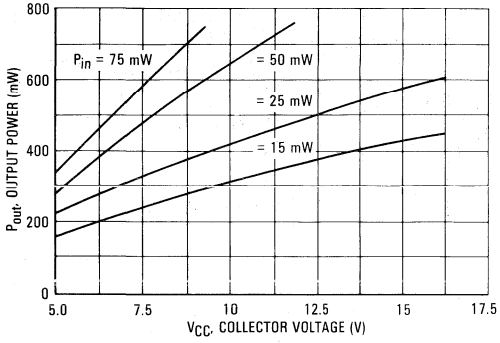


FIGURE 5 — OUTPUT POWER versus FREQUENCY
V_{CC} = 12.5 V

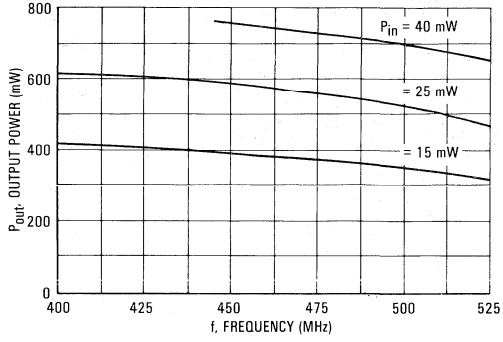


FIGURE 6 — Z_{in} AND Z_{OL} versus COLLECTOR VOLTAGE, INPUT POWER, AND OUTPUT POWER

f FREQUENCY MHz	Z_{in} OHMS			Z_{OL}* OHMS					
	V_{CC} = 7.5-12.5 V			V_{CC} = 7.5 V			V_{CC} = 12.5 V		
	15 mW	25 mW	50 mW	0.25 W	0.50 W	0.75 W	0.25 W	0.50 W	0.75 W
400	4.3 - j13.3	4.9 - j11.0	5.7 - j8.7	31 - j49	44 - j34	42 - j4.9	20 - j68	42 - j60	52 - j54
440	3.9 - j8.8	4.5 - j8.7	5.4 - j6.9	27 - j42	39 - j30	40 - j6.9	19 - j62	37 - j54	49 - j50
480	3.5 - j4.4	4.1 - j6.5	5.0 - j4.3	24 - j36	36 - j25	39 - j9.0	18 - j56	33 - j48	47 - j46
520	3.2 - j2.2	3.8 - j4.3	4.7 - j1.7	22 - j30	34 - j20	37 - j12	17 - j52	31 - j44	47 - j42

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

FIGURE 7 — OUTPUT POWER versus INPUT POWER
f = 870 MHz

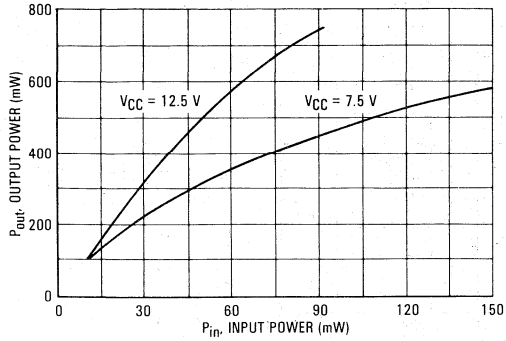


FIGURE 8 — OUTPUT POWER versus FREQUENCY
V_{CC} = 7.5 V

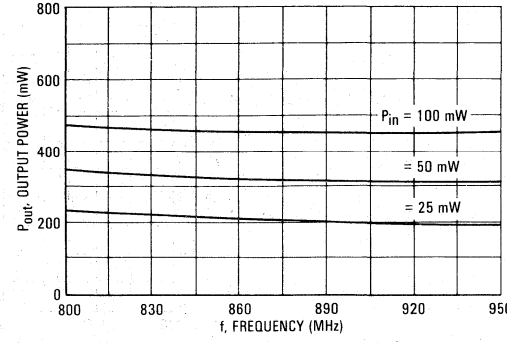


FIGURE 9 — OUTPUT POWER versus COLLECTOR VOLTAGE
f = 870 MHz

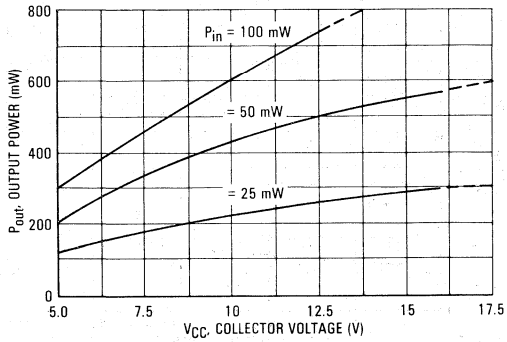


FIGURE 10 — OUTPUT POWER versus FREQUENCY
V_{CC} = 12.5 V

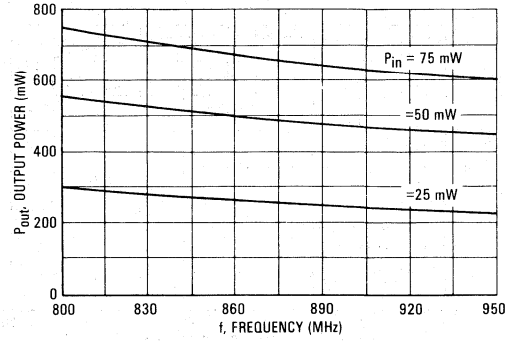
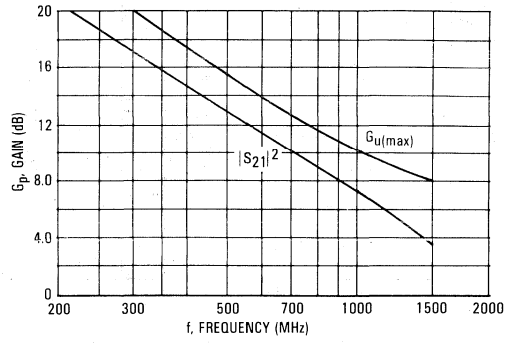


FIGURE 11 — Z_{in} AND Z_{OL} versus COLLECTOR VOLTAGE, INPUT POWER, AND OUTPUT POWER

f FREQUENCY MHz	Z_{in} OHMS			Z_{OL}* OHMS					
	V_{CC} = 7.5-12.5 V			V_{CC} = 7.5 V			V_{CC} = 12.5 V		
	25 mW	50 mW	100 mW	0.25 W	0.50 W	0.75 W	0.25 W	0.50 W	0.75 W
800	2.9 + j2.2	3.8 + j4.4	4.7 + j6.5	15.0 – j36.8	22.7 – j30.6	27.1 – j22.6	14.6 – j43.6	17.2 – j39.7	23.4 – j37.7
850	3.2 + j3.5	3.8 + j5.2	4.8 + j7.4	15.7 – j35.3	23.9 – j28.7	27.3 – j21.5	16.3 – j40.8	17.8 – j39.5	23.7 – j36.8
900	3.8 + j5.7	4.4 + j7.0	5.4 + j8.7	16.4 – j33.7	25.1 – j27.0	27.5 – j20.5	17.3 – j38.2	18.3 – j39.3	23.9 – j36.0
950	4.1 + j7.4	4.5 + j8.8	5.5 + j10.1	17.0 – j32.2	26.3 – j25.2	27.6 – j19.4	17.2 – j36.1	20.1 – j38.5	24.5 – j35.6

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

FIGURE 12 — GAIN versus FREQUENCY
V_{CE} = 10 V, I_C = 50-100 mA



$$G_{u(max)} = \frac{|S_{21}|^2}{(1-|S_{11}|^2)\ (1-|S_{22}|^2)}$$

FIGURE 13 — GAIN versus COLLECTOR CURRENT
V_{CE} = 10 V

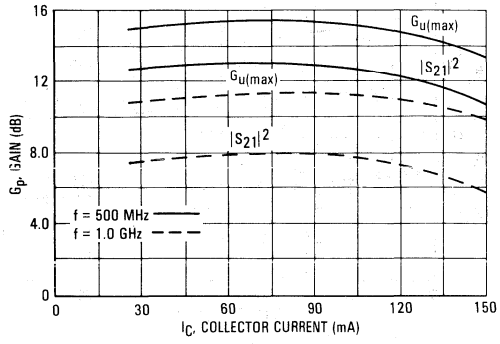


FIGURE 14 — NOISE FIGURE AND ASSOCIATED GAIN versus COLLECTOR CURRENT
V_{CE} = 10 V

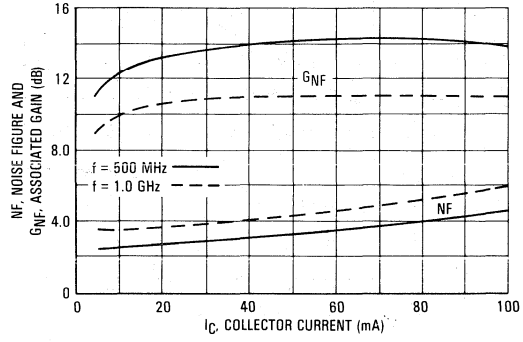


FIGURE 15 — CURRENT GAIN BANDWIDTH PRODUCT versus COLLECTOR CURRENT
V_{CE} = 10 V

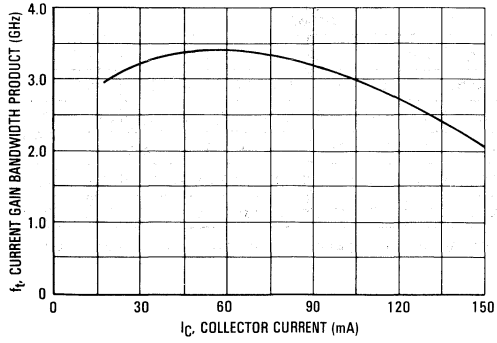


FIGURE 16 — OUTPUT CAPACITANCE versus COLLECTOR BASE VOLTAGE

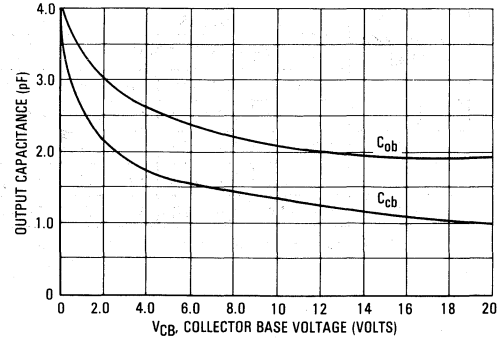
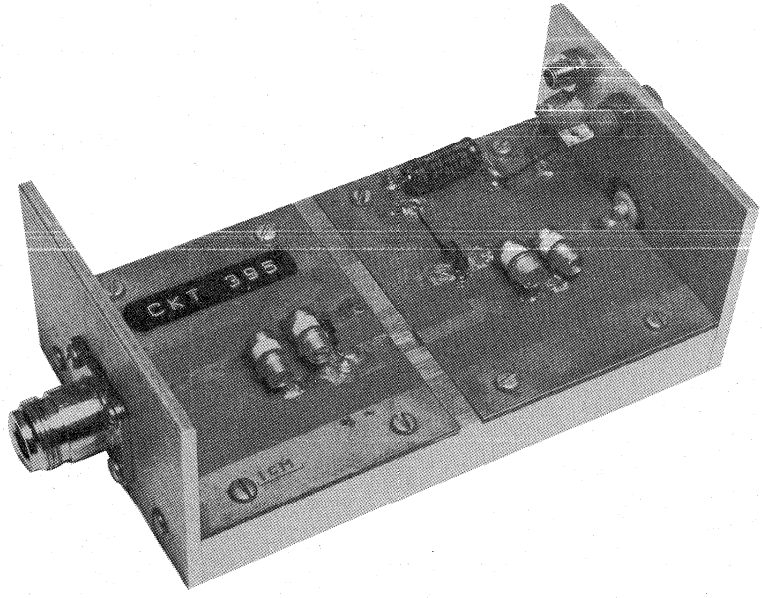


FIGURE 17 — COMMON EMITTER SCATTERING PARAMETERS

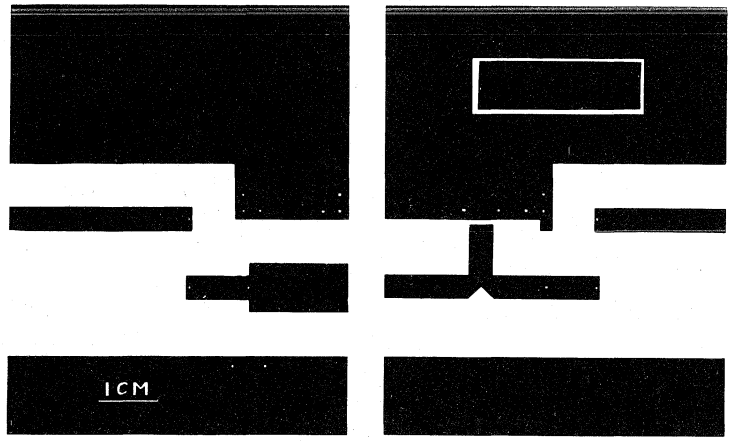
V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
5.0	10	250	0.72	-161	6.20	93	0.057	30	0.30	-91
		500	0.73	179	3.16	76	0.069	43	0.27	-94
		1000	0.76	158	1.62	55	0.105	63	0.27	-119
		1500	0.82	142	1.08	41	0.155	70	0.41	-137
	25	250	0.70	-173	7.17	89	0.045	47	0.26	-123
		500	0.70	172	3.63	75	0.073	60	0.20	-128
		1000	0.74	152	1.90	54	0.134	67	0.21	-157
		1500	0.79	136	1.32	39	0.196	66	0.32	-167
	50	250	0.72	-178	7.63	89	0.038	56	0.27	-139
		500	0.72	170	3.85	77	0068	67	0.23	-141
		1000	0.75	153	2.01	59	0.129	72	0.23	-162
		1500	0.81	137	1.40	46	0.188	70	0.32	-164
	100	250	0.73	179	7.34	88	0.036	61	0.26	-143
		500	0.74	169	3.70	77	0.067	71	0.22	-144
		1000	0.76	153	1.94	59	0.130	74	0.24	-166
		1500	0.81	138	1.36	46	0.191	71	0.32	-167
	150	250	0.78	176	5.19	92	0.033	64	0.22	-131
		500	0.78	167	2.76	78	0.065	74	0.21	-131
		1000	0.80	151	1.49	58	0.129	77	0.24	-155
		1500	0.85	135	1.05	45	0.191	73	0.35	-161
10	10	250	0.69	-157	7.03	94	0.050	33	0.34	-67
		500	0.70	-178	3.59	77	0.060	46	0.32	-69
		1000	0.74	160	1.84	55	0.094	67	0.29	-94
		1500	0.81	142	1.20	41	0.148	76	0.42	-121
	25	250	0.67	-168	8.30	91	0.039	46	0.24	-93
		500	0.68	176	4.25	77	0.060	60	0.21	-89
		1000	0.72	158	2.19	57	0.109	71	0.19	-114
		1500	0.78	142	1.47	44	0.165	74	0.31	-134
	50	250	0.68	-174	8.88	90	0.035	55	0.21	-110
		500	0.68	172	4.49	77	0.060	67	0.18	-104
		1000	0.72	155	2.31	59	0.113	74	0.17	-128
		1500	0.77	139	1.58	46	0.169	74	0.28	-140
	100	250	0.68	-178	8.49	89	0.03	61	0.19	-104
		500	0.69	170	4.32	76	0.06	71	0.17	-97
		1000	0.72	153	2.25	58	0.12	76	0.17	-123
		1500	0.78	137	1.53	44	0.18	75	0.28	-137
	150	250	0.72	178	6.53	91	0.029	64	0.22	-71
		500	0.73	169	3.37	77	0.056	75	0.24	-75
		1000	0.76	152	1.79	57	0.112	80	0.22	-105
		1500	0.83	137	1.22	43	0.175	79	0.34	-129

FIGURE 18 — TUNABLE TEST FIXTURE



3

FIGURE 19 — PRINTED CIRCUIT BOARD LAYOUT



INPUT OUTPUT

NOTE: The Printed Circuit Board shown is 75% of the original.

MRF571
MRF572
MRFC572

The RF Line

NPN SILICON HIGH FREQUENCY TRANSISTORS

. . . designed for low-noise, wide dynamic range front end amplifiers, low-noise VCO's, and microwave power multipliers.

- Low Noise
- High Gain
- Available in Low Cost Plastic, High Reliability Ceramic or Die
- State-of-the-Art Technology
  - Fine Line Geometry
  - Ion Implanted Arsenic Emitters
  - Gold Top Metallization and Wires
  - Silicon Nitride Passivation
- Fully Characterized

f_T = 8.0 GHz @ 50 mA
NF = 1.0 dB @ 500 MHz
NF = 1.5 dB @ 1.0 GHz
NF = 2.5 dB @ 2.0 GHz

HIGH FREQUENCY TRANSISTORS

NPN SILICON

3

MAXIMUM RATINGS		MRFC572 Chip	MRF571 Macro-X Case 317-01	MRF572 Case 303-01	
Ratings	**Symbol**	**Values**			**Unit**
Collector-Emitter Voltage	V_{CEO}	10	10	10	Vdc
Collector-Base Voltage	V_{CBO}	20	20	20	Vdc
Emitter-Base Voltage	V_{EBO}	3.0	3.0	3.0	Vdc
Collector Current — Continuous	I_C	70	70	70	mAdc
Total Device Dissipation @ T_C = 50°C(1) Derate above T_C = 50°C	P_D	0.75 T_J = 200°C max	1.0 10	0.75 5.0	Watts mW/°C
Storage Temperature	T_{stg}	−65 to +200	−65 to +150	−65 to +200	°C

NOTE 1. Case temperature measured on collector lead immediately adjacent to body of package.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_E = 0)		$V_{(BR)CEO}$	10	12	—	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_B = 0)		$V_{(BR)CBO}$	20	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 50 μAdc, I_C = 0)		$V_{(BR)EBO}$	2.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 8.0 Vdc, I_E = 0)		I_{CBO}	—	—	10	μAdc
ON CHARACTERISTICS						
DC Current Gain (I_C = 30 mAdc, V_{CE} = 5.0 Vdc)		h_{FE}	50	—	300	—
DYNAMIC CHARACTERISTICS						
Collector-Base Capacitance (V_{CB} = 6.0 Vdc, I_E = 0, f = 1.0 MHz)		C_{cb}	—	0.7	1.0	pF
Current Gain — Bandwidth Product (V_{CE} = 8.0 Vdc, I_C = 50 mA, f = 1.0 GHz)		f_T	—	8.0	—	GHz
FUNCTIONAL TESTS						
Gain @ Noise Figure (I_C = 5.0 mAdc, V_{CE} = 6.0 Vdc)	f = 0.5 GHz	G_{NF}	—	16.5	—	dB
	f = 1.0 GHz		10	12	—	
Noise Figure (I_C = 5.0 mAdc, V_{CE} = 6.0 Vdc)	f = 0.5 GHz	NF	—	1.0	—	dB
	f = 1.0 GHz		—	1.5	2.0	
MRF571	f = 2.0 GHz		—	2.8	—	
MRF572	f = 2.0 GHz		—	2.5	—	

3

FIGURE 1 — C_{cb}, COLLECTOR-BASE CAPACITANCE versus VOLTAGE

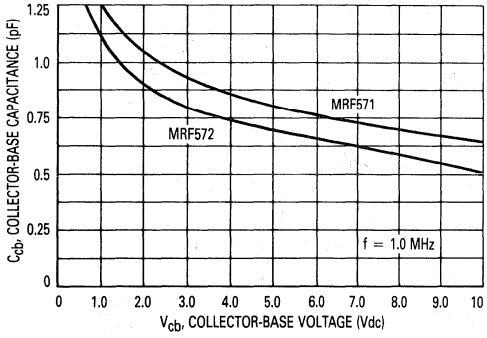


FIGURE 2 — C_{ib}, INPUT CAPACITANCE versus EMITTER BASE VOLTAGE

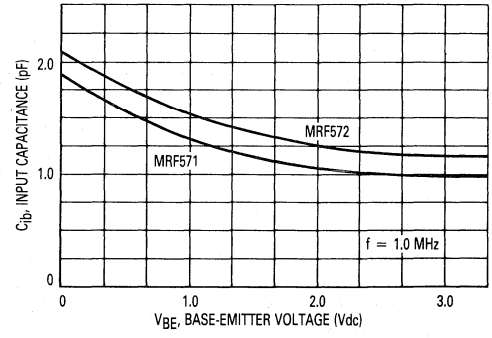


FIGURE 3 — MRF571 — GAIN AT NOISE FIGURE AND NOISE FIGURE versus FREQUENCY

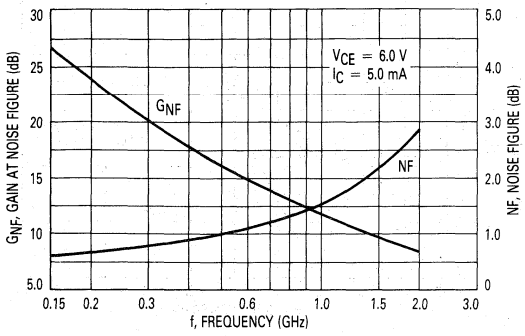


FIGURE 4 — MRF572 — GAIN AT NOISE FIGURE AND NOISE FIGURE versus FREQUENCY

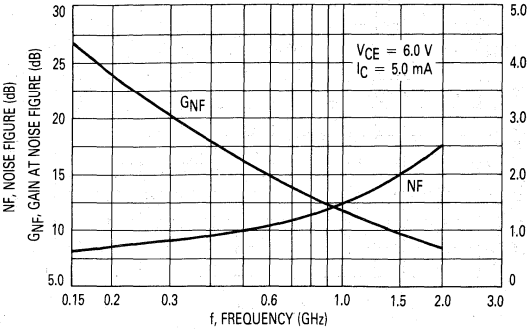


FIGURE 5 — MRF571 and MRF572 — GAIN AT NOISE FIGURE AND NOISE FIGURE versus COLLECTOR CURRENT

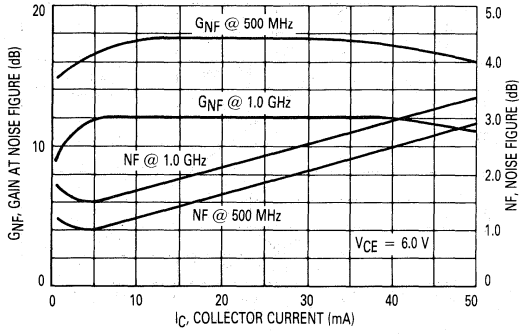


FIGURE 6 — f_T, CURRENT GAIN-BANDWIDTH PRODUCT versus COLLECTOR CURRENT

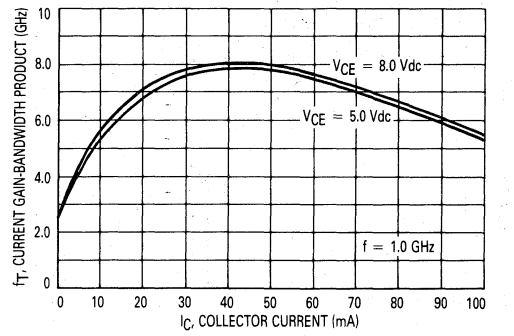


FIGURE 7 — G_{Amax}, MAXIMUM AVAILABLE GAIN versus FREQUENCY

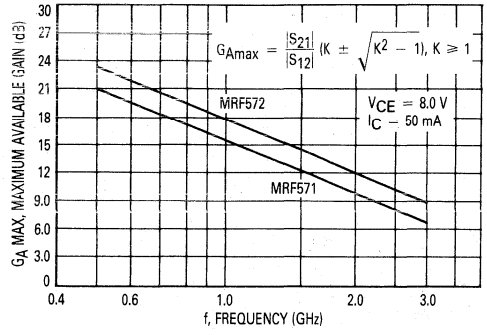


FIGURE 8 — 1.0 dB COMPRESSION PT. AND THIRD ORDER INTERCEPT

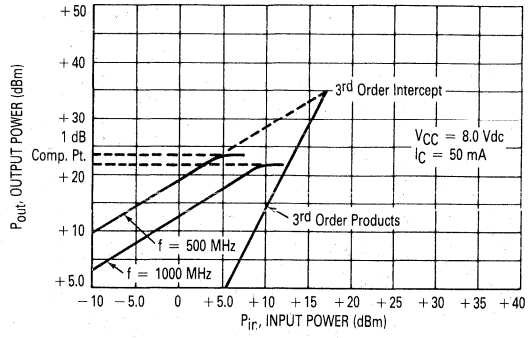


FIGURE 9 — MRF571 — $G_{U}max$ and $|S_{21}|^2$ versus FREQUENCY

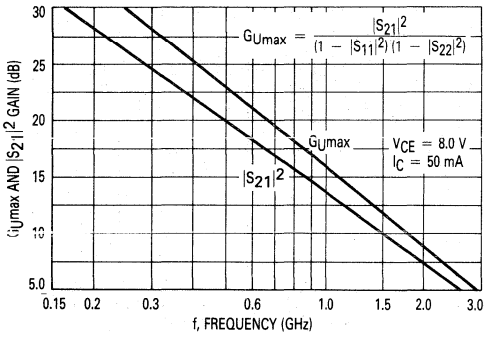
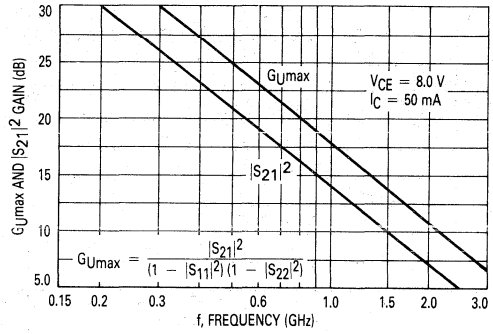
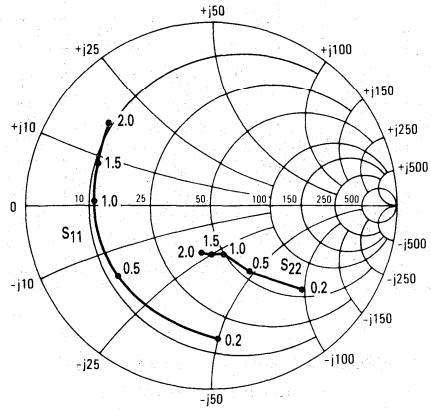


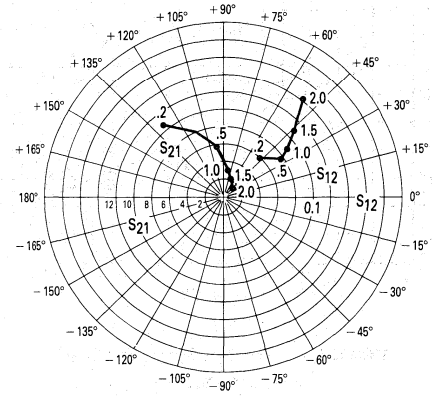
FIGURE 10 — MRF572 — $G_{U}max$ and $|S_{21}|^2$ versus FREQUENCY



MRF571
INPUT/OUTPUT REFLECTION COEFFICIENTS
versus FREQUENCY (GHz)
V_{CE} = 6.0 V, I_C = 5.0 mA



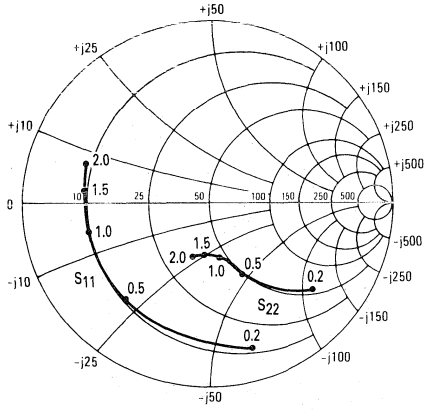
MRF571
FORWARD/REVERSE TRANSMISSION
COEFFICIENTS versus FREQUENCY (GHz)
V_{CE} = 6.0 V, I_C = 5.0 mA



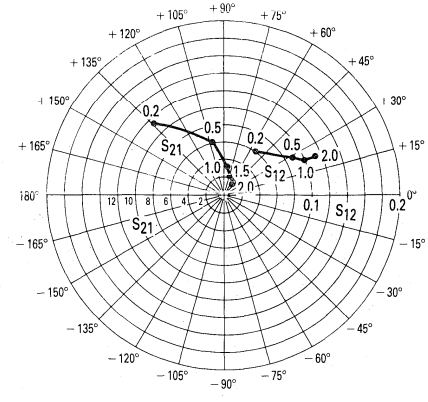
MRF571 COMMON EMITTER S-PARAMETERS

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
6.0	5.0	200	0.74	−86	10.5	129	0.06	48	0.69	−42
		500	0.62	−143	5.5	97	0.08	33	0.41	−59
		1000	0.61	178	3.0	78	0.09	37	0.28	−69
		1500	0.65	158	2.0	62	0.11	44	0.26	−88
		2000	0.70	140	1.6	51	0.14	51	0.27	−99
	10	200	0.64	−111	15	118	0.04	44	0.53	−59
		500	0.58	−160	6.9	93	0.06	42	0.27	−77
		1000	0.59	168	3.7	77	0.09	52	0.16	−91
		1500	0.63	151	2.5	64	0.12	56	0.16	−113
		2000	0.67	134	2.0	53	0.16	57	0.16	−118
	50	200	0.56	−160	20.4	102	0.02	57	0.27	−98
		500	0.57	176	8.4	86	0.05	67	0.14	−130
		1000	0.60	156	4.4	75	0.09	70	0.11	−164
		1500	0.62	152	2.9	64	0.13	68	0.13	−175
		2000	0.66	127	2.4	53	0.18	62	0.11	−178
8.0	5.0	200	0.75	−83	10.7	129	0.06	49	0.71	−39
		500	0.62	−140	5.1	98	0.08	34	0.43	−54
		1000	0.60	−179	3.7	78	0.09	38	0.31	−62
		1500	0.64	159	2.1	62	0.10	45	0.29	−80
		2000	0.69	141	1.7	52	0.13	52	0.29	−91
	10	200	0.64	−99	15.1	120	0.05	46	0.54	−60
		500	0.52	−152	7.1	94	0.07	45	0.32	−75
		1000	0.52	170	3.7	76	0.10	54	0.15	−82
		1500	0.52	150	2.5	62	0.13	56	0.16	−108
		2000	0.57	133	2.0	51	0.18	55	0.16	−107
	50	200	0.52	−153	19.6	102	0.03	56	0.28	−92
		500	0.52	178	8.1	86	0.05	67	0.16	−98
		1000	0.56	157	4.1	73	0.10	70	0.06	−130
		1500	0.54	139	2.8	62	0.13	68	0.11	−146
		2000	0.59	126	2.2	52	0.19	63	0.10	−137

MRF572
INPUT/OUTPUT REFLECTION
COEFFICIENTS versus FREQUENCY (GHz)
V_{CE} = 6.0 V, I_C = 5.0 mA



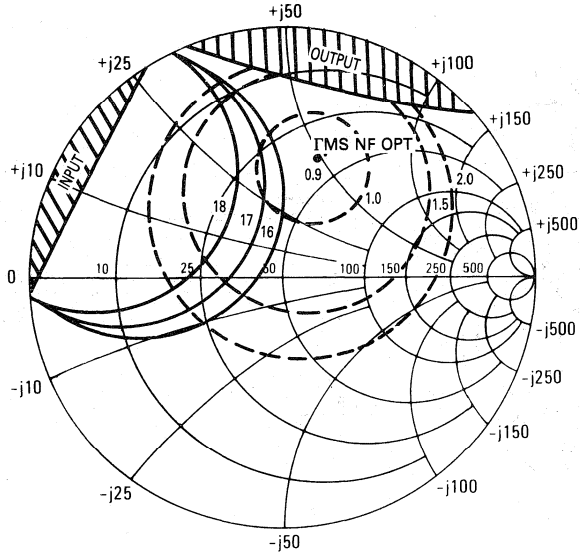
MRF572
FORWARD/REVERSE COEFFICIENTS
versus FREQUENCY (GHz)
V_{CE} = 6.0 V, I_C = 5.0 mA



MRF572 COMMON EMITTER S-PARAMETERS

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
6.0	5.0	200	0.81	−73	10.9	134	0.06	50	0.74	−40
		500	0.68	−130	6.1	102	0.09	29	0.43	−64
		1000	0.66	−167	3.3	79	0.10	22	0.29	−77
		1500	0.66	174	2.3	63	0.10	22	0.27	−94
		2000	0.68	161	1.8	49	0.11	23	0.29	−104
	10	200	0.72	−101	15.9	123	0.05	43	0.57	−58
		500	0.66	−150	7.7	95	0.06	30	0.29	−86
		1000	0.66	−178	4.0	77	0.08	33	0.19	−103
		1500	0.67	166	2.7	63	0.09	36	0.19	−122
		2000	0.69	155	2.1	51	0.10	37	0.20	−129
	50	200	0.67	−154	21.8	104	0.02	43	0.30	−94
		500	0.68	−177	9.0	87	0.03	52	0.17	−129
		1000	0.70	167	4.5	74	0.06	58	0.14	−151
		1500	0.71	157	3.0	62	0.08	59	0.16	−160
		2000	0.73	148	2.3	51	0.10	55	0.17	−161
8.0	5.0	200	0.83	−69	10.9	136	0.06	52	0.75	−36
		500	0.71	−125	6.3	103	0.08	30	0.46	−57
		1000	0.64	−164	3.5	80	0.09	24	0.31	−68
		1500	0.65	176	2.4	63	0.10	23	0.29	−84
		2000	0.66	163	1.8	49	0.11	24	0.30	−94
	10	200	0.74	−94	16.2	125	0.05	45	0.60	−51
		500	0.65	−146	7.9	96	0.06	32	0.31	−74
		1000	0.64	−176	4.2	77	0.07	33	0.20	−87
		1500	0.65	168	2.8	63	0.09	36	0.19	−104
		2000	0.67	156	2.2	50	0.10	37	0.20	−111
	50	200	0.62	−150	22.7	104	0.02	43	0.30	−81
		500	0.64	−174	9.4	86	0.03	51	0.15	−107
		1000	0.68	167	4.8	74	0.05	58	0.10	−126
		1500	0.69	160	3.2	61	0.07	58	0.13	−140
		2000	0.70	147	2.4	50	0.09	55	0.15	−140

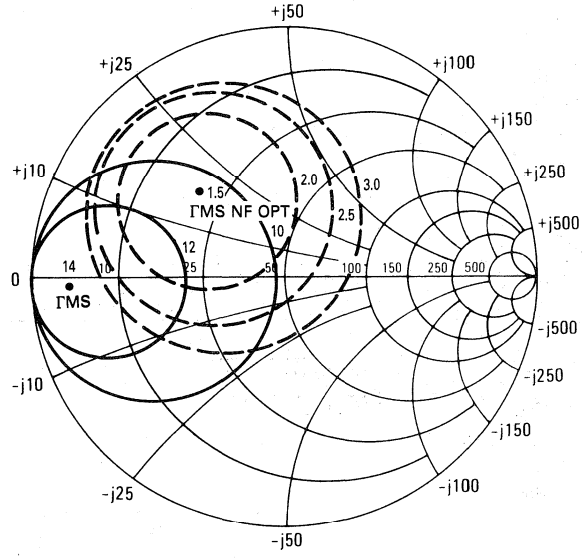
MRF571 — CONSTANT GAIN and NOISE FIGURE CONTOURS



V_{CE} = 6.0 V, I_C = 5.0 mA
f = 500 MHz
▨ — REGION OF INSTABILITY

f(GHz)	NF OPT(dB)	Rn (Ω)	NF50 Ω (dB)
0.5	0.9	9.3	1.3

ΓMS NF OPT	K
0.49 ∠74°	0.58

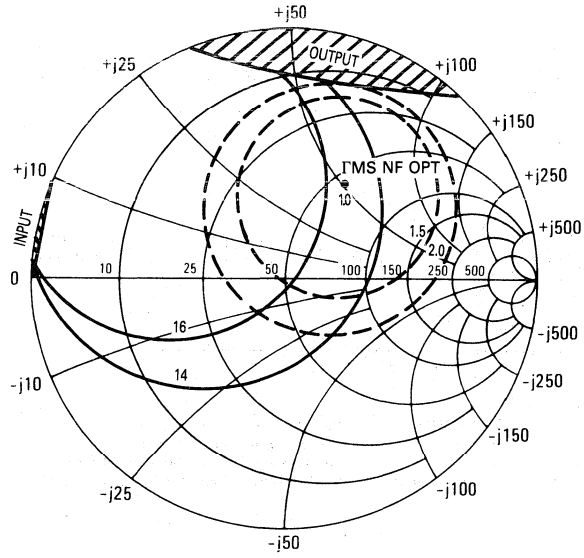


V_{CE} = 6.0 V, I_C = 5.0 mA
f = 1.0 GHz

f(GHz)	NF OPT(dB)	Rn (Ω)	NF50 Ω (dB)	ΓMS NF OPT
1.0	1.5	7.5	2.2	0.48 ∠134°

ΓMS	ΓML
0.89 ∠ − 179°	0.81 ∠66°

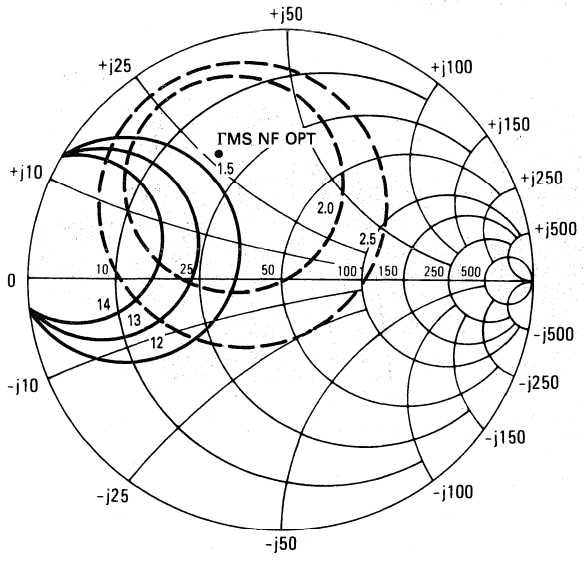
MRF572 CONSTANT GAIN and NOISE FIGURE CONTOURS



V_{CE} = 6.0 V, I = 5.0 mA
f = 500 MHz
▨ — REGION OF INSTABILITY

f(GHz)	Rn (Ω)	NF (50Ω)	ΓMS NF OPT
0.5	17.1	1.5	0.43 ∠ 57°

K	NF OPT
0.55	1.0

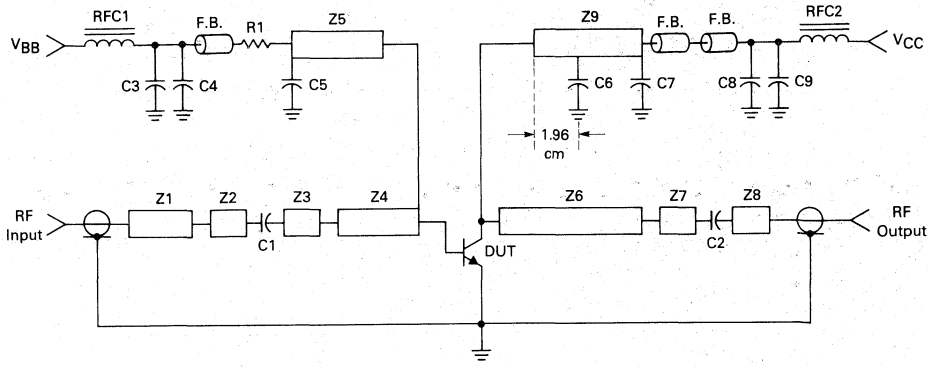


V_{CE} = 6.0 V, I_C = 5.0 mA
f = 1.0 GHz

f(GHz)	NF OPT	Rn (Ω)	NF50 (Ω) (dB)
1.0	1.5	6.0	2.0

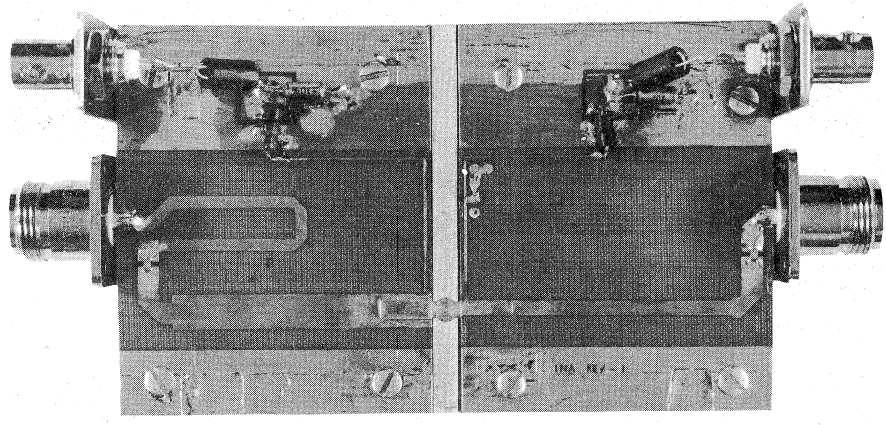
ΓMS NF OPT	K
0.56 ∠ 116°	0.93

MRF571 1.0 GHz TEST CIRCUIT

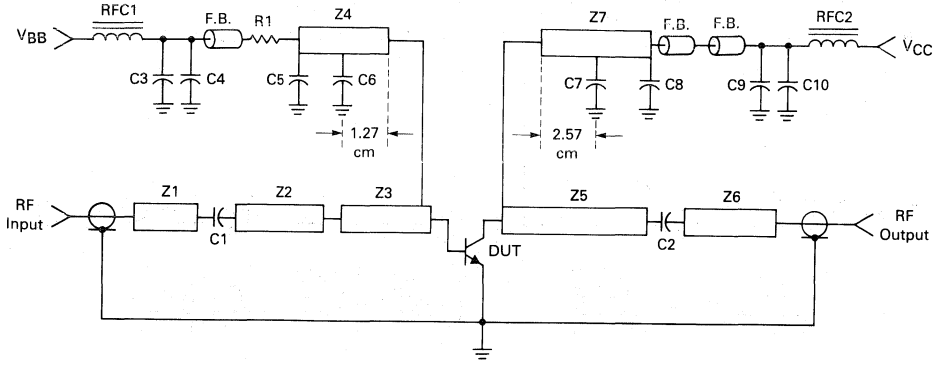


C1, C2, C6	560 pF Chip Capacitor	RFC1, RFC2	VK-200, Ferroxcube
C5, C7	0.018 μF Chip Capacitor	Z1–Z9	Microstrip, See Photomaster
C3, C8	0.1 μF Mylar Capacitor	Bead	Ferrite Bead, Ferroxcube 56-590-65/3B
C4, C9	1.0 μF Electrolytic Capacitor	Board Material	0.0625" Teflon Fiberglass $\epsilon_r = 2.5 \pm 0.05$
R1	2.7 kΩ		

MRF571 TEST CIRCUIT

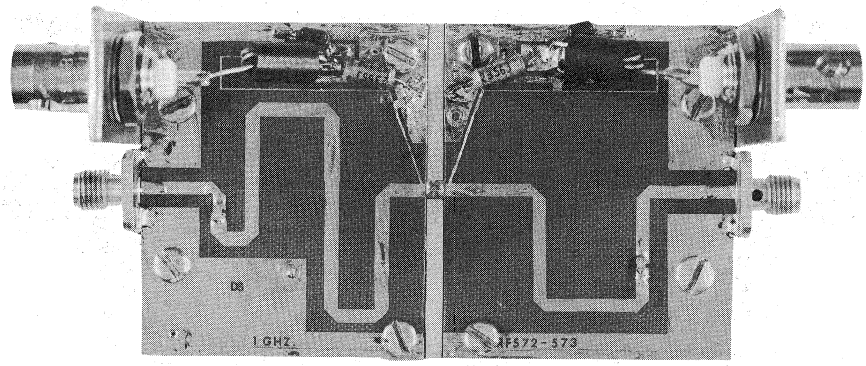


MRF572, 1.0 GHz TEST CIRCUIT

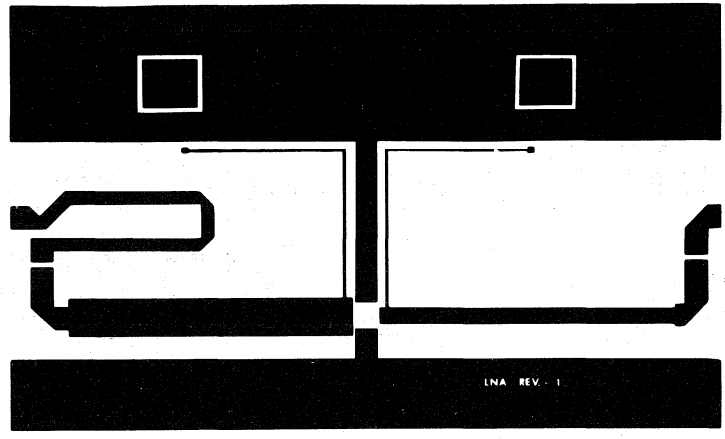


C1, C2, C6, C7	560 pF Chip Capacitor	RFC1, RFC2	VK-200, Ferroxcube
C5, C8	0.018 μF Chip Capacitor	Z1–Z7	Microstrip, See Photomaster
C3, C9	0.1 μF Mylar Capacitor	Bead	Ferrite Bead, Ferroxcube 56-590-65/3B
C4, C10	1.0 μF Electrolytic Capacitor	Board Material	0.031″ Teflon Fiberglass ϵ_r = 2.5 ± 0.05
R1	2.7 kΩ		

MRF572 TEST CIRCUIT

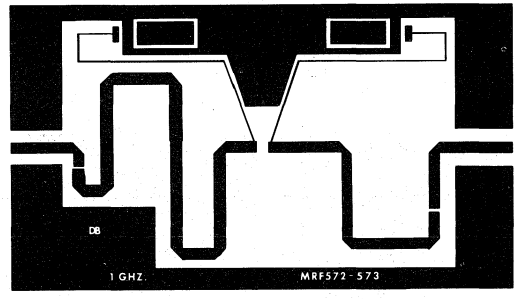


PHOTOMASTER OF MRF571 CIRCUIT LAYOUT

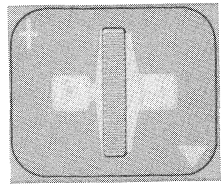


NOTE: The Printed Circuit Board shown is 75% of the original.

PHOTOMASTER OF MRF572 CIRCUIT LAYOUT



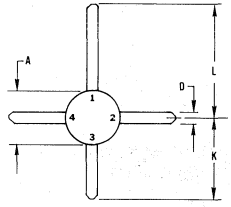
MRFC572 CHIP TOPOGRAPHY

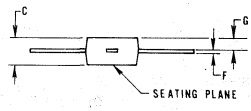


Nominal Chip Size: 0.015″ x 0.016″ x 0.005″
Front Metallization: Gold
Back Metallization: Gold
Emitter/Base Bond Pad: 2.2 x 2.2 mil
#Emitter Fingers: 22
#Base Fingers: 23
Emitter Diffusion: Ion-Implanted Arsenic

OUTLINE DIMENSIONS

4-LEAD PLASTIC MACRO-X



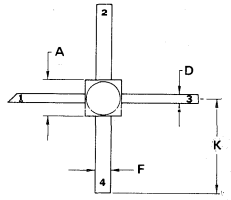


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.44	5.21	0.175	0.205
C	1.90	2.54	0.075	0.100
D	0.84	0.99	0.033	0.039
F	0.20	0.30	0.008	0.012
G	0.76	1.14	0.030	0.045
K	7.24	8.13	0.285	0.320
L	10.54	11.43	0.415	0.450

STYLE 2:
PIN 1. COLLECTOR
2. EMITTER
3. BASE
4. EMITTER

CASE 317-01

0.100" CERAMIC STRIPLINE





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.29	2.67	0.090	0.105
C	0.89	1.40	0.035	0.055
D	0.41	0.61	0.016	0.024
F	0.89	1.09	0.035	0.043
J	0.08	0.15	0.003	0.006
K	4.45	5.84	0.175	0.230

NOTE:
1. DIMENSION K APPLIES TO ALL LEADS.

STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. BASE
4. EMITTER

CASE 303-1

MRF580,A
MRF581,A
MRFC581,A

The RF Line

NPN SILICON HIGH FREQUENCY TRANSISTORS

. . . designed for high current low power amplifiers up to 1.0 GHz.

- Low Noise
- Low Intermodulation Distortion
- High Gain
- State-of-the-Art Technology
  - Fine Line Geometry
  - Arsenic Emitters
  - Gold Top Metallization
  - Nicrome Thin-Film Ballasting Resistors
- Excellent Dynamic Range
- Fully Characterized

f_T = 5.0 GHz @ 75 mA
NF = 2.0 dB @ 500 MHz

HIGH FREQUENCY TRANSISTORS

NPN SILICON

MAXIMUM RATINGS

		MRFC581,A Chip		MRF580,A Case 317A-01		MRF581,A Case 317-01		
Ratings	**Symbol**	**MRFC581**	**MRFC581A**	**MRF580**	**MRF580A**	**MRF581**	**MRF581A**	**Unit**
Collector-Emitter Voltage	V_{CEO}	18	15	18	15	18	15	Vdc
Collector-Base Voltage	V_{CBO}	36	30	36	30	36	30	Vdc
Emitter-Base Voltage	V_{EBO}	2.5		2.5		2.5		Vdc
Collector Current — Continuous	I_C	200		200		200		mAdc
Total Device Dissipation @ T_C = 50°C(1) Derate above T_C = 50°C	P_D	2.5 T_J = 200°C max		2.5 25		2.5 25		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		−65 to +150		−65 to +150		°C

NOTE 1. Case temperature measured on collector lead immediately adjacent to body of package.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	MRF580/581 MRF580A/581A	$V_{(BR)CEO}$	18 15	— —	— —	Vdc
Collector-Base Breakdown Voltage (I_C = 1.0 mAdc, I_E = 0)	MRF580/581 MRF580A/581A	$V_{(BR)CBO}$	36 30	— —	— —	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.10 mAdc, I_C = 0)		$V_{(BR)EBO}$	2.5	—	—	Vdc
Emitter Cutoff Current (V_{EB} = 2.0 Vdc, V_{BE} = 0)		I_{EBO}	—	—	100	μAdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)		I_{CBO}	—	—	100	μAdc
ON CHARACTERISTICS						
DC Current Gain(1) (I_C = 50 mAdc, V_{CE} = 5.0 Vdc)	MRF580/581 MRF580A/581A	h_{FE}	50 90	— —	200 250	—
DYNAMIC CHARACTERISTICS						
Collector Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{cb}	—	1.4	2.0	pF
Current-Gain Bandwidth Product(2) (I_C = 75 mAdc, V_{CE} = 10 Vdc, f = 1.0 GHz)		f_T	—	5.0	—	GHz
FUNCTIONAL TESTS						
Noise Figure, Figure 19 (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz)	MRF580/581 MRF580A/581A	NF	— —	2.0 1.8	3.0 2.5	dB
Power Gain at Optimum Noise Figure, Figure 19 (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz)	MRF580,A	G_{NF}	11	14	—	dB
Power Gain at Optimum Noise Figure, Figure 19 (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz)	MRF581,A	G_{NF}	13	15.5	—	dB
Maximum Unilateral Gain (I_C = 75 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz)	MRF580,A(2)	$G_{U\ max}$	—	15	—	dB
Maximum Unilateral Gain (I_C = 75 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz)	MRF581,A(2)	$G_{U\ max}$	—	17	—	dB
Intermodulation Distortion, Figure 18 (V_{CE} = 10 V, I_C = 75 mA, V_{out} = +50 dBmV)	MRF581,A(3)	IMD(d3)	—	−65	—	dB

NOTES:
1. 300 μs pulse on Tektronix 576 or equivalent.
2. Characterized on HP8542 Automatic Network Analyzer.
3. 2 Tones, f1 = 497 MHz, f2 = 503 MHz, 3rd Order Single Tone reference.

$$G_{Umax} = \frac{|S_{21}|^2}{(1 - |S_{11}|^2)(1 - |S_{22}|^2)}$$

FIGURE 1 — C_{ib} INPUT CAPACITANCE versus VOLTAGE

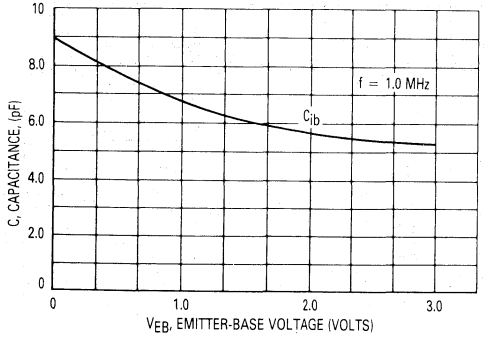


FIGURE 2 — C_{cb}, C_{ob} COLLECTOR-BASE CAPACITANCE versus VOLTAGE

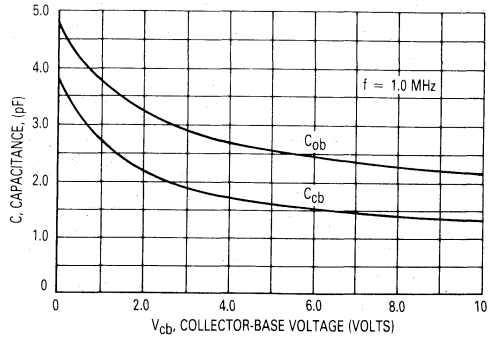


FIGURE 3 — GAIN-BANDWIDTH PRODUCT versus COLLECTOR CURRENT

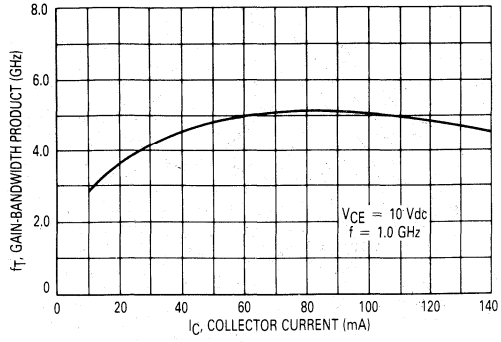
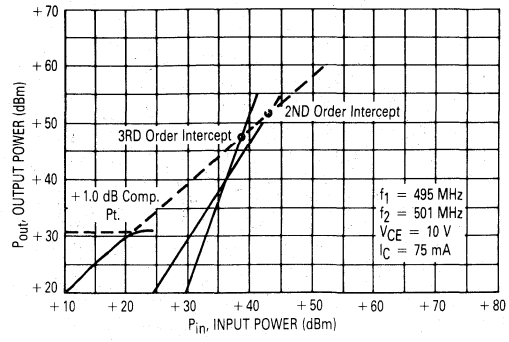


FIGURE 4 — 2ND AND 3RD ORDER INTERCEPT POINTS



MRF580,A TYPICAL PERFORMANCE

FIGURE 5 — $G_{U\ max}$-MAXIMUM UNILATERAL GAIN, $|S_{21}|^2$ versus FREQUENCY

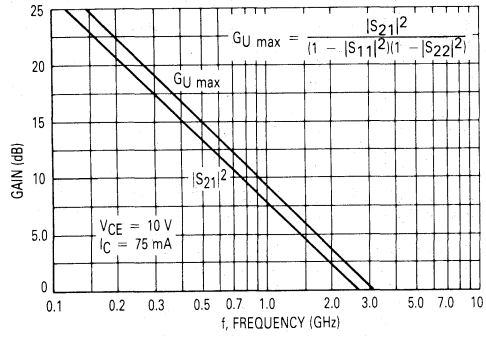


FIGURE 6 — $G_{A\ max}$, MAXIMUM AVAILABLE GAIN versus FREQUENCY

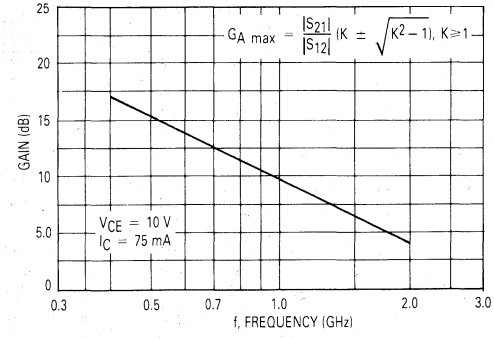


FIGURE 7 — NOISE FIGURE AND GAIN ASSOCIATED WITH NOISE FIGURE versus FREQUENCY

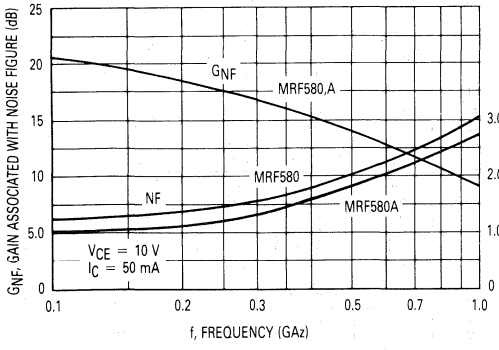


FIGURE 8 — NOISE FIGURE AND GAIN ASSOCIATED WITH NOISE FIGURE versus COLLECTOR CURRENT

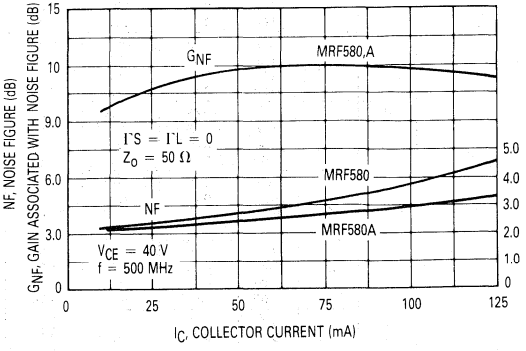
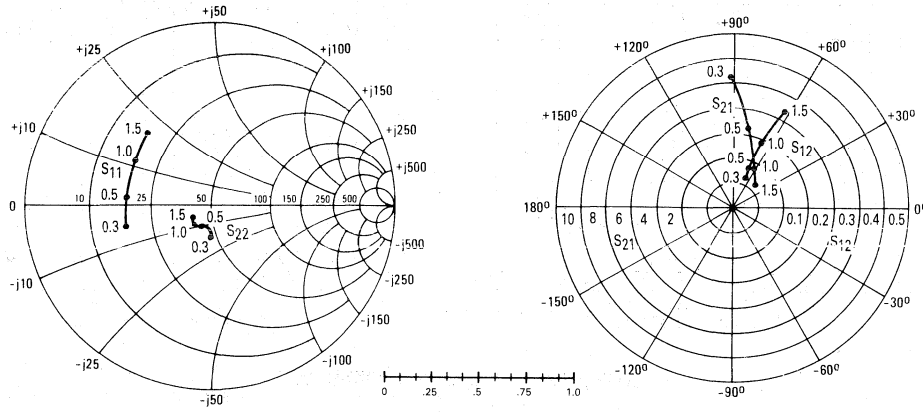


FIGURE 9 — MRF580,A COMMON EMITTER S-PARAMETERS

INPUT/OUTPUT REFLECTION COEFFICIENT versus FREQUENCY V_{CE} = 10 V I_C = 50 mA **FORWARD/REVERSE TRANSMISSION COEFFICIENTS versus FREQUENCY**



V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
5.0	25	300	0.49	−170	5.97	91	0.083	60	0.24	−108
		500	0.52	171	3.63	78	0.127	64	0.18	−117
		1000	0.53	149	1.98	58	0.24	66	0.13	−154
		1500	0.56	125	1.46	44	0.35	60	0.19	−172
	50	300	0.48	−175	6.35	90	0.08	64	0.24	−126
		500	0.51	168	3.85	79	0.13	67	0.18	−139
		1000	0.51	148	2.10	59	0.25	66	0.16	−178
		1500	0.54	123	1.56	46	0.36	58	0.20	169
	75	300	0.48	−177	6.42	90	0.08	65	0.24	−132
		500	0.51	167	3.88	79	0.13	67	0.19	−145
		1000	0.50	147	2.12	59	0.26	65	0.17	175
		1500	0.53	123	1.57	46	0.36	58	0.21	164
	100	300	0.48	−177	6.41	89	0.08	66	0.24	−134
		500	0.51	167	3.87	78	0.13	68	0.19	−148
		1000	0.51	146	2.114	59	0.26	65	0.17	172
		1500	0.53	123	1.58	46	0.36	58	0.21	162
10	25	300	0.44	−164	6.67	92	0.07	61	0.25	−76
		500	0.47	175	4.08	79	0.11	66	0.19	−75
		1000	0.48	152	2.2	60	0.21	68	0.12	−91
		1500	0.52	126	1.56	45	0.32	64	0.15	−129
	50	300	0.47	−167	7.40	91	0.07	65	0.17	−89
		500	0.47	174	4.53	79	0.11	68	0.12	−112
		1000	0.50	149	2.38	62	0.20	67	0.13	−126
		1500	0.53	131	1.71	47	0.31	63	0.11	−147
	75	300	0.41	−171	7.24	91	0.07	66	0.20	−96
		500	0.45	171	4.39	79	0.12	69	0.13	−99
		1000	0.45	150	2.36	61	0.23	67	0.07	−130
		1500	0.48	125	1.72	47	0.33	61	0.12	−157
	100	300	0.42	−172	7.22	90	0.07	67	0.19	−97
		500	0.45	170	4.38	78	0.12	69	0.14	−98
		1000	0.45	149	2.35	60	0.23	67	0.07	−129
		1500	0.49	125	1.71	46	0.33	62	0.11	−158
15	25	300	0.48	−159	7.28	93	0.06	60	0.24	−55
		500	0.48	−179	4.44	80	0.09	66	0.17	−62
		1000	0.51	153	2.33	62	0.18	68	0.19	−82
		1500	0.54	133	1.67	46	0.27	68	0.17	−97
	50	300	0.39	−165	7.49	0.92	0.07	65	0.23	−71
		500	0.42	174	4.57	80	0.11	69	0.18	−67
		1000	0.43	152	2.44	61	0.21	68	0.11	−74
		1500	0.46	126	1.76	47	0.31	64	0.12	−115
	75	300	0.39	−167	7.57	91	0.07	66	0.21	−74
		500	0.42	173	4.57	79	0.11	70	0.17	−69
		1000	0.42	151	2.45	61	0.21	68	0.09	−75
		1500	0.46	126	1.76	46	0.31	64	0.11	−118
	100	300	0.39	−168	7.46	90	0.07	67	0.20	−72
		500	0.43	172	4.53	78	0.11	70	0.17	−66
		1000	0.43	151	2.41	60	0.21	69	0.10	−71
		1500	0.47	126	1.74	46	0.31	64	0.12	−113

MRF581,A TYPICAL PERFORMANCE

FIGURE 10 — $G_{U\ max}$ — MAXIMUM UNILATERAL GAIN, $|S_{21}|^2$ versus FREQUENCY

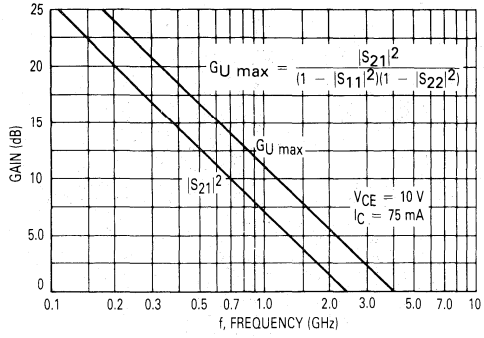


FIGURE 11 — $G_{A\ max}$, MAXIMUM AVAILABLE GAIN versus FREQUENCY

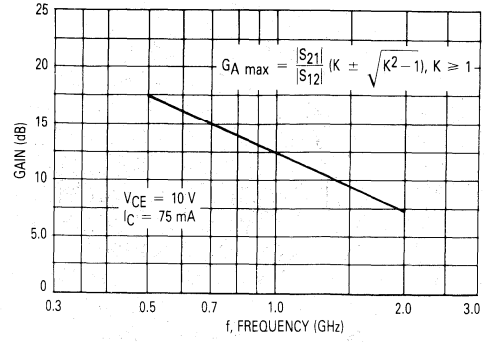


FIGURE 12 — NOISE FIGURE AND GAIN ASSOCIATED WITH NOISE FIGURE versus FREQUENCY

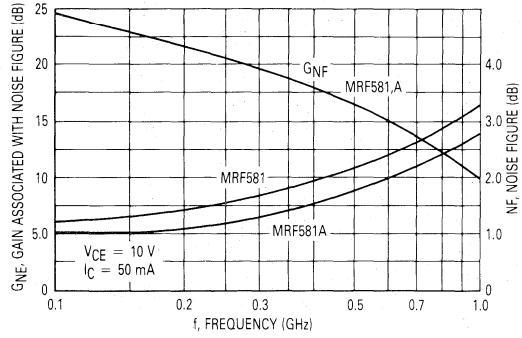


FIGURE 13 — NOISE FIGURE AND GAIN ASSOCIATED WITH NOISE FIGURE versus COLLECTOR CURRENT f = 500 MHz

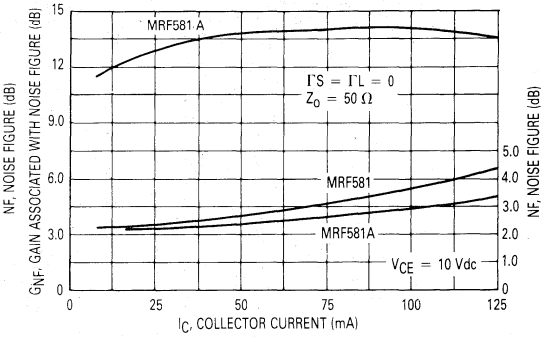


FIGURE 14 — NOISE FIGURE AND GAIN ASSOCIATED WITH NOISE FIGURE versus COLLECTOR CURRENT f = 200 MHz

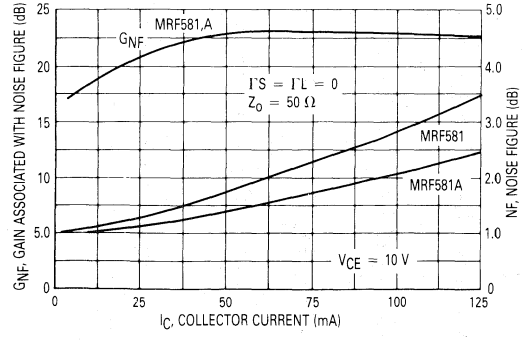


FIGURE 15 — NOISE FIGURE AND GAIN ASSOCIATED WITH NOISE FIGURE versus COLLECTOR CURRENT f = 50 MHz

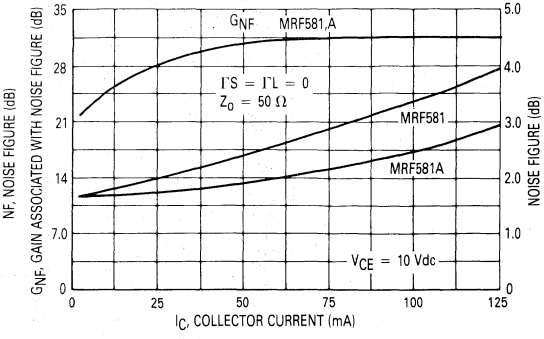
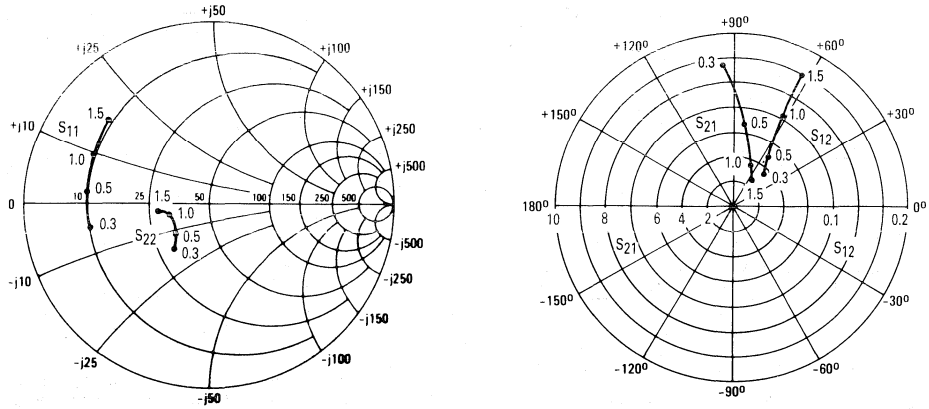


FIGURE 16 — MRF581,A COMMON EMITTER S-PARAMETERS

INPUT/OUTPUT REFLECTION COEFFICIENT versus FREQUENCY

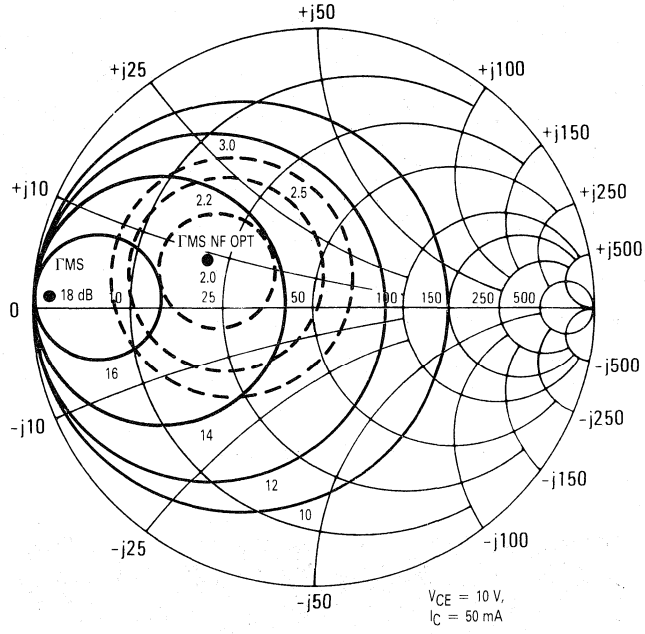
V_{CE} = 10 V, I_C = 50 mA

FORWARD/REVERSE TRANSMISSION COEFFICIENTS versus FREQUENCY



V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
5.0	25	300	0.69	−169	6.57	93	0.06	39	0.34	−129
		500	0.72	176	3.95	82	0.07	47	0.29	−142
		1000	0.73	157	2.10	62	0.12	60	0.27	−165
		1500	0.76	139	1.47	50	0.17	61	0.33	−172
	50	300	0.70	−173	7.14	93	0.05	45	0.38	−144
		500	0.72	173	4.27	82	0.07	53	0.34	−157
		1000	0.72	157	2.24	65	0.13	62	0.33	179
		1500	0.76	138	1.61	53	0.18	61	0.37	173
	75	300	0.70	−175	7.26	92	0.05	48	0.40	−148
		500	0.72	172	4.33	82	0.07	55	0.36	−161
		1000	0.72	155	2.28	65	0.13	63	0.35	176
		1500	0.76	138	1.64	53	0.19	61	0.39	170
	100	300	0.70	−176	7.30	92	0.05	48	0.40	−151
		500	0.72	172	4.34	82	0.07	56	0.37	−163
		1000	0.72	155	2.28	65	0.13	63	0.362	175
		1500	0.75	137	1.64	53	0.19	61	0.39	168
10	25	300	0.66	−165	7.58	95	0.05	40	0.29	−106
		500	0.69	178	4.56	82	0.07	48	0.23	−116
		1000	0.70	159	2.39	64	0.11	61	0.19	−141
		1500	0.74	141	1.65	50	0.16	64	0.26	−153
	50	300	0.65	−169	8.25	94	0.05	46	0.30	−126
		500	0.68	175	4.96	82	0.07	54	0.24	−138
		1000	0.69	157	2.60	65	0.12	63	0.22	−164
		1500	0.72	139	1.82	52	0.17	63	0.27	−171
	75	300	0.66	−171	8.49	93	0.05	48	0.30	−132
		500	0.68	175	5.06	82	0.07	55	0.25	−145
		1000	0.69	157	2.64	65	0.12	64	0.23	−170
		1500	0.72	139	1.86	53	0.17	63	0.27	−176
	100	300	0.66	−172	8.46	93	0.05	49	0.30	−134
		500	0.68	174	5.06	82	0.07	56	0.25	−147
		1000	0.68	157	2.64	65	0.12	64	0.23	−172
		1500	0.72	139	1.86	52	0.17	63	0.27	−177
15	25	300	0.65	−163	7.96	95	0.05	40	0.28	−92
		500	0.67	179	4.82	82	0.06	48	0.21	−98
		1000	0.68	160	2.51	63	0.10	62	0.17	−119
		1500	0.72	141	1.73	49	0.16	65	0.24	−137
	50	300	0.64	−167	8.76	94	0.0	46	0.26	−112
		500	0.66	177	5.37	82	0.06	54	0.20	−122
		1000	0.67	159	2.75	65	0.11	64	0.16	−148
		1500	0.71	141	1.91	51	0.16	64	0.22	−157
	75	300	0.64	−168	8.93	93	0.05	47	0.25	−117
		500	0.66	176	5.34	82	0.06	55	0.20	−128
		1000	0.69	158	2.78	65	0.11	65	0.16	−154
		1500	0.70	140	1.93	51	0.16	64	0.22	−162
	100	300	0.64	−169	8.91	93	0.05	48	0.25	−117
		500	0.66	176	5.33	82	0.6	56	0.19	−129
		1000	0.67	158	2.78	64	0.11	65	0.16	−154
		1500	0.70	140	1.93	51	0.16	64	0.21	−160

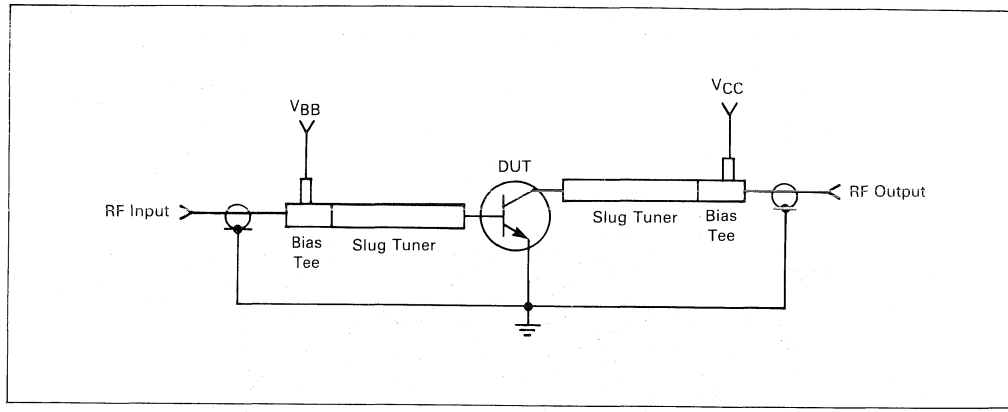
FIGURE 17 — MRF581 CONSTANT GAIN CONTOURS NOISE FIGURE CONTOURS



f(MHz)	ΓMS	ΓML	ΓMS NF OPT	G_AMAX (dB)	Rn (Ω)	NF OPT	NF (50 Ω)
500	0.91/176°	0.78/77°	0.39/159°	18	10.5	2.0	2.5

Circuit Per Figure 19

FIGURE 18 — FUNCTIONAL CIRCUIT SCHEMATIC



3

MRF580,A/581,A TEST CIRCUIT

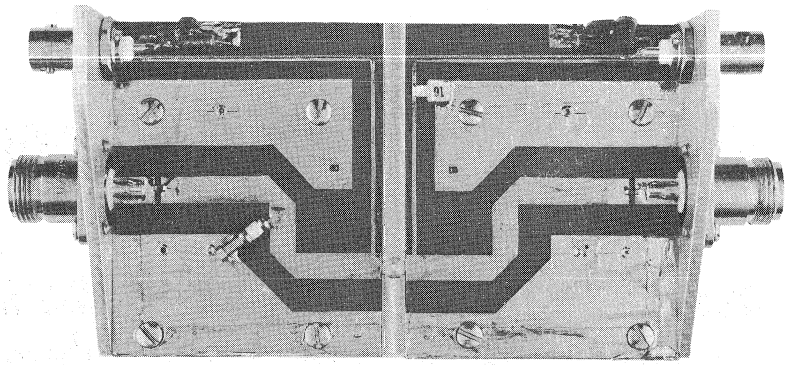
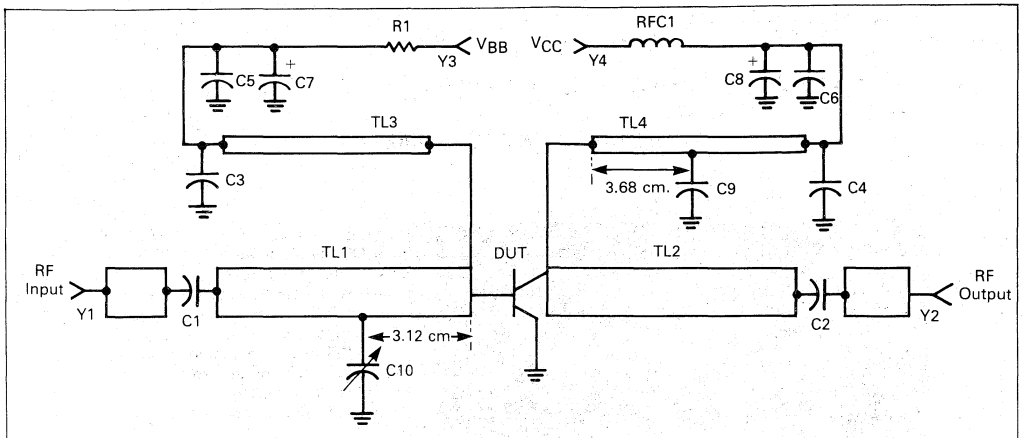


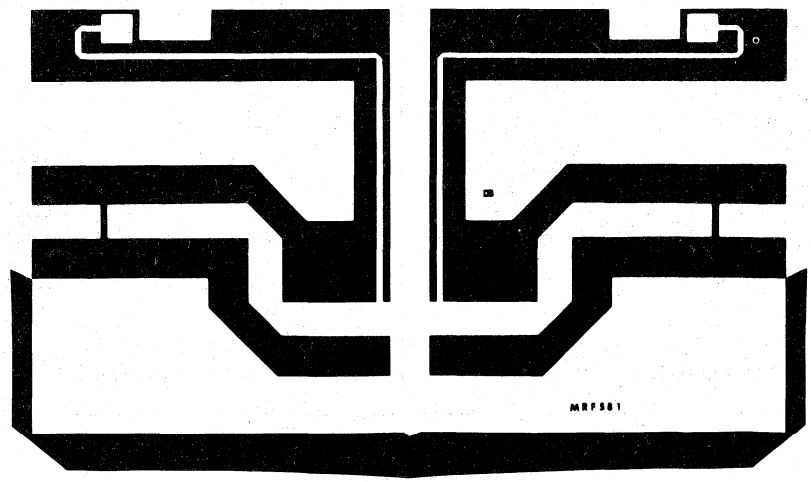
FIGURE 19 — MRF580,A/581,A TEST FIXTURE SCHEMATIC
500 MHz



C1, C2 — 470 pF Chip (Ceramic)
C3, C4 — 0.018 μF Chip Capacitor
C5, C6 — 0.1 μF Mylar
C7, C8 — 1.0 μF, 25 Vdc Electrolytic
C9 — 91 pF Mini-Unelco (C9 Taped 3.68 cm from Collector Connection on TL4 as shown)
C10 — 35–45 pF Johanson Ceramic Capacitor, JMC 5801 or Equivalent (C10 Taped 3.12 cm from Base Connection on TL1)

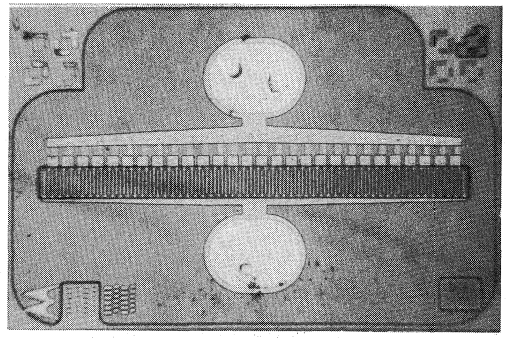
R1 — 2.7 kΩ, 1½ W
RFC1 — 0.15 μH Molded Choke
TL1, TL2 — Z_O = 26 Ω, 0.0625 TFG as shown in Photomaster
TL3, TL4 — λ/4 Microstrip, Z_O = 100 Ω
Y1, Y2 — N-Type Connection (Female)
Y3, Y4 — BNC-Type Connector (Female)
Board Material — 0.0625″ Thick Glass Teflon ϵ_r = 2.5

FIGURE 20 — PC BOARD PHOTOMASTER



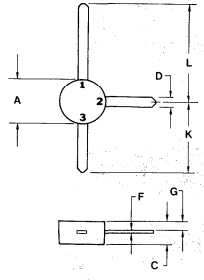
NOTE: The Printed Circuit Board shown is 75% of the original.

MRFC581,A CHIP TOPOGRAPHY



Nominal Chip Size: 0.017″ X 0.027″ X 0.005″
Front Metallization: Gold
Back Metallization: Gold
Emitter/Base Bond Pad: 0.003″ X 0.004″
#Emitter Fingers: 56
#Base Fingers: 57
Emitter Diffusion: Ion-Implanted Arsenic
Fabrication: Fully Ion Implanted
Ballasting: NiCr Resistor
Passivation: Silicon Nitride

3-LEAD PLASTIC MACRO-T

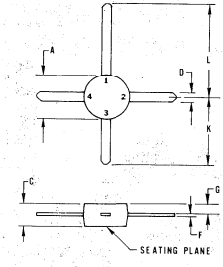


STYLE 2:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.44	5.21	0.175	0.205
C	1.90	2.54	0.075	0.100
D	0.94	0.99	0.033	0.039
F	0.20	0.30	0.008	0.012
G	0.76	1.14	0.030	0.045
K	7.24	8.13	0.285	0.320
L	10.54	11.43	0.415	0.450

CASE 317A-01

4-LEAD PLASTIC MACRO-X



STYLE 2:
PIN 1. COLLECTOR
2. EMITTER
3. BASE
4. EMITTER

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.44	5.21	0.175	0.205
C	1.90	2.54	0.075	0.100
D	0.84	0.99	0.033	0.039
F	0.20	0.30	0.008	0.012
G	0.76	1.14	0.030	0.045
K	7.24	8.13	0.285	0.320
L	10.54	11.43	0.415	0.450

CASE 317-01

MRF586
MRF587

Designer's Data Sheet

The RF Line

NPN SILICON HIGH FREQUENCY TRANSISTORS

. . . designed for use in high-gain, low-noise, ultra-linear, tuned and wideband amplifiers. Ideal for use in CATV, MATV, and instrumentation applications.

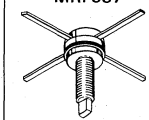
- Low Noise Figure —
  NF = 3.0 dB (Typ) @ f = 500 MHz, I_C = 90 mA
- High Power Gain —
  $G_{U(max)}$ = 16.5 dB (Typ) @ f = 500 MHz
- Ion Implanted
- All Gold Metal System
- High f_T–4.5 GHz MRF586
  5.5 GHz MRF587
- Low Intermodulation Distortion:
  TB_3 = –70 dB
  DIN = 125 dB μV

NF = 3.0 dB @ 0.5 GHz

HIGH FREQUENCY TRANSISTORS

NPN SILICON

3

MAXIMUM RATINGS		MRF586  Case 79-02	MRF587  Case 244A-01	
Ratings	**Symbol**	**Values**		**Unit**
Collector-Emitter Voltage	V_{CEO}	17	17	Vdc
Collector-Base Voltage	V_{CBO}	34	34	Vdc
Emitter-Base Voltage	V_{EBO}	2.5	2.5	Vdc
Collector Current — Continuous	I_C	200	200	mAdc
Total Device Dissipation @ T_C = 50°C Derate above T_C = 50°C	P_D	2.5 17	5.0 33	Watts mW/°C
Storage Temperature Range	T_{stg}	–65 to +200	–65 to +150	°C
Junction Temperature	T_J	200	200	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)		$V_{(BR)CEO}$	17	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 1.0 mAdc, I_E = 0)		$V_{(BR)CBO}$	34	—	—	Vdc
Emitter-Base Breakdown Voltage (I_C = 0, I_E = 0.1 mAdc)		$V_{(BR)EBO}$	2.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)		I_{CBO}	—	—	50	μAdc
ON CHARACTERISTICS						
DC Current Gain (1) (I_C = 50 mAdc, V_{CE} = 5.0 Vdc)		h_{FE}	50	—	200	—
DYNAMIC CHARACTERISTICS						
Current-Gain — Bandwidth Product (2) (I_C = 90 mAdc, V_{CE} = 15 Vdc, f = 0.5 GHz)	MRF586 MRF587	f_T	— —	4.5 5.5	— —	GHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{cb}	—	1.7	2.2	pF
FUNCTIONAL TESTS						
Narrow Band — Figure 23 (I_C = 90 mA, V_{CC} = 15 V, f = 0.5 GHz)						dB
Noise Figure		NF	—	3.0	4.0	
Power Gain at Optimum Noise Figure	MRF586 MRF587	G_{NF}	9.0 11.0	11.0 13.0	— —	
Broad Band — Figures 24 and 25 (I_C = 90 mA, V_{CC} = 15 V, f = 0.3 GHz)						dB
Noise Figure	MRF586 MRF587	NF	— —	5.5 6.3	— —	
Power Gain at Optimum Noise Figure	MRF586 MRF587	G_{NF}	— —	10.0 11.0	— —	
Triple Beat Distortion (I_C = 50 mA, V_{CC} = 15 V, P_{Ref} = 50 dBmV) (I_C = 90 mA, V_{CC} = 15 V, P_{Ref} = 50 dBmV)	MRF586 MRF587	TB_3	— —	-65 -70	— —	dB
DIN 45004 (I_C = 90 mA, V_{CC} = 15 V) (I_C = 90 mA, V_{CC} = 15 V)	MRF586 MRF587	DIN	— —	120 125	— —	dBμV
Maximum Available Power Gain (3) (I_C = 90 mA, V_{CE} = 15 Vdc, f = 0.5 GHz)	MRF586 MRF587	G_{Umax}	— —	14.5 16.5	— —	dB

NOTES:
1. 300 μs pulse on Tektronix 576 or equivalent.
2. Characterized on HP8542 Automatic Network Analyzer.
3. $G_{Umax} = \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)}$

FIGURE 1 — TYPICAL NOISE FIGURE AND ASSOCIATED GAIN versus FREQUENCY

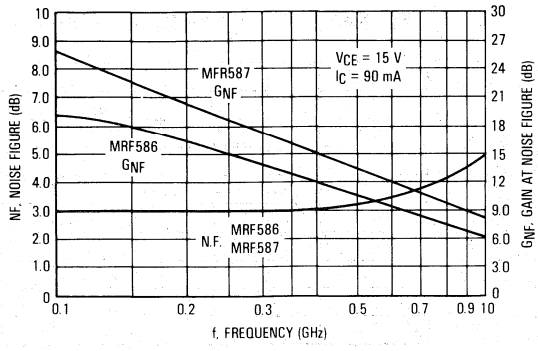


FIGURE 2 — NOISE FIGURE versus COLLECTOR CURRENT

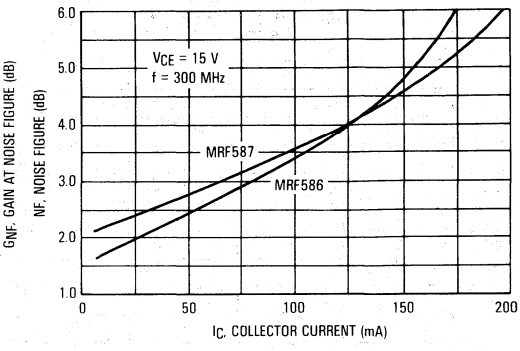


FIGURE 3 — G_{Umax} versus COLLECTOR CURRENT

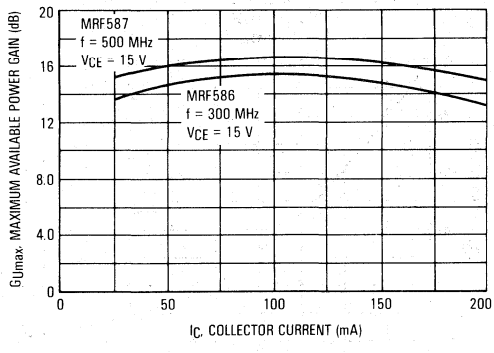
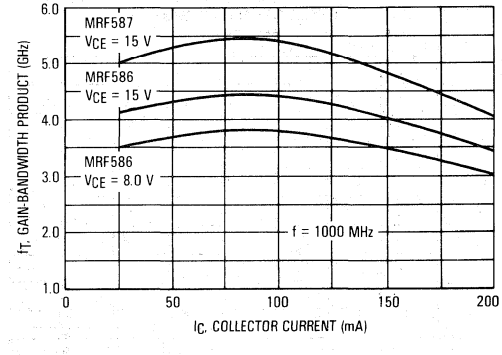


FIGURE 4 — GAIN-BANDWIDTH PRODUCT versus COLLECTOR CURRENT



MRF586 TYPICAL PERFORMANCE

FIGURE 5 — BROADBAND NOISE FIGURE MRF586

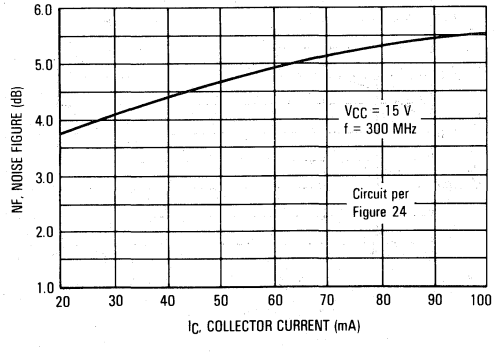
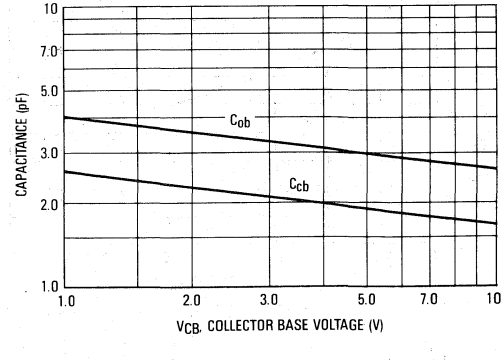


FIGURE 6 — JUNCTION CAPACITANCE versus VOLTAGE MRF586



3

MRF586 TYPICAL PERFORMANCE (continued)

FIGURE 7 — 1.0 dB COMPRESSION POINT versus COLLECTOR CURRENT
MRF586

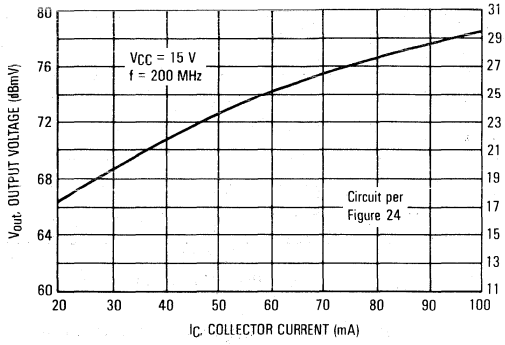


FIGURE 8 — THIRD ORDER INTERCEPT POINT
MRF586

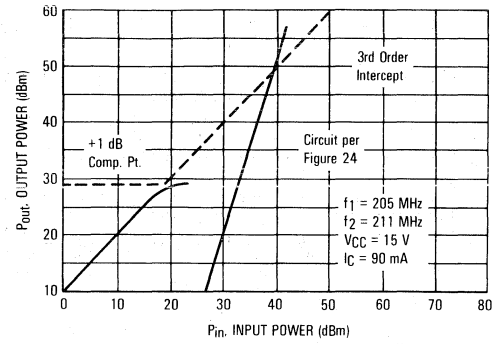


FIGURE 9 — SECOND ORDER DISTORTION versus COLLECTOR CURRENT
MRF586

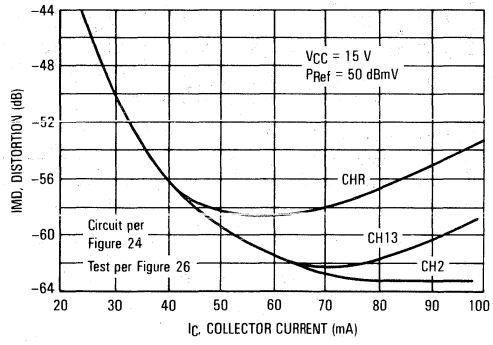


FIGURE 10 — TRIPLE BEAT DISTORTION versus COLLECTOR CURRENT
MRF586

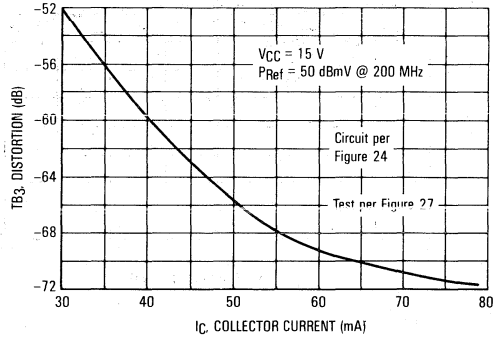


FIGURE 11 — 35-CHANNEL X-MODULATION DISTORTION versus COLLECTOR CURRENT
MRF586

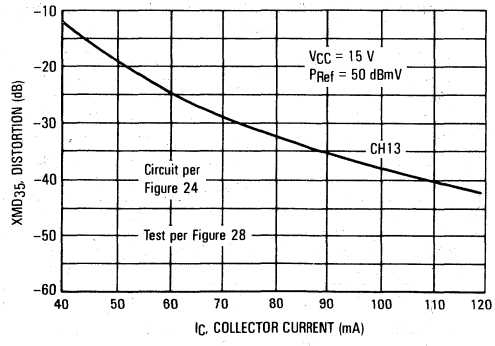


FIGURE 12 — DIN45004B versus COLLECTOR CURRENT
MRF586

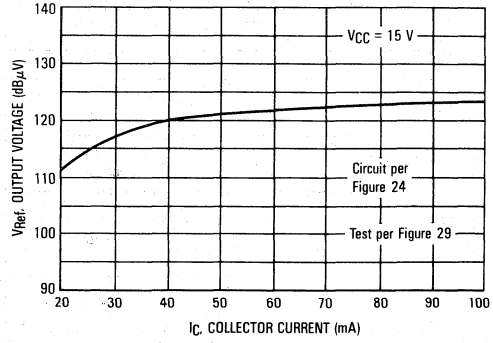
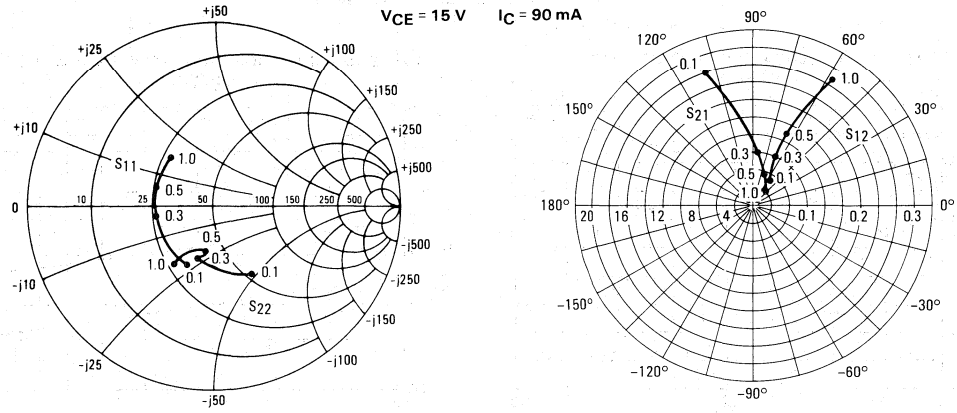


FIGURE 13 — MRF586 COMMON-EMITTER S-PARAMETERS

INPUT/OUTPUT REFLECTION COEFFICIENT versus FREQUENCY (GHz)

FORWARD/REVERSE TRANSMISSION COEFFICIENTS versus FREQUENCY (GHz)



V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
5.0	30	100	0.42	-122	13.45	109	0.05	54	0.45	-74
		300	0.39	-175	5.10	84	0.09	58	0.30	-105
		500	0.41	162	3.11	71	0.16	60	0.32	-125
		1000	0.42	131	1.68	47	0.28	56	0.38	-138
	60	100	0.39	-131	14.35	106	0.05	56	0.41	-84
		300	0.37	180	5.27	83	0.11	62	0.28	-130
		500	0.39	158	3.22	72	0.17	62	0.32	-134
		1000	0.39	127	1.75	49	0.29	55	0.36	-144
	90	100	0.39	-134	14.45	106	0.05	56	0.42	-87
		300	0.38	176	5.27	82	0.11	60	0.33	-132
		500	0.39	155	3.19	70	0.16	59	0.37	-136
		1000	0.36	120	1.70	43	0.28	49	0.45	-143
10	30	100	0.41	-112	14.40	111	0.05	55	0.48	-63
		300	0.35	-170	5.51	85	0.10	60	0.28	-100
		500	0.37	164	3.35	72	0.15	61	0.32	-109
		1000	0.38	132	1.79	47	0.26	58	0.40	-125
	60	100	0.37	-119	15.35	109	0.05	58	0.43	-70
		300	0.33	-174	5.76	84	0.10	62	0.26	-103
		500	0.35	160	3.50	73	0.16	62	0.31	-117
		1000	0.36	128	1.88	49	0.27	57	0.37	-130
	90	100	0.36	-123	15.68	107	0.05	57	0.44	-77
		300	0.33	180	5.78	83	0.10	61	0.32	-117
		500	0.34	154	3.44	70	0.15	59	0.39	-122
		1000	0.31	118	1.84	43	0.25	51	0.49	-133
15	30	100	0.42	-107	14.72	111	0.05	55	0.49	-58
		300	0.33	-167	5.64	85	0.09	60	0.28	-92
		500	0.35	166	3.48	73	0.14	61	0.32	-102
		1000	0.37	133	1.82	47	0.25	59	0.40	-119
	60	100	0.37	-112	15.80	109	0.05	57	0.45	-64
		300	0.31	-171	5.90	85	0.10	63	0.26	-100
		500	0.33	162	3.60	73	0.15	63	0.30	-108
		1000	0.35	130	1.92	49	0.27	58	0.38	-124
	90	100	0.37	-114	16.04	109	0.05	56	0.45	-67
		300	0.31	-173	5.96	84	0.10	61	0.30	-108
		500	0.32	155	3.56	70	0.15	61	0.35	-114
		1000	0.33	120	1.84	45	0.25	55	0.44	-127

MRF587 TYPICAL PERFORMANCE

FIGURE 14 — BROADBAND NOISE FIGURE
MRF587

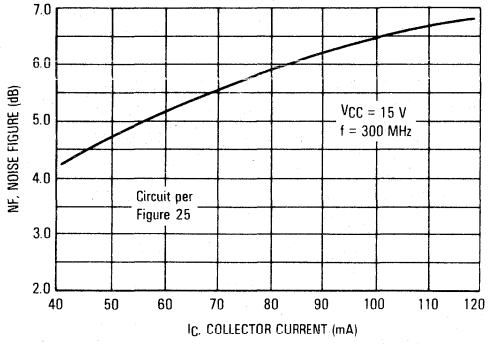


FIGURE 15 — JUNCTION CAPACITANCE versus VOLTAGE
MRF587

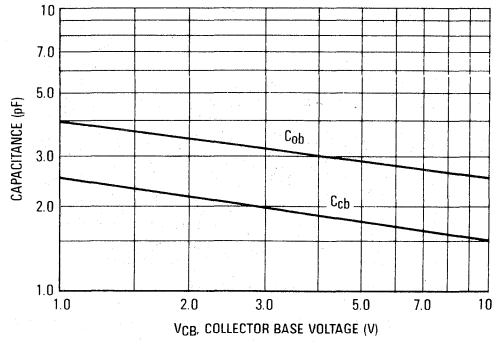


FIGURE 16 — 1.0 dB COMPRESSION POINT versus COLLECTOR CURRENT
MRF587

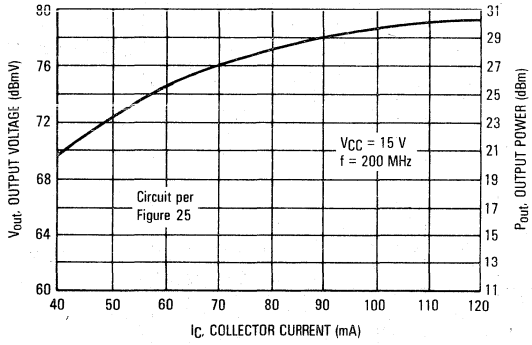
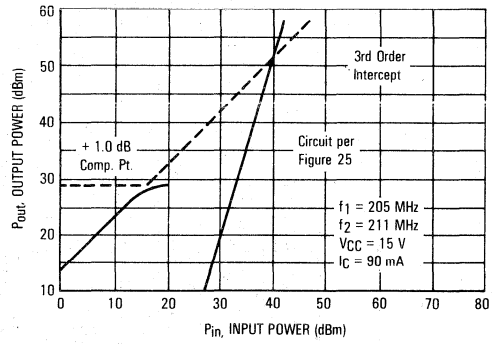


FIGURE 17 — THIRD ORDER INTERCEPT POINT
MRF587



3

MRF587 TYPICAL PERFORMANCE (continued)

FIGURE 18 — SECOND ORDER DISTORTION versus COLLECTOR CURRENT MRF587

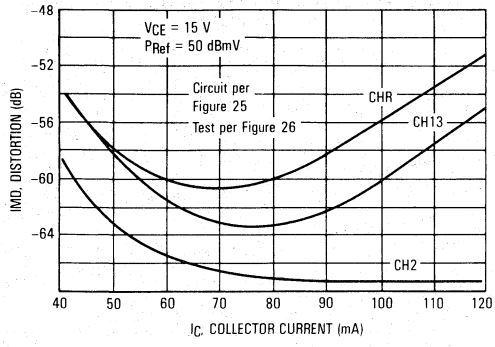


FIGURE 19 — TRIPLE BEAT DISTORTION versus COLLECTOR CURRENT MRF587

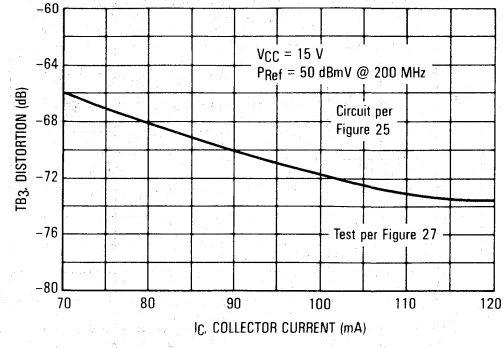


FIGURE 20 — 35-CHANNEL X-MODULATION DISTORTION versus COLLECTOR CURRENT MRF587

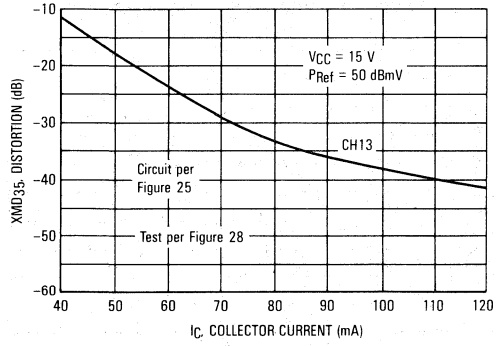
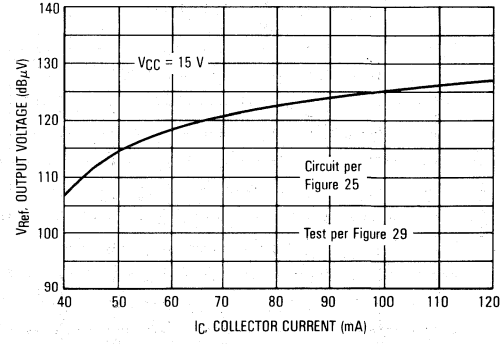


FIGURE 21 — DIN 45004B versus COLLECTOR CURRENT MRF587



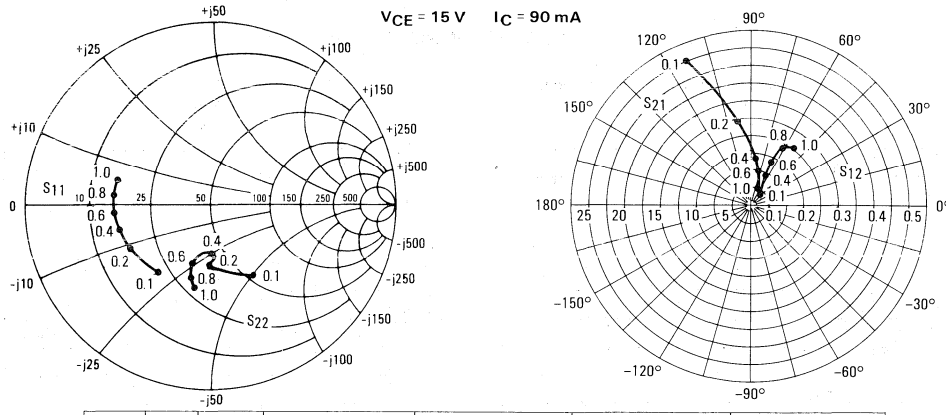
3

FIGURE 22 — MRF587 COMMON-EMITTER S-PARAMETERS

INPUT/OUTPUT REFLECTION COEFFICIENT versus FREQUENCY (GHz)

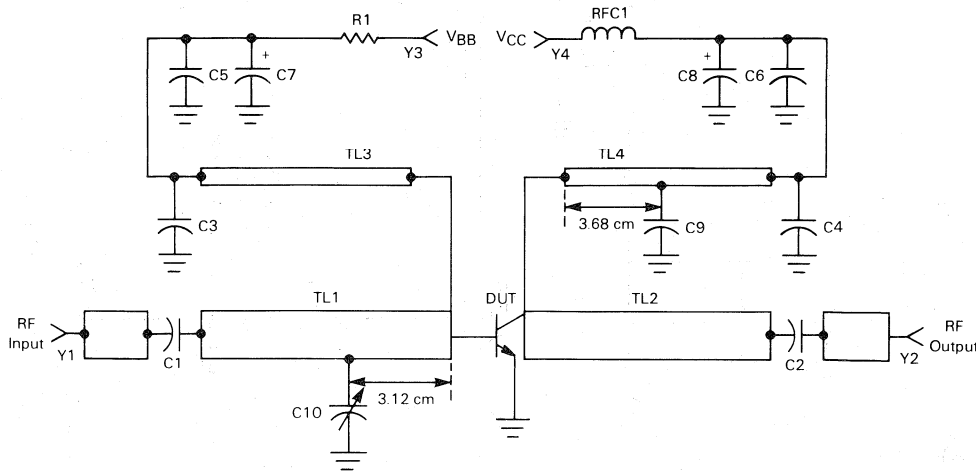
FORWARD/REVERSE TRANSMISSION COEFFICIENTS versus FREQUENCY (GHz)

V_{CE} = 15 V I_C = 90 mA



V_{CE} (Volts)	I_C (mA)	Freq (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
5.0	30	100	0.56	-131	16.45	113	0.04	45	0.49	-91
		200	0.58	-159	9.42	98	0.06	49	0.38	-116
		400	0.60	-178	5.00	86	0.08	55	0.35	-132
		600	0.64	170	3.61	76	0.11	56	0.38	-138
		800	0.67	162	2.92	67	0.14	55	0.41	-144
		1000	0.70	155	2.55	58	0.17	54	0.44	-152
	60	100	0.53	-141	17.89	110	0.04	50	0.47	-102
		200	0.56	-164	10.05	97	0.05	55	0.39	-126
		400	0.59	178	5.31	85	0.09	60	0.38	141
		600	0.63	169	3.82	76	0.12	59	0.40	-146
		800	0.66	161	3.09	67	0.15	57	0.44	-153
		1000	0.69	155	2.67	58	0.18	55	0.47	-160
	90	100	0.52	-145	18.26	109	0.04	52	0.47	-106
		200	0.56	-166	10.20	96	0.05	57	0.39	-130
		400	0.59	177	5.38	85	0.09	62	0.39	-144
		600	0.63	168	3.86	76	0.12	60	0.41	-149
		800	0.66	161	3.12	67	0.15	58	0.45	-155
		1000	0.69	155	2.70	58	0.19	55	0.48	-162
10	30	100	0.53	-122	18.36	115	0.04	48	0.50	-75
		200	0.53	-153	10.63	100	0.05	51	0.36	-96
		400	0.55	175	5.71	87	0.08	57	0.33	-112
		600	0.59	173	4.16	78	0.10	58	0.35	-119
		800	0.62	165	3.37	68	0.13	57	0.39	-127
		1000	0.65	158	2.95	59	0.15	55	0.42	-136
	60	100	0.49	-132	20.19	112	0.03	51	0.46	-85
		200	0.51	-158	11.54	99	0.05	57	0.35	-107
		400	0.53	-178	6.12	87	0.08	61	0.33	-123
		600	0.58	171	4.43	78	0.11	60	0.36	-129
		800	0.60	164	3.58	68	0.14	59	0.40	-136
		1000	0.63	157	3.12	60	0.16	57	0.44	-144
	90	100	0.48	-135	20.82	111	0.03	53	0.45	-88
		200	0.50	-160	11.77	98	0.05	59	0.34	-111
		400	0.53	-179	6.22	86	0.08	63	0.33	-126
		600	0.57	171	4.50	78	0.11	62	0.36	-131
		800	0.60	164	3.64	68	0.14	59	0.41	-139
		1000	0.63	157	3.18	60	0.17	57	0.44	-147
15	30	100	0.49	-112	20.34	118	0.04	54	0.51	-52
		200	0.52	-145	11.51	101	0.05	56	0.36	-77
		400	0.48	-164	6.12	87	0.09	63	0.32	-74
		600	0.52	-174	4.19	75	0.12	62	0.32	-90
		800	0.53	177	3.29	68	0.16	61	0.38	-90
		1000	0.53	168	2.76	61	0.20	56	0.47	-90
	60	100	0.45	-122	22.14	115	0.03	56	0.45	-60
		200	0.49	-150	12.24	99	0.05	60	0.33	-86
		400	0.45	-166	6.45	86	0.09	65	0.30	-83
		600	0.50	-175	4.42	75	0.13	63	0.32	-99
		800	0.51	177	3.47	68	0.16	61	0.38	-98
		1000	0.51	168	2.91	62	0.20	55	0.46	-96
	90	100	0.44	-127	22.76	114	0.03	58	0.43	-62
		200	0.48	-152	12.44	98	0.05	62	0.32	-89
		400	0.44	-167	6.55	85	0.09	66	0.29	-85
		600	0.50	-176	4.47	75	0.13	64	0.32	-102
		800	0.51	176	3.51	69	0.17	61	0.38	-100
		1000	0.51	168	2.95	62	0.20	55	0.46	-98

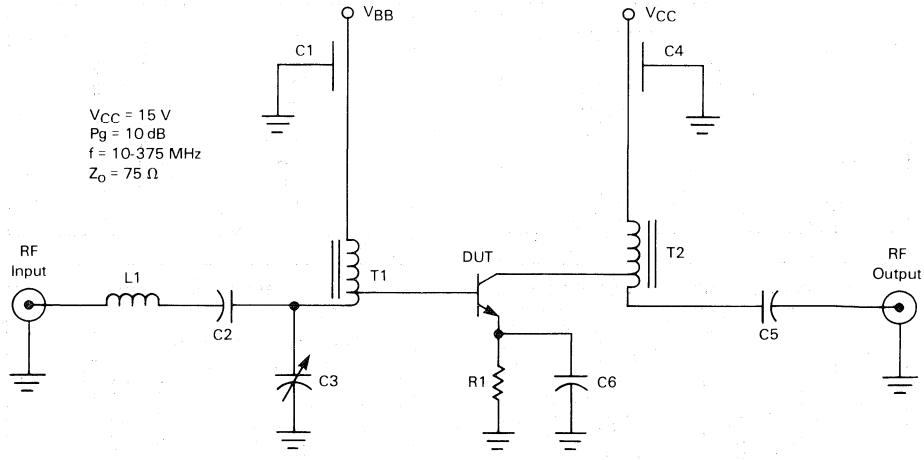
FIGURE 23 — MRF586/587 NARROW BAND TEST FIXTURE SCHEMATIC
500 MHz



C1, C2 — 470 pF Chip (Ceramic)
C3, C4 — 0.018 μF Chip Capacitor
C5, C6 — 0.1 μF Mylar
C7, C8 — 1.0 μF, 25 Vdc Electrolytic
C9 — 91 pF Mini-Unelco (C9 Taped 3.68 cm from Collector Connection on TL4 as shown)
C10 — 35-45 pF Johanson Cerami Capacitor, JMC 5801 or Equivalent (C10 Taped 3.12 cm from Base Connection on TL1)

R1 — 2.7 kΩ, 1½ W
RFC1 — 0.15 μH Molded Choke
TL1, TL2 — Z_o = 26 Ω, 0.0625 TFG as shown in Photomaster
TL3, TL4 — λ/4 Microstrip, Z_o = 100 Ω
Y1, Y2 — N-Type Connection (Female)
Y3, Y4 — BNC-Type Connector (Female)
Board Material — 0.0625" Thick Glass Teflon ϵ_r = 2.5

FIGURE 24 — MRF586 BROADBAND TEST CIRCUIT SCHEMATIC



C1, C4 — 0.01 μF Feedthru
C2, C5 — 0.001 μF
C3 — 0.5-10 pF
C6 — 12 pF

L1 — 1 Turn ⅛" I.D. #20 AWG
R1 — 13 Ω ½ W
T1(1) — 12 Turns Tapped at 4 Turns #30 AWG
T2(1) — 10 Turns Tapped at 2 Turns #30 AWG

(1) Ferronics 12-340-k Core

FIGURE 25 — MRF587 BROADBAND TEST CIRCUIT SCHEMATIC

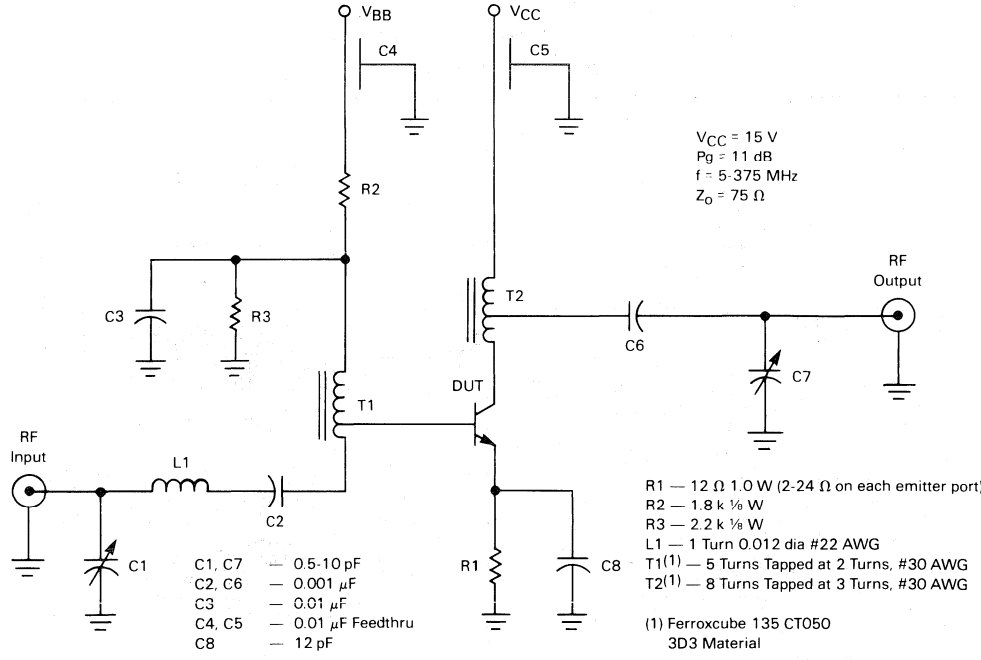


FIGURE 26 — SECOND ORDER DISTORTION TEST

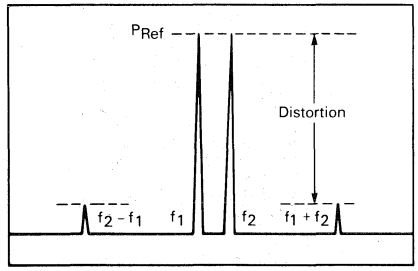


FIGURE 27 — TRIPLE BEAT DISTORTION TEST

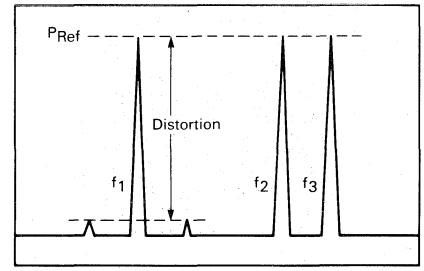


FIGURE 28 — CROSSMODULATION DISTORTION TEST

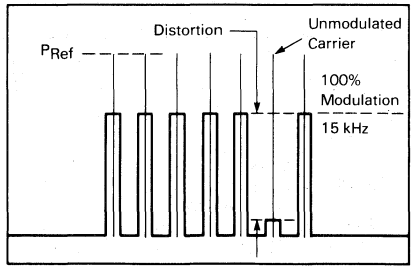
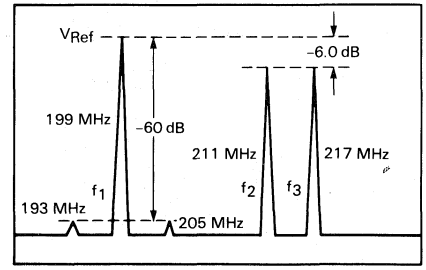
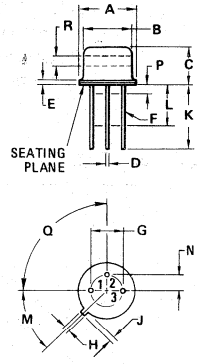


FIGURE 29 — DIN 45004B INTERMODULATION TEST



OUTLINE DIMENSIONS

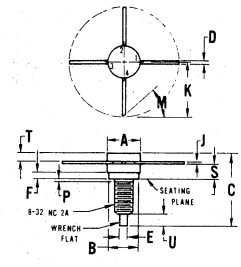


STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02



STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.06	7.26	0.278	0.286
B	6.20	6.50	0.244	0.256
C	15.24	16.51	0.600	0.650
D	0.66	0.86	0.026	0.034
E	1.40	1.65	0.055	0.065
F	1.52	–	0.060	–
J	0.10	0.15	0.004	0.006
K	11.17	–	0.440	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
S	2.74	3.35	0.108	0.132
T	1.40	1.78	0.055	0.070
U	2.92	3.68	0.115	0.145

CASE 244A-01

3

MRF604

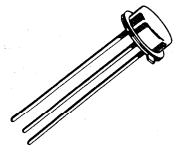
The RF Line

1.0 W – 175 MHz
RF POWER
TRANSISTOR
NPN SILICON

NPN SILICON RF POWER TRANSISTOR

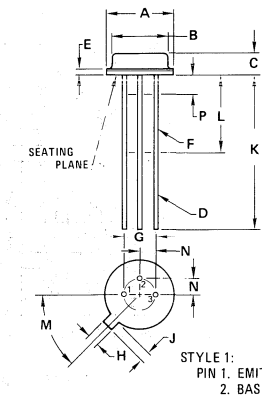
. . . designed for 12.5 Volt VHF large-signal amplifier applications in industrial equipment with restricted available space.

- Specified 12.5 Volt, 175 MHz Characteristics –
  Output Power = 1.0 Watt
  Minimum Gain = 10 dB
  Efficiency = 50%



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CBO}	40	Vdc
Emitter-Base Voltage	V_{EBO}	2.0	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	2.0 11.0	Watts mW/°C
Storage Temperature Range	T_{stg}	−65 to +200	°C



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	1.65	2.16	0.065	0.085
D	0.406	0.533	0.016	0.021
E	–	1.02	–	0.040
F	0.305	0.483	0.012	0.019
G	2.54 BSC		0.100 BSC	
H	0.914	1.17	0.036	0.046
J	0.711	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

All JEDEC dimensions and notes apply

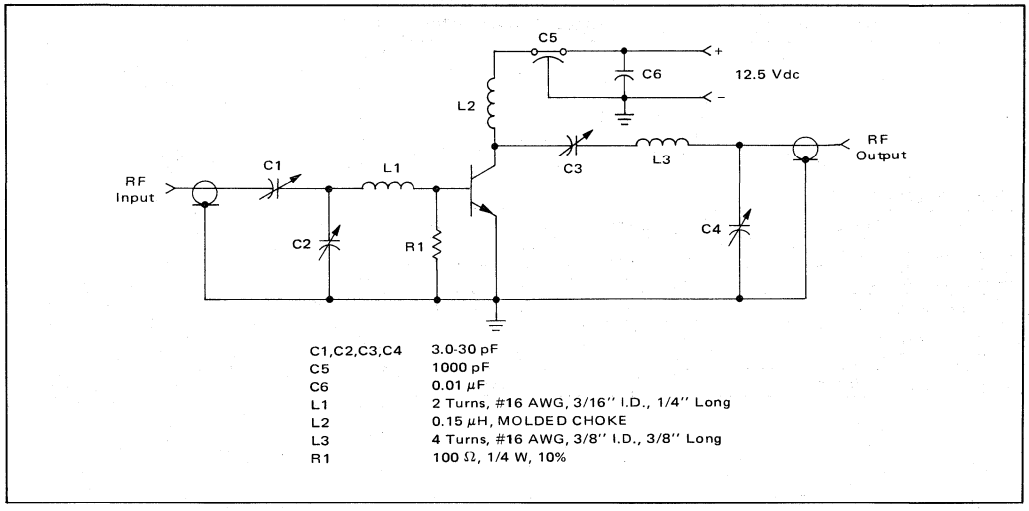
CASE 26-03
TO-46

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	$V_{(BR)CBO}$	40	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	–	–	Vdc
Collector Cutoff Current (V_{CE} = 12 Vdc, I_B = 0)	I_{CEO}	–	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 50 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	20	80	200	–
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 200 MHz)	f_T	800	–	–	MHz
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	–	3.5	pF
FUNCTIONAL TESTS (Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 1.0 W, f = 175 MHz)	G_{PE}	10	–	–	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 1.0 W, f = 175 MHz)	η	50	–	–	%
Series Equivalent Input Impedance (V_{CC} = 12.5 Vdc, P_{out} = 1.0 W, f = 175 MHz)	Z_{in}	–	7.5-j 14	–	Ohms
Series Equivalent Output Impedance (V_{CC} = 12.5 Vdc, P_{out} = 1.0 W, f = 175 MHz)	Z_{out}	–	47-j 60	–	Ohms

3

FIGURE 1 – 175 MHz TEST CIRCUIT SCHEMATIC



C1,C2,C3,C4	3.0-30 pF
C5	1000 pF
C6	0.01 μF
L1	2 Turns, #16 AWG, 3/16" I.D., 1/4" Long
L2	0.15 μH, MOLDED CHOKE
L3	4 Turns, #16 AWG, 3/8" I.D., 3/8" Long
R1	100 Ω, 1/4 W, 10%

FIGURE 2 – OUTPUT POWER versus INPUT POWER

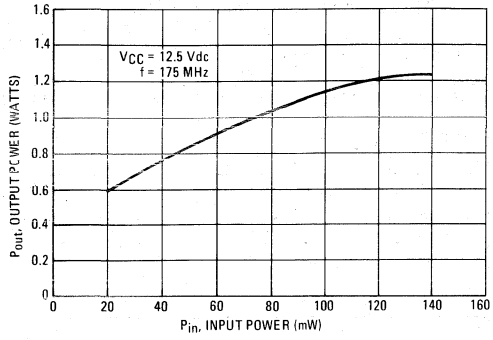


FIGURE 3 – CURRENT-GAIN BANDWIDTH PRODUCT

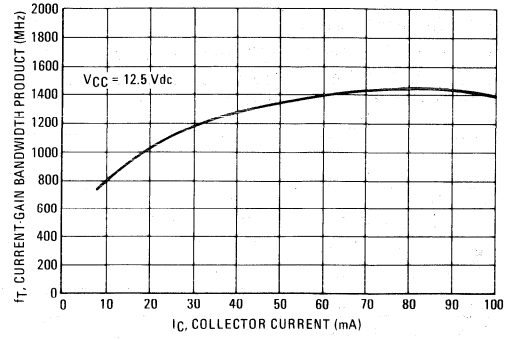
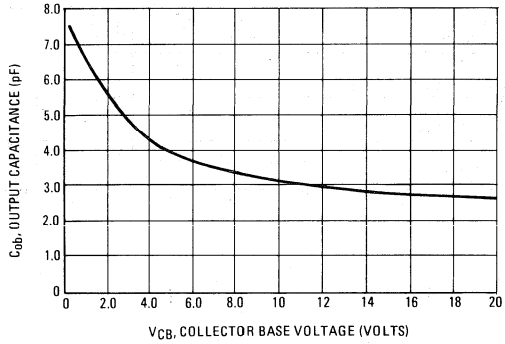


FIGURE 4 – OUTPUT CAPACITANCE versus COLLECTOR BASE VOLTAGE



3

MRF607

The RF Line

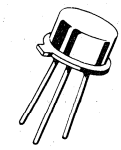
1.75 W — 175 MHz

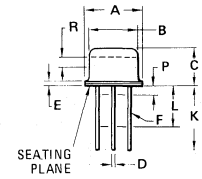
RF POWER
TRANSISTOR
NPN SILICON

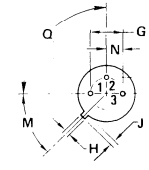
NPN SILICON RF POWER TRANSISTOR

. . . designed for amplifier, frequency multiplier, or oscillator applications in military, mobile, marine and citizens band equipment. Suitable for use as output driver or pre-driver stages in VHF and UHF equipment.

- Specified 12.5 Volt, 175 MHz Characteristics —
  Output Power = 1.75 Watts
  Minimum Gain = 11.5 dB
  Efficiency = 50%
- Characterized through 225 MHz







STYLE 1
PIN 1. EMITTER
2. BASE
3. COLLECTOR

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	3.5	Vdc
Collector Current — Continuous	I_C	0.33	Adc
Total Device Dissipation @ $T_C = 75^oC$ (1) Derate above 75^oC	P_D	3.5 28	Watts mW/^oC
Storage Temperature Range	T_{stg}	-65 to +200	°C

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as class B or C RF amplifiers.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

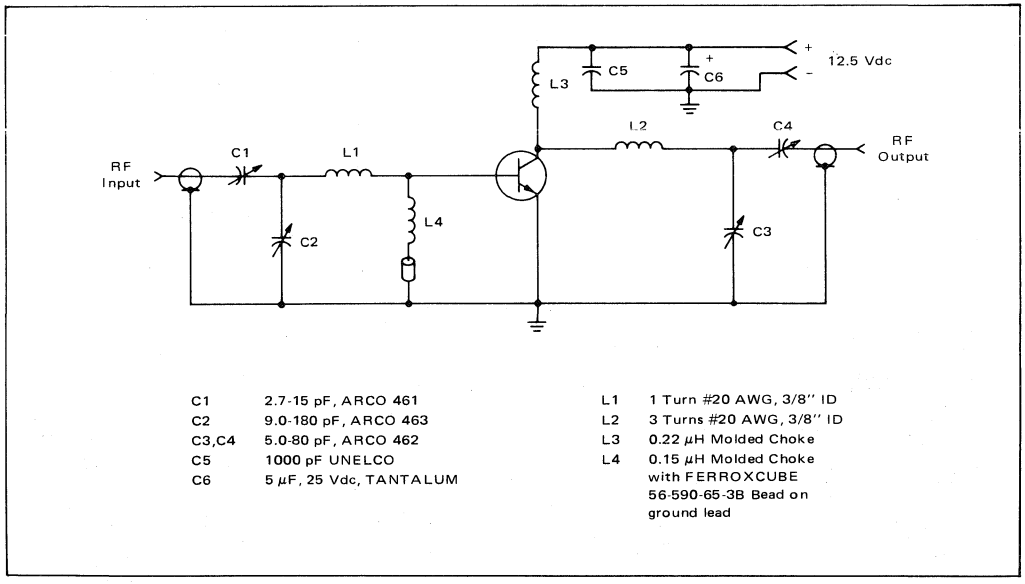
CASE 79-02
TO-39
All JEDEC notes and dimensions apply.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 25 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 25 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	–	Vdc
Emitter Base Breakdown Voltage (I_E = 0.5 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	–	Vdc
Collector Cutoff Current (V_{CE} = 10 Vdc, I_B = 0)	I_{CEO}	–	0.3	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	20	150	–
DYNAMIC CHARACTERISTICS				
Output Capacitance (V_{CB} = 12 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	15	pF
FUNCTIONAL TEST (Figure 1)				
Common-Emitter Amplifier Power Gain (P_{out} = 1.75 W, V_{CC} = 12.5 Vdc, f = 175 MHz)	G_{PE}	11.5	–	dB
Collector Efficiency (P_{out} = 1.75 W, V_{CC} = 12.5 Vdc, f = 175 MHz)	η	50	–	%

FIGURE 1 – 175 MHz TEST CIRCUIT SCHEMATIC



C1	2.7-15 pF, ARCO 461	L1	1 Turn #20 AWG, 3/8" ID
C2	9.0-180 pF, ARCO 463	L2	3 Turns #20 AWG, 3/8" ID
C3,C4	5.0-80 pF, ARCO 462	L3	0.22 μH Molded Choke
C5	1000 pF UNELCO	L4	0.15 μH Molded Choke with FERROXCUBE 56-590-65-3B Bead on ground lead
C6	5 μF, 25 Vdc, TANTALUM		

TYPICAL PERFORMANCE DATA

FIGURE 2 – OUTPUT POWER versus FREQUENCY

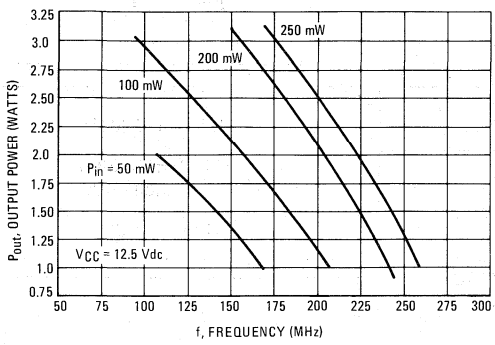


FIGURE 3 – OUTPUT POWER versus INPUT POWER

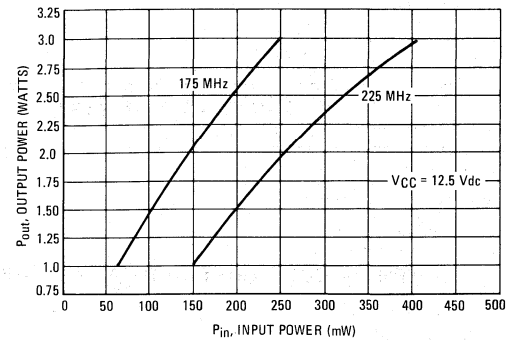


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

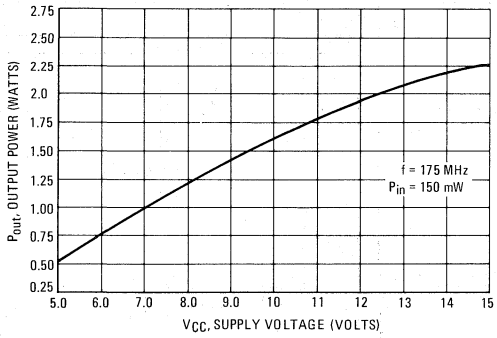
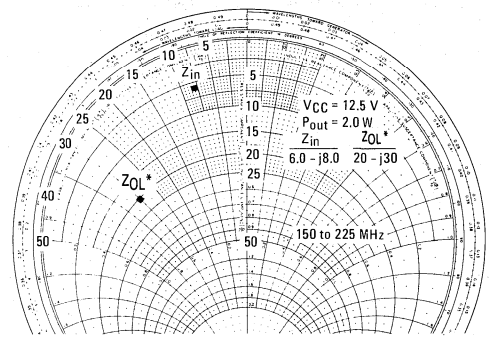


FIGURE 5 – SERIES EQUIVALENT IMPEDANCE PARAMETERS



*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

3

MRF627

The RF Line

0.5 W - 470 MHz

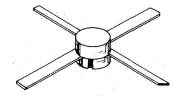
HIGH FREQUENCY TRANSISTORS

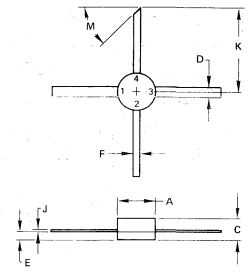
NPN SILICON

NPN SILICON HIGH FREQUENCY TRANSISTORS

. . . designed for 12.5 Volt UHF large-signal amplifier applications in industrial and commercial FM equipment operating in the 407 to 512 MHz range. Ideally suited for requirements that specify optimum performance in a limited space.

- Specified 12.5 Volt, 470 MHz Characteristics –
  Output Power = 0.5 Watts
  Minimum Gain = 10 dB
  Efficiency = 60%





STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CBO}	30	Vdc
Emitter-Base Voltage	V_{EBO}	3.5	Vdc
Collector-Current - Continuous	I_C	150	mAdc
Total Device Dissipation @ $T_C = 25^oC$ Derate Above 25^oC	P_D	2.5 35	Watts $mW/^oC$
Storage Temperature Range	T_{stg}	−65 to +150	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	28.5	$^oC/W$

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.08	5.59	0.200	0.220
C	2.41	3.30	0.095	0.130
D	1.40	1.65	0.055	0.065
E	1.02	1.27	0.040	0.050
F	0.64	0.89	0.025	0.035
J	0.08	0.18	0.003	0.007
K	11.05	–	0.435	–
M	45° NOM		45° NOM	

Case 305A-01

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	30	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	–	–	Vdc
Collector Cutoff Current (V_{CE} = 12 Vdc, I_B = 0)	I_{CEO}	–	–	1.0	mAdc
Emitter Cutoff Current (V_{BE} = 3.5 Vdc, I_C = 0)	I_{EBO}	–	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	15	–	150	–
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product	f_T				GHz
(I_C = 50 mAdc, V_{CE} = 12.5 Vdc, f = 200 MHz)		–	2.5	–	
(I_C = 100 mAdc, V_{CE} = 12.5 Vdc, f = 200 MHz)		–	2.7	–	
(I_C = 150 mAdc, V_{CE} = 12.5 Vdc, f = 200 MHz)		–	2.6	–	
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	3.0	3.5	pF
Input Capacitance (V_{BE} = 1.0 Vdc, I_C = 0, f = 1.0 MHz)	C_{ib}	–	8.8	–	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 0.5 W, f = 470 MHz)	G_{PE}	10	12	–	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 0.5 W, f = 470 MHz)	η	–	60	–	%
Series Equivalent Input Impedance (V_{CC} = 12.5 Vdc, P_{out} = 0.5 W, f = 470 MHz)	Z_{in}	–	6.0-j4.0	–	Ohms
Series Equivalent Output Impedance (V_{CC} = 12.5 Vdc, P_{out} = 0.5 W, f = 470 MHz)	Z_{out}	–	45-j28	–	Ohms

FIGURE 1 – OUTPUT POWER versus INPUT POWER

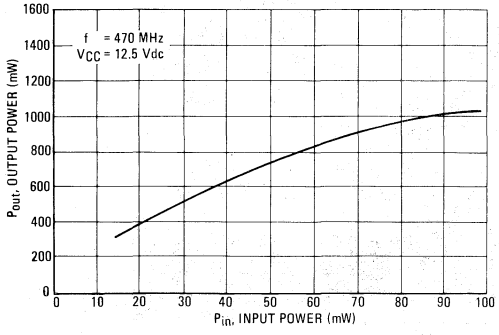
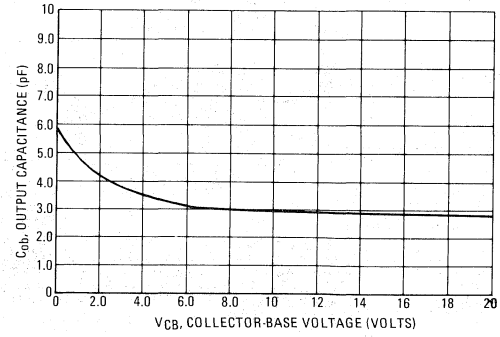
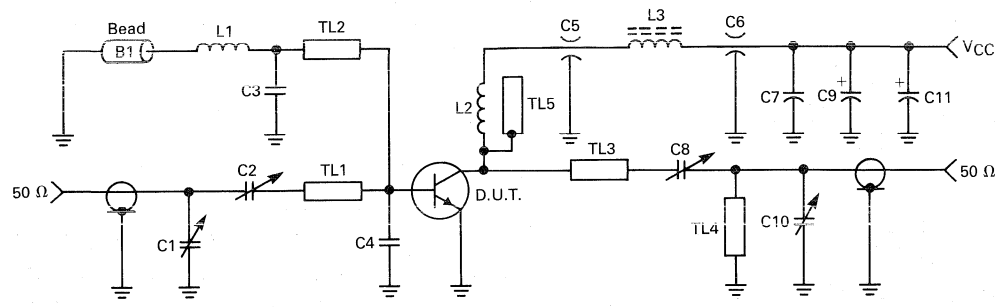


FIGURE 2 – OUTPUT CAPACITANCE versus COLLECTOR BASE VOLTAGE



3

FIGURE 3 — 470 MHz TEST CIRCUIT SCHEMATIC



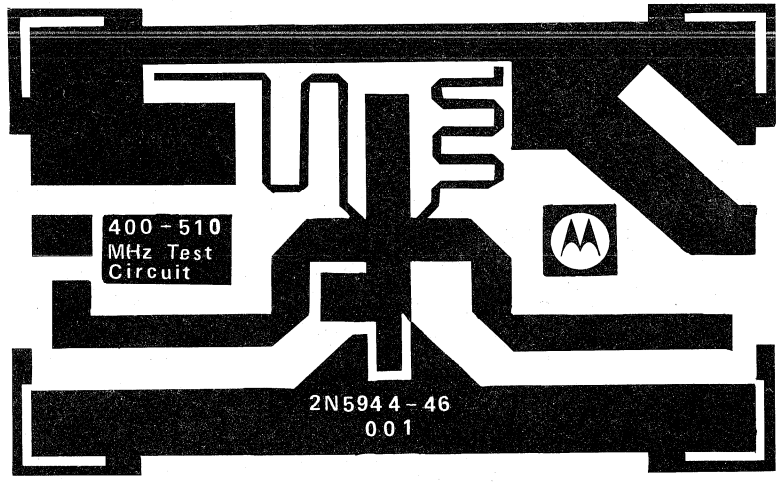
B1 — Ferroxcube Bead — 56-590-65-3B
C1, C2, C8, C10 — Johanson Trimmer, JMC #5501
C3 — 100 pF Unelco 350 Vdc J101
C4 — 15 pF Unelco
C5, C6 — 680 pF Allen Bradley, Feed-Thru
C7 — 0.1 μF Monolithic
C9 — 1 μF Tantalum Sprague ±10% 35 Vdc
C11 — 30 μF Electrolytic 25 Vdc

TL1 — Micro Strip 0.26″ x 2.9″
TL2 — Micro Strip 0.055″ x 3.9″
TL3 — Micro Strip 0.26″ x 2.9″
TL4 — Micro Strip 0.50″ x 1.2″
TL5 — Micro Strip 0.055″ x 2.9″
L1 — #18 AWG Wire 0.750″ Long
L2 — 2 Turns #18 AWG ID ≈ 0.2″
L3 — VK200 20/4B

Board — 0.062″ Glass Teflon
2 oz. Cu. CLAD
ϵ_r = 2.55

3

FIGURE 4 – 470 MHz TEST CIRCUIT LAYOUT



NOTE: The Printed Circuit Board shown is 75% of the original.

FIGURE 5 – TYPICAL S_{11} and S_{22} versus FREQUENCY

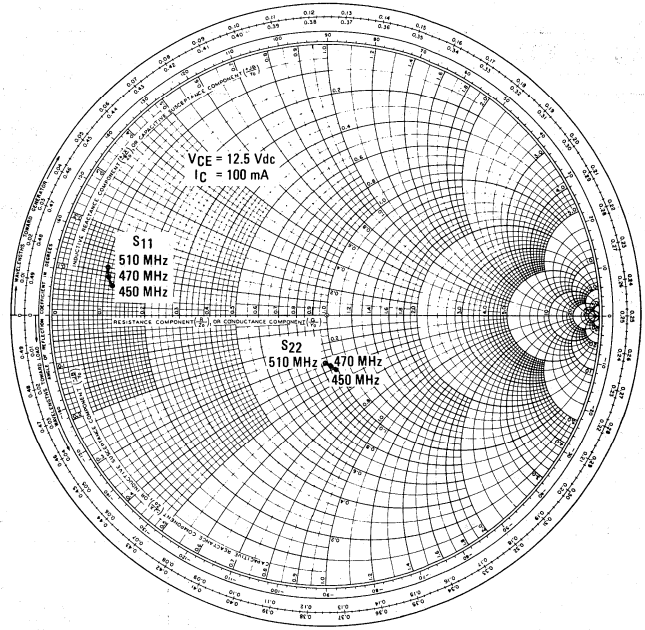


FIGURE 6 – TYPICAL S_{12} versus FREQUENCY

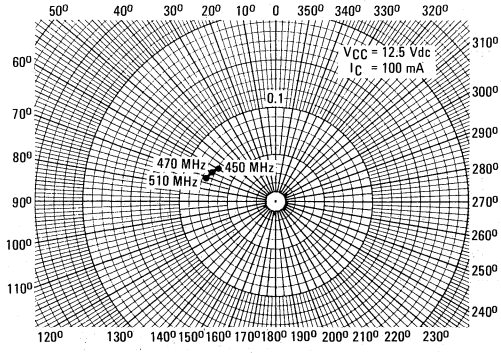
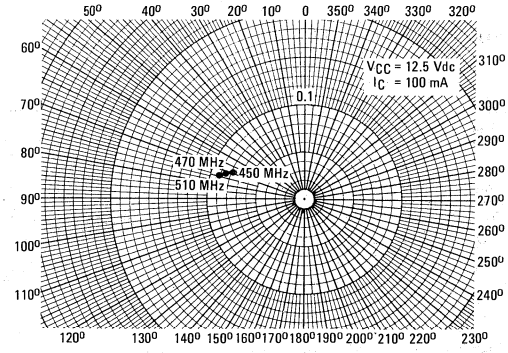


FIGURE 7 – TYPICAL S_{21} versus FREQUENCY



3

MRF630

The RF Line

3.0 W 470 MHz

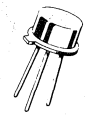
RF POWER TRANSISTOR

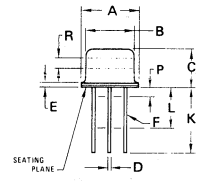
NPN SILICON

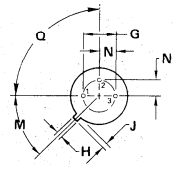
NPN SILICON RF POWER TRANSISTOR

. . . designed for 12.5 Volt UHF large-signal, amplifier applications in industrial and commercial FM equipment operating to 512 MHz.

- Specified 12.5 Volt, 470 MHz Characteristics
  Output Power = 3.0 Watts
  Minimum Gain = 9.5 dB
  Efficiency = 55%
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Grounded Emitter TO-39 Package for High Gain and Excellent Heat Dissipation
- Replaces Medium-Power Stud Mounted Devices
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration







STYLE 5:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH TO-39 OUTLINE SHALL APPLY.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.02	9.30	0.355	0.366
B	8.00	8.51	0.315	0.335
C	4.19	4.57	0.165	0.180
D	0.43	0.53	0.017	0.021
E	0.43	0.89	0.017	0.035
F	0.41	0.48	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.71	0.86	0.028	0.034
J	0.74	1.02	0.029	0.040
K	12.70	–	0.500	–
M	45° NOM		45° NOM	
N	2.54 TYP		0.100 TYP	
Q	90° NOM		90° NOM	

CASE 79-03

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16	Vdc
Collector-Base Voltage	V_{CES}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	1.0	Adc
Total Device Dissipation @ T_C = 25°C Derate Above 25°C	P_D	8.75 50	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

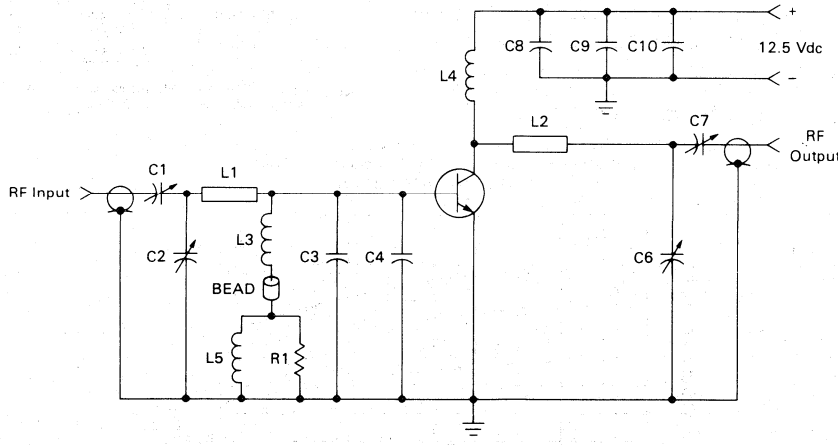
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	20	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 12.5 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	20	60	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	8.0	12	pF
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (Fig. 1) (V_{CC} = 12.5 Vdc, P_{out} = 3.0 W, f = 470 MHz)	G_{PE}	9.5	10.8	—	dB
Collector Efficiency (Fig. 1) (V_{CC} = 12.5 Vdc, P_{out} = 3.0 W, f = 470 MHz)	η	—	55	—	%

FIGURE 1 — 470 MHz TEST CIRCUIT SCHEMATIC



C1, C7 — 1.5 - 20 pF Johanson
C2, C6 — 1 - 10 pF Johanson
C3, C4 — 27 pF Mini-Unelco
C8 — 250 pF Unelco
C9 — 0.047 μF Erie Disc Cap 10 V
C10 — 1.0 μF Electrolytic

L1, L2 — Copper Strap, 1" Length × 0.225 Width × 0.005" Thickness
L3 — 0.33 μH Molded Choke
L4 — 0.12 μH Molded Choke
L5 — 1.2 μH Molded Choke
R1 — 10 Ω, 1/4 W

FIGURE 2 — OUTPUT POWER versus INPUT POWER

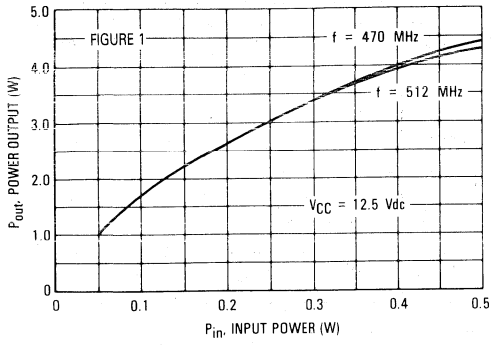


FIGURE 3 — OUTPUT POWER versus FREQUENCY

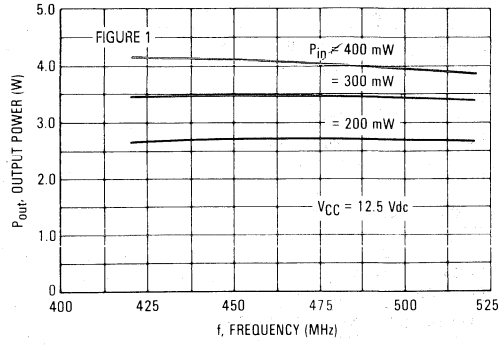


FIGURE 4 — POWER OUT versus SUPPLY VOLTAGE

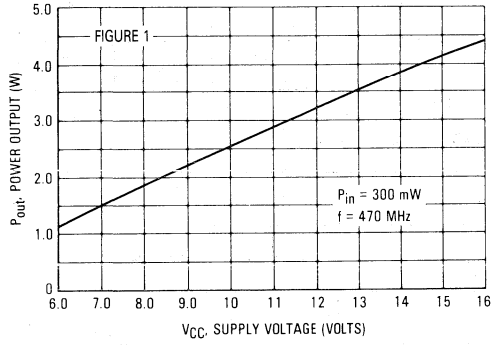
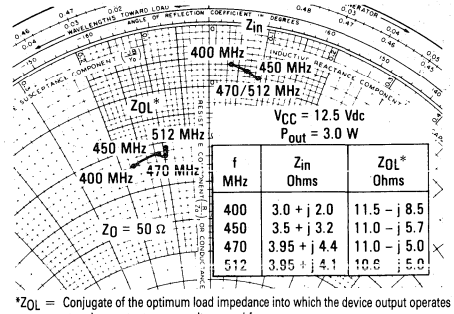


FIGURE 5 — SERIES EQUIVALENT IMPEDANCE



f MHz	Zin Ohms	ZOL* Ohms
400	3.0 + j 2.0	11.5 – j 8.5
450	3.5 + j 3.2	11.0 – j 5.7
470	3.95 + j 4.4	11.0 – j 5.0
512	3.95 + j 4.1	10.6 – j 5.0

*ZOL = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

FIGURE 6 — OUTPUT POWER versus FREQUENCY, BROADBAND CIRCUIT

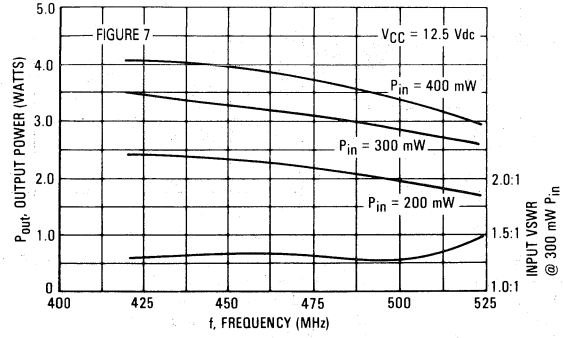
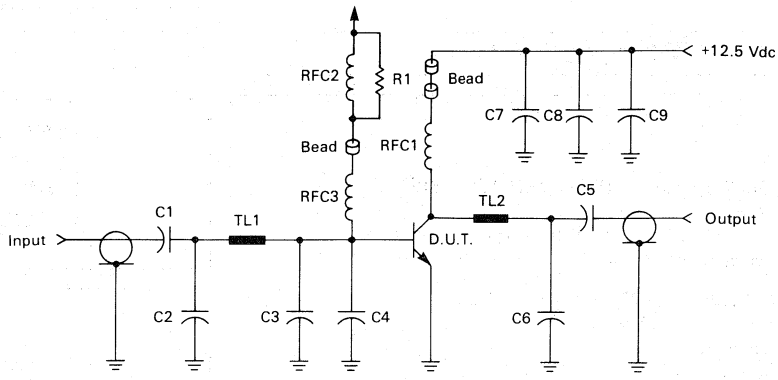


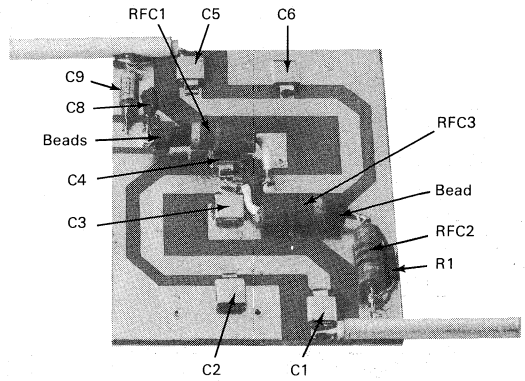
FIGURE 7 — MRF630 BROADBAND CIRCUIT
420-520 MHz



C1, C5 — 43 pF Mini-Unelco
C2 — 10 pF Mini-Unelco
C3 — 18 pF Mini-Unelco
C4 — 27 pF Mini-Unelco
C6 — 6.8 pF Mini-Unelco
C7 — 220 pF Ceramic Chip
C8 — 0.1 mF
C9 — 1.0 mF Tantalum

RFC1 — 0.47 μH Molded Choke
RFC2 — 1.0 μH Molded Choke
RFC3 — 0.3 μH Molded Choke
R1 — 12 Ω/1/4 W
TL1 — Transmission Line 0.166" × 1.85" (WXL)
TL2 — Transmission Line 0.166" × 1.77" (WXL)
Board Material — 2 oz. 0.0625" TFG

FIGURE 8 — BROADBAND CIRCUIT



MRF641

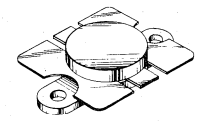
The RF Line

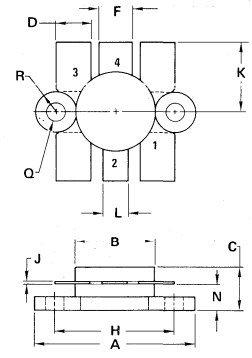
15 W — 470 MHz
CONTROLLED Q
RF POWER
TRANSISTOR
NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed for 12.5 Volt UHF large-signal amplifier applications in industrial and commercial FM equipment operating to 512 MHz.

- Specified 12.5 Volt, 470 MHz Characteristics —
  Output Power = 15 Watts
  Minimum Gain = 7.8 dB
  Efficiency = 55%
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Built-In Matching Network for Broadband Operation
- Tested for Load Mismatch Stress at all Phase Angles with 20:1 VSWR @ 16-Volt High Line and Overdrive.





STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. EMITTER
4. BASE
FLANGE-ISOLATED

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	12.45	12.95	0.490	0.510
C	5.97	7.62	0.235	0.300
D	5.33	5.59	0.210	0.220
F	5.08	5.33	0.200	0.210
H	18.29	18.54	0.720	0.730
J	0.10	0.15	0.004	0.006
K	10.29	—	0.405	—
L	3.81	4.06	0.150	0.160
N	3.81	4.32	0.150	0.170
Q	2.92	3.30	0.115	0.130
R	3.05	3.30	0.120	0.130

CASE 316-01

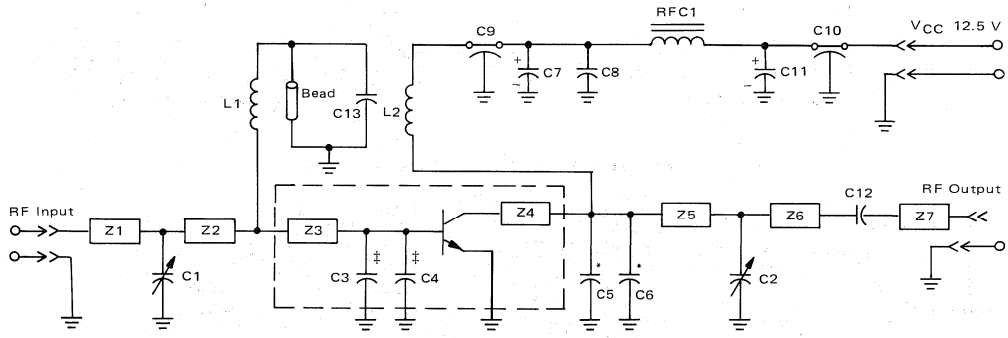
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	3.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.25	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
THERMAL CHARACTERISTICS			
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	–	–	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	30	70	150	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	40	60	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 15 W, f = 470 MHz)	G_{pe}	7.8	8.5	–	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 15 W, f = 470 MHz)	η	55	60	–	%
Output Mismatch Stress (V_{CC} = 16 Vdc, P_{in} = 3.0 W, f = 470 MHz, VSWR = 20:1, All Phase Angles)	ψ	No Degradation in Output Power			

FIGURE 1 – TEST CIRCUIT SCHEMATIC



PARTS

Z1 = 1.225" X 0.187" Microstrip
Z2 = 0.884" X 0.187" Microstrip
Z3 = Capacitor Block (Base)
Z4 = Collector Block
Z5 = 1.1" X 0.187" Microstrip
Z6 = 0.433" X 0.187" Microstrip
Z7 = 0.4" X 0.187" Microstrip

Dotted Area – Capacitor Assembly

C1, C2 – 0.8–10 pF Johanson
C3, C4 – 24 pF Chip Caps 100 mils ATC
C5, C6 – 22 pF Chip Caps 100 mils ATC
C12 – 220 pF Chip Cap 100 mils ATC
C7, C11 – 1.0 μF Tantalum 35 Vdc
C9, C10 – 680 pF Feedthrough Allen-Bradley
C13 – 200 pF UNELCO
C8 – 0.1 μF, 50 V Erie Red Cap
RFC1 – VK 200 – 104B Ferrite Choke
L1 – 4 Turns 0.2" Dia. #16 AWG
L2 – 9 Turns 0.15" Dia. #16 AWG

Bead – Ferroxcube 56-590-65-35EB

NOTES

**C5, C6, are mounted as close to the capacitor assembly as possible.

‡‡C3, C4 are mounted in the capacitor assembly.

Board – 62.5 mil Glass Teflon, ϵ_R = 2.55.

FIGURE 2 – POWER OUTPUT versus POWER INPUT

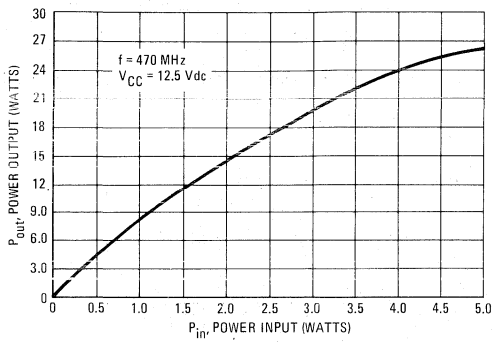


FIGURE 3 – POWER OUTPUT versus FREQUENCY

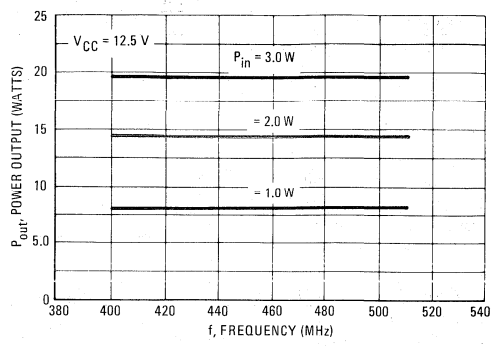


FIGURE 4 – POWER OUTPUT versus SUPPLY VOLTAGE

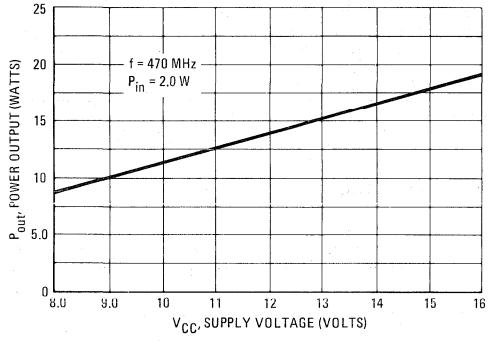


FIGURE 5 – POWER SATURATION PROFILE

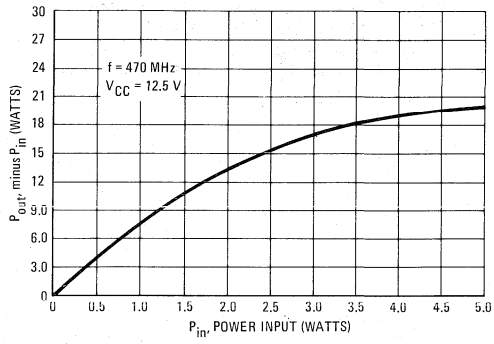
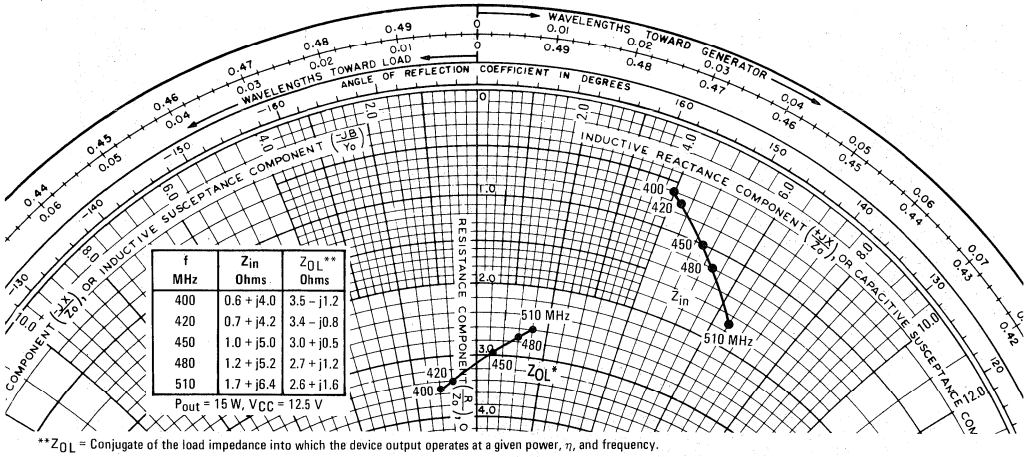


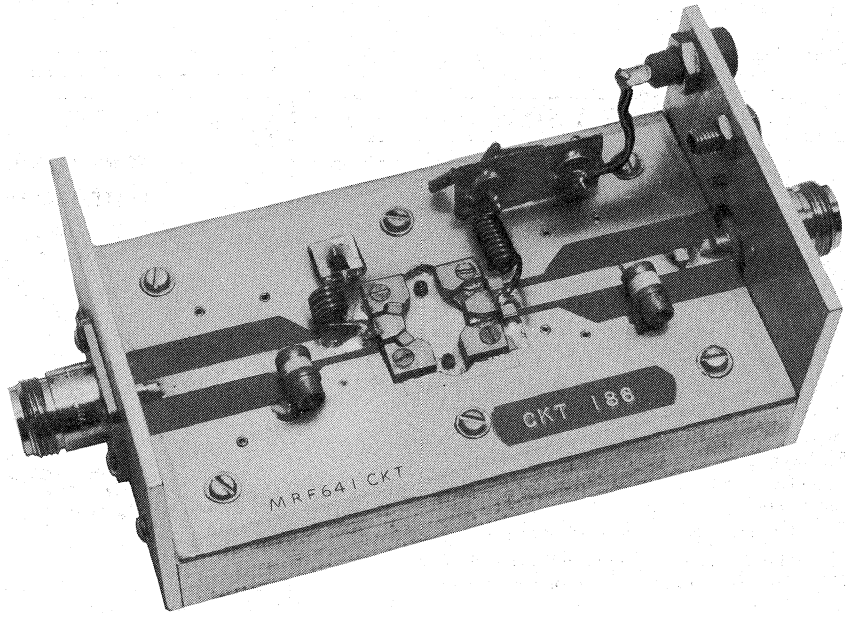
FIGURE 6 – SERIES EQUIVALENT INPUT-OUTPUT IMPEDANCE



f MHz	Z_{in} Ohms	Z_{OL}** Ohms
400	0.6 + j4.0	3.5 – j1.2
420	0.7 + j4.2	3.4 – j0.8
450	1.0 + j5.0	3.0 + j0.5
480	1.2 + j5.2	2.7 + j1.2
510	1.7 + j6.4	2.6 + j1.6

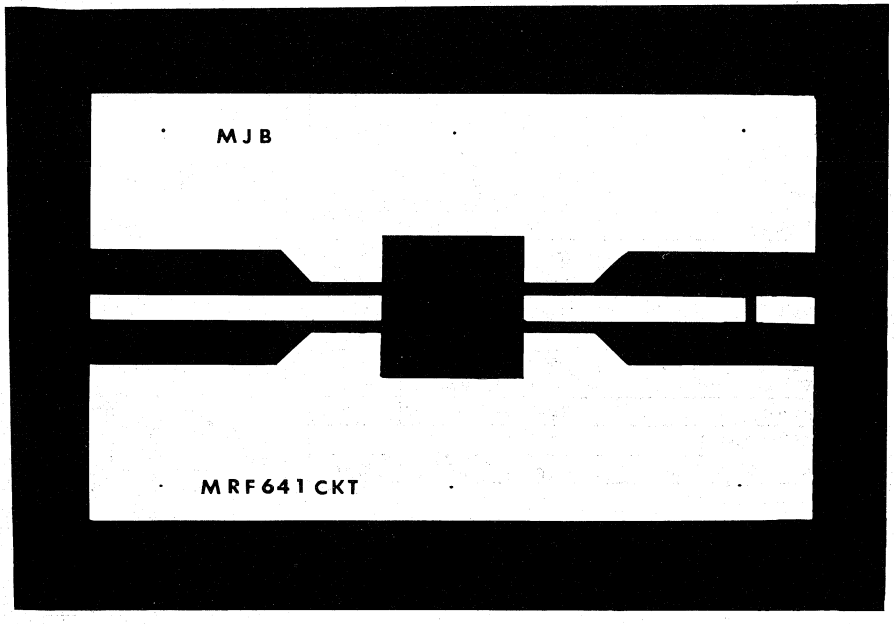
P_{out} = 15 W, V_{CC} = 12.5 V

**Z_{OL} = Conjugate of the load impedance into which the device output operates at a given power, η, and frequency.



3

MRF641 TEST CIRCUIT



NOTE: The Printed Circuit Board shown is 75% of the original.

MRF644

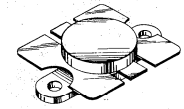
The RF Line

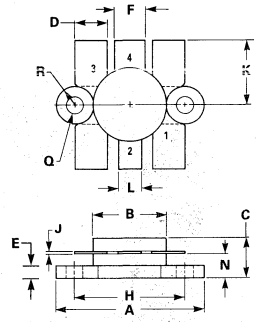
25 W — 470 MHz
CONTROLLED Q
RF POWER
TRANSISTOR
NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed for 12.5 Volt UHF large-signal amplifier applications in industrial and commercial FM equipment operating to 512 MHz.

- Specified 12.5 Volt, 470 MHz Characteristics —
  Output Power = 25 Watts
  Minimum Gain = 6.2 dB
  Efficiency = 60%
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Built-In Matching Network for Broadband Operation
- Tested for Load Mismatch Stress at all Phase Angles with 20:1 VSWR @ 16-Volt High Line and 50% Overdrive.





STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. EMITTER
4. BASE

NOTE:
FLANGE IS ISOLATED IN ALL STYLES.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.14	0.960	0.990
B	12.45	12.95	0.490	0.510
C	5.97	7.62	0.235	0.300
D	5.33	5.58	0.210	0.220
E	2.16	3.04	0.085	0.120
F	5.08	5.33	0.200	0.210
H	18.29	18.54	0.720	0.730
J	0.10	0.15	0.004	0.006
K	10.29	11.17	0.405	0.440
L	3.81	4.06	0.150	0.160
N	3.81	4.31	0.150	0.170
Q	2.92	3.30	0.115	0.130
R	3.05	3.30	0.120	0.130
U	11.94	12.57	0.470	0.495

CASE 316-01

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	4.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	103 0.59	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
THERMAL CHARACTERISTICS			
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.7	°C/W

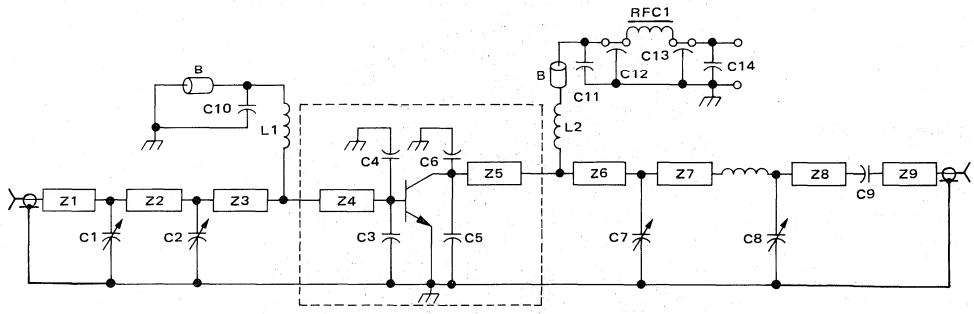
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	–	–	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	40	70	100	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	60	85	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 25 W, I_C (MAX) = 3.6 Adc, f = 470 MHz)	G_{pe}	6.2	7.0	–	dB
Input Power (V_{CC} = 12.5 Vdc, P_{out} = 25 W, f = 470 MHz)	P_{in}	–	5.0	6.0	Watts
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 25 W, I_C (MAX) = 3.6 Adc, f = 470 MHz)	η	55	60	–	%
Output Mismatch Stress (V_{CC} = 16 Vdc, P_{in} = Note 1, f = 470 MHz, VSWR = 20:1, All Phase Angles)	ψ*	No Degradation in Output Power			
Series Equivalent Input Impedance (V_{CC} = 12.5 Vdc, P_{out} = 25 W, f = 470 MHz)	Z_{in}	–	1.2+j3.3	–	Ohms
Series Equivalent Output Impedance (V_{CC} = 12.5 Vdc, P_{out} = 25 W, f = 470 MHz)	Z_{OL}	–	1.9 + j2.1	–	Ohms

Notes:

1. P_{in} = 150% of Drive Requirement for 25 W Output at 12.5 Vdc.
* ψ = Mismatch stress factor—the electrical criterion established to verify the device resistance to load mismatch failure. The mismatch stress test is accomplished in the standard test fixture (Figure 1) terminated in a 20:1 minimum load mismatch at all phase angles.

FIGURE 1 – TEST CIRCUIT SCHEMATIC



C1, C2, C7, C8	1–20 pF JOHANSON Variable	C12, C13	680 pF Feedthrough	Z3	0.20" x 0.20" Microstrip
C3	27 pF 100 mil ATC	L1	5" #22 AWG 0.100" ID	Z4, Z5	1/2" #18 AWG bent in a "V" shape 1/8" Wide
C4	30 pF 100 mil ATC	L2	5" #20 AWG 0.187" ID	Z6	0.20" x 0.20" Microstrip
C5, C6	33 pF 100 mil ATC	RFC1	Ferroxcube VK200-20-4B	Z7	0.70" x 0.20" Microstrip
C9	250 pF 100 mil ATC	B	Ferroxcube Bead 56-590-65-3B	Z8	0.33" x 0.20" Microstrip
C10	100 pF UNELCO	Z1	0.25" x 0.20" Microstrip	Z9	0.50" x 0.20" Microstrip
C11, C14	1 μF 35 V TANTALUM	Z2	1.63" x 0.20" Microstrip	Board	62.5 mil Glass Teflon, ϵ_R = 2.55

FIGURE 2 – POWER OUTPUT versus POWER INPUT

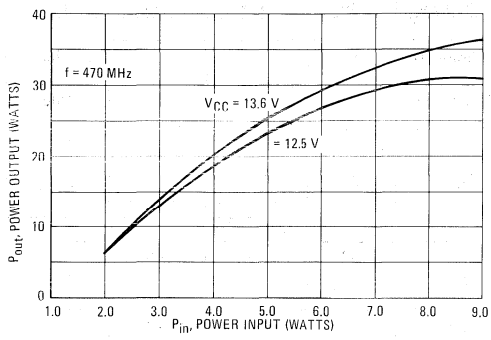


FIGURE 3 – POWER OUTPUT versus FREQUENCY

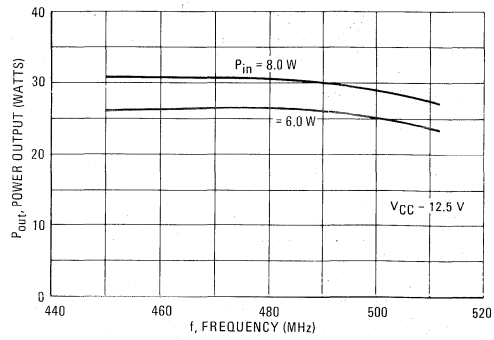


FIGURE 4 – POWER OUTPUT versus SUPPLY VOLTAGE

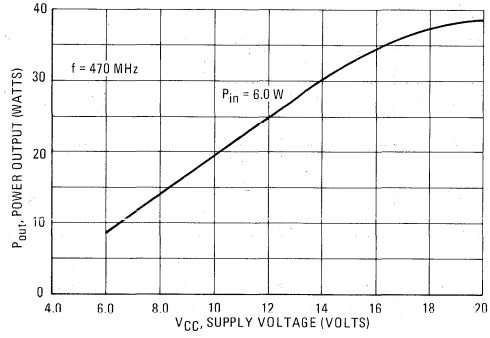


FIGURE 5 – POWER SATURATION PROFILE

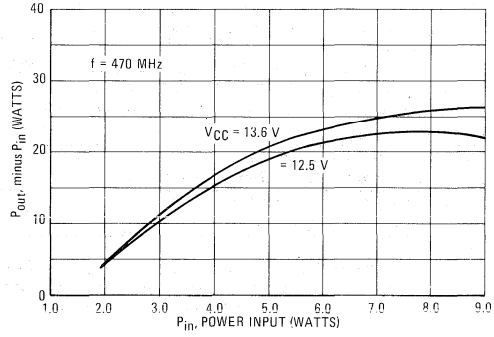
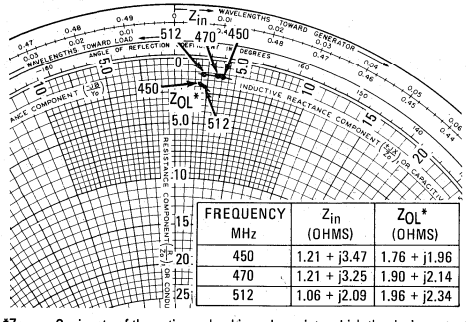


FIGURE 7 – SERIES EQUIVALENT INPUT-OUTPUT IMPEDANCE



FREQUENCY MHz	Z_{in} (OHMS)	Z_{OL}* (OHMS)
450	1.21 + j3.47	1.76 + j1.96
470	1.21 + j3.25	1.90 + j2.14
512	1.06 + j2.09	1.96 + j2.34

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

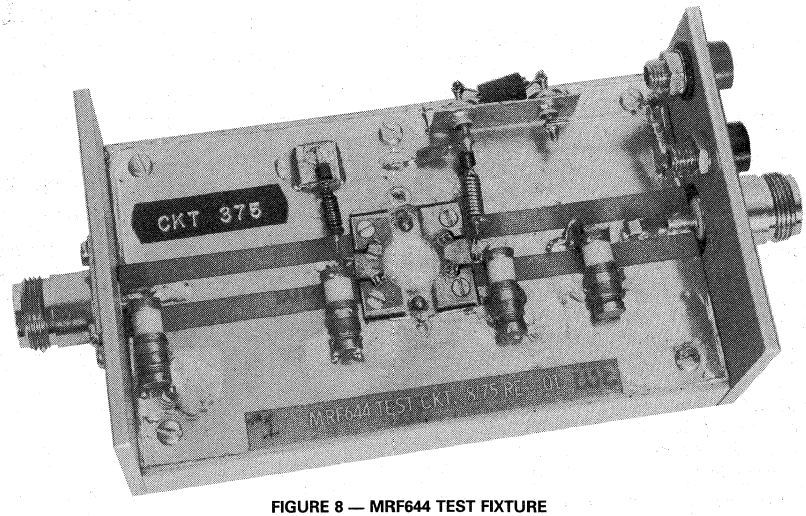
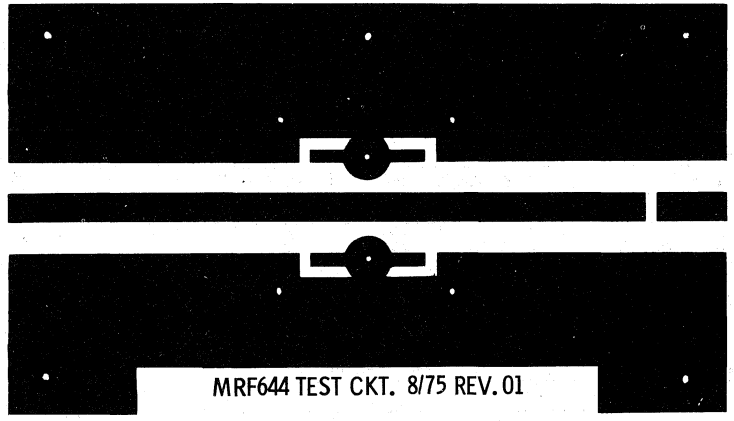


FIGURE 8 — MRF644 TEST FIXTURE



NOTE: The Printed Circuit Board shown is 75% of the original.

FIGURE 9 — PRINTED CIRCUIT BOARD

MRF646

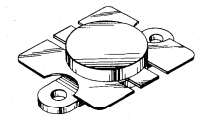
The RF Line

45 W – 470 MHz
CONTROLLED Q
RF POWER
TRANSISTOR
NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed for 12.5 Volt UHF large-signal amplifier applications in industrial and commercial FM equipment operating to 512 MHz.

- Specified 12.5 Volt, 470 MHz Characteristics –
  Output Power = 45 Watts
  Minimum Gain = 4.8 dB
  Efficiency = 55%
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Built-In Matching Network for Broadband Operation
- Tested for Load Mismatch Stress at all Phase Angles with 20:1 VSWR @ 16-Volt High Line and 50% Overdrive.

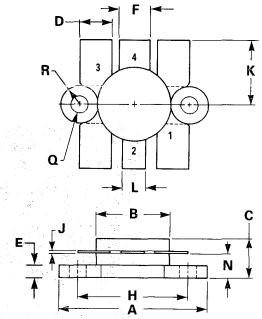


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	9.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	117 0.67	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W



STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. EMITTER
4. BASE

NOTE:
FLANGE IS ISOLATED IN ALL STYLES.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.14	0.960	0.990
B	12.45	12.95	0.490	0.510
C	5.97	7.62	0.235	0.300
D	5.33	5.58	0.210	0.220
E	2.16	3.04	0.085	0.120
F	5.08	5.33	0.200	0.210
H	18.29	18.54	0.720	0.730
J	0.10	0.15	0.004	0.006
K	10.29	11.17	0.405	0.440
L	3.81	4.06	0.150	0.160
N	3.81	4.31	0.150	0.170
Q	2.92	3.30	0.115	0.130
R	3.05	3.30	0.120	0.130
U	11.94	12.57	0.470	0.495

CASE 316-01

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

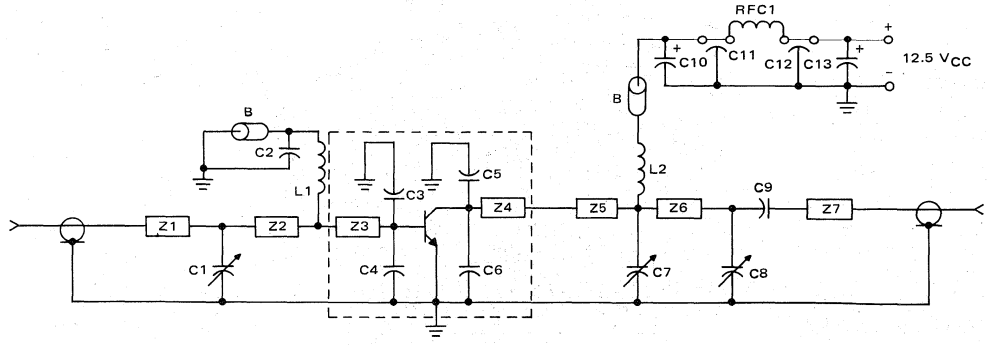
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	–	–	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	70	150	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	90	125	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 45 W, I_C(Max) = 5.8 Adc, f = 470 MHz)	G_{pe}	4.8	5.4	–	dB
Input Power (V_{CC} = 12.5 Vdc, P_{out} = 45 W, f = 470 MHz)	P_{in}	–	13	15	Watts
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 45 W, I_C (Max) = 5.8 Adc, f = 470 MHz)	η	55	60	–	%
Load Mismatch Stress (V_{CC} = 16 Vdc, P_{in} = Note 1, f = 470 MHz, VSWR = 20:1, All Phase Angles)	ψ*	No Degradation in Output Power			
Series Equivalent Input Impedance (V_{CC} = 12.5 Vdc, P_{out} = 45 W, f = 470 MHz)	Z_{in}	–	1.4 + j4.0	–	Ohms
Series Equivalent Output Impedance (V_{CC} = 12.5 Vdc, P_{out} = 45 W, f = 470 MHz)	Z_{OL}*	–	1.2 + j2.8	–	Ohms

Notes:

1. P_{in} = 150% of Drive Requirement for 45 W output @ 12.5 V.

* ψ = Mismatch stress factor—the electrical criterion established to verify the device resistance to load mismatch failure. The mismatch stress test is accomplished in the standard test fixture (Figure 1) terminated in a 20:1 minimum load mismatch at all phase angles.

FIGURE 1 – TEST CIRCUIT SCHEMATIC



C1, C8	1.0–20 pF JOHANSON	L2	5″ # 20 AWG, 0.1″ I.D.
C2	100 pF UNELCO	RFC1	Ferroxcube VR200-20-4B
C3, C6	33 pF 100 mil ATC	Z1	0.525″ x 0.190″ Microstrip
C4	30 pF 100 mil ATC	Z2	1.475″ x 0.190″ Microstrip
C5	39 pF 100 mil ATC	Z3, Z4	(0.2 x 0.2)/0.25 Alumina
C7	1–10 pF JOHANSON	Z5	0.190″ x 0.190″ Microstrip
C9	100 pF 100 mil ATC	Z6	1.150″ x 0.190″ Microstrip
C10, C13	1 μF 35 V TANTALUM	Z7	0.660″ x 0.190″ Microstrip
C11, C12	680 pF Feedthrough	Board	62.5 mil Glass Teflon, ϵ_R = 2.55, λ = 0.0018
B	Ferroxcube Bead 56-590-65-3B		
L1	5″ # 22 AWG, 0.1″ I.D.		

FIGURE 2 – POWER OUTPUT versus POWER INPUT

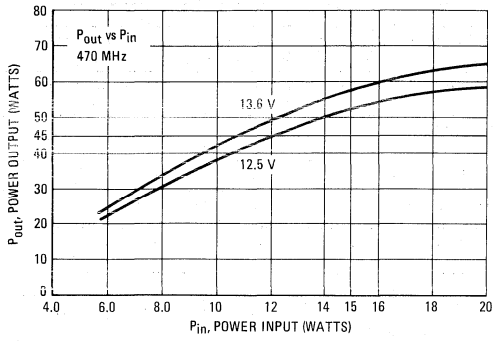


FIGURE 3 – POWER OUTPUT versus FREQUENCY

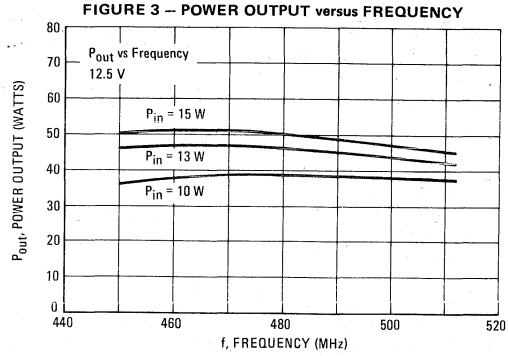


FIGURE 4 – POWER OUTPUT versus SUPPLY VOLTAGE

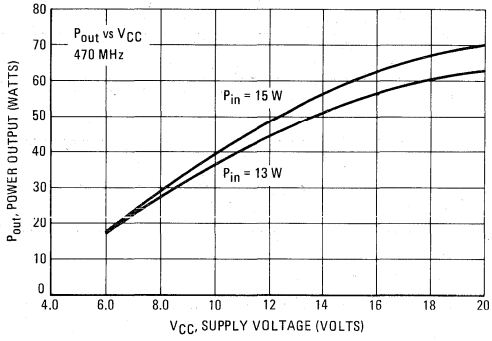


FIGURE 5 – POWER SATURATION PROFILE

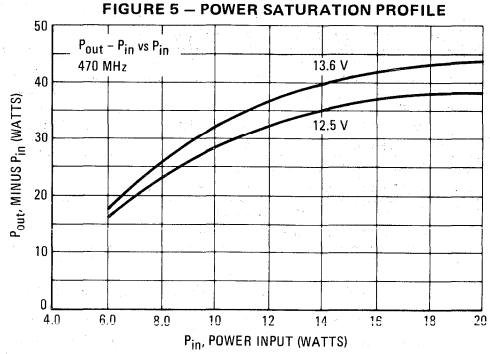
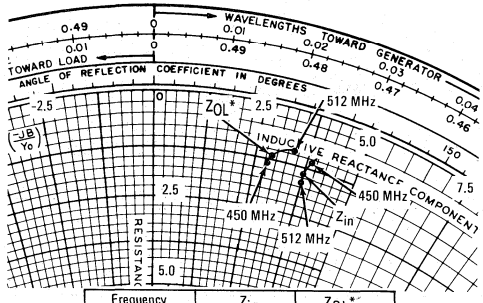


FIGURE 7 – SERIES EQUIVALENT INPUT-OUTPUT IMPEDANCE



Frequency (MHz)	Z_{in} (Ohms)	Z_{OL}* (Ohms)
450	1.21 + j3.91	1.27 + j2.79
470	1.41 + j3.75	1.20 + j2.80
512	1.64 + j3.75	0.93 + j3.36

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

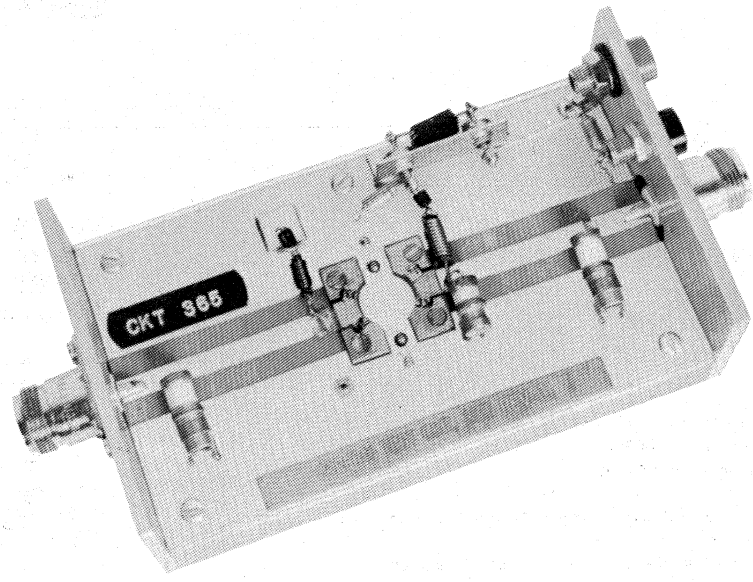
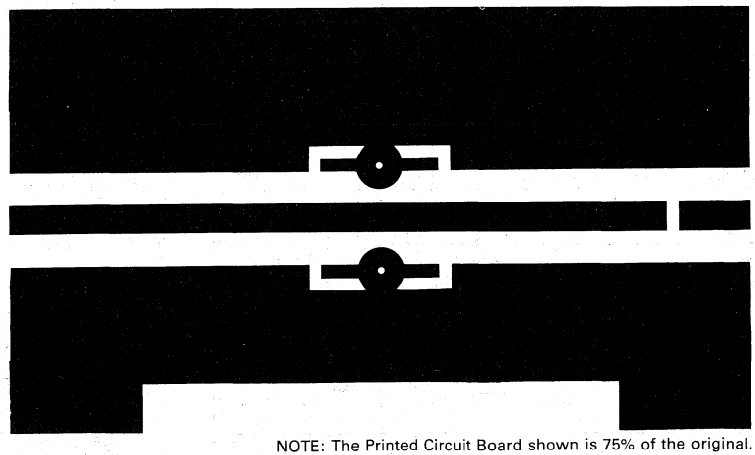


FIGURE 8 — MRF644 TEST FIXTURE



NOTE: The Printed Circuit Board shown is 75% of the original.

FIGURE 9 — PRINTED CIRCUIT BOARD

MRF648

The RF Line

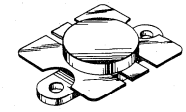
60 W – 470 MHz

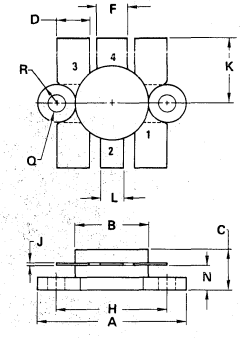
CONTROLLED Q
RF POWER
TRANSISTOR
NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed for 12.5 Volt UHF large-signal amplifier applications in industrial and commercial FM equipment operating to 512 MHz.

- Specified 12.5 Volt, 470 MHz Characteristics
  - Output Power = 60 Watts
  - Minimum Gain = 4.4 dB
  - Efficiency = 55%
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Built-In Matching Network for Broadband Operation
- Tested for Load Mismatch Stress at all Phase Angles with 20:1 VSWR @ 16-Volt High Line and 20% Overdrive





STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. EMITTER
4. BASE
FLANGE-ISOLATED

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	12.45	12.95	0.490	0.510
C	5.97	7.62	0.235	0.300
D	5.33	5.59	0.210	0.220
F	5.08	5.33	0.200	0.210
H	18.29	18.54	0.720	0.730
J	0.10	0.15	0.004	0.006
K	10.29	11.18	0.405	0.440
L	3.81	4.06	0.150	0.160
N	3.81	4.32	0.150	0.170
Q	2.92	3.30	0.115	0.130
R	3.05	3.30	0.120	0.130

CASE 316-01

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	11.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	175 1.0	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W

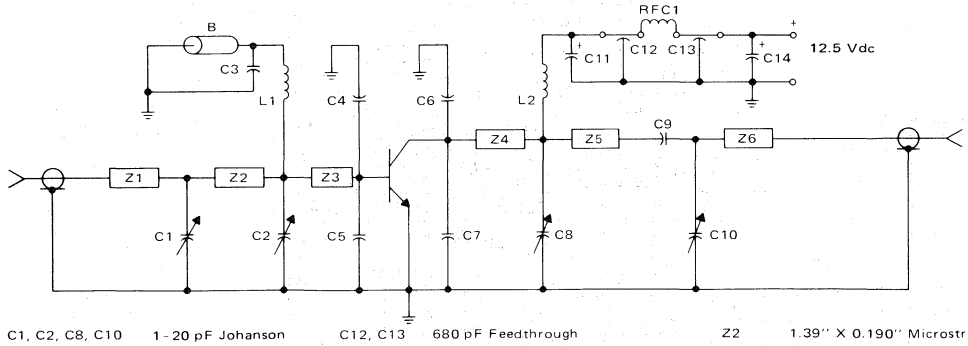
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	–	–	15	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 6.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	70	150	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	130	150	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 60 W, f = 470 MHz)	G_{pe}	4.4	5.0	–	dB
Input Power (V_{CC} = 12.5 Vdc, P_{out} = 60 W, f = 470 MHz)	P_{in}	–	19	22	Watts
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 60 W, f = 470 MHz)	η	55	65	–	%
Output Mismatch Stress (V_{CC} = 16 Vdc, P_{in} = 26 W, f = 470 MHz, VSWR = 20:1, All Phase Angles)	ψ*	No Degradation in Output Power			

Notes:

* ψ = Mismatch stress factor—the electrical criterion established to verify the device resistance to load mismatch failure. The mismatch stress test is accomplished in the standard test fixture (Figure 1) terminated in a 20:1 minimum load mismatch at all phase angles.

FIGURE 1 – TEST CIRCUIT SCHEMATIC



C1, C2, C8, C10	1-20 pF Johanson	C12, C13	680 pF Feedthrough	Z2	1.39" X 0.190" Microstrip
C3	200 pF Unelco	B	Ferroxcube Bead 56-590-65-3B	Z3, Z4	(0.2 X 0.2)/0.25 Alumina
C4, C5	33 pF 100mil ATC	L1	10 Turns #26 AWG 0.1" I.D. X 0.23"	Z5	1.30" X 0.190" Microstrip
C6, C7	36 pF 100mil ATC	L2	10 Turns #20 AWG 0.1" I.D. X 0.50"	Z6	**0.330" X 0.190" Microstrip**
C9	100 pF 100mil ATC	RFC1	Ferroxcube VK200-19-4B	Board	62.5mil Glass Teflon, ϵ_R = 2.55, λ = 0.0018, Dimension: 5.0" X 3.0" X 0.06"
C11, C14	1.0 μF 35 V Tantalum	Z1	0.46" X 0.190" Microstrip		

FIGURE 2 – POWER OUTPUT versus POWER INPUT

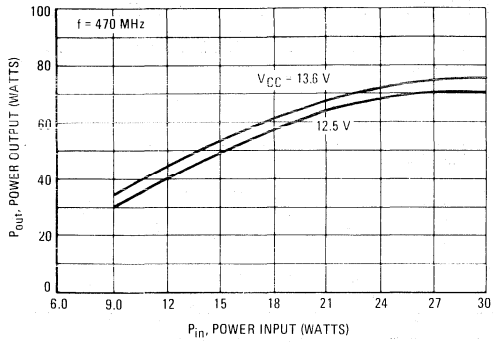


FIGURE 3 – POWER OUTPUT versus FREQUENCY

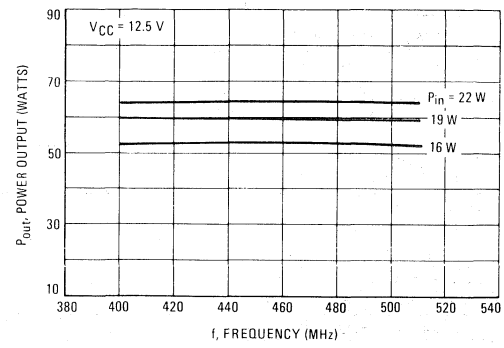


FIGURE 4 – POWER OUTPUT versus SUPPLY VOLTAGE

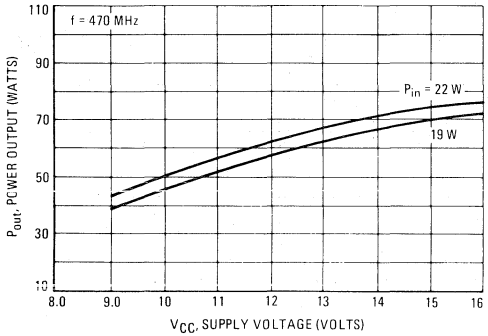


FIGURE 5 – POWER SATURATION PROFILE

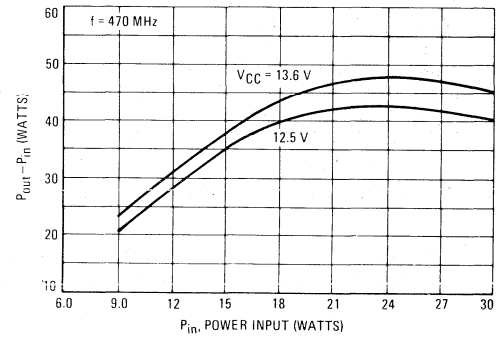
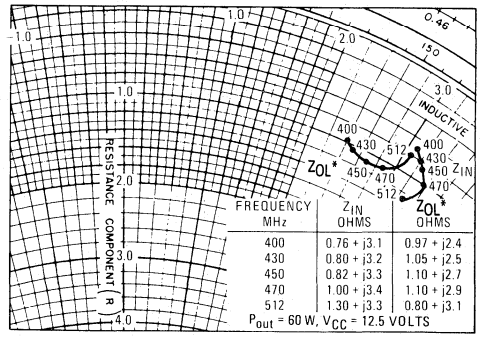


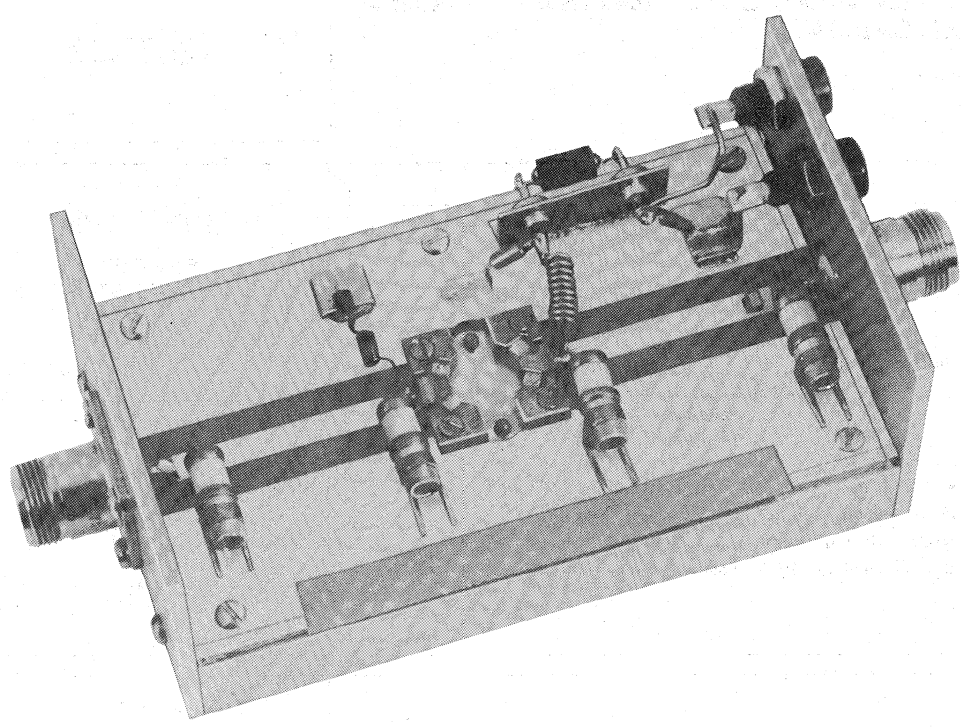
FIGURE 6 – SERIES EQUIVALENT INPUT-OUTPUT IMPEDANCE



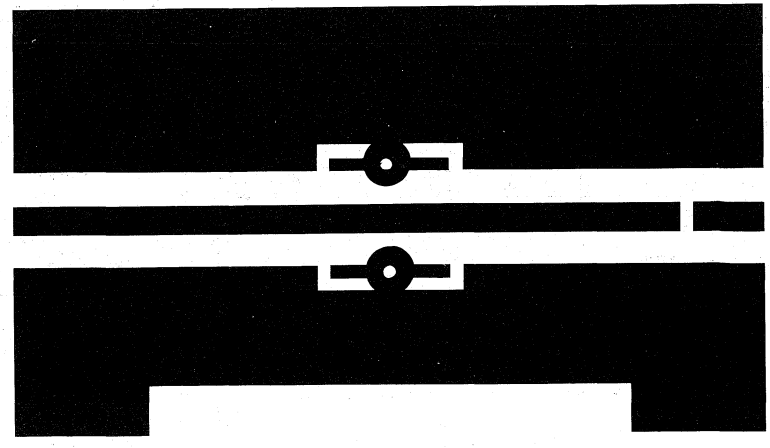
FREQUENCY MHz	Z_{IN} OHMS	Z_{OL}* OHMS
400	0.76 + j3.1	0.97 + j2.4
430	0.80 + j3.2	1.05 + j2.5
450	0.82 + j3.3	1.10 + j2.7
470	1.00 + j3.4	1.10 + j2.9
512	1.30 + j3.3	0.80 + j3.1

P_{out} = 60 W, V_{CC} = 12.5 VOLTS

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.



TEST CIRCUIT TEST FIXTURE



NOTE: The Printed Circuit Board shown is 75% of the original.

MRF652

The RF Line

NPN SILICON RF POWER TRANSISTOR

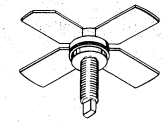
. . . designed for 12.5 Vdc UHF large-signal, amplifier applications in industrial and commercial FM equipment operating to 512 MHz.

- Guaranteed 12.5 Volt, 512 MHz Characteristics
  Output Power = 5.0 Watts
  Minimum Gain = 10 dB
  Efficiency = 65% (Typ)
- Typical Performance at 870 MHz, 12.5 V, 5.0 W Output = 6.0 dB
- Series Equivalent Large-Signal Characterization
- Gold Metallized, Emitter Ballasted for Long Life and Reliability
- Capable of 30:1 VSWR Load Mismatch at 15.5 V Supply Voltage

5.0 W 512 MHz

RF POWER TRANSISTOR

NPN SILICON



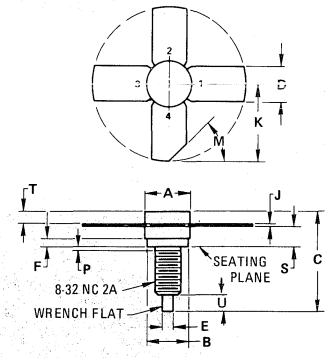
3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	2.0	Adc
Total Device Dissipation @ T_C = 25°C Derate Above 25°C	P_D	25 143	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	7.0	°C/W



STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

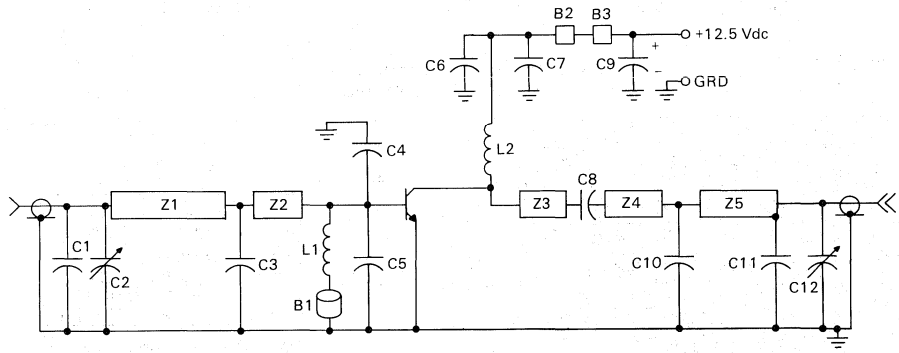
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.06	7.26	0.278	0.286
B	6.20	6.50	0.244	0.256
C	14.99	16.51	0.590	0.650
D	5.46	5.97	0.215	0.235
E	1.40	1.65	0.055	0.065
F	1.52	–	0.060	–
J	0.08	0.18	0.003	0.007
K	11.05	–	0.435	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
S	3.00	3.25	0.118	0.128
T	1.40	1.78	0.055	0.070
U	2.92	3.68	0.115	0.145

CASE 244-04

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 25 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 25 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 25 mAdc, I_E = 0)	$V_{(BR)CBO}$	36	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0)	I_{CES}	—	—	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 200 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	—	150	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	9.5	15	pF
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 5.0 W) f = 512 MHz f = 870 MHz	G_{pe}	10 —	11 6.0	— —	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 5.0 W, f = 512 MHz)	η	—	65	—	%
Load Mismatch (V_{CC} = 15.5 Vdc, P_{out} = 6.0 W, f = 512 MHz, VSWR 30:1 At All Phase Angles)	ψ	No Degradation in Output Power			

FIGURE 1 — 440-512 MHz BROADBAND TEST CIRCUIT



B1–B3 — Ferrite Bead
C1 — 7.0 pF Unelco Mica
C2 — 1.0–6.0 pF Johanson Variable 5201
C3 — 15 pF Unelco Mica
C4 — 43 pF Mini-Underwood Mica
C5 — 56 pF Mini-Underwood Mica
C6 — 1000 pF Unelco Mica
C7 — 0.1 μF Ceramic
C8 — 68 pF Mini-Underwood Mica
C9 — 1.0 μF Electrolytic 25 V
C10, C11 — 5.0 pF Unelco Mica
C12 — 1.0–10 pF Johanson Variable 5501
L1, L2 — 6 Turns, 20 AWG Wire 0.125" ID
Z1, Z2 — 25 Ohm μStripline (See Photo-Mask - Figure 7)
Z3–Z5 — 50 Ohm μStripline (See Photo-Mask - Figure 7)
Board — 0.032" Glass-Teflon

FIGURE 2 — OUTPUT POWER versus INPUT POWER

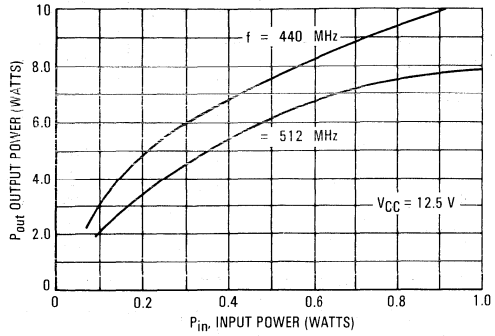


FIGURE 3 — OUTPUT POWER versus FREQUENCY

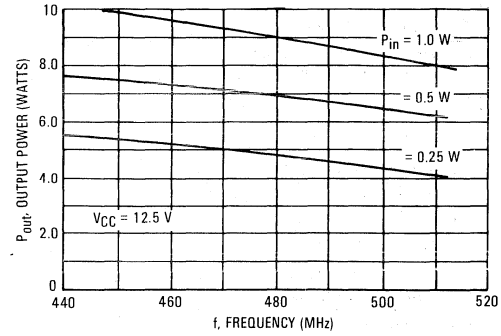


FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE

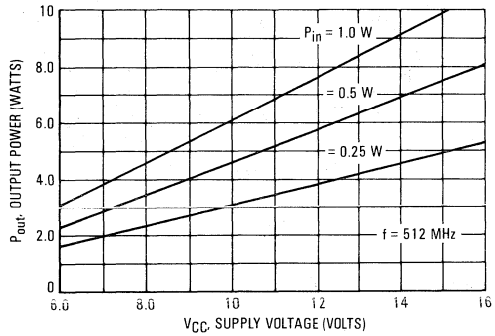


FIGURE 5 — TYPICAL BROADBAND CIRCUIT PERFORMANCE

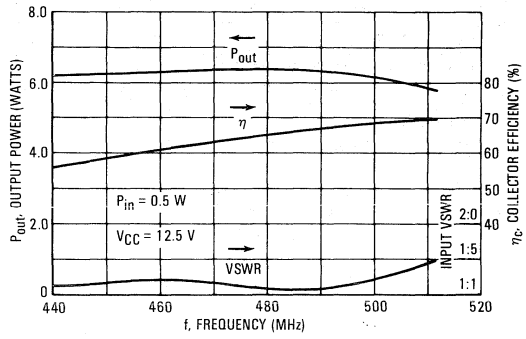
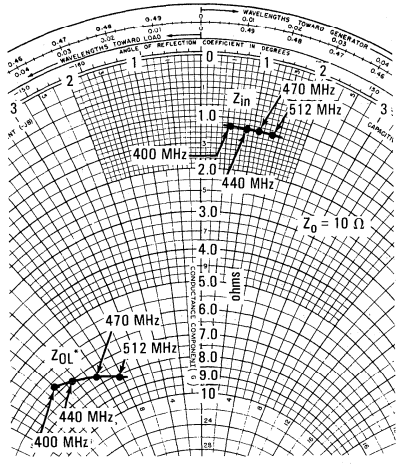


FIGURE 6 — SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCE

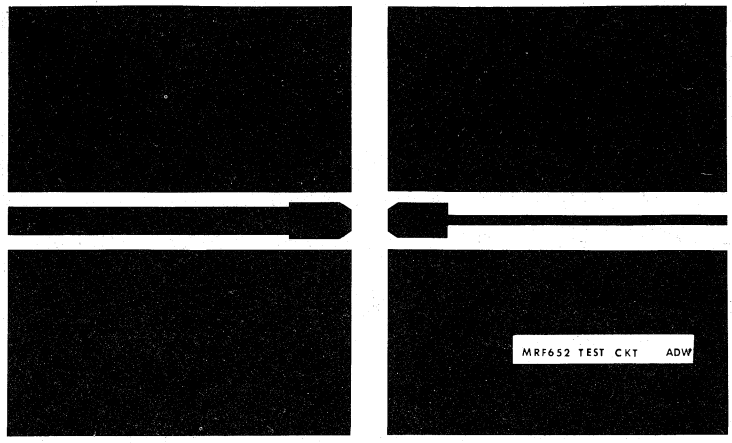


V_{CC} = 12.5 Vdc
P_{out} = 5.0 W

f MHz	Z_{in} Ohms	Z_{OL}^* Ohms
400	1.18 + j0.54	6.7 – j6.9
440	1.19 + j0.88	7.05 – j6.1
470	1.19 + j1.11	7.6 – j5.1
512	1.19 + j1.35	8.1 – j4.1

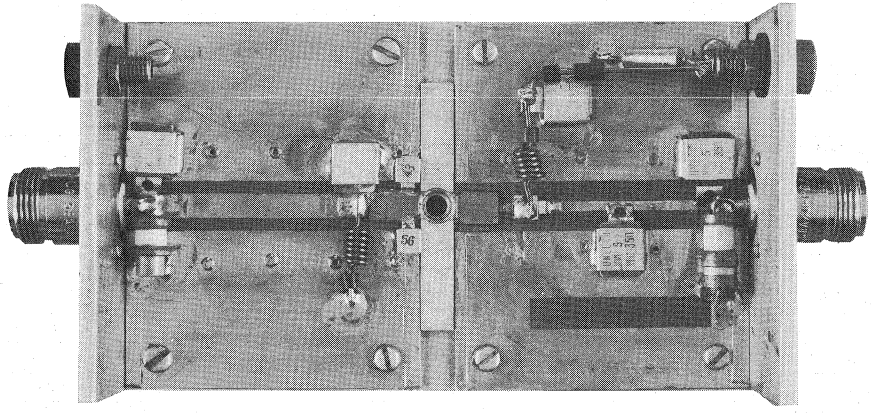
*Z_{OL} = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

FIGURE 7 — PHOTOMASTER BROADBAND TEST CIRCUIT



NOTE: The Printed Circuit Board shown is 75% of the original.

FIGURE 8 — BROADBAND TEST CIRCUIT



MRF653

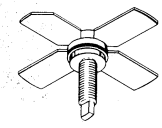
10 W 512 MHz RF POWER TRANSISTOR NPN SILICON

The RF Line

NPN Silicon RF Power Transistor

. . . designed for 12.5 Volt UHF large-signal amplifier applications in industrial and commercial FM equipment operating to 512 MHz.

- Specified 12.5 Volt, 512 MHz Characteristics
  - Output Power = 10 W
  - Gain = 8 dB (Typ)
  - Efficiency = 65% (Typ)
- Gold Metallized, Emitter Ballasted for Long Life and Reliability
- Capable of 20:1 VSWR Load Mismatch at 16 V Supply Voltage



CASE 244-04
CERAMIC

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16.5	Vdc
Collector-Base Voltage	V_{CBO}	38	Vdc
Emitter-Base Voltage	V_{EBO}	4	Vdc
Collector-Current — Continuous	I_C	2.75	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	44 0.25	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	16.5	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	38	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 5 mAdc, I_C = 0)	$V_{(BR)EBO}$	4	—	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0)	I_{CES}	—	—	5	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1 Adc, V_{CE} = 5 Vdc)	h_{FE}	20	—	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1 MHz)	C_{ob}	—	22	28	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 10 W, f = 512 MHz)	G_{pe}	7	8	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 10 W, f = 512 MHz)	η_c	55	65	—	%
Load Mismatch Stress (V_{CC} = 16 Vdc, f = 512 MHz, P_{in}* = 2.6 W, VSWR = 20:1 All Phase Angles)	ψ	No Degradation in Output Power			

*P_{in} = 2 dB over the typical input power required for 10 W output power @ 12.5 Vdc

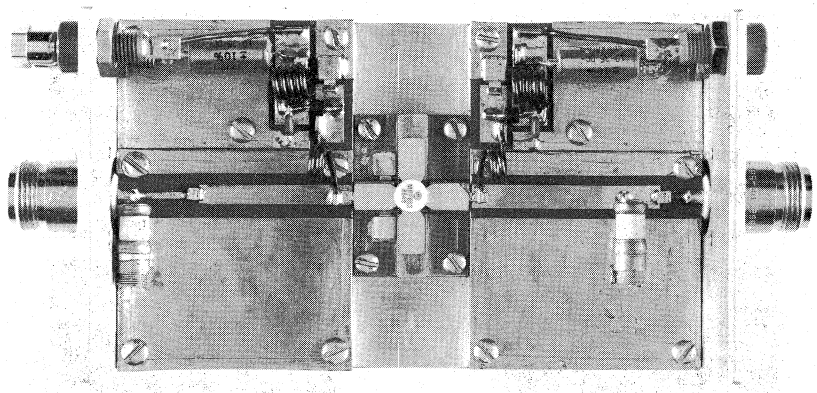
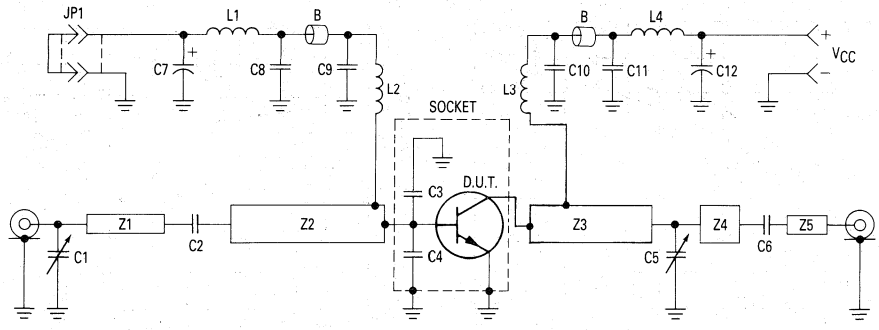


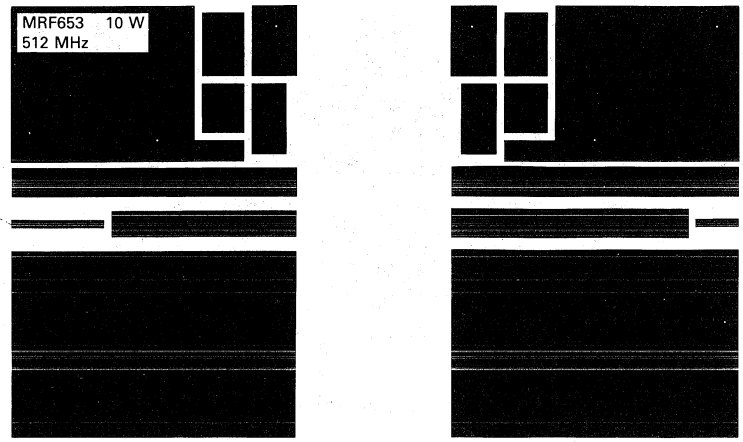
Figure 1. Broadband Test Circuit



C1, C5 — 1–20 pF, Johanson
C2, C6 — 330 pF, 100 Mil ATC
C3, C4 — 36 pF, Mini-Unelco
C7, C12 — 10 μF, 35 V, Tantalum
C8, C11 — 0.1 μF, Ceramic
C9, C10 — 91 pF, Mini-Unelco

L1, L4 — 4-1/2 Turns, #18 AWG, 0.16″ ID
L2, L3 — 2 Turns, #18 AWG, 0.16″ ID
B — Ferrite Bead, Ferroxcube 56-590-65-3B
Z1 — 51 x 630 mils
Z2 — 162 x 1300 mils
Z3 — 210 x 1350 mils
Z4 — 210 x 280 mils
Z5 — 51 x 300 mils
Board Material — 0.032″ epoxy glass G10, 1 oz., copper clad, double sided, ϵ_r = 5
JP1 — Jumper, #14 AWG w/Banana Plugs

Figure 2. Broadband Test Circuit Schematic



NOTE: The Printed Circuit Board shown is 75% of the original.

Figure 3. Photomaster

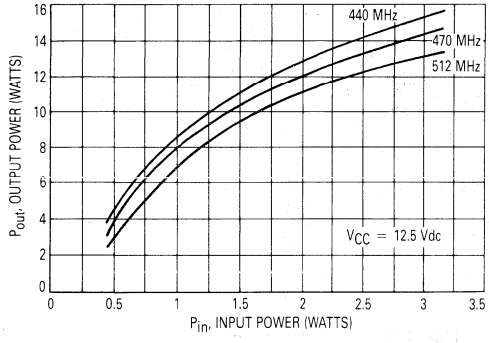


Figure 4. Output Power versus Input Power

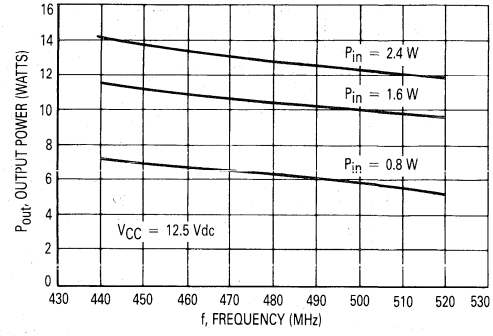


Figure 5. Output Power versus Frequency

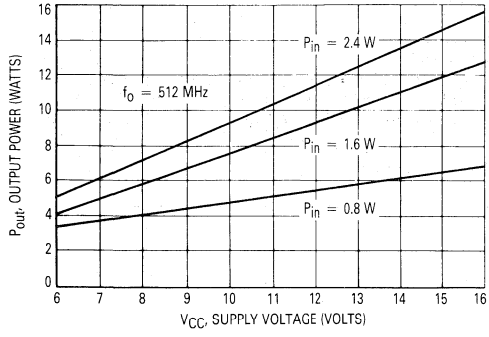


Figure 6. Output Power versus Supply Voltage

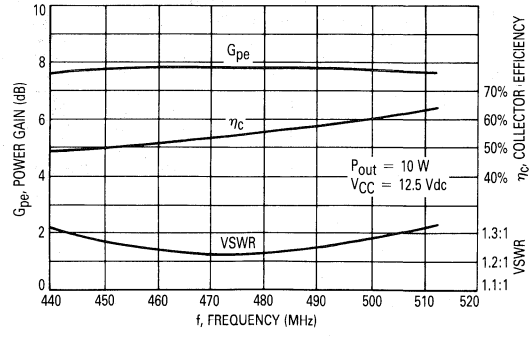


Figure 7. Typical Broadband Circuit Performance

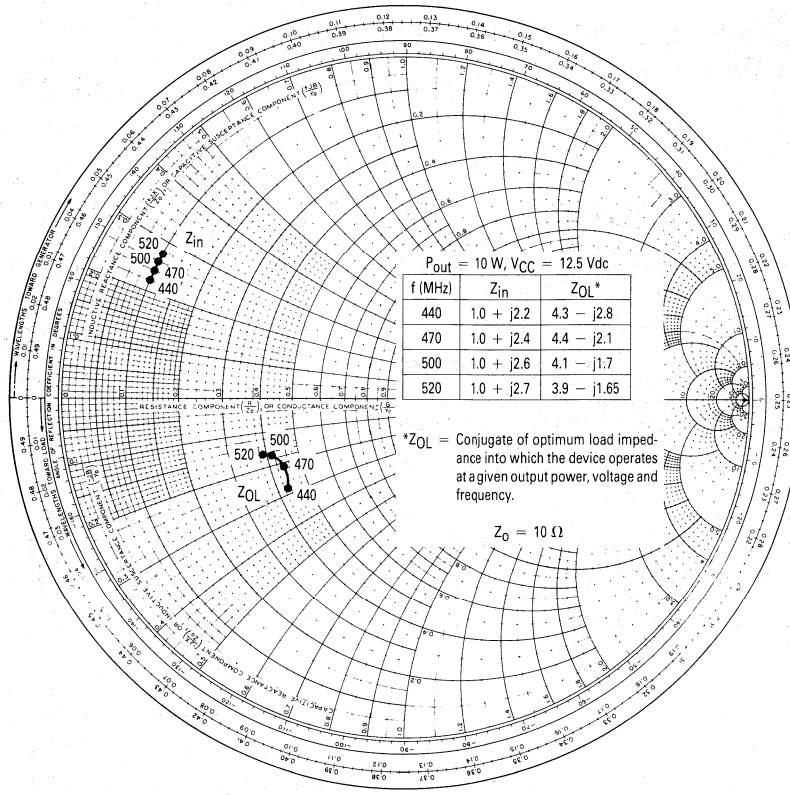
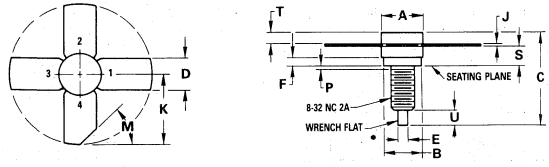


Figure 8. Series Equivalent Input and Output Impedance

OUTLINE DIMENSIONS

CASE 244-04
CERAMIC



STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.06	7.26	0.278	0.286
B	6.20	6.50	0.244	0.256
C	14.99	16.51	0.590	0.650
D	5.46	5.96	0.215	0.235
E	1.40	1.65	0.055	0.065
F	1.52	—	0.060	—
J	0.08	0.17	0.003	0.007
K	11.05	—	0.435	—
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
S	3.00	3.25	0.118	0.128
T	1.40	1.77	0.055	0.070
U	2.92	3.68	0.115	0.145

MRF654

The RF Line

15 W 470 MHz

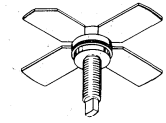
RF POWER TRANSISTOR

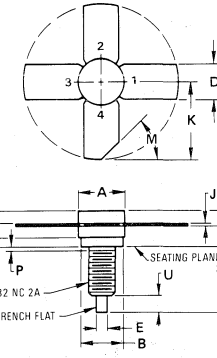
NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed for 12.5 Volt UHF large-signal amplifier applications in industrial and commercial FM equipment operating to 512 MHz.

- Specified 12.5 Volt, 512 MHz Characteristics
  Output Power = 15 W
  Minimum Gain = 7.8 dB
  Efficiency = 55%
- Built-In Matching Network for Broadband Operation
- Gold Metallized, Emitter Ballasted for Long Life and Reliability
- Capable of 20:1 VSWR Load Mismatch at 15.5 V Supply Voltage





STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.06	7.26	0.278	0.286
B	6.20	6.50	0.244	0.256
C	14.99	16.51	0.590	0.650
D	5.46	5.96	0.215	0.235
E	1.40	1.65	0.055	0.065
F	1.52	–	0.060	–
J	0.08	0.17	0.003	0.007
K	11.05	–	0.435	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
S	3.00	3.25	0.118	0.128
T	1.40	1.77	0.055	0.070
U	2.92	3.68	0.115	0.145

CASE 244-04

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Continuous	I_C	4.0	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	44 0.25	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

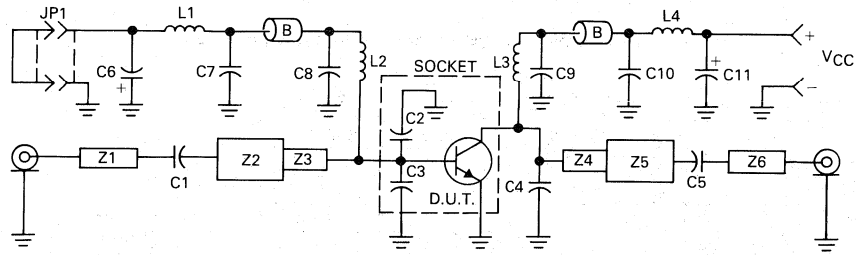
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 25 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 25 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector-Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0)	I_{CES}	—	—	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	—	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	31	45	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 15 W, f = 512 MHz)	G_{pe}	7.8	8.8	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 15 W, f = 512 MHz)	η	55	63	—	%
Load Mismatch Stress (V_{CC} = 15.5 Vdc, f = 470 MHz, 2.0 dB Overdrive, VSWR = 20:1 All Phase Angles)	ψ	No Degradation In Output Power			

FIGURE 1 — 440–512 MHz BROADBAND TEST CIRCUIT



C1, C5 — 68 pF Mini-Unelco
C2, C3 — 33 pF, Mini-Unelco
C4 — 47 pF, Mini-Unelco
C6, C11 — 10 μF, 25 V Tantalum
C7, C10 — 0.1 μF, Ceramic
C8, C9 — 91 pF, Mini-Unelco
L1, L4 — 4½ Turns, #18 AWG, Enamel Covered, 0.16″ ID
L2, L3 — 2 Turns, #18 AWG Enamel Covered, 0.16″ ID
B — Ferrite Bead, Ferroxcube 56-590-65-3B
Z1-Z6 — See PCB Artwork
PCB — 1/32″ G-10, E_r = 4.5 @ UHF
Socket — See Socket Drawings
JP1 — Jumper, #14 AWG w/Banana Plugs

FIGURE 2 — OUTPUT POWER versus INPUT POWER

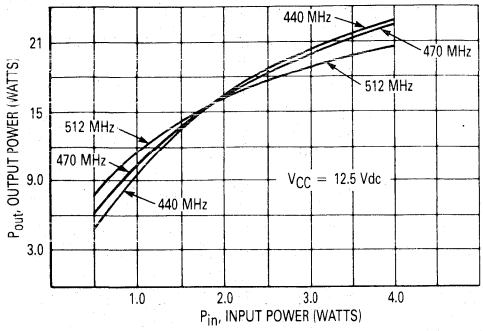


FIGURE 3 — OUTPUT POWER versus FREQUENCY

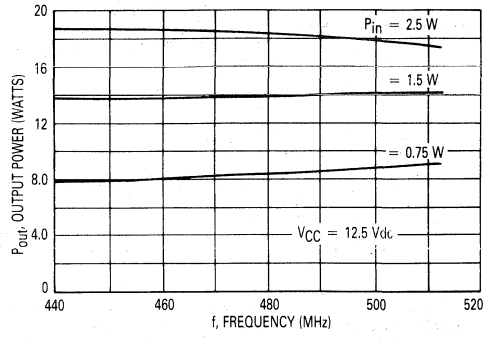


FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE

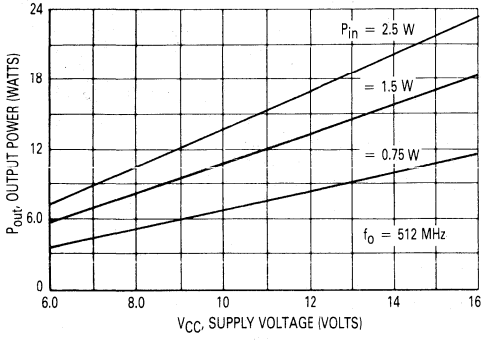


FIGURE 5 — TYPICAL BROADBAND CIRCUIT PERFORMANCE

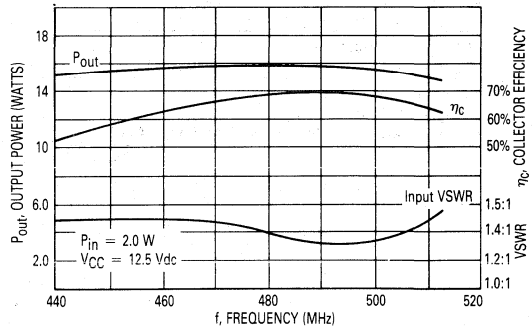
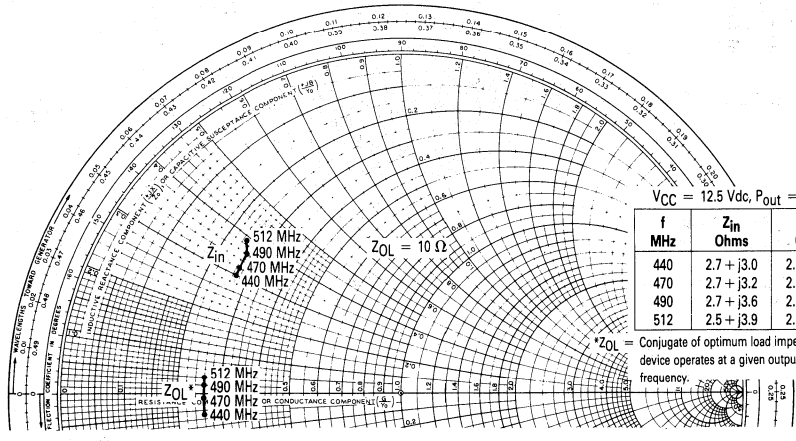


FIGURE 6 — SERIES EQUIVALENT INPUT AND OUTPUT IMPEDANCE



V_{CC} = 12.5 Vdc, P_{out} = 15 W

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
440	2.7 + j3.0	2.6 − j0.5
470	2.7 + j3.2	2.6 − j0.1
490	2.7 + j3.6	2.6 + j0.2
512	2.5 + j3.9	2.6 + j0.4

*Z_{OL} = Conjugate of optimum load impedance into which the device operates at a given output power, voltage and frequency.

FIGURE 7 — 440–512 MHz BROADBAND TEST CIRCUIT

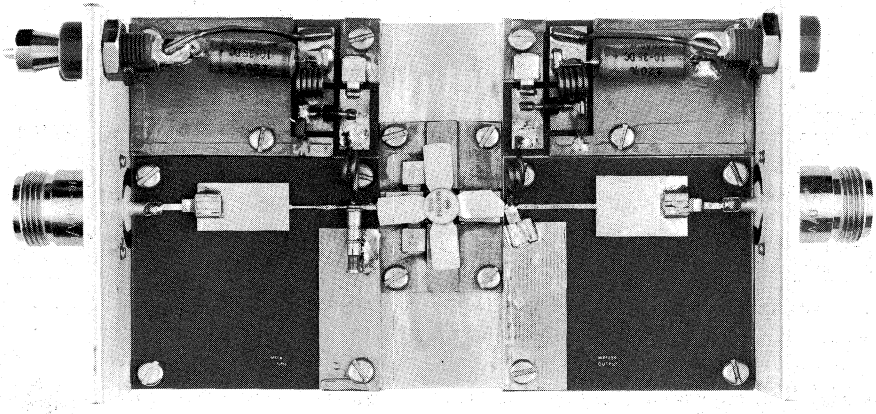
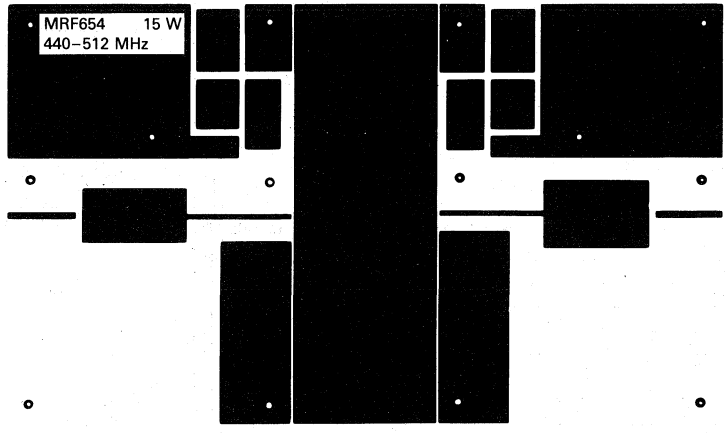


FIGURE 8 — PCB BOARD LAYOUT



NOTE: The Printed Circuit Board shown is 75% of the original.

MRF660

The RF Line

NPN SILICON RF POWER TRANSISTOR

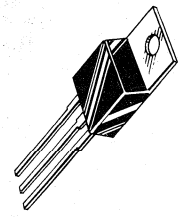
. . . designed for 12.5 volt UHF large signal power amplifier applications in commercial and industrial FM equipment.

- Low Cost Common Emitter TO-220 Package
- Specified 12.5 V, 470 MHz Performance
  Output Power = 7.0 W
  Power Gain = 5.4 dB Min
  Efficiency — 60% Min
- Load Mismatch Capability at High Line and RF Input Overdrive

7.0 W 470 MHz

RF POWER TRANSISTOR

NPN SILICON



3

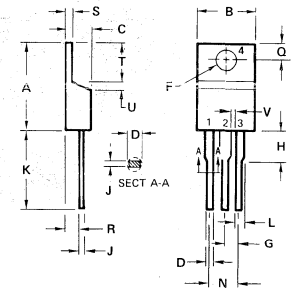
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Continuous	I_C	2.4	Adc
Total Device Dissipation @ $T_C = 25^oC$ (1) Derate above 25^oC	P_D	25 143	Watts $mW/^oC$
Storage Temperature Range	T_{stg}	−65 to +150	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	7.0	$^oC/W$

(1) This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF amplifier.



NOTE:
1. DIM. L & H APPLIES TO ALL LEADS.

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

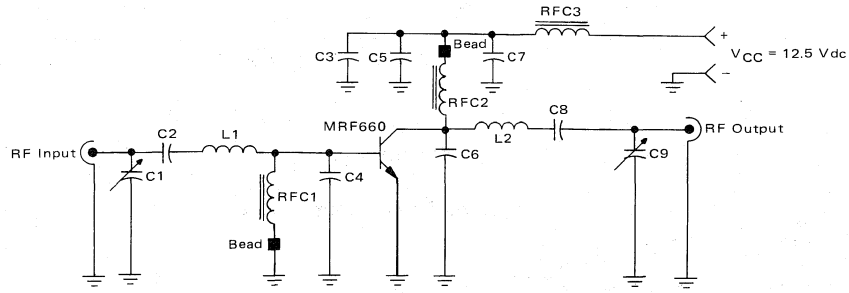
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	–	–	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	20	90	160	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	17	25	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 7.0 W, f = 470 MHz)	G_{PE}	5.4	6.0	–	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 7.0 W, f = 470 Mhz)	η	60	–	–	%

FIGURE 1 – TEST CIRCUIT



C1, C9 – 1–10 pF Johanson
C2, C8 – 15 pF Underwood Elect. Co. Type J101
C3 – 270 pF, ATC Chip Capacitor Case B
C4, C6 – 24 pF ELMENCO MCN01/010
C5 – 0.1 μF Ceramic, Erie
C7 – 1.0 μF, 35 V, Tantalum
L1 – 27 nH Copper Strap 0.150" X 0.025" X 1.5" (See Note)
L2 – 16 nH Copper Strap 0.150" X 0.025" X 1.0" (See Note)
RFC1 – 0.68 μH Molded Choke, Cambion
RFC2 – 4 Turns #20 AWG, 0.312" ID X 0.25" Long
RFC3 – Ferrite Choke, Ferroxcube #VK200-20/4B
Bead – Ferrite Bead, Ferroxcube #56-590-65-3B
Printed Circuit Board Material – 3M #K6098-22062, Teflon Fiberglass or equivalent

NOTE:

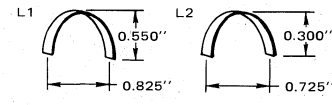


FIGURE 2 – OUTPUT POWER versus INPUT POWER

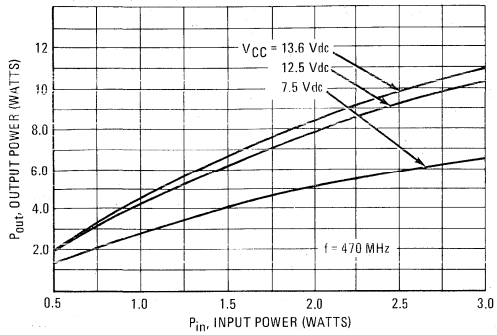


FIGURE 3 – OUTPUT POWER versus FREQUENCY

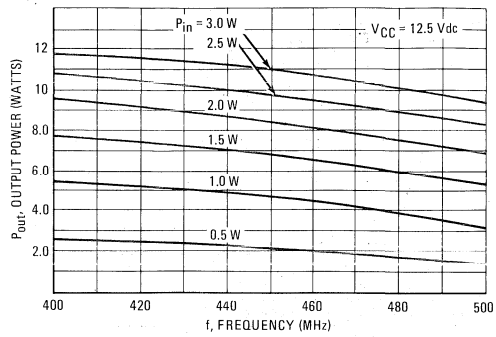


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

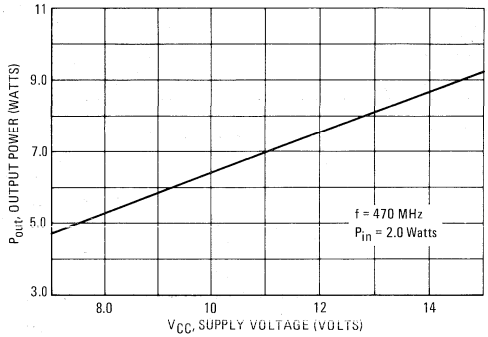
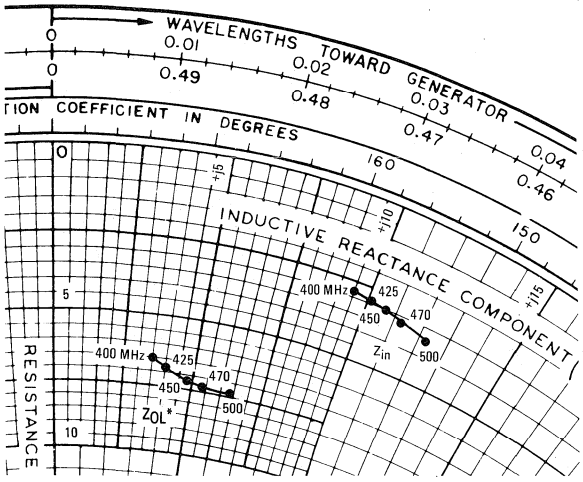


FIGURE 5 – SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCES



P_{in} = 2.0 W, V_{CC} = 12.5 V

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
400	2.8 + j9.0	6.5 + j3.5
425	2.9 + j10.1	6.8 + j4.0
450	3.0 + j10.5	7.2 + j4.8
470	3.1 + j11.2	7.3 + j5.4
500	3.4 + j12.2	7.3 + j6.4

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

FIGURE 6 – UHF TEST AMPLIFIER

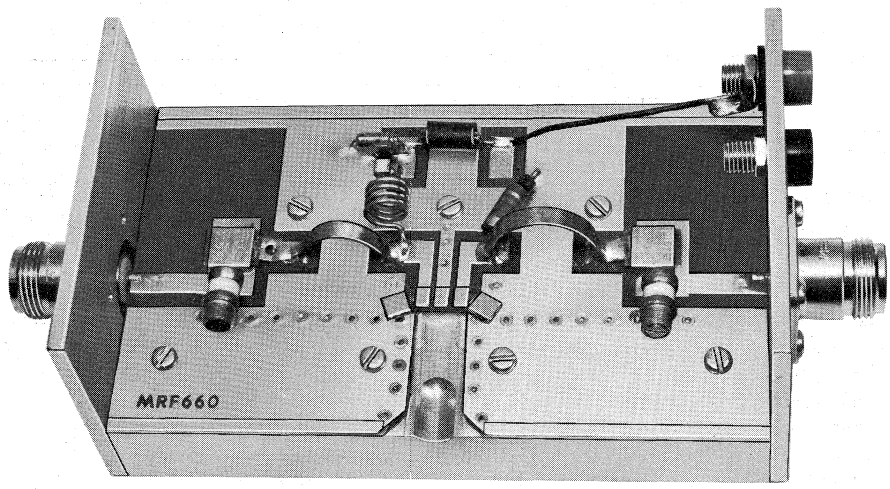
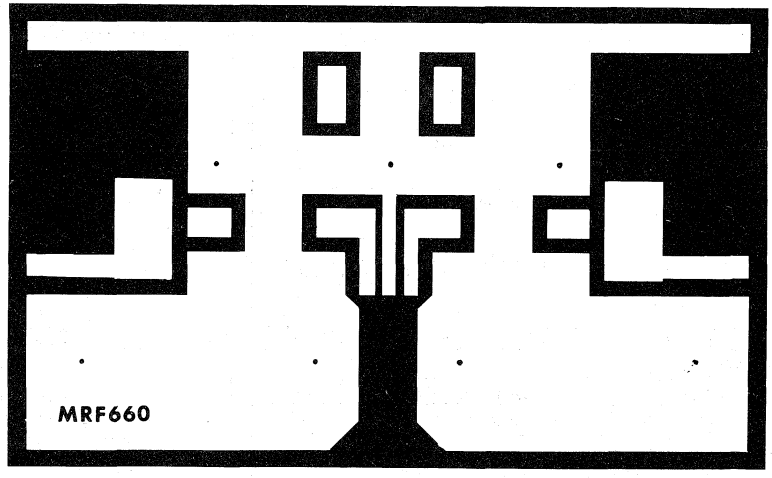


FIGURE 7 – PRINTED CIRCUIT BOARD



NOTE: The Printed Circuit Board shown is 75% of the original.

MRF750

The RF Line

NPN SILICON HIGH FREQUENCY TRANSISTOR

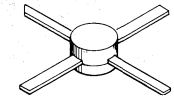
. . . designed for 5.0 to 10 Volt UHF large-signal amplifier applications in industrial and commercial FM equipment operating in the 407 to 512 MHz range. Ideally suited for handheld radios and other equipment where high packaging density is required.

- Specified 7.5 Volt, 470 MHz Characteristics —
  Output Power = 0.5 Watts
  Minimum Gain = 10 dB
  Minimum Efficiency = 55%
- Capable of Withstanding Load Mismatch at Highline and RF Overdrive
- Silicon Nitride Passivation

0.5 W — 470 MHZ — 7.5 V

HIGH FREQUENCY TRANSISTOR

NPN SILICON



3

MAXIMUM RATINGS

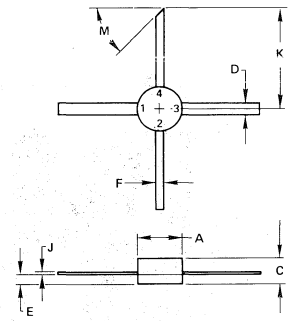
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	13	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current-Continuous	I_C	200	mAdc
Total Device Dissipation @ T_C = 25°C (1) Derate Above 25°C	P_D	2.5 35	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +150°C	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	28.5	°C/W

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

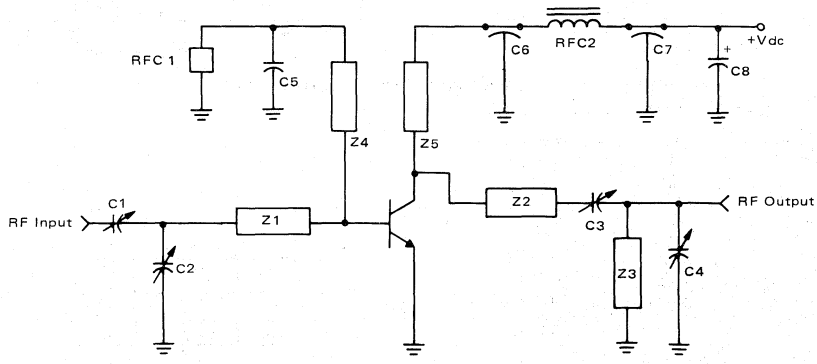
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.08	5.59	0.200	0.220
C	2.41	3.30	0.095	0.130
D	1.40	1.65	0.055	0.065
E	1.02	1.27	0.040	0.050
F	0.64	0.89	0.025	0.035
J	0.08	0.18	0.003	0.007
K	11.05	–	0.435	–
M	45° NOM		45° NOM	

Case 305A-01

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	$V_{(BR)CEO}$	13	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	25	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 9.0 Vdc, I_E = 0)	I_{CBO}	–	–	0.5	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 50 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	20	65	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 7.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	3.0	5.0	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 7.5 Vdc, P_{out} = 0.5 W, f = 470 MHz)	G_{PE}	10	11	–	dB
Collector Efficiency (V_{CC} = 7.5 Vdc, P_{out} = 0.5 W, f = 470 MHz)	η	55	–	–	%

FIGURE 1 – 470 MHz TEST CIRCUIT



C1, C2, C3, C4, – Johanson Trimmer, JMC#5501
C5 – J101, 100 pF Unelco
C6, C7 – 680 pF Allen Bradley Feedthru
C8 – 1.0 μF Tantalum
RFC1 – Ferroxcube Bead, 56-590-65-3B
RFC2 – Choke, VK 200/4B

Z1, Z2 – Microstrip W = 0.26", L = 2.9"
Z3 – Microstrip W = 0.5", L = 1.2"
Z4 – Microstrip W = 0.055", L = 3.9"
Z5 – Microstrip W = 0.055", L = 2.9"
Board Material – Glass Teflon, t = 0.062
ϵ_r = 2.5

FIGURE 2 – POWER GAIN versus FREQUENCY

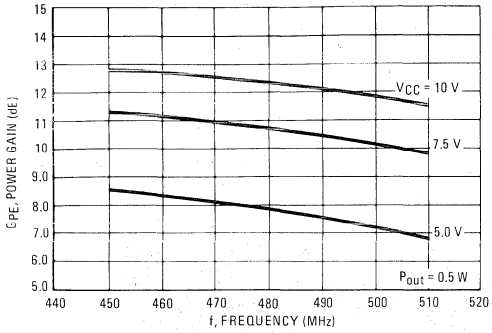


FIGURE 3 – OUTPUT POWER versus INPUT POWER
450 MHz

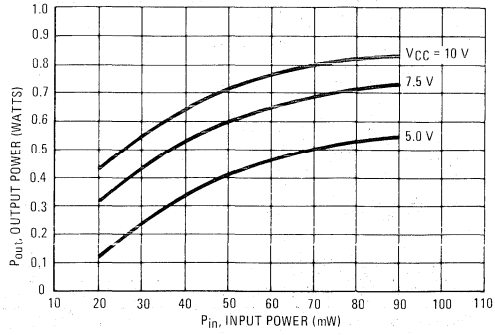


FIGURE 4 – OUTPUT POWER versus INPUT POWER
470 MHz

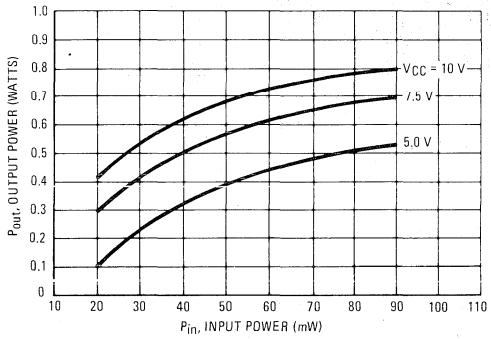


FIGURE 5 – OUTPUT POWER versus INPUT POWER
512 MHz

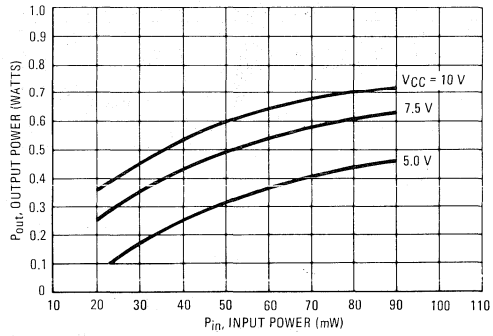
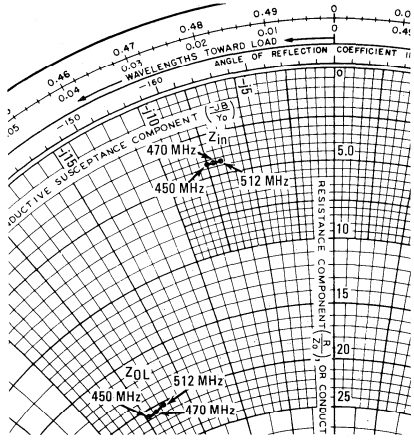


FIGURE 6 – SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCES

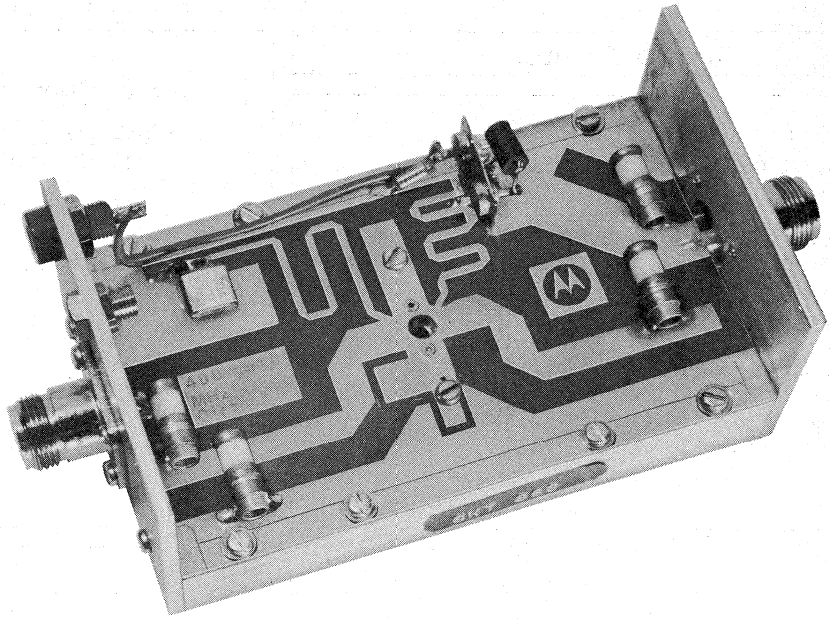


Pout = 0.5 W VCC = 7.5 V

f MHz	Zin Ohms	ZOL* Ohms
450	4.4 –j7.5	20.9 –j19.7
470	4.4 –j7.1	20.7 –j18.9
512	4.4 –j6.7	20.1 –j17.6

*ZOL = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

FIGURE 7 – 470 MHz TEST CIRCUIT



MRF752

The RF Line

2.5 W — 470 MHZ — 7.5 V

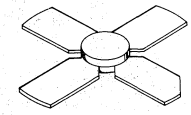
HIGH FREQUENCY TRANSISTOR

NPN SILICON

NPN SILICON HIGH FREQUENCY TRANSISTOR

. . . designed for 5.0 to 10 Volt UHF large-signal amplifier applications in industrial and commercial FM equipment operating in the 407 to 512 MHz range. Ideally suited for handheld radios and other equipment where high packaging density is required.

- Specified 7.5 Volt, 470 MHz Characteristics —
  Output Power = 2.5 Watts
  Minimum Gain = 8.0 dB
  Minimum Efficiency = 55%
- Capable of Withstanding Load Mismatch at High Line and RF Overdrive



MAXIMUM RATINGS

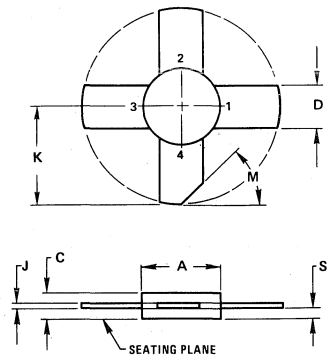
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	13	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current-Continuous	I_C	1.2	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate Above 25°C	P_D	15 85.5	Watts mW/°C
Storage Temperature Range	T_{stg}	−65 to +150°C	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	11.7	°C/W

(1) These devices are designed for RF operation. The total device dissipation rating applied only when the devices are operated as RF amplifiers.

(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

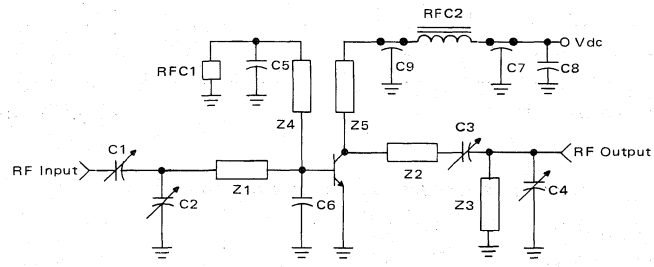
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.06	7.26	0.278	0.286
C	2.84	3.45	0.112	0.136
D	5.46	5.97	0.215	0.235
J	0.08	0.18	0.003	0.007
K	11.05	–	0.435	–
M	45° NOM		45° NOM	
S	1.40	1.65	0.055	0.065

CASE 249-05

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 25 mAdc, I_B = 0)	$V_{(BR)CEO}$	13	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 25 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	25	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 3.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 9.0 Vdc, I_E = 0)	I_{CBO}	–	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	20	85	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 7.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	27	35	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 7.5 Vdc, P_{out} = 2.5 W, f = 470 MHz)	G_{PE}	8.0	9.0	–	dB
Collector Efficiency (V_{CC} = 7.5 Vdc, P_{out} = 2.5 W, f = 470 MHz)	η	55	–	–	%

FIGURE 1 – 470 MHz TEST CIRCUIT



C1, C2, C3, C4 – Johanson Trimmer JMC#5501
C5 – J101, 100 pF Unelco
C6 – J101, 15 pF Unelco
C7, C9 – 680 pF Allen Bradley Feedthru
C8 – 1.0 μF Tantalum

Z1, Z2 – Microstrip W = 0.26", L = 2.9"
Z3 – Microstrip W = 0.5", L = 1.2"
Z4 – Microstrip W = 0.055", L = 3.9"
Z5 – Microstrip W = 0.055", L = 2.9"

RFC1 – Ferroxcube Bead, 56-590-65-3B
RFC2 – Choke, VK 200/4B

Board Material – Glass Teflon
τ = 0.062
ϵ_r = 2.5

FIGURE 2 – POWER GAIN versus FREQUENCY

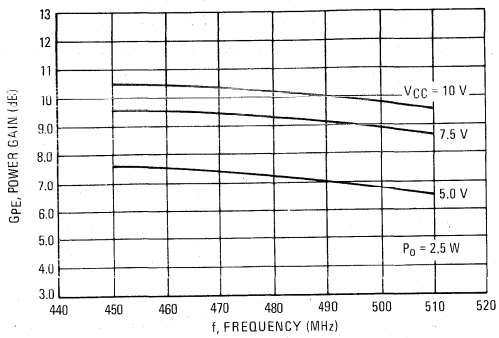


FIGURE 3 – OUTPUT POWER versus INPUT POWER
450 MHz

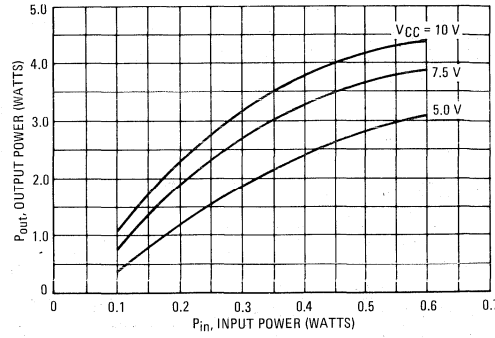


FIGURE 4 – OUTPUT POWER versus INPUT POWER
470 MHz

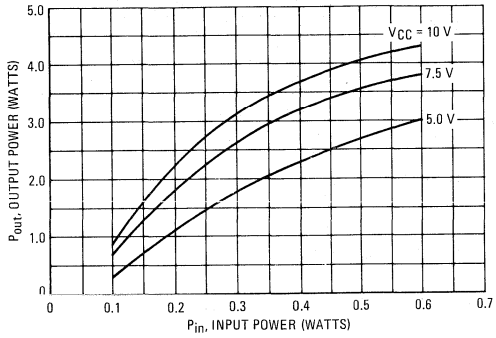


FIGURE 5 – OUTPUT POWER versus INPUT POWER
512 MHz

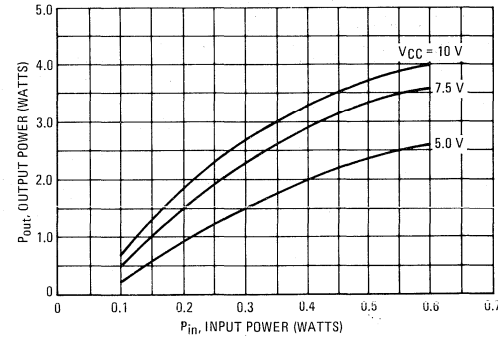
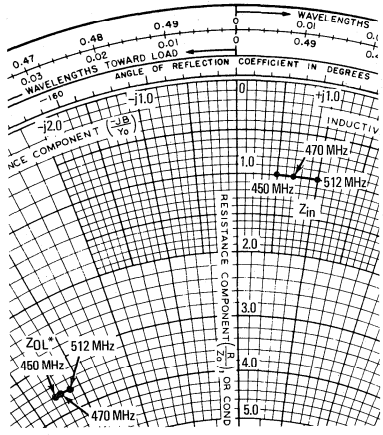


FIGURE 6 – SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCES

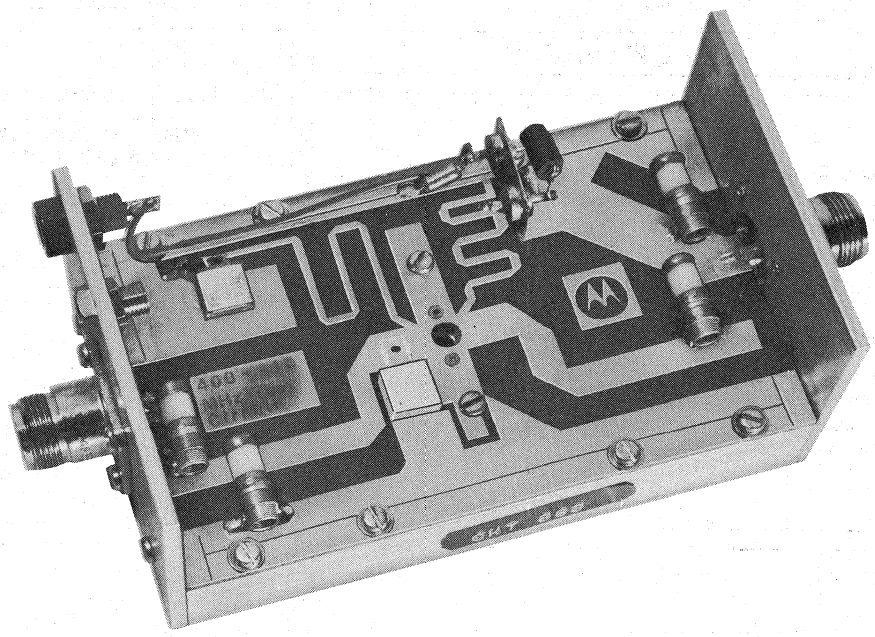


P_{out} = 2.5 W, V_{CC} = 7.5 V

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
450	1.0 +j0.5	3.6 –j3.5
470	1.0 +j0.7	3.6 –j3.4
512	1.0 +j1.0	3.6 –j3.2

*Z_{OL} = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

FIGURE 7 – 470 MHz TEST CIRCUIT



MRF754

The RF Line

8.0 W — 470 MHz — 7.5 V

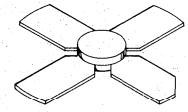
HIGH FREQUENCY TRANSISTOR

NPN SILICON

NPN SILICON HIGH FREQUENCY TRANSISTOR

. . . designed for 5.0 to 10 Volt UHF large-signal amplifier applications in industrial and commercial FM equipment operating in the 407 to 512 MHz range. Ideally suited for handheld radios and other equipment where high packaging density is required.

- Specified 7.5 Volt, 470 MHz Characteristics —
  Output Power = 8.0 Watts
  Minimum Gain = 6.0 dB
  Minimum Efficiency = 55%
- Capable of Withstanding Load Mismatch at Highline and RF Overdrive



3

MAXIMUM RATINGS

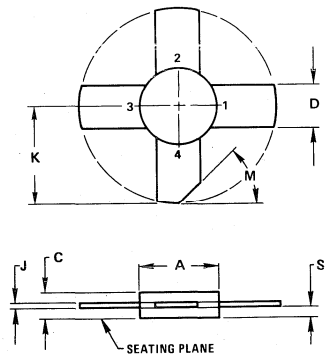
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	13	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Continuous	I_C	3.0	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate Above 25°C	P_D	37.5 214	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +150°C	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	4.7	°C/W

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.



STYLE 2:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

SEATING PLANE = GROUND AND IS CONNECTED TO PIN 1 AND PIN 3.

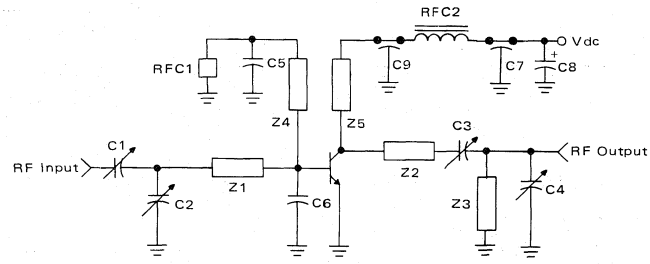
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.06	7.26	0.278	0.286
C	2.84	3.45	0.112	0.136
D	5.46	5.97	0.215	0.235
J	0.08	0.18	0.003	0.007
K	11.05	–	0.435	–
M	45° NOM		45° NOM	
S	1.40	1.65	0.055	0.065

CASE 249-05

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	13	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	25	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 3.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 9.0 Vdc, I_E = 0)	I_{CBO}	—	—	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 200 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	20	85	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 7.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	50	65	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 7.5 Vdc, P_{out} = 8.0 W, f = 470 MHz)	G_{PE}	6.0	7.0	—	dB
Collector Efficiency (V_{CC} = 7.5 Vdc, P_{out} = 8.0 W, f = 470 MHz)	η	55	—	—	%

FIGURE 1 – 470 MHz TEST CIRCUIT



C1, C2, C3, C4 – Johanson Trimmer JMC#5501
C5 – J101, 100 pF Unelco
C6 – J101, 15 pF Unelco
C7, C9 – 680 pF Allen Bradley Feedthru
C8 – 1.0 μF Tantalum

Z1, Z2 – Microstrip W = 0.26", L = 2.9"
Z3 – Microstrip W = 0.5", L = 1.2"
Z4 – Microstrip W = 0.055", L = 3.9"
Z5 – Microstrip W = 0.055", L = 2.9"

RFC1 – Ferroxcube Bead, 56-590-65-3B
RFC2 – Choke, VK 200/4B

Board Material – Glass Teflon
t = 0.062
ϵ_r = 2.5

FIGURE 2 — POWER GAIN versus FREQUENCY

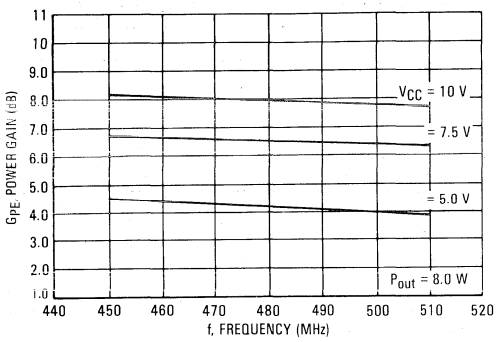


FIGURE 3 — OUTPUT POWER versus INPUT POWER
450 MHz

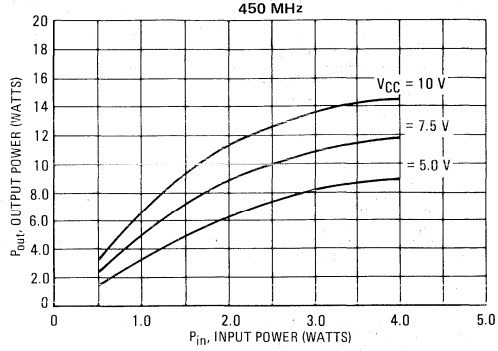


FIGURE 4 — OUTPUT POWER versus INPUT POWER
470 MHz

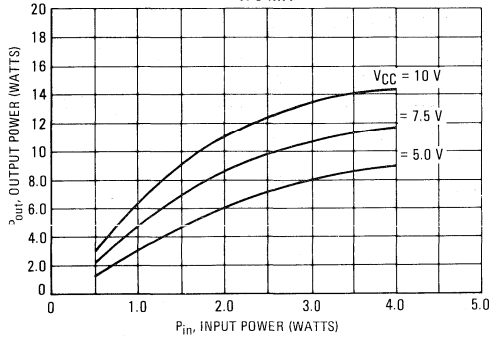


FIGURE 5 — OUTPUT POWER versus INPUT POWER
512 MHz

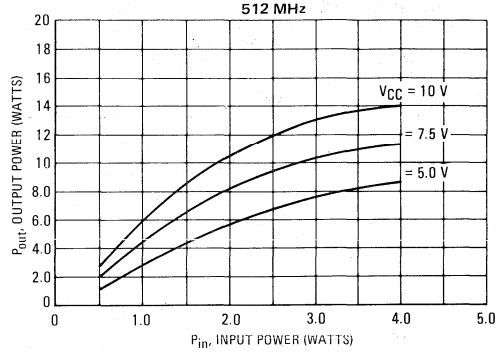
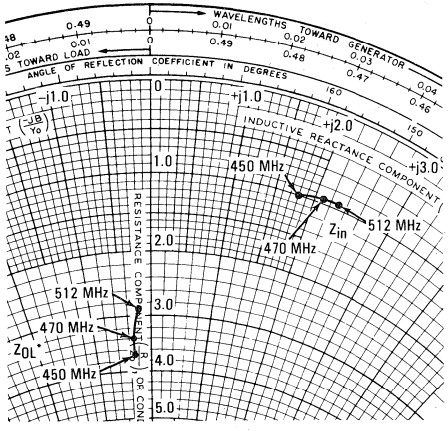


FIGURE 6 — SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCES

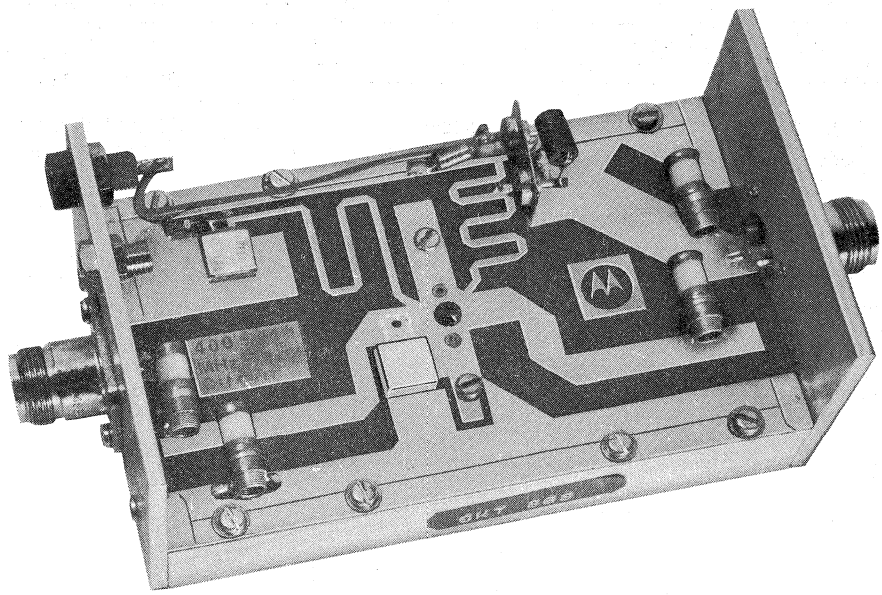


P_{out} = 8.0 W, V_{CC} = 7.5 V

f MHz	Z_{in} Ohms	Z_{OL}^* Ohms
450	1.0 + j1.8	3.7 – j0.3
470	0.9 + j2.1	3.4 – j0.3
512	0.9 + j2.3	2.9 – j0.2

*Z_{OL} = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

FIGURE 7 — 470 MHz TEST CIRCUIT



MRF837

The RF Line

750 mW 870 MHz

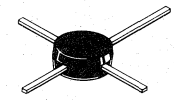
RF LOW POWER TRANSISTOR

NPN SILICON

NPN SILICON RF LOW POWER TRANSISTOR

. . . designed primarily for wideband large signal predriver stages in 800 MHz and UHF frequency ranges.

- Specified @ 12.5 V, 870 MHz Characteristics
  Output Power = 750 mW
  Minimum Gain = 8.0 dB
  Efficiency 60% (Typ)
- Low Cost Macro-X Plastic Package
- State-of-the-Art Technology
  Fine Line Geometry
  Gold Top Metal and Wires
  Silicon Nitride Passivated
  Ion Implanted Arsenic Emitters



Macro-X

3

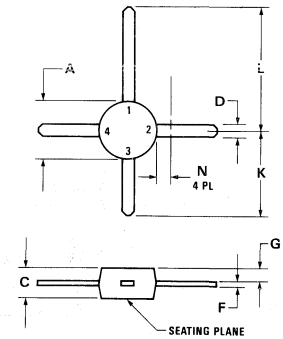
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Continuous	I_C	200	mAdc
Total Device Dissipation @ T_C = 50°C Derate above 50°C (1)	P_D	2.5 25	Watts mW/°C
Storage Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	40	°C/W

(1) Case temperature measured on collector lead immediately adjacent to body of package.



STYLE 2:
PIN 1. COLLECTOR
2. EMITTER
3. BASE
4. EMITTER

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.44	5.21	0.175	0.205
C	1.90	2.54	0.075	0.100
D	0.84	0.99	0.033	0.039
F	0.20	0.30	0.008	0.012
G	0.76	1.14	0.030	0.045
K	7.24	8.13	0.285	0.320
L	10.54	11.43	0.415	0.450
N	–	1.65	–	0.065

NOTE:
DIMENSION D NOT APPLICABLE IN ZONE N.

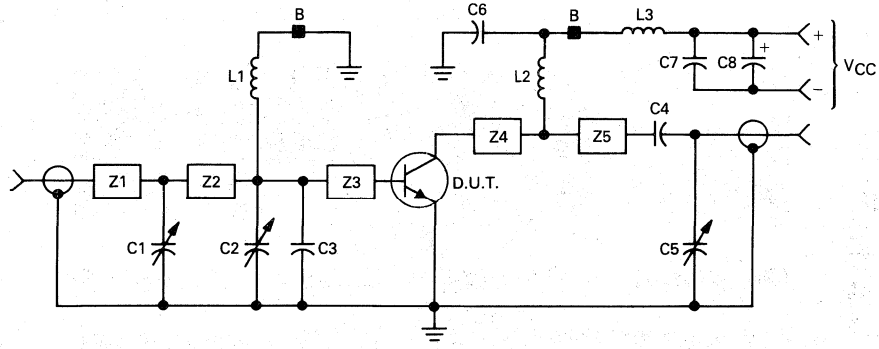
CASE 317-01

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	0.1	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	90	200	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	1.8	2.5	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 0.75 W, f = 870 MHz)	G_{pe}	8.0	10	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 0.75 W, f = 870 MHz)	η	55	60	—	%

3

FIGURE 1 — 800–880 MHz BROADBAND CIRCUIT



C1, C2, C5	— 0.8–8.0 pF Johanson Gigatrim	L1, L2	— 4 Turns, #21 AWG, 5/32″ ID
C3	— 5.0 pF Clamped Mica, Mini-Underwood	L3	— 7 Turns, #21 AWG, 5/32″ ID
C6	— 91 pF Clamped Mica, Mini-Underwood	Z1	— 0.80″ x 0.163″ Microstrip, Z_o = 50 Ω
C4	— 470 pF Ceramic Chip Capacitor	Z2	— 1.375″ x 0.163″ Microstrip, Z_o = 50 Ω
C7	— 68 pF Clamped Mica, Mini-Underwood	Z3, Z4	— 0.375″ x 0.163″ Microstrip, Z_o = 50 Ω
C8	— 1.0 μF 25 V Tantalum	Z5	— 1.35″ x 0.163″ Microstrip, Z_o = 50 Ω
B	— Bead, Ferroxcube 56-590-65/3B	PCB	— 1/16″ Glass Teflon, ϵ_r = 2.56

FIGURE 2 — 800–880 BROADBAND CIRCUIT

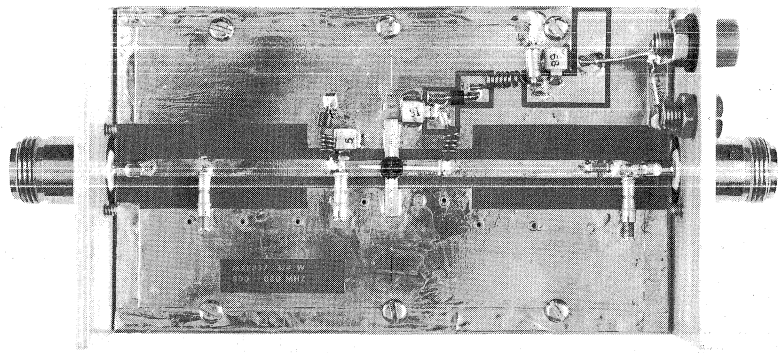
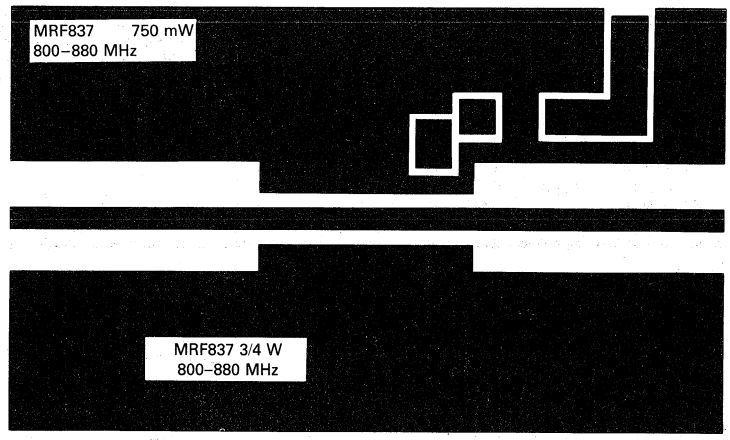


FIGURE 3 — 800–880 MHz BROADBAND CIRCUIT PHOTOMASTER



NOTE: The Printed Circuit Board shown is 75% of the original.

800/900 MHz BAND DATA

FIGURE 4 — BROADBAND PERFORMANCE

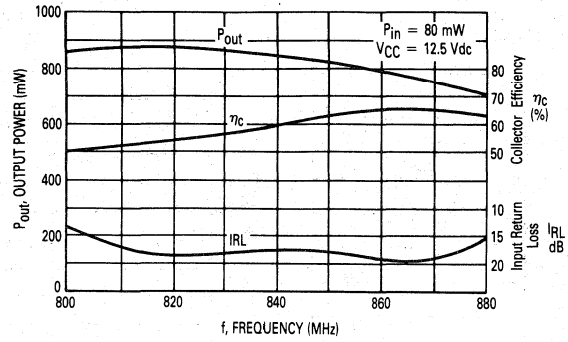


FIGURE 5 — Z_{in} AND Z_{OL} versus COLLECTOR VOLTAGE, INPUT POWER AND OUTPUT POWER

f Frequency MHz	Z_{in} Ohms		Z_{OL}* Ohms	
	V_{CC} = 7.5 V	V_{CC} = 12.5 V	V_{CC} = 7.5 V	V_{CC} = 12.5 V
	P_{in} = 150 mW	P_{in} = 100 mW	P_{out} 806 MHz = 870 mW P_{out} 870 MHz = 820 mW P_{out} 960 MHz = 700 mW	P_{out} 806 MHz = 1.05 W P_{out} 870 MHz = 950 mW P_{out} 960 MHz = 725 mW
806	6.1 + j3.6	4.3 + j0.6	38.3 − j16.4	23.2 − j31.6
870	5.6 + j5.2	6.5 + j3.6	40.8 − j18.9	41.3 − j18.4
960	6.1 + j6.8	6.4 + j4.5	43.8 − j14.7	41.4 − j19.0

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

800/900 MHz BAND DATA (continued)

FIGURE 6 — OUTPUT POWER versus INPUT POWER
f = 870 MHz

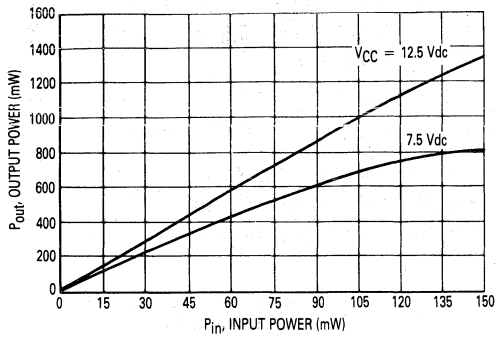


FIGURE 7 — OUTPUT POWER versus FREQUENCY
V_{CC} = 7.5 Vdc

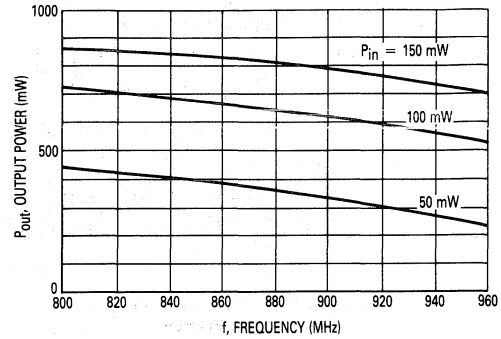


FIGURE 8 — OUTPUT POWER versus COLLECTOR VOLTAGE
f = 870 MHz

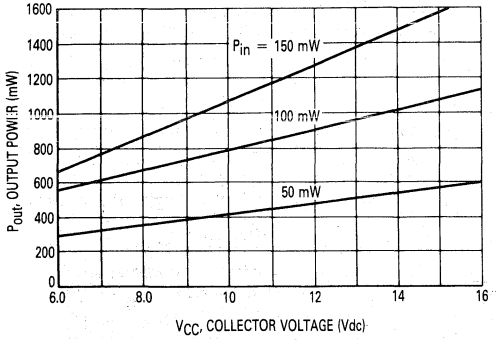
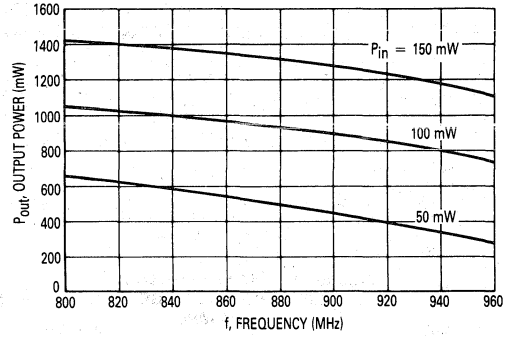


FIGURE 9 — OUTPUT POWER versus FREQUENCY
V_{CC} = 12.5 Vdc



UHF BAND DATA

FIGURE 10 — Z_{in} AND Z_{OL} versus COLLECTOR VOLTAGE, INPUT POWER, AND OUTPUT POWER

f Frequency MHz	Z_{in} Ohms		Z_{OL}* Ohms	
	V_{CC} = 7.5 V	V_{CC} = 12.5 V	V_{CC} = 7.5 V	V_{CC} = 12.5 V
	P_{in} = 75 mW	P_{in} = 50 mW	P_{out} 400 MHz = 875 mW P_{out} 450 MHz = 790 mW P_{out} 512 MHz = 675 mW	P_{out} 400 MHz = 1.25 W P_{out} 450 MHz = 1.1 W P_{out} 512 MHz = 775 mW
400	9.6 − j7.5	8.2 − j11.5	37.8 + j12.3	51.8 − j7.2
450	11.3 − j7.5	9.7 − j11	35.8 + j8.6	52.2 − j16.7
512	11.5 − j6.8	12 − j9.2	42.4 + j0.24	43.7 − j5.7

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

FIGURE 11 — OUTPUT POWER versus INPUT POWER
f = 512 MHz

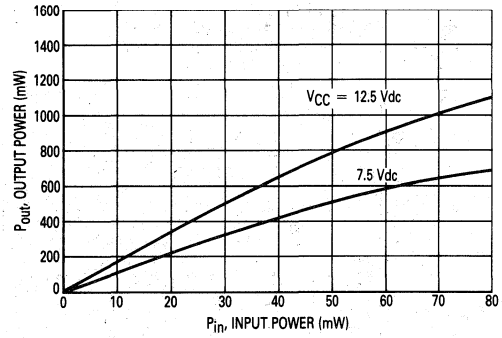


FIGURE 12 — OUTPUT POWER versus FREQUENCY
V_{CC} = 7.5 Vdc

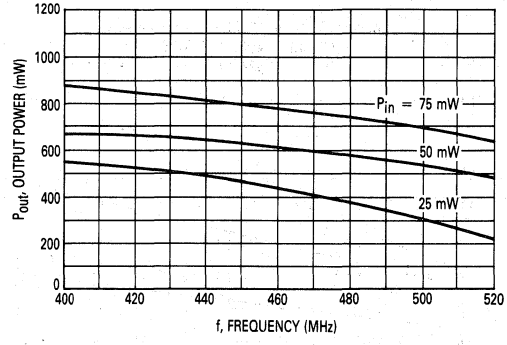


FIGURE 13 — OUTPUT POWER versus COLLECTOR VOLTAGE
f = 512 MHz

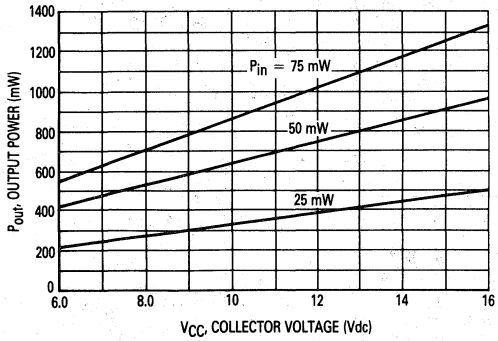
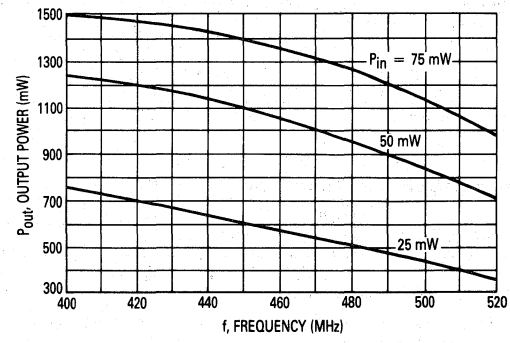


FIGURE 14 — OUTPUT POWER versus FREQUENCY
V_{CC} = 12.5 Vdc



MRF838
MRF838A

The RF Line

1 W—870 MHz

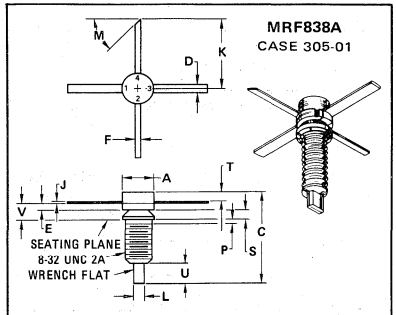
RF POWER
TRANSISTOR

NPN SILICON

NPN SILICON RF POWER TRANSISTOR

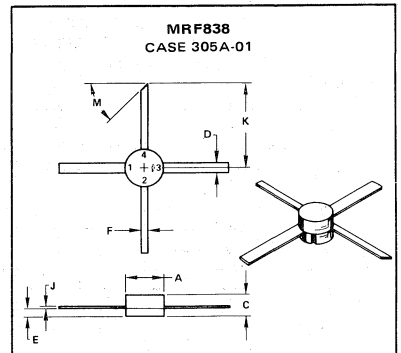
. . . designed for 12.5 volt UHF large-signal, common-emitter amplifier applications in industrial and commercial FM equipment operating in the range of 806–960 MHz.

- Specified 12.5 Volt, 870 MHz Characteristics:
  - Output Power = 1.0 Watt
  - Minimum Gain = 6.5 dB
  - Efficiency = 60% Typ
- Series Equivalent Large-Signal Characterization



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.08	5.59	0.200	0.220
C	13.97	16.26	0.550	0.640
D	1.40	1.65	0.055	0.065
E	1.02	1.27	0.040	0.050
F	0.64	0.89	0.025	0.035
J	0.08	0.18	0.003	0.007
K	11.05	–	0.435	–
L	1.40	1.65	0.055	0.065
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
S	1.40	1.65	0.055	0.065
T	1.40	1.78	0.055	0.070
U	2.79	3.81	0.110	0.150
V	2.41	2.92	0.095	0.115

STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.08	5.59	0.200	0.220
C	2.41	3.30	0.095	0.130
D	1.40	1.65	0.055	0.065
E	1.02	1.27	0.040	0.050
F	0.64	0.89	0.025	0.035
J	0.08	0.18	0.003	0.007
K	11.05	–	0.435	–
M	45° NOM		45° NOM	

STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	0.3	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate Above 25°C	P_D	2.5 0.014	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	70	°C/W

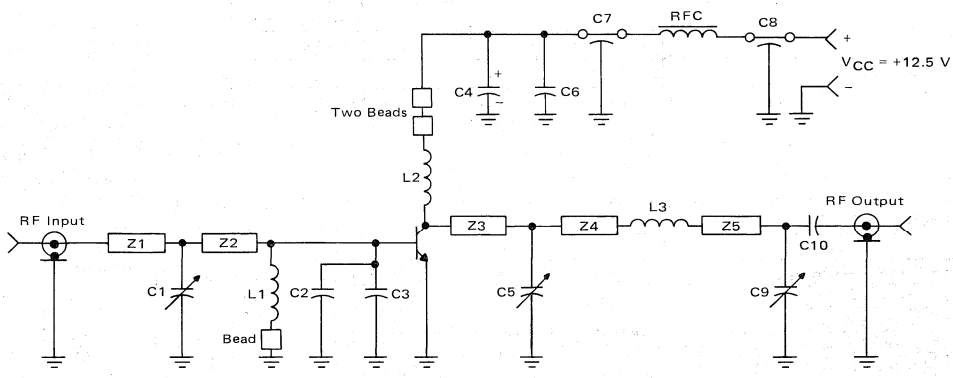
(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	–	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	80	150	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	5.0	7.0	pF
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (P_{out} = 1.0 W, V_{CC} = 12.5 Vdc, f = 870 MHz)	G_{PE}	6.5	7.5	–	dB
Collector Efficiency (P_{out} = 1.0 W, V_{CC} = 12.5 Vdc, f = 870 MHz)	η	50	60	–	%

FIGURE 1 – 870 MHz TEST CIRCUIT



C1, C5, C9 – 0.8-8.0 pF Johanson Gigatrim #7291
C2, C3 – 10 pF ATC Chip Capacitor (Case A)
C4 – 1.0 μF 30 V Tantalum Capacitor
C6 – 0.1 μF Erie Redcap 100 V
C7, C8 – 680 pF Feedthru
C10 – 100 pF Chip Capacitor (100 mil)

L1, L2 – 1 Turn #18 AWG 1/8" Diameter
L3 – #14 AWG 1/2 Turn 0.250" Diameter

RFC – Ferroxcube VK200 20/4B

Bead – Ferroxcube #56-590-65/3B

Z1, Z2 – 1.2" X 0.155" Microstrip
Z3 – 1.05" X 0.155" Microstrip
Z4 – 0.5" X 0.155" Microstrip
Z5 – 1.5" X 0.155" Microstrip

Board Material – 0.0625" Thick Glass-Teflon, ϵ_r = 2.5

FIGURE 2 – OUTPUT POWER versus INPUT POWER

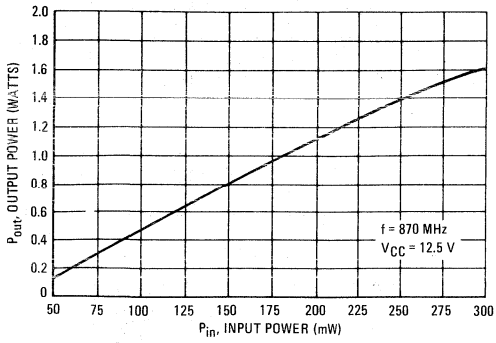


FIGURE 3 – OUTPUT POWER versus FREQUENCY

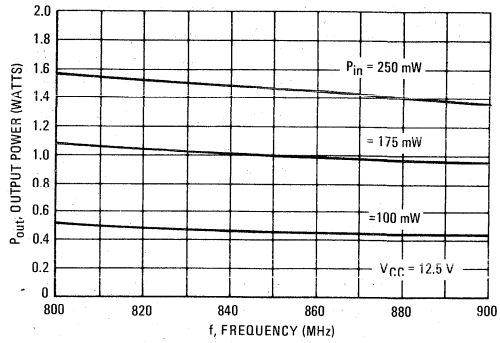


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

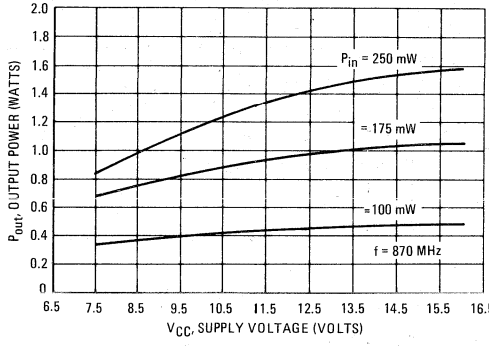
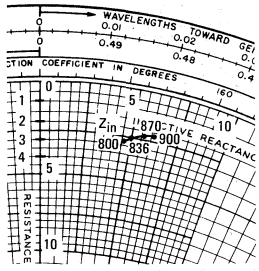


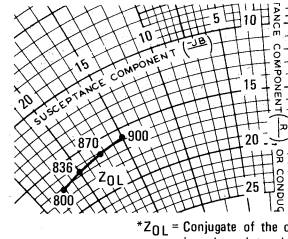
FIGURE 5 – SERIES EQUIVALENT INPUT IMPEDANCE



P_{out} = 1.0 W, V_{CC} = 12.5 Vdc

f MHz	Z_{in} Ohms
800	2.8 + j4.6
836	2.6 + j5.0
870	2.4 + j5.6
900	2.3 + j6.2

FIGURE 6 – SERIES EQUIVALENT OUTPUT IMPEDANCE

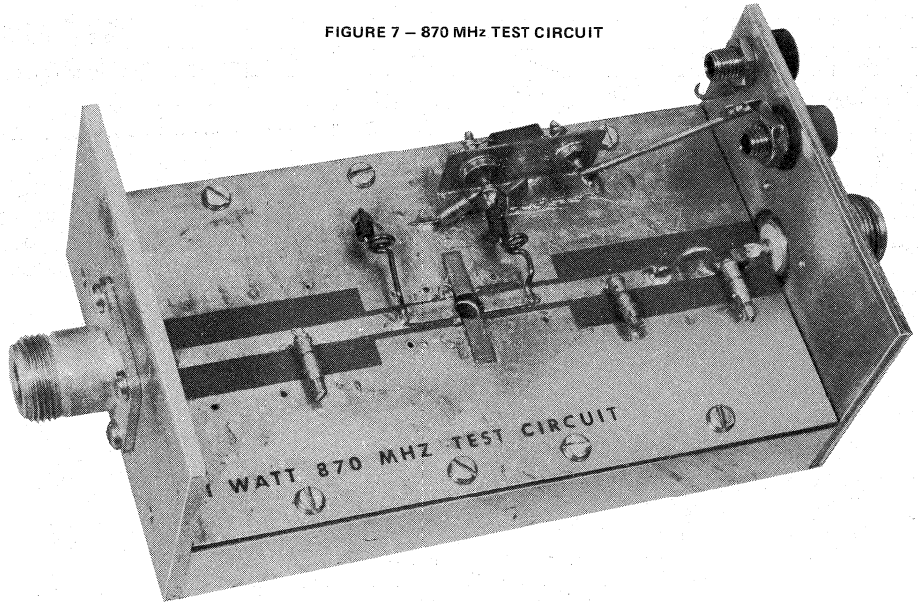


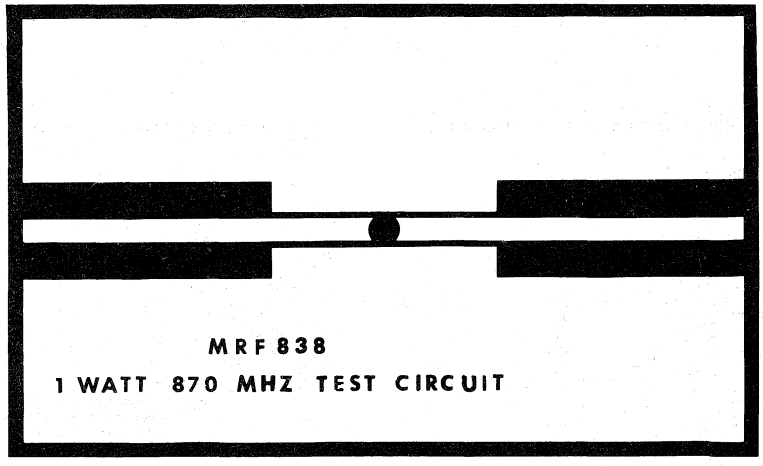
P_{out} = 1.0 W, V_{CC} = 12.5 Vdc

f MHz	Z_{OL}* Ohms
800	17.1 - j22.2
836	16.6 - j20.0
870	16.1 - j17.4
900	15.9 - j15.0

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given power, voltage, and frequency.

FIGURE 7 – 870 MHz TEST CIRCUIT





NOTE: The Printed Circuit Board shown is 75% of the original.

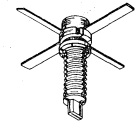
MRF839
MRF839F

3 W 806–960 MHz
RF POWER
TRANSISTORS
COMMON-EMITTER
NPN SILICON

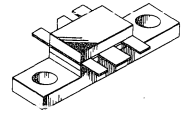
The RF Line
NPN Silicon
RF Power Transistors

. . . designed for 12.5 Volt UHF large-signal, **common-emitter** amplifier applications in industrial and commercial FM equipment operating in the range of 806–960 MHz.

- Specified 12.5 V 870 MHz Characteristics
  - Output Power = 3 Watts
  - Minimum Gain = 8 dB
  - Minimum Efficiency = 55%
- 100% Tested for Load Mismatch at Rated Input Power and 15.5 V
- Series Equivalent Large-Signal Characterization



CASE 305-01
MRF839



CASE 319-04
MRF839F

MAXIMUM RATINGS

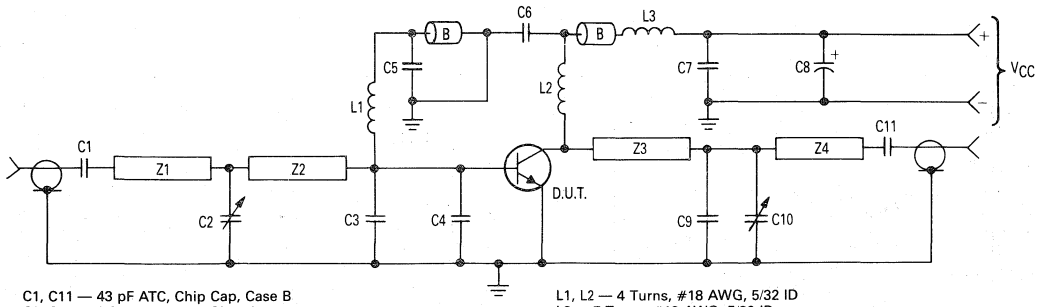
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4	Vdc
Collector-Current — Continuous	I_C	0.6	Adc
Operating Junction Temperature	T_J	200	°C
Total Device Dissipation @ T_C = 110°C Derate above 110°C	P_D	10 111	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	9	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 5 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	4	—	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	1	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5 Vdc)	h_{FE}	10	90	150	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1 MHz)	C_{ob}	—	6.5	10	pF
FUNCTIONAL TESTS (FIGURE 1)					
Common-Emitter Amplifier Power Gain (P_{out} = 3 W, V_{CC} = 12.5 Vdc, f = 870 MHz)	G_{PE}	8	10	—	dB
Collector Efficiency (P_{out} = 3 W, V_{CC} = 12.5 Vdc, f = 870 MHz)	η_c	55	63	—	%
Load Mismatch Stress (V_{CC} = 15.5 Vdc, P_{in} = 0.5 W, f = 870 MHz, VSWR = 20:1, all phase angles)	—	No Degradation in Output Power			



C1, C11 — 43 pF ATC, Chip Cap, Case B
C2, C10 — 0.8–8 Johanson Gigatrim
C3, C4 — 10 pF Clamped Mica, Mini-Underwood
C5, C6, C7 — 68 pF Clamped Mica, Mini-Underwood
C8 — 10 μF, 25 V Tantalum
C9 — 5 pF Clamped Mica, Mini-Underwood
B — Bead, Ferroxcube #56-590-65/3B

L1, L2 — 4 Turns, #18 AWG, 5/32 ID
L3 — 7 Turns, #18 AWG, 5/32 ID
Z1 — 0.850″ x 0.077″ Microstrip, Z_O = 50 Ω
Z2 — 1.100″ x 0.077″ Microstrip, Z_O = 50 Ω
Z3 — 0.920″ x 0.077″ Microstrip, Z_O = 50 Ω
Z4 — 1.150″ x 0.077″ Microstrip, Z_O = 50 Ω
Board Material — 0.032″ Glass Teflon, 2 oz. Copper Clad, ϵ_r = 2.55

Figure 1. MRF839 800–880 MHz Broadband Test Circuit

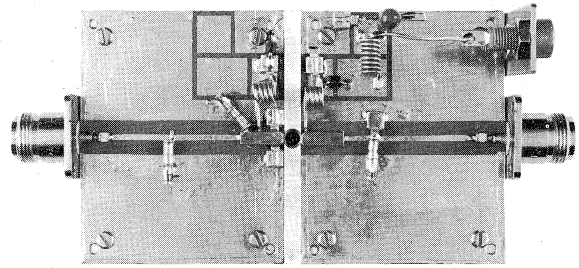


Figure 2. MRF839 Broadband Test Circuit

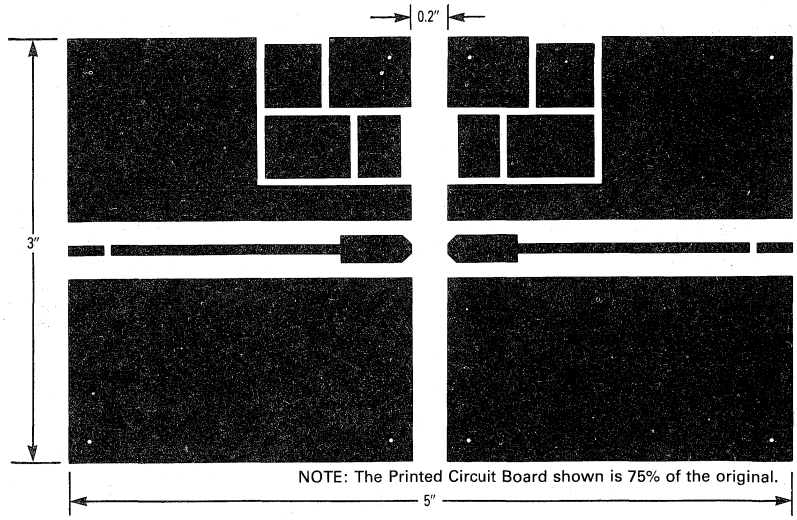


Figure 3. MRF839 Photomaster

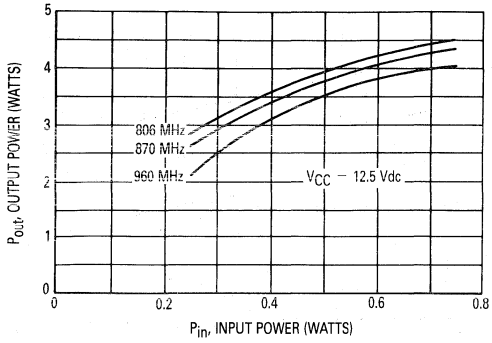


Figure 4. Output Power versus Input Power

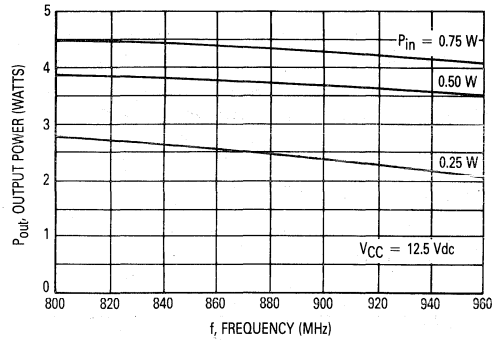


Figure 5. Output Power versus Frequency

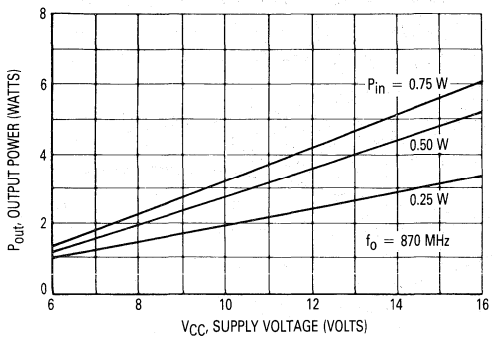


Figure 6. Output Power versus Supply Voltage

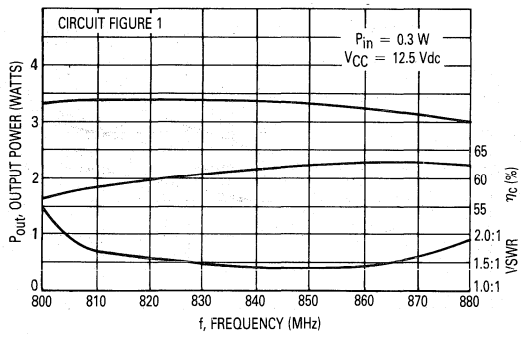
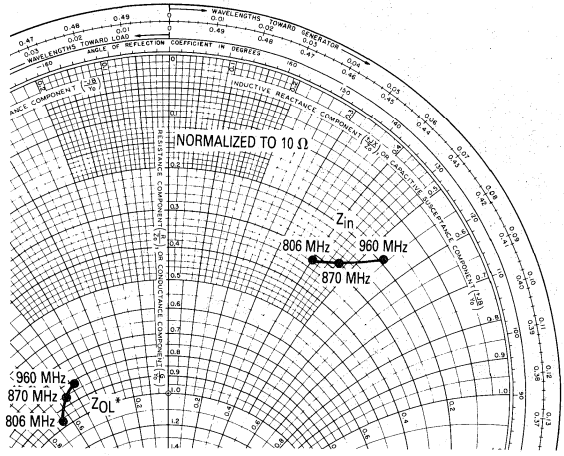


Figure 7. Broadband Performance



P_{out} = 3 Watts, V_{CC} = 12.5 Vdc

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
806	3.1 + j4.0	9.6 − j6.5
870	2.8 + j4.6	8.5 − j5.6
960	1.9 + j5.4	8.1 − j4.8

*Z_{OL} = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

Figure 8. Series Equivalent Input/Output Impedances

MRF839F

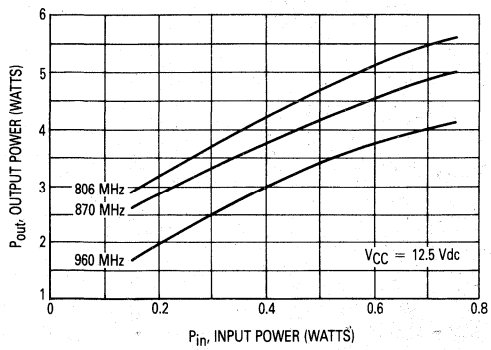


Figure 9. Output Power versus Input Power

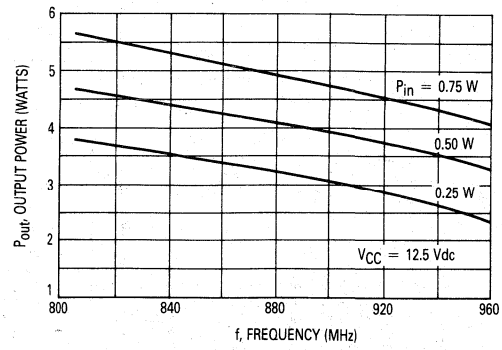


Figure 10. Output Power versus Frequency

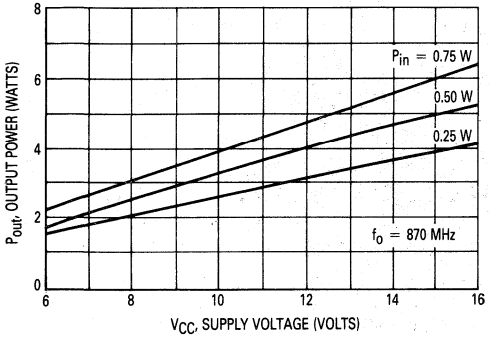


Figure 11. Output Power versus Supply Voltage

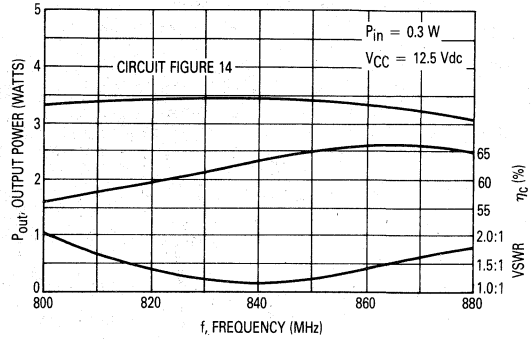
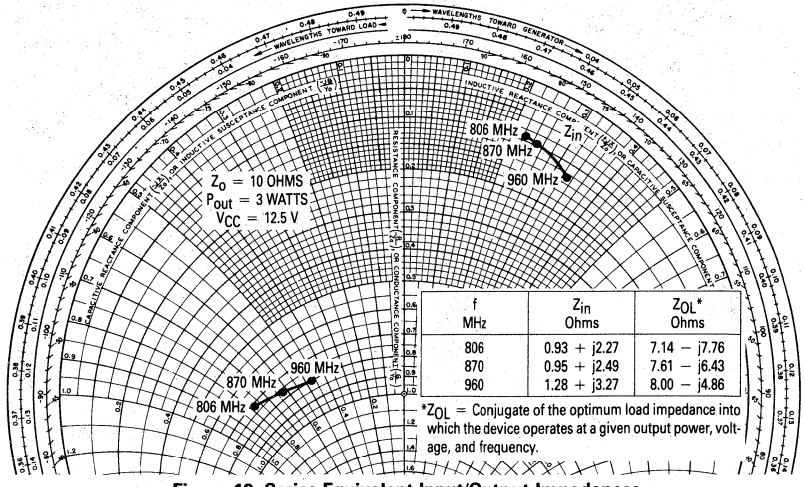


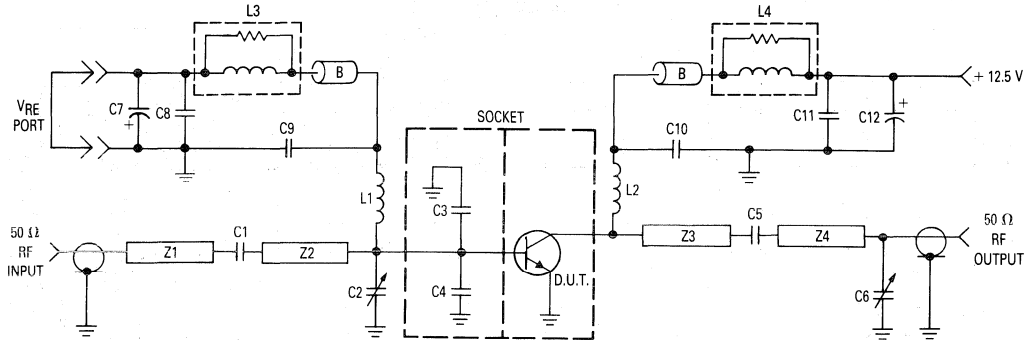
Figure 12. Broadband Performance



f MHz	Z_{in} Ohms	Z_{OL}* Ohms
806	0.93 + j2.27	7.14 − j7.76
870	0.95 + j2.49	7.61 − j6.43
960	1.28 + j3.27	8.00 − j4.86

*Z_{OL} = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

Figure 13. Series Equivalent Input/Output Impedances



C1 — 47 pF Chip Cap (Murata Erie MA20470B)
C3, C4 — 13 pF Mini-Underwood
C5 — 51 pF Chip Cap (ATC 100B510JC500)
C2, C6 — 0.8–8 pF Johanson #7291
C7, C12 — 10 μF, 35 V Electrolytic Capacitor
C8, C11 — 1000 pF Unelco, J101
C9, C10 — 91 pF Mini-Underwood
B — Bead, Ferroxcube #56-590-65/3B

L1, L2 — 4 Turns, #18 Enameled, 5/32″ ID
L3, L4 — 12 Turns, #22 Enameled over 10 Ohm, 1/2 W Carbon Resistor
Z1, Z4 — 50 Ohm Stripline
Z2 — 32 Ohm Stripline (1/4 λ @ 838 MHz)
Z3 — 16 Ohm Stripline (1/4 λ @ 838 MHz)
Board Material — 0.032″ Glass Teflon, 2 oz. Copper Clad, ϵ_r = 2.55

Figure 14. MRF839F 800–880 MHz Broadband Test Circuit

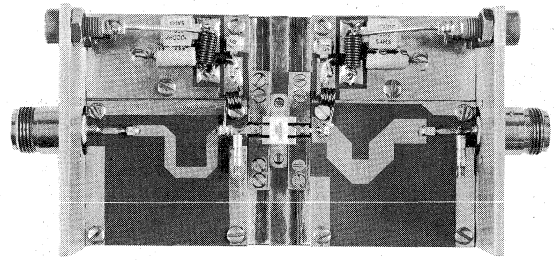
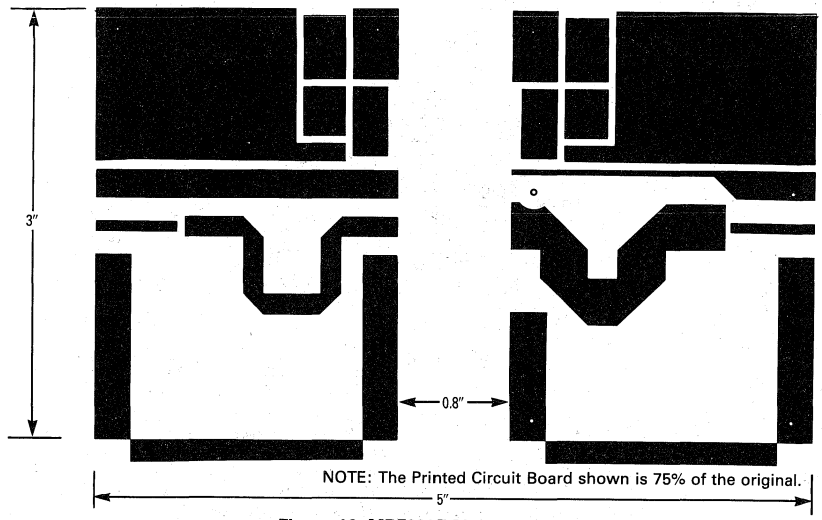


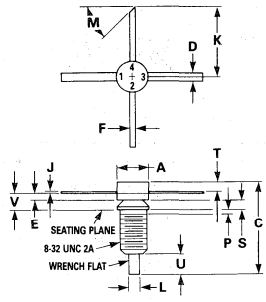
Figure 15. MRF839F Broadband Test Circuit



NOTE: The Printed Circuit Board shown is 75% of the original.

Figure 16. MRF839F Photomaster

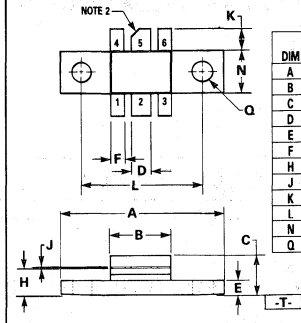
OUTLINE DIMENSIONS



STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.08	5.59	0.200	0.220
C	13.97	16.26	0.550	0.640
D	1.40	1.65	0.055	0.065
E	1.02	1.27	0.040	0.050
F	0.64	0.89	0.025	0.035
J	0.08	0.18	0.003	0.007
K	11.05	—	0.435	—
L	1.40	1.65	0.055	0.065
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
S	1.40	1.65	0.055	0.065
T	1.40	1.78	0.055	0.070
U	2.79	3.81	0.110	0.150
V	2.41	2.92	0.095	0.115

CASE 305-01



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.51	25.02	0.965	0.985
B	9.02	9.52	0.355	0.375
C	5.84	6.60	0.230	0.260
D	2.92	3.18	0.115	0.125
E	2.69	2.95	0.106	0.116
F	1.91	2.16	0.075	0.085
H	4.06	4.31	0.160	0.170
J	0.10	0.15	0.004	0.006
K	2.29	2.79	0.090	0.110
L	18.42 BSC		0.725 BSC	
N	5.72	6.12	0.225	0.241
Q	3.18	3.43	0.125	0.135

NOTES:
1. POSITIONAL TOLERANCE FOR Q HOLES:
   ⌖ | ϕ 0.15 (0.006) Ⓜ | T | A Ⓜ | N Ⓜ
2. IDENTIFICATION NOTCH 1.0mm (0.04) MIN X 45°.
3. DIM D APPLIES 2 PLACES,
   DIM K APPLIES 2 PLACES,
   DIM Q APPLIES 2 PLACES,
   DIM F APPLIES 4 PLACES.
4. DIMENSIONS A AND N ARE DATUMS AND
   -T- IS DATUM SURFACE.
5. DIMENSION B APPLIES TO LEAD FRAME AND Beo.
6. POSITIONAL TOLERANCE FOR D TERMINAL AND DIMENSION B:
   ⌖ | 0.38 (0.15) Ⓜ | T | A Ⓜ | N Ⓜ

STYLE 2:
PIN 1. EMITTER (COMMON)
2. BASE (INPUT)
3. EMITTER (COMMON)
4. EMITTER (COMMON)
5. COLLECTOR (OUTPUT)
6. EMITTER (COMMON)

CASE 319-04

MRF840

The RF Line

10 W – 870 MHz

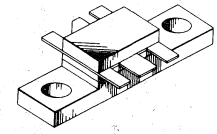
RF POWER
TRANSISTOR

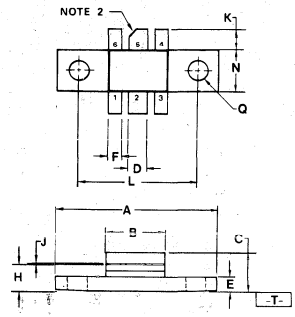
NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed for 12.5 volt UHF large-signal, common-base amplifier applications in industrial and commercial FM equipment operating in the range of 806–960 MHz.

- Specified 12.5 Volt, 870 MHz Characteristics
  Output Power = 10 Watts
  Minimum Gain = 6.0 dB
  Efficiency = 50%
- Series Equivalent Large-Signal Characterization
- Internally Matched Input for Broadband Operation
- Tested for Load Mismatch Stress at All Phase Angles with 20:1 VSWR @ 15.5 Volt Supply and 50% RF Overdrive
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Silicon Nitride Passivated





STYLE 1:
PIN 1. BASE (COMMON)
2. EMITTER (INPUT)
3. BASE (COMMON)
4. BASE (COMMON)
5. COLLECTOR (OUTPUT)
6. BASE (COMMON)

NOTES:
1. POSITIONAL TOLERANCE FOR D HOLES: ⌖ ⌀ 0.15 (0.006) Ⓜ T A Ⓜ N Ⓜ
2. IDENTIFICATION NOTCH 1.0mm (0.04) MIN X 45°.
3. DIM D APPLIES 2 PLACES.
DIM K APPLIES 2 PLACES.
DIM Q APPLIES 2 PLACES.
DIM F APPLIES 4 PLACES.
4. DIMENSIONS A AND N ARE DATUMS AND -T- IS A DATUM SURFACE.
5. DIMENSION B APPLIES TO LEAD FRAME AND Bee.
6. POSITIONAL TOLERANCE FOR D TERMINAL AND DIMENSION B: ⌖ 0.38 (0.15) Ⓜ T A Ⓜ N Ⓜ

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.51	25.02	0.965	0.985
B	9.02	9.52	0.355	0.375
C	5.84	6.60	0.230	0.260
D	2.92	3.18	0.115	0.125
E	2.69	2.95	0.106	0.116
F	1.91	2.16	0.075	0.085
H	4.06	4.31	0.160	0.170
J	0.10	0.15	0.004	0.006
K	2.29	2.79	0.090	0.110
L	18.42 BSC		0.725 BSC	
N	5.72	6.12	0.225	0.241
Q	3.18	3.43	0.125	0.135

CASE 319-04

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	3.8	Adc
Total Device Dissipation @ $T_C = 25^oC$ (1) Derate Above 25^oC	P_D	40 0.32	Watts $W/^oC$
Storage Temperature Range	T_{stg}	−65 to +150	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	3.1	$^oC/W$

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

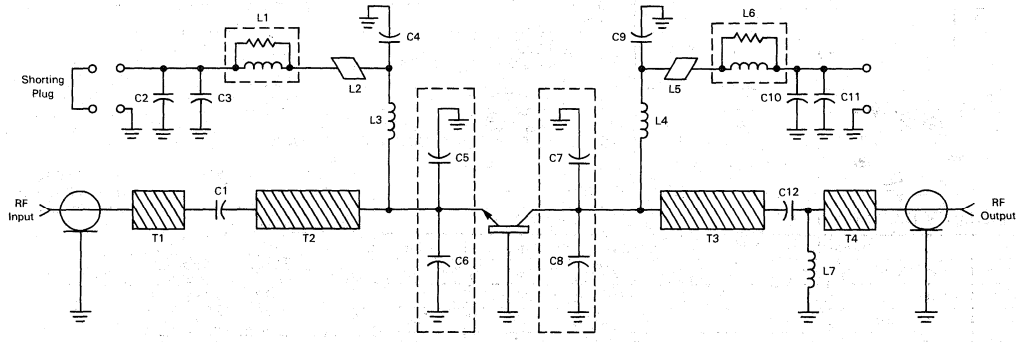
(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	–	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	24	35	pF
FUNCTIONAL TEST					
Common-Base Amplifier Power Gain (P_{out} = 10 W, V_{CC} = 12.5 Vdc, f = 870 MHz)	G_{PB}	6.0	7.0	–	dB
Collector Efficiency (P_{out} = 10 W, V_{CC} = 12.5 Vdc, f = 870 MHz)	η	50	55	–	%
Load Mismatch Stress (V_{CC} = 15.5 Vdc, P_{in} = 3.0 W,* f = 870 MHz, VSWR = 20:1, all phase angles)	–	No Degradation in Output Power			

*P_{in} = 150% of the typical input power requirement for 10 W output power @ 12.5 Vdc.

FIGURE 1 – 870 MHz TEST CIRCUIT



C1, C12 — 50 pF, 100 Mil Chip Capacitor
C2, C11 — 15 μF, 20 V Tantalum
C3, C10 — 1000 pF, 350 V UNELCO
C4, C9 — 91 pF Mini-Underwood
C5 — 15 pF
C6 — 15 pF
C7 — 15 pF
C8 — 15 pF

L1, L6 — 11 Turns 20 AWG Around 10 Ω 1/2 W Resistor
L2, L5 — Ferrite Bead
L3, L4 — 4 Turn 20 AWG 0.2" I.D.
T1, T4 — Z_O = 50 Ω
T2 — Z_O = 30 Ω ℓ = λ/4 @ 838 MHz
T3 — Z_O = 13.5 Ω ℓ = λ/4 @ 838 MHz
L7 — 18 AWG Wire Loop

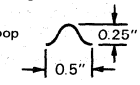


FIGURE 2 – OUTPUT POWER versus INPUT POWER

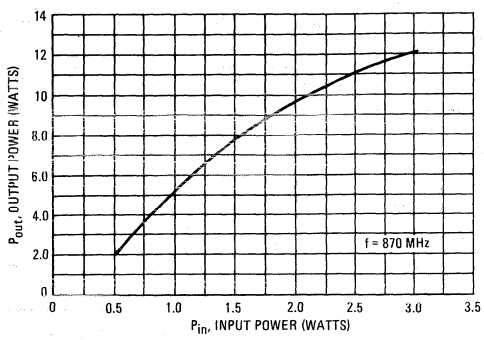


FIGURE 3 – OUTPUT POWER versus FREQUENCY

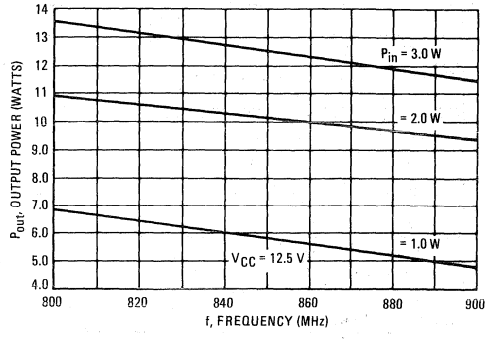


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

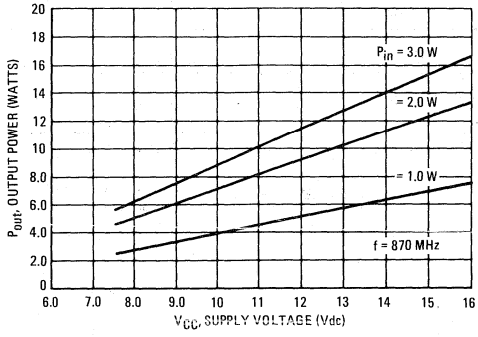
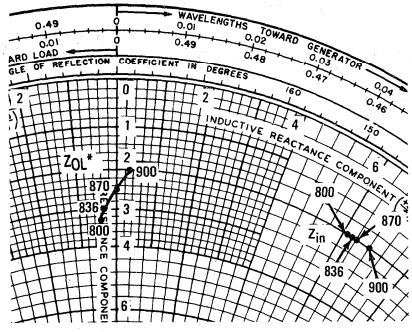


FIGURE 5 – SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCE

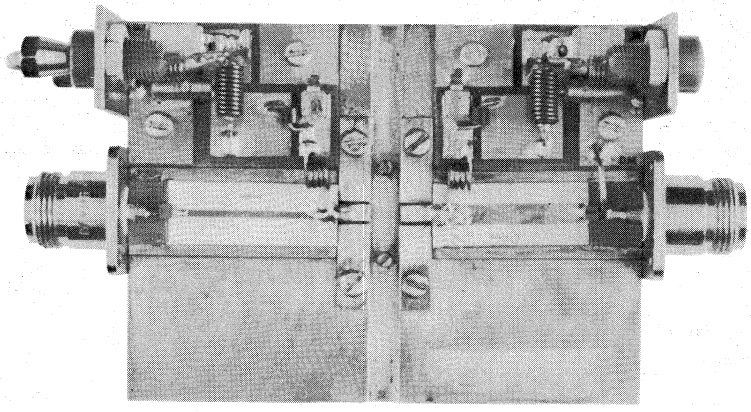


P_{out} = 10 W, V_{CC} = 12.5 Vdc

f MHz	Z_{in} Ohms	Z_{DL}* Ohms
800	2.0 + j6.1	3.3 – j0.4
836	2.0 + j6.2	3.0 – j0.3
870	2.0 + j6.4	2.5 + j0.0
900	2.0 + j6.8	2.0 + j0.3

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

FIGURE 6 – 870 MHz TEST CIRCUIT



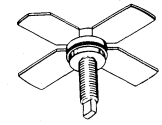
MRF841
MRF841F

5 W 870 MHz
RF POWER
TRANSISTORS
NPN SILICON

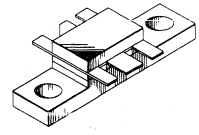
The RF Line
NPN Silicon
RF Power Transistors

. . . designed primarily for wideband large-signal output and driver stages in the 806–960 MHz frequency range.

- Specified 12.5 Volt, 870 MHz Characteristics @ P_{out} = 5 W
  Common Base Gain = 10 dB (Typ)
  Efficiency = 65% (Typ)
- Internally Matched Input for Broadband Operation
- Gold Metallized and Emitter Ballasted for Improved Reliability
- 100% Tested for Load Mismatch at Rated Input Power and 15.5 V



MRF841
CASE 244-04



MRF841F
CASE 319-04

MAXIMUM RATINGS

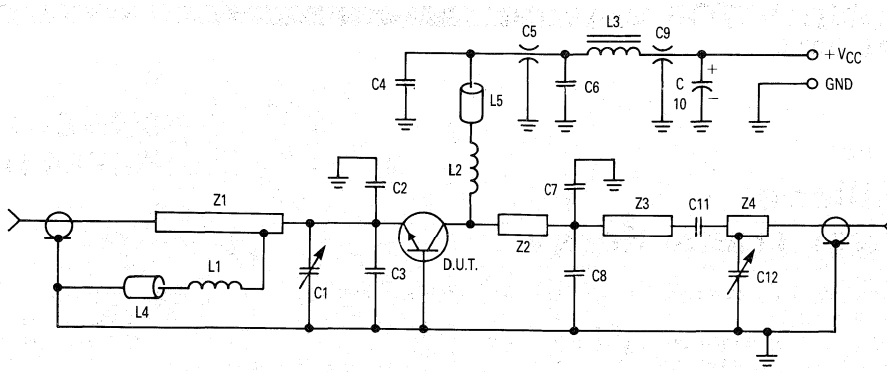
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4	Vdc
Collector Current — Continuous	I_C	2	Adc
Total Device Dissipation @ T_C = 25°C Derate Above 25°C	P_D	25 143	Watts mW/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	7	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 25 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 25 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 5 mAdc, I_C = 0)	$V_{(BR)EBO}$	4	—	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0)	I_{CES}	—	—	1	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 200 mAdc, V_{CE} = 5 Vdc)	h_{FE}	10	—	150	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1 MHz)	C_{ob}	6	9.5	15	pF
FUNCTIONAL TESTS (f = 870 MHz)					
Common-Base Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 5 W)	G_{PB}	8.5	10	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 5 W)	η_c	—	65	—	%
Load Mismatch (V_{CC} = 15.5 Vdc, P_{in} = 710 mW, VSWR = 20:1, all Phase Angles)	ψ	No Degradation in Output Power			



C1, C12 — 0.8–8 pF Johanson 7290 Variable
C2 — 5 pF Mini-Underwood Mica
C3 — 8.2 pF Mini-Underwood Mica
C4 — 91 pF Mini-Underwood Mica
C5, C9 — 680 pF Feedthru
C6 — 0.1 μF Ceramic
C7, C8 — 10 pF Mini-Underwood Mica
C10 — 1 μF Electrolytic
C11 — 43 pF Mini-Underwood

L1, L2 — 4 Turns, #22 AWG Wire, 0.2-inch ID
L3 — VK200 Ferroxcube
L4, L5 — Ferrite Bead, Ferroxcube #56-590-65-3B
Z1 — 2.36″ x 0.145″ Microstrip 33 Ohm Line
Z2 — 0.5″ x 0.175″ Microstrip 28 Ohm Line
Z3 — 1.40″ x 0.175″ Microstrip 28 Ohm Line
Z4 — 0.40″ x 0.175″ Microstrip 28 Ohm Line
Board = 0.032″ Glass Teflon 2 oz. cu clad ϵ_r = 2.55

MRF841
Figure 1. 800–960 MHz Broadband Power Gain Test Circuit

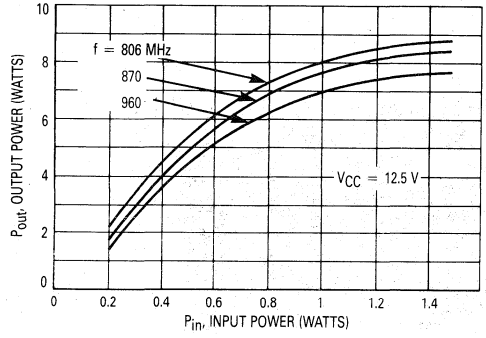


Figure 2. Output Power versus Input Power

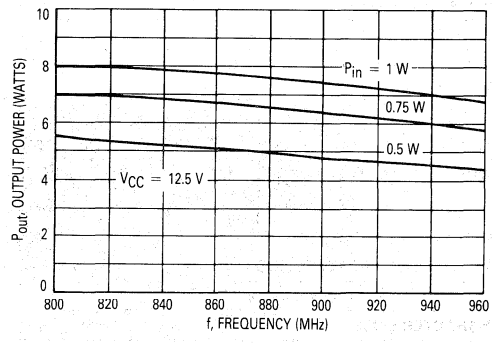


Figure 3. Output Power versus Frequency

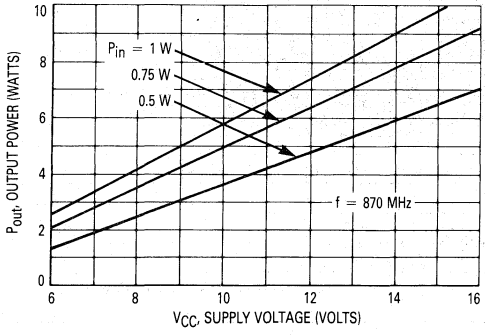


Figure 4. Power Out versus Supply Voltage

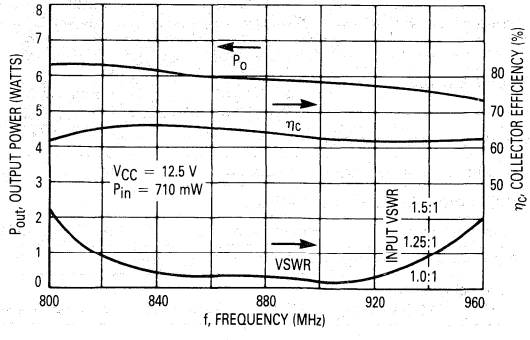


Figure 5. Typical Performance in Broadband Circuit

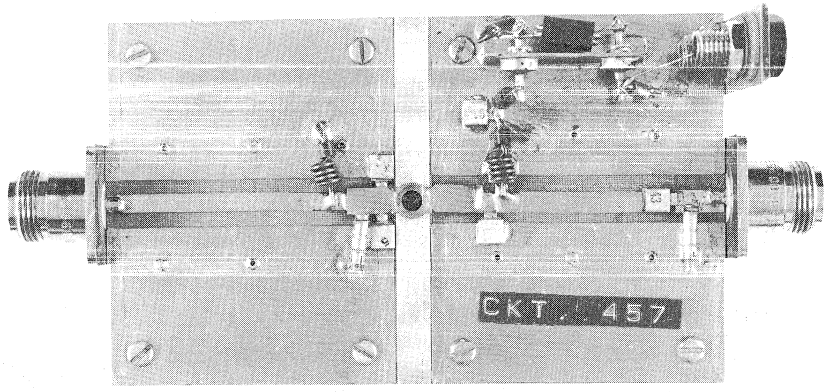


Figure 6. MRF841 Broadband Power Gain Test Circuit

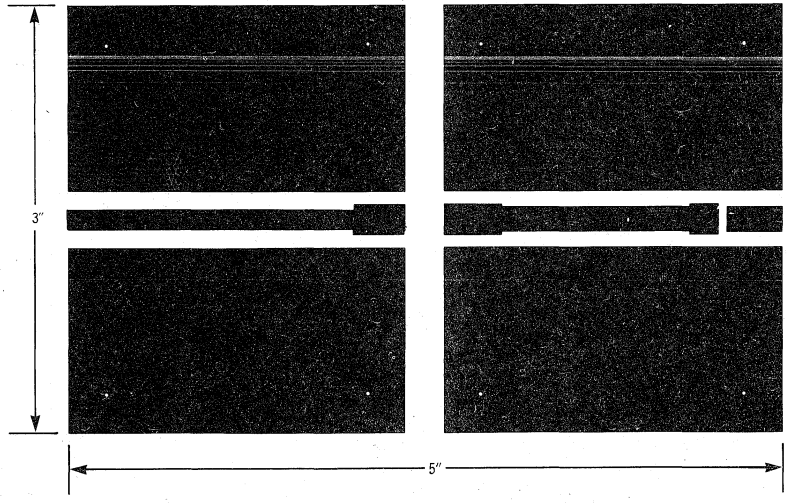


Figure 7. MRF841 Test Circuit Photomaster

NOTE: The Printed Circuit Board shown is 75% of the original.

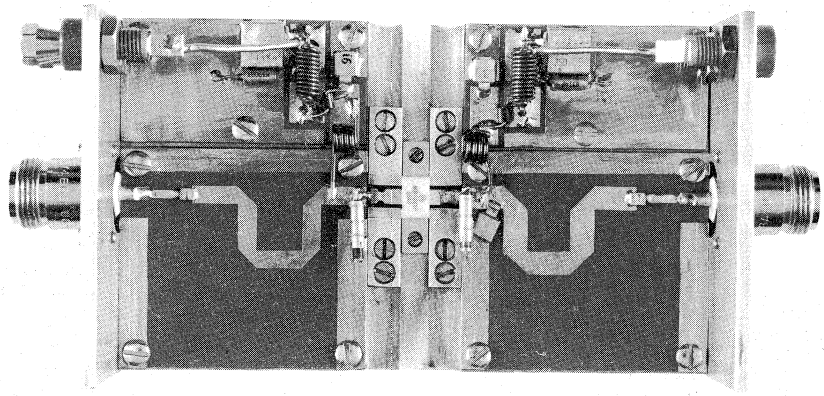


Figure 8. MRF841F Broadband Power Gain Test Circuit

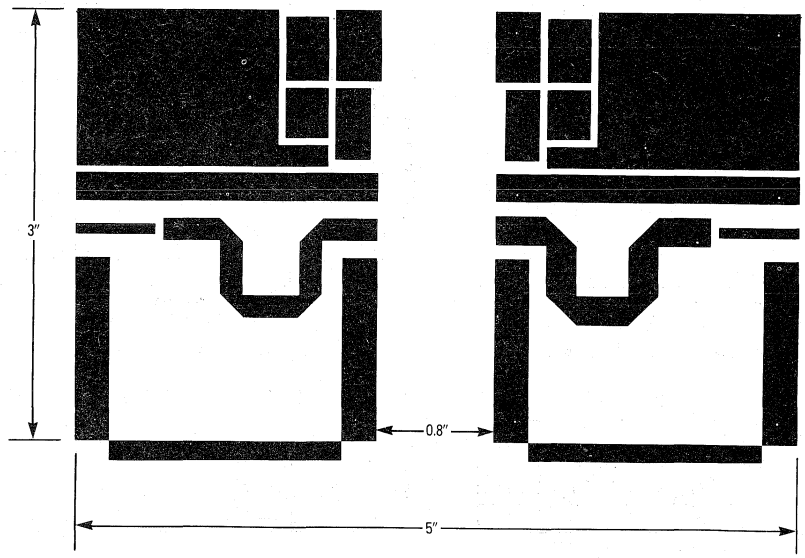
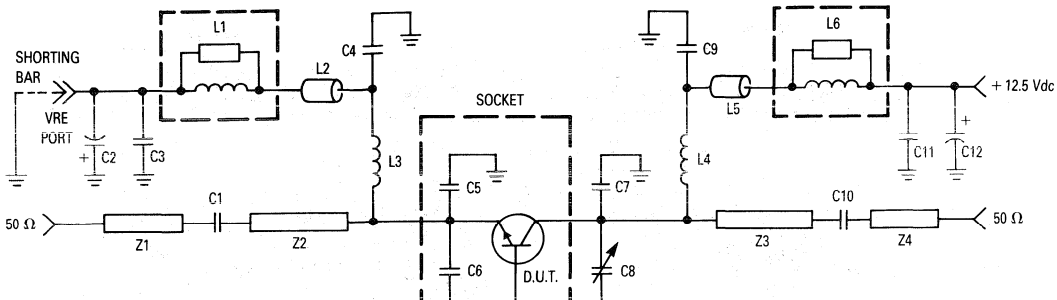


Figure 9. MRF841F Test Circuit Photomaster

NOTE: The Printed Circuit Board shown is 75% of the original.



C1, C10 = 47 pF, 100 Mil ATC
C2, C12 = 1 μF, 35 WV Tantalum
C3, C11 = 1000 pF Underwood J101
C4, C9 = 91 pF Mini Underwood
C5 = 12 pF Mini-Underwood
C6 = 10 pF Mini-Underwood
C7 = 10 pF Mini-Underwood
C8 = Johansen Giga Trim
0.8–8 pF 7290 Variable

L1, L6 = 11 Turns #20 AWG Over 10 Ω 1/2 W
L2, L5 = Ferrite Bead, Ferroxcube #56-590-65-3B
L3, L4 = 4T #18 AWG, 15″ ID
Z1, Z4 = 50 Ω Printed Line
Z2 = 30 Ω Printed Line, λ/4 @ 838 MHz
Z3 = 24 Ω Printed Line, λ/4 @ 838 MHz
Board = 0.032″ Glass Teflon 2 oz. cu clad ϵ_r = 2.55

NOTES: C7 and C8 mounted ≈ 250 mils
down Z3 from collector edge of board

MRF841F

Figure 10. 800–960 MHz Broadband Power Gain Test Circuit

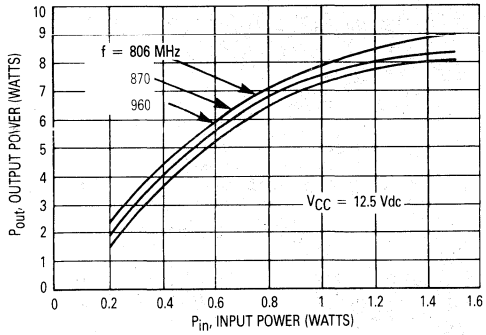


Figure 11. Output Power versus Input Power

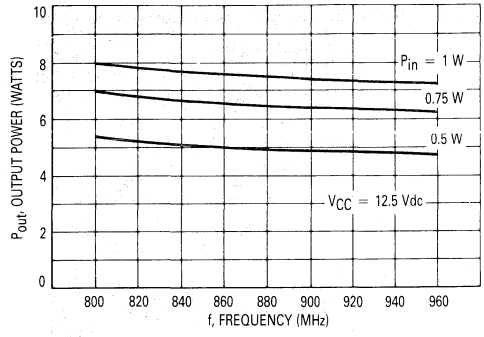


Figure 12. Output Power versus Frequency

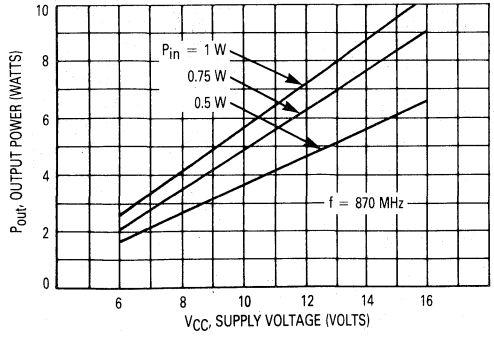


Figure 13. Output Power versus Supply Voltage

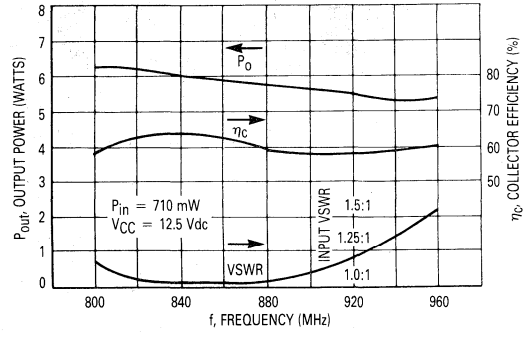
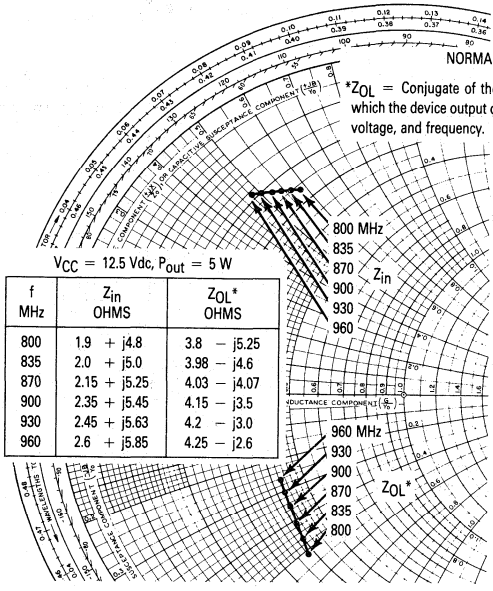


Figure 14. Typical Performance in Broadband Circuit

MRF841



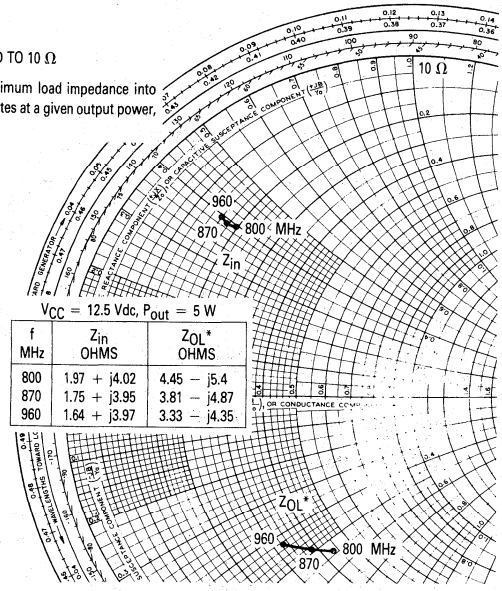
*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

V_{CC} = 12.5 Vdc, P_{out} = 5 W

f MHz	Z_{in} OHMS	Z_{OL}* OHMS
800	1.9 + j4.8	3.8 − j5.25
835	2.0 + j5.0	3.98 − j4.6
870	2.15 + j5.25	4.03 − j4.07
900	2.35 + j5.45	4.15 − j3.5
930	2.45 + j5.63	4.2 − j3.0
960	2.6 + j5.85	4.25 − j2.6

Figure 15. Series Equivalent Input/Output Impedances

MRF841F



V_{CC} = 12.5 Vdc, P_{out} = 5 W

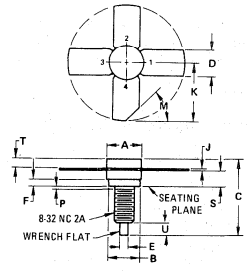
f MHz	Z_{in} OHMS	Z_{OL}* OHMS
800	1.97 + j4.02	4.45 − j5.4
870	1.75 + j3.95	3.81 − j4.87
960	1.64 + j3.97	3.33 − j4.35

Figure 16. Series Equivalent Input/Output Impedances

3

OUTLINE DIMENSIONS

MRF841
CASE 244-04

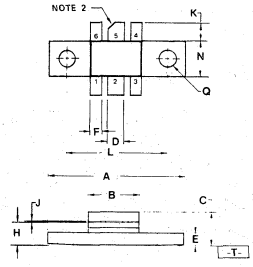


STYLE 4:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	7.06	7.26	0.278	0.286
B	6.20	6.50	0.244	0.256
C	14.99	16.51	0.590	0.650
D	5.46	5.96	0.215	0.235
E	1.40	1.65	0.055	0.065
F	1.52	–	0.060	–
J	0.08	0.17	0.003	0.007
K	11.05	–	0.435	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
S	3.00	3.25	0.118	0.128
T	1.40	1.77	0.055	0.070
U	2.92	3.68	0.115	0.145

MRF841F
CASE 319-04

STYLE 1:
PIN 1. BASE (COMMON)
2. EMITTER (INPUT)
3. BASE (COMMON)
4. BASE (COMMON)
5. COLLECTOR (OUTPUT)
6. BASE (COMMON)



NOTES:
1. POSITIONAL TOLERANCE FOR Q HOLES:
⌖ ⌀ 0.15 (0.006) Ⓜ T A Ⓜ N Ⓜ
2. IDENTIFICATION NOTCH 1.0mm (0.04) MIN X 45°.
3. DIM D APPLIES 2 PLACES.
DIM K APPLIES 2 PLACES.
DIM Q APPLIES 2 PLACES.
DIM F APPLIES 4 PLACES.
4. DIMENSIONS A AND N ARE DATUMS AND -T- IS A DATUM SURFACE.
5. DIMENSION B APPLIES TO LEAD FRAME AND Beo.
6. POSITIONAL TOLERANCE FOR D TERMINAL AND DIMENSION B:
⌖ 0.38 (0.15) Ⓜ T A Ⓜ N Ⓜ

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	24.51	25.02	0.965	0.985
B	9.02	9.52	0.355	0.375
C	5.84	6.60	0.230	0.260
D	2.92	3.18	0.115	0.125
E	2.69	2.95	0.106	0.116
F	1.91	2.16	0.075	0.085
H	4.06	4.31	0.160	0.170
J	0.10	0.15	0.004	0.006
K	2.29	2.79	0.090	0.110
L	18.42 BSC		0.725 BSC	
N	5.72	6.12	0.225	0.241
Q	3.18	3.43	0.125	0.135

MRF842

The RF Line

20 W – 870 MHz

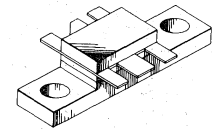
RF POWER
TRANSISTOR

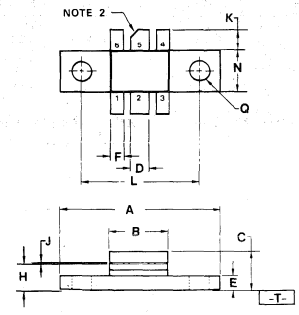
NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed for 12.5 volt UHF large-signal, common-base amplifier applications in industrial and commercial FM equipment operating in the range of 806–960 MHz.

- Specified 12.5 Volt, 870 MHz Characteristics
  Output Power = 20 Watts
  Minimum Gain = 6.0 dB
  Efficiency = 50%
- Series Equivalent Large-Signal Characterization
- Internally Matched Input for Broadband Operation
- 100% Tested for Load Mismatch Stress at All Phase Angles with 20:1 VSWR @ 15.5 Volt Supply and 50% RF Overdrive
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Silicon Nitride Passivated





STYLE 1:
PIN 1. BASE (COMMON)
2. EMITTER (INPUT)
3. BASE (COMMON)
4. BASE (COMMON)
5. COLLECTOR (OUTPUT)
6. BASE (COMMON)

NOTES:
1. POSITIONAL TOLERANCE FOR Q HOLES: ⌖ ⌀ 0.15 (0.006) Ⓜ T A Ⓜ N Ⓜ
2. IDENTIFICATION NOTCH 1.0mm (0.04) MIN X 45°.
3. DIM D APPLIES 2 PLACES.
   DIM K APPLIES 2 PLACES.
   DIM Q APPLIES 2 PLACES.
   DIM F APPLIES 4 PLACES.
4. DIMENSIONS A AND N ARE DATUMS AND -T- IS A DATUM SURFACE.
5. DIMENSION B APPLIES TO LEAD FRAME AND Bee.
6. POSITIONAL TOLERANCE FOR D TERMINAL AND DIMENSION B: ⌖ 0.38 (0.15) Ⓜ T A Ⓜ N Ⓜ

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.51	25.02	0.965	0.985
B	9.02	9.52	0.355	0.375
C	5.84	6.60	0.230	0.260
D	2.92	3.18	0.115	0.125
E	2.69	2.95	0.106	0.116
F	1.91	2.16	0.075	0.085
H	4.06	4.31	0.160	0.170
J	0.10	0.15	0.004	0.006
K	2.29	2.79	0.090	0.110
L	18.42 BSC		0.725 BSC	
N	5.72	6.12	0.225	0.241
Q	3.18	3.43	0.125	0.135

CASE 319-04

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	7.6	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate Above 25°C	P_D	80 0.64	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	1.5	°C/W

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

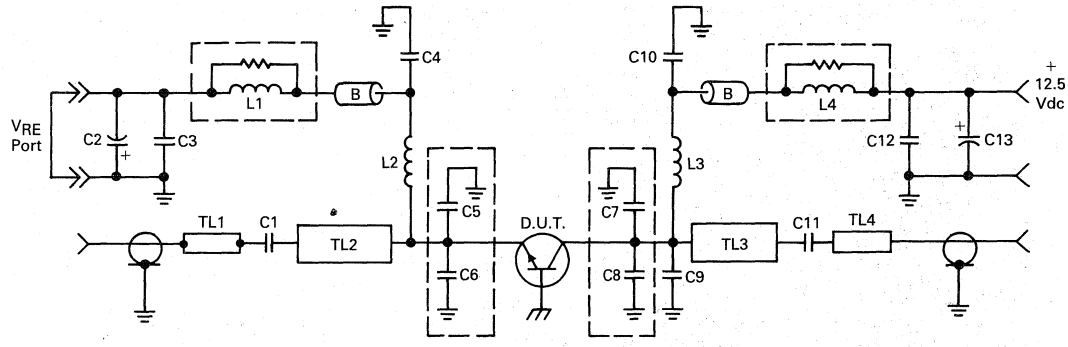
(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36		–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	–	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	45	65	pF
FUNCTIONAL TEST					
Common-Base Amplifier Power Gain (P_{out} = 20 W, V_{CC} = 12.5 Vdc, f = 870 MHz)	G_{PB}	6.0	7.0	–	dB
Collector Efficiency (P_{out} = 20 W, V_{CC} = 12.5 Vdc, f = 870 MHz)	η	50	55	–	%
Load Mismatch Stress (V_{CC} = 15.5 Vdc, P_{in}* = 6.0 W, f = 870 MHz, VSWR = 20:1, all phase angles)	–	No Degradation in Output Power			

*P_{in} = 150% of the typical input power requirement for 20 W output power @ 12.5 Vdc.

FIGURE 1 — 870 MHz TEST CIRCUIT SCHEMATIC



C1, C11 — 51 pF, 100 Mil Chip Capacitor
C2, C13 — 15 μF, 20 WV Tantalum
C3, C12 — 1000 pF Unelco J101
C4, C10 — 91 pF Mini-Underwood
C5 — 15 pF Mini-Underwood
C6 — 12 pF Mini-Underwood
C7, C8 — 21 pF Mini-Underwood
C9 — 11 pF Mini-Underwood

L1, L4 — 11 Turns #20 AWG Over 10 ohm 1/2 W Carbon
L2, L3 — 4 Turns #20 AWG, 200 Mil ID
B — Ferrite Bead, Ferroxcube 56-590-65-3B
TL1, TL4 — Micro Strip, Z_O = 50 Ω
TL2 — Micro Strip, Z_O = 38 Ω, λ/4 @ 838 MHz
TL3 — Micro Strip, Z_O = 24 Ω, λ/4 @ 838 MHz
Board — 0.032" Glass Teflon
2 oz. Cu CLAD, ϵ_r = 2.55

FIGURE 2 – OUTPUT POWER versus INPUT POWER

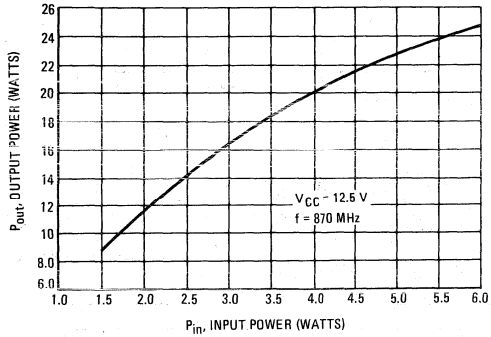


FIGURE 3 – OUTPUT POWER versus FREQUENCY

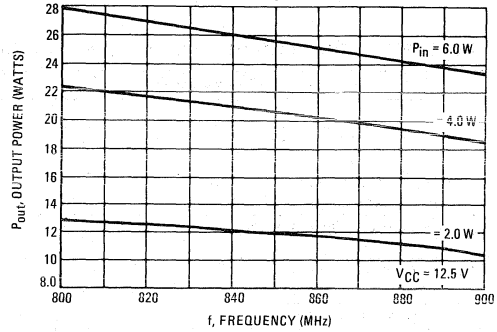


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

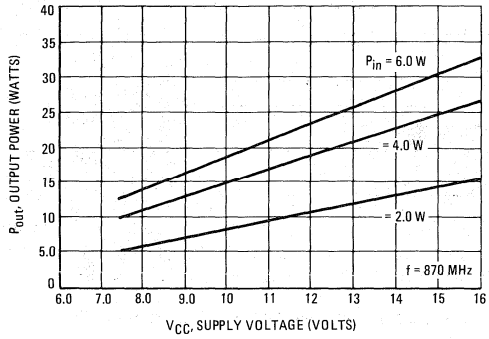
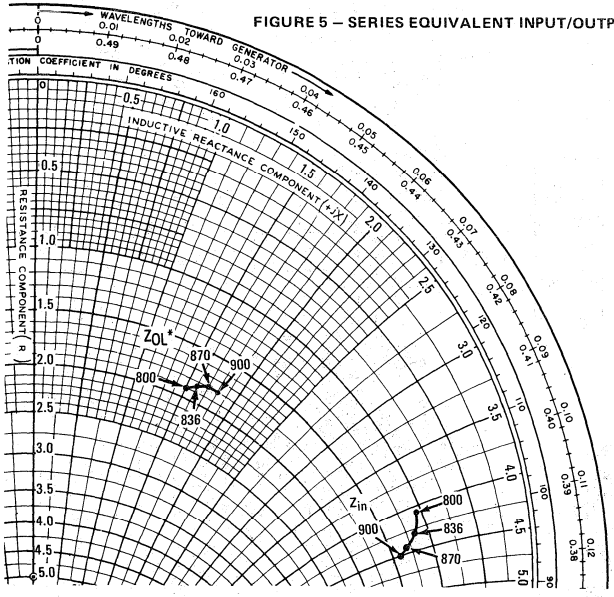


FIGURE 5 – SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCE

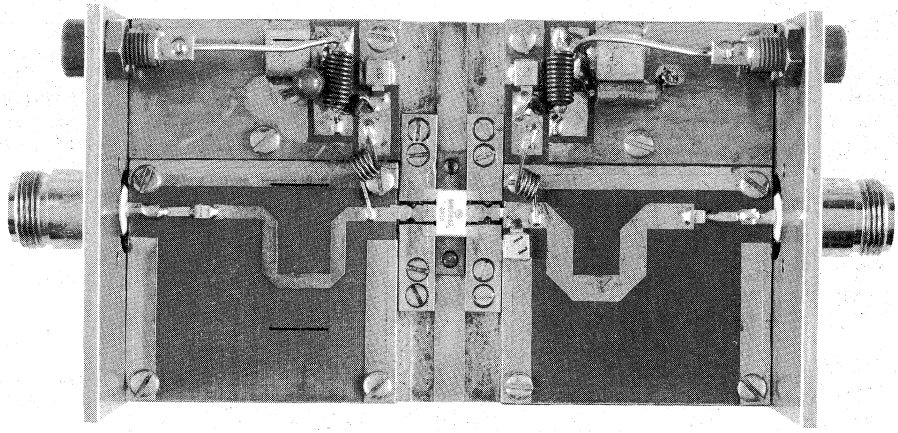


P_{out} = 20 W, V_{CC} = 12.5 Vdc

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
800	1.1 + j4.1	1.9 + j1.5
836	1.2 + j4.3	1.85 + j1.6
870	1.4 + j4.4	1.8 + j1.7
900	1.6 + j4.5	1.8 + j1.8

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

FIGURE 6 – 870 MHz TEST CIRCUIT



MRF843
MRF843F

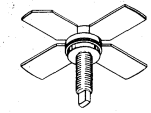
The RF Line

NPN Silicon RF Power Transistors

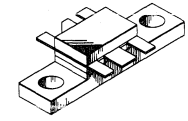
15 W 806–960 MHz
RF POWER
TRANSISTORS
COMMON BASE
NPN SILICON

. . . designed for 12.5 Volt UHF large-signal, **common-base** applications in industrial and commercial FM equipment operating in the range of 806–960 MHz.

- Specified 12.5 Volt, 870 MHz Characteristics
  - Output Power = 15 Watts
  - Minimum Gain = 7 dB
  - Efficiency = 55%
- Internally Matched Input for Broadband Operation
- Gold Metallized and Emitter Ballasted for Long Life
- 100% Tested for Load Mismatch at 2 dB Overdrive and 15.5 V



CASE 244-04
MRF843



CASE 319-04
MRF843F

MAXIMUM RATINGS

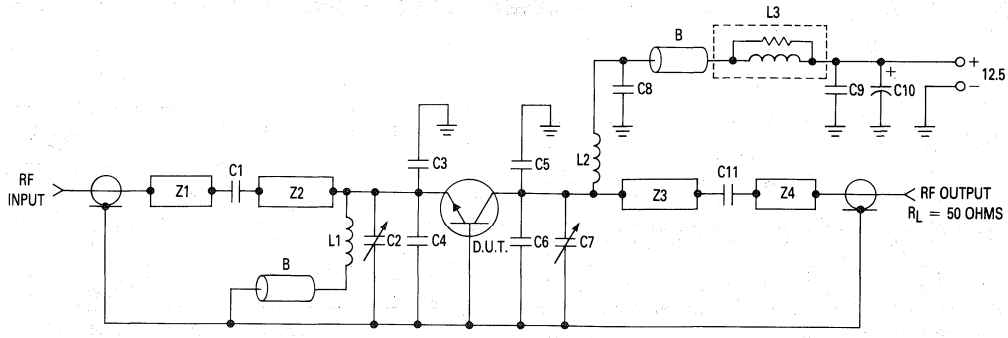
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4	Vdc
Collector-Current — Continuous	I_C	4	Adc
Operating Junction Temperature	T_J	200	°C
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	44 0.25	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 25 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 25 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 5 mAdc, I_C = 0)	$V_{(BR)EBO}$	4	—	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	5	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1 Adc, V_{CE} = 5 Vdc)	h_{FE}	10	—	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1 MHz)	C_{ob}	—	30	45	pF
FUNCTIONAL TESTS					
Common Base Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 15 W, f = 870 MHz)	G_{pb}	7	7.9	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 15 W, f = 870 MHz)	η	55	60	—	%
Load Mismatch Stress (P_{in} = 2 dB Overdrive, V_{CC} = 15.5 V, f = 870 MHz, VSWR = 20:1 @ All Phase Angles)	ψ	No Degradation in Output Power			



C1 — 39 pF ATC 100 Mil Ceramic Chip
C2, C7 — 0.8–8 pF Johanson Gigatrim (7290)
C3, C4 — 8 pF Mini Underwood Mica
C5, C6 — 10 pF Mini Underwood Mica
C8 — 68 pF Mini Underwood Mica
C9 — 1000 pF Unelco
C10 — 10 μF Electrolytic
C11 — 33 pF Mini Underwood Mica
L1 — 4 Turns 0.10″ ID #24 AWG
L2 — 4 Turns 0.20″ ID #24 AWG
L3 — 10 Turns on 10 Ohm ½ W Resistor
Z1 — 0.100″ x 0.525″ Microstrip TX Line
Z2 — 0.100″ x 1.80 36 Ohm Microstrip TX Line
Z3 — 0.200″ x 1.90″ 30 Ohm Microstrip TX Line
Z4 — 0.150″ x 0.450″ Microstrip TX Line
B — Bead, Ferroxcube #56-590-65/3B
Board Material — 0.032″ Glass Teflon 2 oz. Copper Clad ϵ_r = 2.55

Figure 1. MRF843 800–900 MHz Broadband Test Fixture

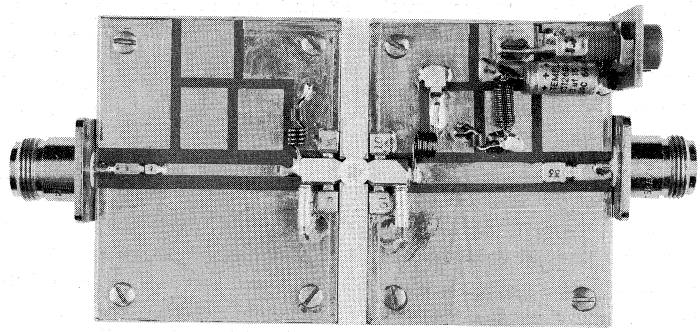


Figure 2. MRF843 800–900 MHz Test Circuit

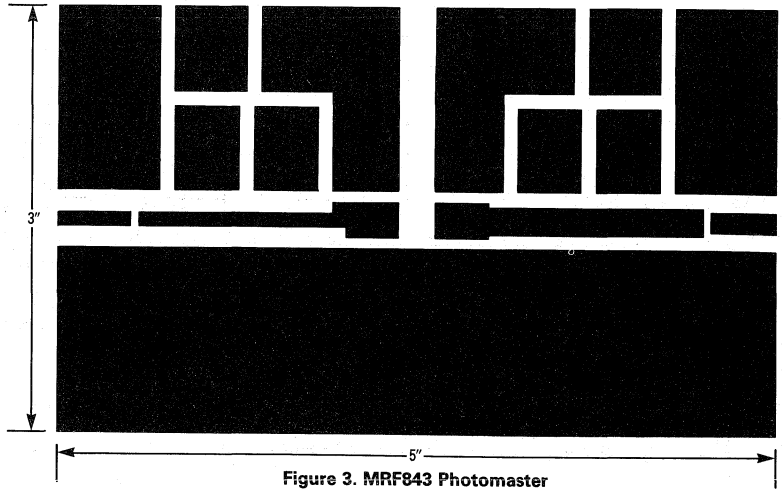


Figure 3. MRF843 Photomaster

NOTE: The Printed Circuit Board shown is 75% of the original.

MRF843

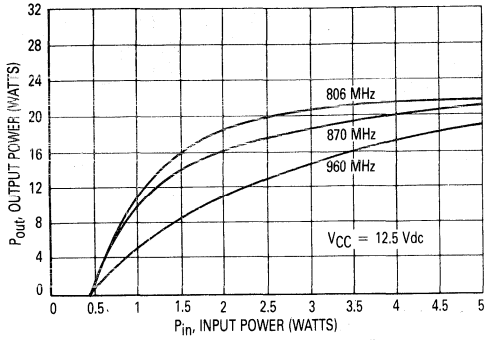


Figure 4. Output Power versus Input Power

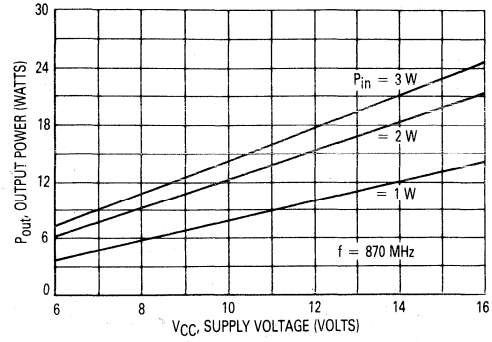


Figure 5. Output Power versus Supply Voltage

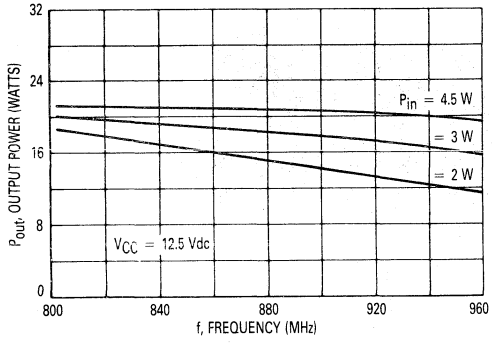


Figure 6. Output Power versus Frequency

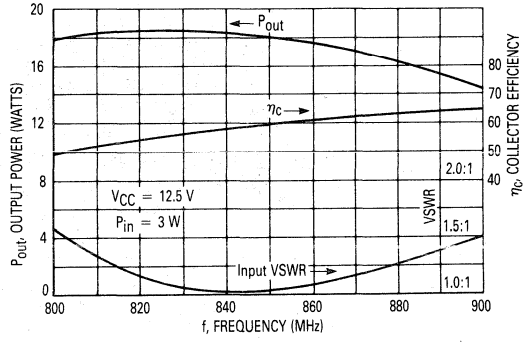
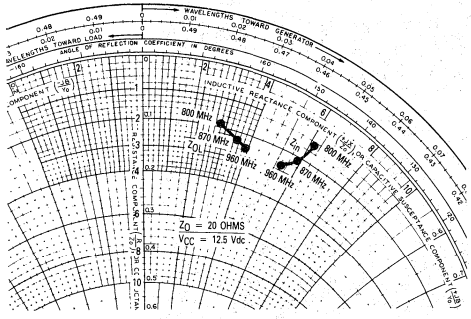


Figure 7. Typical Performance in Broadband Test Fixture



f MHz	Z_{in} Ohms	Z_{OL}* Ohms
800	1.23 + j 6.13	1.98 + j 2.62
870	2.09 + j 5.91	2.24 + j 3.49
960	2.58 + j 5.46	2.51 + j 3.92

NOTE: Circuit tuning and input power adjusted to maintain output power of 15 W and 65% efficiency.

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

Figure 8. Series Equivalent Input and Output Impedance

MRF843F

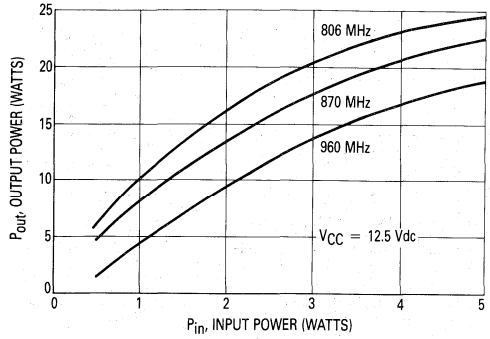


Figure 9. Output Power versus Input Power

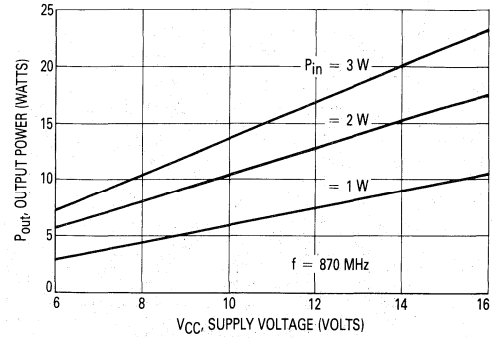


Figure 10. Output Power versus Supply Voltage

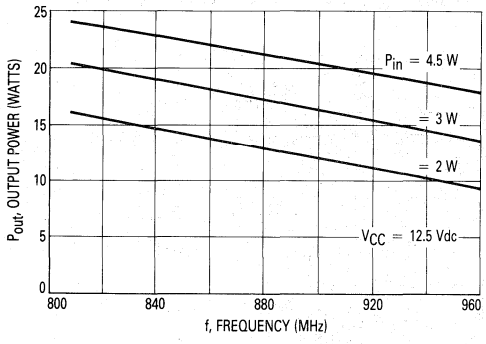


Figure 11. Output Power versus Frequency

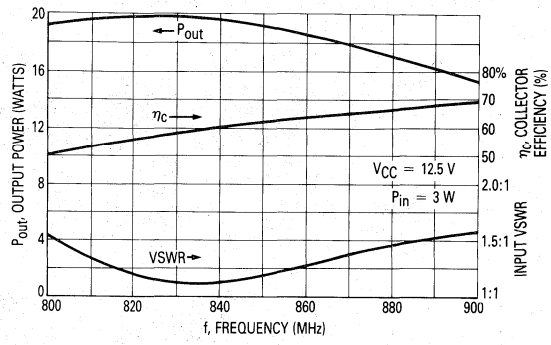
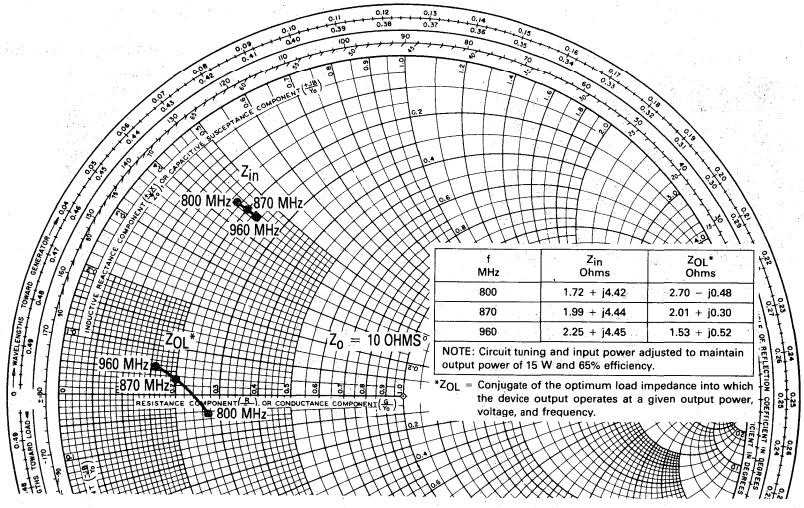


Figure 12. Typical Performance in Broadband Test Fixture

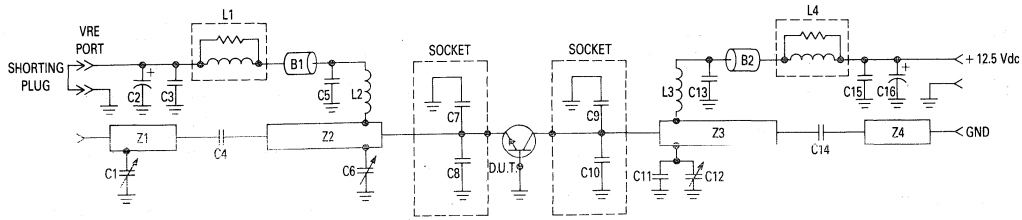


f MHz	Z_{in} Ohms	Z_{OL}* Ohms
800	1.72 + j4.42	2.70 − j0.48
870	1.99 + j4.44	2.01 + j0.30
960	2.25 + j4.45	1.53 + j0.52

NOTE: Circuit tuning and input power adjusted to maintain output power of 15 W and 65% efficiency.

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

Figure 13. Series Equivalent Input and Output Impedance



C1 — 0.6–4.5 pF Johansen Gigatrim (7270)
C2, C16 — 1 μF, 35 WV Tantalum
C3, C15 — 1000 pF Underwood Mica J101
C4, C14 — 47 pF 100 Mil ATC
C5, C13 — 91 pF Mini-Underwood Mica
C6, C12 — 0.8–8 pF Johansen Gigatrim (7290)
C7, C8 — 8 pF Mini-Underwood Mica
C9, C10 — 15 pF Mini-Underwood Mica
C11 — 10 pF Mini-Underwood Mica

L1, L4 — 11 Turns #20 AWG over 100 HM ½ W Resistor
L2, L3 — 4 Turns #18 AWG, 0.15″ ID
B1, B2 — Ferrite Bead, Ferroxcube 56-590-65-3B
Z1, Z4 — 50 Ohm Microstrip
Z2 — 36 Ohm Microstrip λ/4 @ 838 MHz
Z3 — 32 Ohm Microstrip λ/4 @ 838 MHz
Board Material — 0.032″ Glass Teflon, 2 oz. Copper Clad, ϵ_r = 2.55

Figure 14. MRF843F 800–900 MHz Broadband Test Circuit

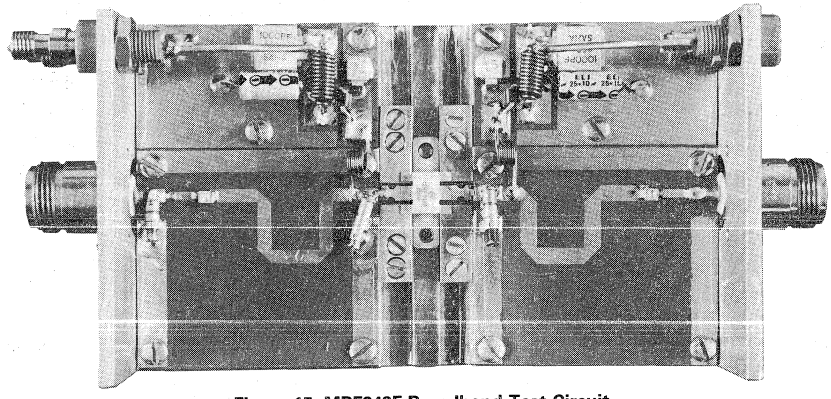


Figure 15. MRF843F Broadband Test Circuit

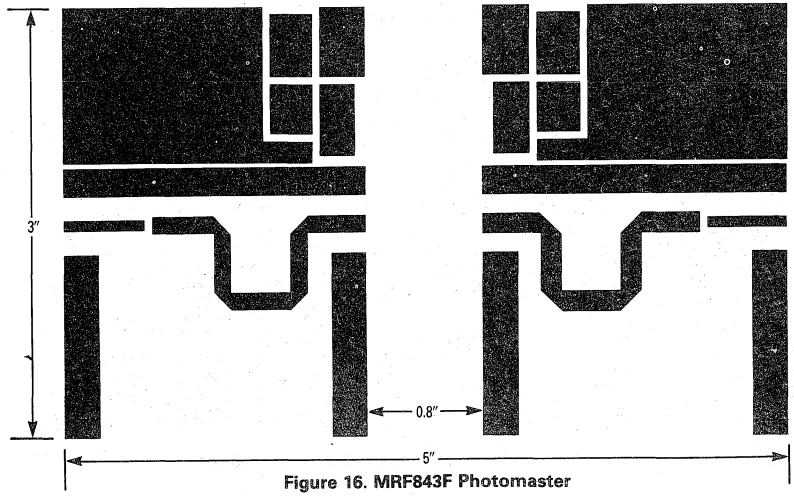
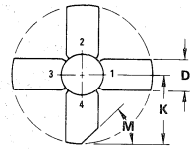
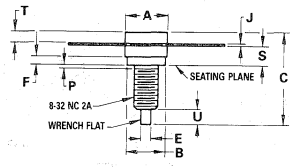


Figure 16. MRF843F Photomaster

NOTE: The Printed Circuit Board shown is 75% of the original.

OUTLINE DIMENSIONS

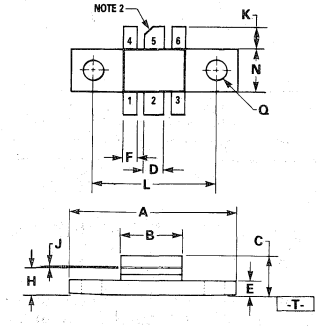




STYLE 4:
PIN 1. BASE 3. BASE
2. EMITTER 4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.06	7.26	0.278	0.286
B	6.20	6.50	0.244	0.256
C	14.99	16.51	0.590	0.650
D	5.46	5.96	0.215	0.235
E	1.40	1.65	0.055	0.065
F	1.52	—	0.060	—
J	0.08	0.17	0.003	0.007
K	11.05	—	0.435	—
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
S	3.00	3.25	0.118	0.128
T	1.40	1.77	0.055	0.070
U	2.92	3.68	0.115	0.145

CASE 244-04



NOTES:
1. POSITIONAL TOLERANCE FOR Q HOLES:
⌖ | ϕ 0.15 (0.006) Ⓜ | T | A Ⓜ | N Ⓜ
2. IDENTIFICATION NOTCH 1.0mm (0.04) MIN X 45°.
3. DIM D APPLIES 2 PLACES,
DIM K APPLIES 2 PLACES,
DIM Q APPLIES 2 PLACES,
DIM F APPLIES 4 PLACES.
4. DIMENSIONS A AND N ARE DATUMS AND
-T- IS DATUM SURFACE.
5. DIMENSION B APPLIES TO LEAD FRAME AND Beo.
6. POSITIONAL TOLERANCE FOR D TERMINAL AND DIMENSION B:
⌖ | 0.38 (0.15) Ⓜ | T | A Ⓜ | N Ⓜ

STYLE 1:
PIN 1. BASE (COMMON)
2. EMITTER (INPUT)
3. BASE (COMMON)
4. BASE (COMMON)
5. COLLECTOR (OUTPUT)
6. BASE (COMMON)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.51	25.02	0.965	0.985
B	9.02	9.52	0.355	0.375
C	5.84	6.60	0.230	0.260
D	2.92	3.18	0.115	0.125
E	2.69	2.95	0.106	0.116
F	1.91	2.16	0.075	0.085
H	4.06	4.31	0.160	0.170
J	0.10	0.15	0.004	0.006
K	2.29	2.79	0.090	0.110
L	18.42 BSC		0.725 BSC	
N	5.72	6.12	0.225	0.241
Q	3.18	3.43	0.125	0.135

CASE 319-04

3

MRF844

The RF Line

30 W-870 MHz

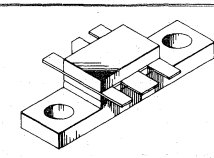
RF POWER TRANSISTOR

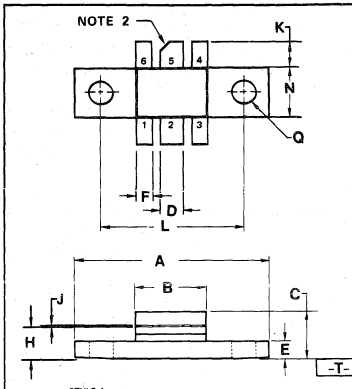
NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed for 12.5 volt UHF large-signal, common-base amplifier applications in industrial and commercial FM equipment operating in the range of 806–960 MHz.

- Specified 12.5 Volt, 870 MHz Characteristics
  Output Power = 30 Watts
  Minimum Gain = 5.2 dB
  Efficiency = 50%
- Series Equivalent Large-Signal Characterization
- Internally Matched Input for Broadband Operation
- Tested for Load Mismatch Stress at All Phase Angles with 20:1 VSWR @ High Line and RF Overdrive
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Silicon Nitride Passivated





STYLE 1:
PIN 1. BASE (COMMON) 4. BASE (COMMON)
2. EMITTER (INPUT) 5. COLLECTOR (OUTPUT)
3. BASE (COMMON) 6. BASE (COMMON)

NOTES:
1. POSITIONAL TOLERANCE FOR Q HOLES: ⌖ | ⌀ 0.15 (0.006) Ⓜ | T | A Ⓜ | N Ⓜ |
2. IDENTIFICATION NOTCH 1.0mm (0.04) MIN X 45°.
3. DIM Q APPLIES 2 PLACES.
   DIM K APPLIES 2 PLACES.
   DIM Q APPLIES 2 PLACES.
   DIM F APPLIES 4 PLACES.
4. DIMENSIONS A AND N ARE DATUMS AND -T- IS A DATUM SURFACE.
5. DIMENSION B APPLIES TO LEAD FRAME AND Beo.
6. POSITIONAL TOLERANCE FOR D TERMINAL AND DIMENSION B: ⌖ | 0.38 (0.15) Ⓜ | T | A Ⓜ | N Ⓜ |

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.51	25.02	0.965	0.985
B	9.02	9.52	0.355	0.375
C	5.84	6.60	0.230	0.260
D	2.92	3.18	0.115	0.125
E	2.69	2.95	0.106	0.116
F	1.91	2.16	0.075	0.085
H	4.06	4.31	0.160	0.170
J	0.10	0.15	0.004	0.006
K	2.29	2.79	0.090	0.110
L	18.42 BSC		0.725 BSC	
N	5.72	6.12	0.225	0.241
Q	3.18	3.43	0.125	0.135

CASE 319-04

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	10.9	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate Above 25°C	P_D	115 0.66	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	1.5	°C/W

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

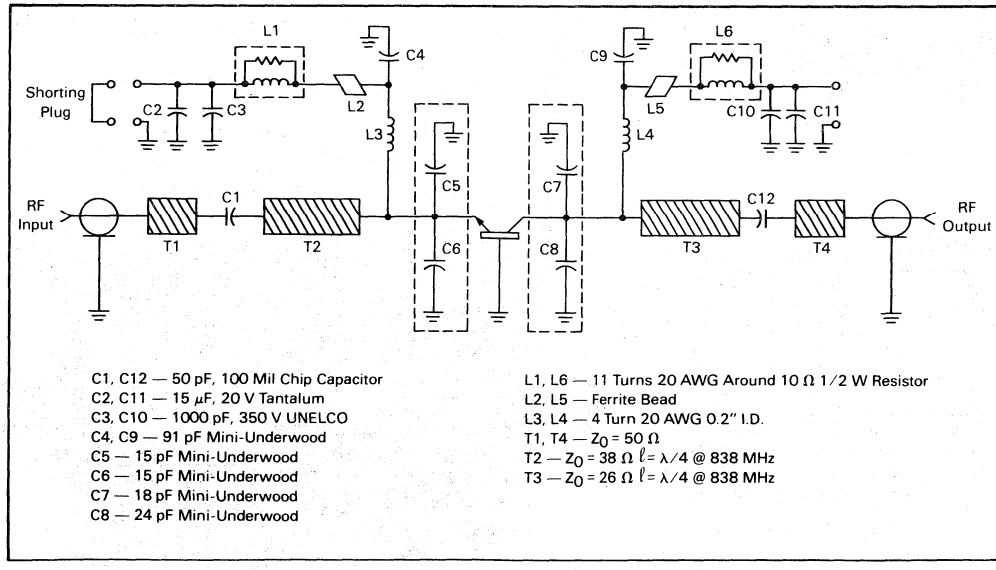
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	40	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	60	90	pF
FUNCTIONAL TEST					
Common-Base Amplifier Power Gain (P_{out} = 30 W, V_{CC} = 12.5 Vdc, f = 870 MHz)	G_{PB}	5.2	6.0	–	dB
Collector Efficiency (P_{out} = 30 W, V_{CC} = 12.5 Vdc, f = 870 MHz)	η	50	55	–	%
Load Mismatch Stress (V_{CC} = 15.5 Vdc, P_{in} = 12 W*, f = 870 MHz, VSWR = 20:1, all phase angles)	–	No Degradation in Output Power			

*P_{in} = 150% of the typical input power requirement for 30 W output power @ 12.5 Vdc.

3

FIGURE 1 – 870 MHz TEST CIRCUIT



C1, C12 — 50 pF, 100 Mil Chip Capacitor
C2, C11 — 15 μF, 20 V Tantalum
C3, C10 — 1000 pF, 350 V UNELCO
C4, C9 — 91 pF Mini-Underwood
C5 — 15 pF Mini-Underwood
C6 — 15 pF Mini-Underwood
C7 — 18 pF Mini-Underwood
C8 — 24 pF Mini-Underwood

L1, L6 — 11 Turns 20 AWG Around 10 Ω 1/2 W Resistor
L2, L5 — Ferrite Bead
L3, L4 — 4 Turn 20 AWG 0.2" I.D.
T1, T4 — Z_O = 50 Ω
T2 — Z_O = 38 Ω $\ell = \lambda/4$ @ 838 MHz
T3 — Z_O = 26 Ω $\ell = \lambda/4$ @ 838 MHz

FIGURE 2 – OUTPUT POWER versus INPUT POWER

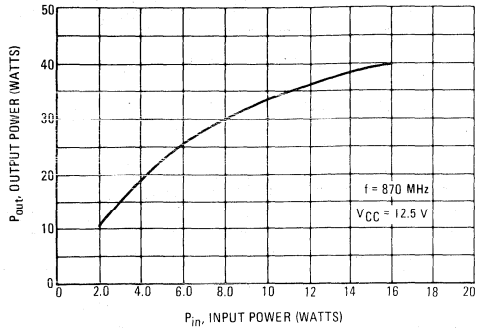


FIGURE 3 – OUTPUT POWER versus FREQUENCY

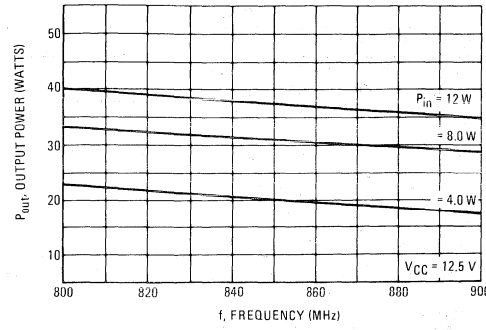


FIGURE 5 – SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCE

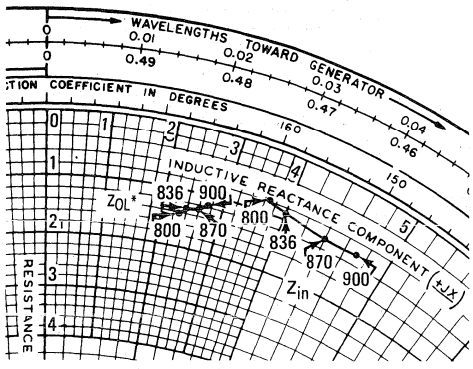
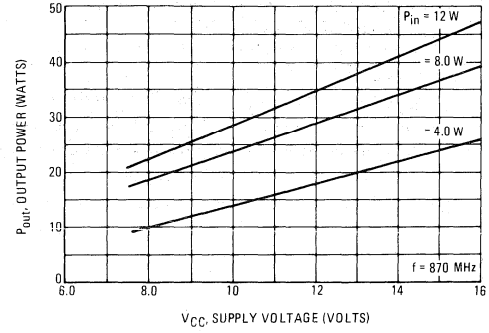


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

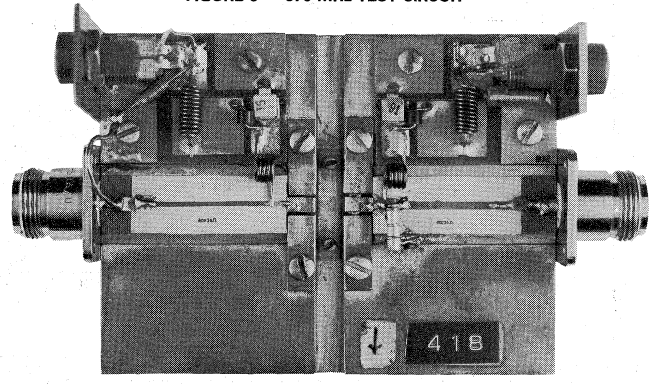


P_{in} = 7.5 W, P_{out} = 30 W, V_{CC} = 12.5 Vdc

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
800	0.8 + j3.7	1.4 + j2.3
836	0.9 + j4.0	1.3 + j2.4
870	1.0 + j4.4	1.25 + j2.6
900	1.0 + j4.7	1.2 + j2.7

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

FIGURE 6 — 870 MHz TEST CIRCUIT



MRF846

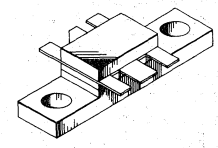
The RF Line

40 W–870 MHz

RF POWER TRANSISTOR

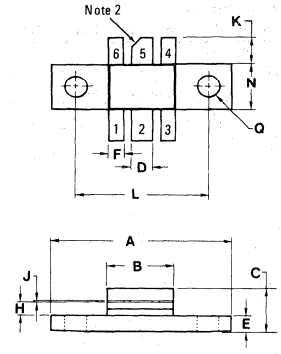
NPN SILICON

NPN SILICON RF POWER TRANSISTOR



. . . designed for 12.5 volt UHF large-signal, common-base amplifier applications in industrial and commercial FM equipment operating in the range of 806–960 MHz.

- Specified 12.5 Volt, 870 MHz Characteristics
  Output Power = 40 Watts
  Minimum Gain = 4.3 dB
  Efficiency = 50%
- Series Equivalent Large-Signal Characterization
- Internally Matched Input for Broadband Operation
- Tested for Load Mismatch Stress at All Phase Angles with 10:1 VSWR @ High Line and RF Overdrive
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Silicon Nitride Passivated



STYLE 1:
PIN 1. BASE (COMMON)
2. EMITTER (INPUT)
3. BASE (COMMON)
4. BASE (COMMON)
5. COLLECTOR (OUTPUT)
6. BASE (COMMON)

NOTES:
1. HOLES WITHIN 0.15 mm (0.006) TRUE POSITION TO EACH OTHER AT MAXIMUM MATERIAL CONDITION.
2. IDENTIFICATION NOTCH 1.0 mm (0.04) MIN × 45°.
3. DIM D APPLIES 2 PLACES, DIM K APPLIES 2 PLACES, DIM Q APPLIES 2 PLACES, DIM F APPLIES 4 PLACES.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.51	25.02	0.965	0.985
B	8.76	9.02	0.345	0.355
C	5.72	6.48	0.225	0.255
D	2.92	3.18	0.115	0.125
E	2.29	2.54	0.090	0.100
F	1.78	2.03	0.070	0.080
H	1.65	1.90	0.065	0.075
J	0.10	0.15	0.004	0.006
K	2.29	2.79	0.090	0.110
L	18.42	BSC	0.725	BSC
N	5.72	5.97	0.225	0.235
Q	3.05	3.30	0.120	0.130

CASE 319-04

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	14.0	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate Above 25°C	P_D	150 0.86	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	1.17	°C/W

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

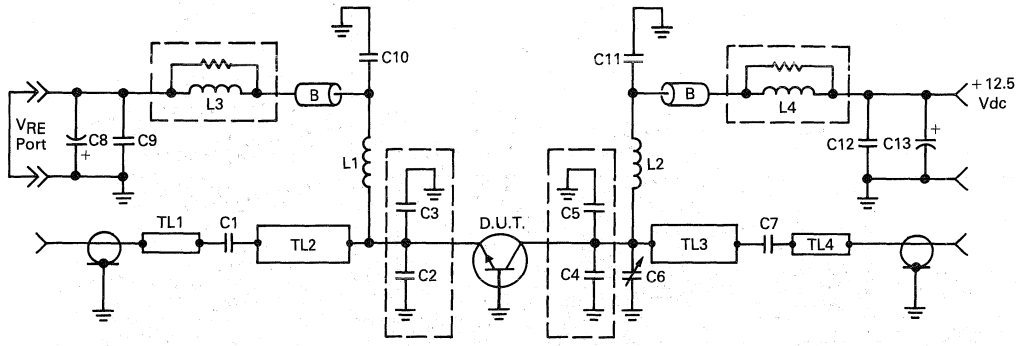
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	50	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	85	120	pF
FUNCTIONAL TEST					
Common-Base Amplifier Power Gain (P_{out} = 40 W, V_{CC} = 12.5 Vdc, f = 870 MHz)	G_{PB}	4.3	5.2	–	dB
Collector Efficiency (P_{out} = 40 W, V_{CC} = 12.5 Vdc, f = 870 MHz)	η	50	55	–	%
Load Mismatch Stress (V_{CC} = 15.5 Vdc, P_{in} = 15 W, f = 870 MHz, VSWR = 10:1, all phase angles)	–	No Degradation in Output Power			

*P_{in} = 125% of the typical input power requirement for 40 W output power @ 12.5 Vdc.

3

FIGURE 1 — 870 MHz TEST CIRCUIT SCHEMATIC



C1 — 43 pF, 100 Mil Chip Capacitor
C2 — 12 pF Mini-Unelco
C3 — 15 pF Mini-Unelco
C4 — 21 pF Mini-Unelco
C5 — 18 pF Mini-Unelco
C6 — 0.8–8.0 pF Johanson Gigatrim
C7 — 47 pF, 100 Mil Chip Capacitor
C8 — 10 μF, 25 WV
C9, C12 — 1000 pF Unelco J101
C10, C11 — 91 pF Mini-Unelco
C13 — 25 μF, 25 WV

L1, L2 — 4 Turns #18 Enameled; 200 Mil ID
L3, L4 — 15 Turns #24 Enameled Over 12 ohm Carbon Resistor
B — Ferrite Bead; Ferroxcube 56-590-65-3B
TL1, TL4 — Micro Strip; 50 Ω
TL2 — Micro Strip; Z_O = 34 Ω, λ/4 @ 838 MHz
TL3 — Micro Strip; Z_O = 30 Ω, λ/4 @ 838 MHz
Board — 0.032″ Glass Teflon
2 oz. Cu CLAD, ϵ_r = 2.55

FIGURE 2 – OUTPUT POWER versus INPUT POWER

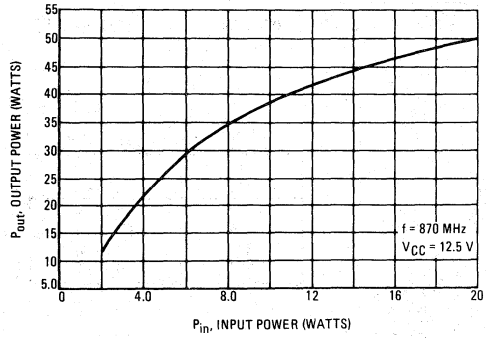


FIGURE 3 – OUTPUT POWER versus FREQUENCY

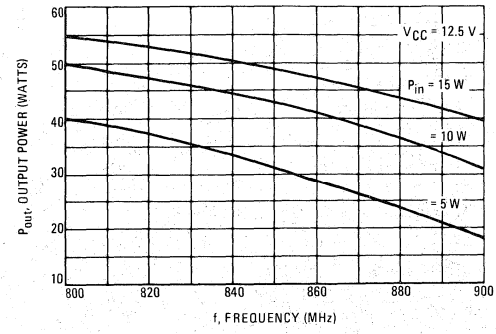


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

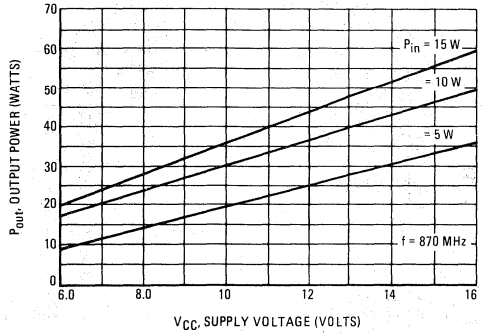


FIGURE 5 — 870 MHz TEST CIRCUIT

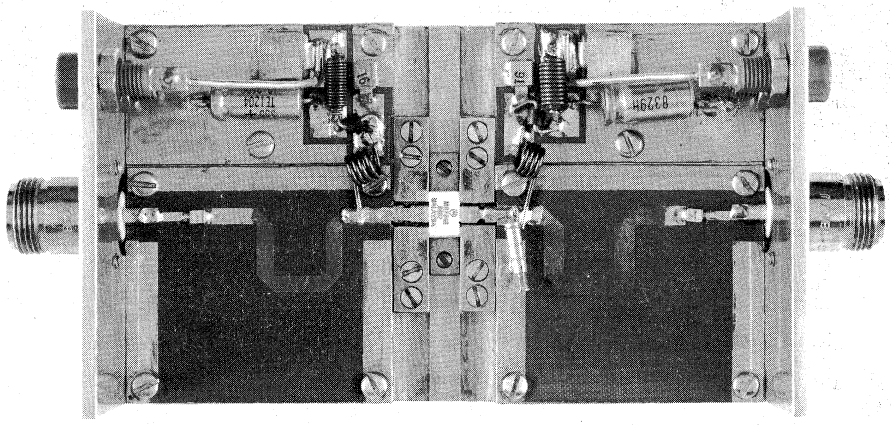
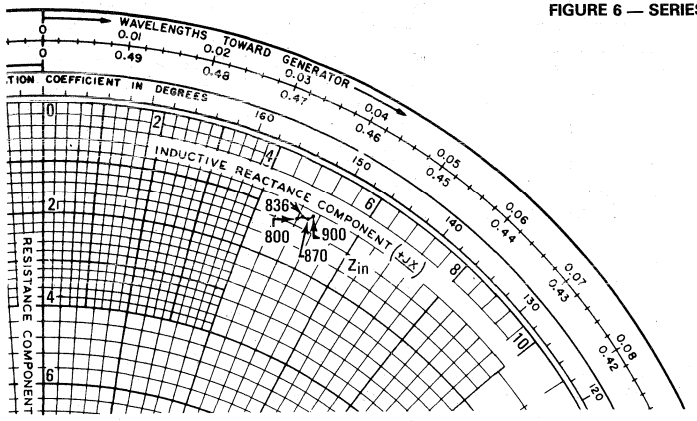


FIGURE 6 — SERIES EQUIVALENT INPUT IMPEDANCES

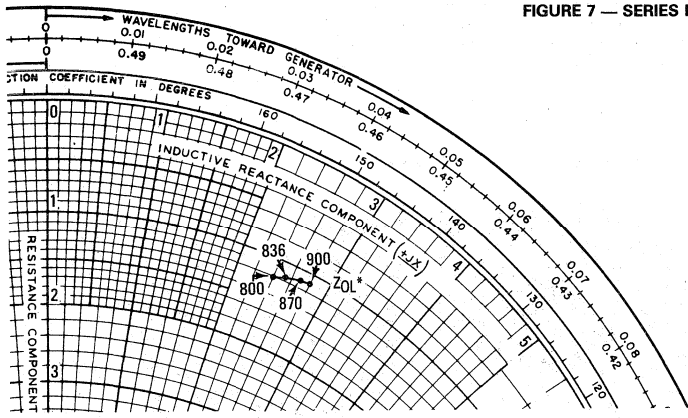


V_{CC} = 12.5 Vdc, P_{in} = 12 W

f MHz	Z_{in} Ohms
800	1.1 + j4.8
836	1.0 + j4.9
870	1.0 + j5.0
900	0.9 + j5.1

3

FIGURE 7 — SERIES EQUIVALENT OUTPUT IMPEDANCES



V_{CC} = 12.5 Vdc, P_{out} = 40 W

f MHz	Z_{OL}* Ohms
800	1.2 + j2.4
836	1.15 + j2.5
870	1.1 + j2.7
900	1.1 + j2.8

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

MRF848

Advance Information

The RF Line

NPN SILICON RF POWER TRANSISTOR

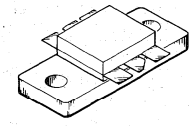
. . . designed for 12.5 Volt UHF large-signal, common base amplifier applications in industrial and commercial FM equipment operating in the range of 804–960 MHz.

- Motorola Advanced Amplifier Concept Package
- Specified 12.5 Volt, 870 MHz Characteristics
  Output Power = 60 Watts
  Minimum Gain = 4.0 dB
  Efficiency = 60%
- Double Input/Output Matched for Wideband Performance and Simplified External Matching
- Series Equivalent Large-Signal Characterization
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Silicon Nitride Passivated

60 W 800–960 MHz

RF POWER TRANSISTOR

NPN SILICON

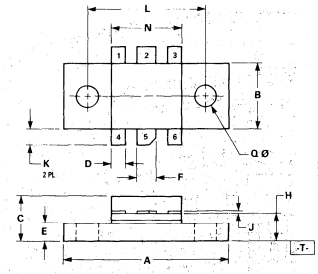


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Continuous	I_C	14	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	175 1.0	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.00	°C/W



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM PLANE.
2. POSITIONAL TOLERANCE FOR Q HOLES: ⌖ ⌀ .13 (0.005) Ⓜ | A Ⓜ | B Ⓜ
3. DIMENSION -D- FOUR PLACES. DIMENSION -F- TWO PLACES.
4. DIMENSIONING AND TOLERANCING PER Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. BASE
5. COLLECTOR
6. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.51	25.02	0.965	0.985
B	9.91	10.41	0.390	0.410
C	6.86	7.36	0.270	0.290
D	1.91	2.28	0.075	0.090
E	2.42	2.92	0.095	0.115
F	5.47	5.96	0.110	0.130
H	3.94	4.44	0.155	0.175
J	0.10	0.15	0.004	0.006
K	2.29	2.94	0.090	0.116
L	18.41 BSC		0.725 BSC	
N	10.54	11.04	0.415	0.435
Q	3.18	3.42	0.125	0.135

CASE 333A

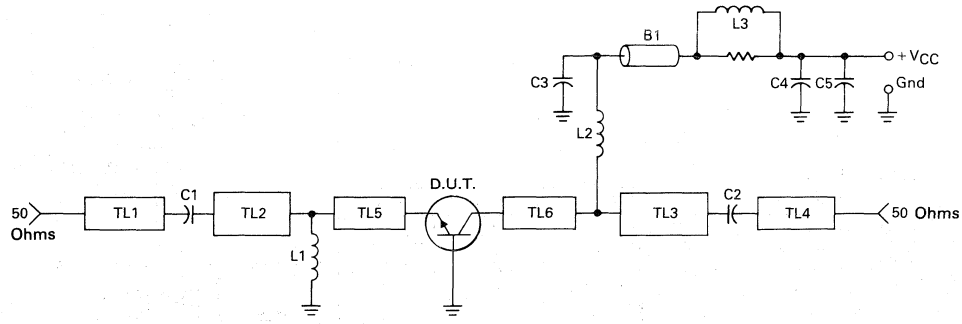
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	20	50	150	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	88	110	pF
FUNCTIONAL TESTS					
Common-Base Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 60 W, f = 870 MHz)	G_{pb}	4.0	4.8	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 60 W, f = 870 MHz)	η	60	68	—	%
Output Mismatch Stress (V_{CC} = 15.5 Vdc, P_{in} = 24 W, f = 870 MHz, VSWR = 10:1, all phase angles)	ψ	No degradation in output power			

3

FIGURE 1 — 800–870 MHz BROADBAND TEST CIRCUIT



C1, C2 — 39 pF, 100 Mil Chip Capacitor
C3 — 91 pF, Mini Underwood
C4 — 1000 pF, 350 V Unelco
C5 — 10 μF, 35 V Tantulum
L1, L2 — 4 Turns #26 AWG Choke
L3 — 11 Turns #20 AWG Choke on 10 Ohm Resistor
B1 — Bead, Ferroxcube 56-390-65/3B

TL1, TL4 — 50 Ohm Microstrip
TL2 — 17.4 Ohm, θ=85° Microstrip @ 870 MHz
TL3 — 15.9 Ohm, θ=70° Microstrip @ 870 MHz
TL5, TL6 — 140 x 200 Mils
Board Material Epsilam-10 50 Mil

FIGURE 2 — OUTPUT POWER versus INPUT POWER

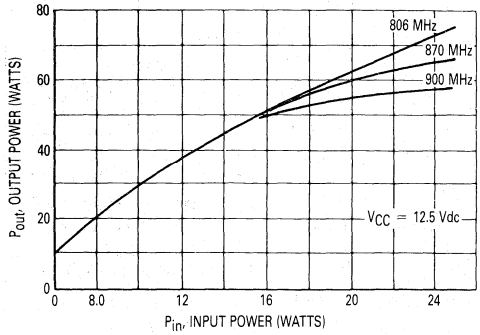


FIGURE 3 — OUTPUT POWER versus SUPPLY VOLTAGE

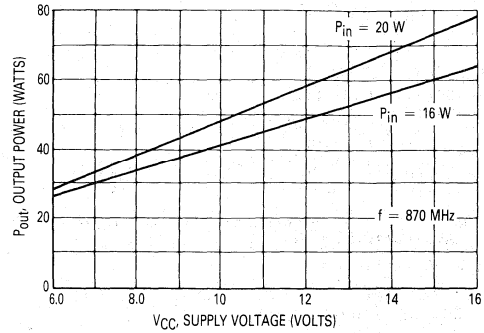


FIGURE 4 — OUTPUT POWER versus FREQUENCY

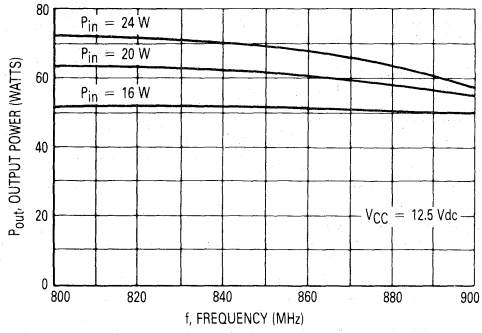


FIGURE 5 — TYPICAL BROADBAND CIRCUIT PERFORMANCE

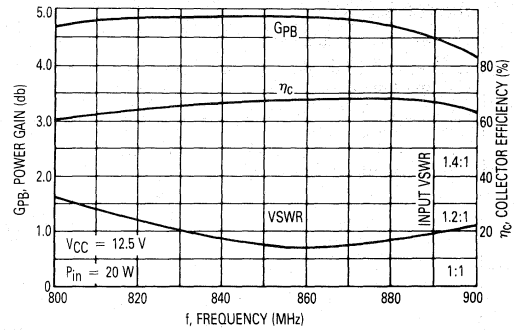
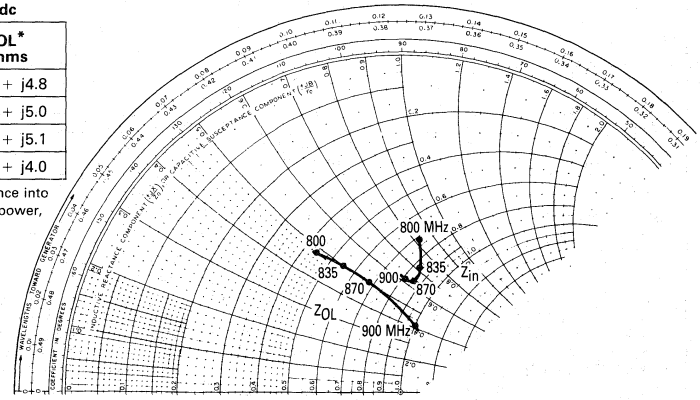


FIGURE 6 — INPUT/OUTPUT IMPEDANCE

P_{out} = 60 Watts, V_{CC} = 12.5 Vdc

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
800	7.16 + j8.2	4.5 + j4.8
835	8.7 + j6.9	5.45 + j5.0
870	8.76 + j6.17	6.75 + j5.1
900	8.25 + j6.06	10.2 + j4.0

*Z_{OL} = Conjugate of optimum load impedance into which the device operates at a given output power, voltage and frequency.



3

MRF873

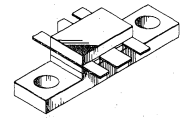
15 W 806-960 MHz RF POWER TRANSISTOR COMMON-EMITTER NPN SILICON

The RF Line

NPN Silicon RF Power Transistor

. . . designed for 12.5 Volt UHF large-signal, **common-emitter** applications in industrial and commercial FM equipment operating in the range of 806–960 MHz.

- Specified 12.5 Volt, 870 MHz Characteristics
  Output Power = 15 Watts
  Minimum Gain = 7 dB
  Efficiency = 60%
- Internally Matched Input for Broadband Operation
- Series Equivalent Large-Signal Characterization
- Capable of withstanding 20:1 VSWR Load Mismatch at Rated Input Power and 15.5 Vdc
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Silicon Nitride Passivated



CASE 319-04

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16.5	Vdc
Collector-Emitter Voltage	V_{CES}	38	Vdc
Emitter-Base Voltage	V_{EBO}	4	Vdc
Collector-Current — Continuous	I_C	2.4	Adc
Operating Junction Temperature	T_J	200	°C
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	44 0.25	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

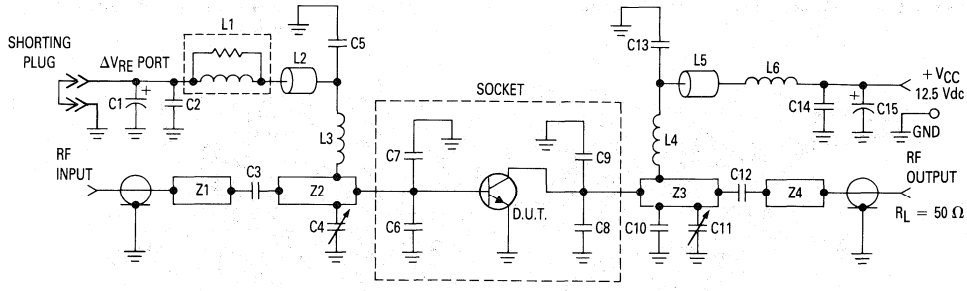
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	16.5	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	38	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 5 mAdc, I_C = 0)	$V_{(BR)EBO}$	4	—	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	5	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1 Adc, V_{CE} = 5 Vdc)	h_{FE}	40	—	200	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1 MHz)	C_{ob}	—	19.5	25	pF

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.
(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (Broadband) (V_{CC} = 12.5 Vdc, P_{out} = 15 W, f = 870 MHz)	G_{pe}	7	8	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 15 W, f = 870 MHz)	η	60	69	—	%
Load Mismatch Stress (V_{CC} = 15.5 Vdc, f = 870 MHz, P_{in} = 3 W, VSWR = 20:1, all phase angles)	ψ	No degradation in output power			



C1, C15 — 10 μF, 25 V Tantalum
C2, C14 — 1000 pF, 350 V Unelco
C3, C12 — 43 pF, 100 Mil ATC Chip Capacitor
C5, C13 — 91 pF, Mini-Unelco
C4, C11 — 0.8–8 pF Johansen Gigatrim 7290 Variable
C6 — 16 pF Mini-Underwood
C7, C8, C9 — 12 pF Mini-Underwood
C10 — 10 pF Mini-Underwood

NOTE: C11 ≈ 0.4" down Z3 from socket edge.

L1 — 13 Turn #20 AWG Around 10 Ω 1/2 W Resistor
L2, L5 — Ferroxcube Bead #56-590-65-3B
L3, L4 — 4 Turns #20 AWG Choke ID 0.2"
L6 — 6 Turns #20 AWG Choke ID 0.2 "
Z1, Z4 — 50 Ohm Microstrip
Z2 — 36 Ohm Microstrip λ/4 @ 838 MHz
Z3 — 26 Ohm Microstrip λ/4 @ 838 MHz

Board Material — 0.032" Glass Teflon 2 oz. Copper Clad ϵ_r = 2.55

Figure 1. 806–900 MHz Broadband Test Fixture

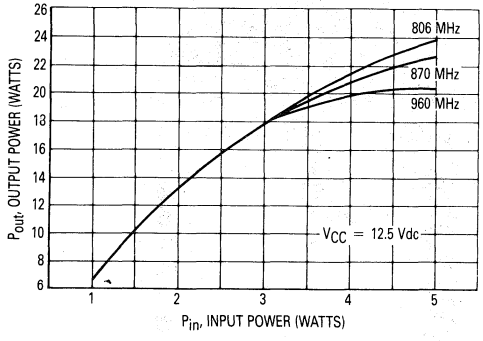


Figure 2. Output Power versus Input Power

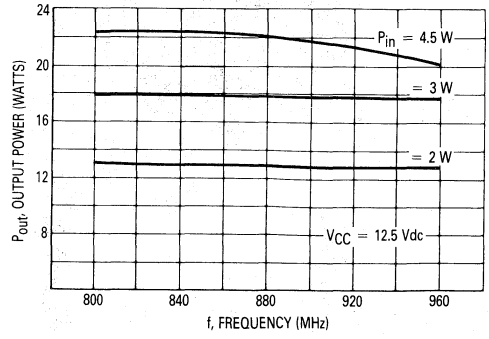


Figure 3. Output Power versus Frequency

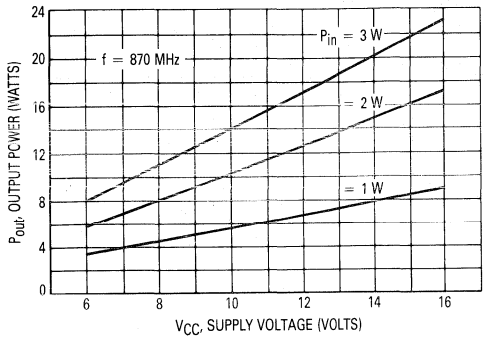


Figure 4. Output Power versus Supply Voltage

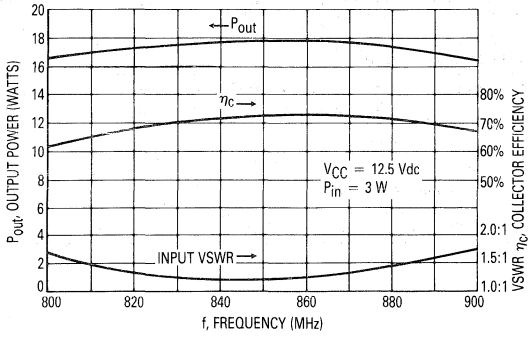


Figure 5. Typical Performance in Broadband Test Fixture

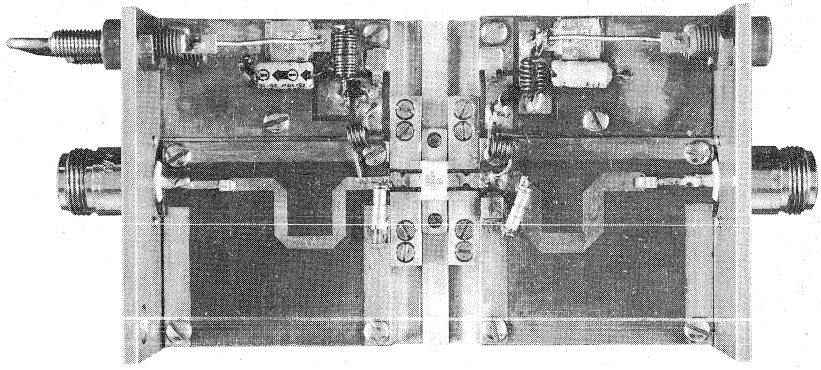


Figure 6. Photo Test Circuit

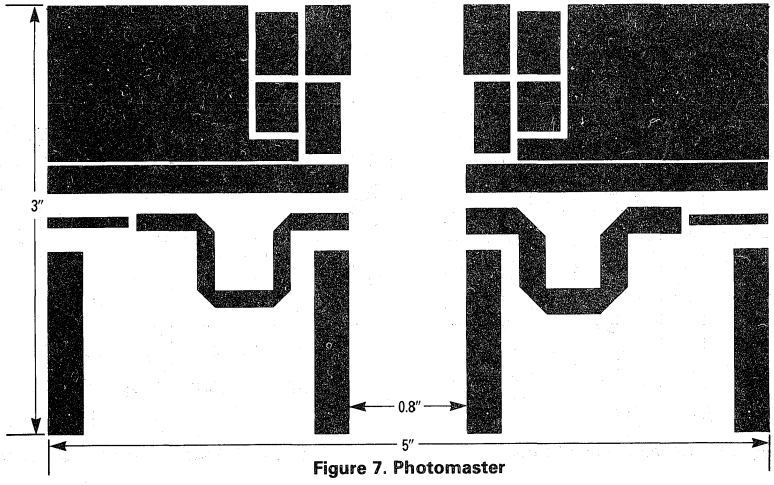
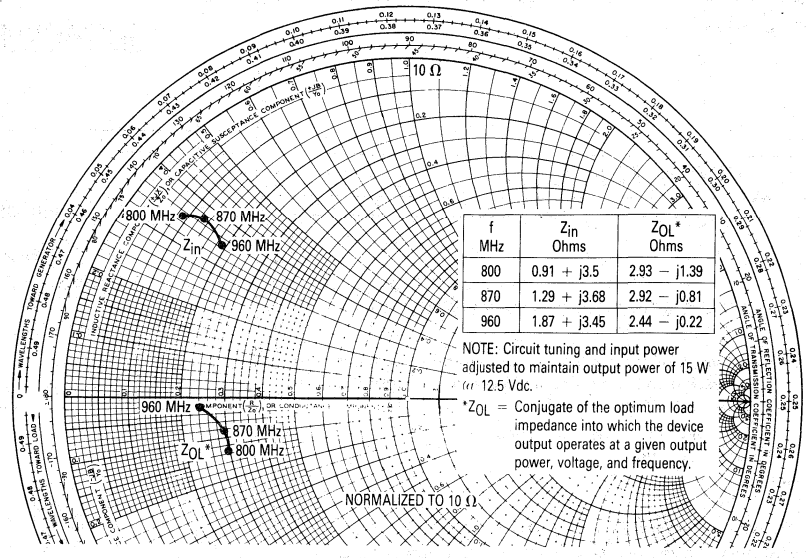


Figure 7. Photomaster

NOTE: The Printed Circuit Board shown is 75% of the original.



f MHz	Z_{in} Ohms	Z_{OL}^* Ohms
800	0.91 + j3.5	2.93 − j1.39
870	1.29 + j3.68	2.92 − j0.81
960	1.87 + j3.45	2.44 − j0.22

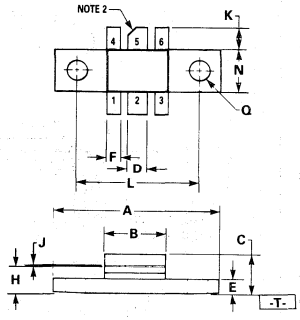
NOTE: Circuit tuning and input power adjusted to maintain output power of 15 W @ 12.5 Vdc.

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

Figure 8. Series Equivalent Input/Output Impedances

3

OUTLINE DIMENSIONS



NOTES:
1. POSITIONAL TOLERANCE FOR Q HOLES: ⌖ ϕ 0.15 (0.006) Ⓜ T A Ⓜ N Ⓜ
2. IDENTIFICATION NOTCH 1.0mm (0.04) MIN X 45°.
3. DIM D APPLIES 2 PLACES,
   DIM K APPLIES 2 PLACES,
   DIM Q APPLIES 2 PLACES,
   DIM F APPLIES 4 PLACES.
4. DIMENSIONS A AND N ARE DATUMS AND -T- IS DATUM SURFACE
5. DIMENSION B APPLIES TO LEAD FRAME AND Beo.
6. POSITIONAL TOLERANCE FOR D TERMINAL AND DIMENSION B: ⌖ 0.38 (0.15) Ⓜ T A Ⓜ N Ⓜ

CASE 319-04

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.51	25.02	0.965	0.985
B	9.02	9.52	0.355	0.375
C	5.84	6.60	0.230	0.260
D	2.92	3.18	0.115	0.125
E	2.69	2.95	0.106	0.116
F	1.91	2.16	0.075	0.085
H	4.06	4.31	0.160	0.170
J	0.10	0.15	0.004	0.006
K	2.29	2.79	0.090	0.110
L	18.42 BSC		0.725 BSC	
N	5.72	6.12	0.225	0.241
Q	3.18	3.43	0.125	0.135

STYLE 2:
PIN 1. EMITTER (COMMON)
2. BASE (INPUT)
3. EMITTER (COMMON)
4. EMITTER (COMMON)
5. COLLECTOR (OUTPUT)
6. EMITTER (COMMON)

MRF890

The RF Line

2.0 W 900 MHz

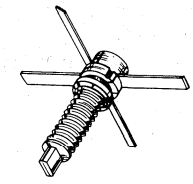
RF POWER TRANSISTOR

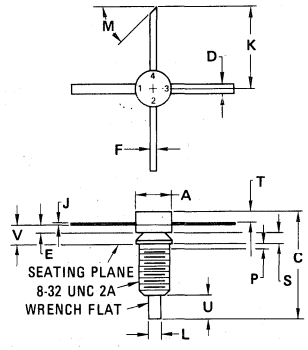
NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed for 24 volt UHF large-signal, common-emitter amplifier applications in industrial and commercial FM equipment operating in the range of 804 – 960 MHz.

- Specified 24 Volt, 900 MHz Characteristics
  Output Power = 2.0 Watts
  Minimum Gain = 9.0 dB
  Efficiency = 55%
- Series Equivalent Large-Signal Characterization
- Capable of 30:1 VSWR Load Mismatch at Rated Output Power and Supply Voltage
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Silicon Nitride Passivated





STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.08	5.59	0.200	0.220
C	13.97	16.26	0.550	0.640
D	1.40	1.65	0.055	0.065
E	1.02	1.27	0.040	0.050
F	0.64	0.89	0.025	0.035
J	0.08	0.18	0.003	0.007
K	11.05	–	0.435	–
L	1.40	1.65	0.055	0.065
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
S	1.40	1.65	0.055	0.065
T	1.40	1.78	0.055	0.070
U	2.79	3.81	0.110	0.150
V	2.41	2.92	0.095	0.115

CASE 305-01

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	55	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	0.5	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate Above 25°C	P_D	7.0 40	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	25	°C/W

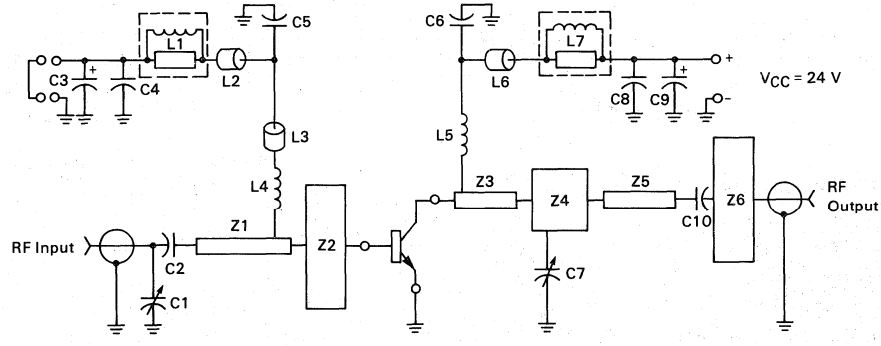
(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	55	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	—	0.5	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	—	100	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 30 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	2.0	—	pF
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (P_{out} = 2.0 W, V_{CC} = 24 Vdc, f = 900 MHz)	G_{PE}	9.0	10.5	—	dB
Collector Efficiency (P_{out} = 2.0 W, V_{CC} = 24 Vdc, f = 900 MHz)	η	55	60	—	%

FIGURE 1 — 850 - 900 MHz TEST CIRCUIT



C1, C7 — Johanson 0.5 - 4.0 pF Giga-Trim
C2, C5, C6 — 91 pF Mini Underwood Mica
C3, C9 — 1.0 μF Electrolytic
C4, C8 — 250 pF Unelco
C10 — 39 pF Mini Underwood
L1, L7 — 10 Turns Around 10 Ω 1/2 W Resistor
L2, L3, L6 — Ferrite Bead
L4, L5 — 4 Turns 26 AWG 0.1" ID
Z1, Z2, Z3, Z4, Z5, Z6 — Distributed Microstrip Elements (see photomask)
Board Material — Glass Teflon ϵ_r = 2.55 t = 0.031"

FIGURE 2 — OUTPUT POWER versus INPUT POWER

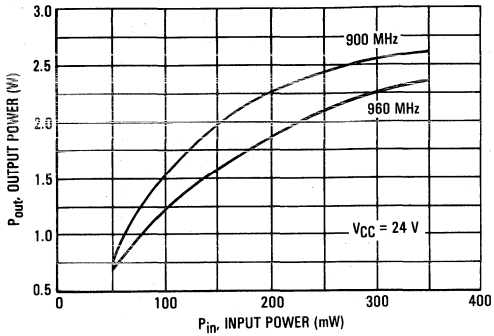


FIGURE 3 — OUTPUT POWER versus SUPPLY VOLTAGE

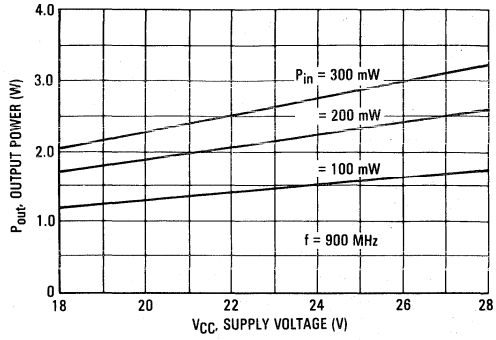


FIGURE 4 — OUTPUT POWER versus FREQUENCY

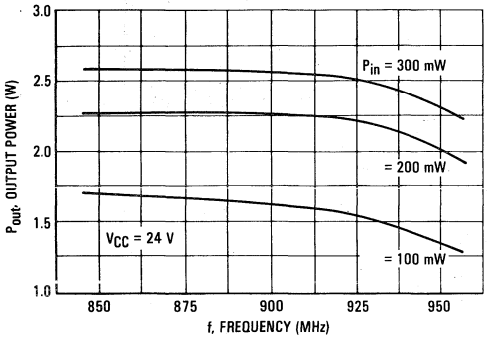


FIGURE 5 — TYPICAL PERFORMANCE IN BROADBAND CIRCUIT

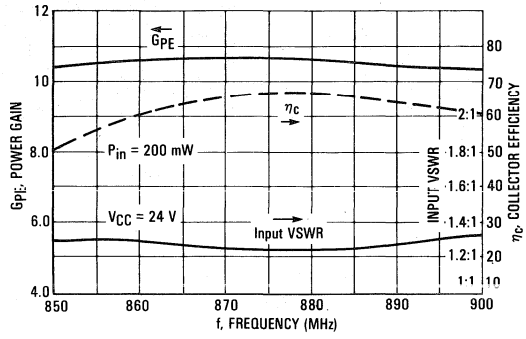
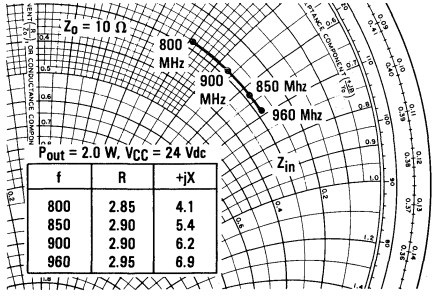
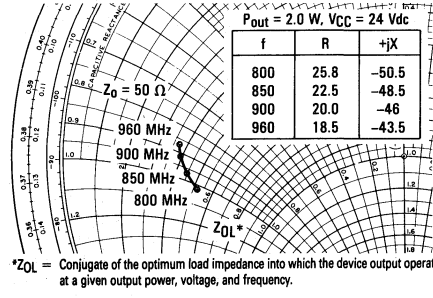


FIGURE 6 — SERIES EQUIVALENT INPUT IMPEDANCE



f	R	+jX
800	2.85	4.1
850	2.90	5.4
900	2.90	6.2
960	2.95	6.9

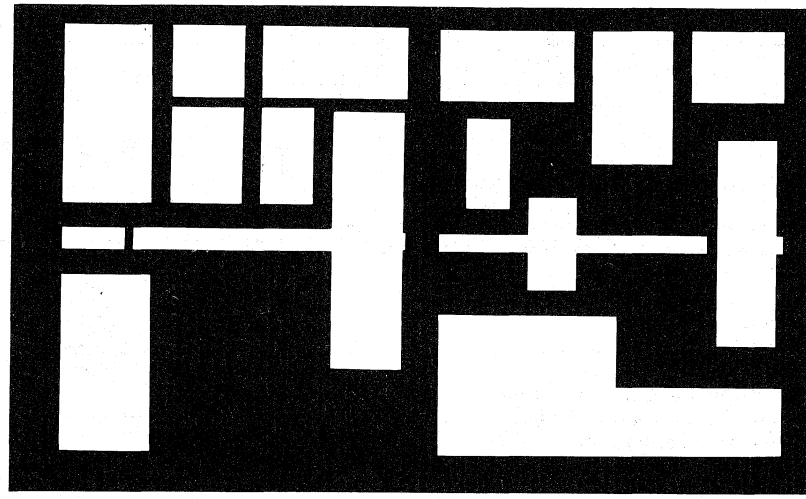
FIGURE 7 — SERIES EQUIVALENT OUTPUT IMPEDANCE



f	R	+jX
800	25.8	−50.5
850	22.5	−48.5
900	20.0	−46
960	18.5	−43.5

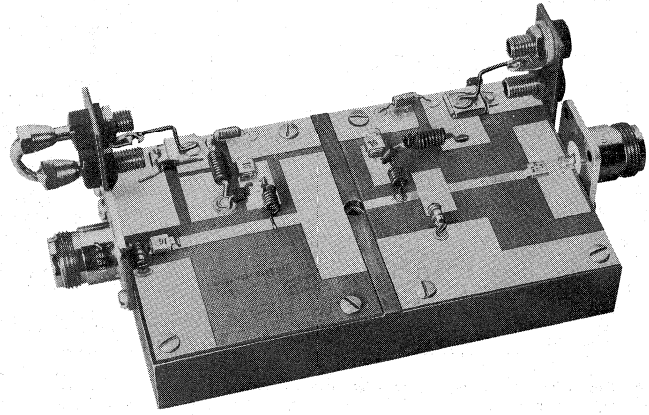
*ZOL = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

FIGURE 8 — PHOTOMASTER FOR TEST FIXTURE



NOTE: The Printed Circuit Board shown is 75% of the original.

FIGURE 9 — 850-900 MHz TEST CIRCUIT



MRF891

The RF Line

5.0 W 900 MHz

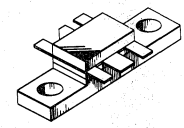
RF POWER TRANSISTOR

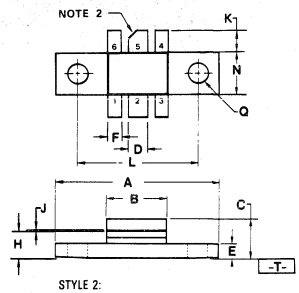
NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed for 24 volt UHF large-signal, common-emitter amplifier applications in industrial and commercial FM equipment operating in the range of 800–960 MHz.

- Specified 24 Volt, 900 MHz Characteristics
  Output Power = 5.0 Watts
  Minimum Gain = 9.0 dB
  Efficiency = 50%
- Series Equivalent Large-Signal Characterization
- Capable of withstanding 20:1 VSWR Load Mismatch at Rated Output Power and Supply Voltage
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Silicon Nitride Passivated





STYLE 2:
PIN 1. EMITTER (COMMON)
2. BASE (INPUT)
3. EMITTER (COMMON)
4. EMITTER (COMMON)
5. COLLECTOR (OUTPUT)
6. EMITTER (COMMON)

NOTES:
1. POSITIONAL TOLERANCE FOR Q HOLES: ⌖ | ϕ 0.15 (0.006) Ⓜ | T | A Ⓜ | N Ⓜ
2. IDENTIFICATION NOTCH 1.0mm (0.04) MIN X 45°.
3. DIM D APPLIES 2 PLACES,
   DIM K APPLIES 2 PLACES,
   DIM Q APPLIES 2 PLACES,
   DIM F APPLIES 4 PLACES.
4. DIMENSIONS A AND N ARE DATUMS AND -T- IS A DATUM SURFACE.
5. DIMENSION B APPLIES TO LEAD FRAME AND Beo.
6. POSITIONAL TOLERANCE FOR D TERMINAL AND DIMENSION B: ⌖ | 0.38 (0.15) Ⓜ | T | A Ⓜ | N Ⓜ

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.51	25.02	0.965	0.985
B	9.02	9.52	0.355	0.375
C	5.84	6.60	0.230	0.260
D	2.92	3.18	0.115	0.125
E	2.69	2.95	0.106	0.116
F	1.91	2.16	0.075	0.085
H	4.06	4.31	0.160	0.170
J	0.10	0.15	0.004	0.006
K	2.29	2.79	0.090	0.110
L	18.42 BSC		0.725 BSC	
N	5.72	6.12	0.225	0.241
Q	3.18	3.43	0.125	0.135

CASE 319-04

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Emitter Voltage	V_{CES}	55	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Continuous	I_C	0.6	Adc
Total Device Dissipation @ T_A = 50°C Derate above 50°C (1)	P_D	18 0.143	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	7.0	°C/W

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

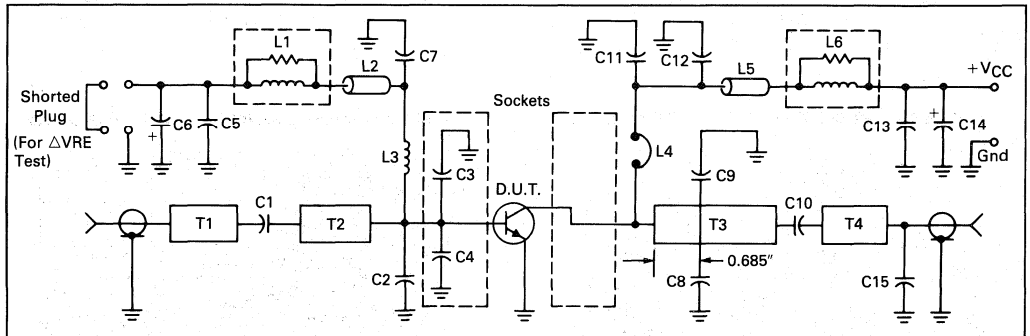
(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	55	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.5 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 200 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	30	—	150	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 24 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	5.1	7.0	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (Broadband) (V_{CC} = 24 Vdc, P_{out} = 5.0 W, f = 900 MHz)	G_{pe}	9.0	10	—	dB
Collector Efficiency (V_{CC} = 24 Vdc, P_{out} = 5.0 W, f = 900 MHz)	η	50	57	—	%
Load Mismatch Stress (V_{CC} = 24 Vdc, P_{in} = 0.63 W, f = 900 MHz, VSWR = 20:1, all phase angles)	ψ	No degradation in output power			

3

FIGURE 1 — BROADBAND TEST FIXTURE



C1	— 39 pF, 100 Mil Chip Capacitor	L1, L6	— 10 Turns #20 AWG Around 10 Ohm 1/2 Watt Resistor
C10	— 47 pF, 100 Mil Chip Capacitor	L3	— 4 Turns #16 AWG Choke
C6, C14	— 10 μF, 25 V Tantalum	L2, L5	— Ferrite Bead
C5, C13	— 1000 pF, 350 V Unelco	L4	— 0.5″, #18 AWG Wire
C7, C11, C12	— 91 pF, Mini-Unelco	T1, T4	— 50 Ohm Microstrip Line
C3, C4	— 12 pF, Mini-Unelco	T2	— W = 165 Mils, ℓ = 1946 Mils
C2, C8, C15	— 0.8–8.0 pF Johansen Gigatrim	T3	— W = 166 Mils, ℓ = 1563 Mils
C9	— 5.0 pF, Mini-Unelco	PC Board	— 0.031″ Glass Teflon (ϵ_r = 2.56)

FIGURE 2 — OUTPUT POWER versus INPUT POWER

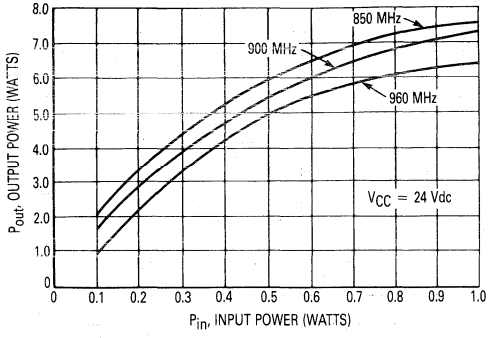


FIGURE 3 — OUTPUT POWER versus SUPPLY VOLTAGE

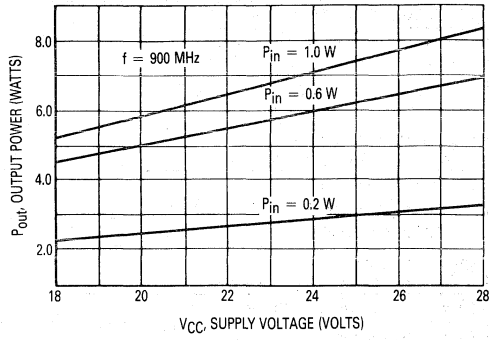


FIGURE 4 — OUTPUT POWER versus FREQUENCY

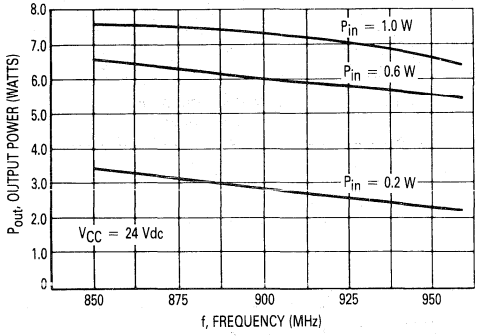


FIGURE 5 — TYPICAL BROADBAND CIRCUIT PERFORMANCE

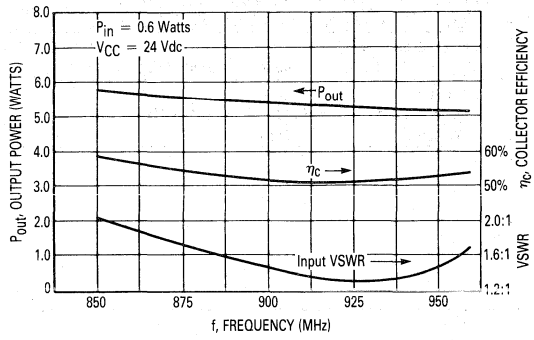


FIGURE 6 — SERIES EQUIVALENT INPUT IMPEDANCE

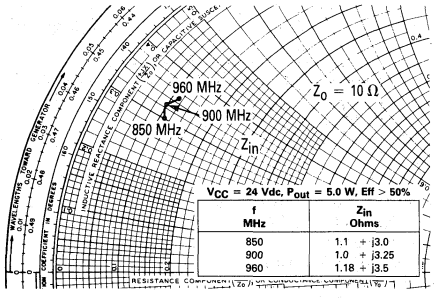


FIGURE 7 — SERIES EQUIVALENT OUTPUT IMPEDANCE

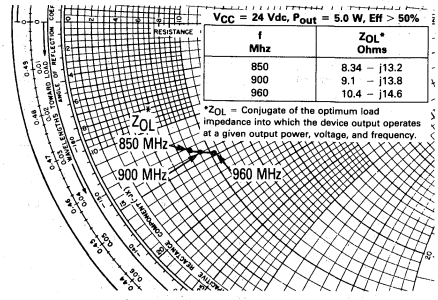
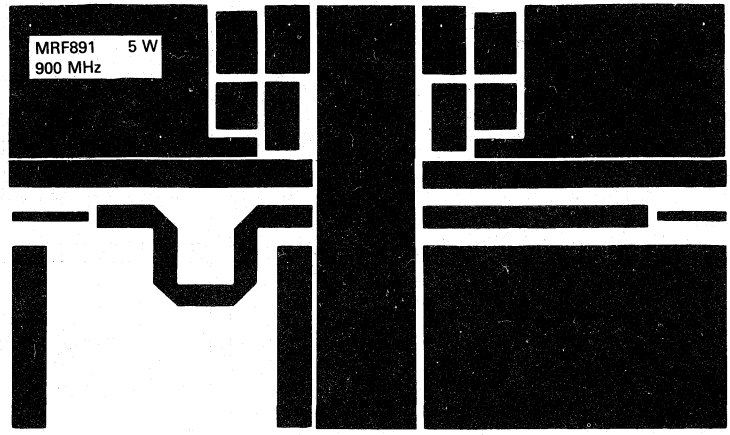
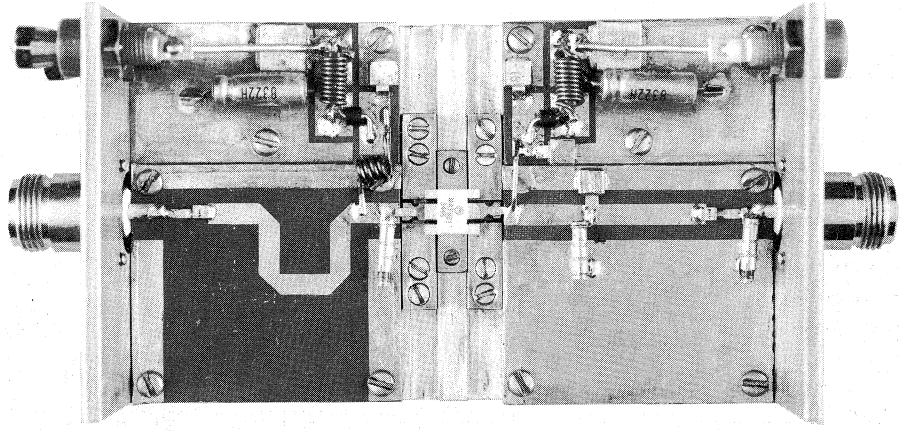


FIGURE 8 — PHOTOMASTER FOR TEST CIRCUIT



NOTE: The Printed Circuit Board shown is 75% of the original.

FIGURE 9 — BROADBAND TEST CIRCUIT



MRF892

The RF Line

14 W 900 MHz

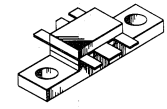
RF POWER TRANSISTOR

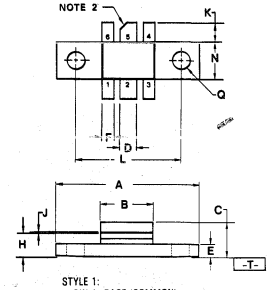
NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed for 24 volt UHF large-signal, common-base amplifier applications in industrial and commercial FM equipment operating in the range of 804 – 960 MHz.

- Specified 24 Volt, 900 MHz Characteristics
  Output Power = 14 Watts
  Minimum Gain = 8.5 dB
  Efficiency = 55%
- Series Equivalent Large-Signal Characterization
- Capable of 30:1 VSWR Load Mismatch at Rated Output Power and Supply Voltage
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Silicon Nitride Passivated





STYLE 1:
PIN 1. BASE (COMMON)
2. EMITTER (INPUT)
3. BASE (COMMON)
4. BASE (COMMON)
5. COLLECTOR (OUTPUT)
6. BASE (COMMON)

NOTES:
1. POSITIONAL TOLERANCE FOR Q HOLES: ⌖ ϕ 0.15 (0.006) Ⓜ T A Ⓜ N Ⓜ
2. IDENTIFICATION NOTCH 1.0mm (0.04) MIN X 45°.
3. DIM D APPLIES 2 PLACES,
   DIM K APPLIES 2 PLACES,
   DIM Q APPLIES 2 PLACES,
   DIM F APPLIES 4 PLACES.
4. DIMENSIONS A AND N ARE DATUMS AND -T- IS A DATUM SURFACE.
5. DIMENSION B APPLIES TO LEAD FRAME AND Beo.
6. POSITIONAL TOLERANCE FOR D TERMINAL AND DIMENSION B: ⌖ 0.38 (0.15) Ⓜ T A Ⓜ N Ⓜ

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	24.51	25.02	0.965	0.985
B	9.02	9.52	0.355	0.375
C	5.84	6.60	0.230	0.260
D	2.92	3.18	0.115	0.125
E	2.69	2.95	0.106	0.116
F	1.91	2.16	0.075	0.085
H	4.06	4.31	0.160	0.170
J	0.10	0.15	0.004	0.006
K	2.29	2.79	0.090	0.110
L	18.42 BSC		0.725 BSC	
N	5.72	6.12	0.225	0.241
Q	3.18	3.43	0.125	0.135

CASE 319-04

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	50.0 V	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	2.5	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate Above 25°C	P_D	50 0.29	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	3.5	°C/W

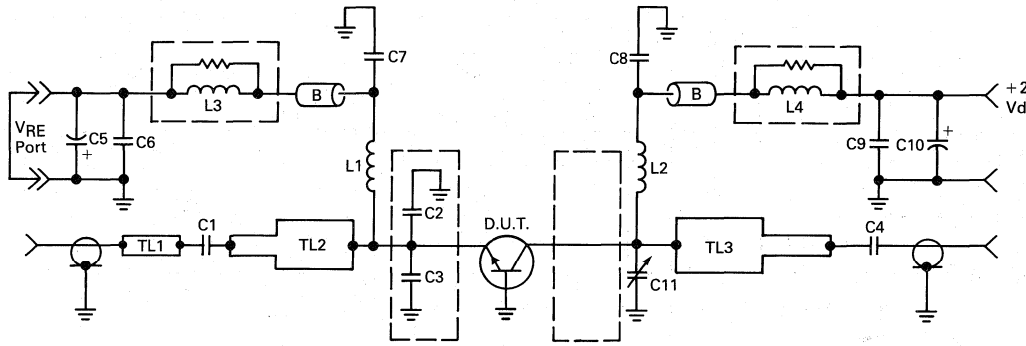
(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 25 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 25 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	50	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	—	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	—	100	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 30 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	12.5	—	pF
FUNCTIONAL TEST					
Common-Base Amplifier Power Gain (P_{out} = 14 W, V_{CC} = 24 Vdc, f = 900 MHz)	G_{PE}	8.5	9.5	—	dB
Collector Efficiency (P_{out} = 14 W, V_{CC} = 24 Vdc, f = 900 MHz)	η	55	60	—	%

FIGURE 1 — 850–900 MHz BROADBAND CIRCUIT SCHEMATIC



C1 — 51 pF, 100 Mil Chip Capacitor
C2, C3 — 13 pF Mini-Unelco
C4 — 43 pF, 100 Mil Chip Capacitor
C5, C10 — 10 μF, 35 WV
C6, C9 — 500 pF Unelco J101
C7, C8 — 91 pF Mini-Unelco
C11 — 0.8–8.0 pF Johanson Gigatrim
L1, L2 — 4 Turns #18 Enameled, 5/32" ID
L3, L4 — 14 Turns #22 Enameled Over 10 Ω Carbon Resistor

B — Ferrite Bead, Ferroxcube 56-590-65-3B
TL1 — Micro Strip, 50 Ω
TL2 — Micro Strip, Z_o = 26 Ω, λ/4 @ 875 MHz
TL3 — Micro Strip, Z_o = 14 Ω, λ/4 @ 875 MHz
Board — 0.032" Glass Teflon
2 oz. Cu CLAD, ϵ_r = 2.55

FIGURE 2 — OUTPUT POWER versus INPUT POWER

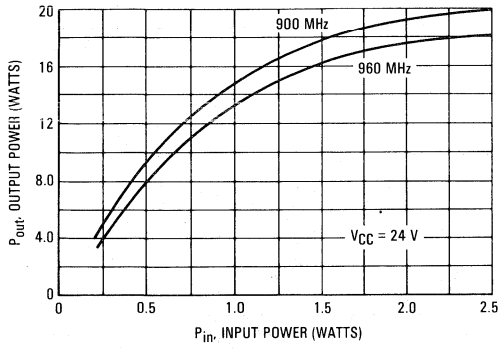


FIGURE 3 — OUTPUT POWER versus SUPPLY VOLTAGE

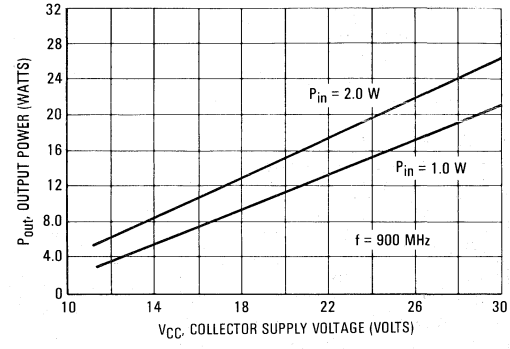


FIGURE 4 — OUTPUT POWER versus FREQUENCY

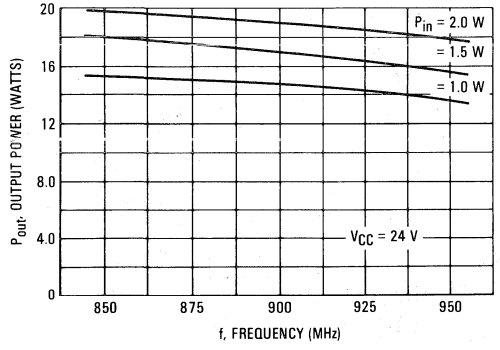


FIGURE 5 — TYPICAL PERFORMANCE IN BROADBAND CIRCUIT

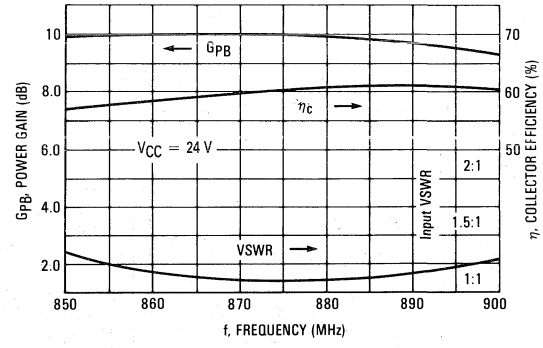
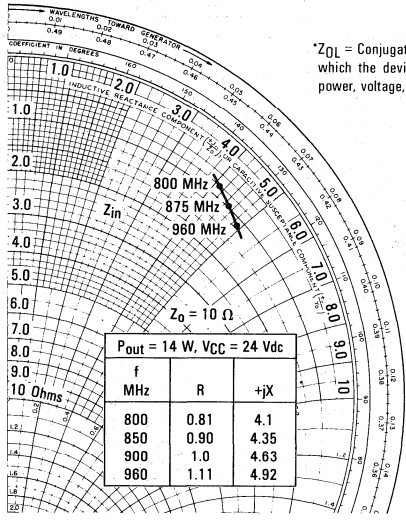


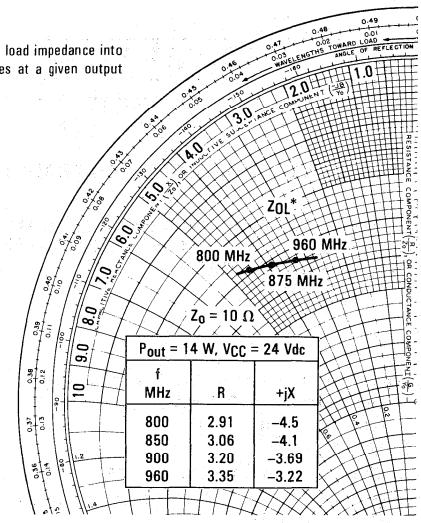
FIGURE 6 — SERIES EQUIVALENT INPUT IMPEDANCE



Pout = 14 W, VCC = 24 Vdc		
f MHz	R	+jX
800	0.81	4.1
850	0.90	4.35
900	1.0	4.63
960	1.11	4.92

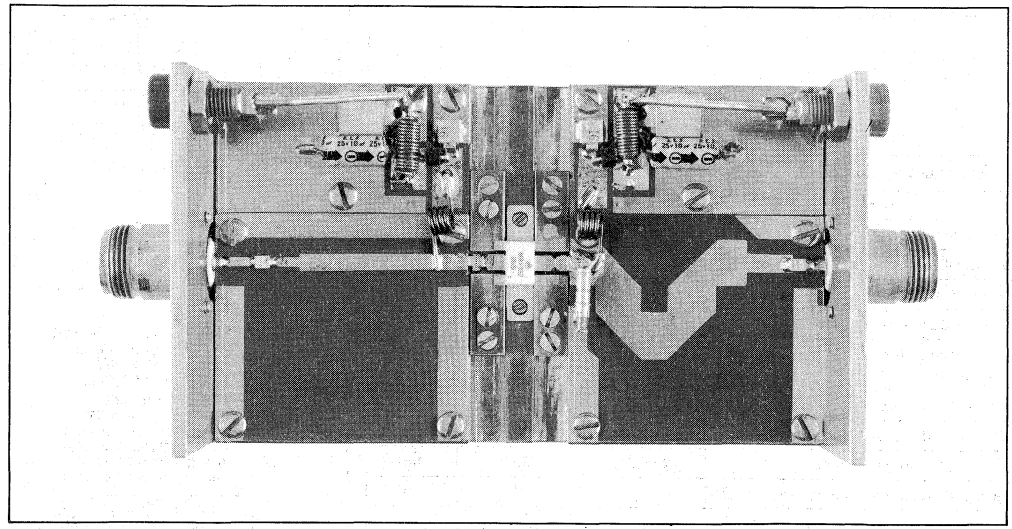
*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

FIGURE 7 — SERIES EQUIVALENT OUTPUT IMPEDANCE



Pout = 14 W, VCC = 24 Vdc		
f MHz	R	+jX
800	2.91	−4.5
850	3.06	−4.1
900	3.20	−3.69
960	3.35	−3.22

FIGURE 8 — 850–900 MHz TEST CIRCUIT



MRF894

The RF Line

30 W 900 MHz

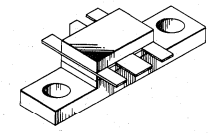
RF POWER TRANSISTOR

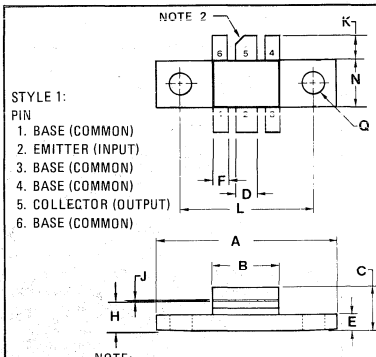
NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed for 24 volt UHF large-signal, common-base amplifier applications in industrial and commercial FM equipment operating in the range of 804 – 960 MHz.

- Specified 24 Volt, 900 MHz Characteristics
  Output Power = 30 Watts
  Minimum Gain = 7.0 dB
  Efficiency = 55%
- Series Equivalent Large-Signal Characterization
- Capable of 30:1 VSWR Load Mismatch at Rated Output Power and Supply Voltage
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Silicon Nitride Passivated





STYLE 1:
PIN
1. BASE (COMMON)
2. EMITTER (INPUT)
3. BASE (COMMON)
4. BASE (COMMON)
5. COLLECTOR (OUTPUT)
6. BASE (COMMON)

NOTE:
1. HOLES WITHIN .15 mm (.006) TRUE POSITION TO EACH OTHER AT MAXIMUM MATERIAL CONDITION.
2. IDENTIFICATION NOTCH 1.0mm (0.04) MIN X 45°.
3. DIM D APPLIES 2 PLACES, DIM K APPLIES 2 PLACES, DIM Q APPLIES 2 PLACES, DIM F APPLIES 4 PLACES.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.51	25.02	0.965	0.985
B	8.76	9.02	0.345	0.355
C	5.84	6.60	0.230	0.260
D	2.92	3.18	0.115	0.125
E	2.69	2.95	0.106	0.116
F	1.91	2.16	0.075	0.085
H	4.06	4.31	0.160	0.170
J	0.10	0.15	0.004	0.006
K	2.29	2.79	0.090	0.110
L	18.42	BSC	0.725	BSC
N	5.72	5.97	0.225	0.235
Q	3.18	3.43	0.125	0.135

CASE 319-04

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	50	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	7.0	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate Above 25°C	P_D	115 0.66	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	1.5	°C/W

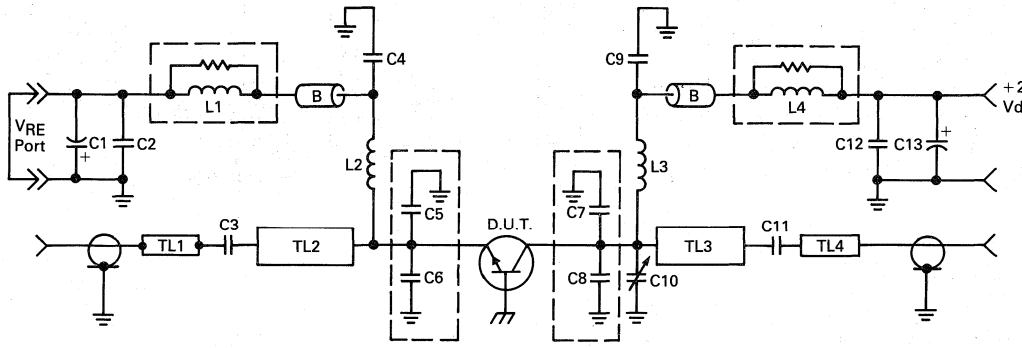
(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 25 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 25 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	50	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	—	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	—	120	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 30 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	45	—	pF
FUNCTIONAL TEST					
Common-Base Amplifier Power Gain (P_{out} = 30 W, V_{CC} = 24 Vdc, f = 900 MHz)	G_{PB}	7.0	8.5	—	dB
Collector Efficiency (P_{out} = 30 W, V_{CC} = 24 Vdc, f = 900 MHz)	η	55	60	—	%

FIGURE 1 — 850–900 MHz BROADBAND CIRCUIT SCHEMATIC



C1, C13 — 5 μF, 50 Vdc
C2, C12 — 1000 pF Unelco
C3, C11 — 47 pF, 100 Mil Chip Capacitor
C4, C9 — 91 pF, Mini-Underwood
C5, C6 — 12 pF, Mini-Underwood
C7 — 18 pF, Mini-Underwood
C8 — 24 pF, Mini-Underwood
C10 — 0.8–8.0 pF Johanson Gigatrim

L1, L4 — 11 Turns #20 Enameled Over 10 Ω Carbon Resistor
L2, L3 — 4 Turns #20 Enameled, .15″ ID
B — Ferrite Bead, Ferroxcube 56-590-65-3B
TL1, TL4 — Micro Strip Line, 50 Ω
TL2 — Micro Strip, Z_O = 30 Ω, λ/4 @ 875 MHz
TL3 — Micro Strip, Z_O = 22 Ω, λ/4 @ 875 MHz
Board — 0.032″ Glass Teflon
2 oz. Cu CLAD, ϵ_r = 2.55

FIGURE 2 — OUTPUT POWER versus INPUT POWER

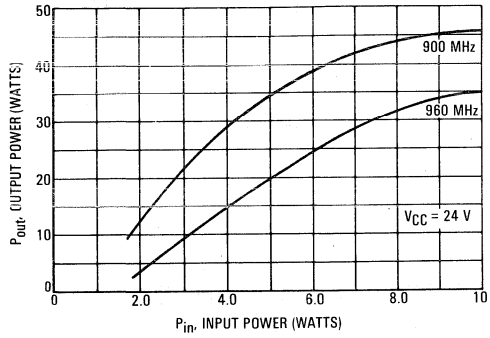


FIGURE 3 — OUTPUT POWER versus FREQUENCY

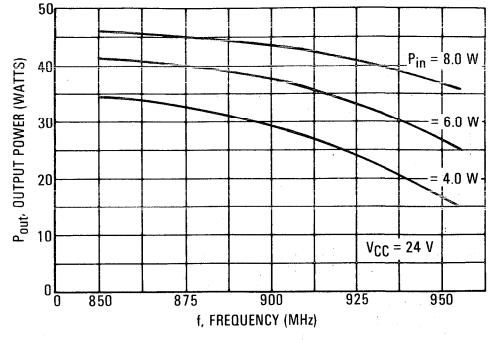


FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE

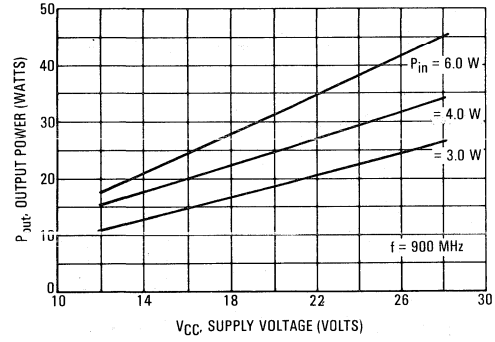


FIGURE 5 — TYPICAL BROADBAND CIRCUIT PERFORMANCE

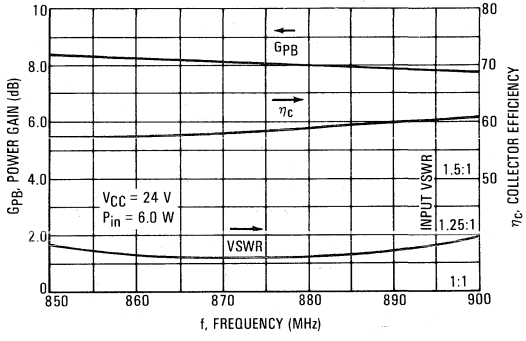
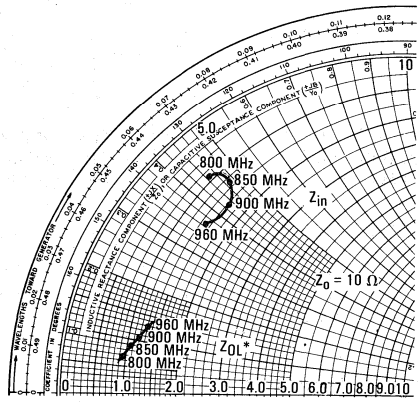


FIGURE 6 — SERIES EQUIVALENT IMPEDANCE

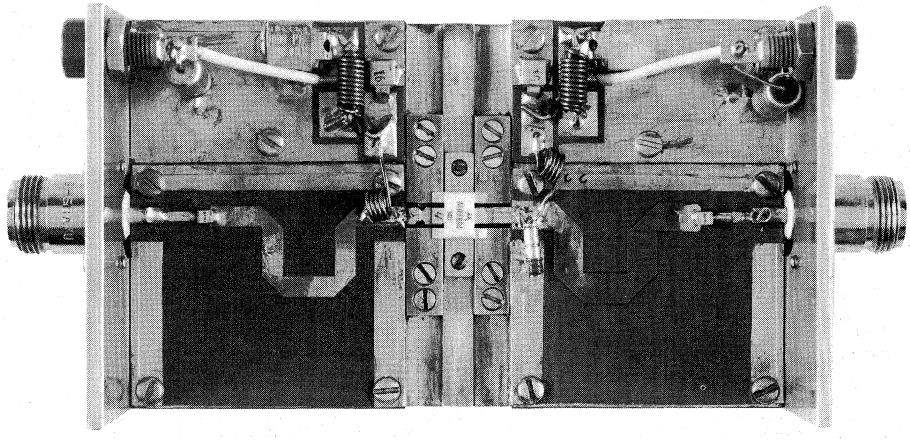


V_{CC} = 24 Vdc, P_{out} = 30 W

f Frequency MHz	Z_{in} Ohms	Z_{OL}* Ohms
800	0.9 + j4.5	1.0 + j0.7
850	1.3 + j4.7	1.1 + j0.9
900	1.6 + j4.4	1.2 + j1.1
960	1.5 + j3.7	1.2 + j1.3

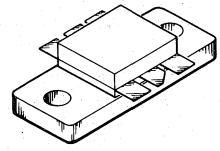
*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

FIGURE 7 — 850-900 MHz BROADBAND CIRCUIT



MRF898

**60 WATTS, 850–960 MHz
RF POWER TRANSISTOR
NPN SILICON**



CASE 333A-01

The RF Line

NPN Silicon RF Power Transistor

. . . designed for 24 Volt UHF large-signal, common base amplifier applications in industrial and commercial FM equipment operating in the range 850–960 MHz.

- Motorola Advanced Amplifier Concept Package
- Specified 24 Volt, 900 MHz Characteristics
  - Output Power = 60 Watts
  - Minimum Gain = 7 dB
  - Efficiency = 60%
- Double Input/Output Matched for Wideband Performance and Simplified External Matching
- Series Equivalent Large-Signal Characterization
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Silicon Nitride Passivated

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	55	Vdc
Emitter-Base Voltage	V_{EBO}	4	Vdc
Collector-Current — Continuous	I_C	10	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	175 1	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

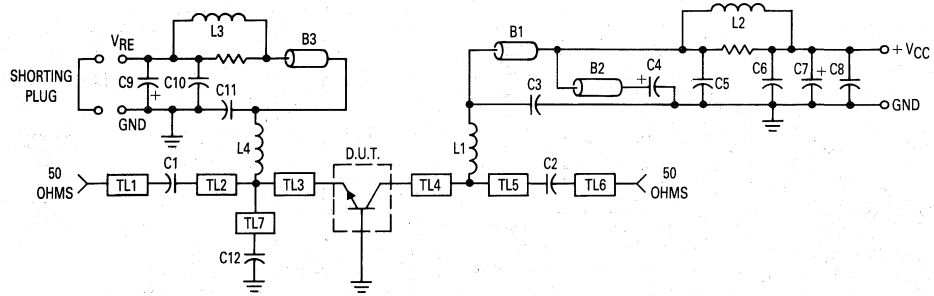
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	30	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	55	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 5 mAdc, I_C = 0)	$V_{(BR)EBO}$	4	—	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	10	mAdc

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (I_C = 2 Adc, V_{CE} = 5 Vdc)	h_{FE}	20	50	150	—
DYNAMIC CHARACTERISTICS					
Output Capacitance* (V_{CB} = 24 Vdc, I_E = 0, f = 1 MHz)	C_{ob}	—	60	—	pF
FUNCTIONAL TESTS					
Common-Base Amplifier Power Gain (V_{CC} = 24 Vdc, P_{out} = 60 W, f = 900 MHz)	G_{pb}	7	7.9	—	dB
Collector Efficiency (V_{CC} = 24 Vdc, P_{out} = 60 W, f = 900 MHz)	η	60	65	—	%
Output Mismatch Stress V_{CC} = 24 V, P_{out} = 60 Watt, f = 900 MHz, VSWR = 5:1 (all phase angles)	ψ	No Degradation in Output Power			

*Value of "C_{ob}" is that of die only. It is not measurable in MRF898 because of internal matching network.



B1, B2, B3 — Bead, Ferroxcube 56-390-65/3B
C1, C2, C12 — 39 pF, 100 Mil Chip Capacitor
C3, C11 — 91 pF, Mini Underwood or Equivalent
C4, C7, C9 — 10 μF, 35 V Electrolytic
C5 — 4000 pF, 1 kV Ceramic
C6, C10 — 1000 pF, 350 V Unelco or Equivalent
C8 — 47 pF, 100 Mil Chip Capacitor
L1, L4 — 4 Turns #18 AWG Choke
L2 — 11 Turns #20 AWG Choke on 10 Ohm, 1 Watt Resistor
L3 — 3 Turns #18 AWG Choke on 10 Ohm, 1 Watt Resistor

Board — 3M Epsilam-10, 50 Mil
TL1, TL6 — 50 Ohm Microstrip
TL2 — 400 x 950 Mils
TL3, TL4 — 140 x 200 Mils
TL5 — 320 x 690 Mils
TL7 — 260 x 230 Mils
Bias Boards — 1/32" G10 or Equivalent

Figure 1. 850–960 MHz Broadband Test Circuit

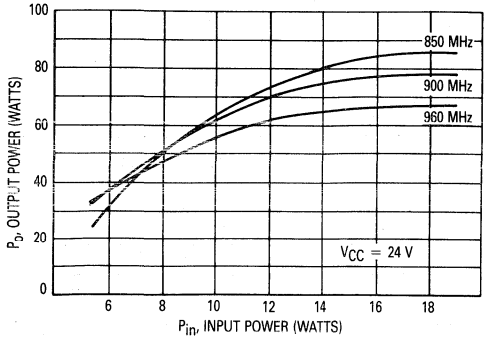


Figure 2. Output Power versus Input Power

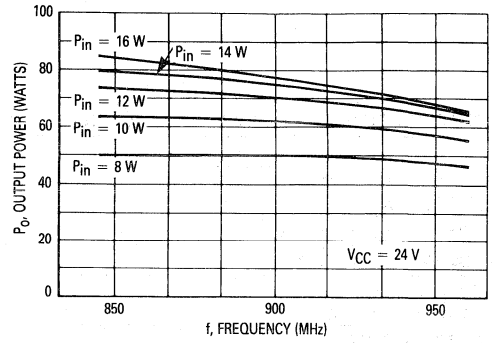


Figure 3. Output Power versus Frequency

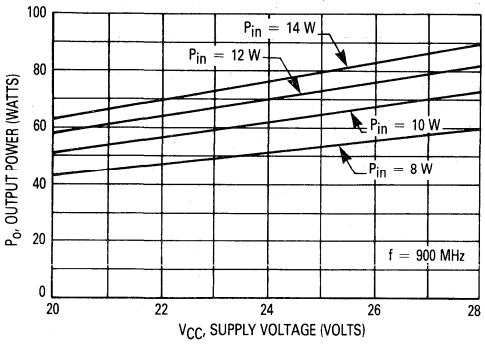


Figure 4. Output Power versus Supply Voltage

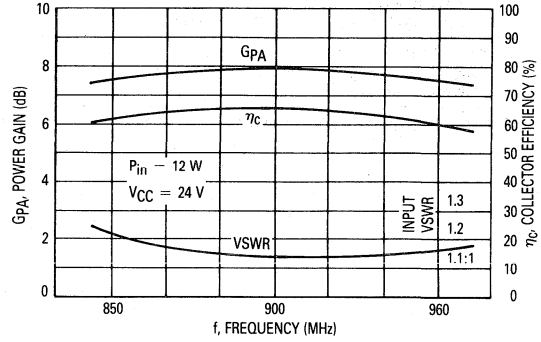
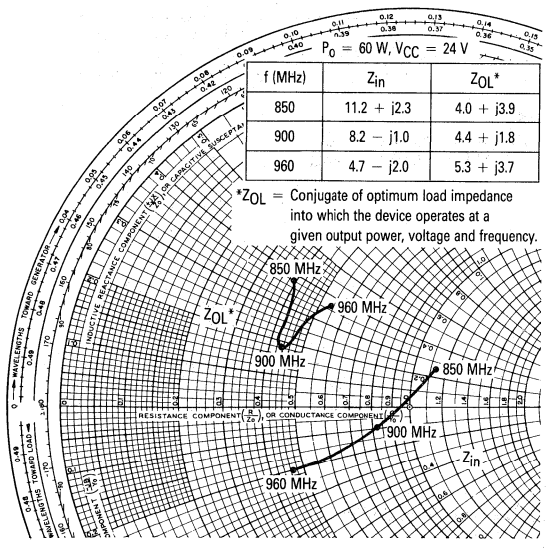


Figure 5. Typical Broadband Circuit Performance

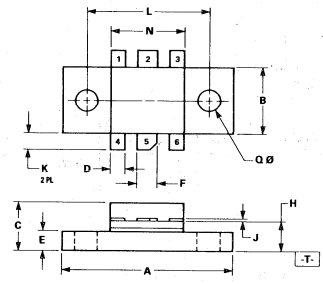


f (MHz)	Z_{in}	Z_{OL}*
850	11.2 + j2.3	4.0 + j3.9
900	8.2 − j1.0	4.4 + j1.8
960	4.7 − j2.0	5.3 + j3.7

*Z_{OL} = Conjugate of optimum load impedance into which the device operates at a given output power, voltage and frequency.

Figure 6. Input/Output Impedance versus Frequency

OUTLINE DIMENSIONS

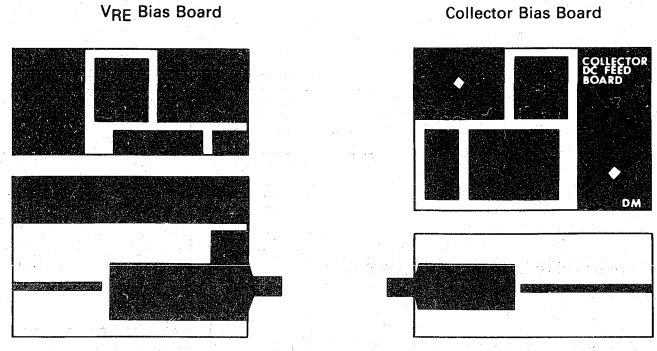


STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. BASE
5. COLLECTOR
6. BASE

NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM PLANE.
2. POSITIONAL TOLERANCE FOR Q HOLES: ⌖ ϕ .13 (0.005) Ⓜ | A Ⓜ | B Ⓜ
3. DIMENSION -D- FOUR PLACES. DIMENSION -F- TWO PLACES.
4. DIMENSIONING AND TOLERANCING PER Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.51	25.02	0.965	0.985
B	9.91	10.41	0.390	0.410
C	6.86	7.36	0.270	0.290
D	1.91	2.28	0.075	0.090
E	2.42	2.92	0.095	0.115
F	5.47	5.96	0.110	0.130
H	3.94	4.44	0.155	0.175
J	0.10	0.15	0.004	0.006
K	2.29	2.94	0.090	0.116
L	18.41 BSC		0.725 BSC	
N	10.54	11.04	0.415	0.435
Q	3.18	3.42	0.125	0.135

CASE 333A-01



NOTE: The Printed Circuit Board shown is 75% of the original.

Figure 7. Photomaster

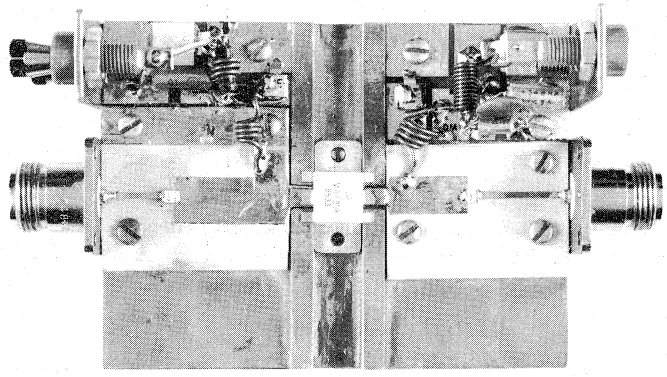


Figure 8. 850–960 Broadband Test Circuit

MRF901

The RF Line

2.5 dB @ 1.0 GHz

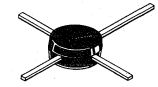
HIGH FREQUENCY TRANSISTOR

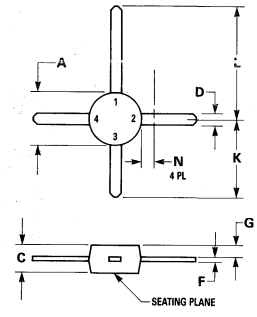
NPN SILICON

NPN SILICON HIGH-FREQUENCY TRANSISTOR

. . . designed primarily for use in high-gain, low-noise small-signal amplifiers. Also usable in applications requiring fast switching times.

- High Current-Gain-Bandwidth Product — f_T = 4.5 GHz (Typ) @ I_C = 15 mAdc
- Low Noise Figure @ f = 1.0 GHz — NF = 2.0 dB (Typ) and 2.5 dB (Max)
- High Power Gain — G_{pe} = 10 dB (Min) @ f = 1.0 GHz
- Third Order Intercept = +23 dBm (Typ)





STYLE 2:
PIN 1. COLLECTOR
2. EMITTER
3. BASE
4. EMITTER

NOTE:
DIMENSION D NOT APPLICABLE IN ZONE N.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.44	5.21	0.175	0.205
C	1.90	2.54	0.075	0.100
D	0.84	0.99	0.033	0.039
F	0.20	0.30	0.008	0.012
G	0.76	1.14	0.030	0.045
K	7.24	8.13	0.285	0.320
L	10.54	11.43	0.415	0.450
N	—	1.65	—	0.065

CASE 317-01

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CBO}	25	Vdc
Emitter-Base Voltage	V_{EBO}	3.0	Vdc
Collector Current — Continuous	I_C	30	mA
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	0.375 3.3	Watt mW/°C
Storage Temperature Range	T_{stg}	150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	300	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	15	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	25	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	2.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	50	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	30	80	200	–
DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwith Product (I_C = 15 mAdc, V_{CE} = 10 Vdc, f = 1.0 GHz)	f_T	–	4.5	–	GHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	–	0.4	1.0	pF
Noise Figure (I_C = 5.0 mAdc, V_{CE} = 6.0 Vdc, f = 1.0 GHz)	NF	–	2.0	2.5	dB
FUNCTIONAL TESTS (Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 6.0 Vdc, I_C = 5.0 mA, f = 1.0 GHz)	G_{pe}	10	12	–	dB
Third Order Intercept (I_C = 5.0 mAdc, V_{CE} = 6.0 Vdc, f = 0.9 GHz)	–	–	+23	–	dBm

FIGURE 1 – 1.0 GHz TEST CIRCUIT SCHEMATIC

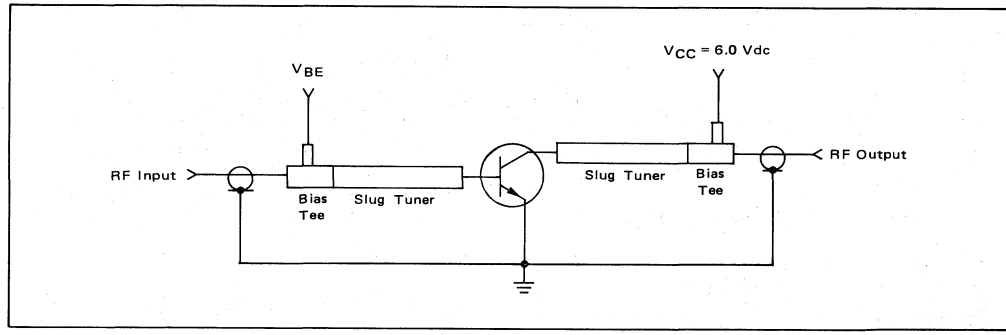


FIGURE 2 — MAXIMUM UNILATERAL GAIN versus FREQUENCY

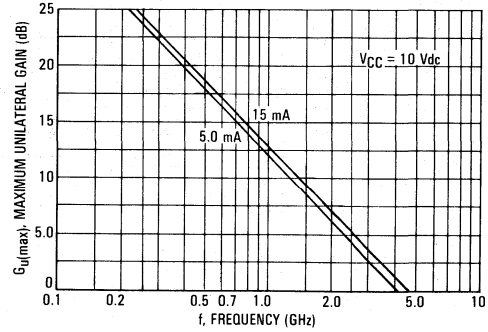


FIGURE 3 — CURRENT GAIN — BANDWIDTH PRODUCT versus COLLECTOR CURRENT

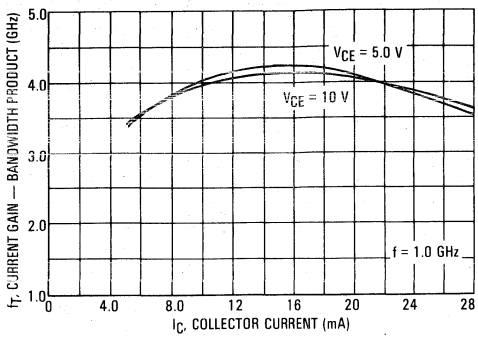


FIGURE 4 — NOISE FIGURE versus FREQUENCY

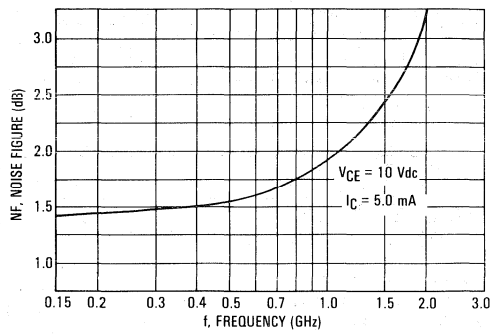


FIGURE 5 — NOISE FIGURE versus COLLECTOR CURRENT

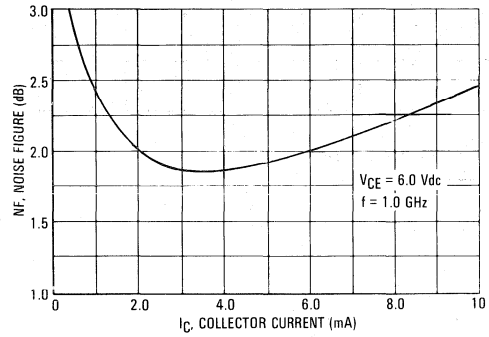


FIGURE 6 — MAXIMUM UNILATERAL GAIN versus COLLECTOR CURRENT

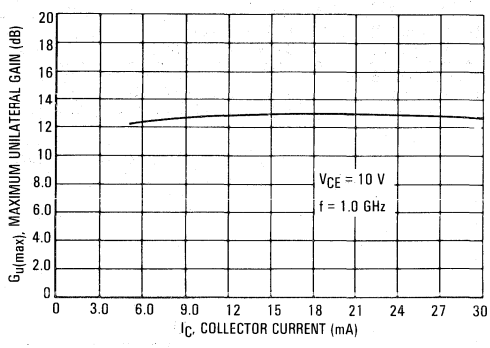


FIGURE 7 — $|S_{21}|^2$ versus FREQUENCY

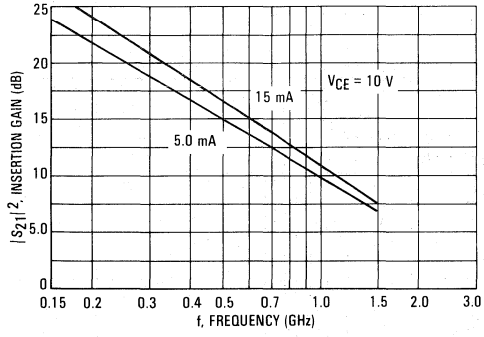


FIGURE 8 — COLLECTOR-BASE CAPACITANCE versus COLLECTOR-BASE VOLTAGE

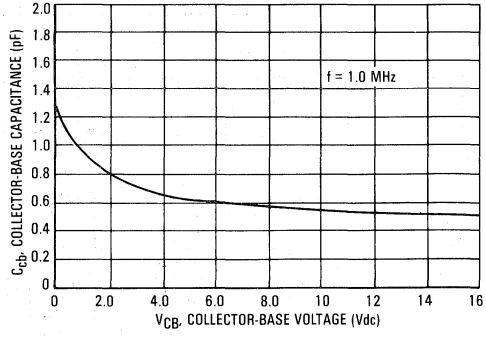


TABLE I

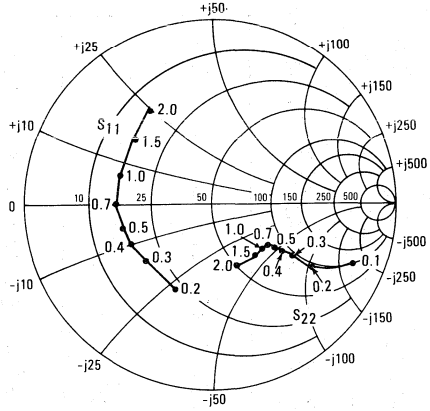
V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
5.0	5.0	100	0.71	-38	11.30	153	0.03	68	0.92	-17
		200	0.62	-75	9.48	133	0.05	55	0.76	-29
		500	0.54	-141	5.40	100	0.07	43	0.48	-44
		1000	0.53	178	2.93	76	0.09	48	0.40	-56
		2000	0.59	130	1.51	48	0.16	62	0.35	-85
	10	100	0.57	-58	16.95	145	0.03	63	0.85	-23
		200	0.51	-103	12.61	123	0.04	53	0.64	-35
		500	0.52	-161	6.24	93	0.06	50	0.38	-45
		1000	0.52	166	3.24	73	0.09	61	0.33	-54
		2000	0.59	125	1.66	47	0.17	67	0.29	-84
	15	100	0.48	-75	20.08	139	0.02	61	0.80	-27
		200	0.47	-121	13.89	117	0.04	53	0.57	-38
		500	0.53	-170	6.44	91	0.05	56	0.34	-44
		1000	0.53	162	3.33	72	0.09	66	0.31	-52
		2000	0.60	123	1.70	46	0.18	68	0.28	-82
	20	100	0.44	-88	21.62	136	0.02	60	0.76	-28
		200	0.47	-132	14.33	114	0.03	54	0.53	-38
		500	0.53	-175	6.45	89	0.05	60	0.32	-41
		1000	0.53	159	3.31	70	0.09	68	0.31	-50
		2000	0.61	122	1.69	45	0.18	70	0.28	-80
	30	100	0.43	-112	21.45	130	0.02	58	0.72	-28
		200	0.50	-148	13.38	109	0.03	57	0.51	-33
		500	0.57	178	5.82	86	0.05	65	0.35	-34
		1000	0.57	156	2.99	68	0.08	73	0.35	-46
		2000	0.65	121	1.50	42	0.18	74	0.33	-78

3

TABLE II

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
10	5.0	100	0.73	-35	11.32	154	0.03	69	0.93	-14
		200	0.63	-69	9.69	135	0.05	57	0.79	-25
		500	0.53	-135	5.65	101	0.07	43	0.54	-38
		1000	0.51	-177	3.11	77	0.08	50	0.47	-48
		2000	0.57	132	1.58	48	0.14	66	0.41	-75
	10	100	0.59	-52	17.06	147	0.02	64	0.87	-19
		200	0.52	-95	13.06	125	0.04	54	0.69	-30
		500	0.49	-156	6.58	95	0.05	51	0.45	-37
		1000	0.50	170	3.44	74	0.08	62	0.41	-45
		2000	0.57	126	1.75	47	0.16	70	0.36	-72
	15	100	0.51	-66	20.36	141	0.02	63	0.83	-22
		200	0.47	-112	14.48	119	0.03	54	0.63	-31
		500	0.50	-166	6.81	92	0.05	57	0.41	-35
		1000	0.50	164	3.54	72	0.08	67	0.39	-43
		2000	0.58	124	1.78	46	0.16	72	0.35	-70
	20	100	0.47	-78	22.08	138	0.02	61	0.80	-23
		200	0.46	-123	15.07	116	0.03	55	0.60	-30
		500	0.50	-171	6.84	90	0.05	60	0.40	-32
		1000	0.51	162	3.51	71	0.08	69	0.39	-41
		2000	0.59	123	1.77	45	0.17	73	0.35	-68
	30	100	0.44	-98	22.70	133	0.02	59	0.76	-23
		200	0.47	-139	14.47	111	0.03	55	0.57	-27
		500	0.53	-177	6.33	87	0.04	65	0.43	-28
		1000	0.54	158	3.26	69	0.07	74	0.43	-39
		2000	0.62	122	1.61	42	0.16	77	0.39	-68

FIGURE 9 — INPUT AND OUTPUT REFLECTION COEFFICIENTS versus FREQUENCY (V_{CE} = 10 V, I_C = 15 mA)



Coordinates in Ohms

FIGURE 10 — FORWARD/REVERSE TRANSMISSION COEFFICIENTS versus FREQUENCY (V_{CE} = 10 V, I_C = 15 mA)

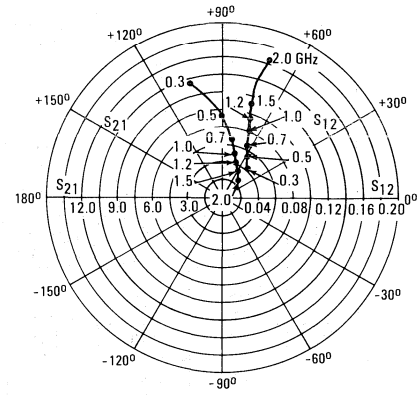
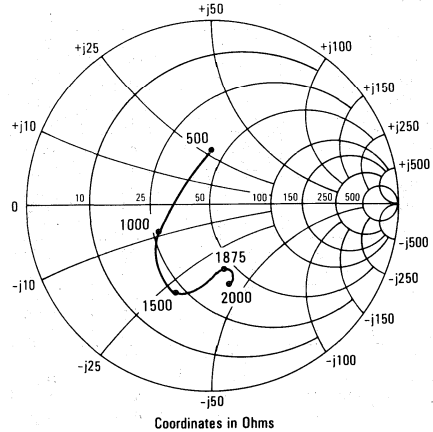
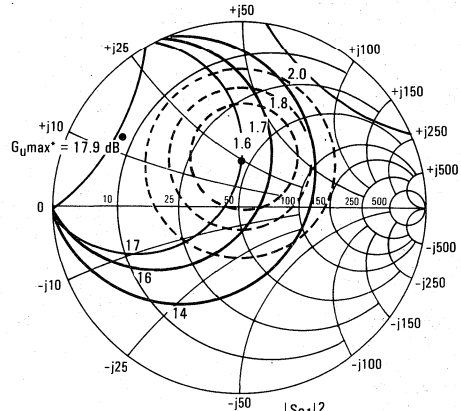


FIGURE 11 — SOURCE IMPEDANCE (Γms) FOR OPTIMUM NOISE FIGURE versus FREQUENCY (V_{CE} = 10 Vdc, I_C = 5.0 mA)



Coordinates in Ohms

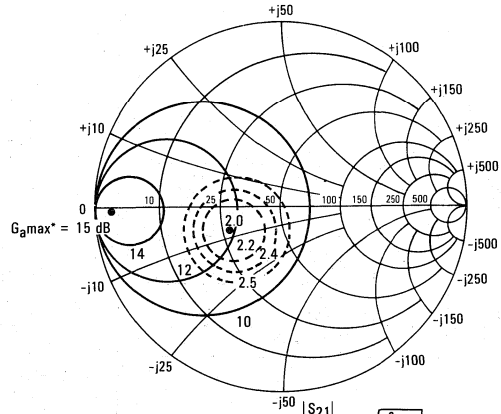
FIGURE 12 — CONSTANT GAIN AND NOISE FIGURE CONTOURS
(V_{CE} = 10 Vdc, I_C = 5.0 mA f = 500 MHz)



*Maximum Unilateral Gain, $G_u max = \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)}$, (K < 1)

3

FIGURE 13 — CONSTANT GAIN AND NOISE FIGURE CONTOURS
(V_{CE} = 10 Vdc, I_C = 5.0 mA f = 1.0 GHz)



*Maximum Available Gain, $G_a max = \frac{|S_{21}|}{|S_{12}|}(K \pm \sqrt{K^2-1})$ (K > 1)

MRF904

The RF Line

NPN SILICON HIGH-FREQUENCY TRANSISTORS

. . . designed for use as low-noise, high-gain, general purpose amplifiers.

- High Current-Gain — Bandwidth Product —
  f_T = 4.0 GHz (Typ) @ I_C = 15 mAdc
- Low Noise Figure —
  NF = 1.5 dB (Typ) @ f = 450 MHz
  = 2.5 dB (Typ) @ f = 1.0 GHz
- High Power Gain —
  G_{max} = 16 dB (Typ) @ f = 450 MHz
  = 10 dB (Typ) @ f = 1.0 GHz
- Excellent Third Order Intercept — +25 dBm (Typ)

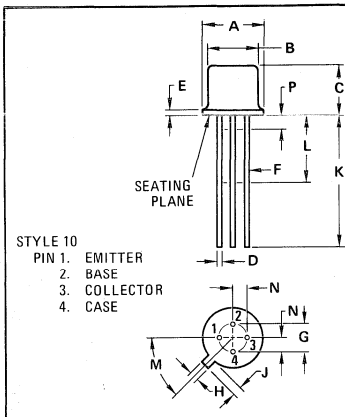
HIGH FREQUENCY
TRANSISTORS
NPN SILICON



3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CBO}	25	Vdc
Emitter-Base Voltage	V_{EBO}	3.0	Vdc
Collector Current — Continuous	I_C	30	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	0.2 1.14	Watt mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C



STYLE 10
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. CASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply

CASE 20-03
TO-72

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	15	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	25	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	50	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	30	–	200	–
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 15 mAdc, V_{CE} = 10 Vdc, f = 1.0 GHz)	f_T	–	4.0	–	GHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	–	–	1.0	pF
Noise Figure	NF				dB
(I_C = 5.0 mAdc, V_{CE} = 6.0 Vdc, f = 450 MHz)		–	1.5	–	
(I_C = 5.0 mAdc, V_{CE} = 6.0 Vdc, f = 1.0 GHz)		–	2.5	–	
FUNCTIONAL TEST					
Unilateralized Gain (1)	G_{max}				dB
(I_C = 5.0 mAdc, V_{CE} = 6.0 Vdc, f = 450 MHz)		–	16	–	
(I_C = 5.0 mAdc, V_{CE} = 6.0 Vdc, f = 1.0 GHz)		–	10	–	

(1) $G_{max} = \dfrac{|s_{21}|^2}{(1-|s_{11}|^2)(1-|s_{22}|^2)}$

3

FIGURE 1 – NOISE FIGURE versus FREQUENCY

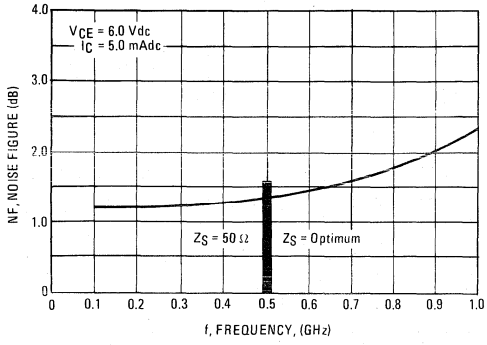


FIGURE 2 – NOISE FIGURE versus COLLECTOR CURRENT

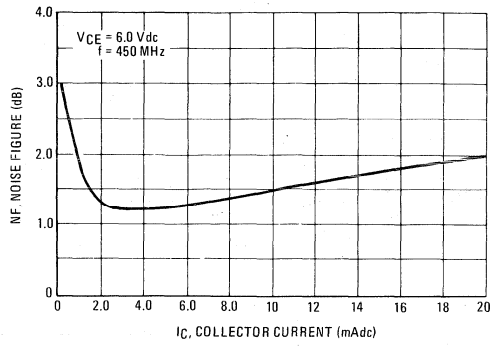


FIGURE 3 – COLLECTOR-BASE CAPACITANCE versus COLLECTOR-BASE VOLTAGE

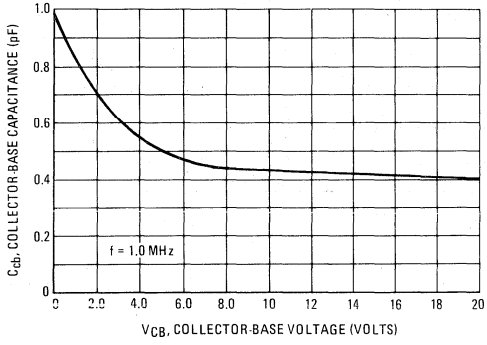


FIGURE 4 – UNILATERALIZED GAIN (G_{max}) versus FREQUENCY

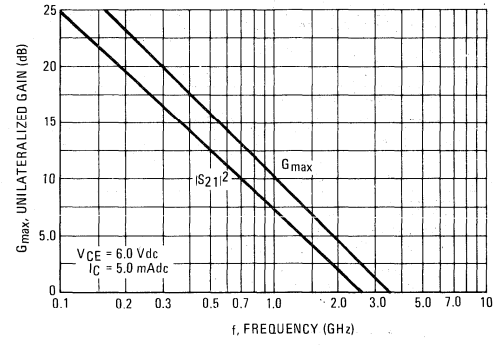


FIGURE 5 – CURRENT-GAIN – BANDWIDTH PRODUCT versus COLLECTOR CURRENT

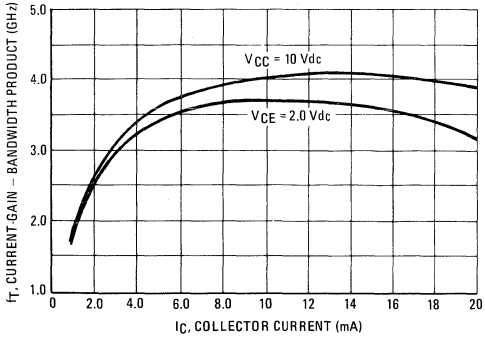


FIGURE 6 – INTERMODULATION DISTORTION versus COLLECTOR CURRENT

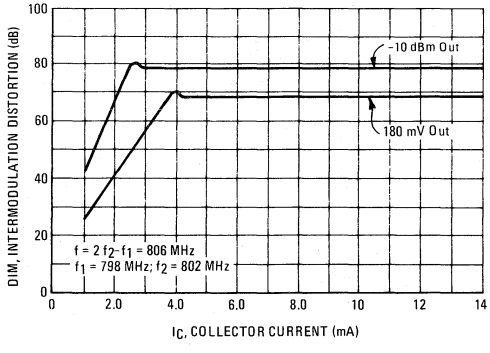


TABLE 1 – S_{11} PARAMETERS

Frequency (MHz)		100		200		500		800		1000	
V_{CC} (Volts)	I_C (mA)	S11	∠ϕ	S11	∠ϕ	S11	∠ϕ	S11	∠ϕ	S11	∠ϕ
1.0	1.0	0.941	-22	0.85	-43	0.57	-91	0.37	-128	0.30	-151
	2.5	0.85	-31	0.67	-57	0.35	-102	0.20	-136	0.14	-157
	5.0	0.69	-44	0.46	-71	0.21	-109	0.10	-144	0.069	-166
	10	0.45	-67	0.28	-94	0.13	-136	0.087	172	0.075	145
	15	0.37	-110	0.31	-145	0.26	170	0.27	139	0.27	122
	30	0.71	-178	0.71	169	0.68	144	0.68	121	0.65	107
3.0	1.0	0.94	-19	0.87	-37	0.61	-80	0.39	-114	0.30	-134
	2.5	0.87	-26	0.71	-47	0.39	-84	0.21	-106	0.15	-115
	5.0	0.74	-34	0.52	-55	0.25	-77	0.13	-82	0.109	-79
	10	0.55	-42	0.35	-58	0.18	-66	0.11	-60	0.105	-55
	15	0.46	-46	0.28	-59	0.15	-64	0.096	-55	0.092	-49
	30	0.28	-95	0.21	-134	0.16	175	0.17	135	0.17	116
6.0	1.0	0.95	-18	0.88	-35	0.63	-76	0.40	-108	0.30	-126
	2.5	0.89	-23	0.74	-43	0.42	-77	0.23	-94	0.17	-100
	5.0	0.77	-31	0.56	-49	0.29	-67	0.18	-69	0.15	-66
	10	0.61	-37	0.40	-50	0.23	-55	0.16	-51	0.16	-50
	15	0.52	-40	0.34	-51	0.20	-52	0.15	-47	0.15	-47
	30	0.36	-55	0.21	-70	0.098	-77	0.037	-59	0.033	-27
10	1.0	0.96	-17	0.89	-33	0.65	-73	0.41	-103	0.31	-121
	2.5	0.89	-22	0.76	-41	0.44	-73	0.25	-88	0.18	-93
	5.0	0.79	-28	0.59	-46	0.32	-63	0.20	-65	0.18	-63
	10	0.64	-34	0.44	-47	0.26	-52	0.19	-49	0.18	-49
	15	0.57	-37	0.38	-48	0.23	-49	0.18	-46	0.17	-46
	30	0.41	-51	0.24	-64	0.12	-67	0.061	-52	0.055	-36

TABLE 2 – S_{21} PARAMETERS

Frequency (MHz)		100		200		500		800		1000	
V_{CC} (Volts)	I_C (mA)	S21	∠ϕ	S21	∠ϕ	S21	∠ϕ	S21	∠ϕ	S21	∠ϕ
1.0	1.0	5.32	156	3.06	137	2.22	97	1.65	70	1.44	56
	2.5	6.79	146	5.57	124	3.15	86	2.14	64	1.81	52
	5.0	10.97	133	7.60	110	3.62	79	2.38	61	2.00	49
	10	13.16	118	8.07	99	3.60	74	2.35	57	1.96	46
	15	9.84	108	5.66	91	2.44	67	1.63	49	1.38	38
	30	1.65	83	0.88	69	0.47	46	0.43	37	0.45	31
3.0	1.0	3.33	159	3.11	142	2.36	103	1.79	76	1.55	62
	2.5	6.89	150	5.85	129	3.48	92	2.38	70	2.00	58
	5.0	11.49	138	8.34	115	4.12	84	2.70	66	2.25	55
	10	15.71	125	9.82	104	4.39	79	2.85	63	2.34	53
	15	16.97	119	10.05	100	4.39	77	2.83	61	2.34	52
	30	12.66	108	7.02	92	2.98	70	1.94	54	1.61	44
6.0	1.0	3.31	160	3.10	144	2.41	106	1.83	79	1.60	65
	2.5	6.80	151	5.85	131	3.60	94	2.46	77	2.07	60
	5.0	11.44	140	8.54	117	4.28	86	2.83	68	2.33	57
	10	15.85	127	10.14	107	4.61	81	2.96	65	2.46	55
	15	17.20	122	10.47	102	4.60	79	2.96	63	2.45	54
	30	16.37	113	9.38	96	4.00	75	2.58	59	2.14	49
10	1.0	3.25	160	3.08	145	2.40	108	1.83	81	1.61	67
	2.5	6.73	152	5.85	132	3.63	96	2.50	74	2.10	62
	5.0	11.19	142	8.49	119	4.34	88	2.85	69	2.37	59
	10	15.59	129	10.16	108	4.66	82	3.00	66	2.47	56
	15	17.04	124	10.49	104	4.65	80	2.99	64	2.47	55
	30	16.18	115	9.38	98	4.03	96	2.60	60	2.14	50

TABLE 3 – S_{12} PARAMETERS

Frequency (MHz)		100		200		500		800		1000	
V_{CC} (Volts)	I_C (mA)	S12	∠ϕ	S12	∠ϕ	S12	∠ϕ	S12	∠ϕ	S12	∠ϕ
1.0	1.0	0.054	73	0.097	61	0.159	41	0.184	36	0.194	37
	2.5	0.051	69	0.084	58	0.140	50	0.189	48	0.220	46
	5.0	0.046	65	0.072	60	0.137	58	0.201	53	0.239	50
	10	0.041	64	0.067	64	0.142	62	0.215	56	0.256	51
	15	0.043	61	0.070	63	0.152	62	0.230	55	0.277	50
	30	0.058	50	0.093	58	0.209	57	0.311	46	0.372	39
3.0	1.0	0.039	75	0.072	65	0.123	46	0.143	42	0.151	44
	2.5	0.037	72	0.063	62	0.110	54	0.150	53	0.174	52
	5.0	0.033	70	0.055	64	0.108	62	0.160	58	0.190	55
	10	0.030	70	0.050	68	0.109	67	0.165	61	0.199	57
	15	0.028	70	0.049	70	0.109	68	0.167	62	0.200	57
	30	0.026	68	0.046	70	0.105	69	0.165	64	0.200	61
6.0	1.0	0.032	76	0.060	66	0.106	49	0.123	45	0.131	48
	2.5	0.031	73	0.054	64	0.095	57	0.130	56	0.151	55
	5.0	0.028	71	0.048	66	0.094	64	0.139	61	0.165	58
	10	0.026	71	0.043	69	0.094	68	0.144	63	0.172	59
	15	0.024	71	0.042	71	0.093	69	0.144	64	0.172	60
	30	0.021	71	0.037	72	0.086	71	0.134	67	0.162	63
10	1.0	0.028	77	0.053	68	0.095	50	0.109	47	0.116	50
	2.5	0.027	74	0.048	65	0.085	58	0.116	57	0.134	57
	5.0	0.025	73	0.043	67	0.084	64	0.125	62	0.148	60
	10	0.023	72	0.037	69	0.084	69	0.128	64	0.153	61
	15	0.022	73	0.037	70	0.084	69	0.128	65	0.152	62
	30	0.019	72	0.033	72	0.076	72	0.119	68	0.143	66

3

TABLE 4 – S_{22} PARAMETERS

Frequency (MHz)		100		200		500		800		1000	
V_{CC} (Volts)	I_C (mA)	S22	∠ϕ	S22	∠ϕ	S22	∠ϕ	S22	∠ϕ	S22	∠ϕ
1.0	1.0	0.966	-12	0.893	-23	0.693	-41	0.612	-53	0.594	-59
	2.5	0.901	-18	0.760	-29	0.548	-42	0.498	-51	0.494	-56
	5.0	0.793	-24	0.619	-32	0.456	-39	0.429	-49	0.439	-54
	10	0.635	-29	0.486	-32	0.390	-36	0.377	-47	0.389	-53
	15	0.453	-29	0.364	-29	0.313	-34	0.309	-48	0.321	-14
	30	0.048	-78	0.035	-88	0.032	-135	0.031	-162	0.007	-167
3.0	1.0	0.976	-9.0	0.926	-18	0.770	-35	0.702	-46	0.683	-51
	2.5	0.935	-13	0.828	-23	0.648	-35	0.608	-43	0.608	-48
	5.0	0.853	-18	0.712	-25	0.577	-32	0.555	-41	0.565	-46
	10	0.758	-20	0.629	-23	0.539	-29	0.529	-39	0.544	-44
	15	0.711	-20	0.601	-22	0.533	-27	0.526	-38	0.540	-44
	30	0.631	-15	0.576	-16	0.548	-25	0.546	-38	0.558	-45
6.0	1.0	0.982	-8.0	0.939	-16	0.803	-31	0.742	42	0.734	-47
	2.5	0.947	-11	0.861	-20	0.699	-31	0.662	-40	0.660	-45
	5.0	0.882	-15	0.759	-21	0.633	-29	0.617	-31	0.627	-43
	10	0.801	-17	0.684	-20	0.607	-26	0.601	-35	0.610	-41
	15	0.769	-17	0.667	-19	0.602	-25	0.601	-35	0.607	-40
	30	0.737	-14	0.672	-15	0.640	-22	0.641	-33	0.655	-40
10	1.0	0.983	-7.0	0.949	-14	0.830	-29	0.774	-39	0.765	-40
	2.5	0.954	-10	0.880	-18	0.733	-29	0.698	-37	0.702	-42
	5.0	0.901	-13	0.793	-19	0.676	-27	0.659	-35	0.668	-41
	10	0.834	-15	0.725	-18	0.646	-24	0.646	-33	0.658	-39
	15	0.802	-15	0.706	-17	0.645	-23	0.648	-33	0.661	-39
	30	0.776	-13	0.712	-14	0.678	-22	0.686	-32	0.699	-38

MRF905

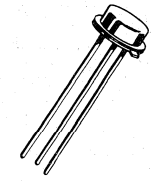
The RF Line

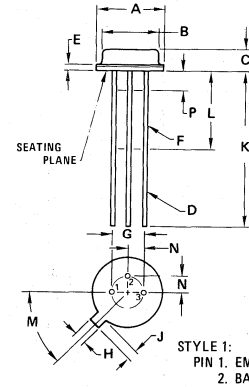
400 mW
RF OSCILLATOR TRANSISTOR
NPN SILICON

NPN SILICON OSCILLATOR TRANSISTOR

. . . designed for microwave communications relay links and low-cost radiosonde service.

- Emitter Ballasted
- Low Current Density for Improved Lifetime
- Collector Connected to Case





STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	1.65	2.16	0.065	0.085
D	0.406	0.533	0.016	0.021
E	–	1.02	–	0.040
F	0.305	0.483	0.012	0.019
G	2.54 BSC		0.100 BSC	
H	0.914	1.17	0.036	0.046
J	0.711	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

All JEDEC dimensions and notes apply

CASE 26-03
TO-46

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CBO}	35	Vdc
Emitter-Base Voltage	V_{EBO}	3.5	Vdc
Collector Current — Continuous	I_C	150	mAdc
Total Power Dissipation @ T_C = 100°C Derate above 100°C	P_D	.75 7.5	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

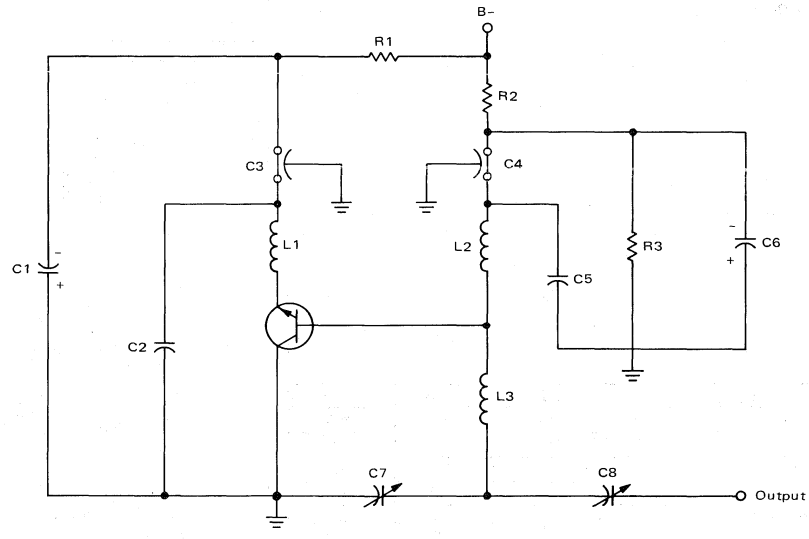
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	133	°C/W

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	30	–	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	35	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	5.0	–	Vdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)	I_{CBO}	–	–	0.1	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 10 Vdc)	h_{FE}	20	60	150	–
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 200 MHz)	f_T	–	2500	–	MHz
Output Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	3.0	5.0	pF
FUNCTIONAL TEST					
Common-Collector Oscillator Output Power (V_E = -20 Vdc, $I_E \cong$ 110 mAdc, f ≅ 1.68 GHz)	P_{out}	400	500	–	mW

FIGURE 1 – 1.68 GHz OSCILLATOR TEST CIRCUIT SCHEMATIC



C1,C6	1.0 μF, 35 Vdc TANTALUM	R1	47 Ohms, 1/4 Watt
C2,C5	0.1 μF Ceramic Disk	R2	510 Ohms, 1/4 Watt
C3,C4	680 pF Feedthru	R3	1.5 kΩ, 1/4 Watt
C7,C8	0.4-6.0 pF JOHANSON	L1,L2	5 Turns, #22 AWG, 0.125" I.D.
		L3	#20 AWG, 0.4" Length.

MRF911

The RF Line

f_T = 5.0 GHz @ 30 mA

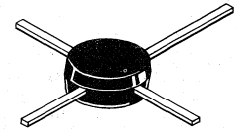
HIGH FREQUENCY TRANSISTOR

NPN SILICON

NPN SILICON HIGH FREQUENCY TRANSISTOR

. . . designed primarily for use in high-gain, low-noise tuned and wideband small-signal amplifiers. Excellent in high-speed switching applications.

- High Current-Gain — Bandwidth Product — f_T = 5.0 GHz (Typ) @ f = 1.0 GHz
- High Power Gain — G_{max} = 12.5 dB (Typ) @ f = 1.0 GHz



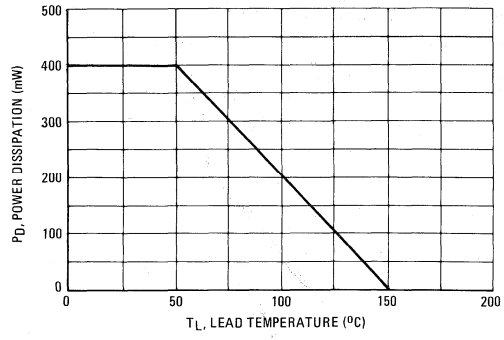
MAXIMUM RATINGS

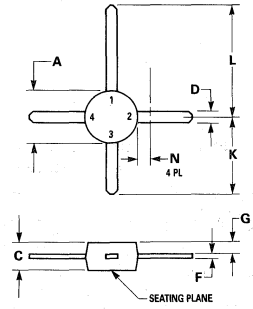
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	12	Vdc
Collector-Base Voltage	V_{CBO}	20	Vdc
Emitter-Base Voltage	V_{EBO}	3.0	Vdc
Collector Current — Peak	I_C	40	mAdc
Total Device Dissipation @ T_L = 50°C Derate Above 50°C	P_D	400 4.0	mW mW/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Lead	$R_{\theta JL}$	250	°C/W

FIGURE 1 — POWER DERATING





STYLE 2:
PIN 1. COLLECTOR
2. EMITTER
3. BASE
4. EMITTER

NOTE:
DIMENSION D NOT APPLICABLE IN ZONE N.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.44	5.21	0.175	0.205
C	1.90	2.54	0.075	0.100
D	0.84	0.99	0.033	0.039
F	0.20	0.30	0.008	0.012
G	0.76	1.14	0.030	0.045
K	7.24	8.13	0.285	0.320
L	10.54	11.43	0.415	0.450
N	—	1.65	—	0.065

CASE 317-01

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	12	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	20	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	50	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 30 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	–	200	–
DYNAMIC CHARACTERISTICS					
Current-Gain Bandwidth Product (I_C = 30 mAdc, V_{CE} = 10 Vdc, f = 1.0 GHz)	f_T	–	5.0	–	GHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	–	0.6	1.0	pF
FUNCTIONAL TESTS					
Noise Figure	NF				dB
(I_C = 5.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 GHz)		–	2.5	–	
(I_C = 5.0 mAdc, V_{CE} = 10 Vdc, f = 2.0 GHz)		–	4.0	–	
Power Gain at Optimum Noise Figure	G_{NF}				dB
(I_C = 5.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 GHz)		–	10	–	
(I_C = 5.0 mAdc, V_{CE} = 10 Vdc, f = 2.0 GHz)		–	6.0	–	
Maximum Available Power Gain (1)	G_{max}				dB
(I_C = 30 mAdc, V_{CE} = 10 Vdc, f = 1.0 GHz)		–	12.5	–	
(I_C = 30 mAdc, V_{CE} = 10 Vdc, f = 2.0 GHz)		–	7.5	–	

(1) $G_{max} = \frac{|S_{21}|^2}{((1-|S_{11}|^2)(1-|S_{22}|^2)}$

FIGURE 2 – POWER GAIN AND NOISE FIGURE versus FREQUENCY

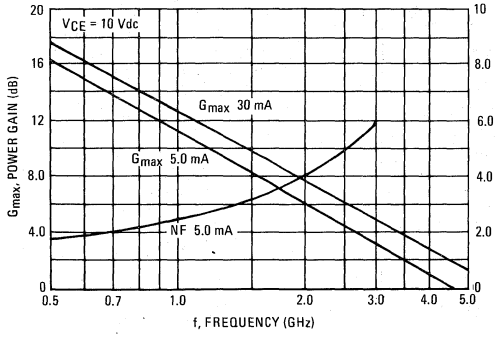


FIGURE 3 – POWER GAIN AND NOISE FIGURE versus COLLECTOR CURRENT

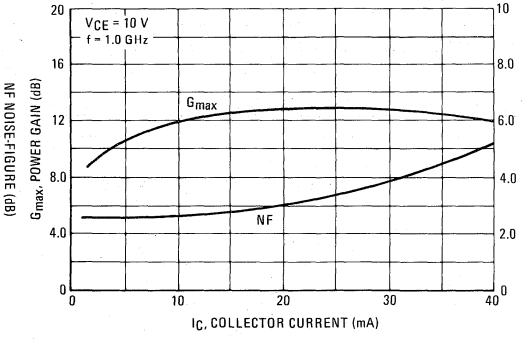


FIGURE 4 – S_{11} PARAMETERS

Frequency (MHz)		500		1000		1500		2000	
V_{CE} (Volts)	I_C (mA)	S_{11}	∠φ	S_{11}	∠φ	S_{11}	∠φ	S_{11}	∠φ
5.0	2.0	0.66	-125	0.64	-175	0.68	160	0.73	140
	5.0	0.57	-150	0.58	170	0.62	150	0.66	135
	10	0.54	-165	0.57	160	0.60	145	0.64	130
	20	0.54	-180	0.57	155	0.60	140	0.64	125
	30	0.54	175	0.57	155	0.61	140	0.65	125
10	2.0	0.66	-120	0.63	-170	0.67	160	0.71	140
	5.0	0.56	-145	0.56	175	0.60	150	0.64	135
	10	0.51	-160	0.53	165	0.57	145	0.61	130
	20	0.49	-175	0.52	160	0.57	145	0.60	130
	30	0.49	-175	0.53	160	0.57	145	0.61	130

FIGURE 5 – S_{22} PARAMETERS

Frequency (MHz)		500		1000		1500		2000	
V_{CE} (Volts)	I_C (mA)	S_{22}	∠φ	S_{22}	∠φ	S_{22}	∠φ	S_{22}	∠φ
5.0	2.0	0.61	-45	0.50	-60	0.48	-80	0.50	-100
	5.0	0.40	-55	0.31	-65	0.30	-85	0.32	-100
	10	0.27	-60	0.20	-70	0.20	-90	0.23	-105
	20	0.19	-70	0.13	-75	0.14	-95	0.17	-110
	30	0.16	-70	0.11	-75	0.13	-95	0.16	-110
10	2.0	0.66	-35	0.55	-50	0.53	-70	0.54	-90
	5.0	0.47	-45	0.38	-50	0.37	-70	0.38	-75
	10	0.35	-45	0.28	-50	0.27	-65	0.29	-85
	20	0.26	-45	0.22	-50	0.22	-65	0.24	-80
	30	0.25	-40	0.21	-45	0.22	-60	0.24	-80

FIGURE 6 – S_{21} PARAMETERS

Frequency (MHz)		500		1000		1500		2000	
V_{CE} (Volts)	I_C (mA)	S_{21}	∠φ	S_{21}	∠φ	S_{21}	∠φ	S_{21}	∠φ
5.0	2.0	3.24	100	1.84	70	1.23	50	0.96	35
	5.0	4.85	90	2.60	70	1.76	50	1.38	40
	10	5.78	85	3.04	70	2.05	50	1.61	40
	20	6.40	85	3.30	65	2.23	50	1.24	40
	30	6.47	80	3.35	65	2.26	50	1.76	40
10	2.0	3.42	100	1.95	70	1.31	50	1.01	35
	5.0	5.20	95	2.80	70	1.89	50	1.45	40
	10	6.22	90	3.28	70	2.20	55	1.71	40
	20	6.82	85	3.55	65	2.37	55	1.84	40
	30	6.90	85	3.55	65	2.36	50	1.81	40

FIGURE 7 – S_{12} PARAMETERS

Frequency (MHz)		500		1000		1500		2000	
V_{CE} (Volts)	I_C (mA)	S_{12}	∠φ	S_{12}	∠φ	S_{12}	∠φ	S_{12}	∠φ
5.0	2.0	0.11	30	0.12	25	0.11	35	0.13	50
	5.0	0.08	40	0.10	45	0.13	55	0.17	55
	10	0.07	50	0.10	55	0.14	60	0.19	60
	20	0.06	60	0.11	65	0.15	65	0.20	60
	30	0.06	65	0.11	65	0.15	65	0.20	60
10	2.0	0.10	35	0.10	30	0.10	40	0.12	55
	5.0	0.07	40	0.09	45	0.12	55	0.15	60
	10	0.06	50	0.09	55	0.13	60	0.17	60
	20	0.06	60	0.10	65	0.13	65	0.18	60
	30	0.06	60	0.10	65	0.14	65	0.18	65

MRF914

The RF Line

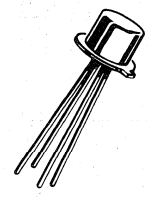
f_T = 4.5 GHz @ 20 mA

HIGH FREQUENCY TRANSISTOR
NPN SILICON

NPN SILICON HIGH FREQUENCY TRANSISTOR

. . . designed for applications requiring high-gain, low-noise and low distortion. Also excellent for high speed switching applications.

- Low Noise Figure –
  NF = 2.0 dB (Typ) @ f = 0.5 GHz
  = 2.5 dB (Typ) @ f = 1.0 GHz
- High Power Gain –
  G_{max} = 15 dB (Typ) @ f = 0.5 GHz
  = 10 dB (Typ) @ f = 1.0 GHz



3

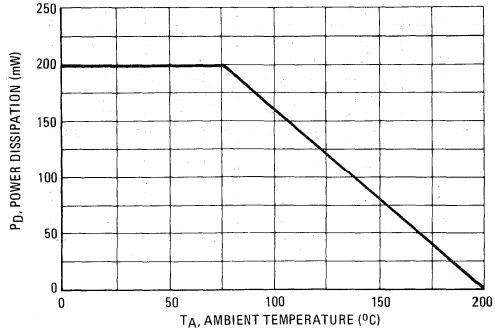
MAXIMUM RATINGS

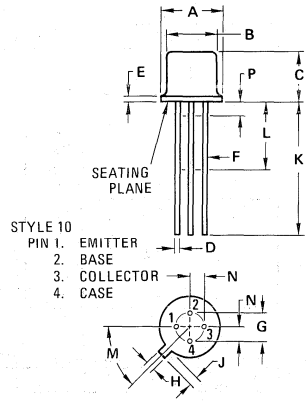
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	12	Vdc
Collector-Base Voltage	V_{CBO}	20	Vdc
Emitter-Base Voltage	V_{EBO}	3.0	Vdc
Collector Current — Peak	I_C	40	mAdc
Total Device Dissipation @ T_A = 75°C Derate Above 75°C	P_D	200 1.6	mW mW/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	625	°C/W

FIGURE 1 – POWER DERATING





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.53	0.016	0.021
E	–	0.76	–	0.030
F	0.41	0.48	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

ALL JEDEC dimensions and notes apply
CASE 20-03
TO-72

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	12	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	20	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	–	–	50	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 20 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	–	200	–
DYNAMIC CHARACTERISTICS					
Current-Gain Bandwidth Product (I_C = 20 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz)	f_T	–	4.5	–	GHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	–	0.7	1.0	pF
FUNCTIONAL TESTS					
Noise Figure	NF				dB
(I_C = 5.0 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz)		–	2.0	–	
(I_C = 5.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 GHz)		–	2.5	–	
Power Gain at Optimum Noise Figure	G_{NF}				dB
(I_C = 5.0 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz)		–	12	–	
(I_C = 5.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 GHz)		–	7.0	–	
Maximum Available Power Gain (1)	G_{max}				dB
(I_C = 20 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz)		–	15	–	
(I_C = 20 mAdc, V_{CE} = 10 Vdc, f = 1.0 GHz)		–	10	–	

(1) $G_{max} = \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)}$

FIGURE 2 – POWER GAIN AND NOISE FIGURE versus FREQUENCY

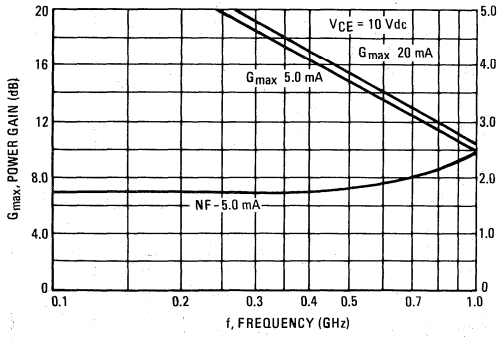
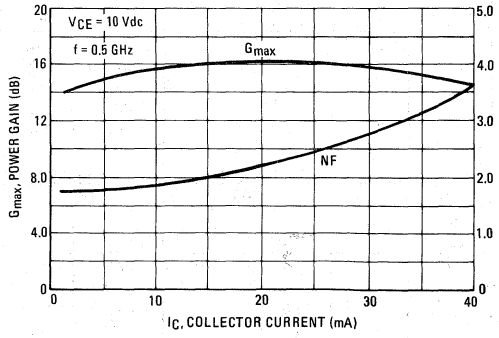


FIGURE 3 – POWER GAIN AND NOISE FIGURE versus COLLECTOR CURRENT



3

FIGURE 4 – S_{11} PARAMETERS

Frequency (MHz)		100		300		500		700		1000	
V_{CE} (Volts)	I_C (mA)	S11	∠φ	S11	∠φ	S11	∠φ	S11	∠φ	S11	∠φ
5.0	2.0	0.84	-35	0.57	-80	0.42	-115	0.34	-140	0.27	-166
	5.0	0.65	-45	0.34	-85	0.23	-115	0.18	-130	0.16	-150
	10	0.48	-50	0.32	-85	0.14	-105	0.12	-115	0.09	-120
	20	0.33	-50	0.15	-75	0.10	-90	0.09	-100	0.09	-101
	30	0.27	-50	0.13	-70	0.09	-85	0.09	-100	0.09	-101
10	2.0	0.86	-30	0.59	-75	0.42	-105	0.34	-130	0.25	-155
	5.0	0.70	-40	0.37	-75	0.24	-95	0.18	-110	0.13	-125
	10	0.55	-45	0.26	-70	0.17	-80	0.14	-90	0.13	-90
	20	0.41	-45	0.21	-60	0.15	-65	0.13	-75	0.14	-80
	30	0.36	-45	0.19	-55	0.14	-65	0.13	-75	0.13	-80

FIGURE 5 – S_{22} PARAMETERS

Frequency (MHz)		100		300		500		700		1000	
V_{CE} (Volts)	I_C (mA)	S22	∠φ	S22	∠φ	S22	∠φ	S22	∠φ	S22	∠φ
5.0	2.0	0.94	-15	0.77	-25	0.68	-30	0.66	-35	0.64	-45
	5.0	0.85	-20	0.63	-30	0.57	-30	0.55	-35	0.55	-45
	10	0.75	-25	0.55	-25	0.51	-30	0.50	-35	0.50	-40
	20	0.66	-25	0.50	-25	0.47	-30	0.47	-35	0.48	-40
	30	0.62	-25	0.49	-25	0.46	-25	0.46	-30	0.47	-40
10	2.0	0.95	-10	0.81	-20	0.74	-30	0.72	-35	0.71	-40
	5.0	0.87	-15	0.69	-25	0.64	-25	0.63	-30	0.63	-40
	10	0.80	-20	0.63	-20	0.59	-25	0.59	-30	0.60	-40
	20	0.72	-20	0.59	-20	0.57	-23	0.57	-30	0.58	-35
	30	0.70	-20	0.59	-20	0.57	-20	0.57	-30	0.58	-35

FIGURE 6 – S_{21} PARAMETERS

Frequency (MHz)		100		300		500		700		1000	
V_{CE} (Volts)	I_C mA	S21	∠φ	S21	∠φ	S21	∠φ	S21	∠φ	S21	∠φ
5.0	2.0	5.99	150	4.06	110	2.90	90	2.27	75	1.71	55
	5.0	11.38	135	5.91	100	3.90	80	2.93	70	2.17	55
	10	15.21	125	6.78	95	4.34	80	3.23	70	2.38	55
	20	17.98	115	7.27	90	4.58	75	3.40	65	2.50	50
	30	18.78	110	7.37	85	4.64	75	3.42	65	2.50	50
10	2.0	6.05	150	4.20	115	3.04	90	2.37	75	1.75	55
	5.0	11.46	135	6.17	100	4.06	85	3.08	70	2.26	55
	10	15.45	127	7.08	95	4.56	80	3.41	70	2.50	55
	20	18.35	120	7.57	90	4.80	75	3.58	65	2.61	55
	30	19.12	115	7.63	90	4.79	75	3.56	65	2.60	55

FIGURE 7 – S_{12} PARAMETERS

Frequency (MHz)		100		300		500		700		1000	
V_{CE} (Volts)	I_C (mA)	S12	∠φ	S12	∠φ	S12	∠φ	S12	∠φ	S12	∠φ
5.0	2.0	0.04	70	0.09	50	0.11	50	0.12	50	0.16	50
	5.0	0.04	70	0.07	60	0.11	60	0.14	60	0.19	55
	10	0.03	70	0.07	70	0.11	65	0.15	65	0.20	55
	20	0.03	75	0.07	70	0.12	70	0.15	65	0.21	55
	30	0.03	75	0.07	70	0.12	70	0.16	65	0.21	57
10	2.0	0.03	70	0.07	55	0.09	50	0.10	50	0.13	55
	5.0	0.03	70	0.06	60	0.09	65	0.12	60	0.15	60
	10	0.03	70	0.06	65	0.09	65	0.12	65	0.17	60
	20	0.03	75	0.06	70	0.09	70	0.13	65	0.18	60
	30	0.03	75	0.06	70	0.10	70	0.13	65	0.17	60

MRF931

The RF Line

LOW CURRENT

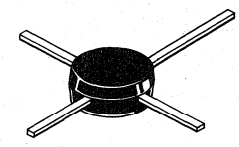
HIGH FREQUENCY TRANSISTOR

NPN SILICON

NPN SILICON HIGH-FREQUENCY TRANSISTOR

. . . designed primarily for use in low-power amplifiers to 1.0 GHz. Ideal for pagers and other battery operated systems where low-power consumption is critical.

- Low-Power Consumption Characterized for I_E = 0.1 to 1.0 mA
- High Current-Gain — Bandwidth Product — f_T = 3.0 GHz (Typ)
- Stripline Design for Optimum Performance



3

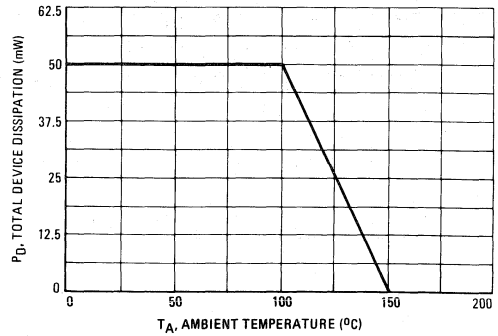
MAXIMUM RATINGS

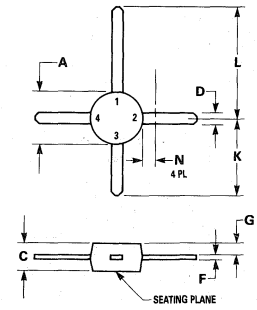
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	5.0	Vdc
Collector-Base Voltage	V_{CBO}	10	Vdc
Emitter-Base Voltage	V_{EBO}	2.0	Vdc
Collector Current — Peak	I_C	5.0	mAdc
Total Device Dissipation @ T_A = 100°C Derate Above 100°C	P_D	50 1.0	mW mW/°C
Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	500	°C/W

FIGURE 1 — POWER DERATING





STYLE 2:
PIN 1. COLLECTOR
2. EMITTER
3. BASE
4. EMITTER

NOTE:
DIMENSION D NOT APPLICABLE IN ZONE N.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.44	5.21	0.175	0.205
C	1.90	2.54	0.075	0.100
D	0.84	0.99	0.033	0.039
F	0.20	0.30	0.008	0.012
G	0.76	1.14	0.030	0.045
K	7.24	8.13	0.285	0.320
L	10.54	11.43	0.415	0.450
N	—	1.65	—	0.065

CASE 317-01

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 0.1 mAdc, I_B = 0)	$V_{(BR)CEO}$	5.0	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 0.01 mAdc, I_E = 0)	$V_{(BR)CBO}$	10	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	2.0		–	Vdc
Collector Cutoff Current (V_{CB} = 5.0 Vdc, I_E = 0)	I_{CBO}	–	–	50	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 0.25 mAdc, V_{CE} = 1.0 Vdc)	h_{FE}	30	–	150	–
DYNAMIC CHARACTERISTICS					
Current-Gain Bandwidth Product (I_E = 1.0 mAdc, V_{CE} = 1.0 Vdc, f = 1.0 GHz)	f_T	–	3.0	–	GHz
Collector-Base Capacitance (V_{CB} = 1.0 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	–	0.35	0.5	pF
FUNCTIONAL TESTS					
Noise Figure	NF				dB
(I_E = 0.25 mAdc, V_{CE} = 1.0 Vdc, f = 0.5 GHz)		–	3.8	–	
(I_E = 0.25 mAdc, V_{CE} = 1.0 Vdc, f = 1.0 GHz)		–	4.3	–	
Power Gain at Optimum Noise Figure	G_{NF}				dB
(I_E = 0.25 mAdc, V_{CE} = 1.0 Vdc, f = 0.5 GHz)		–	16	–	
(I_E = 0.25 mAdc, V_{CE} = 1.0 Vdc, f = 1.0 GHz)		–	10	–	
Transducer Power Gain	G_T				dB
(I_E = 0.5 mAdc, V_{CE} = 1.0 Vdc, f = 0.5 GHz)		–	18	–	
(I_E = 0.5 mAdc, V_{CE} = 1.0 Vdc, f = 1.0 GHz)		–	12	–	

3

FIGURE 2 – TRANSDUCER POWER GAIN AND NOISE FIGURE versus FREQUENCY

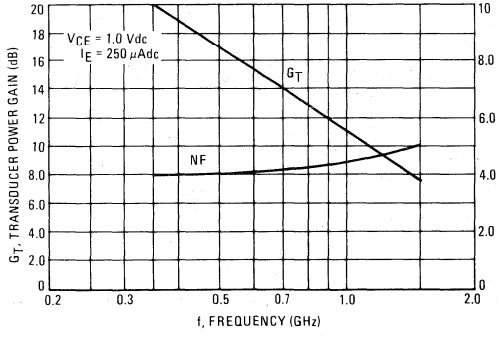
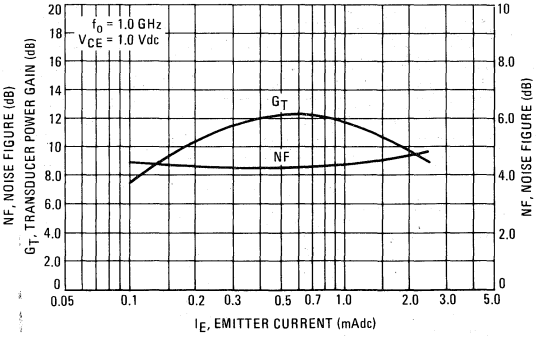


FIGURE 3 – TRANSDUCER POWER GAIN AND NOISE FIGURE versus EMITTER CURRENT



MRF941
MRFC941
MRF942
MMBR941,L
MRF9411,L

Advance Information

The RF Line

NPN Silicon Low Noise, High-Frequency, Transistors

. . . designed for use in low noise, small-signal amplifiers. This series features low noise, high gain, and current capability offered in a variety of packages.

- Fully Implanted Base and Emitter Structure
- 9 Finger, 1.25 Micron Geometry with Gold Top Metal
- Gold Sintered Back Metal
- Tape and Reel packaging Options Available

I_C = 15 mA
LOW NOISE
HIGH FREQUENCY
TRANSISTORS

3

MAXIMUM RATINGS		MRFC941 Chip	MRF941 Macro-X Case 317-01	MRF942 Case 303-01	MMBR941,L SOT-23 Case 318-02	MRF9411,L Case 318B-01 (SOT-143)	
Ratings	**Symbol**	**Values**					**Unit**
Collector-Emitter Voltage	V_{CEO}	10	10	10	10	10	Vdc
Collector-Base Voltage	V_{CBO}	20	20	20	20	20	Vdc
Emitter-Base Voltage	V_{EBO}	1.5	1.5	1.5	1.5	1.5	Vdc
Maximum Junction Temperature	T_{Jmax}	200	150	200	150	150	°C
Collector Current — Continuous(3)	I_C	15	50	15	50	50	mA
Storage Temperature	T_{stg}	−65 to +200	−65 to +150	−65 to +200	−55 to +150	−65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 0.1 mA, I_B = 0)	$V_{(BR)CEO}$	10	13	—	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mA, I_E = 0)	$V_{(BR)CBO}$	20	25	—	Vdc
Emitter Cutoff Current (V_{EB} = 1 V, I_E = 0)	I_{EBO}	—	—	1	μAdc
Collector Cutoff Current (V_{CB} = 10 V, I_E = 0)	I_{CBO}	—	—	1	μAdc
ON CHARACTERISTICS					
DC Current Gain (V_{CE} = 6 V, I_C = 5 mA)	h_{FE}	50	—	200	—

Note 1. Case Temperature is measured on the collector lead where it first contacts the printed circuit board closest to the package.
Note 2. Device offered in other ceramic/plastic packages.
Note 3. I_C — Continuous (MTBF ≈ 10 years)

(continued)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Collector-Base Capacitance (V_{CB} = 10 V, i_E = 0, f = 1 MHz)	C_{cb}	—	0.2	—	pF
Current Gain — Bandwidth Product (V_{CE} = 6 V, I_C = 15 mA, f = 1 GHz)	f_T	—	8	—	GHz
FUNCTIONAL TESTS					
Associated Gain at Minimum Noise Figure	G_{NF}				dB
(V_{CE} = 6 V, I_C = 5 mA, f = 1 GHz)		—	16.5	—	
(V_{CE} = 6 V, I_C = 5 mA, f = 2 GHz)		—	12.5	—	
(V_{CE} = 6 V, I_C = 5 mA, f = 4 GHz)		—	9	—	
Noise Figure	NF_{min}				dB
(V_{CE} = 6 V, I_C = 5 mA, f = 1 GHz)		—	1.2	—	
(V_{CE} = 6 V, I_C = 5 mA, f = 2 GHz)		—	1.7	—	
(V_{CE} = 6 V, I_C = 5 mA, f = 4 GHz)		—	2.8	—	

TYPICAL CHARACTERISTICS

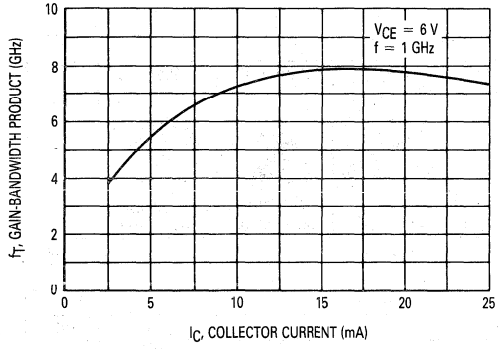


Figure 1. Gain-Bandwidth Product versus Current

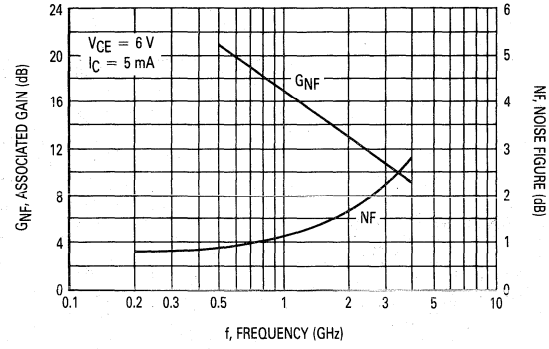


Figure 2. Associated Gain and Optimum Noise Figure versus Frequency

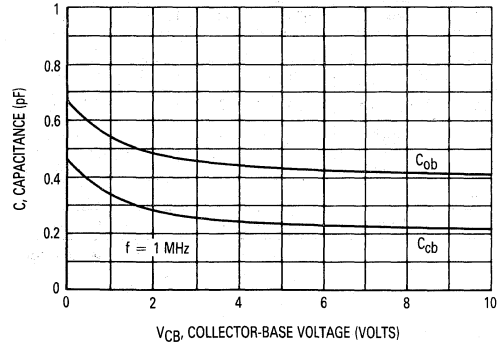


Figure 3. Junction Capacitance versus Voltage

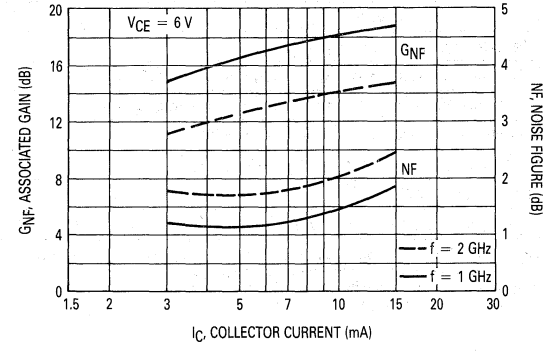


Figure 4. Associated Gain and Optimum Noise Figure versus Collector Current

Advance Information

The RF Line

NPN Silicon Low Noise, High-Frequency Transistors

MRF951
MRFC951
MRF952
MMBR951,L
MRF9511,L

. . . designed for use in high gain, low noise small-signal amplifiers. This series features excellent broadband linearity and is offered in a variety of packages.

- Fully Implanted Base and Emitter Structure
- 18 Finger, 1.25 Micron Geometry with Gold Top Metal
- Gold Sintered Back Metal
- Tape and Reel Packaging Options Available

I_C = 30 mA
LOW NOISE
HIGH FREQUENCY
TRANSISTORS

MAXIMUM RATINGS		MRFC951 Chip	MRF951 Macro-X Case 317-01	MRF952 Case 303-01	MMBR951,L SOT-23 Case 318-02	MRF9511,L Case 318B-01 (SOT-143)	
Ratings	**Symbol**	**Values**					**Unit**
Collector-Emitter Voltage	V_{CEO}	10	10	10	10	10	Vdc
Collector-Base Voltage	V_{CBO}	20	20	20	20	20	Vdc
Emitter-Base Voltage	V_{EBO}	1.5	1.5	1.5	1.5	1.5	Vdc
Maximum Junction Temperature	T_{Jmax}	200	150	200	150	150	°C
Collector Current — Continuous(3)	I_C	30	100	30	100	100	mA
Storage Temperature	T_{stg}	−65 to +200	−65 to +150	−65 to +200	−55 to +150	−65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 0.1 mA, I_B = 0)	$V_{(BR)CEO}$	10	13	—	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mA, I_E = 0)	$V_{(BR)CBO}$	20	25	—	Vdc
Emitter Cutoff Current (V_{EB} = 1 V, I_E = 0)	I_{EBO}	—	—	1	μAdc
Collector Cutoff Current (V_{CB} = 10 V, I_E = 0)	I_{CBO}	—	—	1	μAdc
ON CHARACTERISTICS					
DC Current Gain (V_{CE} = 6 V, I_C = 5 mA)	h_{FE}	50	—	200	—

Note 1. Case Temperature is measured on the collector lead where it first contacts the printed circuit board closest to the package.
Note 2. Device offered in other ceramic/plastic packages.
Note 3. I_C — Continuous (MTBF ≈ 10 years)

(continued)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Collector-Base Capacitance (V_{CB} = 10 V, I_E = 0, f = 1 MHz)	C_{cb}	—	0.3	—	pF
Current Gain — Bandwidth Product (V_{CE} = 6 V, I_C = 30 mA, f = 1 GHz)	f_T	—	7.5	—	GHz
FUNCTIONAL TESTS					
Associated Gain at Minimum	G_{NF}				dB
(V_{CE} = 6 V, I_C = 5 mA, f = 1 GHz)		—	16.5	—	
(V_{CE} = 6 V, I_C = 5 mA, f = 2 GHz)		—	12.5	—	
Noise Figure	NF_{min}				dB
(V_{CE} = 6 V, I_C = 5 mA, f = 1 GHz)		—	1.2	—	
(V_{CE} = 6 V, I_C = 5 mA, f = 2 GHz)		—	1.7	—	

TYPICAL CHARACTERISTICS

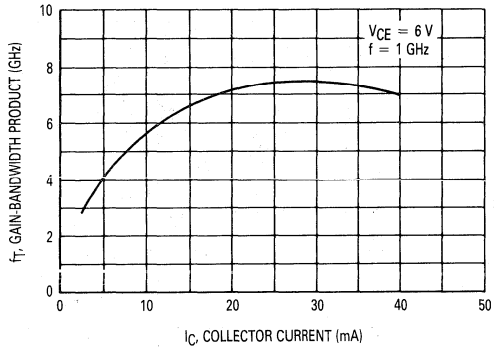


Figure 1. Gain-Bandwidth Product versus Current

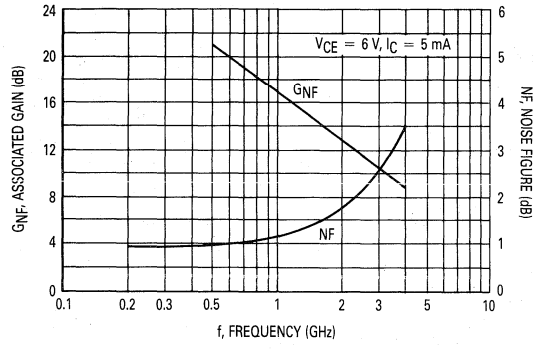


Figure 2. Associated Gain and Optimum Noise Figure versus Frequency

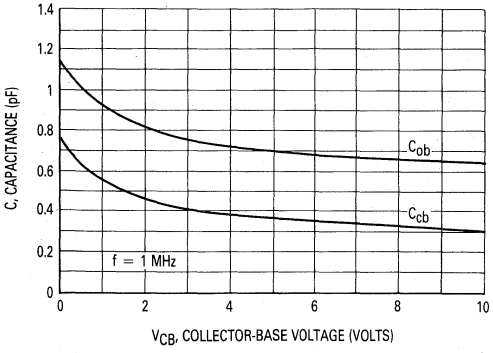


Figure 3. Junction Capacitance versus Voltage

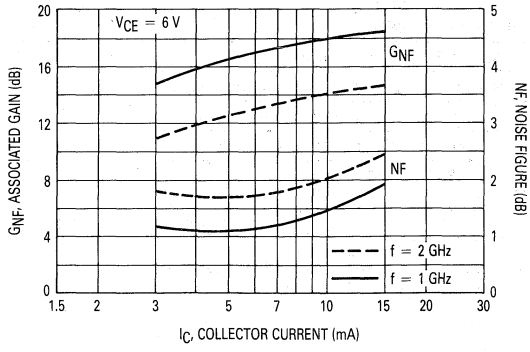


Figure 4. Associated Gain and Optimum Noise Figure versus Collector Current

The RF Line

N-Channel Dual-Gate GaAs Field-Effect Transistor

MRF966
MRFC966

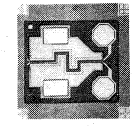
. . . depletion mode dual-gate MES FET designed for high frequency amplifier and mixer applications.

- Excellent Receiver Front End
- Low Noise Figure — NF = 1.2 dB, 1 GHz (Typ)
- High Power Gain — G_p = 17 dB, 1 GHz (Typ)
- Low Reverse Transfer Capacitance — C_{rss} = 40 fF (Typ)
- High Transconductance — g_m = 20 mS (Typ)
- Fully Characterized
- Gold Metallization

N-CHANNEL DUAL-GATE GaAs FIELD-EFFECT TRANSISTOR



MRF966
CASE 317-01



CHIP
MRFC966

3

MAXIMUM RATINGS

Rating	Symbol	MRFC966	MRF966	Unit
Drain-Source Voltage	V_{DS}	10	10	Vdc
Gate-Source Voltage — Reverse	V_{G1S} V_{G2S}	−8 −8	−8 −8	Vdc
Gate-Source Voltage — Forward	V_{G1S} V_{G2S}	+1 +1	+1 +1	Vdc
Drain Current — Continuous	I_D	80	80	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	350 T_J = 125°C Max	350 3.5	mW mW/°C
Storage Channel Temperature Range	T_{stg}	−65 to +125	−65 to +125	°C
Junction Temperature Range	T_J	−65 to +125	−65 to +125	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{G1S} = V_{G2S} = −4.5 Vdc, I_D = 100 μA)	$V_{(BR)DSX}$	10	—	—	Vdc
Gate 1-to-Source Cutoff Voltage (V_{DS} = 5 Vdc, V_{G2S} = 0, I_D = 500 μA)	$V_{G1S(off)}$	−2	—	−4.5	Vdc
Gate 2-to-Source Cutoff Voltage (V_{DS} = 5 Vdc, V_{G1S} = 0, I_D = 500 μA)	$V_{G2S(off)}$	−2	—	−4.5	Vdc
Gate 1 Leakage Current (V_{G1S} = −5 Vdc, V_{G2S} = V_{DS} = 0)	I_{G1SS}	—	—	10	μAdc
Gate 2 Leakage Current (V_{G2S} = −5 Vdc, V_{G1S} = V_{DS} = 0)	I_{G2SS}	—	—	10	μAdc
ON CHARACTERISTICS					
Zero-Gate Voltage Drain Current (V_{DS} = 5 Vdc, V_{G1S} = V_{G2S} = 0)	I_{DSS}	30	50	80	mAdc
SMALL-SIGNAL CHARACTERISTICS					
Transconductance (V_{DS} = 5 Vdc, V_{G2S} = 0, I_D = 10 mA, f = 1 kHz)	g_m	18	20	—	mS
Input Capacitance (V_{DS} = 5 Vdc, V_{G2S} = 0, I_D = 10 mA, f = 1 MHz)	C_{iss}	—	1.5	—	pF
Reverse Transfer Capacitance (V_{DS} = 5 Vdc, V_{G2S} = 0, I_D = 10 mA, f = 1 MHz)	C_{rss}	—	0.04	—	pF

Handling and Packaging — MES devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MES devices should be observed.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL CHARACTERISTICS					
Noise Figure(1) (V_{DS} = 5 Vdc, V_{G2S} = 0, I_{DS} = 10 mA, f = 1 GHz)	NF	—	1.2	1.5	dB
Common Source Power Gain(1) (V_{DS} = 5 Vdc, V_{G2S} = 0, I_{DS} = 10 mA, f = 1 GHz)	G_{ps}	15	17	—	dB
Intermodulation Distortion (V_{DS} = 5 Vdc, I_{DS} = 10 mA, f_1 = 995 MHz, f_2 = 1001 MHz, V_{G2} = 0, P_{in} = −40 dBm)	IMD_3	—	−65	—	dB
Linear Power Point(2) (V_{DS} = 5 Vdc, I_{DS} = 10 mA, f_1 = 995 MHz, f_2 = 1001 MHz, V_{G2} = 0)	P_L	—	+1	—	dBm
Output Power at 1 dB Compression Point (V_{DS} = 5 Vdc, I_{DS} = 10 mA, f = 1 GHz)	P_{out}	—	10	—	dBm

NOTES:
1. Data taken using a 50 Ω test fixture, Microlab SF31N slug tuners, HP11590B bias networks and the HP8970A or Eaton 2075 noise figure meter. Note: V_{G2S} = 0. Refer to Figure 11.
2. The linear power point is the output power level at which either the signal $2f_1 \pm f_2$ or $2f_2 \pm f_1$ are 30 dB below f_1 or f_2.

TYPICAL CHARACTERISTICS

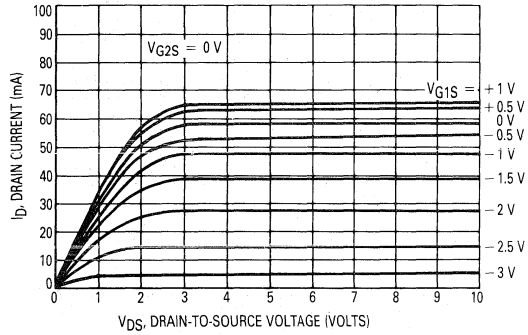


Figure 1. Drain Current versus Drain-To-Source Voltage

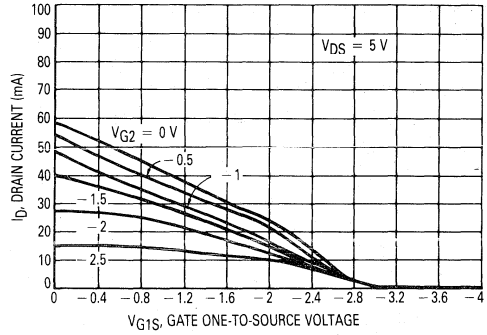


Figure 2. Drain Current versus Gate One-To-Source Voltage

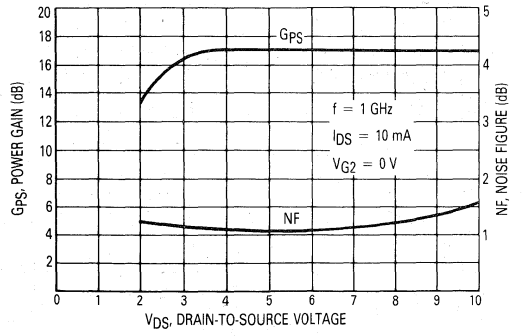


Figure 3. Power Gain and Noise Figure versus Drain-To-Source Voltage

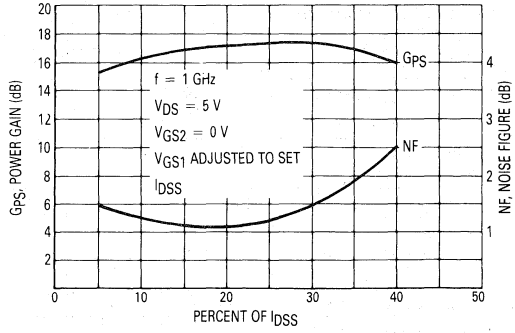


Figure 4. Power Gain and Noise Figure versus Percent of I_{DSS}

TYPICAL CHARACTERISTICS

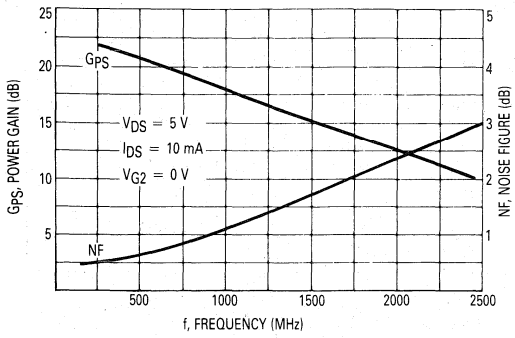


Figure 5. Power Gain and Noise Figure versus Frequency

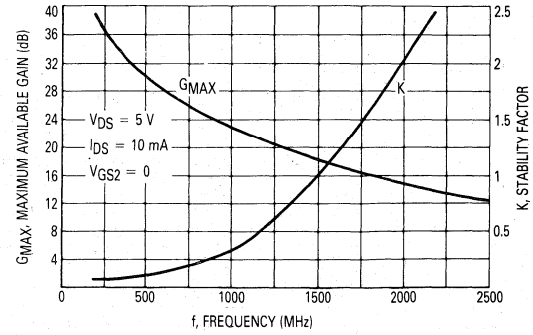


Figure 6. Maximum Available Gain and Stability Factor versus Frequency

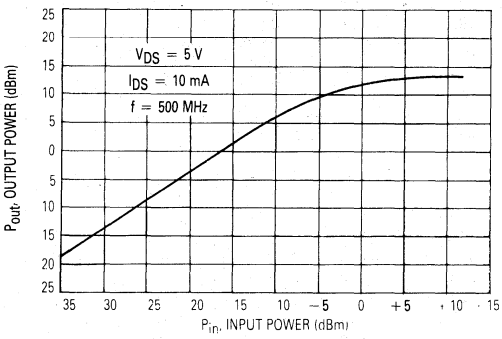


Figure 7. Output Power versus Input Power @ 500 MHz

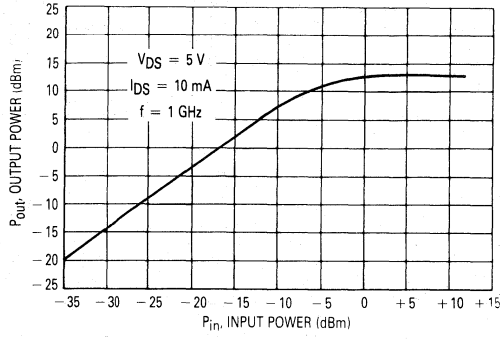


Figure 8. Output Power versus Input Power @ 1 GHz

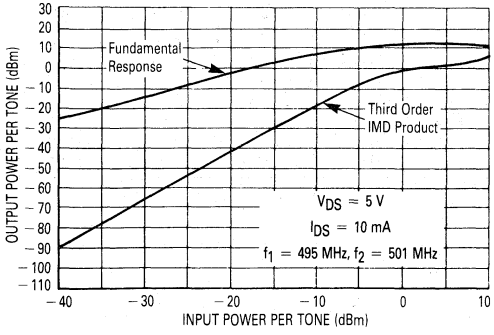


Figure 9. Third Order Intermodulation Distortion @ 500 MHz

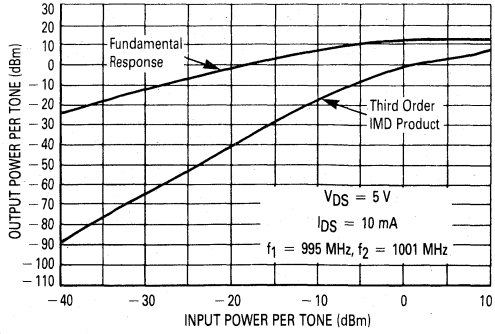


Figure 10. Third Order Intermodulation Distortion @ 1 GHz

COMMON SOURCE S-PARAMETERS

V_{DS} (Volts)	I_{DS} (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
3	5	200	0.997	−5.7	1.251	172.1	0.003	88.3	0.944	−6.4
		500	0.983	−14.3	1.23	161.2	0.007	84.6	0.931	−16
		1000	0.941	−28.3	1.201	142.4	0.013	78.5	0.9	−32.2
		1500	0.866	−42.3	1.133	122	0.016	70.4	0.836	−49.6
		2000	0.762	−55.4	1.011	101.1	0.018	56.2	0.744	−67.5
		2500	0.642	−66.4	0.819	77.4	0.015	25.5	0.608	−87.5
	10	200	0.995	−6.2	1.60	172.0	0.002	84.1	0.93	−6.3
		500	0.981	−15.1	1.58	161.3	0.007	82.5	0.92	−15.8
		1000	0.928	−29.9	1.55	142.9	0.013	81.5	0.90	−31.8
		1500	0.838	−44.4	1.46	122.3	0.016	74.7	0.84	−49.4
		2000	0.716	−57.7	1.31	101.2	0.018	60.1	0.76	−68.4
		2500	0.584	−67.5	1.06	77.4	0.015	26.7	0.63	−89.8
	15	200	0.996	−6.3	1.83	172.0	0.002	76.4	0.93	−6.3
		500	0.979	−15.7	1.80	161.2	0.006	91.5	0.92	−15.6
		1000	0.921	−30.9	1.76	142.3	0.012	82.3	0.90	−31.6
		1500	0.820	−45.9	1.66	121.7	0.016	76.1	0.85	−49.1
		2000	0.689	−58.7	1.48	100.6	0.016	64.1	0.77	−68.2
		2500	0.552	−67.4	1.20	76.7	0.013	28.9	0.65	−90.3
	20	200	0.995	−6.5	1.97	171.9	0.003	85.7	0.92	−6.2
		500	0.977	−16.2	1.93	160.7	0.007	89.0	0.91	−15.3
		1000	0.910	−32.0	1.89	141.7	0.011	84.0	0.89	−31.0
		1500	0.804	−47.1	1.79	120.9	0.016	78.3	0.85	−48.4
		2000	0.669	−59.7	1.59	99.6	0.017	66.2	0.78	−67.4
		2500	0.531	−67.7	1.29	75.8	0.012	32.7	0.66	−89.2
5	5	200	0.997	−5.8	1.27	172.8	0.002	102.6	0.97	−3.8
		500	0.983	−14.3	1.26	162.6	0.004	82.3	0.97	−9.4
		1000	0.939	−28.4	1.24	146.0	0.006	93.4	0.96	−18.8
		1500	0.866	−42.6	1.21	128.4	0.008	102.6	0.95	−28.3
		2000	0.765	−5.3	1.14	111.6	0.007	137.7	0.93	−37.6
		2500	0.642	−68.4	1.05	93.1	0.012	−179.0	0.92	−47.0
	10	200	0.966	−6.0	1.61	172.8	0.002	88.1	0.97	−3.8
		500	0.982	−15.1	1.59	162.8	0.004	85.8	0.97	−9.4
		1000	0.928	−29.9	1.57	146.1	0.006	94.6	0.96	−18.6
		1500	0.841	−44.6	1.53	128.7	0.006	110.4	0.94	−28.0
		2000	0.724	−58.3	1.42	111.6	0.008	152.6	0.93	−37.0
		2500	0.589	−69.4	1.30	93.3	0.014	179.1	0.92	−46.3
	15	200	0.997	−6.2	1.82	172.6	0.001	103.2	0.97	−3.7
		500	0.979	−15.6	1.80	162.5	0.003	85.3	0.96	−9.3
		1000	0.920	−30.8	1.77	145.6	0.005	92.4	0.95	−18.4
		1500	0.824	−45.8	1.72	127.9	0.007	116.3	0.94	−27.3
		2000	0.699	−59.2	1.59	110.8	0.008	154.1	0.93	−36.3
		2500	0.560	−69.6	1.44	92.6	0.017	176.2	0.92	−45.4
	20	200	0.995	−6.5	1.96	172.4	0.002	85.9	0.97	−3.7
		500	0.977	−16.1	1.93	162.1	0.004	80.9	0.96	−9.1
		1000	0.913	−31.7	1.90	144.9	0.005	92.1	0.95	−17.9
		1500	0.810	−47.0	1.83	126.9	0.007	121.4	0.94	−26.9
		2000	0.679	−60.4	1.69	109.7	0.009	153.4	0.93	−35.6
		2500	0.538	−70.0	1.53	91.4	0.017	176.0	0.93	−44.6

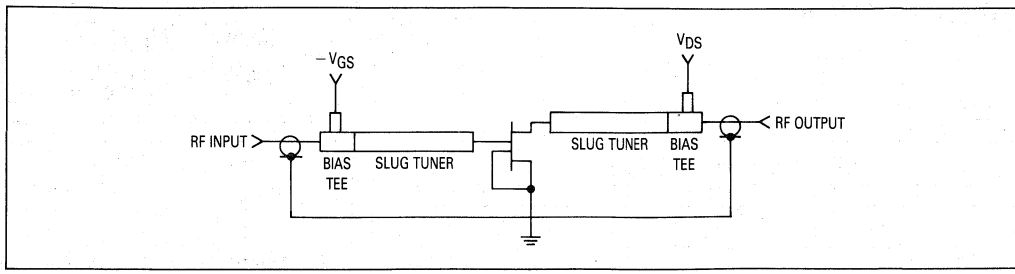
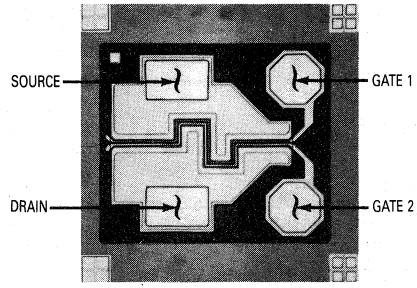


Figure 11. 1 GHz Test Circuit Schematic

f (MHz)	G_{NF} (dB)	NF (dB)	ΓMS NF_{opt}	ΓML NF_{opt}
450	20	0.6	0.82 ∠21°	0.80 ∠11°
1000	17	1.2	0.74 ∠21°	0.77 ∠12°

Figure 12. Source and Load Impedance for Optimum Noise Figure

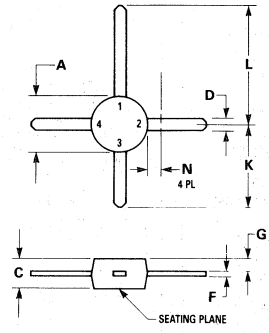


MRFC966 Chip Topography

Nominal Chip Size: 0.017″ x 0.020″ x 0.005″
Drain/Source Bond Pad: 0.003″ x 0.004″
Gate 1/Gate 2 Bond Pad: 0.0035″ x 0.0035″

3

OUTLINE DIMENSIONS



NOTE:
DIMENSION D NOT APPLICABLE IN ZONE N.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.44	5.21	0.175	0.205
C	1.90	2.54	0.075	0.100
D	0.84	0.99	0.033	0.039
F	0.20	0.30	0.008	0.012
G	0.76	1.14	0.030	0.045
K	7.24	8.13	0.285	0.320
L	10.54	11.43	0.415	0.450
N	—	1.65	—	0.065

STYLE 1:
PIN 1. DRAIN
2. SOURCE
3. GATE 1
4. GATE 2

CASE 317-01
PLASTIC MACRO-X

MRF1000MA
MRF1000MB
MRF1000MC

The RF Line

0.7 W 960-1215 MHz

CLASS A/AB MICROWAVE POWER TRANSISTOR

NPN SILICON

MICROWAVE PULSE POWER TRANSISTOR

. . . designed for Class A and AB *common emitter* amplifier applications in the low-power stages of IFF, DME, TACAN, radar transmitters, and CW systems.

- Guaranteed Performance @ 1090 MHz , 18 Vdc — Class A
  Output Power = 0.2 Watt
  Minimum Gain = 10 dB
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Industry Standard Package
- Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Compatible with Other 1000M Types
- Internal Input Matching for Broadband Operation

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CBO}	50	Vdc
Emitter-Base Voltage	V_{EBO}	3.5	Vdc
Collector-Current — Continuous	I_C	200	mAdc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	7.0 40	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	25	°C/W

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

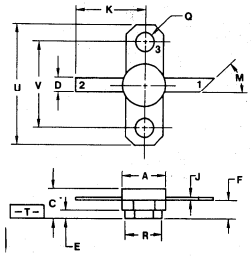
(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

MRF1000MC



STYLE 2:
1. COLLECTOR
2. BASE
3. EMITTER

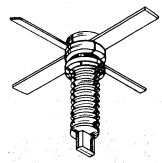
CASE 361A-01



NOTES:
1. DIMENSIONS R AND U ARE DATUMS AND T IS A DATUM SURFACE AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR MOUNTING HOLES: ⌖ ∅ 0.38 (0.015) Ⓜ T U Ⓜ R Ⓜ
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	7.06	7.26	0.278	0.286
C	4.44	5.20	0.175	0.205
D	2.36	2.71	0.093	0.107
E	1.39	1.77	0.055	0.070
F	2.66	3.42	0.105	0.135
J	0.10	0.15	0.004	0.006
K	11.04	–	0.435	
M	45° NOM		45° NOM	
Q	3.04	34.2	0.120	0.135
R	6.09	6.86	0.240	0.260
U	20.06	20.57	0.790	0.810
V	14.27 BSC		0.562 BSC	

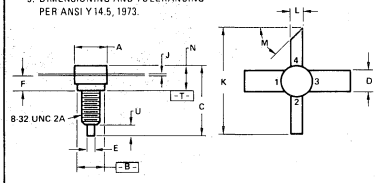
MRF1000MA
CASE 332-01



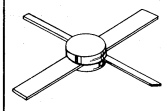
DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	7.01	7.62	0.276	0.300
B	6.20	6.50	0.244	0.256
C	16.26	16.76	0.640	0.660
D	4.95	5.21	0.195	0.205
E	1.40	1.65	0.055	0.065
F	2.92	3.43	0.115	0.135
J	0.08	0.18	0.003	0.007
K	15.24	–	0.600	–
L	2.41	2.67	0.095	0.105
M	45° Nom		45° Nom	
N	5.08	5.46	0.200	0.215
U	2.92	3.68	0.115	0.145

NOTES:
1. DIM B IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS: ⌖ 0.76(0.030) Ⓜ T B Ⓜ
3. T IS SEATING PLANE.
4. DIMENSION K APPLIES TWO PLACES.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

STYLE 2:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR



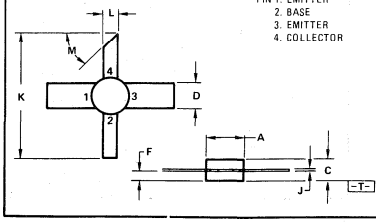
MRF1000MB
CASE 332A-01



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	7.01	7.62	0.276	0.300
B	6.20	6.50	0.244	0.256
C	3.30	3.81	0.130	0.150
D	4.95	5.21	0.195	0.205
F	1.40	1.78	0.055	0.070
J	0.08	0.18	0.003	0.007
K	15.24	–	0.600	–
L	2.41	2.67	0.095	0.105
M	45° NOM		45° NOM	

NOTES:
1. DIM A IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS: ⌖ 0.76 (0.030) Ⓜ T A Ⓜ
3. T IS SEATING PLANE.
4. DIM K APPLIES 2 PLACES.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

STYLE 2:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

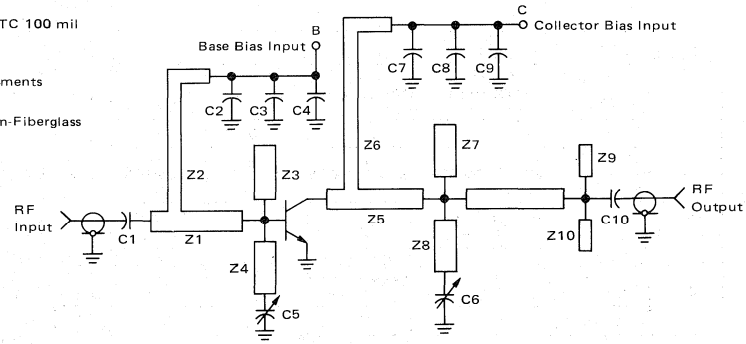


ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

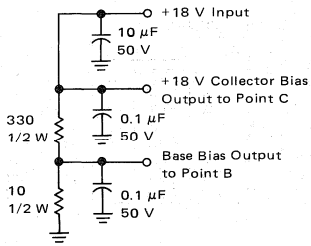
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	50	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 5.0 mAdc, I_E = 0)	$V_{(BR)CBO}$	50	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)	I_{CBO}	—	—	0.5	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	—	100	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	2.0	5.0	pF
FUNCTIONAL TESTS					
Common-Emitter Power Gain — Class A (V_{CE} = 18 Vdc, I_C = 100 mAdc, f = 1090 MHz, P_{out} = 200 mW)	G_{PE}	10	12	—	dB
Common-Emitter Power Gain — Class AB (V_{CE} = 18 Vdc, I_{CQ} = 10 mAdc, f = 1090 MHz, P_{out} = 0.7 W)	G_{PE}	—	10.7	—	dB
Load Mismatch — Class A (V_{CE} = 18 Vdc, I_C = 100 mAdc, f = 1090 MHz, P_{out} = 200 mW, VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Power Output			

FIGURE 1 – 1090 MHz TEST CIRCUIT

C1, C2, C3, C7, C8, C10 – 220 pF ATC 100 mil
C4, C9 – 4.7 μF 50 V Tantalum
C5, C6 – 0.8-8 pF Johanson #7290
Z1-Z10 – Distributed Microstrip Elements – See Figure 8
Board Material – 0.031" Thick Teflon-Fiberglass ϵ_r = 2.56



Class AB Bias Control Circuit
18 V Output I_{CQ} 10 mA Nominal



Class A Constant Current Bias Control Circuit
I_C = 100 mA, V_{CE} = 18 V.

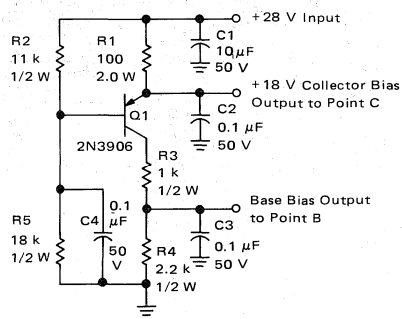


FIGURE 2 – OUTPUT POWER versus INPUT POWER

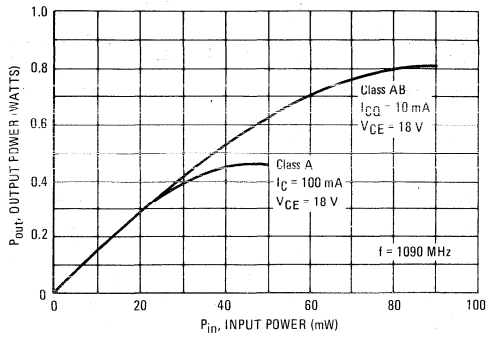


FIGURE 3 – OUTPUT POWER versus FREQUENCY

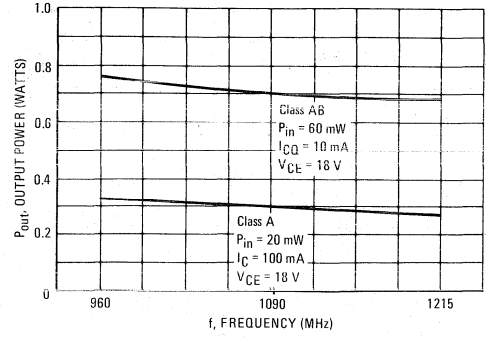


FIGURE 4 – DC SAFE OPERATING AREA

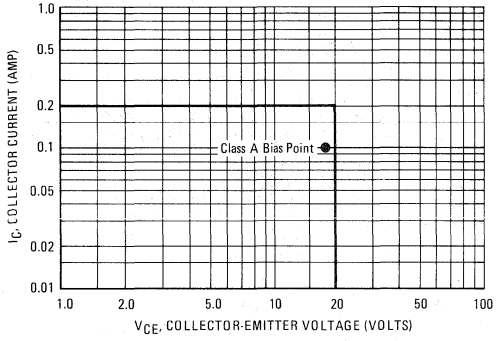


FIGURE 5 – POWER GAIN versus FREQUENCY

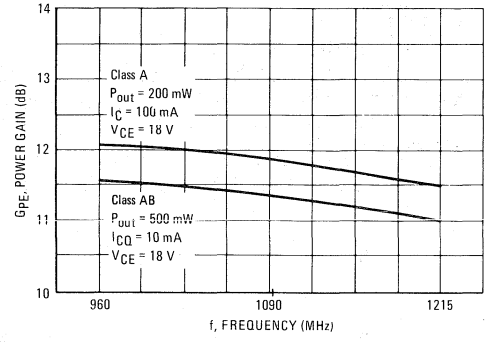
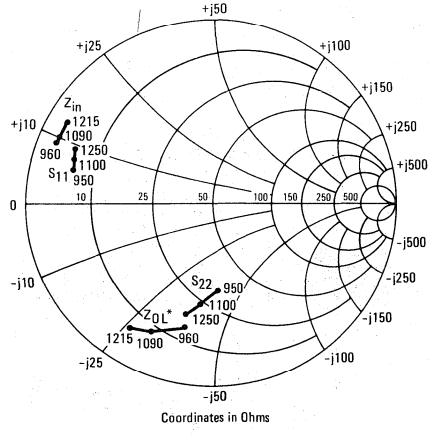


FIGURE 6 – COMMON-EMITTER S-PARAMETERS AND SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCES



SERIES EQUIVALENT IMPEDANCES
P_{out} = 0.5 W, V_{CE} = 18 Vdc,
I_{CQ} = 10 mAdc, Class AB

f MHz	Z_{in} Ohms	Z_{OL}^* Ohms
960	3.0 + j9.0	16 – j40
1090	3.2 + j10	8.5 – j31
1215	2.8 + j12	7.0 – j26

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

S-PARAMETERS – V_{CE} = 18 Vdc, I_C = 100 mAdc, Class A

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
950	0.77	166	2.42	40	0.016	42	0.48	-87
1000	0.78	165	2.36	38	0.016	48	0.50	-90
1050	0.77	163	2.31	33	0.016	46	0.51	-94
1100	0.77	162	2.31	28	0.016	46	0.54	-97
1150	0.78	161	2.20	23	0.015	46	0.57	-100
1200	0.78	159	2.20	19	0.016	47	0.59	-103
1250	0.78	158	2.12	12	0.016	42	0.61	-106

FIGURE 7 – 1090 MHz TEST AMPLIFIER

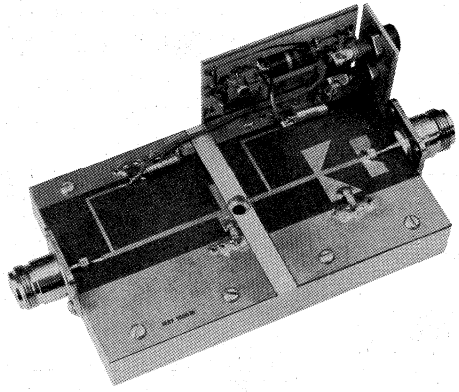
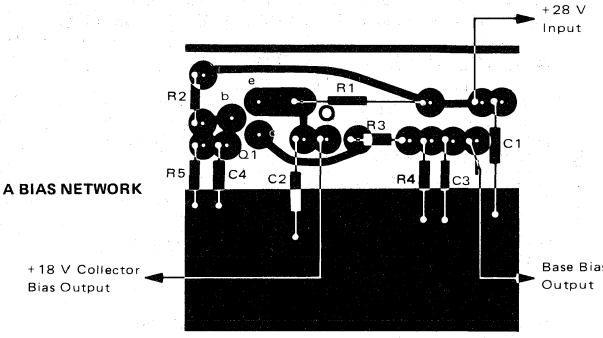
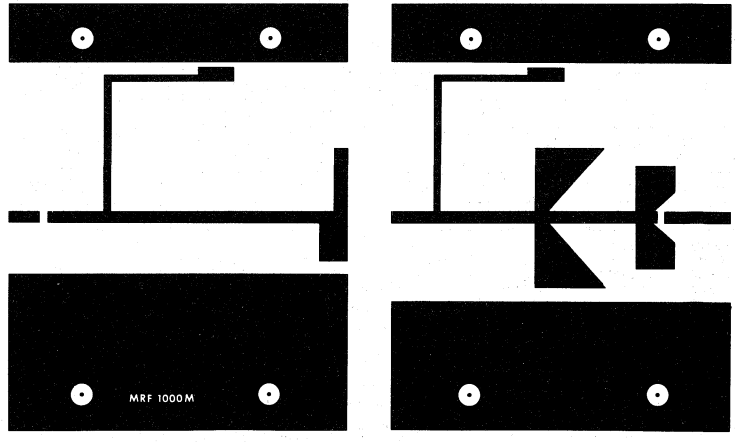


FIGURE 8 – PRINTED CIRCUIT BOARD LAYOUT – 1090 MHz TEST CIRCUIT



AMPLIFIER



NOTE: The Printed Circuit Board shown is 75% of the original.

3

MRF1002MA
MRF1002MB
MRF1002MC

The RF Line

2.0 W PEAK 960-1215 MHz

MICROWAVE POWER TRANSISTOR

NPN SILICON

MICROWAVE PULSE POWER TRANSISTOR

. . . designed for Class B and C *common base* amplifier applications in short and long pulse TACAN, IFF, DME, and radar transmitters.

- Guaranteed Performance @ 1090 MHz , 35 Vdc
  Output Power = 2.0 Watts Peak
  Minimum Gain = 10 dB
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Industry Standard Package
- Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Compatible with Other 1002M Types
- Internal Input Matching for Broadband Operation

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CBO}	50	Vdc
Emitter-Base Voltage	V_{EBO}	3.5	Vdc
Collector-Current — Continuous	I_C	250	mAdc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	7.0 40	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

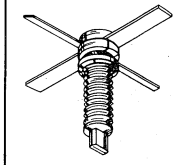
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	25	°C/W

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

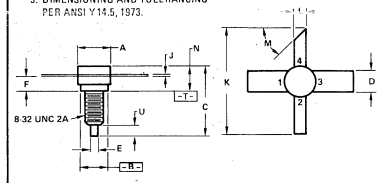
MRF1002MA
CASE 332-01



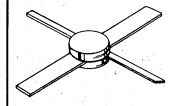
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.01	7.62	0.276	0.300
B	6.20	6.50	0.244	0.256
C	16.26	16.76	0.640	0.660
D	4.95	5.21	0.195	0.205
E	1.40	1.65	0.055	0.065
F	2.92	3.43	0.115	0.135
J	0.08	0.18	0.003	0.007
K	15.24	–	0.600	–
L	2.41	2.67	0.095	0.105
M	45° Nom		45° Nom	
N	5.08	5.46	0.200	0.215
U	2.92	3.68	0.115	0.145

NOTES:
1. DIM [B] IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ 0.76(0.030)Ⓜ T BⓂ
3. [T] IS SEATING PLANE.
4. DIMENSION K APPLIES TWO PLACES.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR



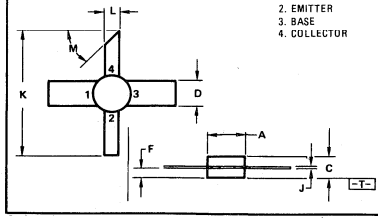
MRF1002MB
CASE 332A-01



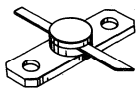
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.01	7.62	0.276	0.300
B	6.20	6.50	0.244	0.256
C	3.30	3.81	0.130	0.150
D	4.95	5.21	0.195	0.205
F	1.40	1.78	0.055	0.070
J	0.08	0.18	0.003	0.007
K	15.24	–	0.600	–
L	2.41	2.67	0.095	0.105
M	45° NOM		45° NOM	

NOTES:
1. DIM [A] IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ 0.76 (0.030) Ⓜ T AⓂ
3. [T] IS SEATING PLANE.
4. DIM K APPLIES 2 PLACES.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

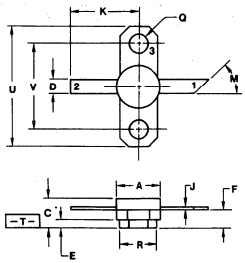
STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR



MRF1002MC



STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. BASE



CASE 361A-01

NOTES:
1. DIMENSIONS R AND U ARE DATUMS AND T IS A DATUM SURFACE AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR MOUNTING HOLES:
   ⌖ ∮ 0.38 (0.015) Ⓜ T U Ⓜ R Ⓜ
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

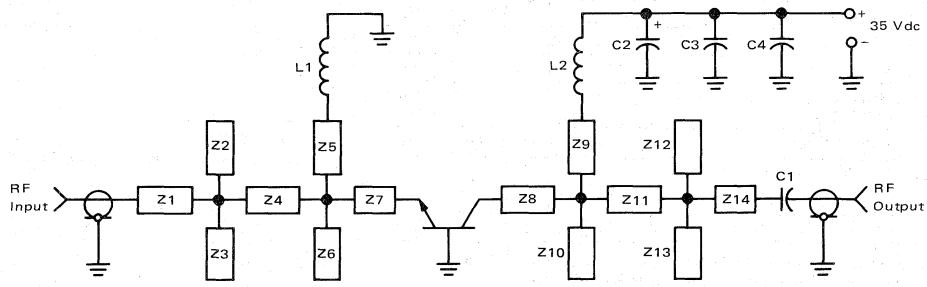
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.06	7.26	0.278	0.286
C	4.44	5.20	0.175	0.205
D	2.36	2.71	0.093	0.107
E	1.39	1.77	0.055	0.070
F	2.66	3.42	0.105	0.135
J	0.10	0.15	0.004	0.006
K	11.04	–	0.435	–
M	45° NOM		45° NOM	
Q	3.04	34.2	0.120	0.135
R	6.08	6.86	0.240	0.260
U	20.06	20.57	0.790	0.810
V	14.27 BSC		0.562 BSC	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	50	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 5.0 mAdc, I_E = 0)	$V_{(BR)CBO}$	50	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 35 Vdc, I_E = 0)	I_{CBO}	—	—	0.5	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	—	100	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 35 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	2.5	5.0	pF
FUNCTIONAL TESTS (Pulse Width = 10 μs, Duty Cycle = 1.0%)					
Common-Base Amplifier Power Gain (V_{CC} = 35 Vdc, P_{out} = 2.0 W pk, f = 1090 MHz)	G_{PB}	10	12	—	dB
Collector Efficiency (V_{CC} = 35 Vdc, P_{out} = 2.0 W pk, f = 1090 MHz)	η	40	45	—	%
Load Mismatch (V_{CC} = 35 Vdc, P_{out} = 2.0 W, f = 1090 MHz VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Power Output			

3

FIGURE 1 – 1090 MHz TEST CIRCUIT



C1, C3 – 220 pF Chip Capacitor, 100 mil ATC
C2 – 20 μF/50 Vdc Electrolytic
C4 – 0.1 μF Erie Redcap
L1, L2 – 2 Turns #18 AWG, 1/8" ID
Z1-Z14 – Distributed Microstrip Elements – See Figure 9
Board Material – 0.031" Thick Teflon-Fiberglass,
ϵ_r = 2.56

FIGURE 2 – OUTPUT POWER versus INPUT POWER

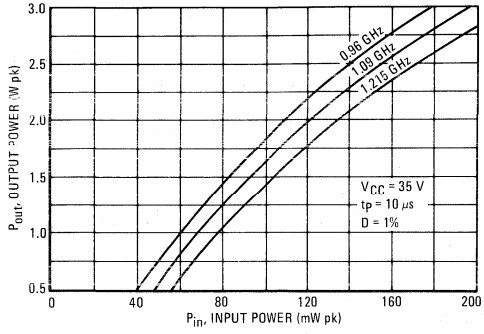


FIGURE 3 – OUTPUT POWER versus FREQUENCY

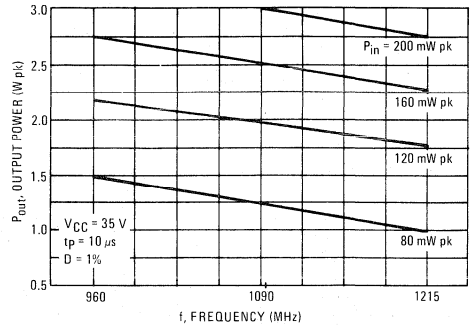


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

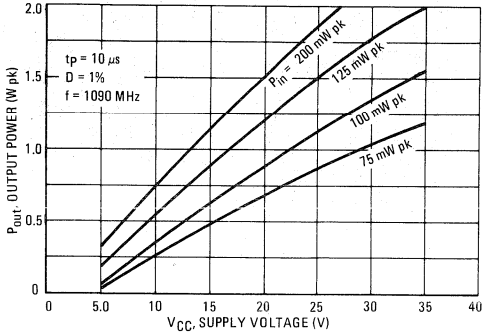


FIGURE 5 – POWER GAIN versus FREQUENCY

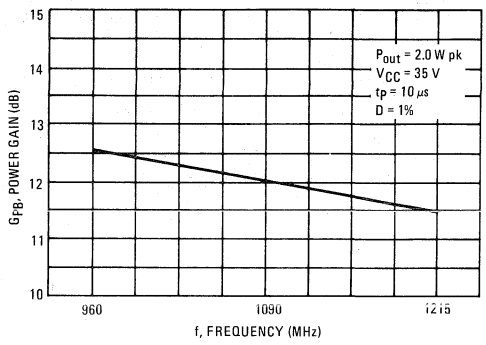
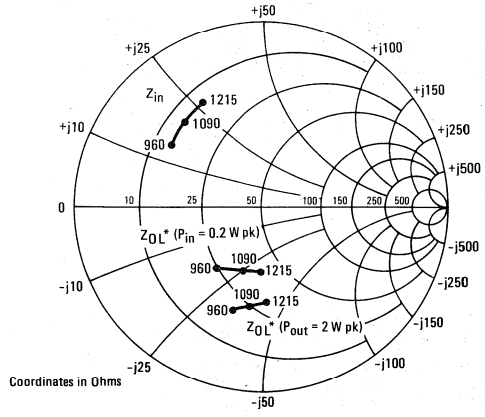


FIGURE 6 – SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCE



V_{CC} = 35 Vdc,
t_P = 10 μs, D = 1.0%

f MHz	Z_{in} Ohms	Z_{OL}* Ohms P_{out} = 2 W pk	Z_{OL}* Ohms P_{in}=0.2 W pk
960	15.5 + j16.5	20 + j32.5	25 + j21
1090	15 + j20	25 + j34	31 + j26
1215	14 + j27	33.5 + j42.5	37 + j32.5

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

FIGURE 7 – 1090 MHz TEST AMPLIFIER

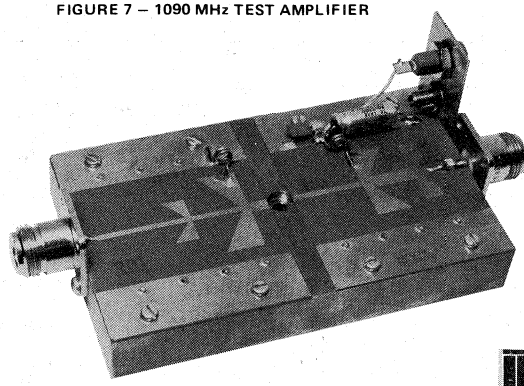


FIGURE 8 – TYPICAL LONG PULSE PERFORMANCE

P_{out} = 2.0 W pk
V_{CC} = 35 V
t_P = 1.0 ms
D = 10%
f = 1090 MHz

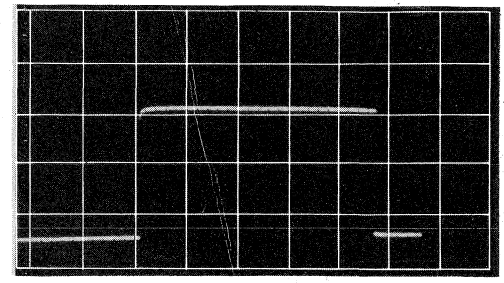
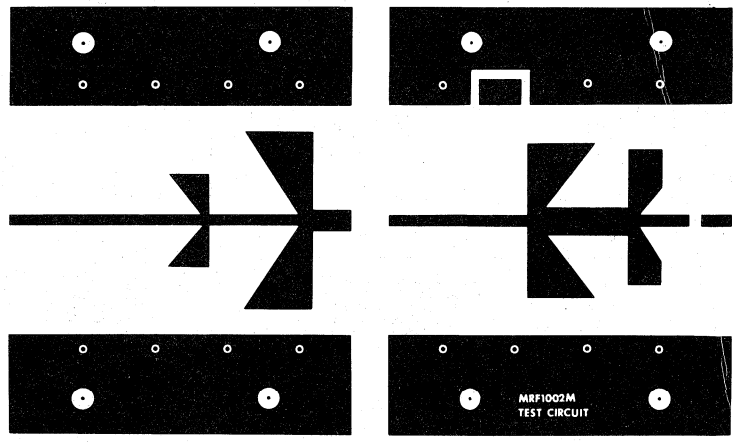


FIGURE 9 – PRINTED CIRCUIT BOARD LAYOUT – 1090 MHz TEST CIRCUIT



NOTE: The Printed Circuit Board shown is 75% of the original.

MRF1004MA
MRF1004MB
MRF1004MC

The RF Line

4.0 W 960-1215 MHz

MICROWAVE POWER TRANSISTOR

NPN SILICON

MICROWAVE PULSE POWER TRANSISTOR

. . . designed for Class B and C *common base* amplifier applications in short and long pulse TACAN, IFF, DME, and radar transmitters.

- Guaranteed Performance @ 1090 MHz , 35 Vdc
  Output Power = 4.0 Watts Peak
  Minimum Gain = 10 dB
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Industry Standard Package
- Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Compatible with Other 1004M Types
- Internal Input Matching for Broadband Operation

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CBO}	50	Vdc
Emitter-Base Voltage	V_{EBO}	3.5	Vdc
Collector-Current — Continuous	I_C	250	mAdc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	7.0 40	Watts mW/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

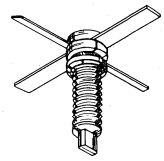
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	25	°C/W

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

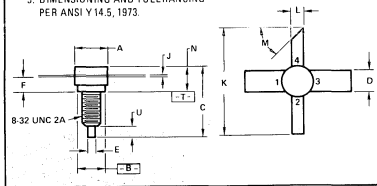
MRF1004MA
CASE 332-01



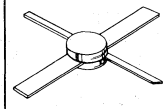
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.01	7.62	0.276	0.300
B	6.20	6.50	0.244	0.256
C	16.26	16.76	0.640	0.660
D	4.95	5.21	0.195	0.205
E	1.40	1.65	0.055	0.065
F	2.92	3.43	0.115	0.135
J	0.08	0.18	0.003	0.007
K	15.24	–	0.600	–
L	2.41	2.67	0.095	0.105
M	45° Nom		45° Nom	
N	5.08	5.46	0.200	0.215
U	2.92	3.68	0.115	0.145

NOTES:
1. DIM [B] IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ 0.76(0.030)Ⓜ T BⓂ
3. [-T-] IS SEATING PLANE.
4. DIMENSION K APPLIES TWO PLACES.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR



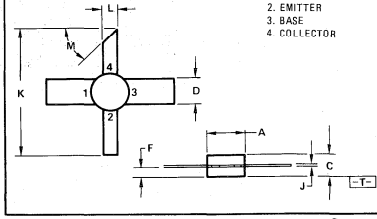
MRF1004MB
CASE 332A-01



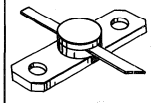
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.01	7.62	0.276	0.300
B	6.20	6.50	0.244	0.256
C	3.30	3.81	0.130	0.150
D	4.95	5.21	0.195	0.205
F	1.40	1.78	0.055	0.070
J	0.08	0.18	0.003	0.007
K	15.24	–	0.600	–
L	2.41	2.67	0.095	0.105
M	45° NOM		45° NOM	

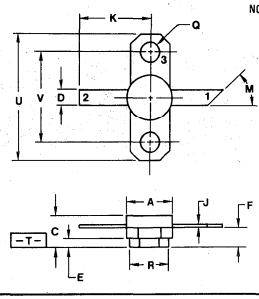
NOTES:
1. DIM [A] IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ 0.76 (0.030) Ⓜ T A Ⓜ
3. [-T-] IS SEATING PLANE.
4. DIM K APPLIES 2 PLACES.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR



MRF1004MC
CASE 361A-01





STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

NOTES:
1. DIMENSIONS R AND U ARE DATUMS AND T IS A DATUM SURFACE AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR MOUNTING HOLES:
   ⌖ ∅ 0.38 (0.015) Ⓜ T U Ⓜ R Ⓜ
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

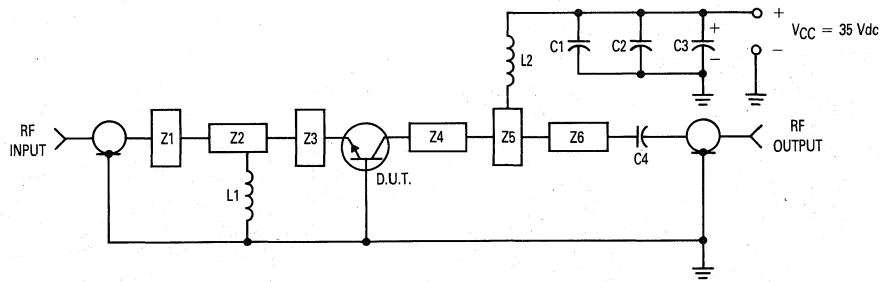
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.06	7.26	0.278	0.286
C	4.44	5.20	0.175	0.205
D	2.36	2.71	0.093	0.107
E	1.39	1.77	0.055	0.070
F	2.66	3.42	0.105	0.135
J	0.10	0.15	0.004	0.006
K	11.04	–	0.435	–
M	45° NOM		45° NOM	
Q	3.04	34.2	0.120	0.135
R	6.09	6.66	0.240	0.260
U	20.06	20.57	0.790	0.810
V	14.27 BSC		0.562 BSC	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	50	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 5.0 mAdc, I_E = 0)	$V_{(BR)CBO}$	50	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 35 Vdc, I_E = 0)	I_{CBO}	—	—	0.5	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 75 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	—	100	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 35 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	3.3	5.0	pF
FUNCTIONAL TESTS (Pulse Width = 10 μs, Duty Cycle = 1.0%)					
Common-Base Amplifier Power Gain (V_{CC} = 35 Vdc, P_{out} = 4.0 W pk, f = 1090 MHz)	G_{PB}	10	11	—	dB
Collector Efficiency (V_{CC} = 35 Vdc, P_{out} = 4.0 W pk, f = 1090 MHz)	η	40	45	—	%
Load Mismatch (V_{CC} = 35 Vdc, P_{out} = 4.0 W pk, f = 1090 MHz VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Power Output			

3

FIGURE 1. 1090 MHz TEST CIRCUIT



L1, L2 — 3 Turns #18 AWG, 1/8" ID
C1 — 0.1 μF
C2, C4 — 220 pF Chip Capacitor
C3 — 20 μF, 50 V Electrolytic
Board Material — 0.031" Thick Glass Teflon
Z1–Z6 Distributed Microstrip Elements — See Figure 9

FIGURE 2 – OUTPUT POWER versus INPUT POWER

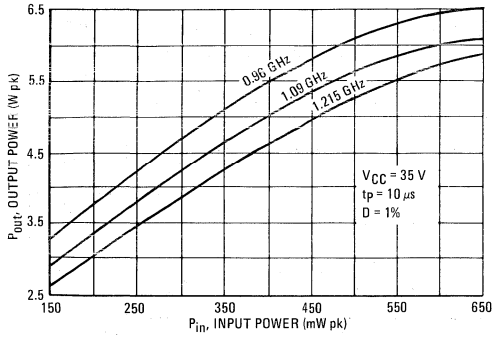


FIGURE 3 – OUTPUT POWER versus FREQUENCY

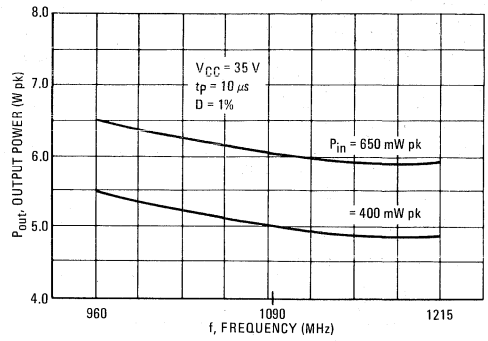


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

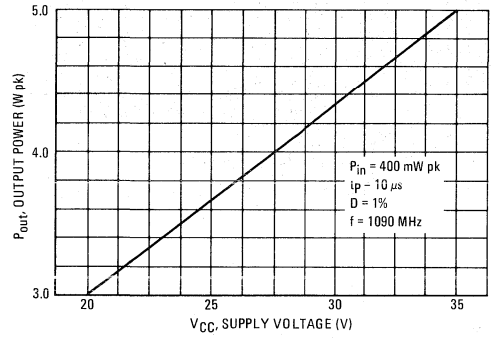


FIGURE 5 – POWER GAIN versus FREQUENCY

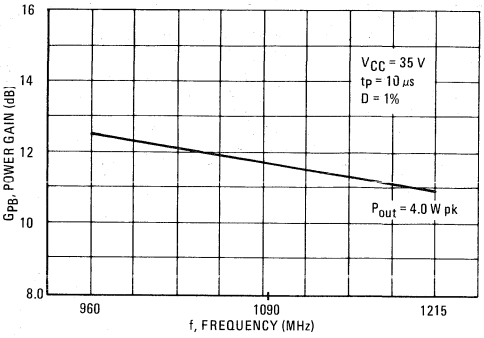
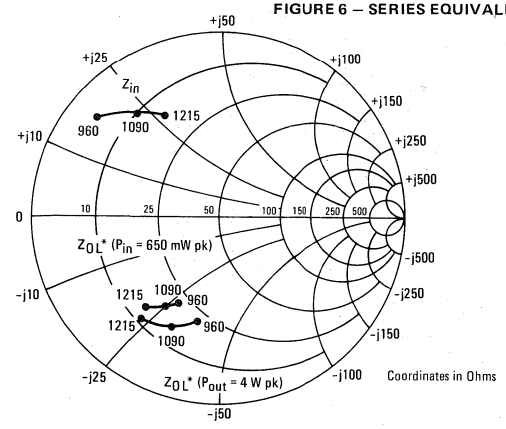


FIGURE 6 – SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCE



f MHz	Z_{in} Ohms	Z_{OL}* (P_{in} = 400 mW pk) Ohms	Z_{OL}* (P_{out} = 4 W pk) Ohms
960	5.0 + 17.5	23.5 – j26	22.5 – j36
1090	10 + j23	18.5 – j25	15 – j32.5
1215	16 + j29.5	15.5 – j23.5	11 – j23

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

FIGURE 7 – 1090 MHz TEST AMPLIFIER

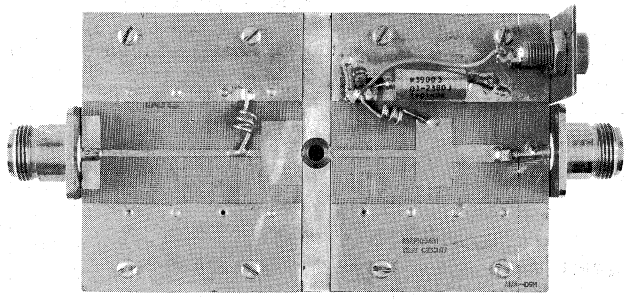


FIGURE 8 – TYPICAL LONG PULSE PERFORMANCE

P_{out} = 4.0 W pk
V_{CC} = 35 V
t_P = 1.0 ms
D = 10%
f = 1090 MHz

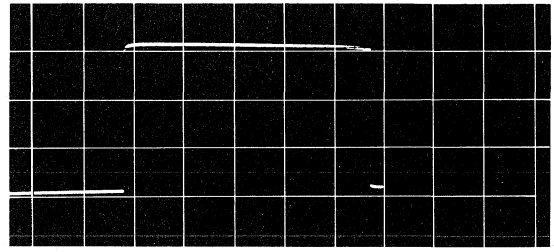
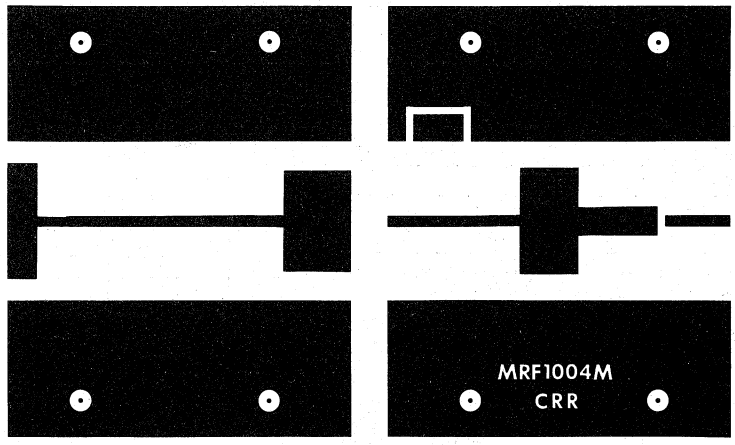


FIGURE 9 – PRINTED CIRCUIT BOARD LAYOUT – 1090 MHz TEST CIRCUIT



NOTE: The Printed Circuit Board shown is 75% of the original.

MRF1008MA
MRF1008MB
MRF1008MC

The RF Line

8.0 W PEAK 960-1215 MHz

MICROWAVE POWER TRANSISTOR

NPN SILICON

MICROWAVE PULSE POWER TRANSISTOR

. . . designed for Class B and C *common-base* amplifier applications in short and long pulse TACAN, IFF, DME, and radar transmitters.

- Guaranteed Performance @ 1090 MHz, 35 Vdc
  Output Power = 8.0 Watts Peak
  Minimum Gain = 10 dB
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Industry Standard Package
- Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Compatible with Other 1008M Types
- Internal Input Matching for Broadband Operation

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CBO}	50	Vdc
Emitter-Base Voltage	V_{EBO}	3.5	Vdc
Collector-Current — Continuous	I_C	500	mAdc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	11.6 67	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

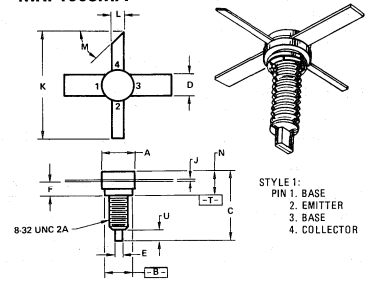
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	15	°C/W

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

MRF1008MA



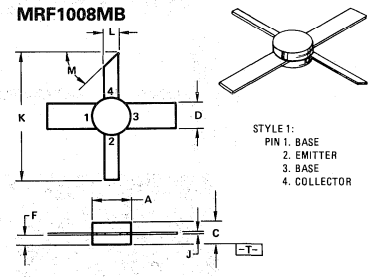
STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	7.01	7.62	0.276	0.300
B	6.20	6.50	0.244	0.256
C	16.26	16.76	0.640	0.660
D	4.95	5.21	0.195	0.205
E	1.40	1.65	0.055	0.065
F	2.92	3.43	0.115	0.135
J	0.08	0.18	0.003	0.007
K	15.24	–	0.600	–
L	2.41	2.67	0.095	0.105
M	45° Nom		45° Nom	
N	5.08	5.46	0.200	0.215
U	2.92	3.68	0.115	0.145

NOTES:
1. DIM [B] IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:
   [⌖] 0.76(0.030)Ⓜ [T] [B]Ⓜ
3. [T] IS SEATING PLANE.
4. DIMENSION K APPLIES TWO PLACES.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

CASE 332-01

MRF1008MB



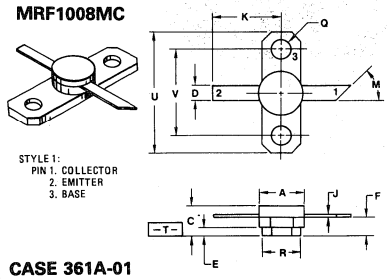
STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR

NOTES:
1. DIM [A] IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:
   [⌖] 0.76 (0.030)Ⓜ [T] [A]Ⓜ
3. [T] IS SEATING PLANE.
4. DIM K APPLIES 2 PLACES.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	7.01	7.62	0.276	0.300
B	6.20	6.50	0.244	0.256
C	3.30	3.81	0.130	0.150
D	4.95	5.21	0.195	0.205
F	1.40	1.78	0.055	0.070
J	0.08	0.18	0.003	0.007
K	15.24	–	0.600	–
L	2.41	2.67	0.095	0.105
M	45° NOM		45° NOM	

CASE 332A-01

MRF1008MC



STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

NOTES:
1. DIMENSIONS R AND U ARE DATUMS AND T IS A DATUM SURFACE AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR MOUNTING HOLES:
   [⌖] ø 0.38 (0.015)Ⓜ [T] [U]Ⓜ [R]Ⓜ
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	7.06	7.26	0.278	0.286
C	4.44	5.20	0.175	0.205
D	2.36	2.71	0.093	0.107
E	1.39	1.77	0.055	0.070
F	2.66	3.42	0.105	0.135
J	0.10	0.15	0.004	0.006
K	11.04	–	0.435	–
M	45° NOM		45° NOM	
Q	3.04	34.2	0.120	0.135
R	6.09	6.66	0.240	0.260
U	20.06	20.57	0.790	0.810
V	14.27 BSC		0.562 BSC	

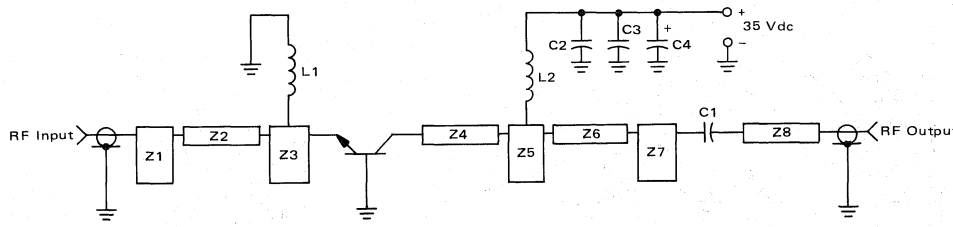
CASE 361A-01

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	50	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 5.0 mAdc, I_E = 0)	$V_{(BR)CBO}$	50	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 35 Vdc, I_E = 0)	I_{CBO}	—	—	0.5	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 150 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	—	100	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 35 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	3.5	6.0	pF
FUNCTIONAL TESTS (Pulse Width = 10 μs, Duty Cycle =1%)					
Common-Base Amplifier Power Gain (V_{CC} = 35 Vdc, P_{out} = 8.0 W Peak, f = 1090 MHz)	G_{PB}	10	12	—	dB
Collector Efficiency (V_{CC} = 35 Vdc, P_{out} = 8.0 W Peak, f = 1090 MHz)	η	40	45	—	%
Load Mismatch (V_{CC} = 35 Vdc, P_{out} = 8.0 W Peak, f = 1090 MHz, VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Output Power			

3

FIGURE 1 – 1090 MHz TEST CIRCUIT



C1, C2 – 220 pF 100 mil Chip Capacitor
C3 – 0.1 μF
C4 – 10 μF/50 V Electrolytic Capacitor

L1, L2 – 3 Turns #18 AWG, 1/8" ID
Z1 – Z8 – Microstrip, See Photomaster
Board Material – 0.031" Glass Teflon, ϵ_r = 2.5

FIGURE 2 – OUTPUT POWER versus INPUT POWER

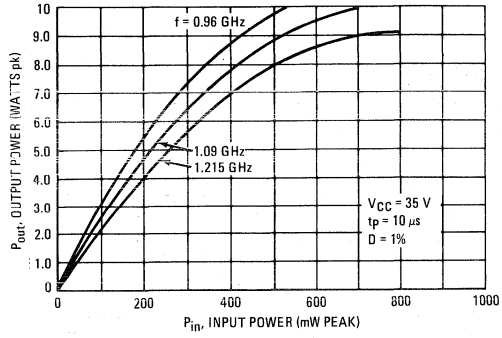


FIGURE 3 – OUTPUT POWER versus FREQUENCY

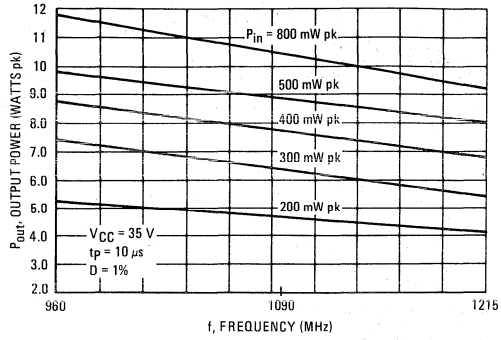


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

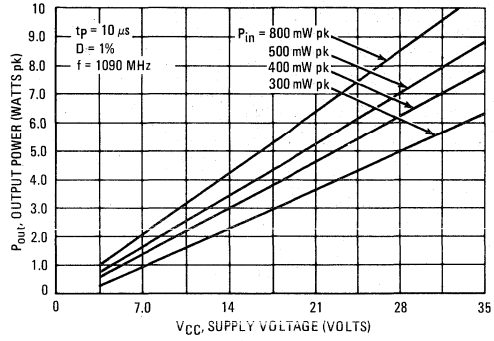


FIGURE 5 – POWER GAIN versus FREQUENCY

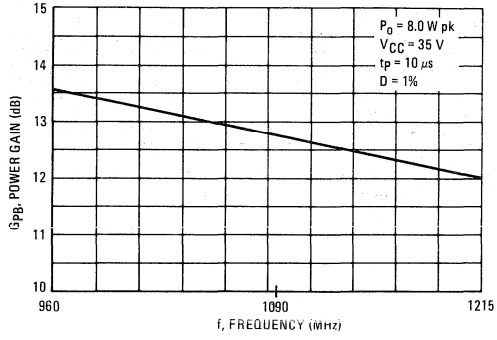
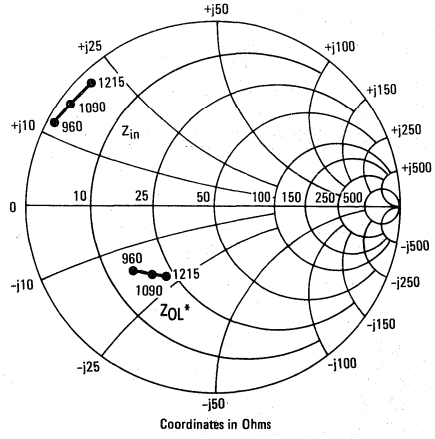


FIGURE 6 – SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCES



VCC = 35 V
Po = 8.0 W pk

f MHz	Zin Ohms	*ZOL Ohms
960	1.5 + j13	17 – j16
1090	2.0 + j17	20 – j18.5
1215	3.0 + j20	23 – j20

*ZOL = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

FIGURE 7–1090 MHz TEST AMPLIFIER

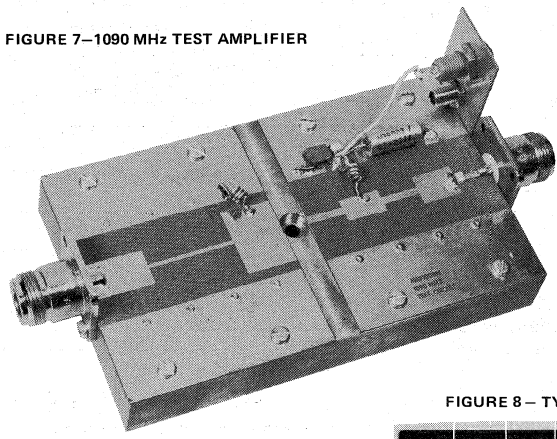


FIGURE 8 – TYPICAL LONG PULSE PERFORMANCE

P_{out} = 8.0 W peak
V_{CC} = 35 V
t_P = 1 ms
D = 10%
f = 1090 MHz

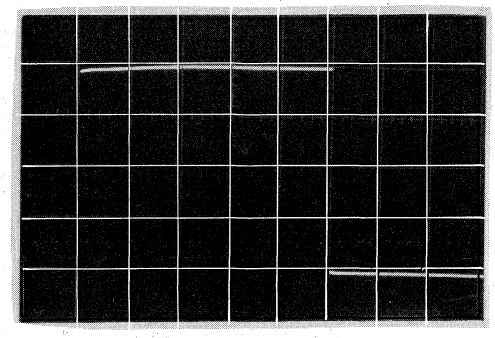
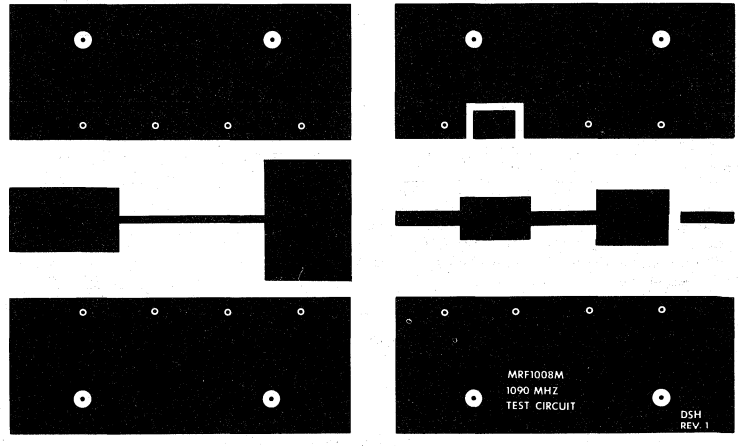


FIGURE 9–PRINTED CIRCUIT BOARD LAYOUT–1090 MHz TEST CIRCUIT



NOTE: The Printed Circuit Board shown is 75% of the original.

o Soldered Eyelet

3

MRF1015MA
MRF1015MB
MRF1015MC

The RF Line

15 W PEAK 960-1215 MHz

MICROWAVE POWER TRANSISTOR

NPN SILICON

MICROWAVE PULSE POWER TRANSISTOR

. . . designed for Class B and C *common base* amplifier applications in short and long pulse TACAN, IFF, DME, and radar transmitters.

- Guaranteed Performance @ 1090 MHz, 50 Vdc
  Output power = 15 Watts Peak
  Minimum Gain = 10 dB
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Industry Standard Package
- Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Compatible with Other 1015M Types
- Internal Input Matching for Broadband Operation

3

MAXIMUM RATINGS

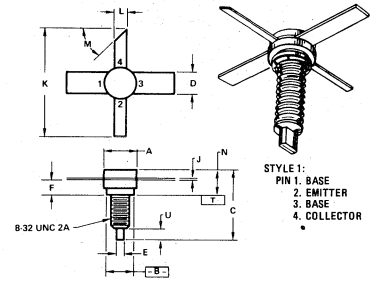
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CES}	60	Vdc
Collector-Base Voltage	V_{CBO}	60	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Continuous	I_C	1.0	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	17.5 100	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	10	°C/W

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.
(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

MRF1015MA

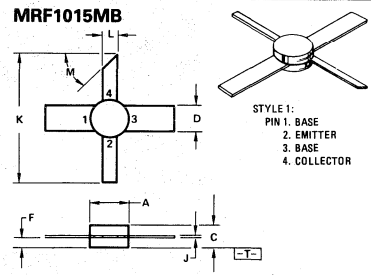


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.01	7.62	0.276	0.300
B	6.20	6.50	0.244	0.256
C	16.26	16.76	0.640	0.660
D	4.95	5.21	0.195	0.205
E	1.40	1.65	0.055	0.065
F	2.92	4.32	0.115	0.170
J	0.08	0.18	0.003	0.007
K	15.24	–	0.600	–
L	2.41	2.67	0.095	0.105
M	45° Nom		45° Nom	
N	4.57	6.22	0.180	0.245
U	2.92	3.68	0.115	0.145

NOTES:
1. DIM B IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ 0.76(0.030) Ⓜ T B Ⓜ
3. T IS SEATING PLANE.
4. DIMENSION K APPLIES TWO PLACES.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

CASE 332-03

MRF1015MB

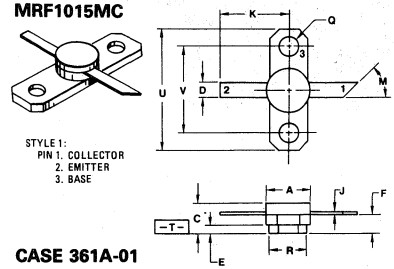


NOTES:
1. DIM A IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ 0.76 (0.030) Ⓜ T A Ⓜ
3. T IS SEATING PLANE.
4. DIM K APPLIES 2 PLACES.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.01	7.62	0.276	0.300
C	3.30	3.81	0.130	0.150
D	4.95	5.21	0.195	0.205
F	1.40	1.78	0.055	0.070
J	0.08	0.18	0.003	0.007
K	15.24	–	0.600	–
L	2.41	2.67	0.095	0.105
M	45° NOM		45° NOM	

CASE 332A-01

MRF1015MC



NOTES:
1. DIMENSIONS R AND U ARE DATUMS AND T IS A DATUM SURFACE AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR MOUNTING HOLES:
   ⌖ ∅ 0.38 (0.015) Ⓜ T U Ⓜ R Ⓜ
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.06	7.26	0.278	0.286
C	4.44	5.20	0.175	0.205
D	2.36	2.71	0.093	0.107
E	1.39	1.77	0.055	0.070
F	2.66	3.42	0.105	0.135
J	0.10	0.15	0.004	0.006
K	11.04	–	0.435	–
M	45° NOM		45° NOM	
Q	3.04	34.2	0.120	0.135
R	6.09	6.86	0.240	0.260
U	20.06	20.57	0.790	0.810
V	14.27 BSC		0.562 BSC	

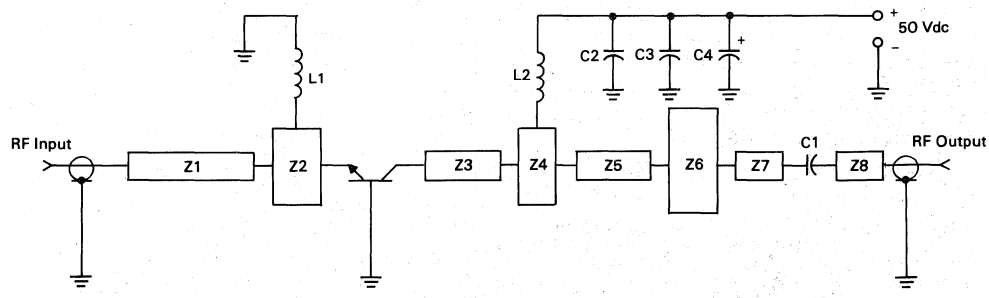
CASE 361A-01

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 10 mAdc, I_E = 0)	$V_{(BR)CBO}$	60	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0)	I_{CBO}	—	—	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	40	100	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 50 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	5.0	7.5	pF
FUNCTIONAL TESTS (Pulse Width = 10 μs, Duty Cycle = 1%)					
Common-Base Amplifier Power Gain (V_{CC} = 50 Vdc, P_{out} = 15 W Peak, f = 1090 MHz)	G_{PB}	10	12.5	—	dB
Collector Efficiency (V_{CC} = 50 Vdc, P_{out} = 15 W Peak, f = 1090 MHz)	η	30	35		%
Load Mismatch (V_{CC} = 50 Vdc, P_{out} = 15 W Peak, f = 1090 MHz) (VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Power Output			

3

FIGURE 1 — 1090 MHz TEST CIRCUIT



C1, C2 — 220 pF 100 mil Chip Capacitor
C3 — 0.1 μF
C4 — 47 μF/75 V Electrolytic Capacitor
L1, L2 — 3 Turns #18 AWG, 1/8" ID
Z1-Z8 — Microstrip, See Photomaster, Figure 8
Board Material — 0.032" Glass Teflon
ϵ_r = 2.5

FIGURE 2 — OUTPUT POWER versus INPUT POWER

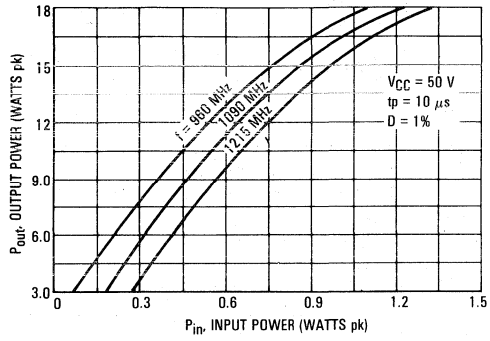


FIGURE 3 — OUTPUT POWER versus FREQUENCY

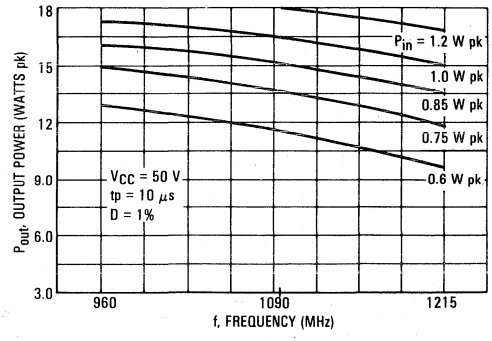


FIGURE 4 - OUTPUT POWER versus SUPPLY VOLTAGE

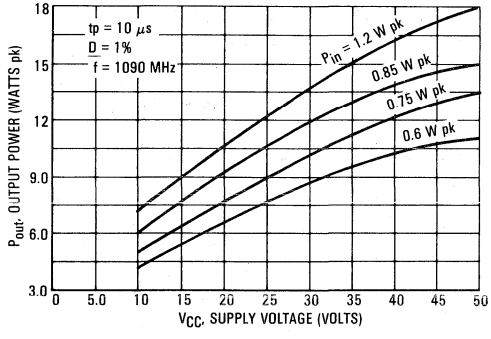


FIGURE 5 — POWER GAIN versus FREQUENCY

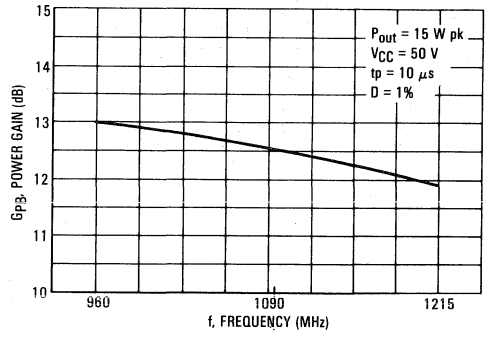
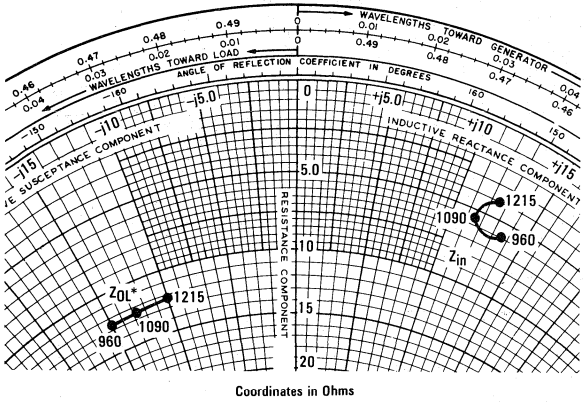


FIGURE 6 — SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCES



Coordinates in Ohms

P_{out} = 15 W pk V_{CC} = 50 V
tp = 10 μs D = 1%

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
960	5.9 + j13.6	12.5 – j15
1090	5.5 + j11.5	12.4 – j12.8
1215	4.0 + j12.5	12.1 – j10

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

FIGURE 7 — 1090 MHz TEST AMPLIFIER

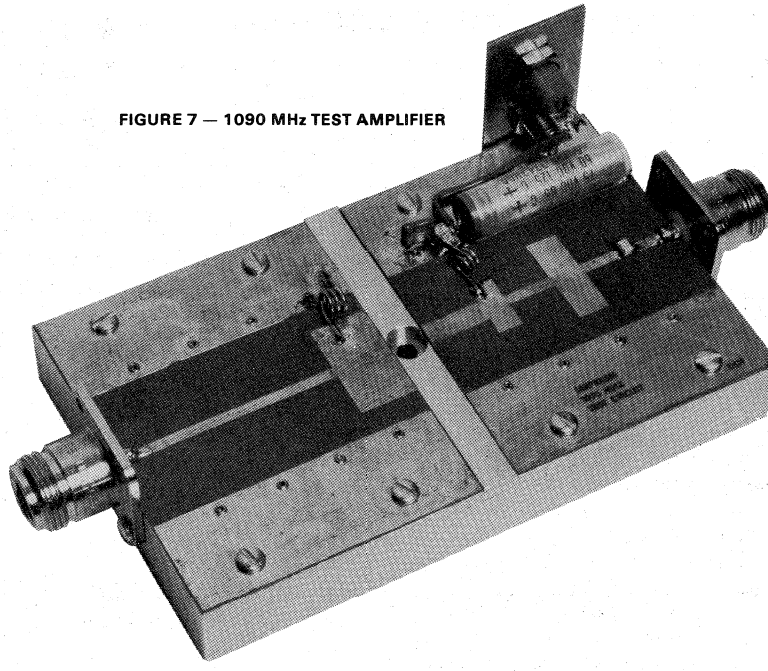
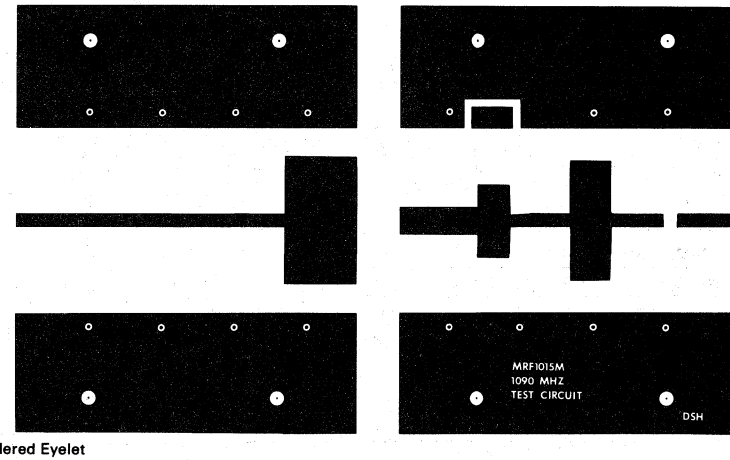


FIGURE 8 — PRINTED CIRCUIT BOARD LAYOUT — 1090 MHz TEST CIRCUIT



⊙ Soldered Eyelet
⊙ 4–40 Screw Placement

NOTE: The Printed Circuit Board shown is 75% of the original.

MRF1035MA
MRF1035MB
MRF1035MC

The RF Line

35 W PEAK — 960-1215 MHz

MICROWAVE POWER TRANSISTOR

NPN SILICON

MICROWAVE PULSE POWER TRANSISTOR

. . . designed for Class B and C *common-base* amplifier applications in short and long pulse TACAN, IFF, DME, and radar transmitters.

- Guaranteed Performance @ 1090 MHz, 50 Vdc
  Output Power = 35 Watts Peak
  Minimum Gain = 10 dB
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Industry Standard Package
- Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Compatible with Other 1035M Types
- Internal Input Matching for Broadband Operation

3

MAXIMUM RATINGS

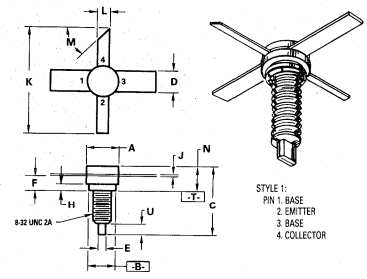
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CES}	60	Vdc
Collector-Base Voltage	V_{CBO}	60	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Continuous	I_C	2.0	Adc
Total Device Dissipation @ T_C = 25°C(1) Derate above 25°C	P_D	35 200	Watts mW/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	5.0	°C/W

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.
(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

MRF1035MA

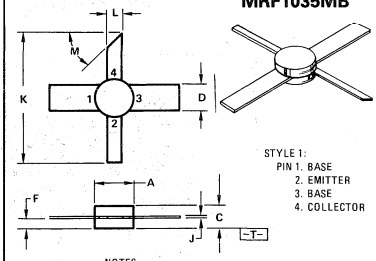


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	6.86	7.62	0.270	0.300
B	6.10	6.60	0.240	0.260
C	16.26	16.76	0.640	0.660
D	4.95	5.21	0.195	0.205
E	1.40	1.65	0.055	0.065
F	2.67	4.32	0.105	0.170
H	1.40	1.65	0.055	0.065
J	0.08	0.18	0.003	0.007
K	15.24	—	0.600	—
L	2.41	2.67	0.095	0.105
M	45° Nom		45° Nom	
N	4.57	6.22	0.180	0.245
U	2.92	3.68	0.115	0.145

NOTES:
1. DIM B IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS.
   ⌖ 0.76 (0.030) M T B M
3. T IS SEATING PLANE.
4. DIMENSION K APPLIES TWO PLACES.
5. DIMENSIONING AND TOLERANCING PER ANSI Y 14.5, 1973.

CASE 332-04

MRF1035MB

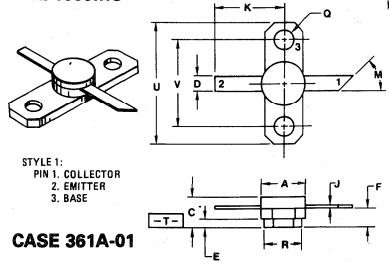


NOTES:
1. DIM A IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ 0.76 (0.030) M T A M
3. T IS SEATING PLANE.
4. DIM K APPLIES 2 PLACES.
5. DIMENSIONING AND TOLERANCING PER ANSI Y 14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.01	7.62	0.276	0.300
B	6.20	6.50	0.244	0.256
C	3.30	3.81	0.130	0.150
D	4.95	5.21	0.195	0.205
F	1.40	1.78	0.055	0.070
J	0.08	0.18	0.003	0.007
K	15.24	—	0.600	—
L	2.41	2.67	0.095	0.105
M	45° NOM		45° NOM	

CASE 332A-01

MRF1035MC



NOTES:
1. DIMENSIONS R AND U ARE DATUMS AND T IS A DATUM SURFACE AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR MOUNTING HOLES:
   ⌖ ⌀ 0.38 (0.015) M T U M R M
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

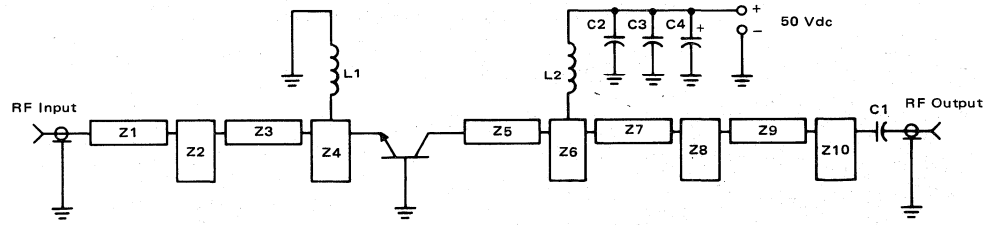
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.06	7.26	0.278	0.286
C	4.44	5.20	0.175	0.205
D	2.36	2.71	0.093	0.107
E	1.39	1.77	0.055	0.070
F	2.66	3.42	0.105	0.135
J	0.10	0.15	0.004	0.006
K	11.04	—	0.435	—
M	45° NOM		45° NOM	
Q	3.04	34.2	0.120	0.135
R	8.09	8.66	0.240	0.260
U	20.06	20.57	0.790	0.810
V	14.27 BSC		0.562 BSC	

CASE 361A-01

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 20 mAdc, I_E = 0)	$V_{(BR)CBO}$	60	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 2.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0)	I_{CBO}	–	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	40	100	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 50 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	10	15	pF
FUNCTIONAL TESTS (Pulse Width = 10 μs, Duty Cycle = 1%)					
Common-Base Amplifier Power Gain (V_{CC} = 50 Vdc, P_{out} = 35 W Peak, f = 1090 MHz)	G_{PB}	10	12.4	–	dB
Collector Efficiency (V_{CC} = 50 Vdc, P_{out} = 35 W Peak, f = 1090 MHz)	η	30	34	–	%
Load Mismatch (V_{CC} = 50 Vdc, P_{out} = 35 W Peak, f = 1090 MHz, VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Output Power			

FIGURE 1 – 1090 MHz TEST CIRCUIT



C1, C2 – 220 pF 100 mil Chip Capacitor
C3 – 0.1 μF
C4 – 10 μF/75 V Electrolytic
L1, L2 – 3 Turns #18 AWG, 1/8" ID

Z1–Z10 – Microstrip, See Photomaster
Board Material – 0.031" Glass Teflon
ϵ_R = 2.5

FIGURE 2 – OUTPUT POWER versus INPUT POWER

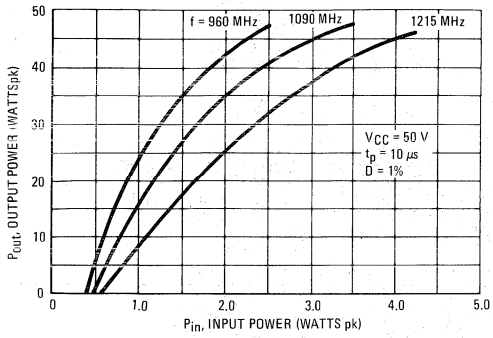


FIGURE 3 – OUTPUT POWER versus FREQUENCY

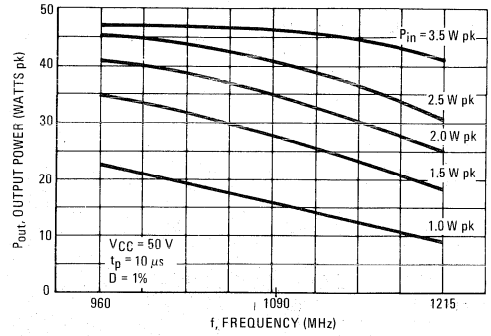


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

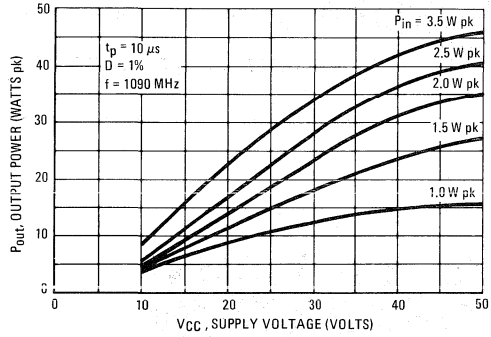


FIGURE 5 – POWER GAIN versus FREQUENCY

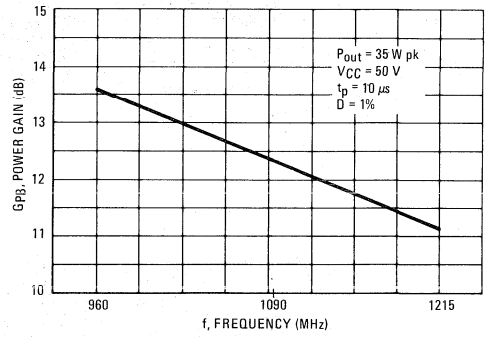
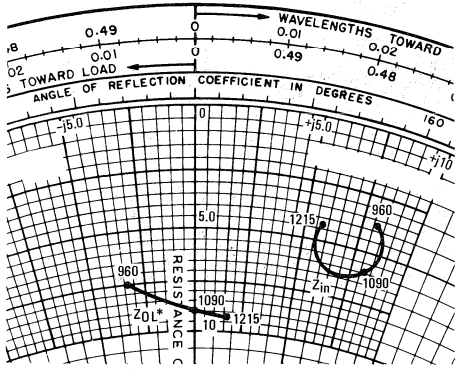


FIGURE 6 – SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCES



P_{out} = 35 W Pk V_{CC} = 50 V
t_p = 10 μs D = 1%

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
960	3.8 + j 8.2	7.5 – j 3.3
1090	6.0 + j 8.2	9.0 + j 0
1215	4.2 + j 5.7	9.1 + j 1.7

*Z_{OL} = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

FIGURE 7 – 1090 MHz TEST AMPLIFIER

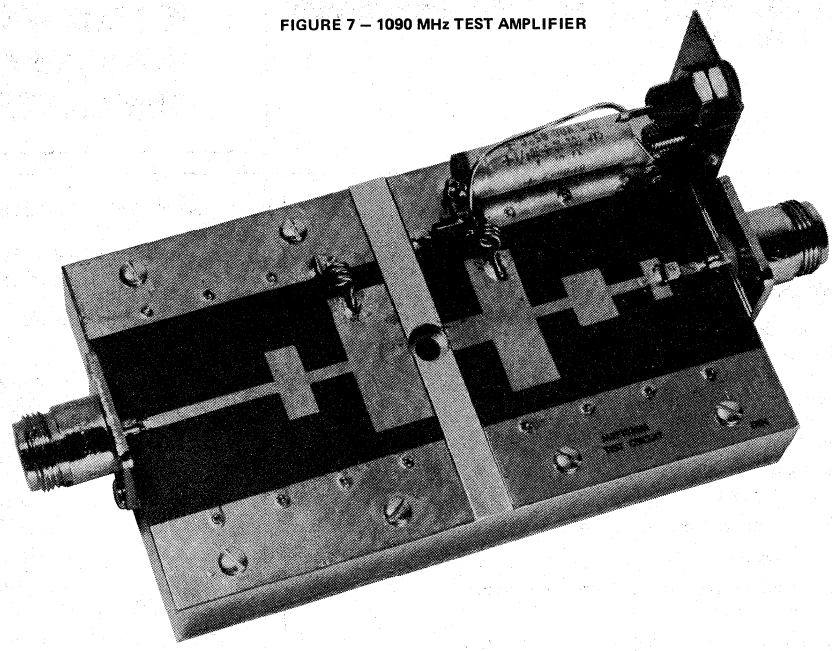
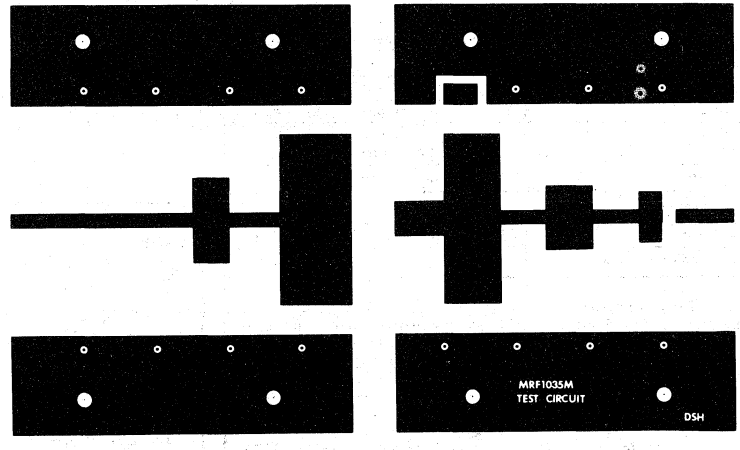


FIGURE 8 – PRINTED CIRCUIT BOARD LAYOUT – 1090 MHz TEST CIRCUIT



⊙ Soldered Eyelets

NOTE: The Printed Circuit Board shown is 75% of the original.

MRF1090MA
MRF1090MB
MRF1090MC

The RF Line

90 W PEAK, 960-1215 MHz

MICROWAVE POWER TRANSISTOR

NPN SILICON

MICROWAVE PULSE POWER TRANSISTOR

. . . designed for Class B and C *common base* amplifier applications in short pulse TACAN, IFF, and DME transmitters.

- Guaranteed Performance @ 1090 MHz, 50 Vdc
  Output power = 90 Watts Peak
  Minimum Gain = 8.4 dB
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Industry Standard Package
- Nitride Passivated
- Gold Metallized for Long Life and Resistance to Metal Migration
- Compatible with Other 1090M and 1075M Types
- Internal Input Matching for Broadband Operation

3

MAXIMUM RATINGS

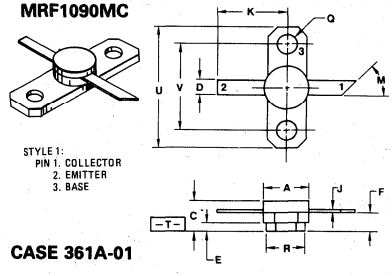
Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	70	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Peak (1)	I_C	6.0	Adc
Peak Device Dissipation @ T_C = 25°C (1) (2) Derate above 25°C	P_D	290 1.66	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (3)	$R_{\theta JC}$	0.6	°C/W

(1) Pulse Width = 10 μs, Duty Cycle = 1%.
(2) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF short pulse amplifiers.
(3) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

MRF1090MC



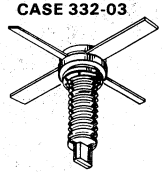
STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

CASE 361A-01

NOTES:
1. DIMENSIONS R AND U ARE DATUMS AND T IS A DATUM SURFACE AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR MOUNTING HOLES: ⌖ ∅ 0.38 (0.015) Ⓜ T U Ⓜ R Ⓜ
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.06	7.26	0.278	0.286
C	4.44	5.20	0.175	0.205
D	2.36	2.71	0.093	0.107
E	1.39	1.77	0.055	0.070
F	2.66	3.42	0.105	0.135
J	0.10	0.15	0.004	0.006
K	11.04	–	0.435	–
M	45° NOM		45° NOM	
Q	3.04	3.4.2	0.120	0.135
R	6.09	6.86	0.240	0.260
U	20.06	20.57	0.790	0.810
V	14.27 BSC		0.562 BSC	

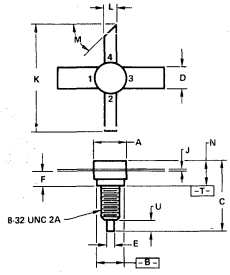
MRF1090MA
CASE 332-03



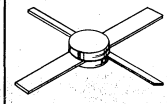
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.01	7.62	0.276	0.300
B	6.20	6.50	0.244	0.256
C	16.26	16.76	0.640	0.660
D	4.95	5.21	0.195	0.205
E	1.40	1.65	0.055	0.065
F	2.92	4.32	0.115	0.170
J	0.08	0.18	0.003	0.007
K	15.24	–	0.600	–
L	2.41	2.67	0.095	0.105
M	45° Nom		45° Nom	
N	4.57	6.22	0.180	0.245
U	2.92	3.68	0.115	0.145

NOTES.
1. DIM -B- IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS: ⌖ 0.76(0.030)Ⓜ T BⓂ
3. -T- IS SEATING PLANE.
4. DIMENSION K APPLIES TWO PLACES.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR



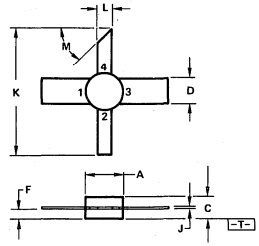
MRF1090MB
CASE 332A-01



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.01	7.62	0.276	0.300
C	3.30	3.81	0.130	0.150
D	4.95	5.21	0.195	0.205
F	1.40	1.78	0.055	0.070
J	0.08	0.18	0.003	0.007
K	15.24	–	0.600	–
L	2.41	2.67	0.095	0.105
M	45° NOM		45° NOM	

NOTES:
1. DIM -A- IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS: ⌖ 0.76 (0.030) Ⓜ T A Ⓜ
3. -T- IS SEATING PLANE.
4. DIM K APPLIES 2 PLACES.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR

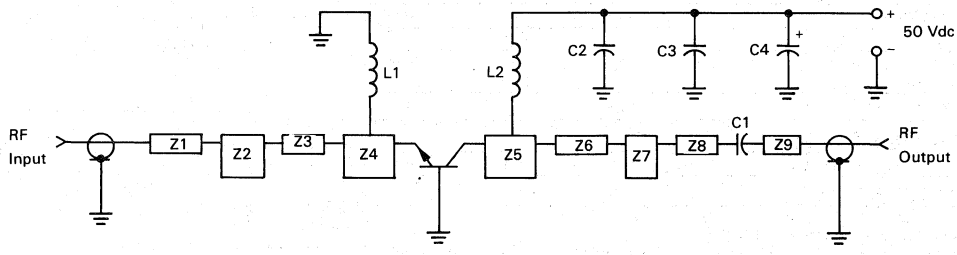


ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 25 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	70	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 25 mAdc, I_E = 0)	$V_{(BR)CBO}$	70	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0)	I_{CBO}	—	—	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain* (I_C = 2.5 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	30	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 50 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	12	16	pF
FUNCTIONAL TESTS (Pulse Width = 10 μs, Duty Cycle = 1.0%)					
Common-Base Amplifier Power Gain (V_{CC} = 50 Vdc, P_{out} = 90 W pk, f = 1090 MHz)	G_{PB}	8.4	10.8	—	dB
Collector Efficiency (V_{CC} = 50 Vdc, P_{out} = 90 W pk, f = 1090 MHz)	η	35	40	—	%
Load Mismatch (V_{CC} = 50 Vdc, P_{out} = 90 W pk, f = 1090 MHz) VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Power Output			

* 80 μs Pulse on Tektronix 576 or equivalent.

FIGURE 1 — 1090 MHz TEST CIRCUIT



C1, C2 — 220 pF Chip Capacitor, 100-mil ATC
C3 — 0.1 μF
C4 — 47 μF, 75 V
L1, L2 — 3 Turns, #18 AWG, 1/8″ ID
Z1–Z9 — Distributed Microstrip Elements — See Figure 9
Board Material — 0.031″ Thick Glass Teflon,
ϵ_r = 2.5

FIGURE 2 — OUTPUT POWER versus INPUT POWER

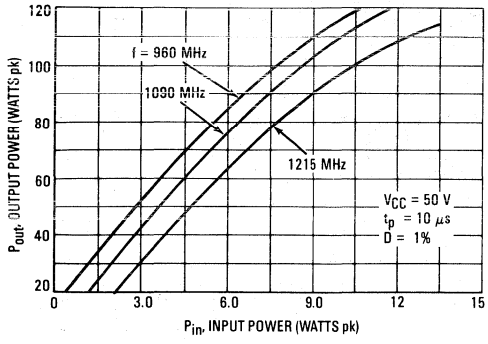


FIGURE 3 — OUTPUT POWER versus FREQUENCY

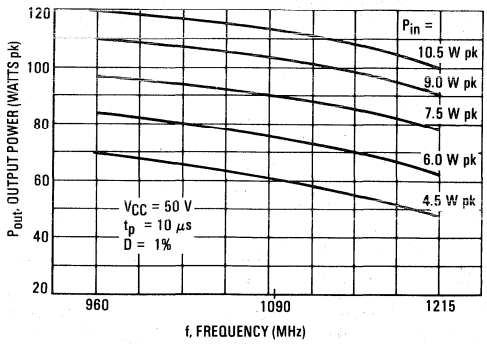


FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE

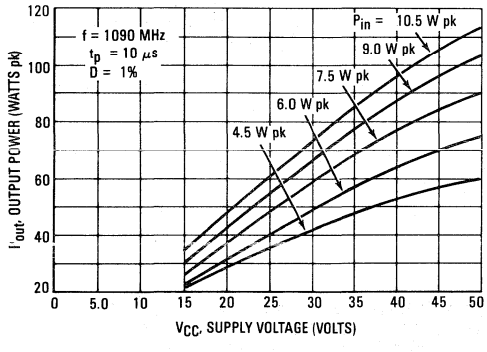


FIGURE 5 — POWER GAIN versus FREQUENCY

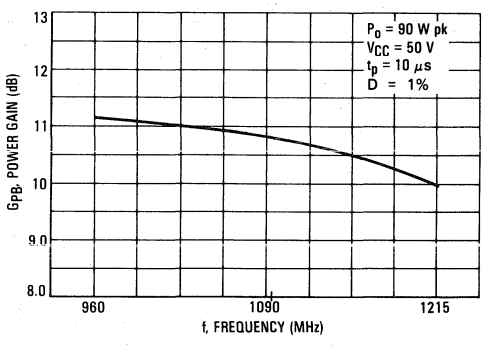
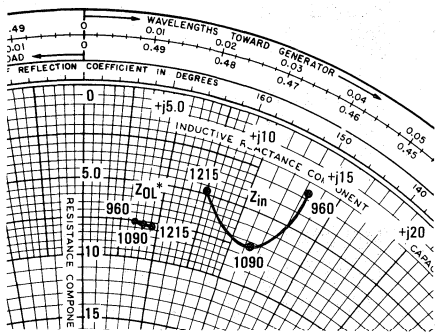


FIGURE 6 — SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCE



Coordinates in Ohms

P_{out} 90 W pk V_{CC} = 50 V
t_p = 10 μs D = 1%

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
960	2.8 + j13.2	7.6 + j3.5
1090	7.4 + j11.4	7.6 + j4.0
1215	4.7 + j7.5	7.7 + j4.5

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

FIGURE 7 — 1090 MHz TEST AMPLIFIER

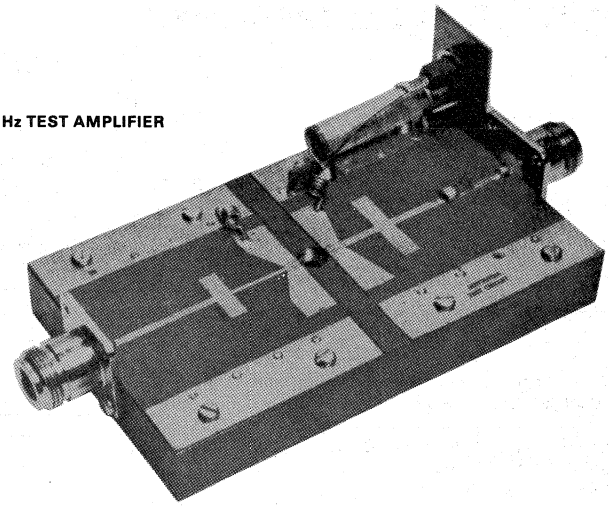


FIGURE 8 — TYPICAL PULSE PERFORMANCE

P_{out} = 90 W pk
V_{CC} = 50 V
t_p = 10 μs
D = 1%
f = 1090 MHz

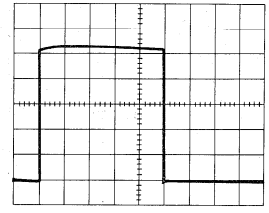
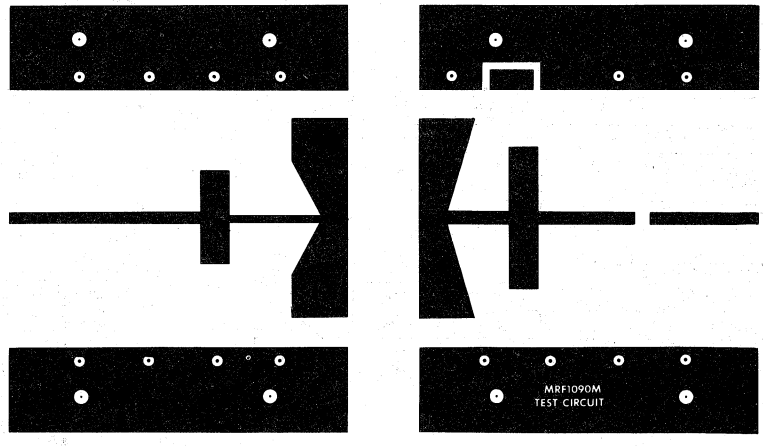


FIGURE 9 — PRINTED CIRCUIT BOARD LAYOUT — 1090 MHz TEST CIRCUIT



⊙ Soldered Eyelet
⊙ 4–40 Screw Placement

NOTE: The Printed Circuit Board shown is 75% of the original.

MRF1150M

The RF Line

150 W PEAK, 1020-1150 MHz

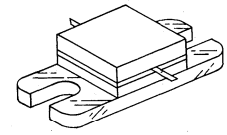
MICROWAVE POWER TRANSISTOR

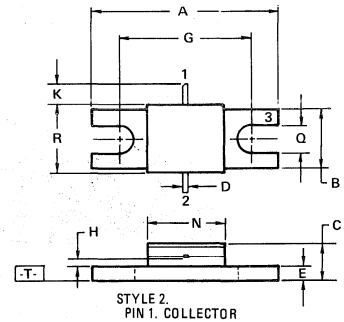
NPN SILICON

MICROWAVE PULSE POWER TRANSISTOR

. . . designed for Class B and C *common base* amplifier applications in short pulse TACAN, IFF, and DME transmitters.

- Guaranteed Performance @ 1090 MHz, 50 Vdc
  Output Power = 150 Watts Peak
  Minimum Gain = 7.8 dB
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Industry Standard Package
- Nitride Passivated
- Gold Metallized for Long Life and Resistance to Metal Migration
- Compatible with Other 1150M Types
- Internal Input and Output Matching for Broadband Operation





STYLE 2.
PIN 1. COLLECTOR
2. EMITTER
3. BASE

NOTES:
1. DIMENSIONS -A- AND -B- ARE DATUMS.
2. POSITIONAL TOLERANCE FOR MOUNTING HOLES:
   ⌖ .76(0.030) Ⓜ T A Ⓜ B Ⓜ
3. -T- IS SEATING PLANE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.61	23.11	0.890	0.910
B	9.65	9.91	0.380	0.390
C	4.06	5.84	0.160	0.230
D	0.51	0.76	0.020	0.030
E	1.40	1.65	0.055	0.065
G	16.51 BSC		0.650 BSC	
H	1.14	1.77	0.045	0.070
K	2.54	–	0.100	–
N	9.91	10.41	0.390	0.410
Q	3.00	3.61	0.118	0.142
R	9.91	10.41	0.390	0.410

CASE 336-03

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	70	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Peak (1, 2)	I_C	12	Adc
Peak Device Dissipation @ T_C = 25°C (1, 2) Derate above 25°C	P_D	583 3.33	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (1,2,3)	$R_{\theta JC}$	0.3	°C/W

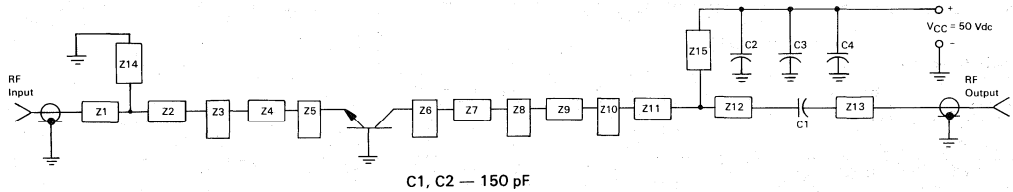
(1) Pulse Width = 10 μs, Duty Cycle = 1%.
(2) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF short pulse amplifiers.
(3) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	70	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 50 mAdc, I_E = 0)	$V_{(BR)CBO}$	70	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0)	I_{CBO}	—	—	10	mAdc
ON CHARACTERISTICS					
DC Current Gain* (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	30	—	—
FUNCTIONAL TESTS (Pulse Width = 10 μs, Duty Cycle = 1.0%)					
Common-Base Amplifier Power Gain (V_{CC} = 50 Vdc, P_{out} = 150 W pk, f = 1090 MHz)	G_{PB}	7.8	8.7	—	dB
Collector Efficiency (V_{CC} = 50 Vdc, P_{out} = 150 W pk, f = 1090 MHz)	η	33	—	—	%
Load Mismatch (V_{CC} = 50 Vdc, P_{out} = 150 W pk, f = 1090 MHz, VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Power Output			

*80 μs Pulse on Tektronix 576 or equivalent.

FIGURE 1 — 1090 MHz TEST CIRCUIT



C1, C2 — 150 pF
C3 — 0.1 μF/100 V
C4 — 47 μF/75 V, Electrolytic
Z1–Z15 — Distributed Microstrip Elements
Board Material — 0.0031″ Thick Teflon-Fiberglass
ϵ_r = 2.55

FIGURE 2 — OUTPUT POWER versus INPUT POWER

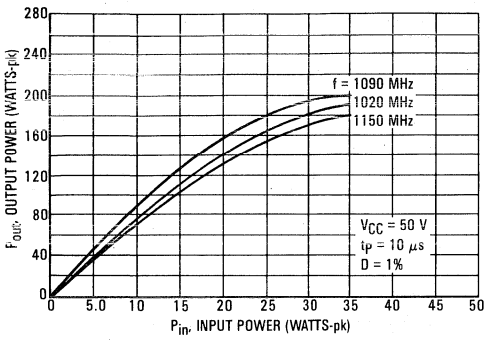


FIGURE 3 — OUTPUT POWER versus FREQUENCY

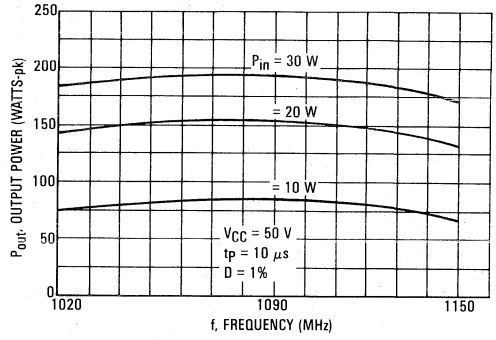


FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE

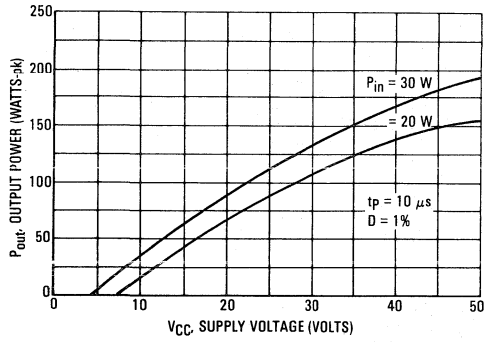
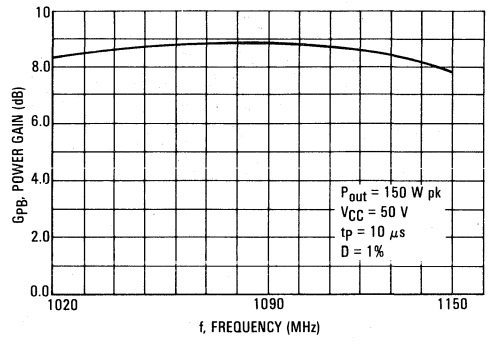


FIGURE 5 — POWER GAIN versus FREQUENCY



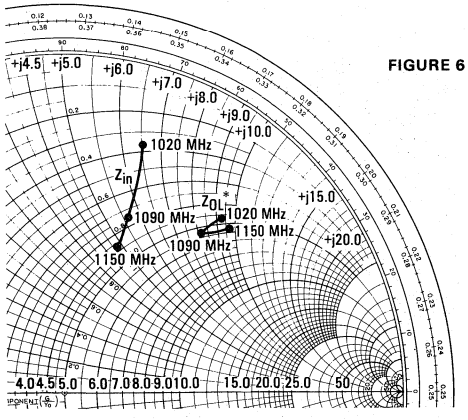


FIGURE 6 — SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCE

P_{out} = 150 W-pk V_{CC} = 50 V
t_P = 10 μs D = 1%

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
1020	1.85 + j6.6	4.6 + j9.4
1090	3.5 + j5.7	5.3 + j8.1
1150	4.4 + j4.8	5.2 + j9.7

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

FIGURE 7 — OUTPUT POWER, INPUT VSWR, POWER GAIN versus FREQUENCY

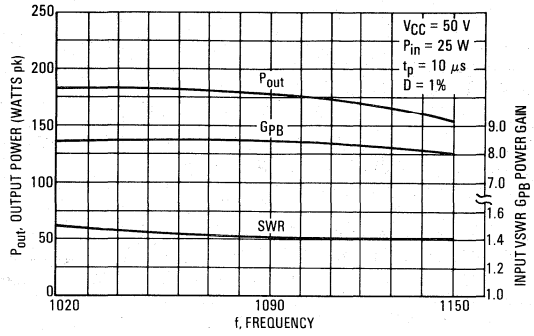


FIGURE 8 — 1090 MHz TEST CIRCUIT

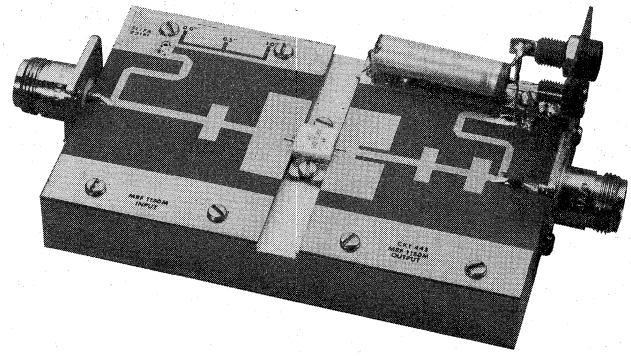
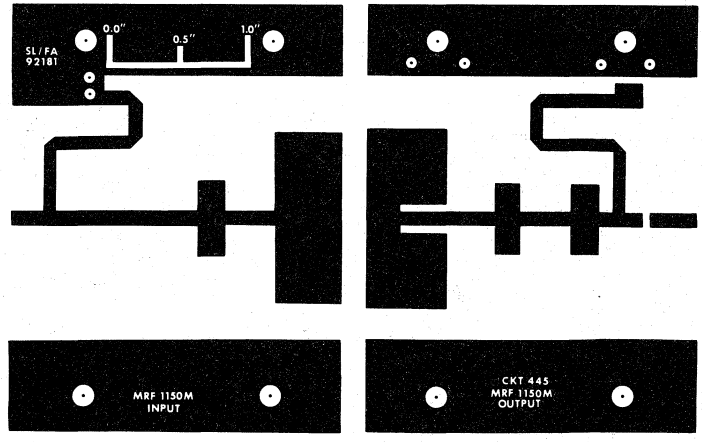


FIGURE 9 — 1090 MHz PHOTOMASTER



NOTE: The Printed Circuit Board shown is 75% of the original.

MRF1150MA
MRF1150MB
MRF1150MC

The RF Line

150 W PEAK, 960-1215 MHz

MICROWAVE POWER TRANSISTOR

NPN SILICON

MICROWAVE PULSE POWER TRANSISTOR

. . . designed for Class B and C *common base* amplifier applications in short pulse TACAN, IFF, and DME transmitters.

- Guaranteed Performance @ 1090 MHz, 50 Vdc
  Output power = 150 Watts Peak
  Minimum Gain = 7.8 dB
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Industry Standard Package
- Nitride Passivated
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Compatible with Other 1150M Types
- Internal Input Matching for Broadband Operation

3

MAXIMUM RATINGS

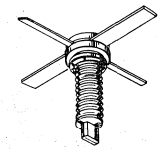
Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	70	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Peak (1)	I_C	12	Adc
Peak Device Dissipation @ T_C = 25°C (1) (2) Derate above 25°C	P_D	583 3.33	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (3)	$R_{\theta JC}$	0.3	°C/W

(1) Pulse Width = 10 μs, Duty Cycle = 1%.
(2) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF short pulse amplifiers.
(3) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

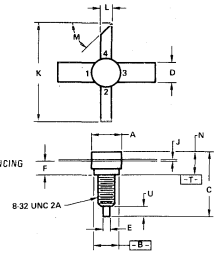
MRF1150MA
CASE 332-01



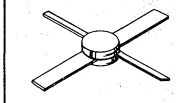
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.01	7.62	0.276	0.300
B	6.20	6.50	0.244	0.256
C	16.26	16.76	0.640	0.660
D	4.95	5.21	0.195	0.205
E	1.40	1.65	0.055	0.065
F	2.92	3.43	0.115	0.135
J	0.08	0.18	0.003	0.007
K	15.24	–	0.600	–
L	2.41	2.67	0.095	0.105
M	45° Nom		45° Nom	
N	5.08	5.46	0.200	0.215
U	2.92	3.68	0.115	0.145

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR

NOTES:
1. DIM [B] IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ 0.76(0.030)Ⓜ T B Ⓜ
3. [T] IS SEATING PLANE.
4. DIMENSION K APPLIES TWO PLACES.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.



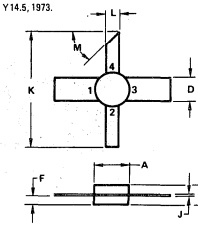
MRF1150MB
CASE 332A-01



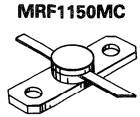
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.01	7.62	0.276	0.300
B	6.20	6.50	0.244	0.256
C	3.30	3.81	0.130	0.150
D	4.95	5.21	0.195	0.205
F	1.40	1.78	0.055	0.070
J	0.08	0.18	0.003	0.007
K	15.24	–	0.600	–
L	2.41	2.67	0.095	0.105
M	45° NOM		45° NOM	

NOTES:
1. DIM [A] IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ 0.76 (0.030) Ⓜ T A Ⓜ
3. [T] IS SEATING PLANE.
4. DIM K APPLIES 2 PLACES.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

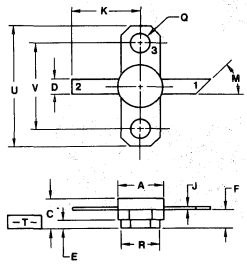
STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR



MRF1150MC



STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. BASE



CASE 361A-01

NOTES:
1. DIMENSIONS R AND U ARE DATUMS AND T IS A DATUM SURFACE AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR MOUNTING HOLES:
   ⌖ ∅ 0.38 (0.015) Ⓜ T U Ⓜ R Ⓜ
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

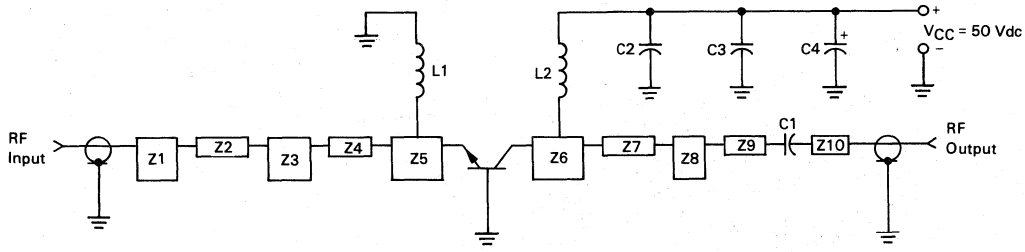
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.06	7.26	0.278	0.286
C	4.44	5.20	0.175	0.205
D	2.36	2.71	0.093	0.107
E	1.39	1.77	0.055	0.070
F	2.66	3.42	0.105	0.135
J	0.10	0.15	0.004	0.006
K	11.04	–	0.435	–
M	45° NOM		45° NOM	
Q	3.04	34.2	0.120	0.135
R	6.09	6.88	0.240	0.260
U	20.06	20.57	0.790	0.810
V	14.27 BSC		0.562 BSC	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	70	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 50 mAdc, I_E = 0)	$V_{(BR)CBO}$	70	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0)	I_{CBO}	—	—	10	mAdc
ON CHARACTERISTICS					
DC Current Gain* (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	30	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 50 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	25	32	pF
FUNCTIONAL TESTS (Pulse Width = 10 μs, Duty Cycle = 1.0%)					
Common-Base Amplifier Power Gain (V_{CC} = 50 Vdc, P_{out} = 150 W pk, f = 1090 MHz)	G_{PB}	7.8	9.8	—	dB
Collector Efficiency (V_{CC} = 50 Vdc, P_{out} = 150 W pk, f = 1090 MHz)	η	35	40	—	%
Load Mismatch (V_{CC} = 50 Vdc, P_{out} = 150 W pk, f = 1090 MHz) VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Power Output			

*80 μs Pulse on Tektronix 576 or equivalent.

FIGURE 1 — 1090 MHz TEST CIRCUIT



C1, C2 — 220 pF Chip Capacitor, 100-mil ATC
C3 — 0.1 μF/100 V
C4 — 47 μF/75 V Electrolytic
L1, L2 — 3 Turns, #18 AWG, 1/8″ ID
Z1–Z10 — Distributed Microstrip Elements — See Figure 9
Board Material — 0.031″ Thick Teflon-Fiberglass,
ϵ_r = 2.5

FIGURE 2 — OUTPUT POWER versus INPUT POWER

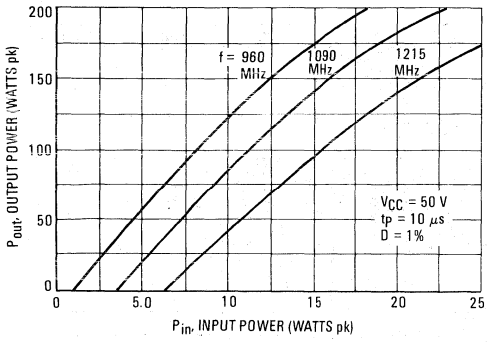


FIGURE 3 — OUTPUT POWER versus FREQUENCY

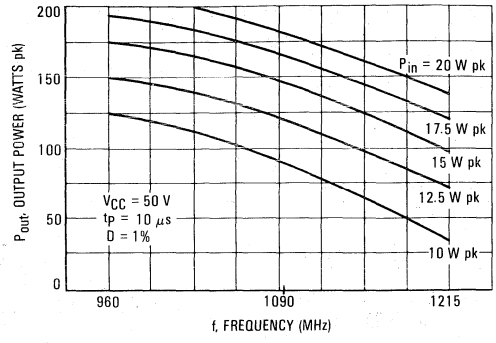


FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE

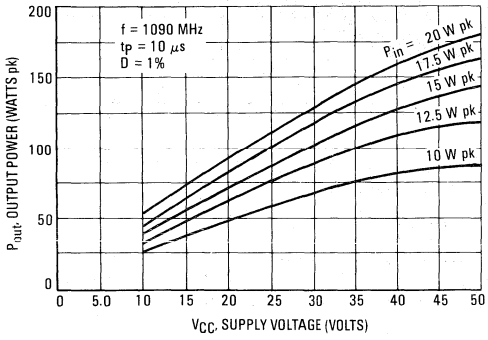


FIGURE 5 — POWER GAIN versus FREQUENCY

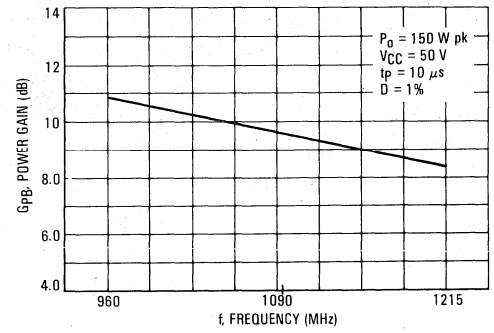
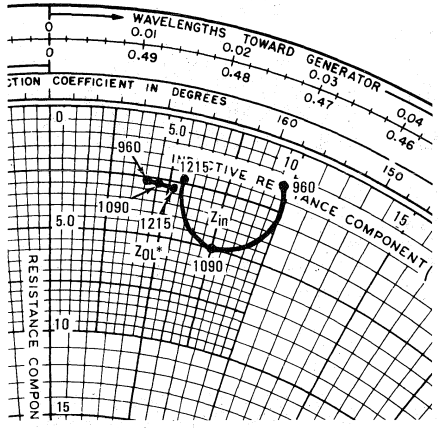


FIGURE 6 — SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCE



P_{out} = 150 W pk V_{CC} = 50 V
t_P = 10 μs D = 1%

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
960	1.5 + j9.6	2.6 + j4.1
1090	5.0 + j7.5	2.7 + j4.6
1215	2.4 + j5.6	2.8 + j5.3

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

FIGURE 7 — 1090 MHz TEST AMPLIFIER

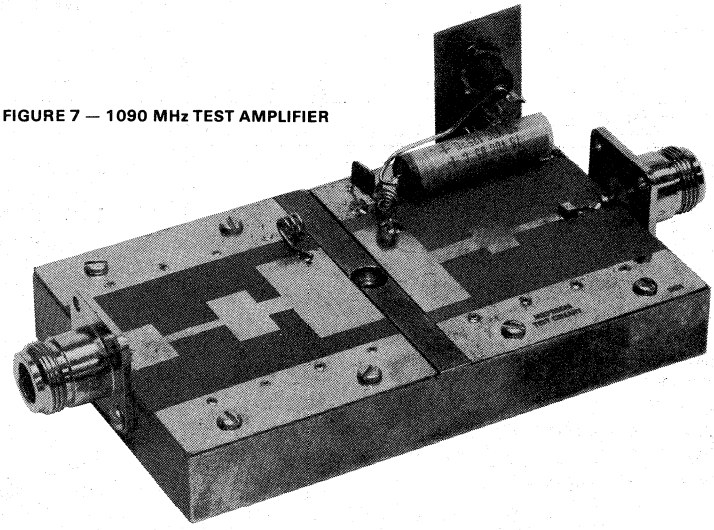


FIGURE 8 — TYPICAL PULSE PERFORMANCE

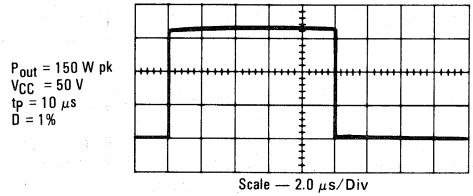
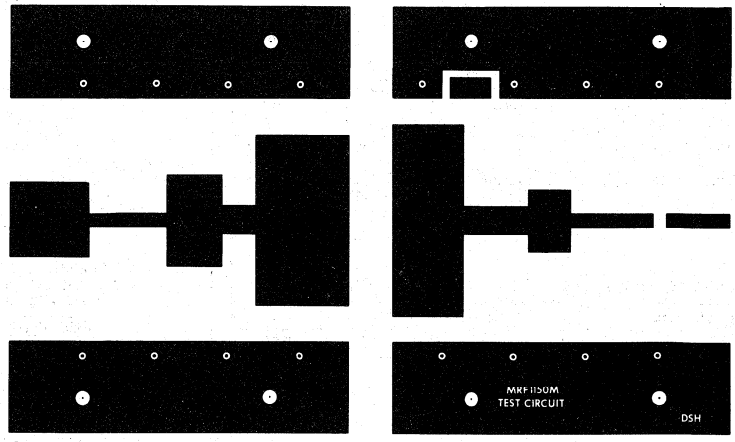


FIGURE 9 — PRINTED CIRCUIT BOARD LAYOUT — 1090 MHz TEST CIRCUIT



⊙ Soldered Eyelet

NOTE: The Printed Circuit Board shown is 75% of the original.

MRF1250M

The RF Line

250 W PEAK, 1020-1150 MHz

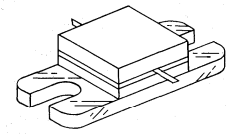
MICROWAVE POWER TRANSISTOR

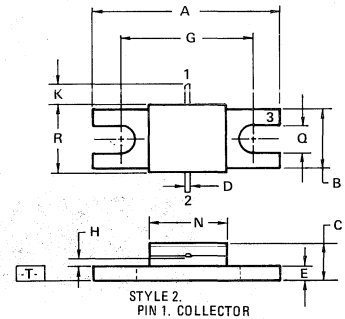
NPN SILICON

MICROWAVE PULSE POWER TRANSISTOR

. . . designed for Class B and C *common base* amplifier applications in short pulse TACAN, IFF, and DME transmitters.

- Guaranteed Performance @ 1090 MHz, 50 Vdc
  Output Power = 250 Watts Peak
  Minimum Gain = 6.0 dB
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Industry Standard Package
- Nitride Passivated
- Gold Metallized for Long Life and Resistance to Metal Migration
- Compatible with Other 1250M Types
- Internal Input and Output Matching for Broadband Operation





STYLE 2.
PIN 1. COLLECTOR
2. EMITTER
3. BASE

NOTES:
1. DIMENSIONS -A- AND -B- ARE DATUMS.
2. POSITIONAL TOLERANCE FOR MOUNTING HOLES:
   ⌖ .76(0.030) Ⓜ T A Ⓜ B Ⓜ
3. -T- IS SEATING PLANE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	22.61	23.11	0.890	0.910
B	9.65	9.91	0.380	0.390
C	4.06	5.84	0.160	0.230
D	0.51	0.76	0.020	0.030
E	1.40	1.65	0.055	0.065
G	16.51 BSC		0.650 BSC	
H	1.14	1.77	0.045	0.070
K	2.54	–	0.100	–
N	9.91	10.41	0.390	0.410
Q	3.00	3.61	0.118	0.142
R	9.91	10.41	0.390	0.410

CASE 336-03

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	70	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Peak (1, 2)	I_C	24	Adc
Peak Device Dissipation @ T_C = 25°C (1, 2) Derate above 25°C	P_D	1166 6.67	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (1,2,3)	$R_{\theta JC}$	0.15	°C/W

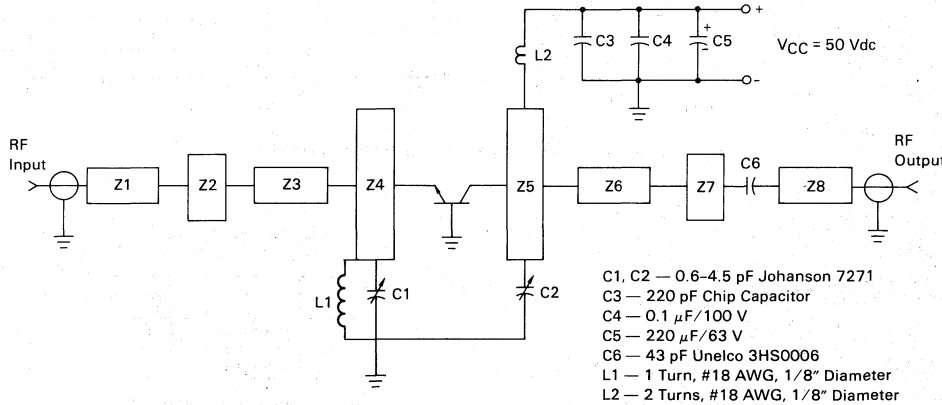
(1) Pulse Width = 10 μs, Duty Cycle = 1%.
(2) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF short pulse amplifiers.
(3) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	70	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 100 mAdc, I_E = 0)	$V_{(BR)CBO}$	70	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0)	I_{CBO}	—	—	20	mAdc
ON CHARACTERISTICS					
DC Current Gain* (I_C = 10 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	30	—	—
FUNCTIONAL TESTS (Pulse Width = 10 μs, Duty Cycle = 1.0%)					
Common-Base Amplifier Power Gain (V_{CC} = 50 Vdc, P_{out} = 250 W pk, f = 1090 MHz)	G_{PB}	6.0	7.2	—	dB
Collector Efficiency (V_{CC} = 50 Vdc, P_{out} = 250 W pk, f = 1090 MHz)	η	33	—	—	%
Load Mismatch (V_{CC} = 50 Vdc, P_{out} = 250 W pk, f = 1090 MHz, VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Power Output			

*80 μs Pulse on Tektronix 576 or equivalent.

FIGURE 1 — 1090 MHz TEST CIRCUIT



C1, C2 — 0.6-4.5 pF Johanson 7271
C3 — 220 pF Chip Capacitor
C4 — 0.1 μF/100 V
C5 — 220 μF/63 V
C6 — 43 pF Unelco 3HS0006
L1 — 1 Turn, #18 AWG, 1/8″ Diameter
L2 — 2 Turns, #18 AWG, 1/8″ Diameter
Z1-Z8 — Distributed Microstrip Elements — See Figure 9
Board Material — 0.062″ Thick Teflon*-Fiberglass, ϵ_r = 2.55

*Registered Trademark of DuPont

FIGURE 2 — OUTPUT POWER versus INPUT POWER

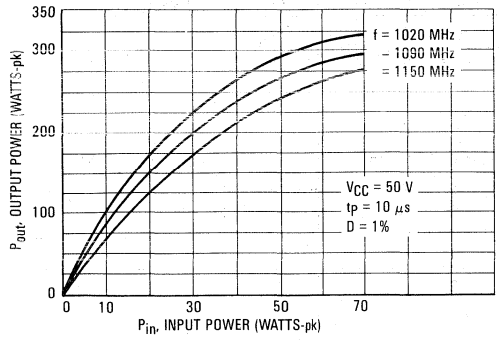


FIGURE 3 — OUTPUT POWER versus FREQUENCY

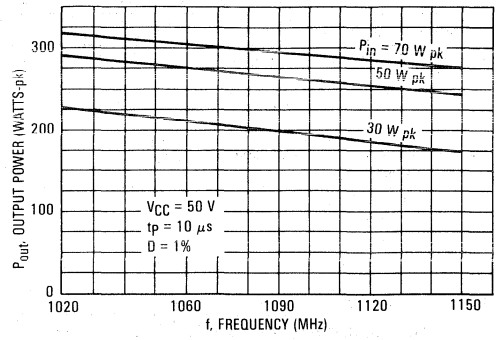


FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE

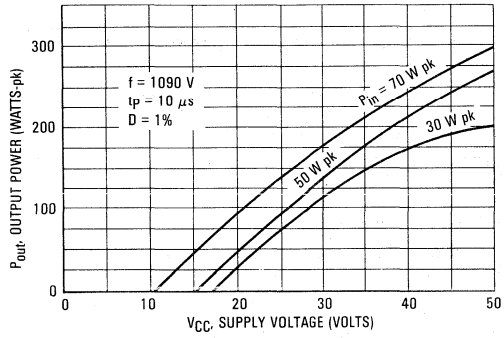


FIGURE 5 — POWER GAIN versus FREQUENCY

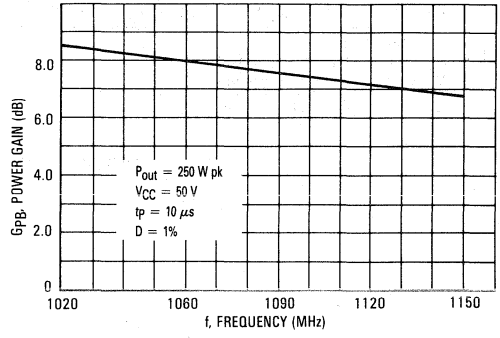
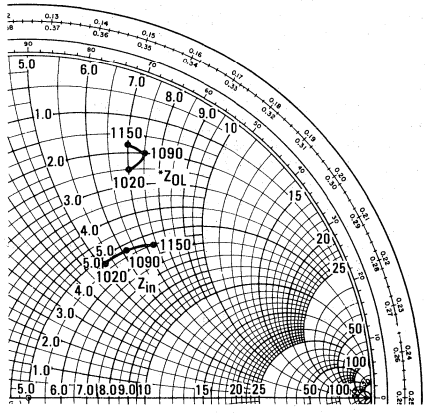


FIGURE 6 — SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCE



P_{out} = 250 W-pk V_{CC} = 50 V
tp = 10 μs D = 1%

f MHz	Z_{in} Ohms	Z_{OL}^* Ohms
1020	5.2 + j5.2	2.5 + j7.0
1090	5.2 + j6.2	2.0 + j7.5
1150	5.5 + j7.3	1.8 + j7.0

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

FIGURE 7 — 1090 MHz TEST AMPLIFIER

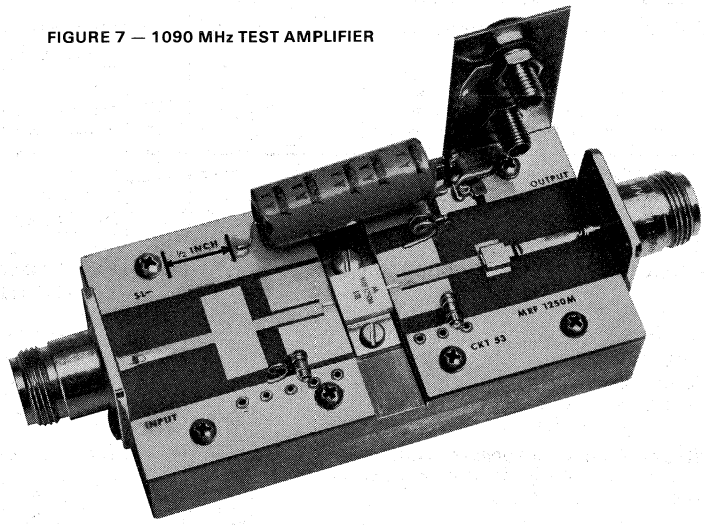


FIGURE 8 — TYPICAL PULSE PERFORMANCE

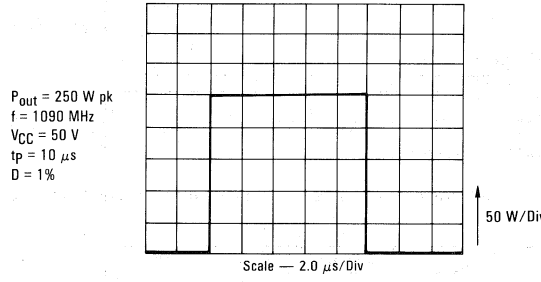
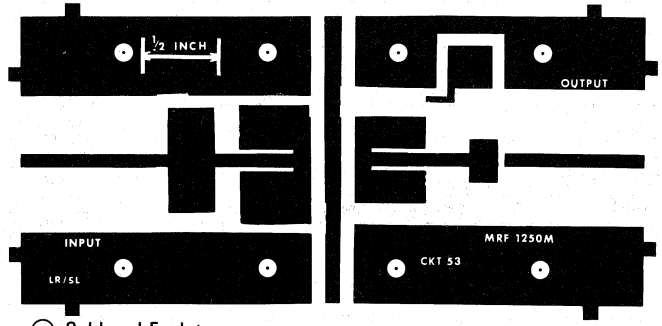


FIGURE 9 — PRINTED CIRCUIT BOARD LAYOUT — 1090 MHz TEST CIRCUIT



⊙ Soldered Eyelet

NOTE: The Printed Circuit Board shown is 75% of the original.

MRF1325M

The RF Line

MICROWAVE PULSE POWER TRANSISTOR

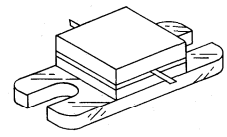
. . . designed for Class B and C *common base* amplifier applications in short pulse TACAN, IFF, and DME transmitters.

- Guaranteed Performance @ 1090 MHz, 50 Vdc
  Output Power = 325 Watts Peak
  Minimum Gain = 6.0 dB
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Industry Standard Package
- Nitride Passivated
- Gold Metallized for Long Life and Resistance to Metal Migration
- Compatible with Other 1325M Types
- Internal Input and Output Matching for Broadband Operation

325 W PEAK, 1020-1150 MHz

MICROWAVE POWER TRANSISTOR

NPN SILICON



3

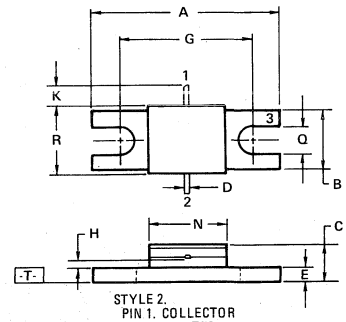
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	70	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Peak (1, 2)	I_C	24	Adc
Peak Device Dissipation @ T_C = 25°C (1, 2) Derate above 25°C	P_D	1166 6.67	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (1,2,3)	$R_{\theta JC}$	0.15	°C/W

(1) Pulse Width = 10 μs, Duty Cycle = 1%.
(2) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF short pulse amplifiers.
(3) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.



STYLE 2.
PIN 1. COLLECTOR
2. EMITTER
3. BASE

NOTES:
1. DIMENSIONS -A- AND -B- ARE DATUMS.
2. POSITIONAL TOLERANCE FOR MOUNTING HOLES:
   ⌖ .76(0.030) Ⓜ T A Ⓜ B Ⓜ
3. -T- IS SEATING PLANE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.61	23.11	0.890	0.910
B	9.65	9.91	0.380	0.390
C	4.06	5.84	0.160	0.230
D	0.51	0.76	0.020	0.030
E	1.40	1.65	0.055	0.065
G	16.51 BSC		0.650 BSC	
H	1.14	1.77	0.045	0.070
K	2.54	–	0.100	–
N	9.91	10.41	0.390	0.410
Q	3.00	3.61	0.118	0.142
R	9.91	10.41	0.390	0.410

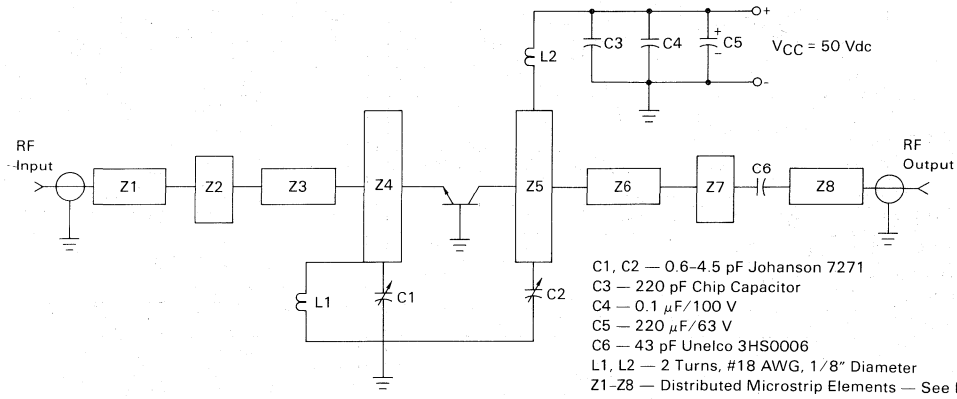
CASE 336-03

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	70	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 100 mAdc, I_E = 0)	$V_{(BR)CBO}$	70	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0)	I_{CBO}	—	—	20	mAdc
ON CHARACTERISTICS					
DC Current Gain* (I_C = 10 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	30	—	—
FUNCTIONAL TESTS (Pulse Width = 10 μs, Duty Cycle = 1.0%)					
Common-Base Amplifier Power Gain (V_{CC} = 50 Vdc, P_{out} = 325 W pk, f = 1090 MHz)	G_{PB}	6.0	7.2	—	dB
Collector Efficiency (V_{CC} = 50 Vdc, P_{out} = 325 W pk, f = 1090 MHz)	η	33	—	—	%
Load Mismatch (V_{CC} = 50 Vdc, P_{out} = 325 W pk, f = 1090 MHz, VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Power Output			

*80 μs Pulse on Tektronix 576 or equivalent.

FIGURE 1 — 1090 MHz TEST CIRCUIT



C1, C2 — 0.6-4.5 pF Johanson 7271
C3 — 220 pF Chip Capacitor
C4 — 0.1 μF/100 V
C5 — 220 μF/63 V
C6 — 43 pF Unelco 3HS0006
L1, L2 — 2 Turns, #18 AWG, 1/8" Diameter
Z1-Z8 — Distributed Microstrip Elements — See Figure 9
Board Material — 0.062" Thick Teflon*-Fiberglass,
ϵ_r = 2.55

*Registered Trademark of DuPont

FIGURE 2 — OUTPUT POWER versus INPUT POWER

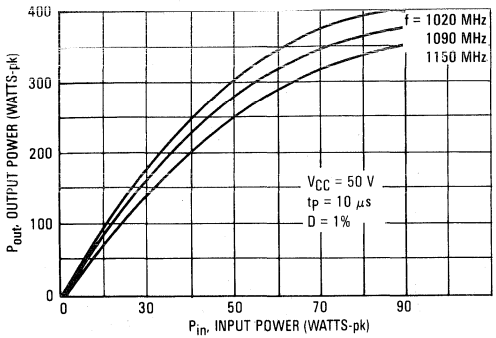


FIGURE 3 — OUTPUT POWER versus FREQUENCY

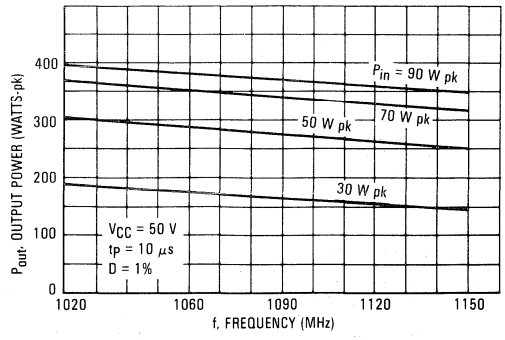


FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE

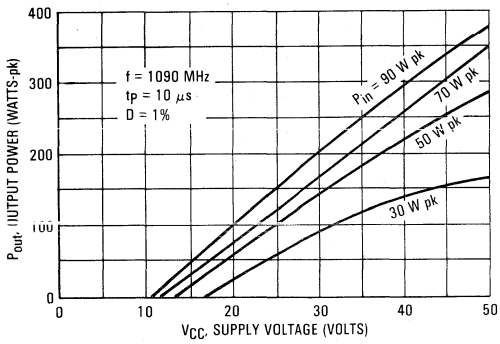


FIGURE 5 — POWER GAIN versus FREQUENCY

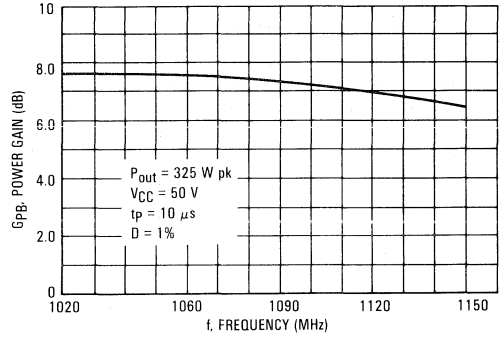
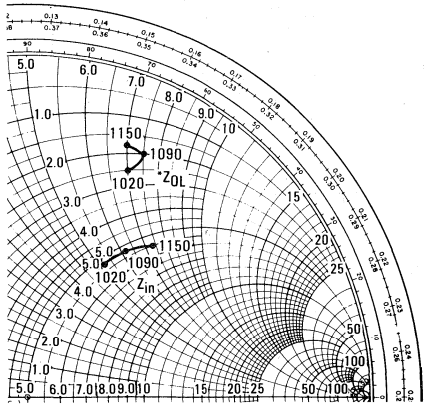


FIGURE 6 — SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCE



P_{out} = 325 W-pk V_{CC} = 50 V
t_P = 10 μs D = 1%

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
1020	5.2 + j5.2	2.5 + j7.0
1090	5.2 + j6.2	2.0 + j7.5
1150	5.5 + j7.3	1.8 + j7.0

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

FIGURE 7 — 1090 MHz TEST AMPLIFIER

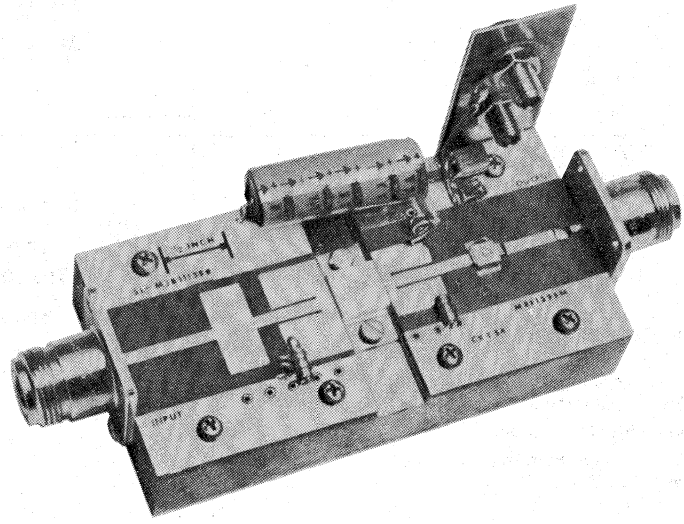


FIGURE 8 — TYPICAL PULSE PERFORMANCE

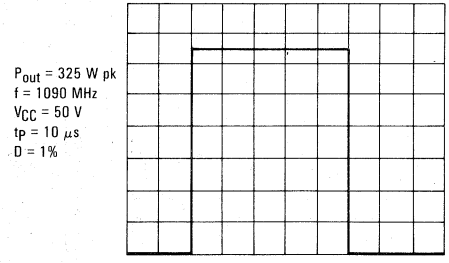
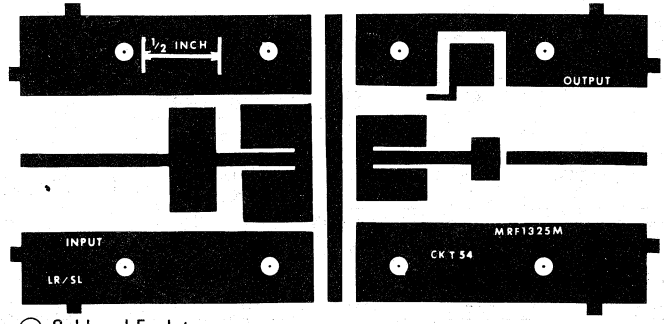


FIGURE 9 — PRINTED CIRCUIT BOARD LAYOUT — 1090 MHz TEST CIRCUIT



⊙ Soldered Eyelet

NOTE: The Printed Circuit Board shown is 75% of the original.

MRF1946
MRF1946A

The RF Line

30 W 136–220 MHz

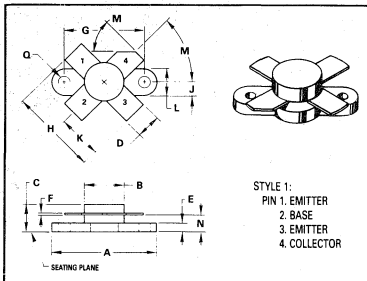
RF POWER TRANSISTOR

NPN SILICON

NPN SILICON POWER TRANSISTOR

Designed for 12.5 volt large-signal power amplifiers in commercial and industrial equipment.

- High Common Emitter Power Gain
- Specified 12.5 V, 175 MHz Performance
  Output Power = 30 Watts
  Power Gain = 10 dB
  Efficiency = 60%
- Diffused Emitter Resistor Ballasting
- Characterized to 220 MHz
- Load Mismatch at High Line and Overdrive Conditions



STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	24.38	25.15	0.960	0.990
B	9.40	9.91	0.370	0.390
C	5.82	7.14	0.229	0.281
D	5.46	5.97	0.215	0.235
E	2.16	2.67	0.085	0.105
F	0.10	0.15	0.004	0.006
G	18.29	18.54	0.720	0.730
H	20.07	20.57	0.790	0.810
K	10.03	10.29	0.395	0.405
L	6.22	6.48	0.245	0.255
M	40°	50°	40°	50°
N	3.81	4.57	0.150	0.180
Q	2.87	3.30	0.113	0.130

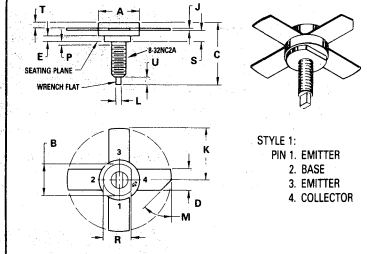
CASE 211-07
MRF1946

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Continuous	I_C	8.0	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	100 0.57	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	°C/W



STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

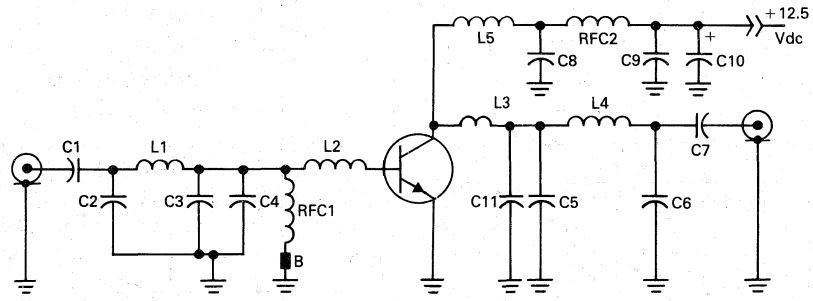
DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	17.02	20.07	0.670	0.790
D	5.46	5.97	0.215	0.235
E	1.78	—	0.070	—
J	0.08	0.18	0.003	0.007
K	12.45	—	0.490	—
L	1.40	1.78	0.055	0.070
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.11	2.54	0.083	0.100
U	2.49	3.35	0.098	0.132

CASE 145A-09
MRF1946A

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 25 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 25 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	40	75	150	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	75	100	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 30 W, f = 175 MHz)	G_{pe}	10	11	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 30 W, f = 175 MHz)	η	60	70	—	%
Load Mismatch (V_{CC} = 15.5 Vdc, P_{in} = 2.0 dB Overdrive, Load VSWR = 30:1)	ψ	No Degradation in Output Power			

FIGURE 1 — BROADBAND TEST CIRCUIT SCHEMATIC



C1 = 56 pF Mini-Unelco, 3HS0006-56
C2 = 47 pF Mini-Unelco, 3HS0006-47
C3, C4 = 180 pF Chip Cap, ATC 100B181JC500
C5 = 150 pF Unelco, J101–150
C6 = 39 pF Mini-Unelco, 3HS0006-39
C7, C8 = 1000 pF Chip Cap, ATC 100B102JC50
C9 = 0.1 μF Ceramic Capacitor
C10 = 10 μF, 25 V Electrolytic Capacitor
C11 = 56 pF Mini-Unelco, 3HS0006-56

L1 = 2 Turns #18 AWG, 0.125″ ID
L2, L3 = Circuit Board and Mounting Pad Inductance
L4 = 3 Turns #18 AWG, 0.125″ ID
L5 = 6 Turns #16 Enameled, 0.250″ ID

RFC1 = 0.15 μH Molded Choke w/Ferrite Bead
RFC2 = Ferrite Choke, Fair Rite VK200-4B

Board Material = 1/32″ Glass
Teflon, 1 oz. Cu Plating

Bead — Ferroxcube

FIGURE 2 — OUTPUT POWER versus INPUT POWER

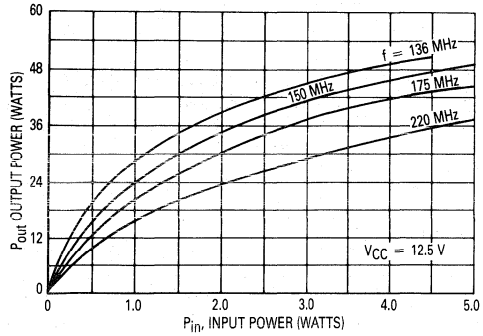


FIGURE 3 — OUTPUT POWER versus FREQUENCY

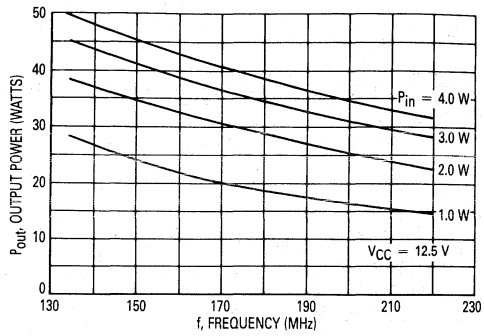


FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 220 MHz

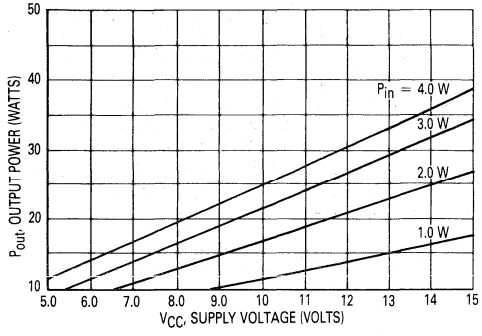


FIGURE 5 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 175 MHz

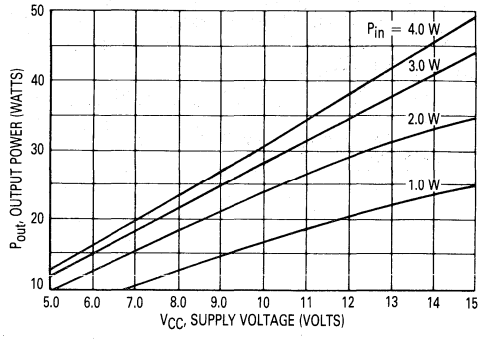


FIGURE 6 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 150 MHz

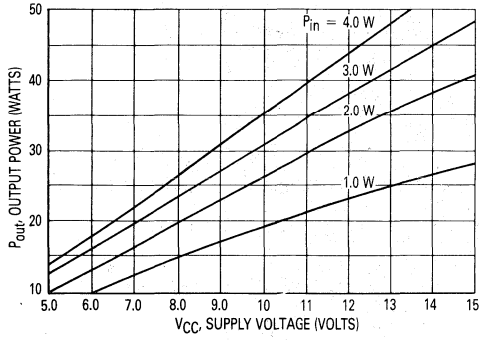


FIGURE 7 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 136 MHz

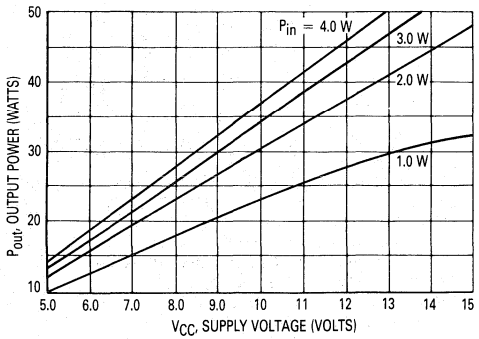


FIGURE 8 — TYPICAL PERFORMANCE IN A BROADBAND CIRCUIT

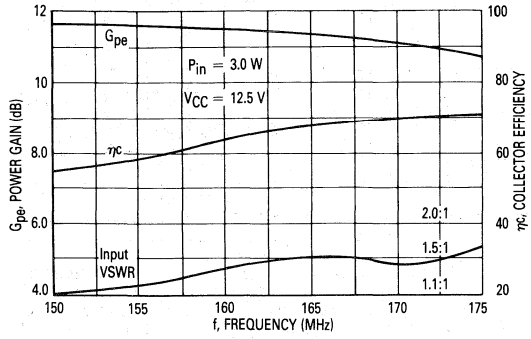
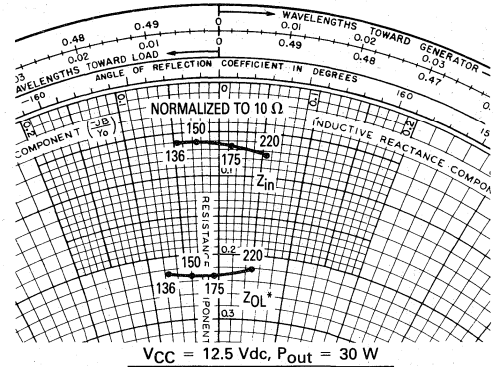


FIGURE 9 — SERIES EQUIVALENT INPUT AND OUTPUT IMPEDANCE



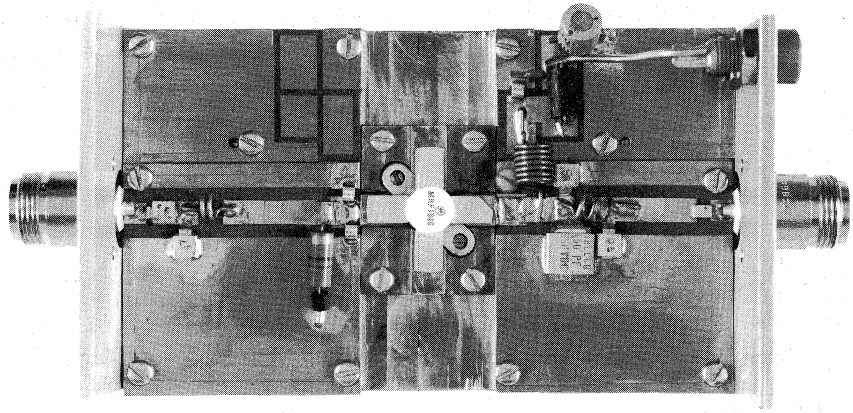
V_{CC} = 12.5 Vdc, P_{out} = 30 W

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
136	0.60 − j0.48	2.22 − j0.74
150	0.63 − j0.26	2.30 − j0.40
175	0.62 + j0.13	2.35 − j0.04
220	0.73 + j0.57	2.20 + j0.43

*Z_{OL} = Conjugate of optimum load impedance into which the device operates at a given output power, voltage and frequency.

3

FIGURE 10 — BROADBAND TEST CIRCUIT



MRF2001
MRF2001B

The RF Line

NPN SILICON MICROWAVE POWER TRANSISTOR

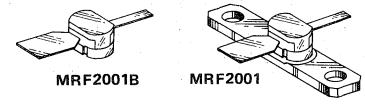
. . . designed for Class B and C amplifier or oscillator applications in the 1.0 to 2.3 GHz frequency range.

- Guaranteed Performance @ 2 GHz, 28 Vdc
  Output Power = 1.0 Watt
  Minimum Gain = 9.0 dB
- 100% Tested for Load Mismatch at All Phase Angles With 10:1 VSWR
- Hermetically Sealed Industry Standard Package
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Compatible with Older 2001 Types
- Other Devices in the 2000 Series:
  MRF2003 3 W
  MRF2005 5 W
  MRF2010 10 W

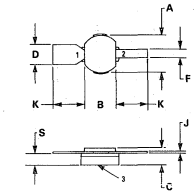
1.0 W 2 GHz

MICROWAVE POWER TRANSISTOR

NPN SILICON



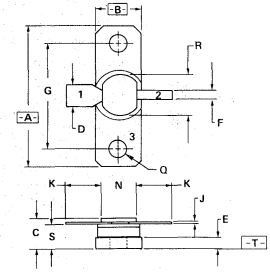
MRF2001B MRF2001



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	5.72	5.97	0.225	0.235
B	4.44	4.70	0.175	0.185
C	2.29	2.74	0.090	0.108
D	2.92	3.18	0.115	0.125
F	1.14	1.40	0.045	0.055
J	0.08	0.15	0.003	0.006
K	—	9.52	—	0.375
S	1.52	1.78	0.060	0.070

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

CASE 328-02



NOTES:
1. [A] AND [B] ARE DATUMS.
2. [T] IS SEATING PLANE.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLES: "Q"
   [⌖] 0.15 (0.006) [T] [A] [B]
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	20.19	20.57	0.795	0.810
B	6.22	6.48	0.245	0.255
C	3.68	4.19	0.145	0.165
D	2.92	3.18	0.115	0.125
E	1.40	1.65	0.055	0.065
F	1.14	1.40	0.045	0.055
G	14.22 BSC		0.560 BSC	
J	0.08	0.15	0.003	0.006
K	—	9.52	—	0.375
N	4.44	4.70	0.175	0.185
Q	3.25	3.35	0.128	0.132
R	5.72	5.97	0.225	0.235
S	2.92	3.43	0.115	0.135

STYLE 1:
1. EMITTER
2. COLLECTOR
3. BASE

CASE 328A-01

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CBO}	45	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Continuous	I_C	250	mAdc
Total Device Dissipation @ $T_C = 25^oC$ (1) Derate above 25^oC	P_D	7.0 40	Watts $mW/^oC$
Storage Temperature Range	T_{stg}	−65 to +200	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	25	$^oC/W$

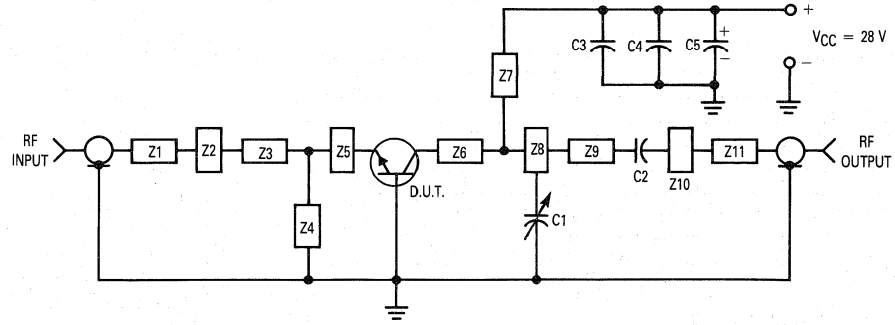
(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, R_{BE} = 10 Ω)	$V_{(BR)CER}$	45	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 5.0 mAdc, I_E = 0)	$V_{(BR)CBO}$	45	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 28 Vdc, I_E = 0)	I_{CBO}	–	–	0.5	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	–	100	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	2.5	5.0	pF
FUNCTIONAL TESTS					
Common-Base Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 1.0 W, f = 2.0 GHz)	G_{PB}	9.0	10	–	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 1.0 W, f = 2.0 GHz)	η	30	35	–	%
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 1.0 W, f = 2.0 GHz, VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Power Output			

FIGURE 1. 2 GHz TEST CIRCUIT



Z1–Z11 — Microstrip
C1 — 0.4–2.5 pF Johanson 7285
C2, C3 — 56 pF Chip Capacitor
C4 — 0.1 μF
C5 — 10 μF 50 V Electrolytic
Board Material — 0.062" Glass Teflon

FIGURE 2 – OUTPUT POWER versus INPUT POWER (f = 1 GHz)

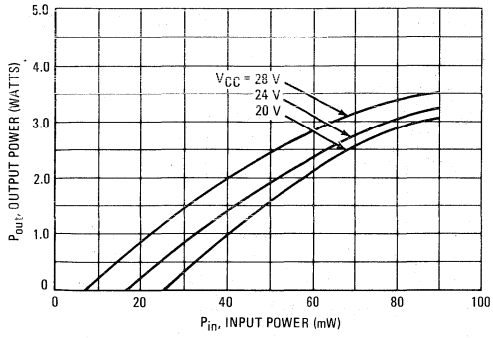


FIGURE 3 – OUTPUT POWER versus INPUT POWER (f = 2 GHz)

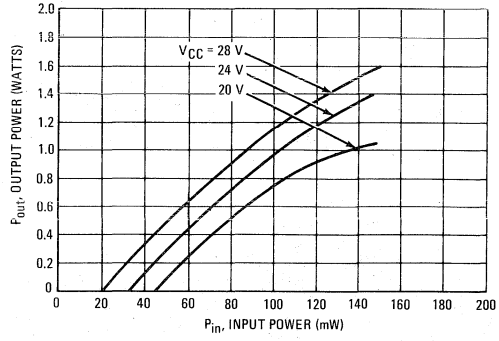


FIGURE 4 – OUTPUT POWER versus FREQUENCY

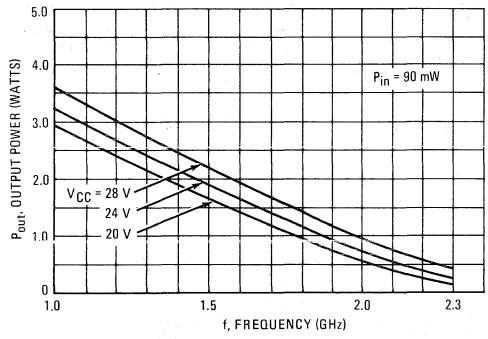


FIGURE 5 – POWER GAIN versus FREQUENCY

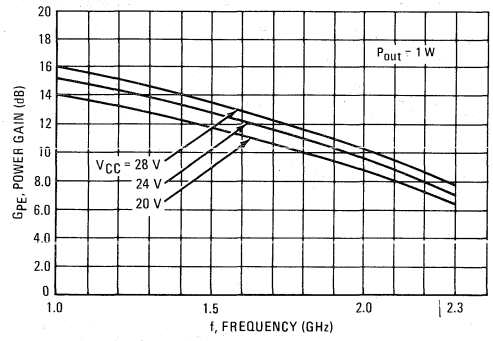
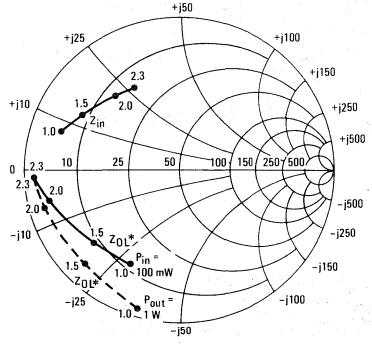


FIGURE 6 – SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCE



Coordinates in Ohms

V_{CC} = 28 V

f GHz	Z_{in} Ohms	Z_{OL}* Ohms P_{in} = 100 mW	Z_{OL}* Ohms P_{out} = 1 W
1.0	6.6 + j8.4	11 – j28.9	4.9 – j37.4
1.5	8.5 + j12.2	8.1 – j17.3	4.6 – j21.0
2.0	11.5 + j19.5	4.2 – j6.0	3.5 – j7.0
2.3	13.4 + j26.0	3.4 – j1.8	3.4 – j1.8

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

FIGURE 7 – 2 GHz TEST AMPLIFIER

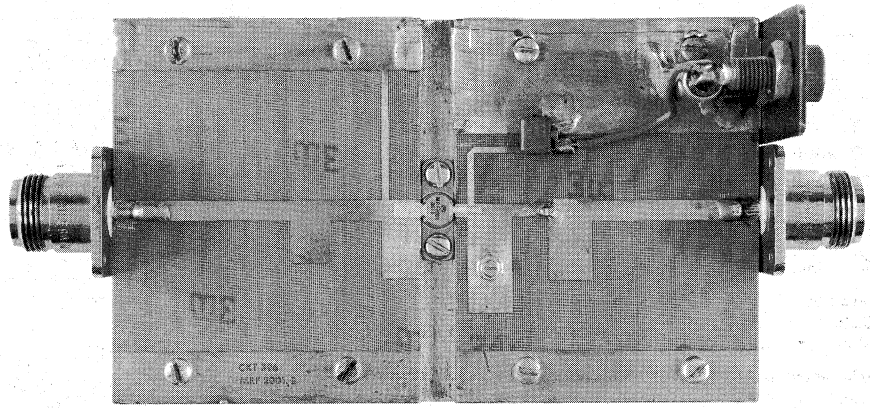
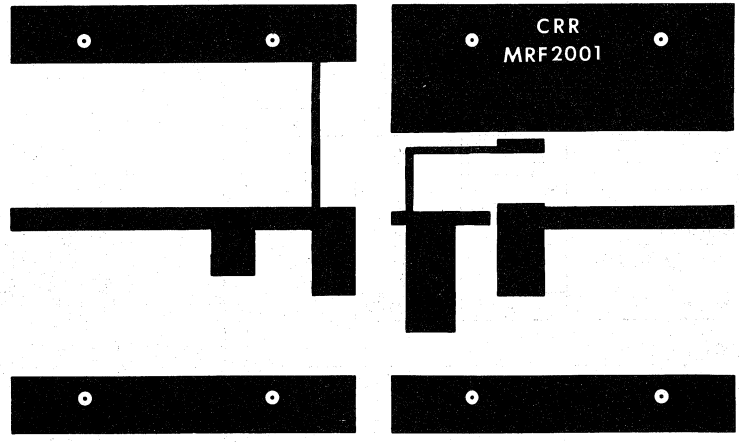


FIGURE 8 – PRINTED CIRCUIT BOARD LAYOUT – 2 GHz TEST CIRCUIT



NOTE: The Printed Circuit Board shown is 75% of the original.

MRF2001M

The RF Line

NPN SILICON MICROWAVE POWER TRANSISTOR

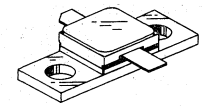
. . . designed for Class B and C *common base* broadband amplifier applications in the 1.7 to 2.3 GHz frequency range.

- Internal Input Matching for Broadband Operation
- Guaranteed Performance @ 2 GHz, 24 Vdc
  Output power = 1.0 Watt
  Minimum Gain = 8.5 dB
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Hermetically Sealed Industry Standard Package
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Silicon Nitride Passivation
- Characterized for Operation from 20 V to 28 V Supply Voltages

1.0 W 2 GHz

MICROWAVE POWER TRANSISTOR

NPN SILICON



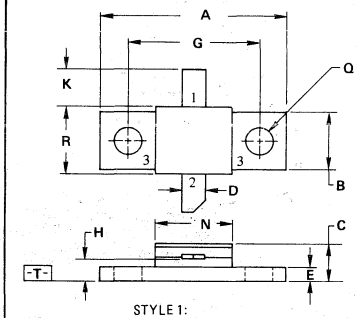
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CBO}	45	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Continuous	I_C	250	mAdc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	7.0 40	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	25	°C/W

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.
(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.



STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. DIMENSIONS -A- AND -B- ARE DATUMS.
2. POSITIONAL TOLERANCE FOR MOUNTING HOLES: ⌖ Ø.13(0.005)Ⓜ T AⓂ BⓂ
3. -T- IS SEATING PLANE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

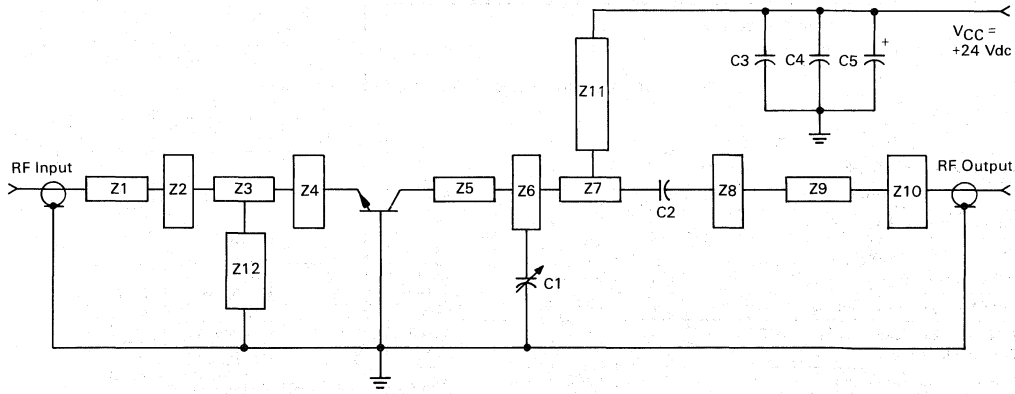
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	20.07	20.57	0.790	0.810
B	6.22	6.48	0.245	0.255
C	3.68	4.06	0.145	0.160
D	2.29	2.79	0.090	0.110
E	1.42	1.73	0.056	0.068
G	14.27 BSC		0.560 BSC	
H	2.29	2.79	0.090	0.110
K	3.43	4.19	0.135	0.165
N	7.87	8.38	0.310	0.330
Q	3.05	3.30	0.120	0.130
R	7.24	7.49	0.285	0.295

CASE 337-02

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	45	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 5.0 mAdc, I_E = 0)	$V_{(BR)CBO}$	45	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 28 Vdc, I_E = 0)	I_{CBO}	—	—	0.5	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	—	100	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 24 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	4.0	6.0	pF
FUNCTIONAL TESTS					
Common-Base Amplifier Power Gain (V_{CC} = 24 Vdc, P_{out} = 1.0 W, f = 2.0 GHz)	G_{PB}	8.5	9.5	—	dB
Collector Efficiency (V_{CC} = 24 Vdc, P_{out} = 1.0 W, f = 2.0 GHz)	η	35	40		
Load Mismatch (V_{CC} = 24 Vdc, P_{out} = 1.0 W, f = 2.0 GHz) VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Power Output			

FIGURE 1 — 2.0 GHz TEST CIRCUIT



Z1–Z12 — Microstrip, See Photomaster
C1 — 0.6–4.5 pF Johanson 7271
C2, C3 — 56 pF Chip Capacitor
C4 — 0.1 μF
C5 — 10 μF, 35 V
Board Material — 0.0312" Teflon Fiberglass
ϵ_r = 2.5 ± 0.05

FIGURE 2 — OUTPUT POWER versus INPUT POWER (f = 1.7 GHz)

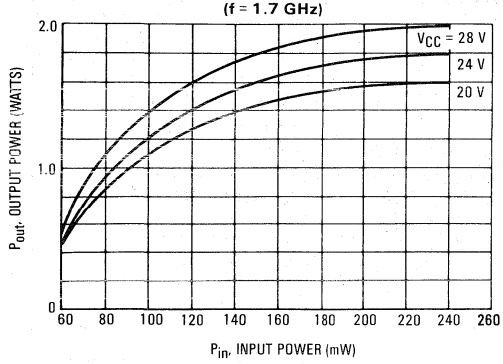


FIGURE 3 — OUTPUT POWER versus INPUT POWER (f = 2.0 GHz)

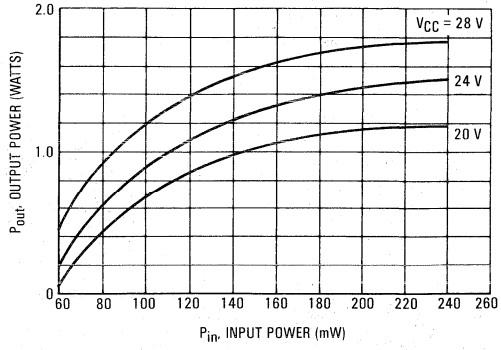


FIGURE 4 — OUTPUT POWER versus INPUT POWER (f = 2.3 GHz)

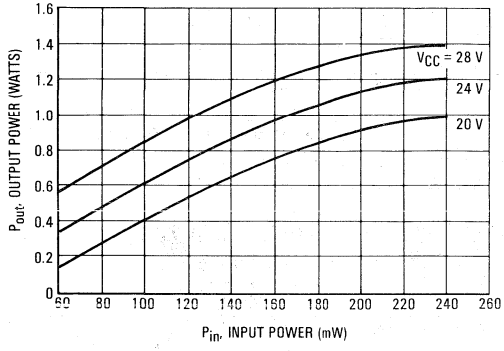


FIGURE 5 — POWER GAIN versus FREQUENCY

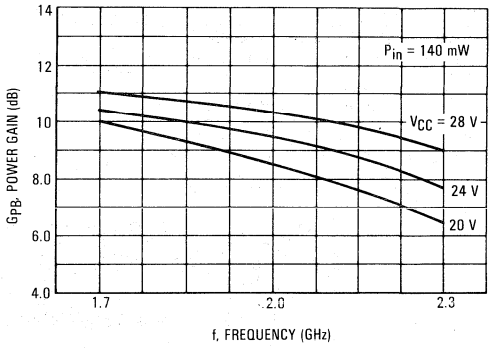
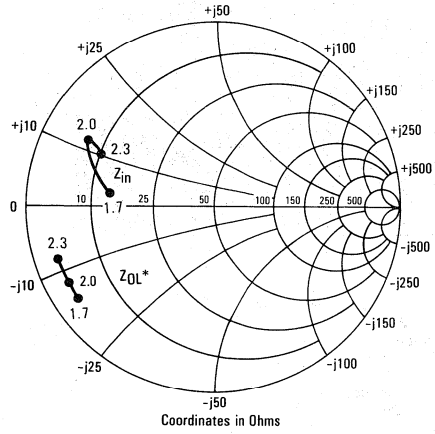


FIGURE 6 — SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCE



V_{CC} = 24 V, P_{in} = 140 mW

f GHz	Z_{in} Ohms	Z_{OL}* Ohms
1.7	15.5 + j 3.0	4.5 – j15.0
2.0	7.5 + j11.0	4.0 – j12.0
2.3	10.0 + j10.0	3.0 – j 7.0

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

FIGURE 7 — 2 GHz TEST AMPLIFIER

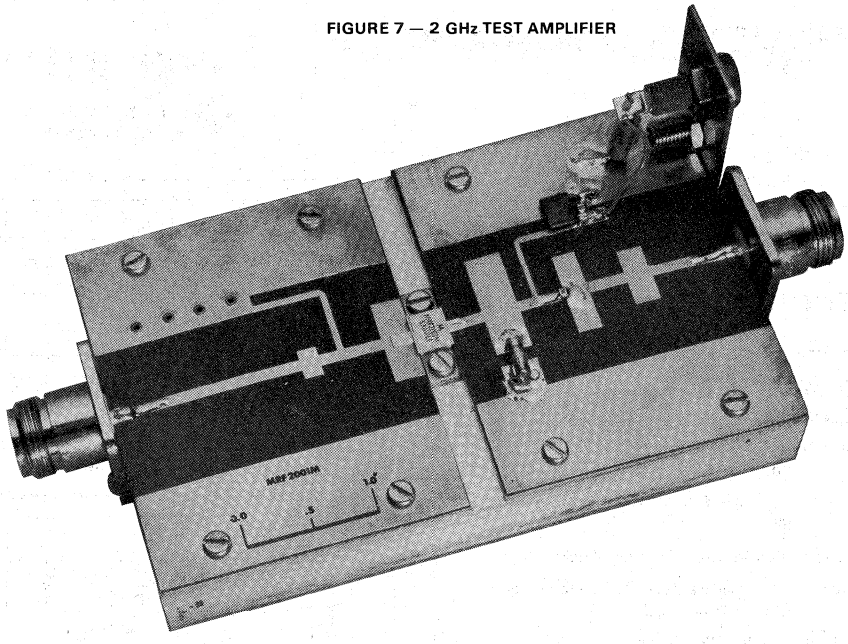
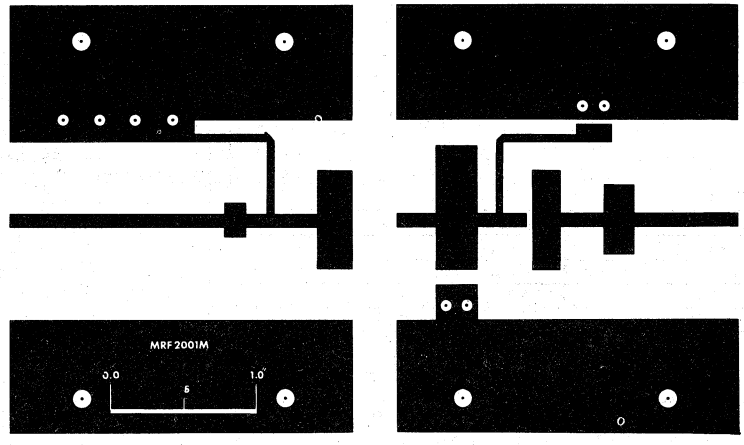


FIGURE 8 — PRINTED CIRCUIT BOARD LAYOUT — 2.0 GHz TEST CIRCUIT



Denotes Eyelet

4–40 Screw Placement

NOTE: The Printed Circuit Board shown is 75% of the original.

MRF2003
MRF2003B

The RF Line

NPN SILICON MICROWAVE POWER TRANSISTOR

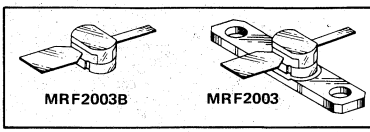
. . . designed for Class B and C amplifier or oscillator applications in the 1.0 to 2.3 GHz frequency range.

- Guaranteed Performance @ 2 GHz, 28 Vdc
  Output Power = 3.0 Watts
  Minimum Gain = 7.8 dB
- 100% Tested for Load Mismatch at All Phase Angles With 10:1 VSWR
- Hermetically Sealed Industry Standard Package
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Compatible with Older 2003 Types
- Other Devices in the 2000 Series:
  MRF2001 1 W
  MRF2005 5 W
  MRF2010 10 W

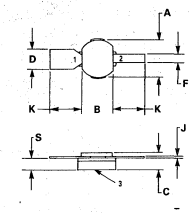
3.0 W 2 GHz

MICROWAVE POWER TRANSISTOR

NPN SILICON



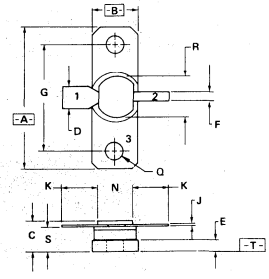
MRF2003B MRF2003



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	5.72	5.97	0.225	0.235
B	4.44	4.70	0.175	0.185
C	2.29	2.74	0.090	0.108
D	2.92	3.18	0.115	0.125
F	1.14	1.40	0.045	0.055
J	0.08	0.15	0.003	0.006
K	—	9.52	—	0.375
S	1.52	1.78	0.060	0.070

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

CASE 328-02



NOTES:
1. A AND B ARE DATUMS.
2. T IS SEATING PLANE.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLES: "Q"
   ⌖ 0.15 (0.006) M T A M B M
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	20.19	20.57	0.795	0.810
B	6.22	6.48	0.245	0.255
C	3.68	4.19	0.145	0.165
D	2.92	3.18	0.115	0.125
E	1.40	1.65	0.055	0.065
F	1.14	1.40	0.045	0.055
G	14.22 BSC		0.560 BSC	
J	0.08	0.15	0.003	0.006
K	—	9.52	—	0.375
N	4.44	4.70	0.175	0.185
Q	3.25	3.35	0.128	0.132
R	5.72	5.97	0.225	0.235
S	2.92	3.43	0.115	0.135

STYLE 1:
1. EMITTER
2. COLLECTOR
3. BASE

CASE 328A-01

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CBO}	45	Vdc
Emitter-Base Voltage	V_{EBO}	3.5	Vdc
Collector-Current — Continuous	I_C	0.5	Adc
Total Device Dissipation @ $T_C = 25^oC$ (1) Derate above 25^oC	P_D	11.6 67	Watts $mW/^oC$
Storage Temperature Range	T_{stg}	−65 to +200	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	15	$^oC/W$

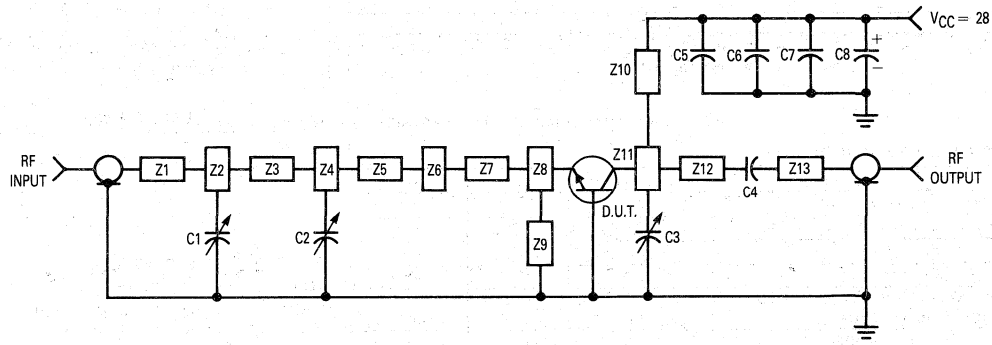
(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, R_{BE} = 10 Ω)	$V_{(BR)CER}$	45	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 5.0 mAdc, I_E = 0)	$V_{(BR)CBO}$	45	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	–	–	Vdc
Collector Cutoff Current (V_{CB} = 28 Vdc, I_E = 0)	I_{CBO}	–	–	0.5	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 150 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	–	100	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	4.0	6.0	pF
FUNCTIONAL TESTS					
Common-Base Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 3.0 W, f = 2.0 GHz)	G_{PB}	7.8	8.9	–	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 3.0 W, f = 2.0 GHz)	η	30	35		
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 3.0 W, f = 2.0 GHz, VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Power Output			

FIGURE 1 – 2 GHz TEST CIRCUIT



Z1–Z13 — Microstrip
C1, C2, C3 — 0.4–2.5 pF Johanson
C4, C5, C6 — 56 pF Chip Capacitor
C7 — 0.1 μF
C8 — 10 μF 50 V Electrolytic
Board Material — 0.062" Glass Teflon

FIGURE 2 – OUTPUT POWER versus INPUT POWER (f = 1 GHz)

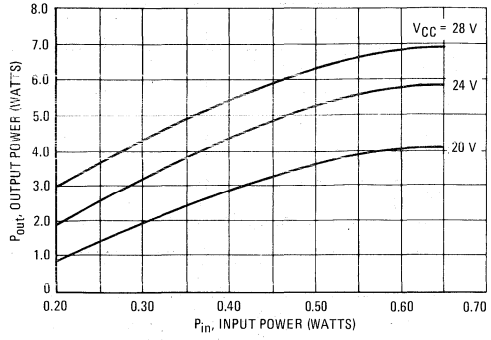


FIGURE 3 – OUTPUT POWER versus INPUT POWER (f = 2 GHz)

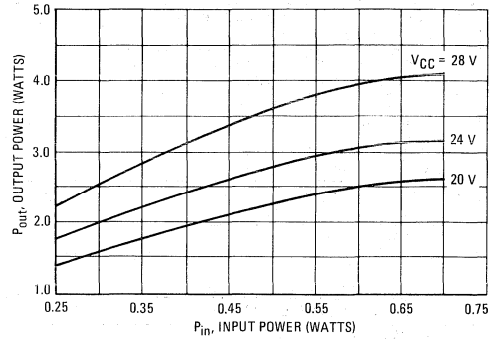


FIGURE 4 – OUTPUT POWER versus FREQUENCY

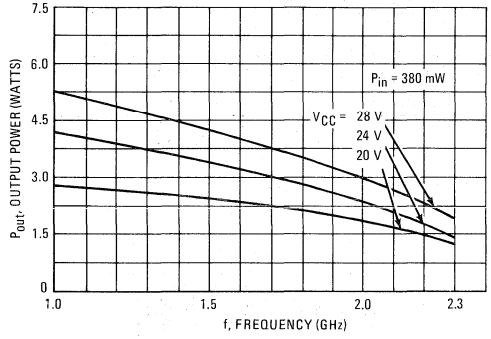


FIGURE 5 – POWER GAIN versus FREQUENCY

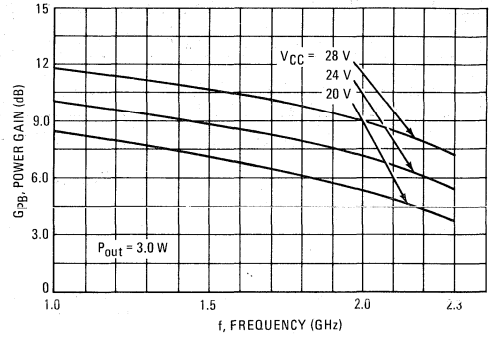
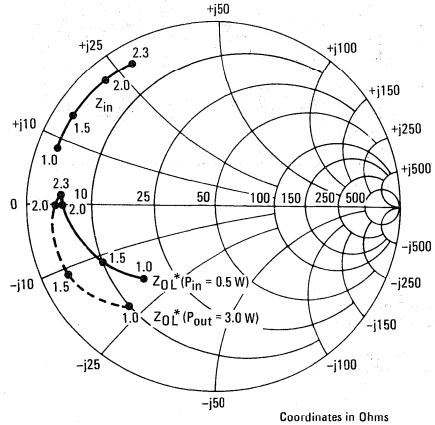


FIGURE 6 – MRF2003 SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCE



V_{CC} = 28 V

f GHz	Z_{in} Ohms	Z_{OL}^* P_{in} = 0.5 W Ohms	Z_{OL}^* P_{out} = 3 W Ohms
1.0	2.0 + j9.0	17.5 – j18	10 – j23
1.5	3.0 + j14.5	10 – j10.5	3.0 – j10.5
2.0	4.0 + j23	6.5 + j0	5.0 + j0
2.3	4.5 + j29	5.5 + j1.7	5.5 + j1.7

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

FIGURE 7 – 2 GHz TEST AMPLIFIER

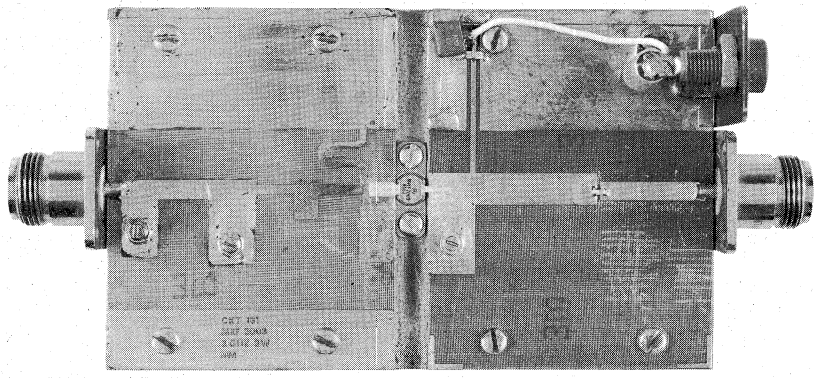
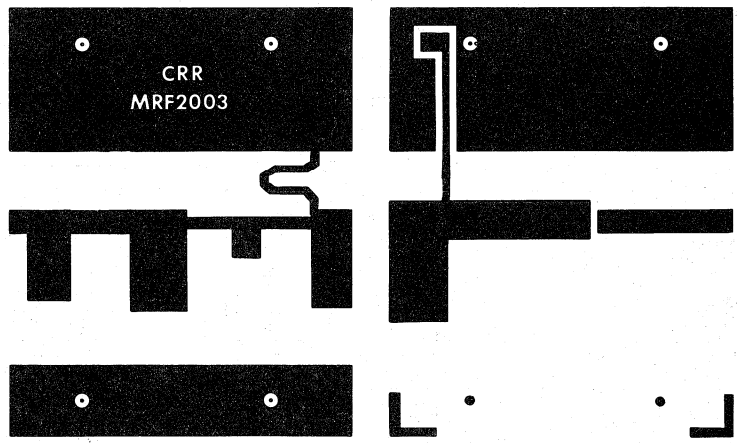


FIGURE 8 – PRINTED CIRCUIT BOARD LAYOUT
2 GHz TEST CIRCUIT



NOTE: The Printed Circuit Board shown is 75% of the original.

MRF2003M

The RF Line

NPN SILICON MICROWAVE POWER TRANSISTOR

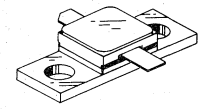
. . . designed for Class B and C *common base* broadband amplifier applications in the 1.7 to 2.3 GHz frequency range.

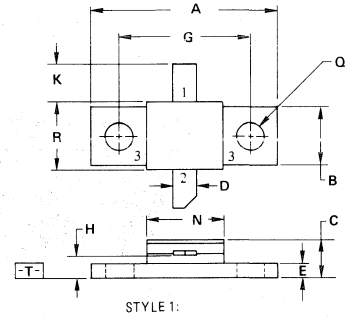
- Internal Input Matching for Broadband Operation
- Guaranteed Performance @ 2 GHz, 24 Vdc
  Output power = 3.0 Watt
  Minimum Gain = 8.0 dB
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Hermetically Sealed Industry Standard Package
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Silicon Nitride Passivation
- Characterized for Operation from 20 V to 28 V Supply Voltages

3.0 W 2 GHz

MICROWAVE POWER TRANSISTOR

NPN SILICON





STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. DIMENSIONS -A- AND -B- ARE DATUMS.
2. POSITIONAL TOLERANCE FOR MOUNTING HOLES: ⌖ Ø.13(0.005) Ⓜ T A Ⓜ B Ⓜ
3. -T- IS SEATING PLANE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.07	20.57	0.790	0.810
B	6.22	6.48	0.245	0.255
C	3.68	4.06	0.145	0.160
D	2.29	2.79	0.090	0.110
E	1.42	1.73	0.056	0.068
G	14.27 BSC		0.560 BSC	
H	2.29	2.79	0.090	0.110
K	3.43	4.19	0.135	0.165
N	7.87	8.38	0.310	0.330
Q	3.05	3.30	0.120	0.130
R	7.24	7.49	0.285	0.295

CASE 337-02

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CBO}	45	Vdc
Emitter-Base Voltage	V_{EBO}	3.5	Vdc
Collector-Current — Continuous	I_C	500	mAdc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	11 63	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

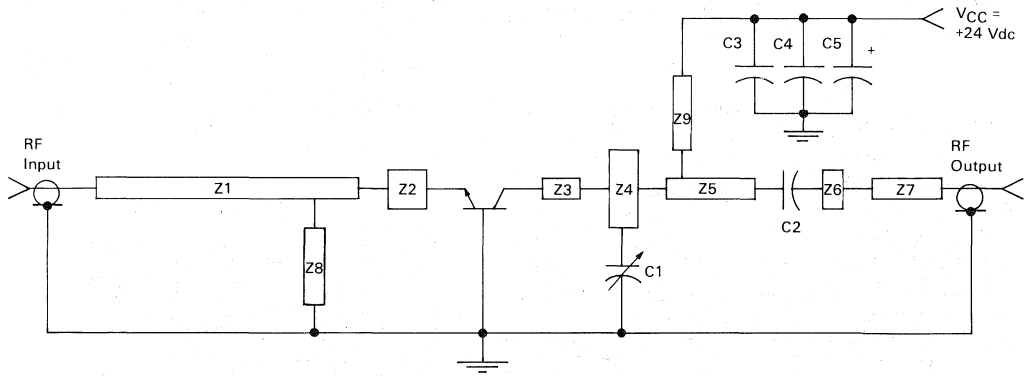
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	16	°C/W

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.
(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 5.0 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	45	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 5.0 mAdc, I_E = 0)	$V_{(BR)CBO}$	45	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 28 Vdc, I_E = 0)	I_{CBO}	—	—	0.5	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 150 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	—	100	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 24 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	4.0	6.0	pF
FUNCTIONAL TESTS					
Common-Base Amplifier Power Gain (V_{CC} = 24 Vdc, P_{out} = 3.0 W, f = 2.0 GHz)	G_{PB}	8.0	8.5	—	dB
Collector Efficiency (V_{CC} = 24 Vdc, P_{out} = 3.0 W, f = 2.0 GHz)	η	35	40		
Load Mismatch (V_{CC} = 24 Vdc, P_{out} = 3.0 W, f = 2.0 GHz VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Power Output			

FIGURE 1 — 2.0 GHz TEST CIRCUIT



Z1–Z9 — Microstrip, See Photomaster
C1 — 0.6–4.5 pF Johanson 7271
C2, C3 — 56 pF Chip Capacitor
C4 — 0.1 μF
C5 — 10 μF, 35 V
Board Material — 0.0312" Teflon Fiberglass
ϵ_r = 2.5 ± 0.05

FIGURE 2 — OUTPUT POWER versus INPUT POWER
(f = 1.7 GHz)

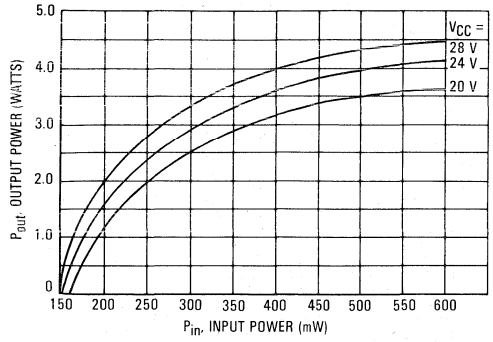


FIGURE 3 — OUTPUT POWER versus INPUT POWER
(f = 2.0 GHz)

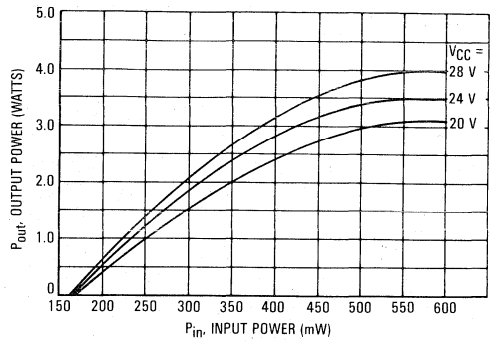


FIGURE 4 — OUTPUT POWER versus INPUT POWER
(f = 2.3 GHz)

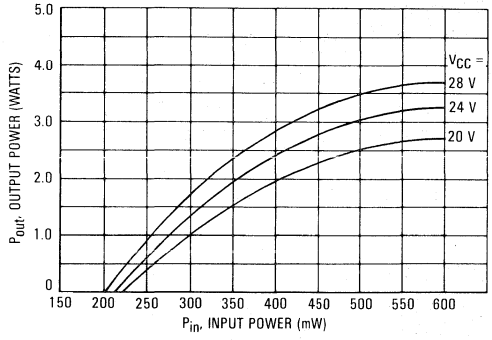


FIGURE 5 — POWER GAIN versus FREQUENCY

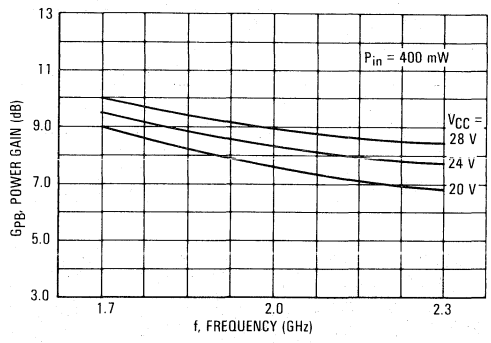
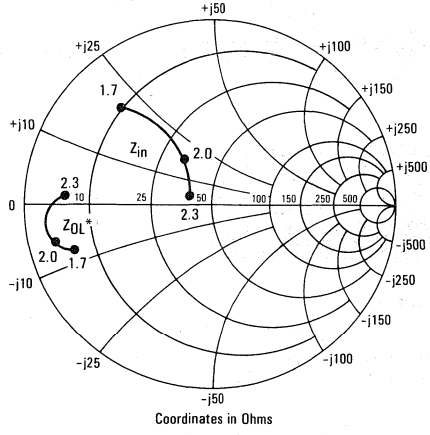


FIGURE 6 — SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCE



Coordinates in Ohms

V_{CC} = 24 V, P_{in} = 400 mW

f GHz	Z_{in} Ohms	Z_{OL}* Ohms
1.7	9.5 + j 21	6.5 – j8.5
2.0	**35 + j20**	4.0 – j5.0
2.3	41 + j3.5	**7.0 + j1.5**

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

FIGURE 7 — 2 GHz TEST AMPLIFIER

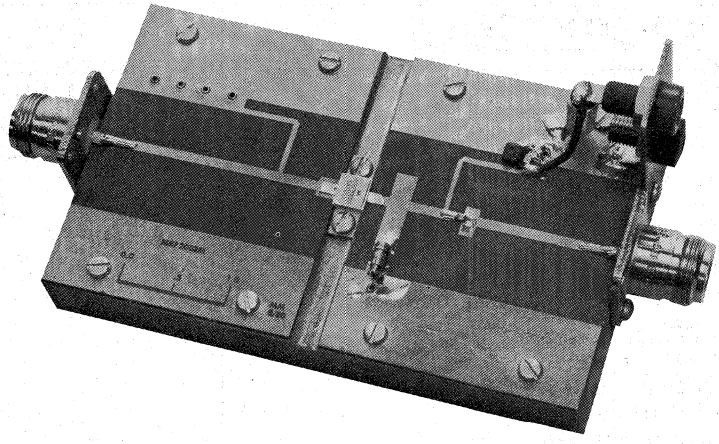
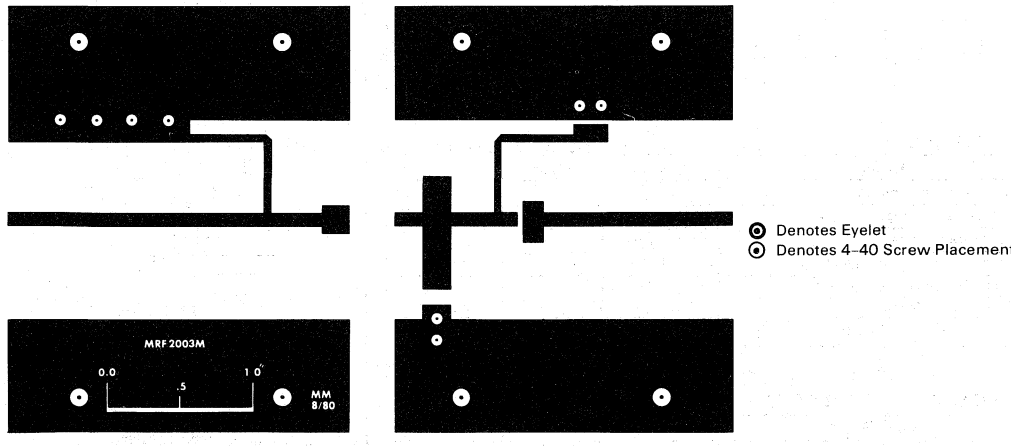


FIGURE 8 — PRINTED CIRCUIT BOARD LAYOUT — 2.0 GHz TEST CIRCUIT



NOTE: The Printed Circuit Board shown is 75% of the original.

MRF2005
MRF2005B

The RF Line

5.0 W 2 GHz

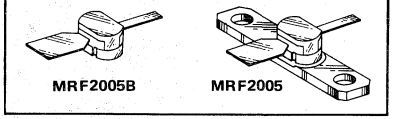
MICROWAVE POWER TRANSISTOR

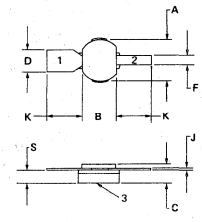
NPN SILICON

NPN SILICON MICROWAVE POWER TRANSISTOR

. . . designed for Class B and C amplifier or oscillator applications in the 1.0 to 2.3 GHz frequency range.

- Guaranteed Performance @ 2 GHz, 28 Vdc
  Output Power = 5.0 Watts
  Minimum Gain = 8.0 dB
- 100% Tested for Load Mismatch at All Phase Angles With 10:1 VSWR
- Hermetically Sealed Industry Standard Package
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Compatible with Older 2005 Types
- Other Devices in the 2000 Series:
  MRF2001 1 W
  MRF2003 3 W
  MRF2010 10 W

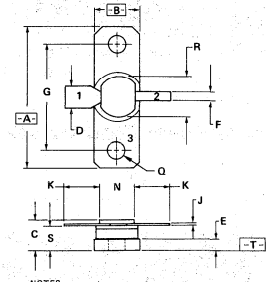




DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.72	5.97	0.225	0.235
B	4.44	4.70	0.175	0.185
C	2.29	2.74	0.090	0.108
D	2.92	3.18	0.115	0.125
F	1.14	1.40	0.045	0.055
J	0.08	0.15	0.003	0.006
K	—	9.52	—	0.375
S	1.52	1.78	0.060	0.070

STYLE 1:
1. EMITTER
2. COLLECTOR
3. BASE

CASE 328-02



NOTES:
1. [A] AND [B] ARE DATUMS.
2. [T] IS SEATING PLANE.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLES: "Q"
   ⌖ 0.15 (0.006) M T A M B M
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.19	20.57	0.795	0.810
B	6.22	6.48	0.245	0.255
C	3.68	4.19	0.145	0.165
D	2.92	3.18	0.115	0.125
E	1.40	1.65	0.055	0.065
F	1.14	1.40	0.045	0.055
G	14.22 BSC		0.560 BSC	
J	0.08	0.15	0.003	0.006
K	—	9.52	—	0.375
N	4.44	4.70	0.175	0.185
Q	3.25	3.35	0.128	0.132
R	5.72	5.97	0.225	0.235
S	2.92	3.43	0.115	0.135

STYLE 1:
1. EMITTER
2. COLLECTOR
3. BASE

CASE 328A-01

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CBO}	45	Vdc
Emitter-Base Voltage	V_{EBO}	3.5	Vdc
Collector-Current — Continuous	I_C	1.0	Adc
Total Device Dissipation @ $T_C = 25^oC$ (1) Derate above 25^oC	P_D	25 140	Watts mW/^oC
Storage Temperature Range	T_{stg}	−65 to +200	^oC

THERMAL CHARACTERISTICS

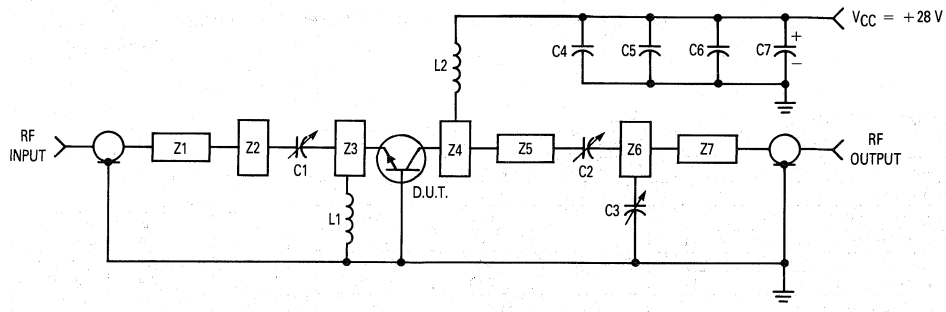
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	7.0	$^oC/W$

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.
(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, R_{BE} = 10 Ω)	$V_{(BR)CER}$	45	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 10 mAdc, I_E = 0)	$V_{(BR)CBO}$	45	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	–	–	Vdc
Collector Cutoff Current (V_{CB} = 28 Vdc, I_E = 0)	I_{CBO}	–	–	0.5	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 200 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	–	100	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	7.5	10	pF
FUNCTIONAL TESTS					
Common-Base Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 5.0 W, f = 2.0 GHz)	G_{PB}	8.0	9.0	–	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 5.0 W, f = 2.0 GHz)	η	30	35		
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 5.0 W, f = 2.0 GHz, VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Power Output			

FIGURE 1 – 2 GHz TEST CIRCUIT



Z1–Z7 — Microstrip
C1, C2, C3 — 0.6–4.5 pF Johanson
C4, C5 — 220 pF Chip Capacitor
C6 — 0.1 μF
C7 — 10 μF, 35 V Electrolytic
L1 — 3 Turns #22 1/8" I.D.
L2 — 2 Turns #24 7/32" I.D.
Board Material — 0.062" Glass Teflon

FIGURE 2 – OUTPUT POWER versus INPUT POWER (f = 1 GHz)

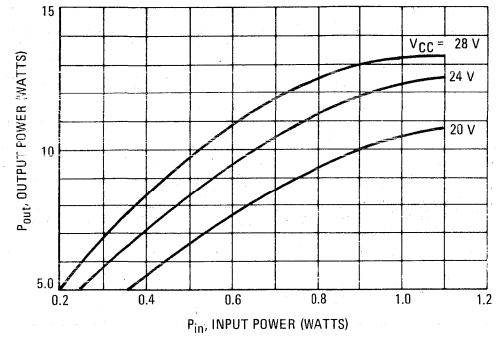


FIGURE 3 – OUTPUT POWER versus INPUT POWER (f = 2 GHz)

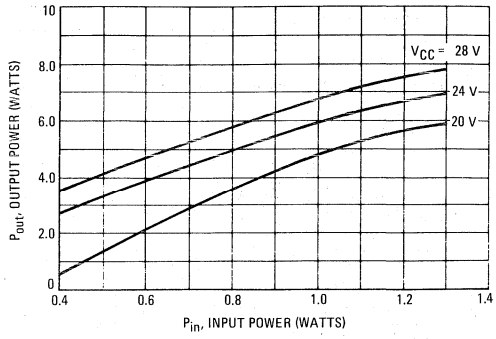


FIGURE 4 – OUTPUT POWER versus FREQUENCY

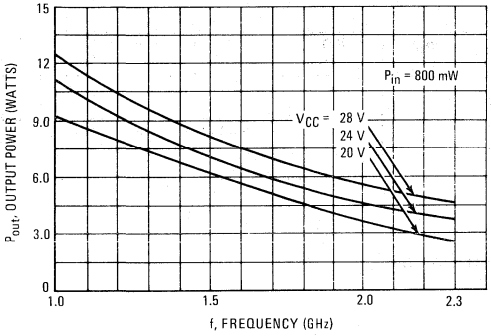


FIGURE 5 – POWER GAIN versus FREQUENCY

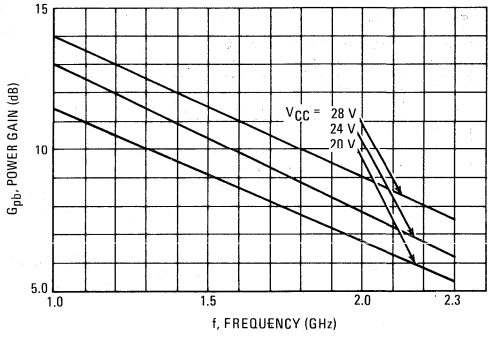
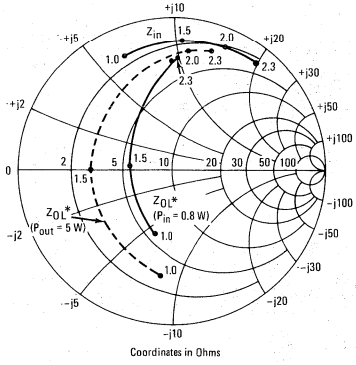


FIGURE 6 – SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCE



V_{CC} = 28 V

f GHz	Z_{in} Ohms	Z_{OL}* Ohms (P_{in} = 0.8 W)	Z_{OL}* Ohms (P_{out} = 5 W)
1.0	1.5 + j5.7	6.3 – j5.6	3.2 – j8.8
1.5	1.5 + j10.5	5.6 + j0.4	3.0 + j0
2.0	2.0 + j17	2.5 + j9.0	2.3 + j10.6
2.3	2.2 + j19.5	2.4 + j9.8	2.4 + j14.5

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

FIGURE 7 – 2 GHz TEST AMPLIFIER

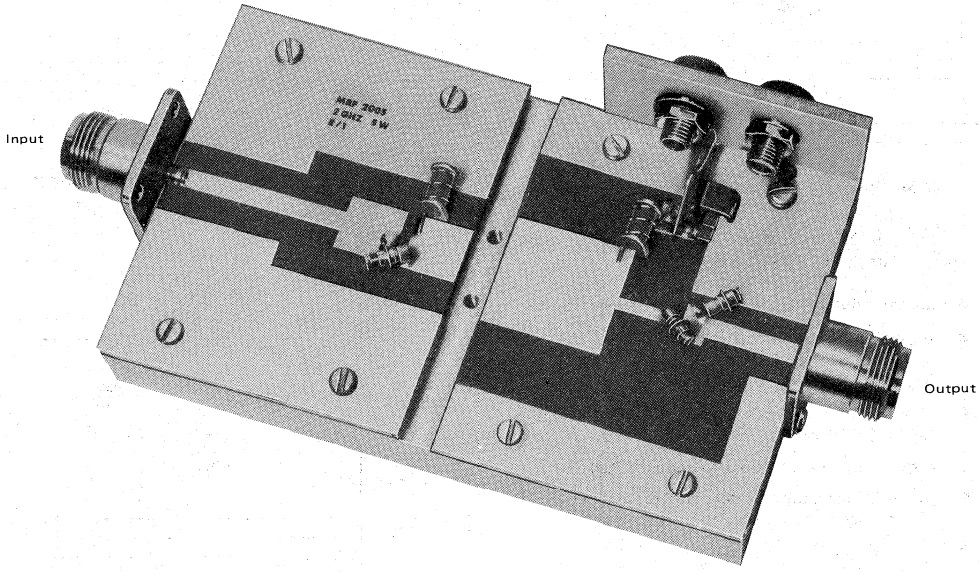
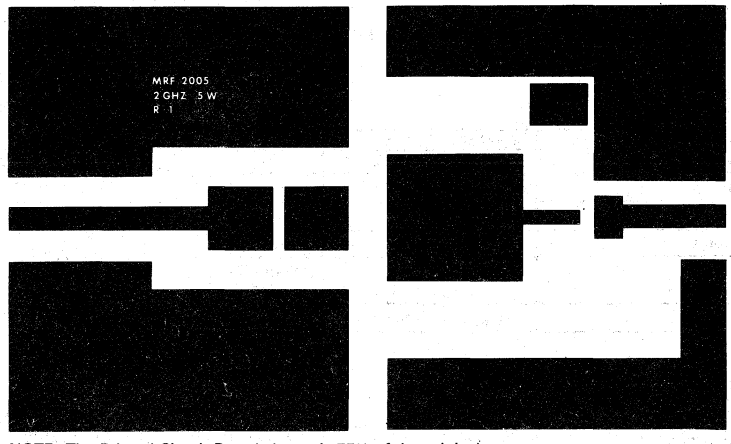


FIGURE 8 – PRINTED CIRCUIT BOARD LAYOUT – 2 GHz TEST CIRCUIT



NOTE: The Printed Circuit Board shown is 75% of the original.

MRF2005M

The RF Line

NPN SILICON MICROWAVE POWER TRANSISTOR

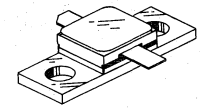
. . . designed for Class B and C *common base* broadband amplifier applications in the 1.7 to 2.3 GHz frequency range.

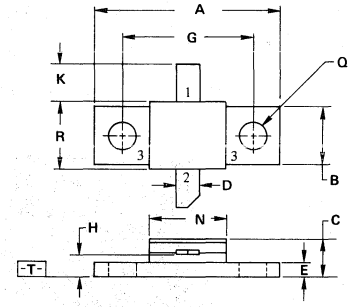
- Internal Input Matching for Broadband Operation
- Guaranteed Performance @ 2 GHz, 24 Vdc
  Output power = 5.0 Watts
  Minimum Gain = 7.5 dB
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Hermetically Sealed Industry Standard Package
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Silicon Nitride Passivation
- Characterized for Operation from 20 V to 28 V Supply Voltages

5.0 W 2 GHz

MICROWAVE POWER TRANSISTOR

NPN SILICON





STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. DIMENSIONS -A- AND -B- ARE DATUMS.
2. POSITIONAL TOLERANCE FOR MOUNTING HOLES: ⌖ Ø.13(0.005)Ⓜ T AⓂ BⓂ
3. -T- IS SEATING PLANE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	20.07	20.57	0.790	0.810
B	6.22	6.48	0.245	0.255
C	3.68	4.06	0.145	0.160
D	2.29	2.79	0.090	0.110
E	1.42	1.73	0.056	0.068
G	14.27 BSC		0.560 BSC	
H	2.29	2.79	0.090	0.110
K	3.43	4.19	0.135	0.165
N	7.87	8.38	0.310	0.330
Q	3.05	3.30	0.120	0.130
R	7.24	7.49	0.285	0.295

CASE 337-02

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CBO}	45	Vdc
Emitter-Base Voltage	V_{EBO}	3.5	Vdc
Collector-Current — Continuous	I_C	1.0	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	22 130	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

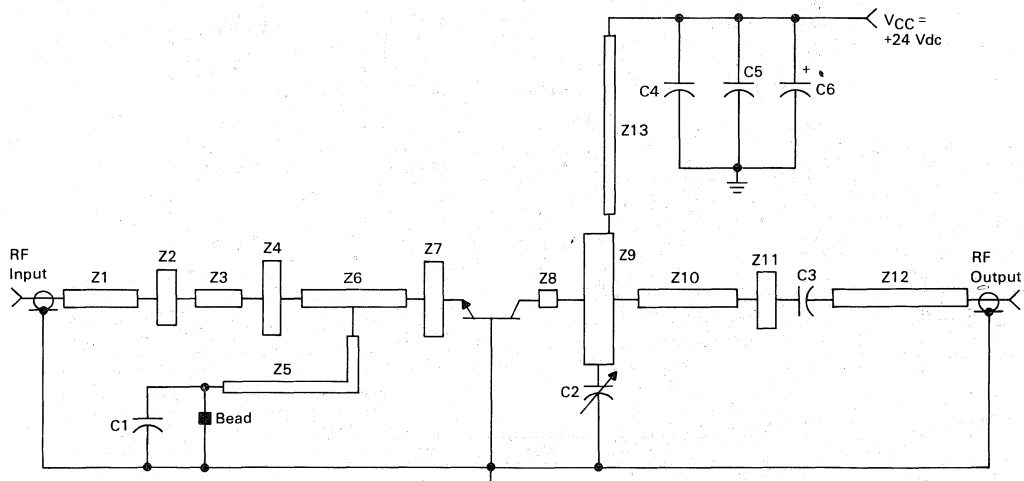
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	8.0	°C/W

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.
(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	45	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 10 mAdc, I_E = 0)	$V_{(BR)CBO}$	45	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 2.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 28 Vdc, I_E = 0)	I_{CBO}	—	—	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 300 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	—	100	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 24 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	7.5	10	pF
FUNCTIONAL TESTS					
Common-Base Amplifier Power Gain (V_{CC} = 24 Vdc, P_{out} = 5.0 W, f = 2.0 GHz)	G_{PB}	7.5	8.0	—	dB
Collector Efficiency (V_{CC} = 24 Vdc, P_{out} = 5.0 W, f = 2.0 GHz)	η	35	40		%
Load Mismatch (V_{CC} = 24 Vdc, P_{out} = 5.0 W, f = 2.0 GHz) VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Power Output			

FIGURE 1 — 2.0 GHz TEST CIRCUIT



C1, C3, C4 — 68 pF Chip Capacitor
C2 — 0.6-4.5 pF Johanson 7271
C5 — 0.1 μF
C6 — 10 μF, 35 V
Z1-Z13 — Microstrip, See Photomaster, Figure 8.

Bead — Ferroxcube 56-590-65/3B
Board Material — 0.031" Teflon Fiberglass
ϵ_r = 2.5 ± 0.05

FIGURE 2 — OUTPUT POWER versus INPUT POWER (f = 1.7 GHz)

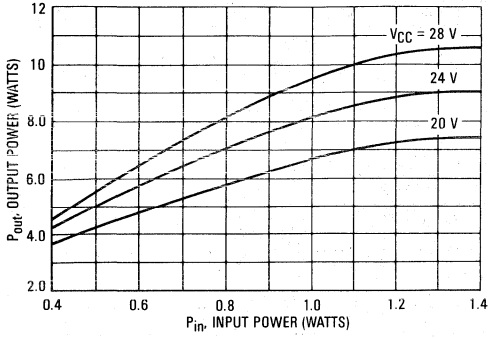


FIGURE 3 — OUTPUT POWER versus INPUT POWER (f = 2.0 GHz)

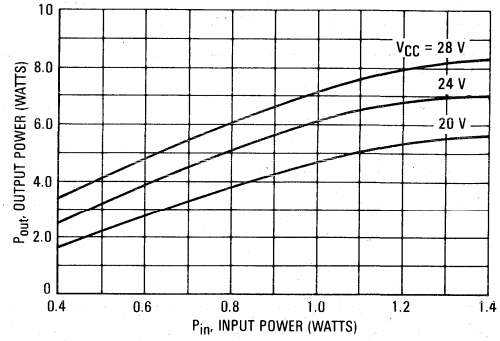


FIGURE 4 — OUTPUT POWER versus INPUT POWER (f = 2.3 GHz)

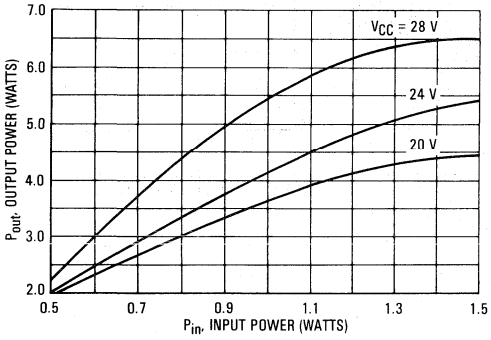


FIGURE 5 — POWER GAIN versus FREQUENCY

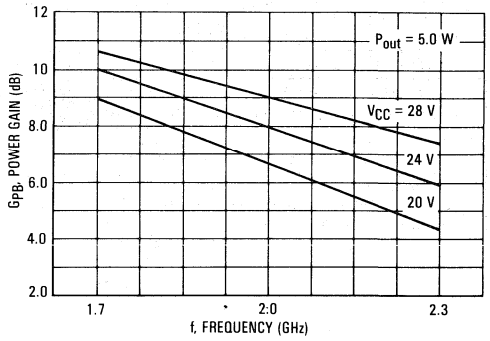
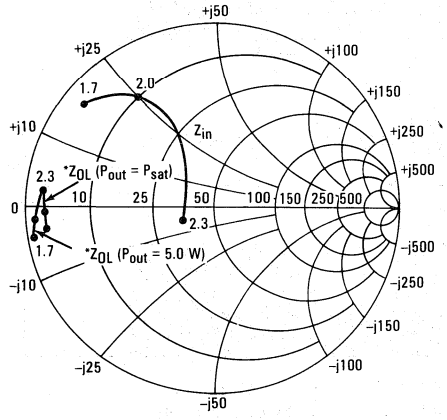


FIGURE 6 — SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCE



Coordinates in Ohms

V_{CC} = 24 V

f GHz	Z_{in} Ohms	Z_{OL}*, Ohms P_{out} = P_{sat}	Z_{OL}*, Ohms P_{out} = 5.0 W
1.7	4.0 + j17	2.9 – j3.5	1.5 – j4.4
2.0	10 + j25	3.1 – j0.85	1.75 – j1.3
2.3	37 – j5.0	2.9 + j2.2	2.90 + j2.2

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

FIGURE 7 — 2 GHz TEST AMPLIFIER

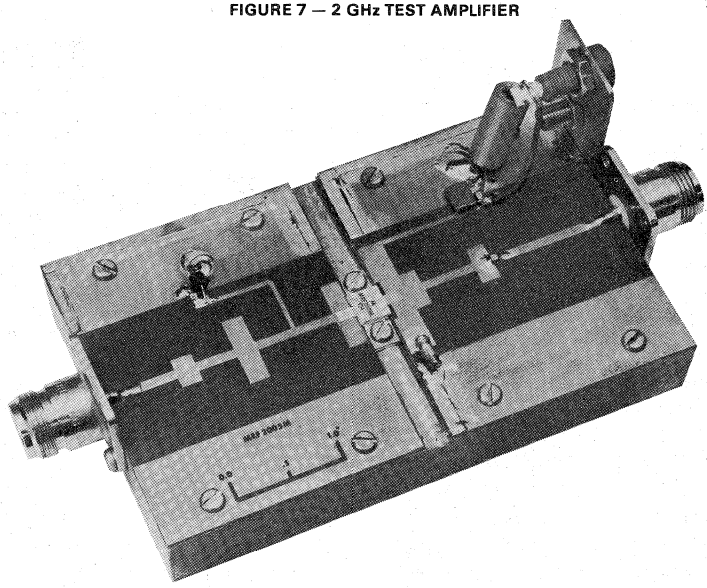
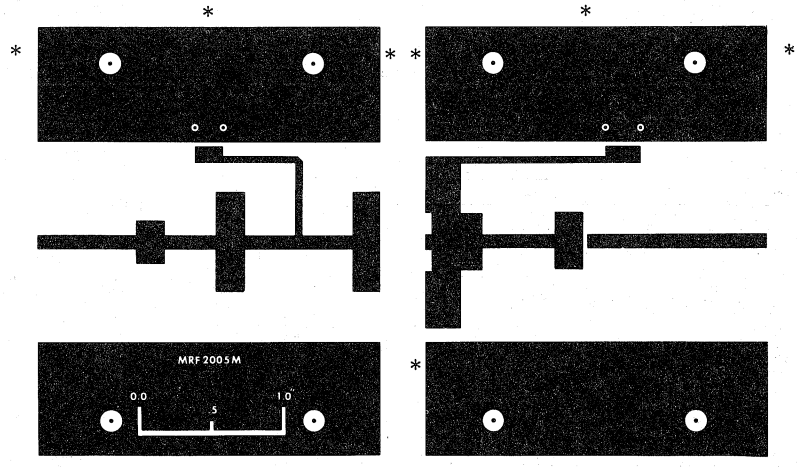


FIGURE 8 — PRINTED CIRCUIT BOARD LAYOUT — 2.0 GHz TEST CIRCUIT



⊙ Denotes Eyelet
⊙ 4-40 Screw Placement
* Foil Wrap to Bottom Ground Plane

NOTE: The Printed Circuit Board shown is 75% of the original.

MRF2010
MRF2010B

The RF Line

10 W 2 GHz

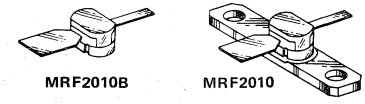
MICROWAVE POWER TRANSISTOR

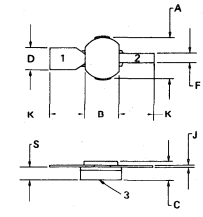
NPN SILICON

NPN SILICON MICROWAVE POWER TRANSISTOR

. . . designed for Class B and C amplifier or oscillator applications in the 1.0 to 2.3 GHz frequency range.

- Guaranteed Performance @ 2 GHz, 28 Vdc
  Output Power = 10 Watts
  Minimum Gain = 6.0 dB
- 100% Tested for Load Mismatch at All Phase Angles With 10:1 VSWR
- Hermetically Sealed Industry Standard Package
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Compatible with Older 2010 Types
- Other Devices in the 2000 Series:
  MRF2001 1 W
  MRF2003 3 W
  MRF2005 5 W

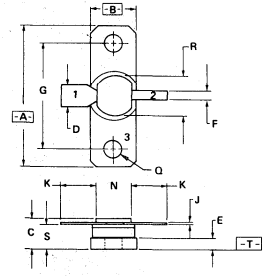




DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.72	5.97	0.225	0.235
B	4.44	4.70	0.175	0.185
C	2.29	2.54	0.090	0.100
D	2.92	3.18	0.115	0.125
F	1.14	1.40	0.045	0.055
J	0.08	0.15	0.003	0.006
K	–	9.52	–	0.375
S	1.52	1.78	0.060	0.070

STYLE 1:
1. EMITTER
2. COLLECTOR
3. BASE

CASE 328-02



NOTES:
1. -A- AND -B- ARE DATUMS.
2. -T- IS SEATING PLANE.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLES: "Q"
   ⌖ 0.15 (0.006) M T A M B M
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.19	20.57	0.795	0.810
B	6.22	6.48	0.245	0.255
C	3.68	4.19	0.145	0.165
D	2.92	3.18	0.115	0.125
E	1.40	1.65	0.055	0.065
F	1.14	1.40	0.045	0.055
G	14.22 BSC		0.560 BSC	
J	0.08	0.15	0.003	0.006
K	–	9.52	–	0.375
N	4.44	4.70	0.175	0.185
Q	3.25	3.35	0.128	0.132
R	5.72	5.97	0.225	0.235
S	2.92	3.43	0.115	0.135

STYLE 1:
1. EMITTER
2. COLLECTOR
3. BASE

CASE 328A-01

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CBO}	45	Vdc
Emitter-Base Voltage	V_{EBO}	3.5	Vdc
Collector-Current — Continuous	I_C	2.0	Adc
Total Device Dissipation @ $T_C = 25^oC$ (1) Derate above 25^oC	P_D	35 200	Watts mW/^oC
Storage Temperature Range	T_{stg}	−65 to +200	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	5.0	$^oC/W$

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

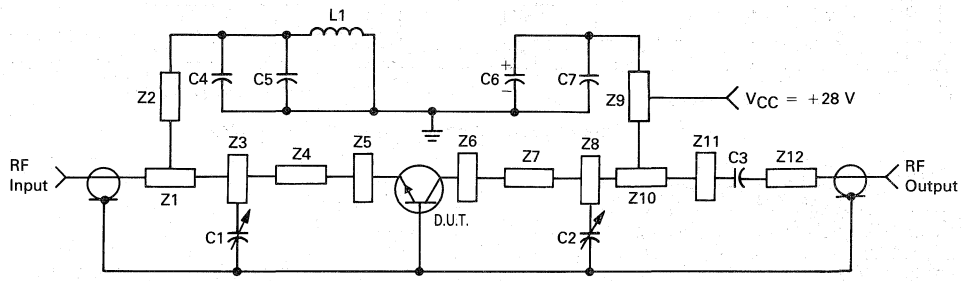
(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

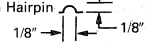
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, R_{BE} = 10 Ω)	$V_{(BR)CER}$	45	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 20 mAdc, I_E = 0)	$V_{(BR)CBO}$	45	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 2.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	–	–	Vdc
Collector Cutoff Current (V_{CB} = 28 Vdc, I_E = 0)	I_{CBO}	–	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	–	100	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	12	15	pF
FUNCTIONAL TESTS					
Common-Base Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 10 W f = 2.0 GHz)	G_{PB}	6.0	7.0	–	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 10 W, f = 2.0 GHz)	η	30	35		
Load Mismatch (V_{CC} = 28 Vdc, P_{out} = 10 W, f = 2.0 GHz, VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Power Output			

3

FIGURE 1 – 2 GHz TEST CIRCUIT



Z1–Z12 — Microstrip
C1, C2 — 0.4–2.5 pF Johanson
C3, C4, C5, C7 — 39 pF Chip Capacitor
C6 — 20 μF, 50 V Electrolytic
L1 — #18 AWG Hairpin



Board Material — 0.032" Glass Teflon

FIGURE 2 – OUTPUT POWER versus INPUT POWER
(f = 1.0 GHz)

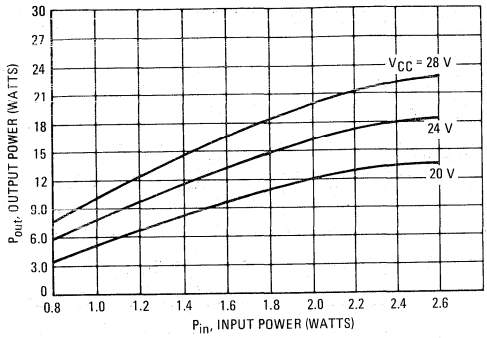


FIGURE 3 – OUTPUT POWER versus INPUT POWER
(f = 2.0 GHz)

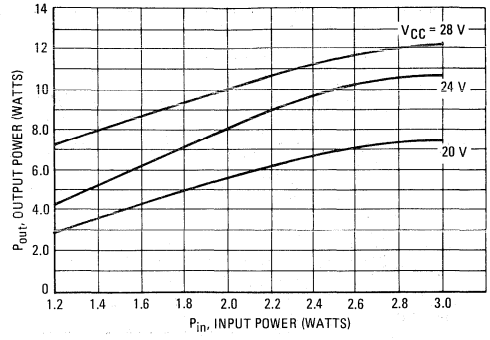


FIGURE 4 – OUTPUT POWER versus FREQUENCY

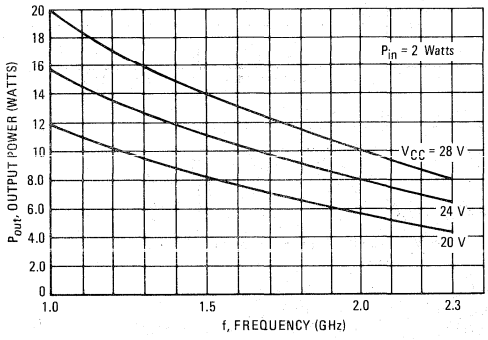


FIGURE 5 – POWER GAIN versus FREQUENCY

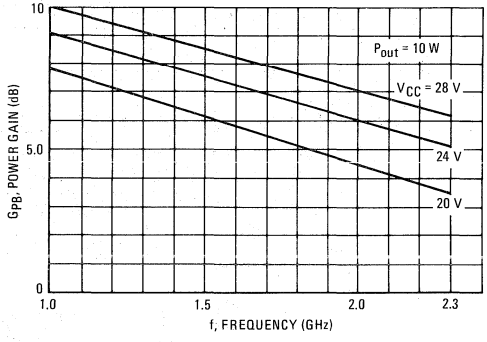
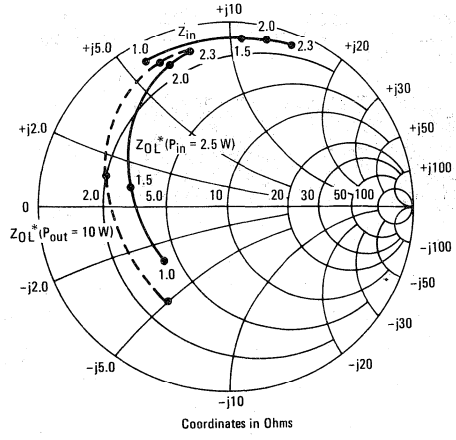


FIGURE 6 – SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCE



V_{CC} = 28 V

f GHz	Z_{in} Ohms	Z_{OL}^* P_{in} = 2.5 W Ohms	Z_{OL}^* P_{out} = 10 W Ohms
1.0	1.0 + j6.0	4.5 – j3.0	3.2 – j5.0
1.5	1.0 + j11	3.5 + j1.0	2.0 + j1.3
2.0	1.5 + j13	1.5 + j7.0	1.4 + j6.5
2.3	1.5 + j16	1.3 + j8.0	1.3 + j8.0

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

FIGURE 7 – 2 GHz TEST AMPLIFIER

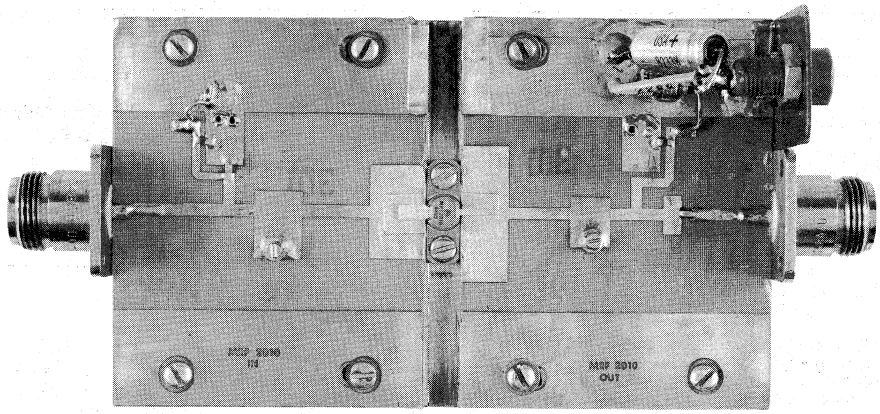
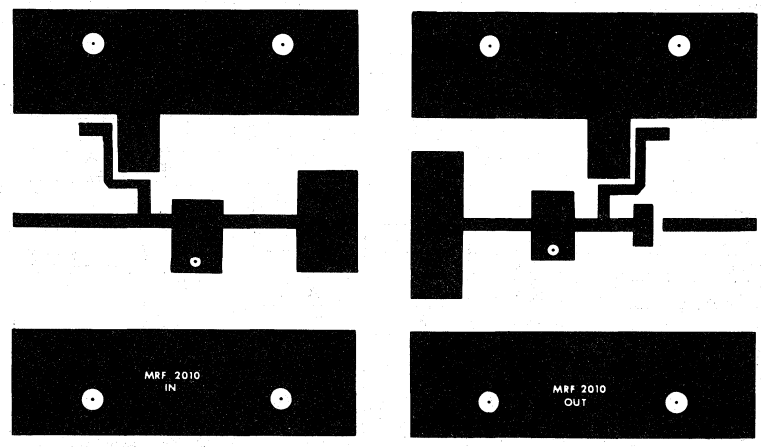


FIGURE 8 – PRINTED CIRCUIT BOARD LAYOUT – 2 GHz TEST CIRCUIT



NOTE: The Printed Circuit Board shown is 75% of the original.

3

MRF2010M

The RF Line

NPN SILICON MICROWAVE POWER TRANSISTOR

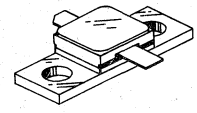
. . . designed for Class B and C *common base* broadband amplifier applications in the 1.7 to 2.3 GHz frequency range.

- Internal Input Matching for Broadband Operation
- Guaranteed Performance @ 2 GHz, 24 Vdc
  Output Power = 10 Watts
  Minimum Gain = 7.0 dB
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Hermetically Sealed Industry Standard Package
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Silicon Nitride Passivation
- Characterized for Operation from 20 V to 28 V Supply Voltages

10 W 2 GHz

MICROWAVE POWER TRANSISTOR

NPN SILICON



3

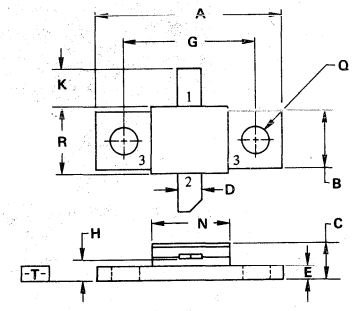
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CBO}	45	Vdc
Emitter-Base Voltage	V_{EBO}	3.5	Vdc
Collector-Current — Continuous	I_C	2.0	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	35 200	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	5.0	°C/W

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.
(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.



NOTES:
1. DIMENSIONS -A- AND -B- ARE DATUMS.
2. POSITIONAL TOLERANCE FOR MOUNTING HOLES: ⌖ ø.13(0.005)Ⓜ T AⓂ BⓂ
3. -T- IS SEATING PLANE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.07	20.57	0.790	0.810
B	6.22	6.48	0.245	0.255
C	3.68	4.06	0.145	0.160
D	2.29	2.79	0.090	0.110
E	1.42	1.73	0.056	0.068
G	14.27 BSC		0.560 BSC	
H	2.29	2.79	0.090	0.110
K	3.43	4.19	0.135	0.165
N	7.87	8.38	0.310	0.330
Q	3.05	3.30	0.120	0.130
R	7.24	7.49	0.285	0.295

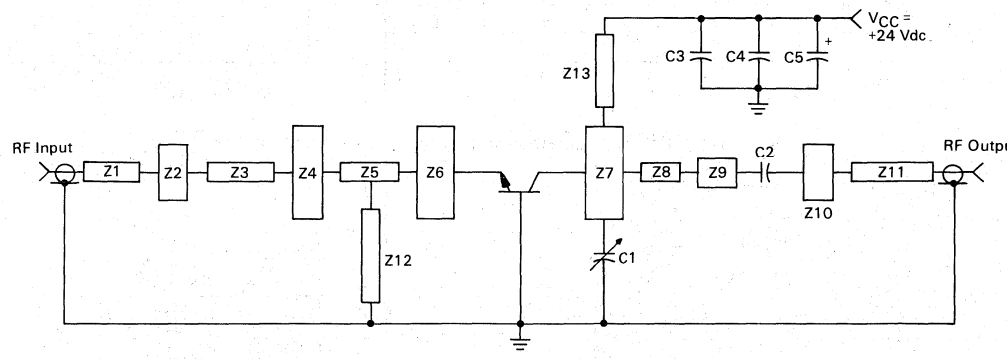
CASE 337-02

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	45	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 20 mAdc, I_E = 0)	$V_{(BR)CBO}$	45	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 2.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 28 Vdc, I_E = 0)	I_{CBO}	—	—	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	—	100	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 24 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	14	18	pF
FUNCTIONAL TESTS					
Common-Base Amplifier Power Gain (V_{CC} = 24 Vdc, P_{out} = 10 W, f = 2.0 GHz)	G_{PB}	7.0	8.0	—	dB
Collector Efficiency (V_{CC} = 24 Vdc, P_{out} = 10 W, f = 2.0 GHz)	η	35	40		
Load Mismatch (V_{CC} = 24 Vdc, P_{out} = 10 W, f = 2.0 GHz, VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Power Output			

3

FIGURE 1 — 2 GHz TEST CIRCUIT



Z1–Z13 — Microstrip, See Photomaster, Figure 8.
C2, C3 — 68 pF Chip Capacitor
C4 — 0.1 μF
C5 — 10 μF, 35 V
C1 — 0.6–4.5 pF Johanson 7271
Board Material — 0.0312" Teflon Fiberglass
ϵ_r = 2.5 ± 0.05

FIGURE 2 — OUTPUT POWER versus INPUT POWER
(f = 1.7 GHz)

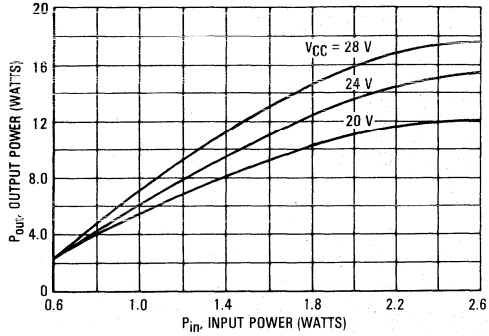


FIGURE 3 — OUTPUT POWER versus INPUT POWER
(f = 2.0 GHz)

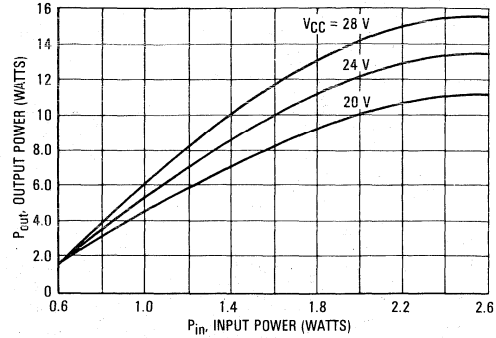


FIGURE 4 — OUTPUT POWER versus INPUT POWER
(f = 2.3 GHz)

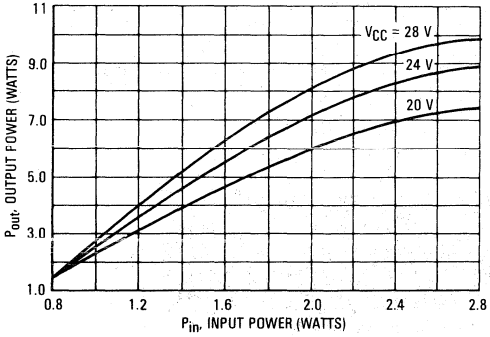


FIGURE 5 — POWER GAIN versus FREQUENCY

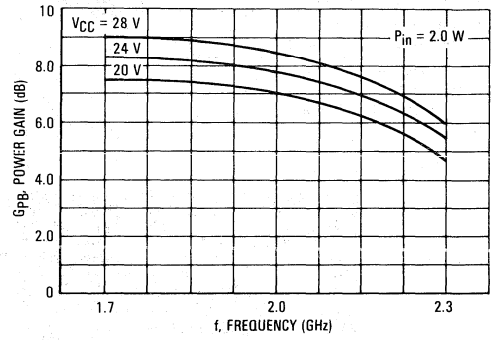
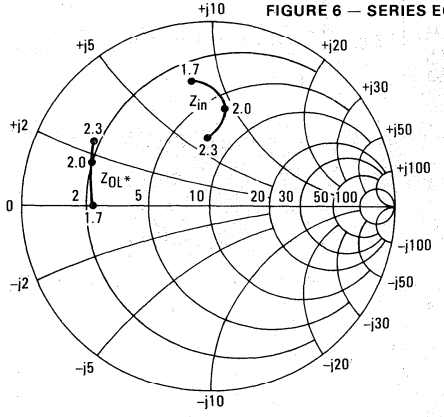


FIGURE 6 — SERIES EQUIVALENT INPUT/OUTPUT IMPEDANCE



V_{CC} = 24 V, P_{in} = 2.0 W

f GHz	Z_{in} Ohms	Z_{OL}* Ohms
1.7	3.5 + j8.0	2.3 + j0
2.0	7.0 + j9.5	2.0 + j1.6
2.3	8.0 + j6.5	1.8 + j2.2

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

FIGURE 7 — 2 GHz TEST AMPLIFIER

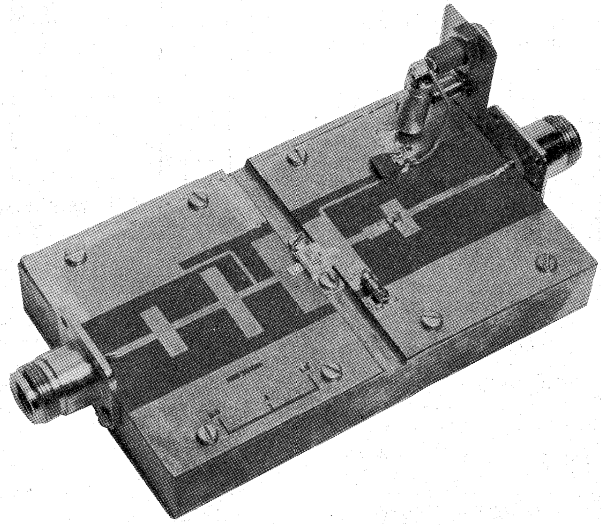
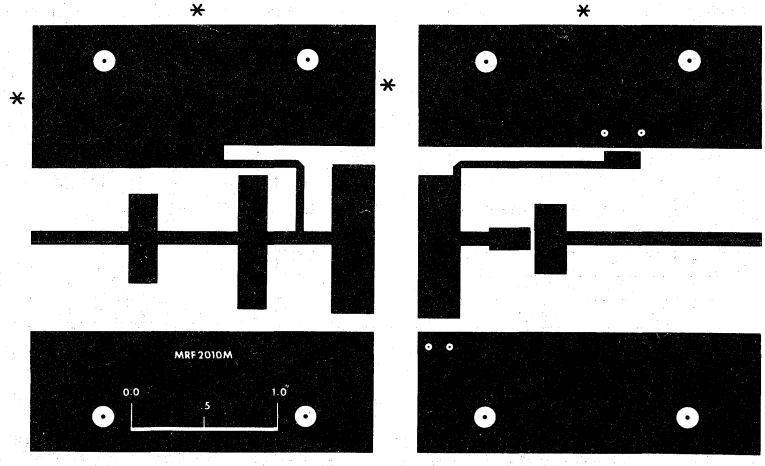


FIGURE 8 — 2 GHz TEST CIRCUIT PHOTOMASTER



⊙ Denotes Eyelet
⊙ Denotes 4–40 Screw Placement
✱ Foil Wrap to Bottom Ground Plane

NOTE: The Printed Circuit Board shown is 75% of the original.

MRF2016M

The RF Line

16 W 2 GHz

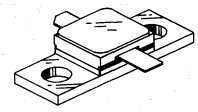
MICROWAVE POWER TRANSISTOR

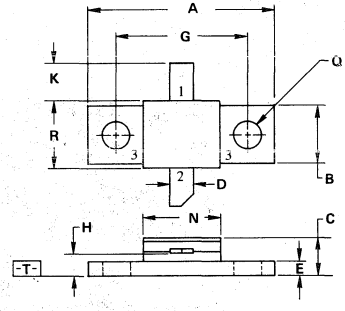
NPN SILICON

NPN SILICON MICROWAVE POWER TRANSISTOR

. . . designed for Class B and C *common base* broadband amplifier applications in the 1.7 to 2.3 GHz frequency range.

- Internal Input Matching for Broadband Operation
- Guaranteed Performance @ 2 GHz, 24 Vdc
  Output power = 16 Watts
  Minimum Gain = 6.5 dB
- 100% Tested for Load Mismatch at All Phase Angles with 10:1 VSWR
- Hermetically Sealed Industry Standard Package
- Gold Metallized, Emitter Ballasted for Long Life and Resistance to Metal Migration
- Silicon Nitride Passivation
- Characterized for Operation from 20 V to 28 V Supply Voltages





NOTES:
1. DIMENSIONS -A- AND -B- ARE DATUMS.
2. POSITIONAL TOLERANCE FOR MOUNTING HOLES: ⌖ ø.13(0.005)Ⓜ T AⓂ BⓂ
3. -T- IS SEATING PLANE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.07	20.57	0.790	0.810
B	6.22	6.48	0.245	0.255
C	3.68	4.06	0.145	0.160
D	2.29	2.79	0.090	0.110
E	1.42	1.73	0.056	0.068
G	14.27 BSC		0.560 BSC	
H	2.29	2.79	0.090	0.110
K	3.43	4.19	0.135	0.165
N	7.87	8.38	0.310	0.330
Q	3.05	3.30	0.120	0.130
R	7.24	7.49	0.285	0.295

CASE 337-02

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CBO}	45	Vdc
Emitter-Base Voltage	V_{EBO}	3.5	Vdc
Collector-Current — Continuous	I_C	3.0	Adc
Total Device Dissipation @ T_C = 25°C (1) Derate above 25°C	P_D	50 286	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	3.5	°C/W

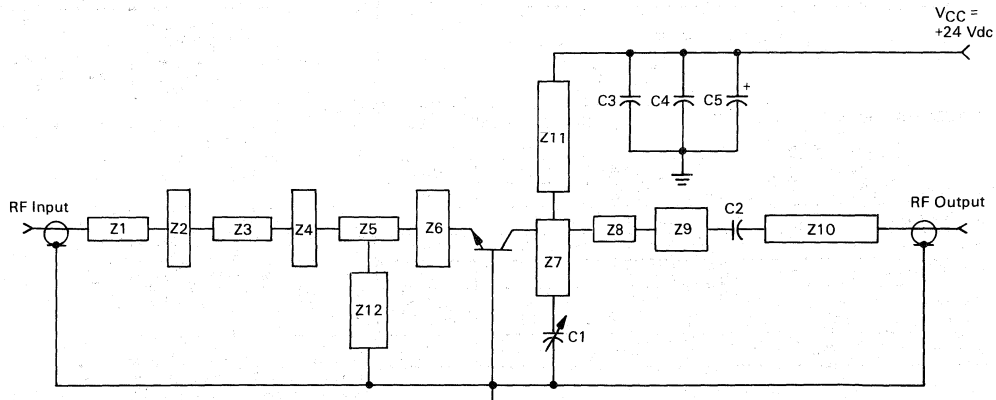
(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.
(2) Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 30 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 30 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	45	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 30 mAdc, I_E = 0)	$V_{(BR)CBO}$	45	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	3.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 28 Vdc, I_E = 0)	I_{CBO}	—	—	3.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	—	100	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 24 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	20	25	pF
FUNCTIONAL TESTS					
Common-Base Amplifier Power Gain (V_{CC} = 24 Vdc, P_{out} = 16 W, f = 2.0 GHz)	G_{PB}	6.5	7.0	—	dB
Collector Efficiency (V_{CC} = 24 Vdc, P_{out} = 16 W, f = 2.0 GHz)	η	35	40		%
Load Mismatch (V_{CC} = 24 Vdc, P_{out} = 16 W, f = 2.0 GHz) VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Power Output			

3

FIGURE 1 — 2 GHz TEST CIRCUIT



C1 — 0.6-4.5 pF Johanson 7271
C2, C3 — 68 pF Chip Capacitor
C4 — 0.1 μF
C5 — 10 μF, 35 V
Z1-Z12 — Microstrip, See Photomaster

Board Material — 0.031 " Teflon Fiberglass
ϵ_r = 2.5 ± 0.05

FIGURE 2 — OUTPUT POWER versus INPUT POWER
(f = 1.7 GHz)

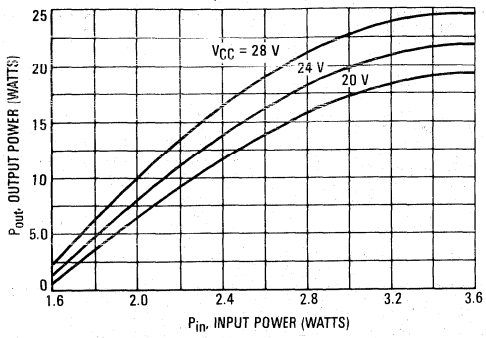


FIGURE 3 — OUTPUT POWER versus INPUT POWER
(f = 2.0 GHz)

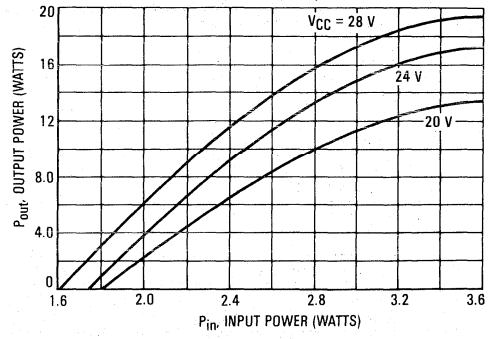


FIGURE 4 — OUTPUT POWER versus INPUT POWER
(f = 2.3 GHz)

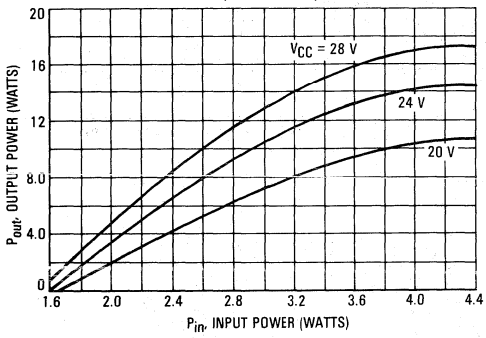
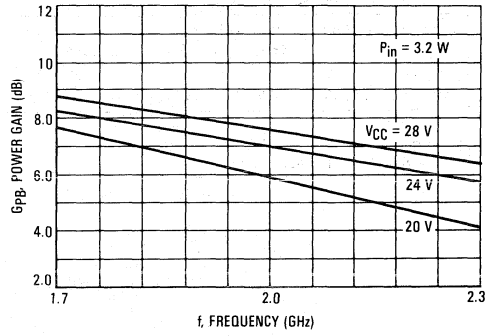


FIGURE 5 — POWER GAIN versus FREQUENCY



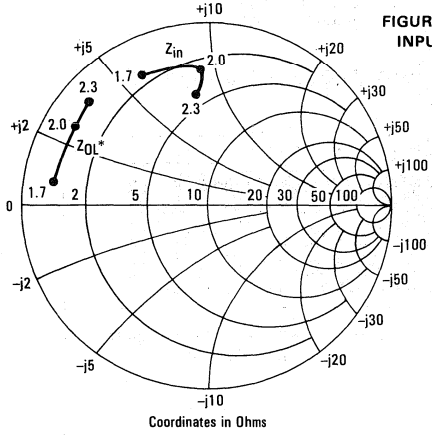


FIGURE 6 — SERIES EQUIVALENT
INPUT/OUTPUT IMPEDANCE

V_{CC} = 24 V, P_{in} = 3.2 W

f GHz	Z_{in} Ohms	Z_{OL}* Ohms
1.7	1.8 + j6.1	1.2 + j1.0
2.0	2.4 + j9.2	1.0 + j2.6
2.3	4.4 + j8.3	1.0 + j3.5

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

FIGURE 7 — 2 GHz TEST AMPLIFIER

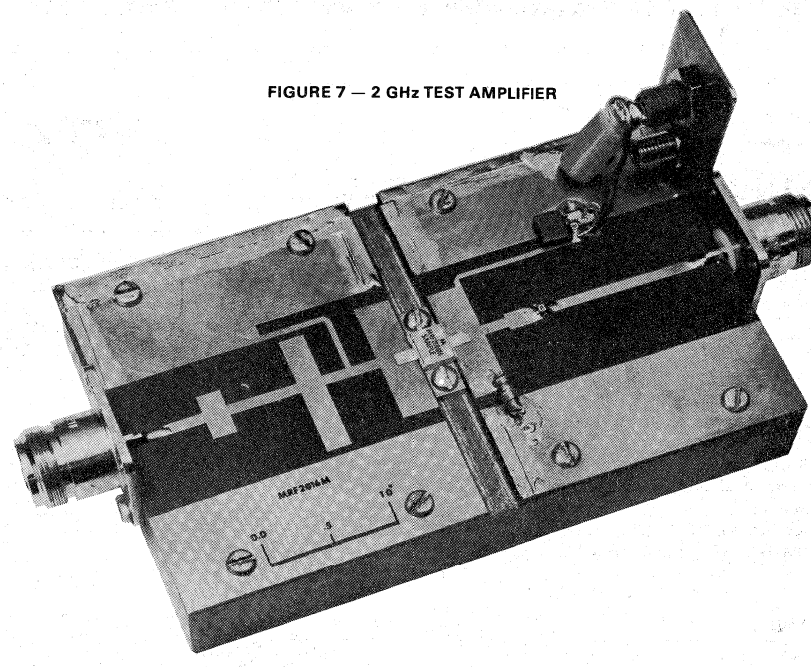
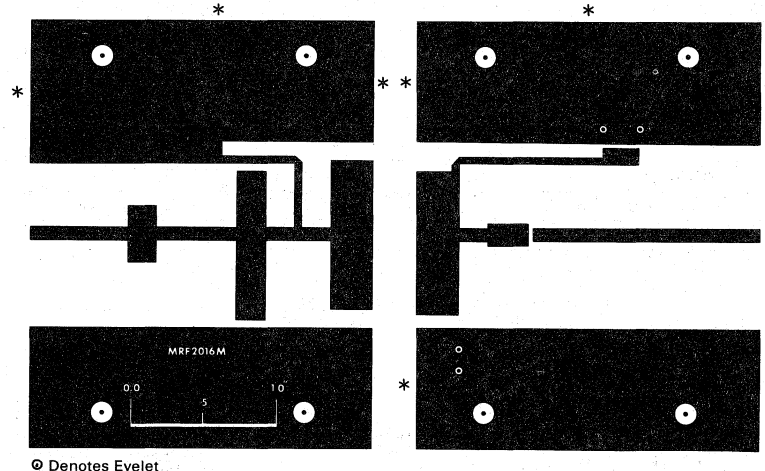


FIGURE 8 — PRINTED CIRCUIT BOARD LAYOUT — 2 GHz TEST CIRCUIT

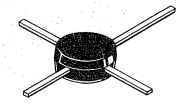


⊙ Denotes Eyelet
⊙ 4–40 Screw Placement
∗ Foil Wrap to Bottom Ground Plane

NOTE: The Printed Circuit Board shown is 75% of the original.

MRF2369

f_T = 6 GHz @ 50 mA
NF = 1.5 dB @ 1 GHz
HIGH FREQUENCY
TRANSISTOR
NPN SILICON



The RF Line

NPN Silicon High Frequency Transistors

. . . designed for low-noise, wide dynamic range front end amplifiers, low-noise VCO's and microwave power multipliers.

- Low Noise
- High Gain
- Available in Low Cost Plastic
- State-of-the-Art Technology
  - Fine Line Geometry
  - Ion Implanted Arsenic Emitters
  - Gold Top Metallization and Wires
  - Silicon Nitride Passivation
- Fully Characterized
- Higher Voltage Version of MRF571
- Internally Ballasted for Improved Ruggedness

3

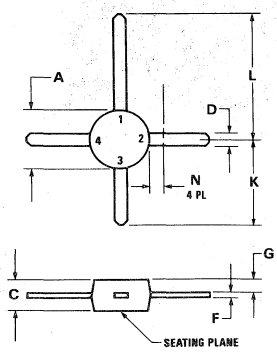
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CBO}	30	Vdc
Emitter-Base Voltage	V_{EBO}	2.5	Vdc
Collector Current — Continuous	I_C	70	mAdc
Total Device Dissipation @ T_C = 50°C (1) Derate above 50°C	P_D	0.75 7.5	Watt mW/°C
Storage Temperature	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	133	°C/W

OUTLINE DIMENSIONS



STYLE 2:
PIN 1. COLLECTOR
2. EMITTER
3. BASE
4. EMITTER

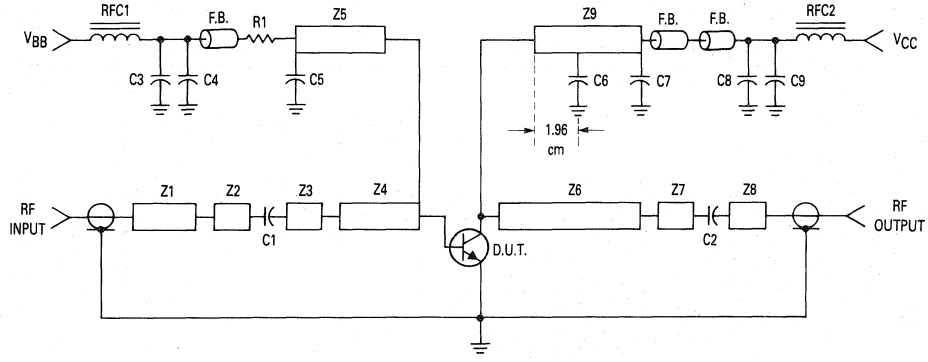
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.44	5.21	0.175	0.205
C	1.90	2.54	0.075	0.100
D	0.84	0.99	0.033	0.039
F	0.20	0.30	0.008	0.012
G	0.76	1.14	0.030	0.045
K	7.24	8.13	0.285	0.320
L	10.54	11.43	0.415	0.450
N	–	1.65	–	0.065

NOTE:
DIMENSION D NOT APPLICABLE IN ZONE N.

MACRO-X
CASE 317-01

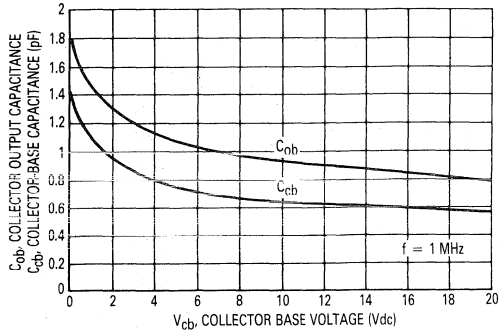
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 1 mAdc, I_B = 0)		$V_{(BR)CEO}$	15	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)		$V_{(BR)CBO}$	30	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 50 μAdc, I_C = 0)		$V_{(BR)EBO}$	2.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)		I_{CBO}	—	—	10	μAdc
ON CHARACTERISTICS						
DC Current Gain (I_C = 30 mAdc, V_{CE} = 5 Vdc)		h_{FE}	50	—	300	—
DYNAMIC CHARACTERISTICS						
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)		C_{cb}	—	0.7	1	pF
Current Gain — Bandwidth Product (V_{CE} = 10 Vdc, I_C = 40 mA, f = 1 GHz)		f_T	—	6	—	GHz
FUNCTIONAL TESTS						
Gain @ Noise Figure (I_C = 5 mAdc, V_{CE} = 10 Vdc)	f = 0.5 GHz f = 1 GHz	G_{NF}	— 10	16.5 12	— —	dB
Noise Figure (I_C = 5 mAdc, V_{CE} = 10 Vdc)	f = 0.5 GHz f = 1 GHz f = 2 GHz	NF	— — —	1 1.5 2.8	— 2 —	dB



C1, C2, C6	560 pF Chip Capacitor	RFC1, RFC2	VK-200, Ferroxcube
C5, C7	0.018 μF Chip Capacitor	Z1–Z9	Microstrip, See Photomaster
C3, C8	0.1 μF Mylar Capacitor	Bead	Ferrite Bead, Ferroxcube 56-590-65/3B
C4, C9	1 μF Electrolytic Capacitor	Board Material	0.0625″ Teflon Fiberglass ϵ_r = 2.5 ± 0.05
R1	2.7 kΩ		

Figure 1. MRF2369 1 GHz Test Circuit



C_{ob}, Collector Output Capacitance
Figure 2. C_{cb}, Collector-Base Capacitance versus Voltage

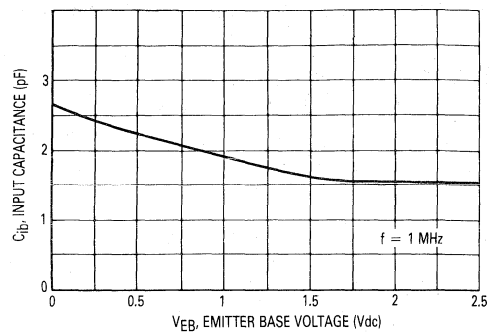


Figure 3. C_{ib}, Input Capacitance versus Emitter Base Voltage

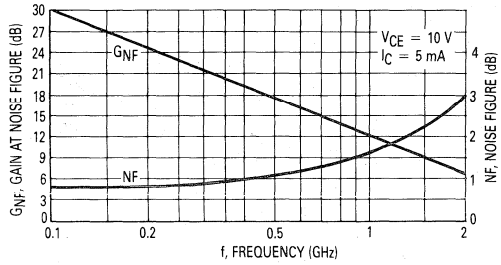


Figure 4. Gain at Noise Figure and Noise Figure versus Frequency

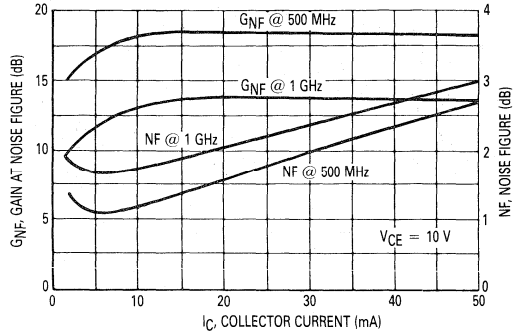


Figure 5. Gain at Noise Figure and Noise Figure versus Collector Current

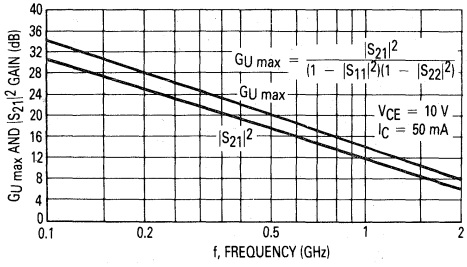


Figure 6. $G_{U\,max}$ and $|S_{21}|^2$ versus Frequency

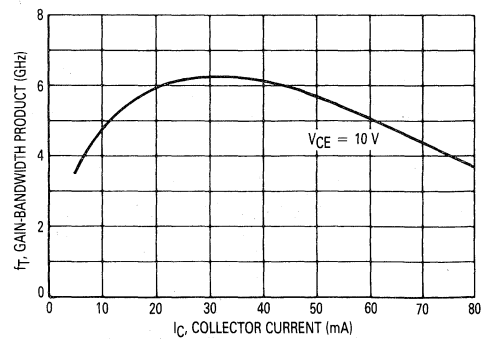
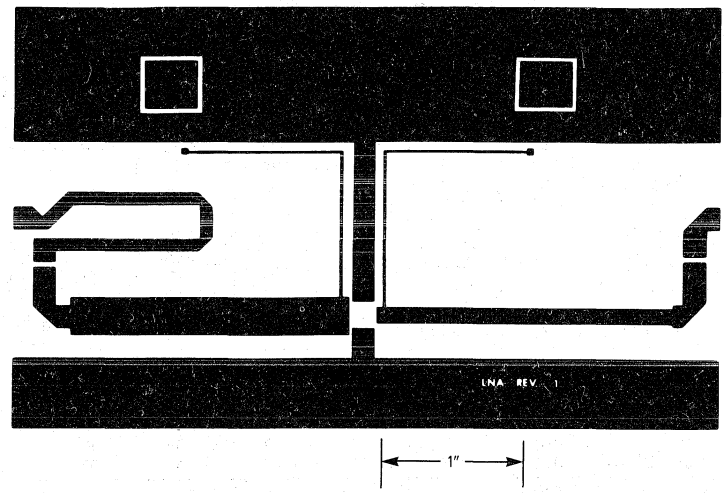


Figure 7. Gain-Bandwidth Product versus Collector Current

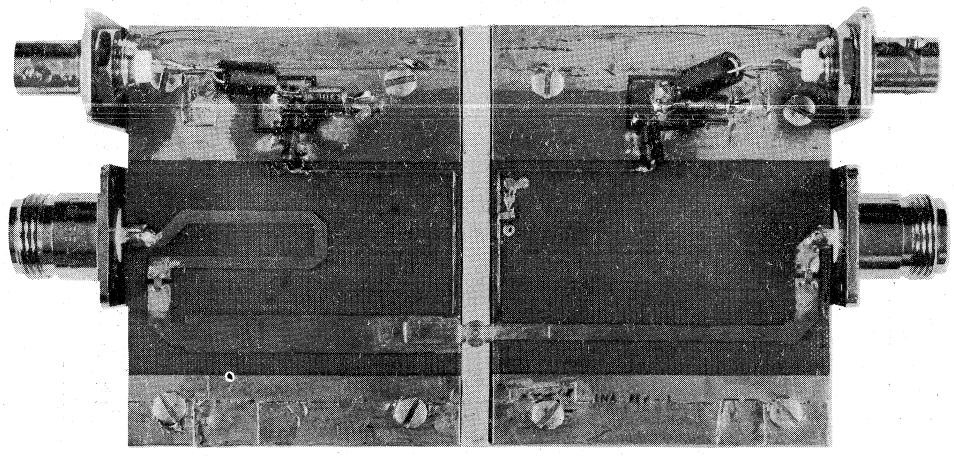
MRF2369 Common Emitter S-Parameters

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
5	5	100	0.83	−45	14.1	152	0.03	69	0.88	−24
		200	0.70	−81	10.5	130	0.06	51	0.74	−37
		500	0.63	−140	5.7	98	0.08	35	0.47	−57
		1000	0.59	175	3	72	0.10	38	0.36	−68
		1500	0.57	150	2	56	0.12	45	0.35	−85
		2000	0.56	128	1.5	43	0.15	50	0.37	−96
	10	100	0.72	−63	21.2	142	0.03	61	0.83	−33
		200	0.63	−103	14.4	122	0.05	49	0.60	−51
		500	0.59	−156	7	93	0.07	42	0.35	−69
		1000	0.56	166	3.6	71	0.09	50	0.24	−79
		1500	0.55	143	2.4	57	0.12	55	0.24	−95
		2000	0.53	123	1.8	45	0.16	55	0.26	−101
	25	100	0.54	−93	29.1	132	0.02	63	0.68	−47
		200	0.57	−132	17.9	111	0.03	50	0.45	−66
		500	0.57	−173	7.9	88	0.05	53	0.23	−83
		1000	0.55	157	3.9	70	0.09	62	0.15	−93
		1500	0.54	137	2.6	57	0.13	62	0.16	−109
		2000	0.52	118	2	46	0.18	59	0.18	−109
	50	100	0.51	−118	31.6	126	0.02	63	0.58	−52
		200	0.57	−150	17.9	106	0.03	50	0.36	−66
		500	0.59	178	7.6	85	0.05	61	0.19	−76
		1000	0.58	153	3.7	68	0.09	67	0.15	−82
		1500	0.57	135	2.5	55	0.13	67	0.16	−100
		2000	0.55	116	1.9	44	0.17	63	0.19	−103
10	5	100	0.87	−39	14	155	0.03	70	0.89	−22
		200	0.75	−74	10.8	133	0.05	55	0.78	−32
		500	0.64	−134	6.1	100	0.08	37	0.53	−47
		1000	0.57	179	3.2	73	0.09	40	0.42	−57
		1500	0.56	153	2.1	56	0.11	47	0.41	−73
		2000	0.54	130	1.6	44	0.13	54	0.44	−83
	10	100	0.76	−57	21.9	145	0.02	70	0.83	−28
		200	0.64	−95	15.1	124	0.04	52	0.64	−43
		500	0.57	−151	7.5	94	0.06	43	0.40	−55
		1000	0.54	169	3.8	72	0.08	52	0.30	−61
		1500	0.53	146	2.5	57	0.11	57	0.30	−76
		2000	0.51	125	1.9	45	0.15	59	0.33	−84
	25	100	0.60	−82	30.4	133	0.02	60	0.73	−40
		200	0.56	−123	19.1	114	0.03	49	0.48	−53
		500	0.54	−168	8.5	89	0.05	54	0.28	−60
		1000	0.52	159	4.3	70	0.08	63	0.21	−64
		1500	0.52	139	2.8	57	0.12	64	0.22	−79
		2000	0.50	120	2.1	46	0.16	63	0.25	−84
	50	100	0.54	−104	33.5	127	0.01	60	0.63	−44
		200	0.55	−141	19.4	107	0.02	51	0.40	−51
		500	0.55	−177	8.3	85	0.04	61	0.26	−52
		1000	0.54	155	4.1	68	0.08	68	0.22	−56
		1500	0.54	137	2.7	55	0.11	69	0.23	−73
		2000	0.52	118	2	45	0.16	66	0.27	−81



NOTE: The Printed Circuit Board shown is 75% of the original.

Photomaster of MRF2369 Circuit Layout



MRF2369 Test Circuit

MRF2628

The RF Line

15 W 136–220 MHz

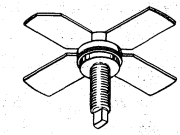
RF POWER TRANSISTOR

NPN SILICON

NPN SILICON POWER TRANSISTOR

Designed for 12.5 volt VHF large-signal power amplifiers in commercial and industrial FM equipment.

- Compact .280 Stud Package
- Specified 12.5 V, 175 MHz Performance
  Output Power = 15 Watts
  Power Gain = 12 dB Min
  Efficiency = 60% Min
- Characterized to 220 MHz
- Load Mismatch Capability at High Line and Overdrive

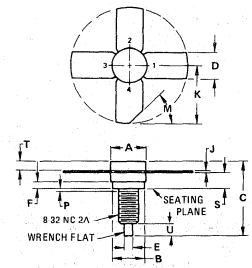


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	18	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector-Current — Continuous	I_C	2.5	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	40 0.23	Watts W/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.0	°C/W



STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.06	7.26	0.278	0.286
B	6.20	6.50	0.244	0.256
C	14.99	16.51	0.590	0.650
D	5.46	5.97	0.215	0.235
E	1.40	1.65	0.055	0.065
F	1.52	–	0.060	–
J	0.08	0.18	0.003	0.007
K	11.05	–	0.435	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
S	3.00	3.25	0.118	0.128
T	1.40	1.78	0.055	0.070
U	2.92	3.68	0.115	0.145

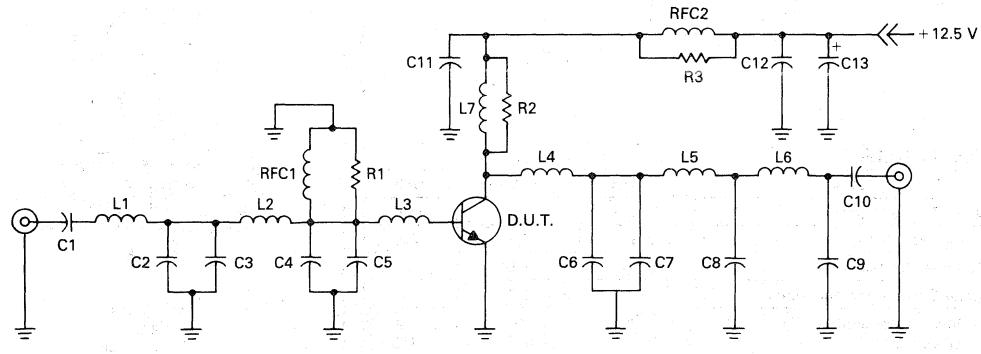
CASE 244-04

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 25 mAdc, I_B = 0)	$V_{(BR)CEO}$	18	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 25 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	—	—	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	70	150	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	33	60	pF
FUNCTIONAL TESTS (Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 15 W, f = 175 MHz)	G_{pe}	12	13	—	dB
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 15 W, f = 175 MHz)	η	60	68	—	%
Load Mismatch (V_{CC} = 15.5 V, P_{in} = 2.0 dB Overdrive, Load VSWR = 30:1)	ψ	No Degradation in Output Power			

3

FIGURE 1 — BROADBAND CIRCUIT



C1, C10, C11 = 1000 pF Ceramic Chip Capacitor
C2 = 27 pF Mini Unelco Capacitor
C3 = 33 pF Mini Unelco Capacitor
C4, C5 = 270 pF Unelco J101 Capacitor
C6, C9 = 18 pF Mini Unelco Capacitor
C7 = 91 pF Mini Unelco Capacitor
C8 = 68 pF Mini Unelco Capacitor
C12 = 0.1 μF Monolythic Capacitor
C13 = 100 μF, 15 V Electrolytic
L1 = 3 Turns #18 AWG, 3/16" ID
L2 = 1 1/8" #18 AWG into 1/2" High Loop
L3 = Copper Pad, 0.200 x 0.400 x 0.060
L4 = 1/4" #18 AWG into 1/8" High Loop
L5 = 3 Turns #24 AWG Enameled, 3/32" ID
L6 = 6 Turns #24 AWG Enameled, 3/32" ID
L7 = 1 3/4" #16 AWG into 3/4" High Loop
R1 = 12 Ω, 1/2 W Carbon
R2 = 100 Ω, 1.0 W Carbon
R3 = 10 Ω, 1.0 W Carbon
RFC1 = 0.15 μH Molded Choke
RFC2 = Ferrocube Choke, VK200-4B

FIGURE 2 — OUTPUT POWER versus FREQUENCY

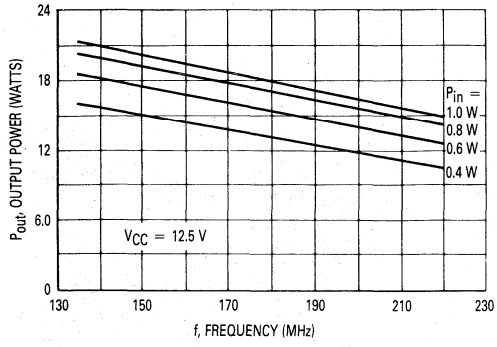


FIGURE 3 — OUTPUT POWER versus INPUT POWER

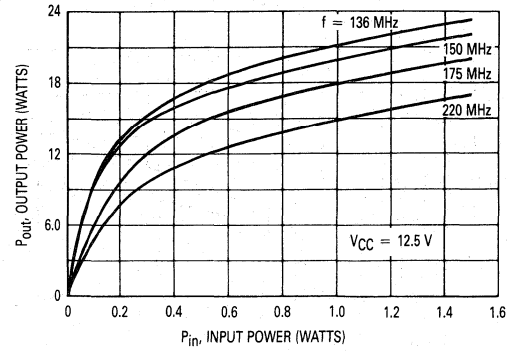


FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 220 MHz

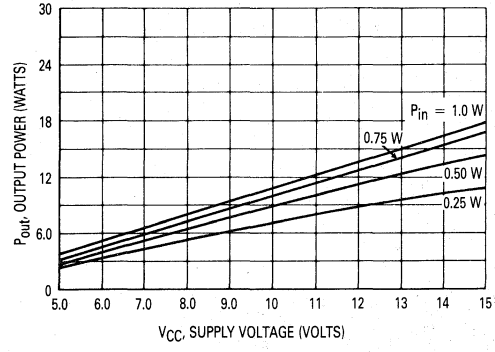


FIGURE 5 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 175 MHz

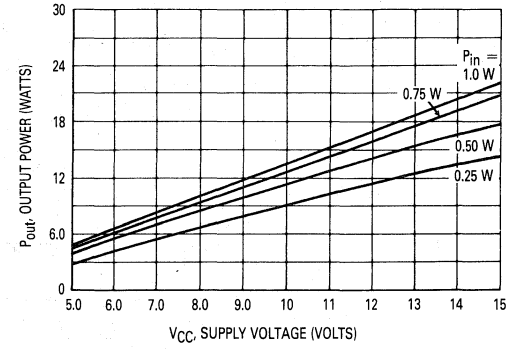


FIGURE 6 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 150 MHz

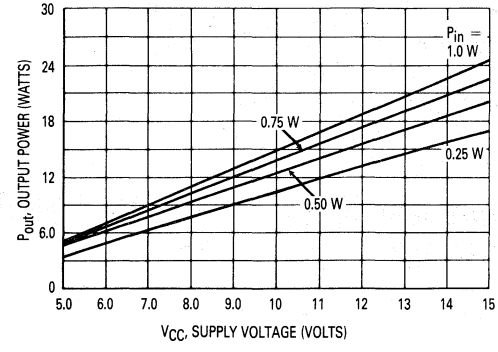
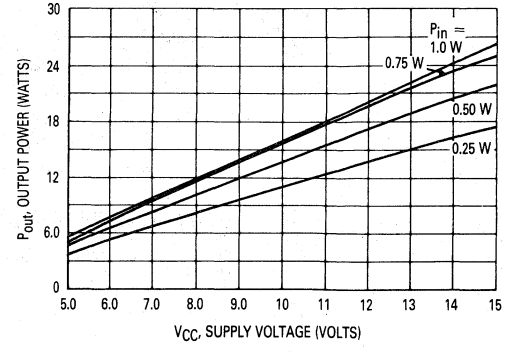


FIGURE 7 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 136 MHz



3

FIGURE 8 — TYPICAL PERFORMANCE IN A BROADBAND CIRCUIT

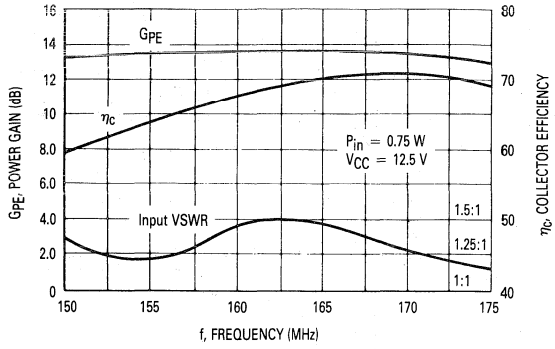
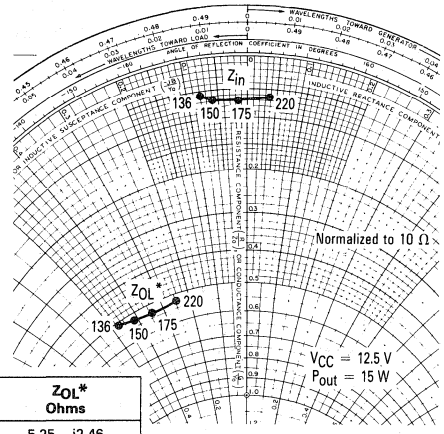


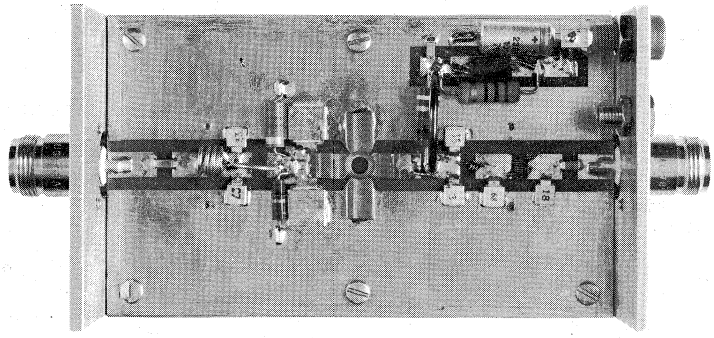
FIGURE 9 — SERIES EQUIVALENT IMPEDANCE



f MHz	Z_{in} Ohms	Z_{OL}* Ohms
220	0.62 + j0.39	5.25 – j2.46
175	0.69 – j0.17	5.26 – j3.46
150	0.68 – j0.61	5.23 – j4.14
136	0.59 – j0.80	5.07 – j4.76

*Z_{OL} = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage, and frequency.

FIGURE 10 — BROADBAND TEST CIRCUIT



MRF4070

The RF Line

70 W 175 MHz

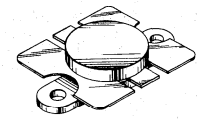
CONTROLLED Q
RF POWER
TRANSISTOR

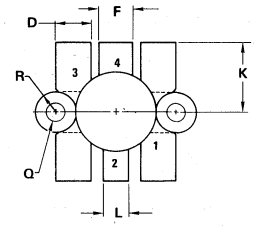
NPN SILICON

NPN SILICON RF POWER TRANSISTORS

. . . designed for 12.5 Volt VHF large-signal amplifier applications in industrial and commercial FM equipment operating to 175 MHz.

- Specified 12.5 Volt, 175 MHz Characteristics —
  Output Power = 70 Watts
  Minimum Gain = 5.0 dB
  Efficiency = 55%
- Characterized With Series Equivalent Large-Signal Impedance Parameters
- Built-In Matching Network for Broadband Operation
- Capable of Withstanding VSWR of 20:1 at Rated P_{out} and 15.5 V





STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. EMITTER
4. BASE
FLANGE-ISOLATED

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	12.45	12.95	0.490	0.510
C	5.97	7.62	0.235	0.300
D	5.33	5.59	0.210	0.220
F	5.08	5.33	0.200	0.210
H	18.29	18.54	0.720	0.730
J	0.10	0.15	0.004	0.006
K	10.29	11.18	0.405	0.440
L	3.81	4.06	0.150	0.160
N	3.81	4.32	0.150	0.170
Q	2.92	3.30	0.115	0.130
R	3.05	3.30	0.120	0.130

CASE 316-01

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Peak	I_C	20	Adc
Total Device Dissipation @ T_C = 25°C Derate Above 25°C	P_D	250 1.43	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R\theta_{JC}$	0.7	°C/W

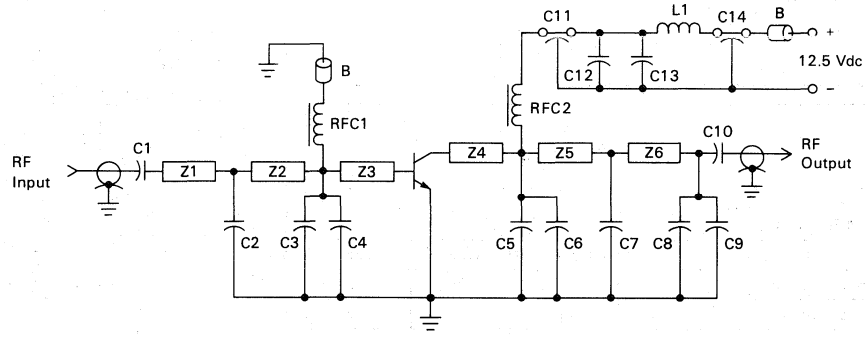
3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CBO}$	36	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 12.5 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0	—	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	—	275	pF
FUNCTIONAL TESTS (Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 70 Watts, F = 175 MHz)	G_{PE}	5.0	—	—	dB
Input Power (V_{CC} = 12.5 Vdc, P_{out} = 70 Watts, f = 175 MHz)	P_{in}	—	—	20	Watts
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 70 Watts, f = 175 MHz)	η	55	—	—	%

3

FIGURE 1 — 175 MHz TEST CIRCUIT SCHEMATIC



C1, C10 — 470 pF Unelco
C2 — 40 pF Unelco
C3, C4, C5, C6 — 150 pF Unelco
C7 — 80 pF Unelco
C8 — 25 pF Unelco
C9 — 15 pF Unelco
C11, C14 — 1000 pF Unelco
C12 — 0.05 μF Erie Disc Ceramic
C13 — 10 μF Electrolytic

Z1 = Microstrip 0.5 cm W × 3.5 cm L
Z2 = Microstrip 0.5 cm W × 9.0 cm L
Z3 = Microstrip 0.5 cm W × 1.0 cm L
Z4 = Microstrip 0.5 cm W × 1.0 cm L
Z5 = Microstrip 0.5 cm W × 1.0 cm L
Z6 = Microstrip 0.5 cm W × 9.0 cm L

RFC1 = 0.15 μH Molded Choke
RFC2 = 10 Turns #18 AWG Enameled Wire on 470 Ω, 2.0 W Resistor
L1 = 2.0 cm AWG #16 Wire
B = Fairite #2643021801, Ferrite Bead
Board Material = G10
$\epsilon_r \approx 5$
t = 62 mils

FIGURE 2 — OUTPUT POWER versus INPUT POWER

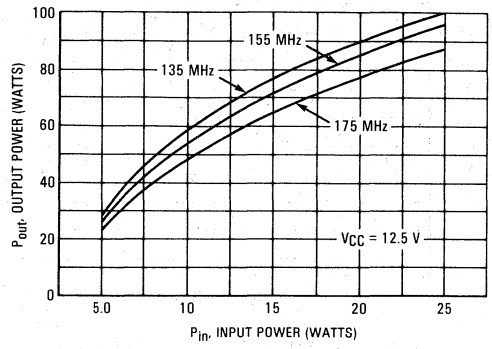


FIGURE 3 — OUTPUT POWER versus INPUT POWER

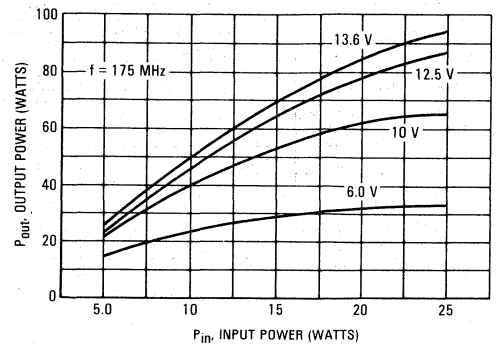


FIGURE 4 — OUTPUT POWER versus FREQUENCY

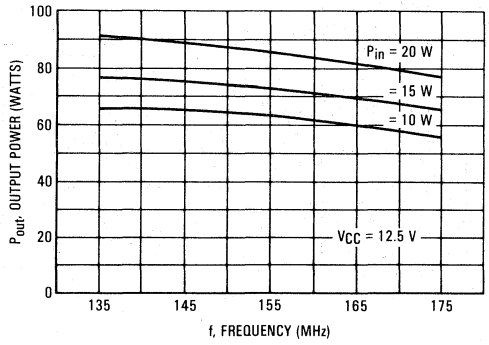
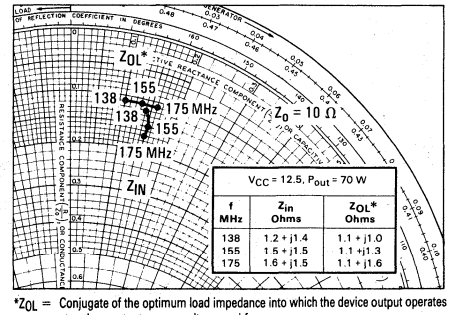


FIGURE 5 – SERIES EQUIVALENT IMPEDANCE



*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

3

FIGURE 6 — OUTPUT POWER versus SUPPLY VOLTAGE

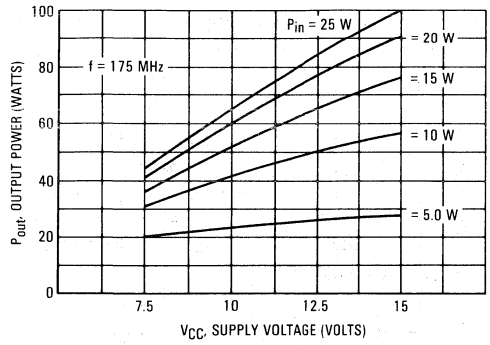


FIGURE 7 — OUTPUT POWER versus VOLTAGE

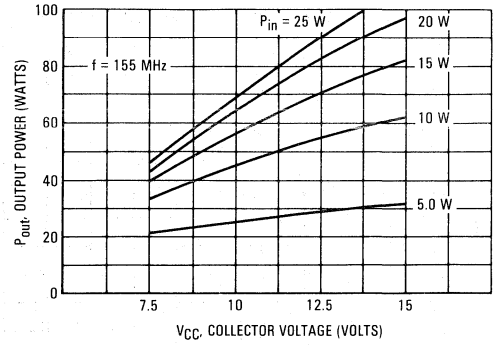


FIGURE 8 — OUTPUT POWER versus VOLTAGE

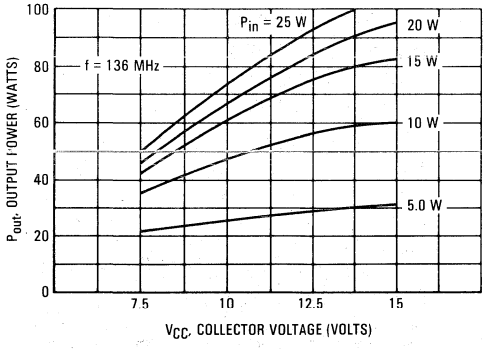
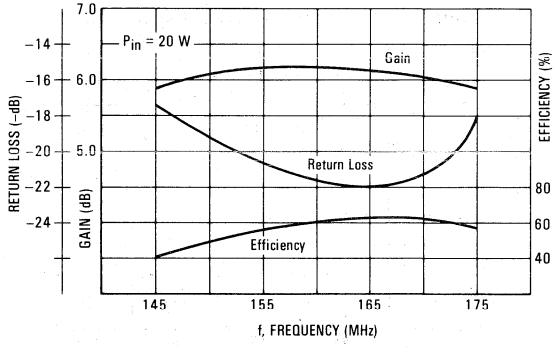


FIGURE 9 BROADBAND PERFORMANCE GAIN, RETURN LOSS, EFFICIENCY versus FREQUENCY



MRF5174

The RF Line

2 W – 400 MHz

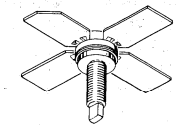
RF POWER TRANSISTOR

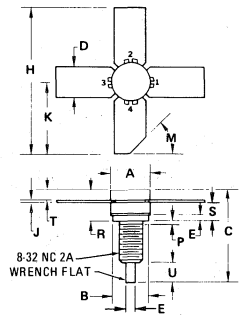
NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed primarily for wideband large-signal driver and pre-driver amplifier stages in the 260-600 MHz frequency range.

- Specified 28-Volt, 400-MHz Characteristics –
  Output Power = 2.0 Watts
  Minimum Gain = 12 dB
  Efficiency = 50%
- Characterized from 200 to 600 MHz
- Includes Series Equivalent Impedances





STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.06	7.26	0.278	0.286
B	6.25	6.45	0.246	0.254
C	15.49	16.51	0.610	0.650
D	5.59	5.84	0.220	0.230
E	1.52 NOM		0.060 NOM	
H	26.80	27.05	1.055	1.065
J	0.127 NOM		0.005 NOM	
K	13.41	13.51	0.528	0.532
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
R	4.52	5.03	0.178	0.198
S	3.00	3.25	0.118	0.128
T	1.40	1.65	0.055	0.065
U	2.92	3.68	0.115	0.145

CASE 244

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	33	Vdc
Collector-Base Voltage	V_{CBO}	60	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current – Continuous	I_C	0.5	Adc
Total Device Dissipation @ $T_A = 25^oC$ (1) Derate above 25^oC	P_D	5.0 28	Watts $mW/^oC$
Storage Temperature Range	T_{stg}	–65 to+150	^oC

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

THERMAL CHARACTERISTICS

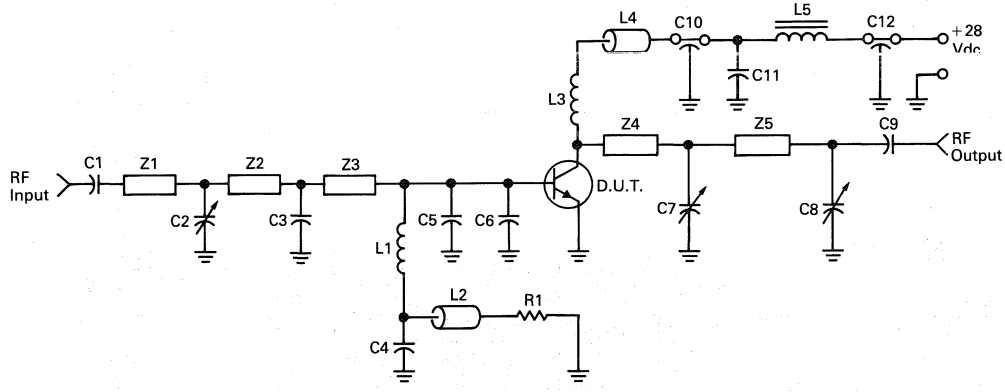
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	25	$^oC/W$

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	$V_{(BR)CEO}$	33	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 20 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	–	0.1	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	–	100	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 30 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	–	8.0	pF
FUNCTIONAL TESTS (Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 2.0 W, f = 400 MHz)	G_{PE}	12	–	–	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 2.0 W, f = 400 MHz)	η	50	–	–	%

3

FIGURE 1 – 400 MHz TEST CIRCUIT SCHEMATIC



C1, 9 — 0.02 μF Chip
C2 — 0.0–10 pF Johanson 2951
C3 — 15 pF Unelco
C4 — 100 pF Unelco
C5, 6 — 5.1 pF ATC 100 mil Chip
C7, 8 — 0.8–20 pF Johanson 3906
C10, 12 — 680 pF Feedthru
C11 — 1.0 μF Tantalum 35 V

R1 — 2.7 Ohm 1/2 Watt

L1 — 3.9 μH Molded Choke
L2, 4 — Ferrite Bead Ferroxcube 56-590-65-38
L3 — 0.15 μH Molded Choke
L5 — Ferrite Choke VK200-20-4B

Z1–Z5 — Microstrip, See Photomaster

Board Material — 0.062" Glass Teflon

FIGURE 2 – OUTPUT POWER versus FREQUENCY

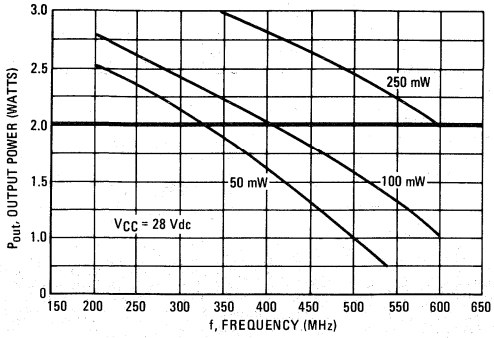


FIGURE 3 – OUTPUT POWER versus INPUT POWER

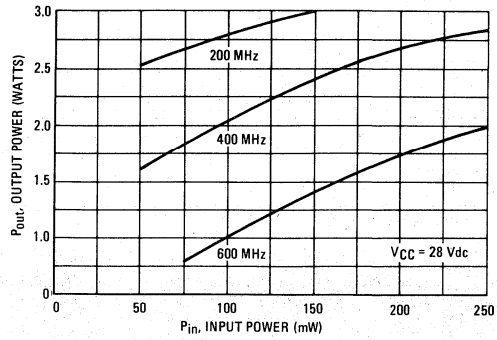


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

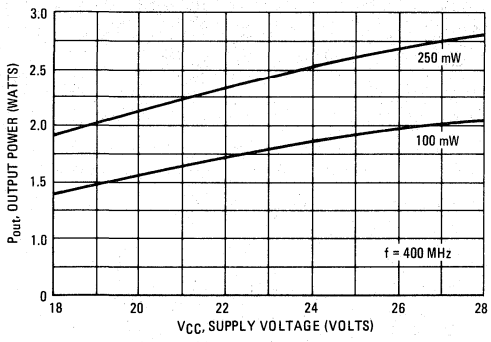
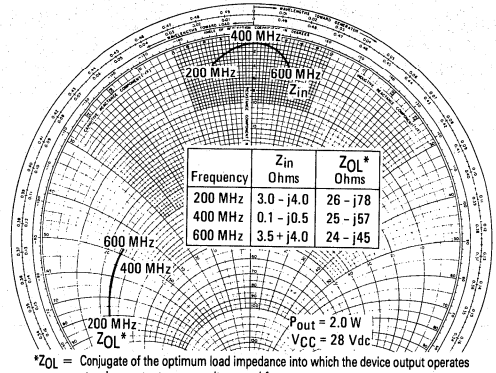


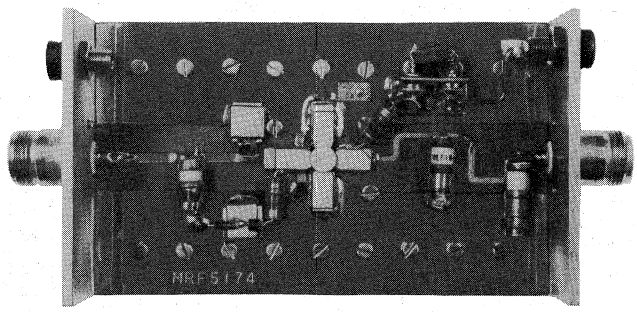
FIGURE 5 – SERIES EQUIVALENT IMPEDANCE



Frequency	Z_{in} Ohms	Z_{OL}^* Ohms
200 MHz	3.0 - j4.0	26 - j78
400 MHz	0.1 - j0.5	25 - j57
600 MHz	3.5 + j4.0	24 - j45

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

FIGURE 6 – 400 MHz TEST CIRCUIT



3

MRF5175

The RF Line

5 W – 400 MHz

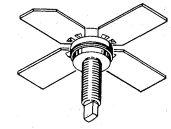
RF POWER TRANSISTOR

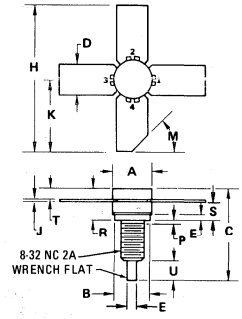
NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed primarily for wideband large-signal driver and predriver amplifier stages in the 200-600 MHz frequency range.

- Specified 28-Volt, 400-MHz Characteristics –
  Output Power = 5.0 Watts
  Minimum Gain = 11 dB
  Efficiency = 50%
- Characterized from 200 to 600 MHz
- Includes Series Equivalent Impedances





STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.06	7.26	0.278	0.286
B	6.25	6.45	0.246	0.254
C	15.49	16.51	0.610	0.650
D	5.59	5.84	0.220	0.230
E	1.52 NOM		0.060 NOM	
H	26.80	27.05	1.055	1.065
J	0.127 NOM		0.005 NOM	
K	13.41	13.51	0.528	0.532
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
R	4.52	5.03	0.178	0.198
S	3.00	3.25	0.118	0.128
T	1.40	1.65	0.055	0.065
U	2.92	3.68	0.115	0.145

CASE 244

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	33	Vdc
Collector-Base Voltage	V_{CBO}	60	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current – Continuous	I_C	1.0	Adc
Total Device Dissipation @ $T_A = 25^oC$ (1). Derate above 25^oC	P_D	12 69	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

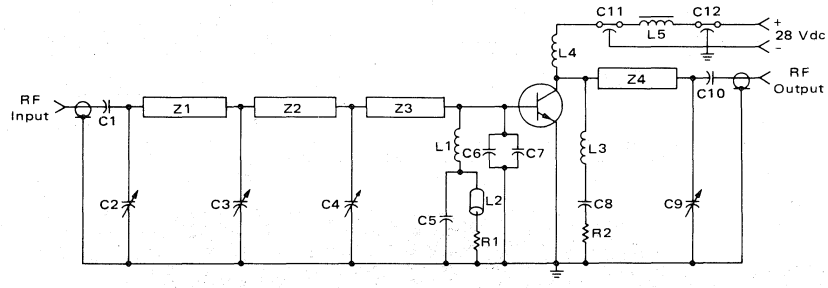
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 30 mAdc, I_B = 0)	$V_{(BR)CEO}$	33	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 30 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	–	0.5	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	–	100	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 30 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	–	15	pF
FUNCTIONAL TESTS (Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 5.0 W, f = 400 MHz)	G_{PE}	11	–	–	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 5.0 W, f = 400 MHz)	η	50	–	–	%

FIGURE 1 – 400 MHz TEST CIRCUIT SCHEMATIC



C1,C10 0.018 μF VITRAMON Chip
C2,C3,C9 1.0-10 pF JOHANSON Type 2951
C4 1.0-20 pF JOHANSON Type 3906
C5 100 pF UNDERWOOD (UNELCO)
C6,C7 5.0 pF ATC Chip
C8 0.1 μF ERIE Disc Ceramic
C11,C12 680 pF ALLEN BRADLEY Feedthru

L1 3.9 μH Molded Choke
L2 Ferrite Bead, FERROXCUBE 56-590-65-3B
L3 4 Turns, #22 AWG, 0.1" ID
L4 6 Turns, #20 AWG, 1/8" ID
L5 Ferrite Choke, FERROXCUBE VK200-20-4B

R1 2.7 Ohm, 1/8 Watt, 10%
R2 5.1 Ohm, 1/8 Watt, 10%

Z1,Z3 Microstrip Line, 0.1" W x 0.5" L
Z2 Microstrip Line, 0.1" W x 0.4" L
Z4 Microstrip Line, 0.075" W x 2.5" L

Board – Glass Teflon, ϵ_R = 2.56, t = 0.062"
Input/Output Connectors – Type N

FIGURE 2 – OUTPUT POWER versus FREQUENCY

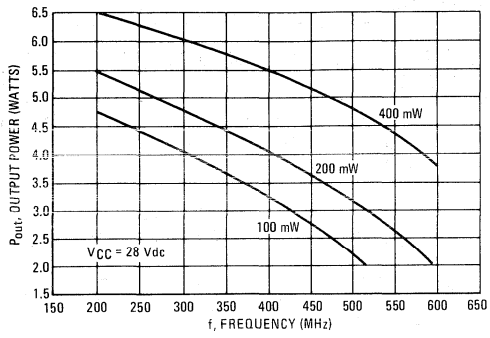


FIGURE 3 – OUTPUT POWER versus INPUT POWER

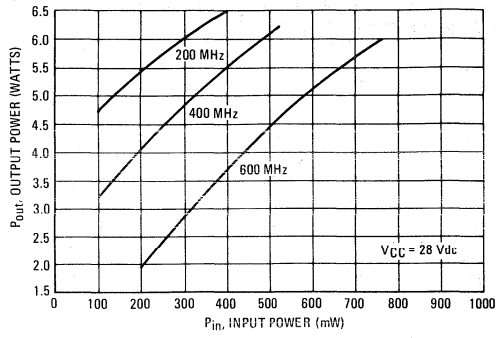


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

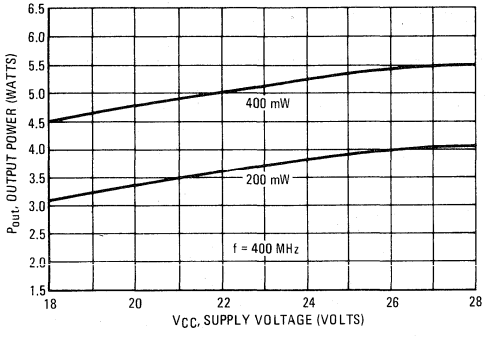
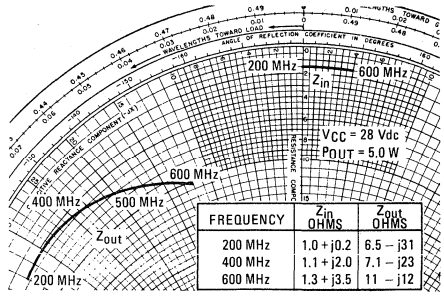
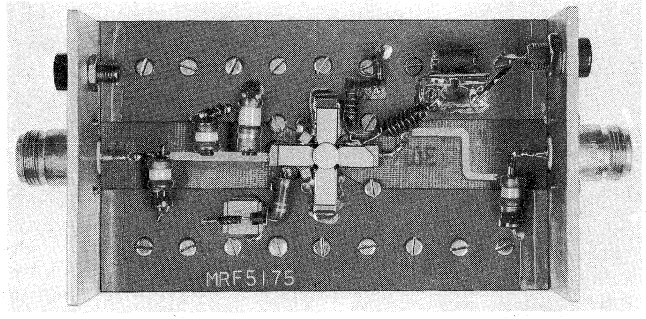


FIGURE 5 – SERIES EQUIVALENT IMPEDANCE



FREQUENCY	Z_{in} OHMS	Z_{out} OHMS
200 MHz	1.0 + j0.2	6.5 – j31
400 MHz	1.1 + j2.0	7.1 – j23
600 MHz	1.3 + j3.5	11 – j12

FIGURE 6 – 400 MHz TEST CIRCUIT



MRF5176

The RF Line

15 W — 400 MHz

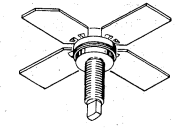
RF POWER TRANSISTOR

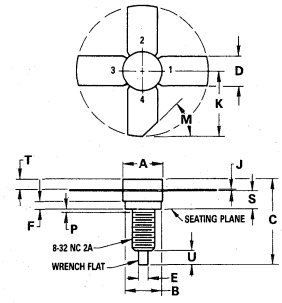
NPN SILICON

NPN SILICON RF POWER TRANSISTOR

. . . designed primarily for wideband large-signal driver and predriver amplifier stages in the 200-600 MHz frequency range.

- Specified 28 Volt, 400 MHz Characteristics —
  Output Power = 15 Watts
  Minimum Gain = 10 dB
  Efficiency = 50%
- Characterized from 200 to 600 MHz
- Includes Series Equivalent Impedances





STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.06	7.26	0.278	0.286
B	6.20	6.50	0.244	0.256
C	14.99	16.51	0.590	0.650
D	5.46	5.96	0.215	0.235
E	1.40	1.65	0.055	0.065
F	1.52	—	0.060	—
J	0.08	0.17	0.003	0.007
K	11.05	—	0.435	—
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
S	3.00	3.25	0.118	0.128
T	1.40	1.77	0.055	0.070
U	2.92	3.68	0.115	0.145

CASE 244-04

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	33	Vdc
Collector-Base Voltage	V_{CBO}	60	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	2.0	Adc
Total Device Dissipation @ $T_A = 25^oC$ (1) Derate above 25^oC	P_D	30 170	Watts $mW/^oC$
Storage Temperature Range	T_{stg}	-65 to +200	^oC

(1) These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as RF amplifiers.

THERMAL CHARACTERISTICS

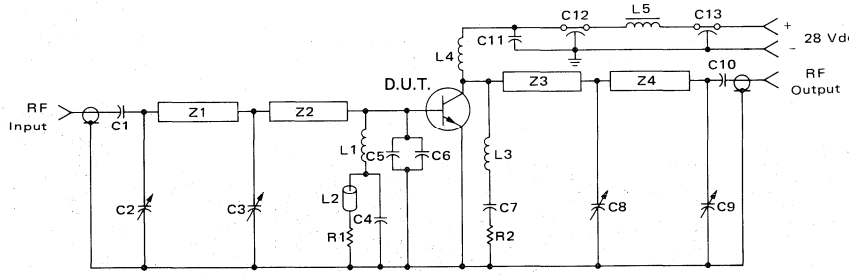
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.0	$^oC/W$

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	33	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 2.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0			Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	–	100	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 30 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	–	25	pF
FUNCTIONAL TESTS (Figure 1)					
Common-Emitter Amplifier Power Gain (V_{CC} = 28 Vdc, P_{out} = 15 W, f = 400 MHz)	G_{PE}	10	–	–	dB
Collector Efficiency (V_{CC} = 28 Vdc, P_{out} = 15 W, f = 400 MHz)	η	50	–	–	%

3

FIGURE 1 – 400 MHz TEST CIRCUIT SCHEMATIC



C1,C10 0.018 μF VITRAMON Chip
C2,C3,C8 1.0-20 pF JOHANSON Type 3906
C4 100 pF UNDERWOOD (UNELCO)
C5,C6 56 pF ATC Chip
C7 0.1 μF ERIE Disc Ceramic
C9 1.0-20 pF JOHANSON Type 3906
C11 1.0 μF, 35 V TANTALUM
C12,C13 680 pF ALLEN BRADLEY Feedthru

L1 3.9 μH Molded Choke
L2 Ferrite Bead, FERROXCUBE, 56-590-65-3B
L3 3 Turns, #20 AWG, 0.1" ID
L4 6 Turns, #20 AWG, 1/4" ID
L5 Ferrite Choke, FERROXCUBE, VK200-20-4B

R1 207 Ω, 1/8 W, 10%
R2 5.1 Ω, 1/8 W, 10%

Z1 Microstrip Line, 0.1" W x 1.2" L
Z2 Microstrip Line, 0.25" W x 0.7" L
Z3,Z4 Microstrip Line, 0.075" W x 1.25" L

Board – Glass Teflon, ϵ_R = 2.56, t = 0.062"
Input/Output Connectors – Type N

FIGURE 2 – OUTPUT POWER versus FREQUENCY

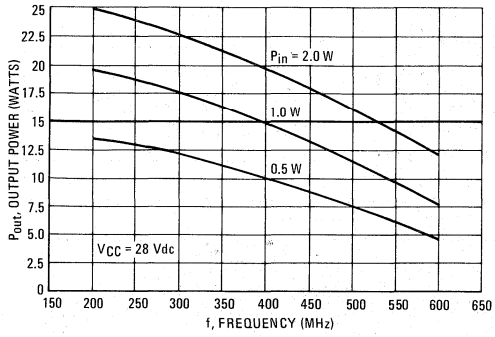


FIGURE 3 – OUTPUT POWER versus INPUT POWER

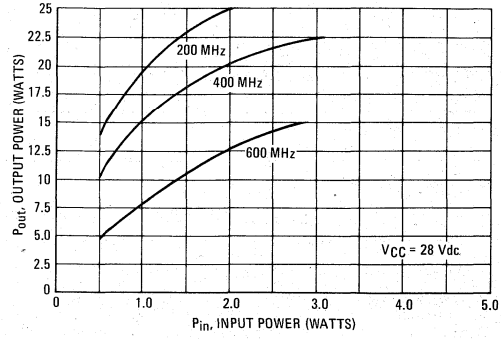


FIGURE 4 – OUTPUT POWER versus SUPPLY VOLTAGE

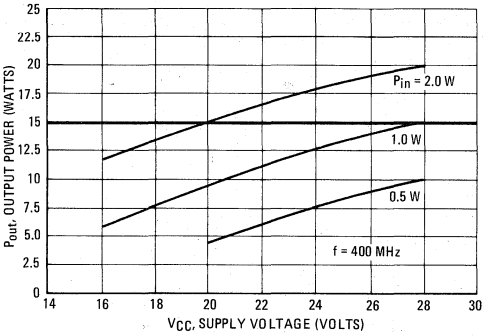
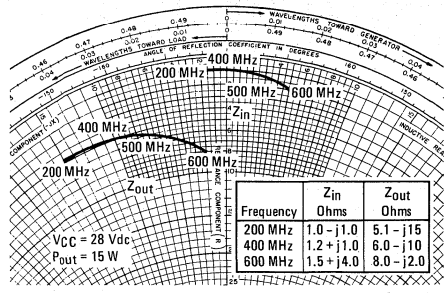
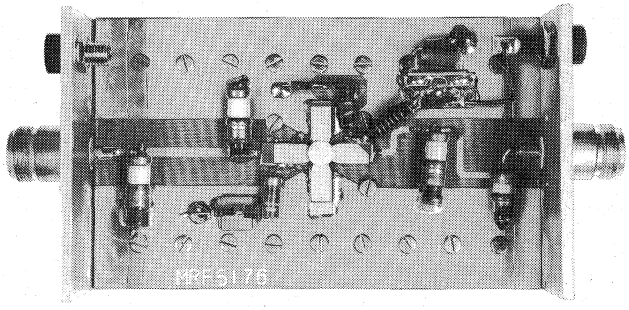


FIGURE 5 – SERIES EQUIVALENT IMPEDANCE



Frequency	Z_{in} Ohms	Z_{out} Ohms
200 MHz	1.0 - j1.0	5.1 - j15
400 MHz	1.2 + j1.0	6.0 - j10
600 MHz	1.5 + j4.0	8.0 - j2.0

FIGURE 6 – 400 MHz TEST CIRCUIT



MRF5177
MRF5177A

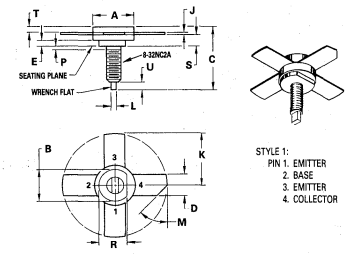
The RF Line

30 W, 400 MHz
RF POWER TRANSISTOR
NPN SILICON

NPN SILICON RF POWER TRANSISTOR

...designed for VHF/UHF power amplifier applications. This device is optimized for rugged performance in 225-400 MHz communications equipment.

- Performance @ 400 MHz, 28 Vdc —
  Power Output = 30 W (Min)
  Gain = 6.0 dB (Min)
- Isothermal Design for Rugged Performance —
  Tested at 30:1 VSWR through all phase angles



STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.78	0.370	0.385
B	8.13	8.38	0.320	0.330
C	17.02	20.07	0.670	0.790
D	5.46	5.97	0.215	0.235
E	1.78	—	0.070	—
J	0.08	0.18	0.003	0.007
K	12.45	—	0.490	—
L	1.40	1.78	0.055	0.070
M	45° NOM		45° NOM	
P	—	1.27	—	0.050
R	7.59	7.80	0.299	0.307
S	4.01	4.52	0.158	0.178
T	2.11	2.54	0.083	0.100
U	2.49	3.35	0.098	0.132

CASE 145A-09
MRF5177A

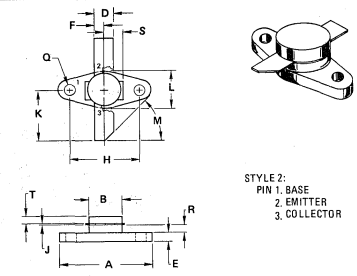
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	35	Vdc
Collector-Base Voltage	V_{CBO}	60	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	4.0	Adc
Base Current	I_B	1.0	Adc
Total Device Dissipation @ $T_C = 25^oC$) (1) Derate Above 25^oC	P_D —	58 0.33	Watts $W/^oC$
Storage Temperature Range	T_{stg}	-65 to +200	^oC

(1) This device is designed for RF Power operation. The total device dissipation rating applies only when the device is operated as a Class C RF Amplifier.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.0	$^oC/W$



STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

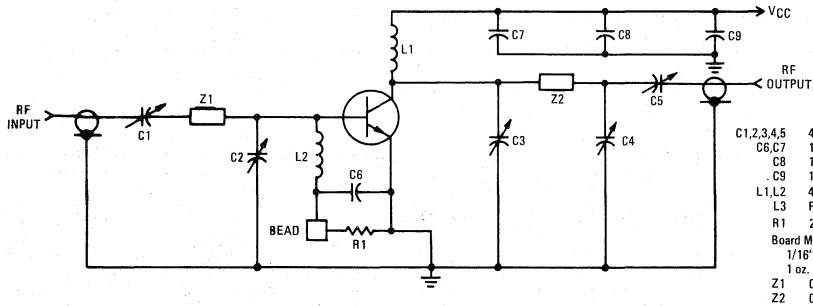
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.08	21.59	0.830	0.850
B	9.27	9.78	0.365	0.385
D	5.59	5.84	0.220	0.230
E	2.03	2.41	0.080	0.095
F	2.79	2.92	0.110	0.115
H	15.11	15.37	0.595	0.605
J	0.10	0.15	0.004	0.006
K	13.08	13.59	0.515	0.535
L	9.91	10.41	0.390	0.410
M	45°	NOM	45°	NOM
Q	2.92	3.18	0.115	0.125
R	1.52	2.03	0.060	0.080
S	—	5.38	—	0.212
T	2.03	2.54	0.080	0.100

CASE 215
MRF5177

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

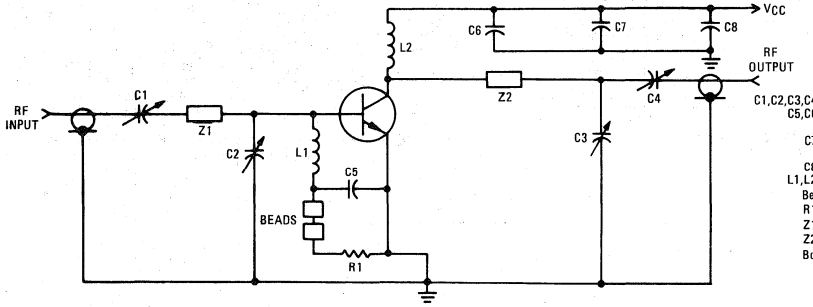
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, I_B = 0)	$V_{(BR)CEO}$	35	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 50 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	60	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 2.0 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	2.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5.0 Vdc) (I_C = 4.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10 10	100 –	–
DYNAMIC CHARACTERISTICS				
Output Capactiance (V_{CB} = 28 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	50	pF
FUNCTIONAL TESTS (Figures 1 and 9)				
Common-Emitter Amplifier Power Gain (P_{out} = 30 W, V_{CC} = 28 Vdc, f = 400 MHz)	G_{PE}	6.0	–	dB
Collector Efficiency (P_{out} = 30 W, V_{CC} = 28 Vdc, f = 400 MHz)	η	60	–	%
Saturated Power (P_{in} = 11 W, V_{CC} = 28 Vdc, f = 400 MHz)	P_{sat}	36	–	Watts
Electrical Ruggedness (P_{out} = 30 W, V_{CC} = 28 Vdc, f = 400 MHz, $T_C \leq 50°C$)	VSWR > 30:1 through all phase angles in a 3 second time interval, After which, devices will meet G_{PE} test limits.			

FIGURE 1 – 400 MHz TEST CIRCUIT
(Typical Performance Data for 300-500 MHz Operation)



C1,2,3,4,5 4.0-40 pF ARCO 422 or equivalent
C6,C7 100 pF ATC or equivalent
C8 10,000 pF ATC or equivalent
C9 1.0 μF, 35 V Tantalum
L1,L2 4 Turns, #20 AWG, 1/4" ID
L3 Ferrite Bead, Ferroxcube 56-590-65/3B
R1 2.7 ohms, 1/4 W, Carbon
Board Material:
1/16" Teflon Fiberglass
1 oz. copper, two-sided
Z1 0.3" Width, x 2.7" Length
Z2 0.3" Width, x 2.7" Length

FIGURE 2 – 200-300 MHz TEST CIRCUIT
(Typical Performance Data)



C1,C2,C3,C4 7.0-100 pF ARCO 423 or equivalent
C5,C6 100 pF Porcelain Chip Capacitor (ATC-100 or equivalent)
C7 10,000 pF Porcelain Chip Capacitor (ATC-100 or equivalent)
C8 1.0 μF, 35-V Tantalum
L1,L2 7 Turns #20 AWG, 1/4" ID
Beads, Ferroxcube 56-590 65/3B
R1 2.7 ohms, 1/2 W, Carbon
Z1 0.3" Width x 3.31" Length
Z2 0.3" Width x 4.53" Length
Board Material:
1/16" Glass-Teflon
1 oz. Copper, 2-sided

FIGURE 3 – OUTPUT POWER versus FREQUENCY

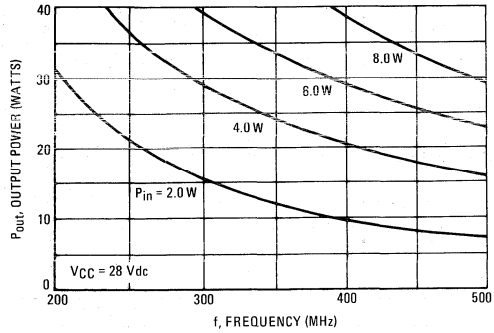


FIGURE 4 – OUTPUT POWER versus INPUT POWER

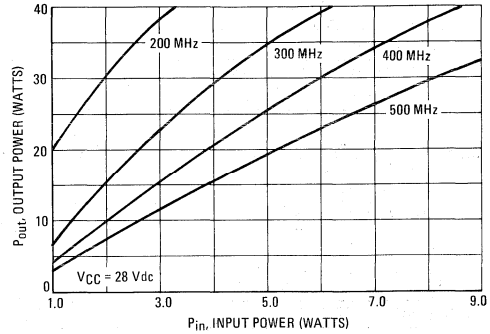


FIGURE 5 – OUTPUT POWER versus SUPPLY VOLTAGE

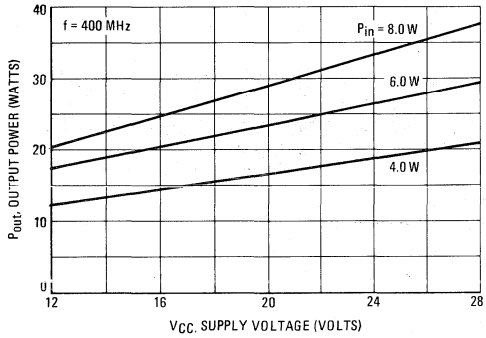


FIGURE 6 – OUTPUT POWER versus SUPPLY VOLTAGE

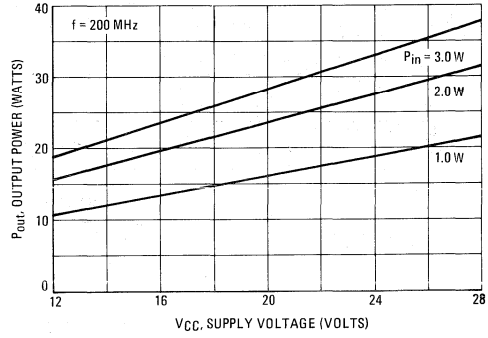


FIGURE 7 – RF POWER DERATING

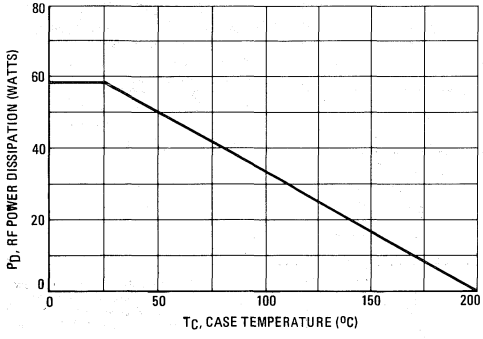
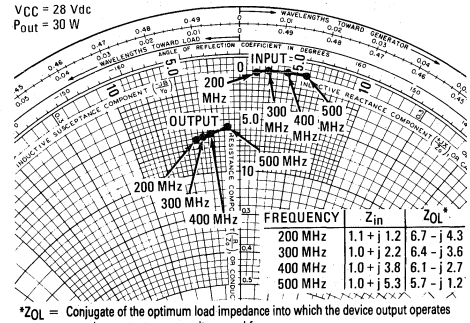


FIGURE 8 – SERIES EQUIVALENT IMPEDANCE



FREQUENCY	Z_{in}	Z_{OL}^*
200 MHz	1.1 + j 1.2	6.7 - j 4.3
300 MHz	1.0 + j 2.2	6.4 - j 3.6
400 MHz	1.0 + j 3.8	6.1 - j 2.7
500 MHz	1.0 + j 5.3	5.7 - j 1.2

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

MRF5711
BF430*
MRF5711L
BF430L*

*European Part Numbers

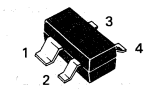
The RF Line

NPN Silicon High-Frequency Transistor

. . . designed primarily for use in the high-gain, low-noise small-signal amplifiers for operation up to 3.5 GHz. Also usable in applications requiring fast switching times.

- High Current-Gain-Bandwidth Product — f_T = 7.5 GHz (Typ) @ I_C = 50 mAdc
- Low Noise Figure @ f = 1 GHz — $NF_{(matched)}$ = 1.6 dB (Typ)
- High Power Gain — $G_{pe\ (matched)}$ = 13.5 dB (Typ)
- Guaranteed RF Parameters
- Surface Mounted SOT-143 Offers Improved RF Performance
  - Lower Package Parasitics
  - Higher Gain
- Available In Both Standard Profile (MRF5711) and Low Profile (MRF5711L)
- Tape and Reel Packaging Options

SURFACE MOUNTED HIGH FREQUENCY TRANSISTOR NPN SILICON



CASE 318B-01
SOT-143

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	10	Vdc
Collector-Base Voltage	V_{CBO}	20	Vdc
Emitter-Base Voltage	V_{EBO}	2.5	Vdc
Collector-Current — Continuous	I_C	70	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	0.58 4.64	Watts mW/°C
Total Device Dissipation(1) @ T_C = 75°C Derate above 75°C	P_D	0.58 7.73	Watts mW/°C
Maximum Junction Temperature	T_{Jmax}	150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	216	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	130	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1 mAdc, I_B = 0)	$V_{(BR)CEO}$	10	12	—	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	20	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 50 μAdc, I_C = 0)	$V_{(BR)EBO}$	2.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 8 Vdc, I_E = 0)	I_{CBO}	—	—	10	μAdc

Note 1. Case Temperature is measured on the collector lead where it first contacts the printed circuit board closest to the package.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS						
DC Current Gain (I_C = 30 mAdc, V_{CE} = 5 Vdc)		h_{FE}	50	—	300	—
DYNAMIC CHARACTERISTICS						
Collector-Base Capacitance (V_{CB} = 6 Vdc, I_E = 0, f = 1 MHz)	Figure 1	C_{cb}	—	0.75	1	pF
Current Gain — Bandwidth Product (V_{CE} = 8 Vdc, I_C = 50 mA, f = 1 GHz)	Figure 7	f_T	—	7.5	—	GHz
FUNCTIONAL TESTS						
Power Gain at Minimum Noise Figure (V_{CE} = 6 Vdc, I_C = 5 mA, f = 1 GHz)	Figure 5	G_{NFmin}	—	13.5	—	dB
Noise Figure (V_{CE} = 6 Vdc, I_C = 5 mA, f = 1 GHz)	Figure 5	NF_{min}	—	1.6	—	dB
Power Gain in 50 Ω System (V_{CE} = 6 Vdc, I_C = 5 mA, f = 1 GHz)	Figure 2	G_{NF}	9	10	—	dB
Noise Figure (V_{CE} = 6 Vdc, I_C = 5 mA, f = 1 GHz)	Figure 2	NF	—	2.2	3	dB

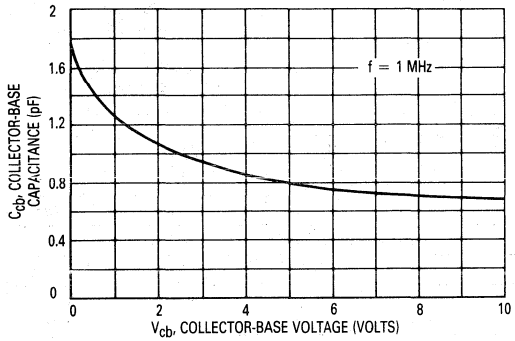


Figure 1. Collector-Base Capacitance versus Collector-Base Voltage

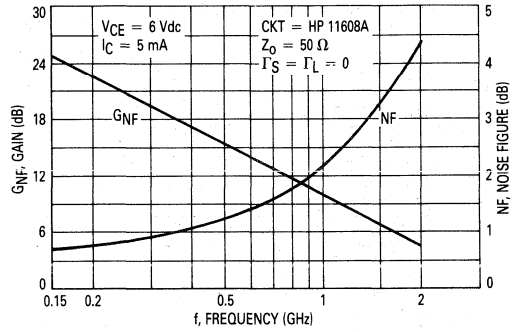


Figure 2. Gain and Noise Figure versus Frequency

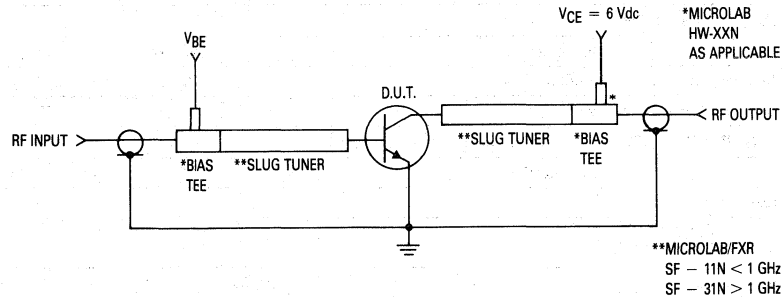


Figure 3. Functional Circuit Schematic

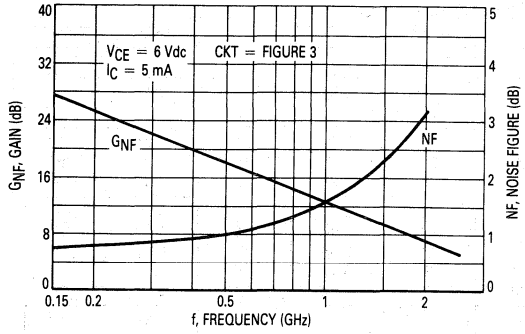


Figure 4. Gain and Noise Figure versus Frequency

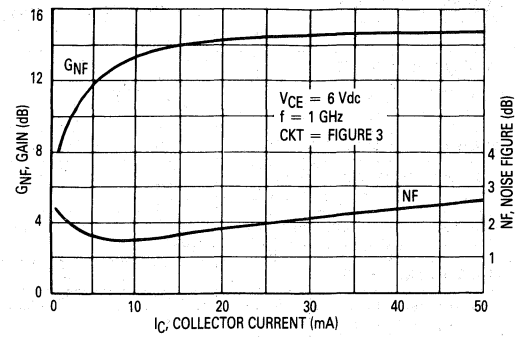


Figure 5. Gain and Noise Figure versus Collector Current

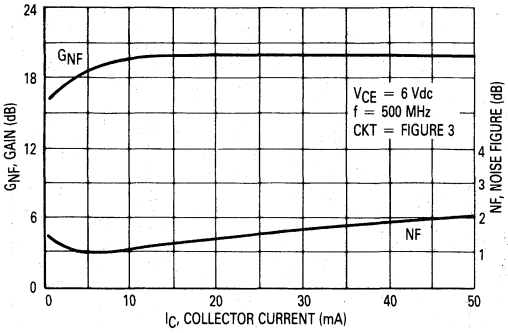


Figure 6. Gain and Noise Figure versus Collector Current

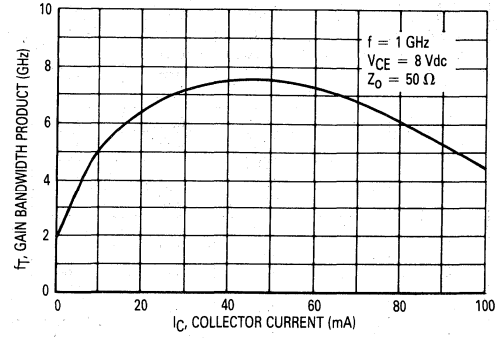


Figure 7. Gain Bandwidth Product versus Collector Current

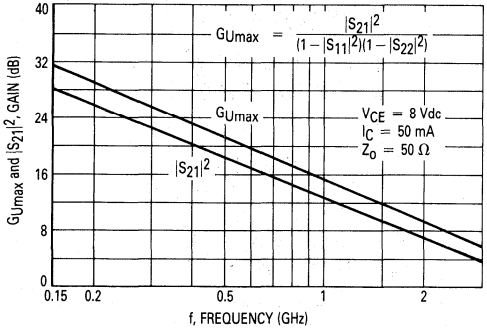


Figure 8. G_{Umax} and $|S_{21}|^2$ versus Frequency

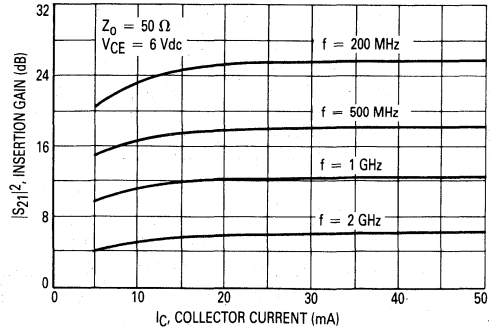
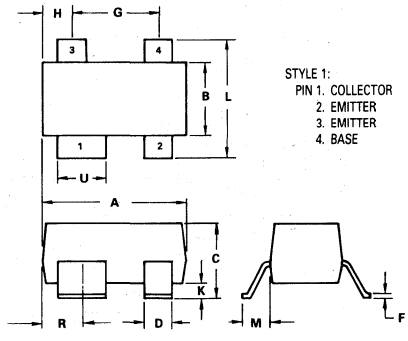


Figure 9. Insertion Gain versus Collector Current

COMMON EMITTER S-PARAMETERS

V_{CE} (Vdc)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
6	5	200	0.79	−90	10.9	128	0.06	46	0.70	−45
		500	0.72	−144	5.7	96	0.08	28	0.42	−66
		1000	0.69	−177	3	75	0.09	28	0.31	−77
		1500	0.66	164	2	59	0.10	32	0.34	−89
		2000	0.65	147	1.6	47	0.12	38	0.32	−94
	10	200	0.72	−115	15.2	118	0.05	41	0.55	−66
		500	0.69	−160	6.9	92	0.06	34	0.30	−92
		1000	0.67	174	3.6	74	0.08	42	0.21	−108
		1500	0.64	159	2.4	60	0.10	46	0.23	−114
		2000	0.64	143	1.8	49	0.12	50	0.20	−116
	50	200	0.67	−159	20	102	0.02	48	0.33	−111
		500	0.67	179	8.2	85	0.04	58	0.33	−142
		1000	0.66	174	3.8	72	0.07	65	0.21	−158
		1500	0.63	151	2.7	61	0.10	64	0.22	−158
		2000	0.58	138	2.1	51	0.14	62	0.17	−165
8	5	200	0.80	−87	11.1	130	0.06	47	0.71	−42
		500	0.72	−141	5.9	97	0.08	30	0.44	−60
		1000	0.70	−177	3.1	75	0.09	28	0.33	−68
		1500	0.66	166	2.1	60	0.10	32	0.35	−80
		2000	0.61	149	1.6	47	0.12	39	0.35	−85
	10	200	0.72	−113	15.6	119	0.05	42	0.56	−61
		500	0.68	−159	7.2	92	0.06	34	0.31	−82
		1000	0.66	175	3.7	74	0.08	41	0.21	−92
		1500	0.64	160	2.5	61	0.09	47	0.23	−101
		2000	0.60	144	2	49	0.13	50	0.21	−103
	50	200	0.66	−156	20.9	103	0.02	48	0.31	−101
		500	0.65	−179	8.6	85	0.04	58	0.19	−128
		1000	0.64	164	4.3	72	0.07	65	0.16	−144
		1500	0.61	153	2.9	61	0.10	65	0.17	−142
		2000	0.58	137	2.3	51	0.13	64	0.14	145

OUTLINE DIMENSIONS



STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. EMITTER
4. BASE

	DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
	A	2.80	3.04	0.110	0.120
	B	1.20	1.39	0.047	0.055
	C	0.85	1.14	0.033	0.045
	D	0.38	0.45	0.015	0.018
	F	0.85	0.15	0.003	0.006
	G	1.78	2.03	0.070	0.080
	H	0.51	0.60	0.020	0.024
	K	0.10	0.25	0.004	0.010
	L	2.11	2.48	0.083	0.098
	M	0.46	0.60	0.018	0.024
	R	0.71	0.83	0.028	0.033
	U	0.78	0.88	0.031	0.035
*	K	0.013	0.102	0.0005	0.0040

***Low Profile = Case 318A-02**

CASE 318B-01
SOT-143

MRF5812
BF433*

*European Part Number

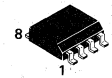
**SURFACE MOUNT
LOW POWER
TRANSISTOR
NPN SILICON**

The RF Line

NPN Silicon RF Low Power Transistor

. . . designed for high current, low power amplifiers up to 2 GHz.

- High Current Gain-Bandwidth Product — f_T = 5.5 GHz (Typ) @ I_C = 75 mA
- Low Noise — 2 dB (Typ) @ 500 MHz
- Low Intermodulation Distortion
- High Gain — 15.5 dB (Typ) @ 500 MHz
- Low Cost SORF Plastic Surface Mount Package
- State-of-the-Art Technology
  - Fine Line Geometry
  - Gold Top Metal and Wires
  - Silicon Nitride Passivated
  - Ion Implanted Arsenic Emitters
- Die Same as MRF581,A



**CASE 751-02
SORF
(SO-8)**

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CBO}	30	Vdc
Emitter-Base Voltage	V_{EBO}	2.5	Vdc
Collector-Current — Continuous	I_C	200	mAdc
Total Device Dissipation @ T_C = 80°C (1) Derate above 80°C	P_D	1.5 22.2	Watts mW/°C
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.5 11.8	Watts mW/°C
Operating Junction and Storage Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	45	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	85	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5 mAdc, I_B = 0)	$V_{(BR)CEO}$	15	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 5 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	30	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	2.5	—	—	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CBO}	—	—	0.1	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	90	200	—

(1) Case temperature is measured on the collector lead where the lead contacts the printed circuit board closest to the body of the package.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Collector Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)	C_{cb}	—	1.2	2	pF
Current-Gain Bandwidth Product (1) (I_C = 75 mAdc, V_{CE} = 10 Vdc, f = 1 GHz)	f_T	—	5.5	—	GHz
FUNCTIONAL TESTS					
Noise Figure (Optimum) (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz) Figure 4	NF	—	2	—	dB
Noise Figure (50 Ohm Insertion) (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz) Figure 5	NF	—	2.5	3	dB
Power Gain Associated with Noise Figure (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz) Figure 5	G_{NF}	13	15.5	—	dB
Maximum Unilateral Gain (1) (I_C = 75 mAdc, V_{CE} = 10 Vdc, f = 0.5 GHz)	G_{Umax}	—	17	—	dB
Intermodulation Distortion (2) Figure 1 (V_{CE} = 10 V, I_C = 75 mA, V_{out} = +50 dBmV)	IMD(d3)	—	−65	—	dB

Notes: (1) Characterized on HP8542 Automatic Network Analyzer. $G_{Umax} = \frac{|S_{21}|^2}{(1 - |S_{11}|^2)(1 - |S_{22}|^2)}$

(2) 2 Tones, f1 = 497 MHz, f2 = 503 MHz, 3rd Order Single Tone Reference.

3

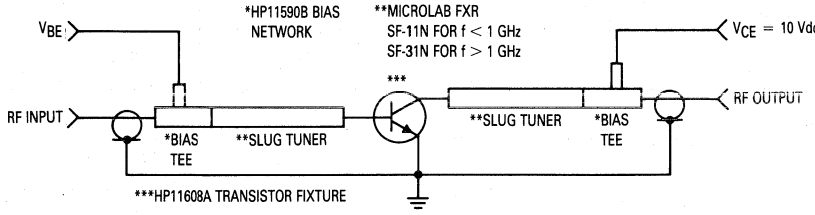


Figure 1. Functional Circuit Schematic

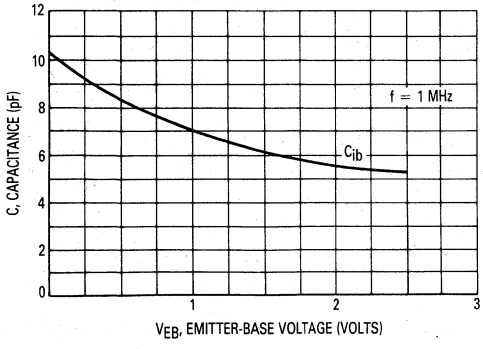


Figure 2. C_{ib} Input Capacitance versus Voltage

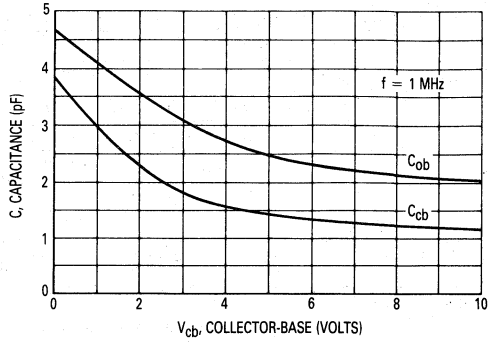


Figure 3. C_{cb}, C_{ob} Collector-Base Capacitance versus Voltage

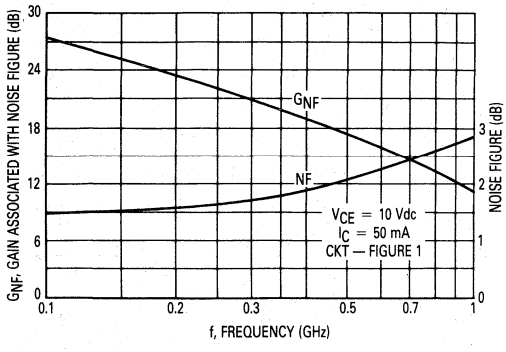


Figure 4. Noise Figure and Gain Associated with Noise Figure versus Frequency

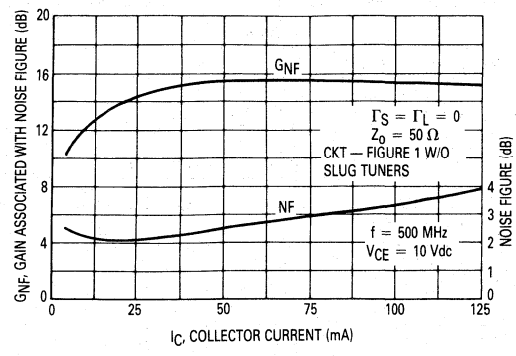


Figure 5. Noise Figure and Gain Associated with Noise Figure versus Collector Current

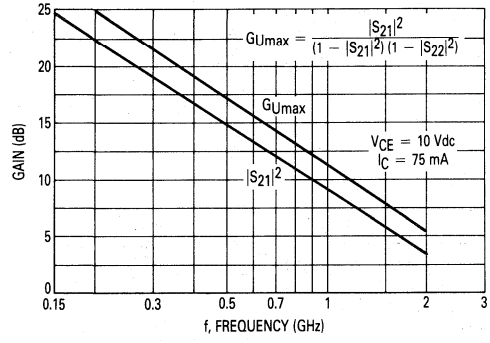


Figure 6. G_{Umax} — Maximum Unilateral Gain, $|S_{21}|^2$ versus Frequency

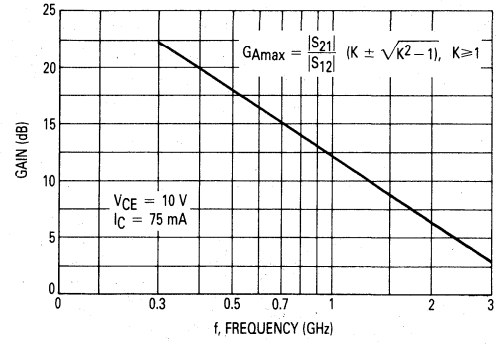


Figure 7. G_{Amax}, Maximum Available Gain versus Frequency

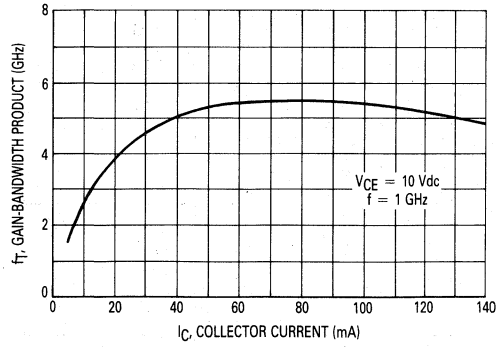


Figure 8. Gain-Bandwidth Product versus Collector Current

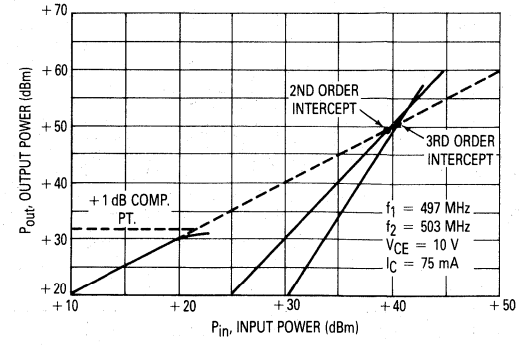
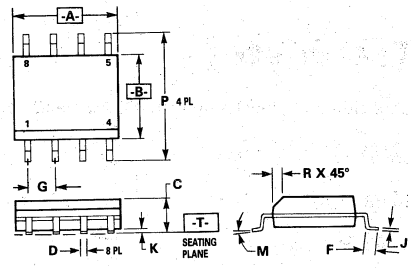


Figure 9. 2nd and 3rd Order Intercept Points and 1 dB Compression Point

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
5	25	100	0.66	−123	18.3	118	0.04	43	0.53	−79
		300	0.66	−167	7	92	0.06	44	0.31	−120
		500	0.65	178	4.3	81	0.08	52	0.28	−133
		1000	0.62	154	2.2	63	0.13	61	0.28	−141
		2000	0.57	109	1.3	39	0.28	57	0.31	−148
		3000	0.55	68	1	23	0.41	41	0.34	−164
	50	100	0.64	−133	20.2	114	0.04	44	0.51	−93
		300	0.65	−171	7.6	91	0.06	50	0.34	−137
		500	0.65	175	4.6	81	0.08	56	0.31	148
		1000	0.61	152	2.3	63	0.13	63	0.28	−149
		2000	0.56	109	1.3	39	0.28	57	0.3	−150
		3000	0.52	70	1	23	0.41	39	0.29	−169
	75	100	0.64	−137	20.8	113	0.04	44	0.5	−99
		300	0.66	−173	7.7	91	0.06	52	0.35	−142
		500	0.64	174	4.7	82	0.08	59	0.32	−154
		1000	0.61	151	2.4	65	0.14	64	0.3	−164
		2000	0.54	107	1.4	42	0.3	55	0.27	−167
		3000	0.52	69	1.1	24	0.42	37	0.25	−172
	100	100	0.64	−140	20.8	112	0.03	44	0.5	−103
		300	0.65	−174	7.6	90	0.06	53	0.36	−145
		500	0.64	173	4.7	81	0.08	60	0.33	−156
		1000	0.61	151	2.4	65	0.15	64	0.31	−166
		2000	0.54	107	1.4	42	0.3	54	0.27	−169
		3000	0.52	65	1.1	24	0.42	37	0.25	−174
10	25	100	0.65	−112	20.2	121	0.04	46	0.56	−62
		300	0.63	−162	8	93	0.05	46	0.29	−93
		500	0.62	−178	5	82	0.07	52	0.25	−102
		1000	0.6	157	2.5	63	0.11	63	0.26	−112
		2000	0.55	112	1.4	39	0.25	61	0.35	−125
		3000	0.55	69	1	23	0.39	47	0.4	−145
	50	100	0.63	−122	22.9	117	0.03	46	0.5	−74
		300	0.62	−167	8.8	92	0.05	51	0.28	−112
		500	0.6	178	5.3	82	0.07	58	0.24	−122
		1000	0.58	154	2.7	64	0.12	65	0.23	−129
		2000	0.51	111	1.5	40	0.26	59	0.28	−132
		3000	0.5	70	1.2	24	0.39	44	0.34	−144
	75	100	0.63	−126	23.8	116	0.03	45	0.49	−80
		300	0.63	−168	9	92	0.05	51	0.28	−120
		500	0.62	177	5.5	82	0.07	58	0.24	−130
		1000	0.58	154	2.8	65	0.12	65	0.23	−137
		2000	0.52	111	1.5	41	0.26	58	0.27	−135
		3000	0.5	70	1.2	24	0.39	42	0.32	−145
	100	100	0.62	−128	23.8	114	0.03	46	0.46	−82
		300	0.62	−169	8.9	91	0.05	54	0.26	−120
		500	0.6	176	5.4	81	0.07	61	0.23	−130
		1000	0.57	152	2.8	64	0.12	66	0.21	−136
		2000	0.51	109	1.5	40	0.27	59	0.26	−134
		3000	0.5	68	1.2	24	0.39	43	0.32	−145
15	25	100	0.66	−106	21	123	0.03	47	0.57	−54
		300	0.63	−159	8.5	94	0.05	46	0.3	−77
		500	0.61	−177	5.2	82	0.06	52	0.26	−84
		1000	0.58	156	2.6	62	0.11	64	0.28	−96
		2000	0.54	110	1.4	36	0.23	63	0.39	−115
		3000	0.56	68	1	22	0.37	49	0.46	−137
	50	100	0.62	−114	24	119	0.03	46	0.51	−64
		300	0.6	−163	9.2	93	0.05	51	0.26	−92
		500	0.58	−179	5.7	81	0.07	58	0.22	−100
		1000	0.56	154	2.9	63	0.12	66	0.23	−109
		2000	0.52	109	1.5	39	0.25	60	0.32	−118
		3000	0.52	67	1.1	22	0.37	46	0.39	−137
	75	100	0.62	−118	24.6	117	0.03	46	0.48	−67
		300	0.59	−165	9.4	92	0.05	53	0.24	−96
		500	0.58	179	5.7	81	0.07	60	0.21	−104
		1000	0.56	154	2.9	63	0.12	66	0.22	−111
		2000	0.5	109	1.5	38	0.25	60	0.31	−118
		3000	0.52	67	1.1	22	0.37	46	0.38	−136
	100	100	0.62	−121	24.8	116	0.03	46	0.46	−68
		300	0.6	−165	9.3	91	0.05	53	0.23	−96
		500	0.58	179	5.7	81	0.07	61	0.2	−102
		1000	0.56	155	2.9	63	0.12	65	0.22	−109
		2000	0.5	111	1.5	39	0.25	62	0.32	−117
		3000	0.5	68	1.1	23	0.37	47	0.39	−136

Figure 10. Common Emitter S-Parameters

OUTLINE DIMENSIONS



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. POSITIONAL TOLERANCE FOR D DIMENSION (8 PLACES):
   ⌖ | 0.25 (0.010) Ⓜ | T | B Ⓢ | A Ⓢ
3. POSITIONAL TOLERANCE FOR P DIMENSION (4 PLACES):
   ⌖ | 0.25 (0.010) Ⓜ | B Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: MILLIMETER.
6. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
7. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

CASE 751-02
SORF
(SO-8)

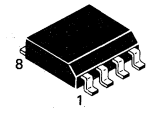
MRF8372

The RF Line
NPN Silicon
RF Low Power Transistor

**750 mW 870 MHz
RF LOW POWER
TRANSISTOR
NPN SILICON**

. . . designed primarily for wideband large signal predriver stages in 800 MHz and UHF frequency ranges.

- Specified @ 12.5 V, 870 MHz Characteristics
  - Output Power = 750 mW
  - Common Emitter Power Gain = 10 dB (Typ)
  - Efficiency 60% (Typ)
- Low Cost SORF Plastic Surface Mounted Package
- State-of-the-Art Technology
  - Fine Line Geometry
  - Gold Top Metal and Wires
  - Silicon Nitride Passivated
  - Ion Implanted Arsenic Emitters



**CASE 751-02
SORF
(SO-8)**

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	16	Vdc
Collector-Base Voltage	V_{CBO}	36	Vdc
Emitter-Base Voltage	V_{EBO}	4	Vdc
Collector-Current — Continuous	I_C	200	mAdc
Total Device Dissipation @ T_C = 80°C (1) Derate above 80°C	P_D	1.5 22.2	Watts mW/°C
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.5 11.8	Watts mW/°C
Operating Junction and Storage Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	45	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	85	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

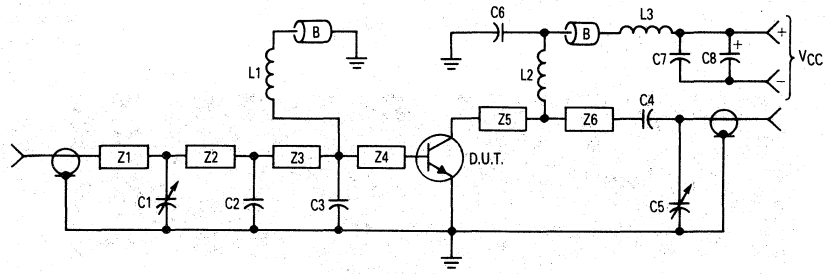
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 5 mAdc, I_B = 0)	$V_{(BR)CEO}$	16	—	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 5 mAdc, V_{BE} = 0)	$V_{(BR)CES}$	36	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	4	—	—	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	—	—	0.1	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	90	200	—

(1) Case temperature is measured on the collector lead where the lead contacts the printed circuit board closest to the body of the package.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f = 1 MHz)	C_{ob}	—	1.8	2.5	pF
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain Figures 1, 3 (V_{CC} = 12.5 Vdc, P_{out} = 0.75 W, f = 870 MHz)	G_{pe}	8	10	—	dB
Collector Efficiency Figures 1, 3 (V_{CC} = 12.5 Vdc, P_{out} = 0.75 W, f = 870 MHz)	η	55	60	—	%



C1,C5 — 0.8–8 pF Johanson Gigatrim
C2,C3 — 10 pF Ceramic Chip Capacitor
C6 — 91 pF Clamped Mica, Mini-Underwood
C4 — 47 pF Ceramic Chip Capacitor
C7 — 91 pF Clamped Mica, Mini-Underwood
C8 — 1 μF 25 V Tantalum
B — Bead, Ferroxcube 56-590-65/3B

L1,L2 — 4 Turns, #21 AWG, 5/32" ID
L3 — 7 Turns, #21 AWG, 5/32" ID
Z1,Z2 — 1" x 0.078" Microstrip, Z_O = 50 Ohms
Z3 — 0.25" x 0.078" Microstrip, Z_O = 50 Ohms
Z4 — 0.15" x 0.078" Microstrip, Z_O = 50 Ohms
Z5 — 0.30" x 0.078" Microstrip, Z_O = 50 Ohms
Z6 — 1.63" x 0.078" Microstrip, Z_O = 50 Ohms
PCB — 1/32" Glass Teflon, ϵ_r = 2.56

Figure 1. 800–900 MHz Broadband Circuit

800/900 MHz BAND DATA

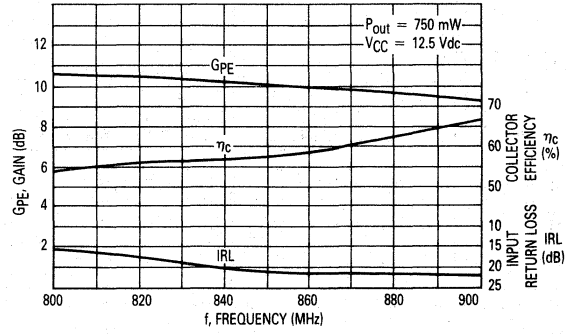


Figure 2. Typical Broadband Performance

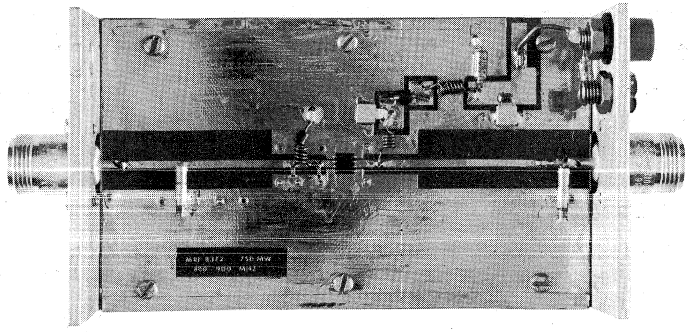
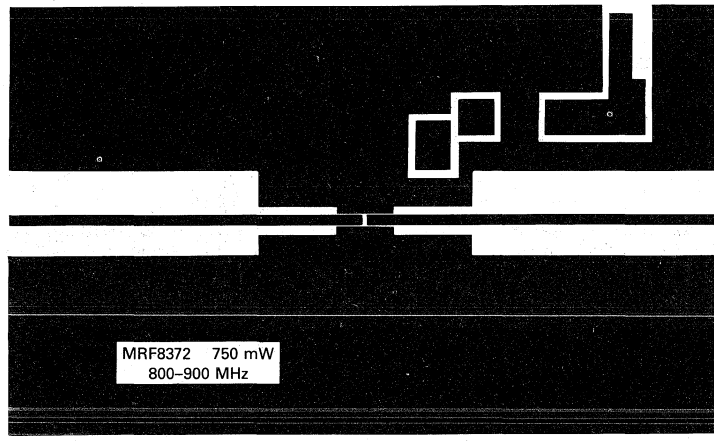


Figure 3. 800–900 Broadband Circuit



NOTE: The Printed Circuit Board shown is 75% of the original.

Figure 4. 800–900 MHz Broadband Circuit Photomaster

f Frequency MHz	Z_{in} Ohms		Z_{OL}* Ohms	
	V_{CC} = 7.5 V	V_{CC} = 12.5 V	V_{CC} = 7.5 V	V_{CC} = 12.5 V
	P_{in} = 150 mW	P_{in} = 100 mW	P_{out} 806 MHz = 820 mW P_{out} 870 MHz = 635 mW P_{out} 960 MHz = 530 mW	P_{out} 806 MHz = 1.05 mW P_{out} 870 MHz = 855 mW P_{out} 960 MHz = 580 mW
806	8.0 + j1.9	4.0 + j1.2	24.7 − j19.2	20.9 − j31.0
870	5.2 + j3.5	6.0 + j1.9	36.9 − j20.5	32.1 − j26.6
960	6.8 + j4.0	6.1 + j2.5	39.3 − j18.5	36.3 − j25.7

*Z_{OL} = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.

Figure 5. Z_{in} and Z_{OL} versus Collector Voltage, Input Power and Output Power

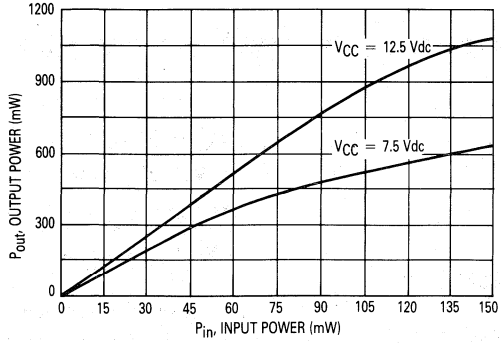


Figure 6. Output Power versus Input Power
f = 870 MHz

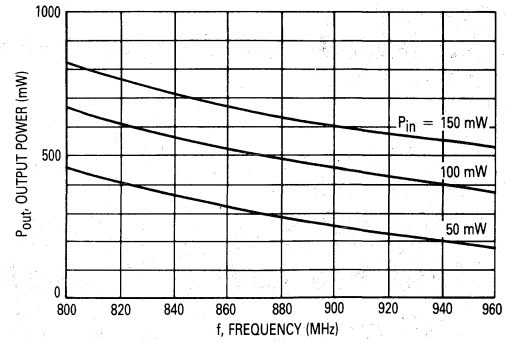


Figure 7. Output Power versus Frequency
V_{CC} = 7.5 Vdc

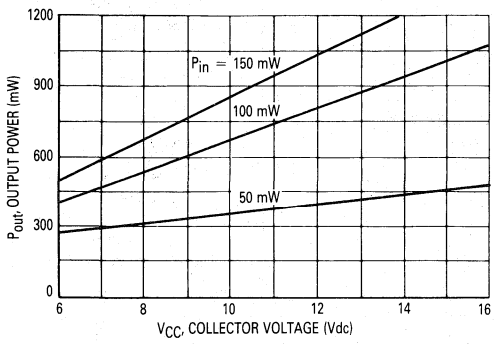


Figure 8. Output Power versus Collector Voltage
f = 870 MHz

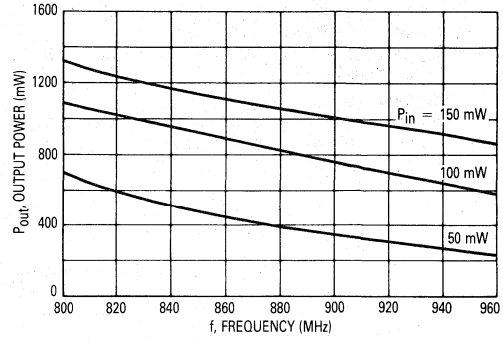
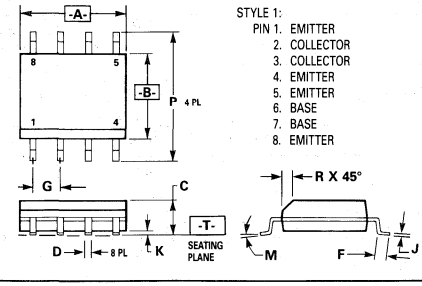


Figure 9. Output Power versus Frequency
V_{CC} = 12.5 Vdc

OUTLINE DIMENSIONS



STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. POSITIONAL TOLERANCE FOR D DIMENSION (8 PLACES):
⌖ | 0.25 (0.010) Ⓜ | T | B Ⓢ | A Ⓢ |
3. POSITIONAL TOLERANCE FOR P DIMENSION (4 PLACES):
⌖ | 0.25 (0.010) Ⓜ | B Ⓜ |
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: MILLIMETER.
6. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
7. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

CASE 751-02
SORF
(SO-8)

MRF9011
BF431*
MRF9011L
BF431L*

*European Part Numbers

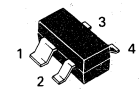
The RF Line

NPN Silicon High-Frequency Transistor

. . . designed primarily for use in high-gain, low-noise small-signal amplifiers for operation up to 2.5 GHz. Also usable in applications requiring fast switching times.

- High Current-Gain-Bandwidth Product — f_T = 3.8 GHz (Typ) @ I_C = 15 mAdc
- Low Noise Figure @ f = 1 GHz — $NF_{(matched)}$ = 1.8 dB (Typ)
- High Power Gain — $G_{pe(matched)}$ = 13.5 dB (Typ) @ f = 1 GHz
- Guaranteed RF Parameters
- Surface Mounted SOT-143 Offers Improved RF Performance
  - Lower Package Parasitics
  - High Gain
- Available In Both Standard Profile (MRF9011) and Low Profile (MRF9011L)
- Tape and Reel Packaging Options

SURFACE MOUNTED HIGH FREQUENCY TRANSISTOR NPN SILICON



CASE 318B-01
SOT-143

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CBO}	25	Vdc
Emitter-Base Voltage	V_{EBO}	2	Vdc
Collector-Current — Continuous	I_C	30	mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	0.30 3.3	Watt mW/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	300	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1 mAdc, I_B = 0)	$V_{(BR)CEO}$	15	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	25	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	2	—	—	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	—	—	50	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5 mAdc, V_{CE} = 5 Vdc)	h_{FE}	30	80	200	—

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS						
Current-Gain-Bandwidth Product (I_C = 15 mAdc, V_{CE} = 10 Vdc, f = 1 GHz)	Figure 6	f_T	—	3.8	—	GHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)	Figure 1	C_{cb}	—	0.55	1	pF
FUNCTIONAL TESTS						
Power Gain at Minimum Noise Figure (V_{CE} = 10 Vdc, I_C = 5 mA, f = 1 GHz)	Figure 5	G_{NFmin}	—	13.5	—	dB
Noise Figure (V_{CE} = 10 Vdc, I_C = 5 mA, f = 1 GHz)	Figure 5	NF_{min}	—	1.8	—	dB
Power Gain in 50 Ω System (V_{CE} = 10 Vdc, I_C = 5 mA, f = 1 GHz)	Figure 2	G_{NF}	9	10.2	—	dB
Noise Figure (V_{CE} = 10 Vdc, I_C = 5 mA, f = 1 GHz)	Figure 2	NF	—	2.3	3	dB

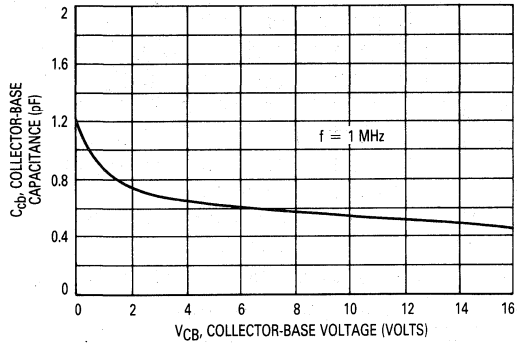


Figure 1. Collector-Base Capacitance versus Collector-Base Voltage

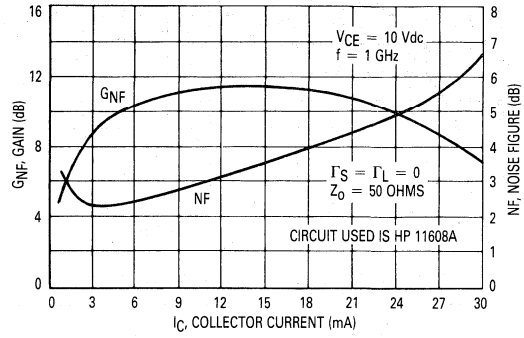


Figure 2. Gain and Noise Figure versus Collector Current

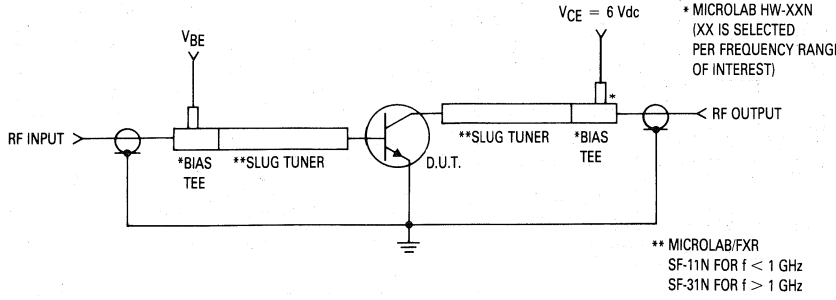


Figure 3. Functional Circuit Schematic

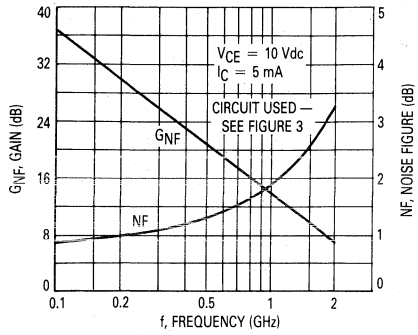


Figure 4. Gain and Noise Figure versus Frequency

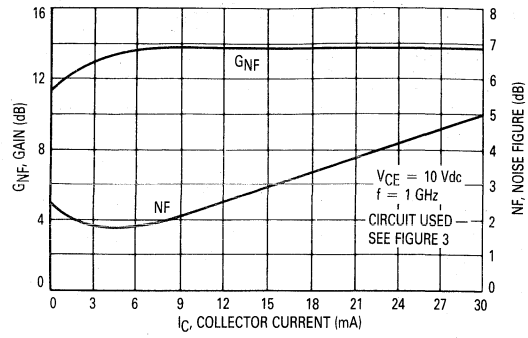


Figure 5. Gain and Noise Figure versus Collector Current

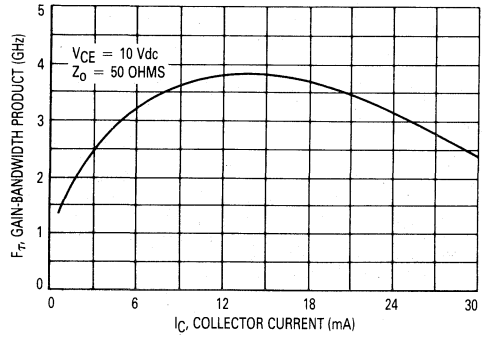


Figure 6. Gain-Bandwidth Product versus Collector Current

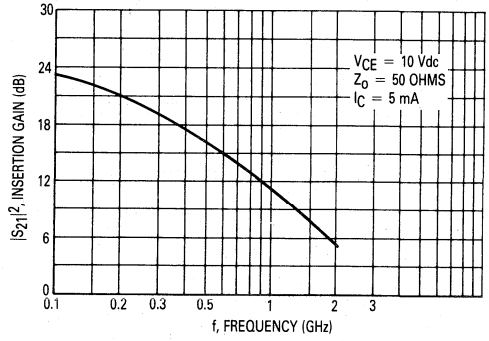


Figure 7. Insertion Gain versus Frequency

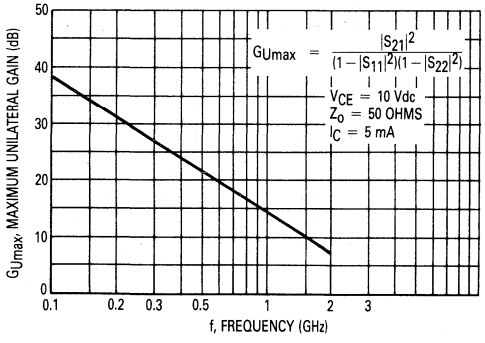
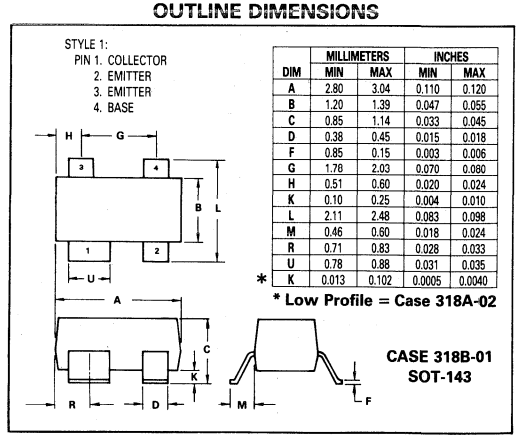


Figure 8. Maximum Unilateral Gain versus Frequency

OUTLINE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.110	0.120
B	1.20	1.39	0.047	0.055
C	0.85	1.14	0.033	0.045
D	0.38	0.45	0.015	0.018
F	0.85	0.15	0.003	0.006
G	1.78	2.03	0.070	0.080
H	0.51	0.60	0.020	0.024
K	0.10	0.25	0.004	0.010
L	2.11	2.48	0.083	0.098
M	0.46	0.60	0.018	0.024
R	0.71	0.83	0.028	0.033
U	0.78	0.88	0.031	0.035
K	0.013	0.102	0.0005	0.0040

* Low Profile = Case 318A-02

CASE 318B-01
SOT-143

COMMON EMITTER S-PARAMETERS

V_{CE} (Vdc)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
5	5	100	0.85	−41	13.64	153	0.03	65	0.93	−17
		200	0.78	−76	10.77	134	0.05	54	0.80	−29
		500	0.71	−131	6.10	102	0.08	35	0.55	−42
		1000	0.66	−169	3.22	77	0.08	33	0.45	−48
		2000	0.60	152	1.65	47	0.11	46	0.47	−63
	10	100	0.72	−59	20.01	145	0.03	62	0.87	−23
		200	0.70	−100	14.31	123	0.04	49	0.67	−36
		500	0.66	−150	7.03	94	0.06	38	0.44	−43
		1000	0.63	179	3.57	73	0.07	45	0.37	−46
		2000	0.58	147	1.79	46	0.11	57	0.41	−60
	15	100	0.65	−75	23.44	138	0.02	57	0.81	−27
		200	0.66	−118	15.56	116	0.04	46	0.59	−38
		500	0.65	−159	7.10	90	0.05	42	0.40	−40
		1000	0.63	174	3.57	71	0.06	52	0.35	−43
		2000	0.59	144	1.77	45	0.11	62	0.40	−58
	20	100	0.61	−89	24.32	133	0.02	51	0.77	−28
		200	0.66	−130	15.11	111	003	43	0.55	−35
		500	0.66	−166	6.68	88	0.04	46	0.41	−34
		1000	0.65	171	3.32	69	0.06	56	0.39	−39
		2000	0.61	143	1.65	43	0.10	65	0.44	−56
	30	100	0.63	−132	13.18	118	0.02	47	0.72	−15
		200	0.68	−157	7.07	104	0.02	44	0.66	−16
		500	0.69	−177	3.23	90	0.03	55	0.62	−24
		1000	0.70	165	1.78	71	0.05	65	0.59	−38
		2000	0.66	138	0.93	42	0.09	79	0.62	−62
10	5	100	0.85	−38	13.67	155	0.03	70	0.93	−14
		200	0.80	−71	10.97	136	0.05	56	0.83	−24
		500	0.70	−126	6.35	104	0.07	37	0.60	−35
		1000	0.65	−166	3.39	78	0.07	36	0.51	−40
		2000	0.58	154	1.74	48	0.10	50	0.54	−55
	10	100	0.75	−55	20.12	147	0.02	66	0.88	−19
		200	0.71	−94	14.60	125	0.04	50	0.72	−30
		500	0.65	−145	7.33	96	0.05	39	0.50	−35
		1000	0.62	−177	3.74	74	0.06	46	0.45	−38
		2000	0.57	149	1.88	47	0.10	60	0.49	−53
	15	100	0.68	−68	23.53	140	0.02	61	0.85	−22
		200	0.67	−110	15.90	119	0.03	49	0.65	−31
		500	0.64	−155	7.45	92	0.04	42	0.47	−32
		1000	0.62	177	3.74	71	0.06	53	0.44	−35
		2000	0.58	146	1.90	45	0.09	65	0.50	−51
	20	100	0.64	−79	24.77	135	0.02	56	0.81	−23
		200	0.64	−122	15.81	114	0.03	46	0.62	−29
		500	0.64	−161	7.10	89	0.04	46	0.48	−28
		1000	0.62	174	3.53	70	0.05	56	0.46	−33
		2000	0.59	145	1.75	44	0.09	68	0.53	−50
	30	100	0.61	−114	16.25	123	0.01	48	0.79	−15
		200	0.63	−147	9.10	107	0.02	49	0.71	−15
		500	0.65	−172	4.22	90	0.03	53	0.66	−22
		1000	0.66	168	2.27	71	0.05	63	0.63	−33
		2000	0.63	140	1.15	41	0.08	79	0.67	−53

MRF9331
BF432*
MRF9331L
BF432L*

*European Part Numbers

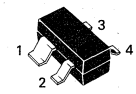
SURFACE MOUNTED
HIGH FREQUENCY
TRANSISTOR
NPN SILICON

The RF Line

NPN Silicon High-Frequency Transistor

. . . designed primarily for use in low power amplifiers to 1 GHz. Ideal for pagers and other battery operated systems where low power consumption is critical.

- Low Power Consumption Characterized for I_E = 0.1 to 1 mA
- High Current-Gain-Bandwidth Product — f_T = 5 GHz (Typ) @ I_C = 1 mAdc
- Low Noise Figure and High Power Gain @ f = 1 GHz — NF(matched) = 2.5 dB (Typ) & GNF(matched) = 12.5 dB (Typ)
- Guaranteed RF Parameters
- Surface Mounted SOT-143 Offers Improved RF Performance
  Lower Package Parasitics
  High Gain
- Available In Both Standard Profile (MRF9331) and Low Profile (MRF9331L)
- Tape and Reel Packaging Options



CASE 318A-02
SOT-143

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	8	Vdc
Collector-Base Voltage	V_{CBO}	15	Vdc
Emitter-Base Voltage	V_{EBO}	2	Vdc
Collector-Current — Continuous	I_C	1	mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 1	mW mW/°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	500	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 0.1 mAdc, I_B = 0)	$V_{(BR)CEO}$	8	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 0.01 mAdc, I_E = 0)	$V_{(BR)CBO}$	15	—	—	Vdc
Emitter-Base Leakage Current (V_{EB} = 2 Vdc, I_C = 0)	I_{EBO}	—	—	0.1	mAdc
Collector Cutoff Current (V_{CB} = 5 Vdc, I_E = 0)	I_{CBO}	—	—	50	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 0.5 mAdc, V_{CE} = 1 Vdc)	h_{FE}	30	80	200	—

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS						
Current-Gain-Bandwidth Product (I_C = 1 mAdc, V_{CE} = 1 Vdc, f = 1 GHz)	Figure 2	f_T	3.5	5	—	GHz
Collector-Base Capacitance (V_{CB} = 1 Vdc, I_E = 0, f = 1 MHz)	Figure 1	C_{cb}	—	0.21	0.3	pF
FUNCTIONAL TESTS						
Power Gain at Minimum Noise Figure (V_{CE} = 1 Vdc, I_C = 0.5 mA, f = 1 GHz)	Figure 5, 3	G_{NFmin}	—	12.5	—	dB
Noise Figure (V_{CE} = 1 Vdc, I_C = 0.5 mA, f = 1 GHz)	Figure 5, 3	NF_{min}	—	2.5	—	dB

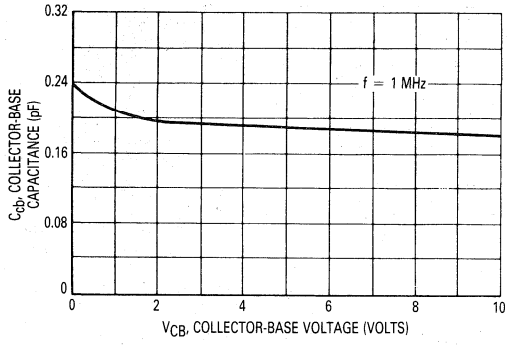


Figure 1. Collector-Base Capacitance versus Collector-Base Voltage

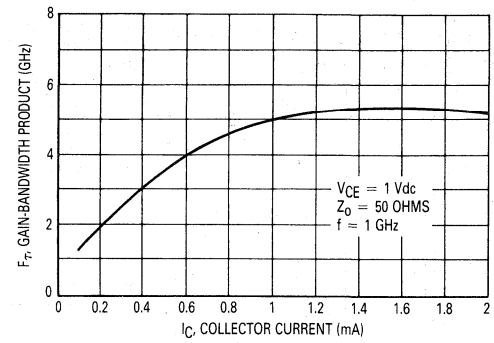


Figure 2. Current Gain-Bandwidth Product versus Collector Current

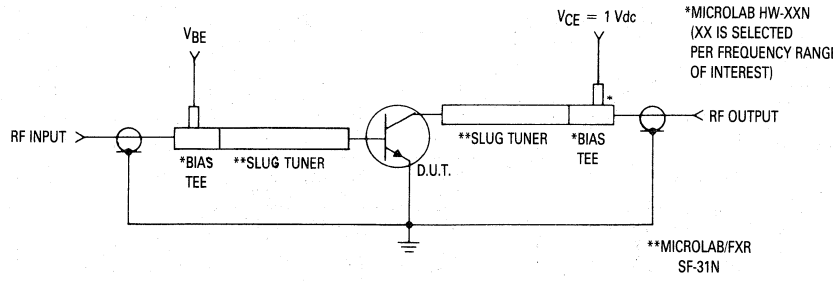


Figure 3. Functional Circuit Schematic

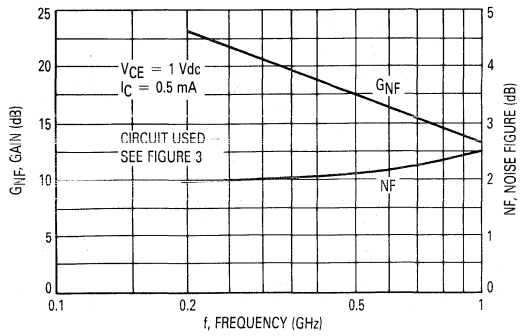


Figure 4. Gain and Noise Figure versus Frequency

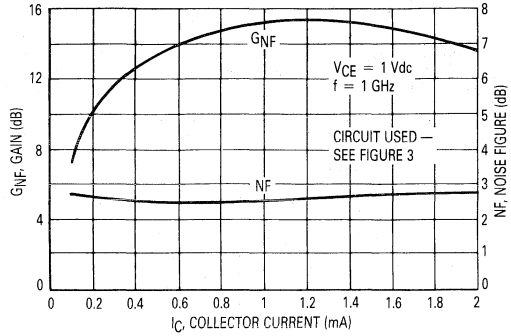


Figure 5. Gain and Noise Figure versus Collector Current

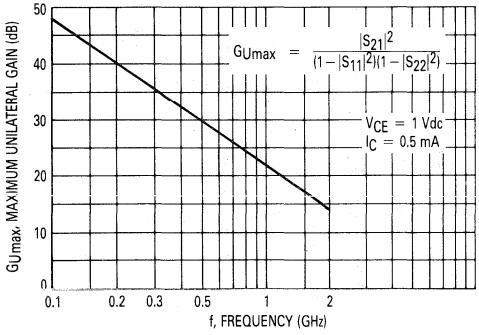
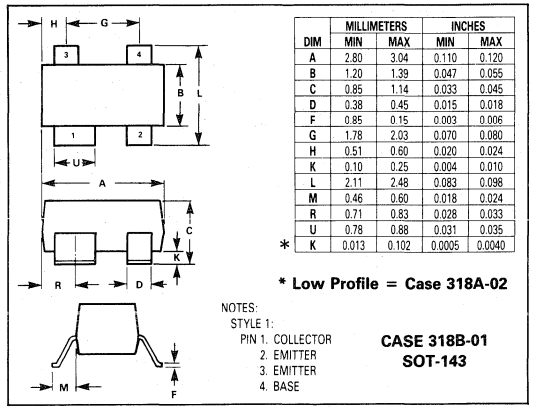


Figure 6. Maximum Unilateral Gain versus Frequency

OUTLINE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.110	0.120
B	1.20	1.39	0.047	0.055
C	0.85	1.14	0.033	0.045
D	0.38	0.45	0.015	0.018
F	0.85	0.15	0.003	0.006
G	1.78	2.03	0.070	0.080
H	0.51	0.60	0.020	0.024
K	0.10	0.25	0.004	0.010
L	2.11	2.48	0.083	0.098
M	0.46	0.60	0.018	0.024
R	0.71	0.83	0.028	0.033
U	0.78	0.88	0.031	0.035
* K	0.013	0.102	0.0005	0.0040

*** Low Profile = Case 318A-02**

COMMON EMITTER S-PARAMETERS

V_{CE} (Vdc)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
1	0.1	100	0.99	−1	0.35	174	0.01	87	1	−1
		200	1	−3	0.35	171	0.03	86	1	−4
		500	0.97	−9	0.34	156	0.07	81	1	−9
		1000	0.98	−19	0.38	134	0.13	72	1	−21
		2000	0.98	−36	0.45	103	0.22	59	1	−38
	0.25	100	0.99	−1	0.77	175	0.01	86	1	−1
		200	1	−4	0.77	173	0.03	86	1	−4
		500	0.96	−11	0.73	160	0.06	79	0.99	−11
		1000	0.96	−23	0.75	140	0.13	70	0.98	−23
		2000	0.94	−42	0.77	110	0.21	56	0.93	−42
	0.5	100	0.99	−2	1.43	174	0.01	86	1	−1
		200	0.99	−5	1.42	172	0.03	84	1	−5
		500	0.95	−13	1.33	158	0.06	77	0.99	−12
		1000	0.92	−28	1.3	137	0.13	67	0.95	−25
		2000	0.83	−51	1.2	107	0.19	54	0.91	−43

COMMON EMITTER S-PARAMETERS (Continued)

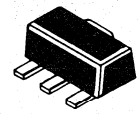
V_{CE} (Vdc)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
1	1	100	0.97	−3	2.68	173	0.01	85	1	−2
		200	0.97	−8	2.68	169	0.03	83	1	−6
		500	0.91	−19	2.42	152	0.06	74	0.96	−15
		1000	0.82	−37	2.22	128	0.11	62	0.89	−29
		2000	0.63	−59	1.74	97	0.17	53	0.8	−46
	2	100	0.93	−6	4.55	169	0.01	84	0.99	−4
		200	0.92	−13	4.3	163	0.03	81	0.98	−9
		500	0.81	−29	3.8	142	0.06	69	0.91	−19
		1000	0.62	−52	3.1	115	0.1	59	0.81	−31
		2000	0.4	−66	2	85	0.14	55	0.75	−44
3	0.1	100	0.99	−1	0.34	175	0.01	88	1	−1
		200	1	−3	0.34	172	0.03	86	1	−3
		500	0.99	−8	0.32	157	0.06	81	1	−9
		1000	0.99	−18	0.36	137	0.11	73	1	−20
		2000	1	−34	0.43	107	0.2	61	1	−37
	0.25	100	0.99	−1	0.76	175	0.01	86	1	−1
		200	1	−4	0.76	173	0.03	86	1	−4
		500	0.98	−10	0.72	161	0.06	80	1	−10
		1000	0.98	−21	0.75	143	0.11	72	0.99	−22
		2000	0.97	−40	0.75	113	0.19	59	0.98	−39
	0.5	100	0.99	−2	1.4	175	0.01	86	1	−1
		200	0.99	−5	1.42	172	0.03	84	1	−4
		500	0.96	−12	1.3	159	0.06	78	0.99	−11
		1000	0.93	−25	1.3	141	0.11	68	0.96	−23
		2000	0.87	−47	1.2	111	0.18	57	0.93	−41
	1	100	0.97	−3	2.67	174	0.01	85	1	−2
		200	0.98	−7	2.67	170	0.02	84	1	−6
		500	0.93	−17	2.42	154	0.06	76	0.97	−14
		1000	0.84	−34	2.29	133	0.1	65	0.91	−26
		2000	0.67	−55	1.82	101	0.16	56	0.85	−43
	2	100	0.95	−5	4.64	172	0.01	85	1	−3
		200	0.94	−10	4.62	166	0.02	81	0.99	−8
		500	0.85	−25	4	147	0.05	72	0.94	−17
		1000	0.69	−44	3.4	122	0.09	63	0.84	−29
		2000	0.48	−61	2.3	91	0.13	57	0.78	−42
5	0.1	100	1	0	0.36	175	0.01	85	1	−1
		200	1	−3	0.34	172	0.02	87	1	−3
		500	0.99	−8	0.32	158	0.06	82	1	−9
		1000	1	−17	0.36	138	0.11	74	1	−19
		2000	0.94	−35	0.42	108	0.2	63	1	−36
	0.25	100	1	−1	0.76	176	0.01	86	1	−1
		200	1	−3	0.76	174	0.02	86	1	−4
		500	0.97	−9	0.71	161	0.06	80	1	−10
		1000	0.97	−20	0.74	143	0.11	73	0.99	−21
		2000	0.97	−38	0.75	115	0.18	61	0.99	−38
	0.5	100	0.99	−1	1.4	175	0.01	86	1	−1
		200	1	−5	1.41	173	0.02	85	1	−4
		500	0.98	−12	1.3	159	0.06	79	0.99	−11
		1000	0.93	−25	1.3	141	0.1	70	0.97	−23
		2000	0.87	−45	1.2	111	0.17	58	0.94	−40
	1	100	0.98	−3	2.7	174	0.01	86	1	−2
		200	0.98	−7	2.7	170	0.02	84	1	−5
		500	0.93	−17	2.42	155	0.5	76	0.97	−13
		1000	0.85	−33	2.3	134	0.09	66	0.92	−26
		2000	0.67	−55	2	103	0.15	57	0.85	−42
	2	100	0.95	−4	4.6	172	0.01	86	1	−3
		200	0.94	−10	4.6	166	0.02	83	1	−7
		500	0.86	−24	3.9	148	0.5	73	0.94	−16
		1000	0.7	−43	3.4	123	0.9	64	0.86	−28
		2000	0.5	−60	2.3	92	0.13	59	0.8	−40

MXR3866

Die Source Same as 2N3866

RF TRANSISTOR

NPN SILICON



CASE 345-01, STYLE 1
SOT-89

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	V
Collector-Base Voltage	V_{CBO}	55	V
Emitter-Base Voltage	V_{EBO}	3.5	V
Collector Current — Continuous	I_C	0.4	A
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Total Device Dissipation, T_A = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Storage Temperature	T_{stg}	150	°C
*Thermal Resistance Junction to Ambient	$R_{\theta JA}$	125	°C/W

*Package mounted on 99.5% alumina 10 x 12 x 0.6 mm.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

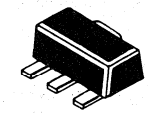
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 5.0 mA, R_{BE} = 10 Ω)	$V_{(BR)CER}$	55	—	V
Collector-Emitter Sustaining Voltage (I_C = 5.0 mA)	$V_{CEO(sus)}$	30	—	V
Collector-Base Breakdown Voltage (I_C = 0.1 mA)	$V_{(BR)CBO}$	55	—	V
Emitter-Base Breakdown Voltage (I_E = 0.1 mA)	$V_{(BR)EBO}$	3.5	—	V
Collector Cutoff Current (V_{CE} = 28 V)	I_{CEO}	—	20	μA
Collector Cutoff Current (V_{CE} = 55 V, V_{BE} = 1.5 V)	I_{CEX}	—	100	μA
ON CHARACTERISTICS				
DC Current Gain (I_C = 0.36 A, V_{CE} = 5.0 V) (I_C = 0.05 A, V_{CE} = 5.0 V)	h_{FE}	 5.0 10	 — 200	—
Collector-Emitter Saturation Voltage (I_C = 100 mA, I_B = 20 mA)	$V_{CE(sat)}$	—	1.0	V
SMALL-SIGNAL CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 50 mA, V_{CE} = 15 V, f = 200 MHz)	f_T	500	—	MHz
Output Capacitance (V_{CB} = 30 V, f = 1.0 MHz)	C_{obo}	—	3.0	pF

MXR5160

Die Source Same as 2N5160

RF TRANSISTOR

PNP SILICON



CASE 345-01, STYLE 1
SOT-89

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	V
Collector-Base Voltage	V_{CBO}	60	V
Emitter-Base Voltage	V_{EBO}	4.0	V
Collector Current — Continuous	I_C	0.4	A
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Total Device Dissipation, T_A = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Storage Temperature	T_{stg}	150	°C
*Thermal Resistance Junction to Ambient	$R_{\theta JA}$	125	°C/W

*Package mounted on 99.5% alumina 10 x 12 x 0.6 mm.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

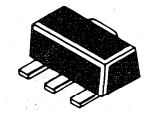
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I_C = 5.0 mA)	$V_{CEO(sus)}$	40	—	V
Emitter-Base Breakdown Voltage (I_E = 0.1 mA)	$V_{(BR)EBO}$	4.0	—	V
Collector Cutoff Current (V_{CB} = 28 V)	I_{CBO}	—	1.0	μA
Collector Cutoff Current (V_{CE} = 60 V)	I_{CES}	—	0.1	mA
Emitter Cutoff Current (V_{CE} = 28 V)	I_{CEO}	—	20	μA
ON CHARACTERISTICS				
DC Current Gain (I_C = 50 mA, V_{CE} = 5.0 V)	h_{FE}	10	—	—
SMALL-SIGNAL CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 50 mA, V_{CE} = 15 V, f = 200 MHz)	f_T	500	—	MHz

MXR5583

Die Source Same as 2N5583

HIGH FREQUENCY RF TRANSISTOR

PNP SILICON



CASE 345-01, STYLE 1
SOT-89

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	V
Collector-Base Voltage	V_{CBO}	30	V
Emitter-Base Voltage	V_{EBO}	3.0	V
Collector Current — Continuous	I_C	500	mA
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Total Device Dissipation, T_A = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Storage Temperature	T_{stg}	150	°C
*Thermal Resistance Junction to Ambient	$R_{\theta JA}$	125	°C/W

*Package mounted on 99.5% alumina 10 x 12 x 0.6 mm.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

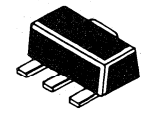
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage(1) (I_C = 10 mA)	$V_{(BR)CEO}$	30	—	V
Collector-Base Breakdown Voltage (I_C = 10 μA)	$V_{(BR)CBO}$	30	—	V
Emitter-Base Breakdown Voltage (I_E = 100 μA)	$V_{(BR)EBO}$	3.0	—	V
Collector Cutoff Current (V_{CB} = 20 V)	I_{CBO}	—	50	nA
Emitter Cutoff Current (V_{EB} = 2.0 V)	I_{EBO}	—	0.5	μA
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 40 mA, V_{CE} = 2.0 V) (I_C = 100 mA, V_{CE} = 2.0 V) (I_C = 300 mA, V_{CE} = 5.0 V)	h_{FE}	 20 25 15	 — 100 —	—
Collector-Emitter Saturation Voltage (1) (I_C = 100 mA, I_B = 10 mA)	$V_{CE(sat)}$	—	0.8	V
Base-Emitter On Voltage (1) (I_C = 100 mA, V_{CE} = 2.0 V)	$V_{BE(on)}$	—	1.8	V
SMALL-SIGNAL CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 40 mA, V_{CE} = 10 V, f = 100 MHz) (I_C = 100 mA, V_{CE} = 10 V, f = 100 MHz)	f_T	 1000 1300	 — —	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

MXR5943

Die Source Same as 2N5943

RF TRANSISTOR
NPN SILICON



CASE 345-01, STYLE 1
SOT-89

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	V
Collector-Base Voltage	V_{CBO}	40	V
Emitter-Base Voltage	V_{EBO}	3.5	V
Collector Current — Continuous	I_C	400	mA
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

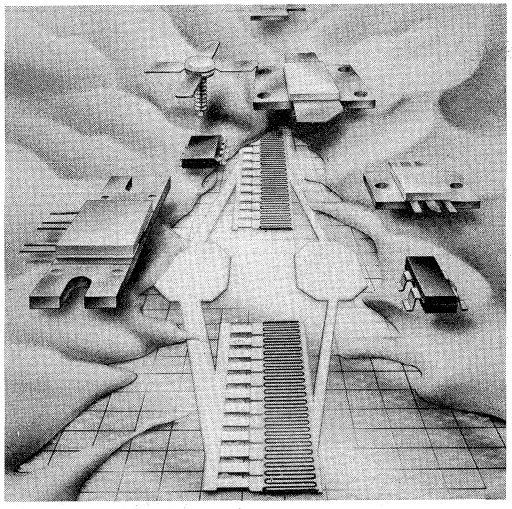
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Total Device Dissipation, T_A = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Storage Temperature	T_{stg}	150	°C
*Thermal Resistance Junction to Ambient	$R_{\theta JA}$	125	°C/W

*Package mounted on 99.5% alumina 10 x 12 x 0.6 mm.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 5.0 mA)	$V_{(BR)CEO}$	30	—	V
Collector-Base Breakdown Voltage (I_C = 100 μA)	$V_{(BR)CBO}$	40	—	V
Emitter-Base Breakdown Voltage (I_E = 100 μA)	$V_{(BR)EBO}$	3.5	—	V
Collector Cutoff Current (V_{CE} = 20 V)	I_{CEO}	—	50	μA
Collector Cutoff Current (V_{CB} = 15 V)	I_{CBO}	—	10	μA
ON CHARACTERISTICS				
DC Current Gain (I_C = 50 mA, V_{CE} = 15 V)	h_{FE}	25	300	—
Collector-Emitter Saturation Voltage (I_C = 100 mA, I_B = 10 mA)	$V_{CE(sat)}$	—	0.2	V
Base-Emitter Saturation Voltage (I_C = 100 mA, I_B = 10 mA)	$V_{BE(sat)}$	—	1.0	V
SMALL SIGNAL CHARACTERISTICS				
Current-Gain — Bandwidth Product	f_T			MHz
(I_C = 25 mA, V_{CE} = 15 V, f = 200 MHz)		1000	—	
(I_C = 50 mA, V_{CE} = 15 V, f = 200 MHz)		1200	—	
(I_C = 100 mA, V_{CE} = 15 V, f = 200 MHz)		1000	—	



Amplifiers 4

MHW590

The RF Line

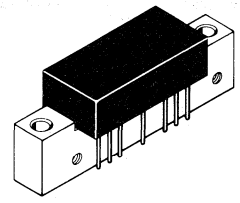
LOW DISTORTION WIDEBAND AMPLIFIER MODULE

. . . low-noise, high-gain, ultra-linear, thin-film hybrid. Designed for multi-purpose broadband 50 to 100 ohm system applications requiring superior gain and current stability with temperature.

- Supply Voltage = 24 V Nominal
- Broadband Power Gain —
  G_p = 34 dB (Typ) @ f = 10-400 MHz
- Broadband Noise Figure —
  NF = 3.5 dB (Typ) @ f = 300 MHz
- Ideal for Low Level Wideband Linear Amplifiers and AM Modulators in VHF/UHF Communications Equipment and RF Instrumentation Applications

10–400 MHz

HIGH GAIN AMPLIFIER



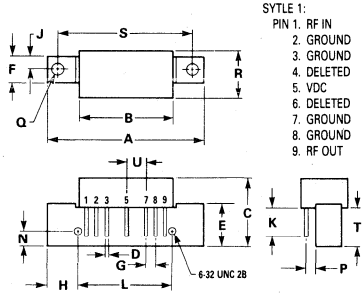
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{DC}	28	Vdc
Input Power	P_{in}	5.0	dBm
Operating Case Temperature Range	T_C	-20 to +90	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ELECTRICAL CHARACTERISTICS

(V_{DC} = 24 Vdc, Z_o = 50 Ω, T_C = 25°C. All characteristics guaranteed over bandwidth listed under "Frequency Range", unless specified otherwise.)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	10	—	400	MHz
Power Gain	G_p	31.5	34	35.5	dB
Gain Flatness	F	—	—	±1.5	dB
Voltage Standing Wave Ratio, In/Out (f = 10-300 MHz) (f = 300-400 MHz)	VSWR	 — —	 1.5:1 2:1	 — —	
1 dB Compression (f = 10 MHz) (f = 200 MHz) (f = 400 MHz)	P1	 — 700 —	 800 800 300	 — — —	mW
Reverse Isolation	P_{RI}	43	50	—	dB
2nd Harmonic (P_{out} = 10 mW)	d_{so}	—	-66	—	dB
Third Order Intercept	I_{TO}	—	43	—	dBm
Peak Envelope Power for -32 dB Distortion	PEP	—	500	—	mW
Noise Figure (f = 60 MHz) (f = 300 MHz)	NF	 — —	 4.0 3.5	 — 5.5	dB
DC Voltage	V_{DC}	—	24	28	V
DC Current	I_{DC}	—	300	340	mA



SYTLE 1:
PIN 1. RF IN
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUT

NOTE:
1. MOUNTING HOLES WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.41	2.67	0.095	0.105
H	9.65	9.78	0.380	0.385
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.335
L	25.40 BSC		1.000 BSC	
N	4.06	4.32	0.160	0.170
P	2.16	2.92	0.085	0.115
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
T	11.05	11.43	0.435	0.450
U	4.95	5.21	0.195	0.205

CASE 714-03

FIGURE 1 – POWER GAIN AND RETURN LOSS versus FREQUENCY

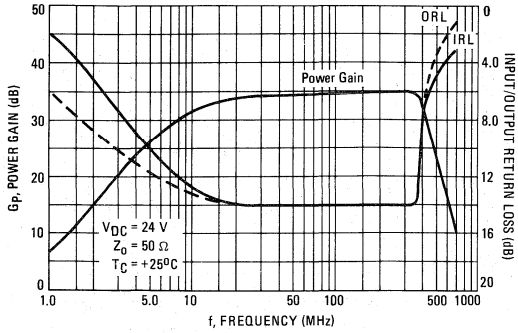


FIGURE 2 – POWER GAIN versus FREQUENCY

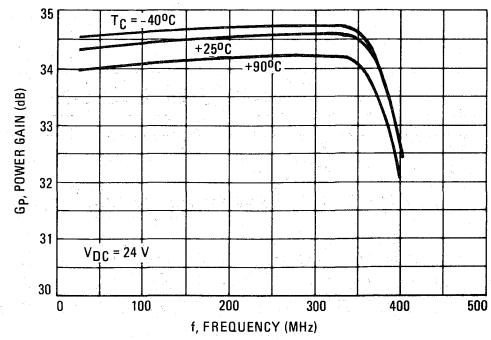


FIGURE 3 – POWER GAIN versus SUPPLY VOLTAGE

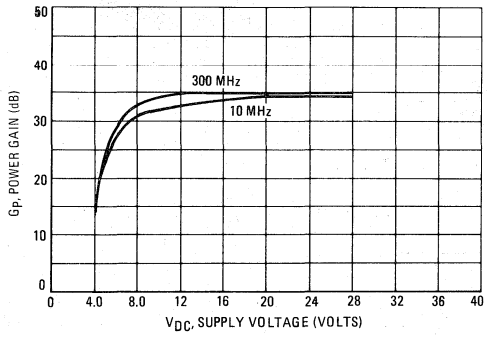


FIGURE 4 – NOISE FIGURE versus SUPPLY VOLTAGE

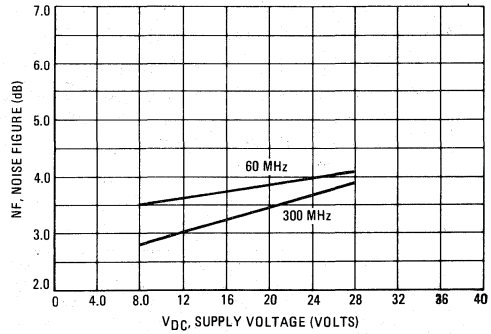


FIGURE 5 – OUTPUT POWER versus INPUT POWER

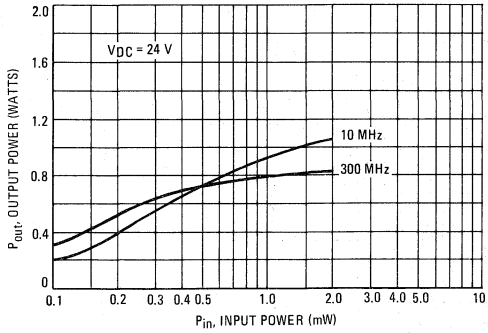
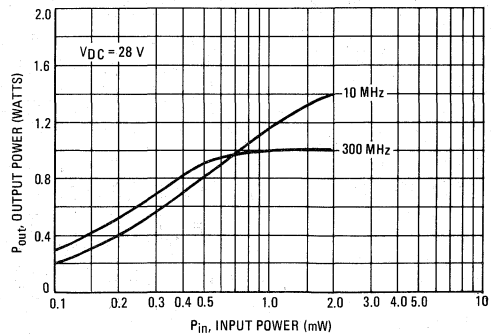


FIGURE 6 – OUTPUT POWER versus INPUT POWER



4

FIGURE 7 – INTERMODULATION DISTORTION – THIRD ORDER versus OUTPUT POWER

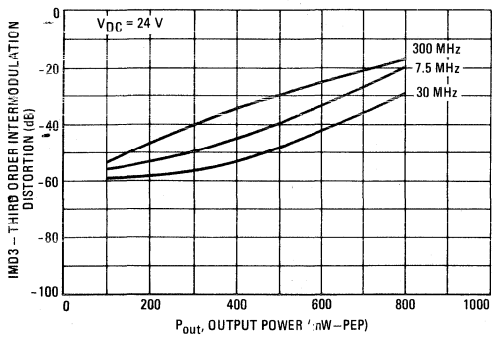


FIGURE 8 – INTERMODULATION DISTORTION – FIFTH ORDER versus OUTPUT POWER

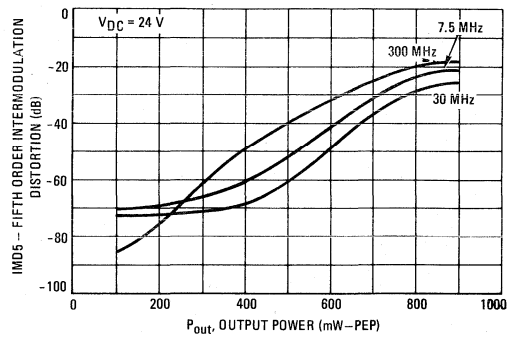


FIGURE 9 – INTERMODULATION DISTORTION – THIRD ORDER versus OUTPUT POWER

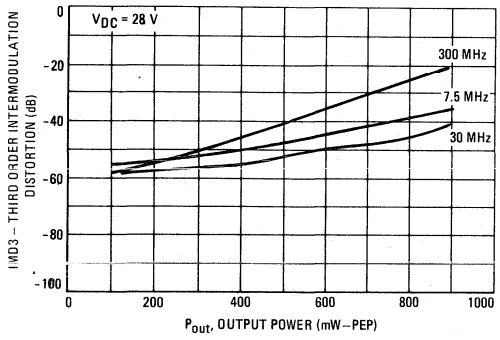


FIGURE 10 – INTERMODULATION DISTORTION – FIFTH ORDER versus OUTPUT POWER

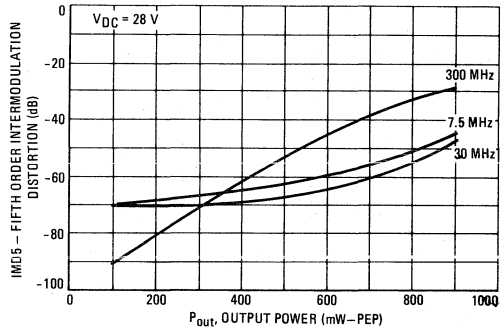
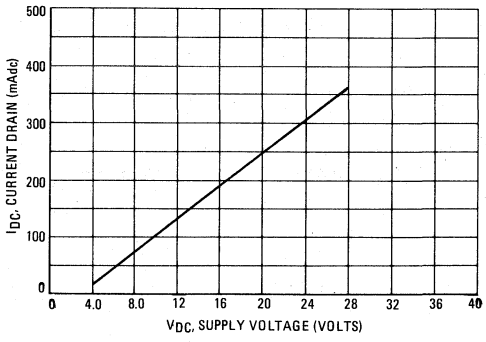


FIGURE 11 – DC CURRENT DRAIN versus SUPPLY VOLTAGE



4

MHW591

The RF Line

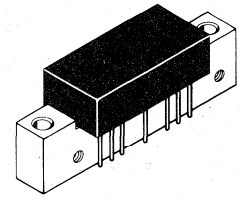
LOW DISTORTION WIDEBAND AMPLIFIER MODULE

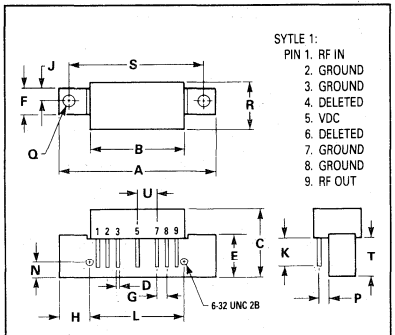
. . . low-noise, high-gain, ultra-linear, thin-film hybrid. Designed for multi-purpose broadband 50 to 100 ohm system applications requiring superior gain and current stability with temperature.

- Supply Voltage = 13.6 V Nominal
- Broadband Power Gain —
  G_p = 36.5 dB (Typ) @ f = 1-250 MHz
- Broadband Noise Figure —
  NF = 3.7 dB (Typ) @ f = 30 MHz
- Ideal for Low Level Wideband Linear Amplifiers and AM Modulators in HF/SSB, VHF Communications Equipment and RF Instrumentation Applications

1.0–250 MHz

HIGH GAIN AMPLIFIER





NOTE:
1. MOUNTING HOLES WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.41	2.67	0.095	0.105
H	9.65	9.78	0.380	0.385
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.335
L	25.40 BSC		1.000 BSC	
N	4.06	4.32	0.160	0.170
P	2.16	2.92	0.085	0.115
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
T	11.05	11.43	0.435	0.450
U	4.95	5.21	0.195	0.205

CASE 714-03

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{DC}	16	Vdc
Input Power	P_{in}	3.0	dBm
Operating Case Temperature Range	T_C	-20 to +90	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{DC} = 13.6 Vdc, Z_o = 50 Ω, T_C = 25°C. All characteristics guaranteed over bandwidth listed under "Frequency Range", unless specified otherwise.)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	1.0	—	250	MHz
Power Gain	G_p	34.5	36.5	38	dB
Gain Flatness	F	—	—	±1.5	dB
Voltage Standing Wave Ratio, In/Out	VSWR				
(f = 1.0-30 MHz)		—	1.5:1	—	
(f = 30-250 MHz)		—	2:1	—	
1 dB Compression	P1				mW
(f = 30 MHz)		650	800	—	
(f = 100 MHz)		—	700	—	
(f = 250 MHz)		—	250	—	
Peak Envelope Power	PEP				mW
(IMD3 = -30 dB, f = 30 MHz)		700	850	—	
(IMD3 = -30 dB, f = 100 MHz)		—	600	—	
(IMD3 = -30 dB, f = 250 MHz)		—	300	—	
Noise Figure	NF				dB
(f = 30 MHz)		—	3.7	5.0	
(f = 100 MHz)		—	3.7	—	
(f = 250 MHz)		—	4.5	—	
DC Voltage	V_{DC}	—	13.6	16	V
DC Current	I_{DC}	—	300	340	mA

4

FIGURE 1 – POWER GAIN versus FREQUENCY

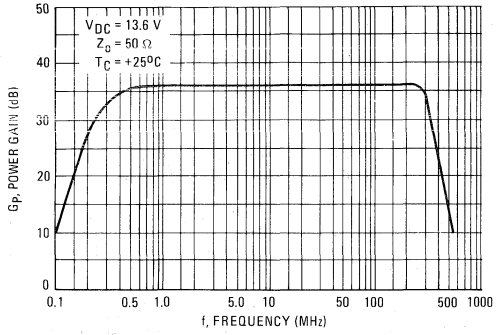


FIGURE 2 – POWER GAIN versus FREQUENCY

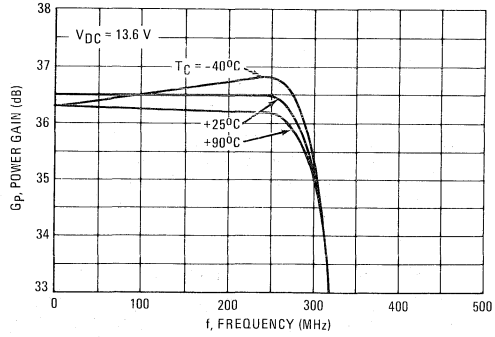


FIGURE 3 – POWER GAIN versus SUPPLY VOLTAGE

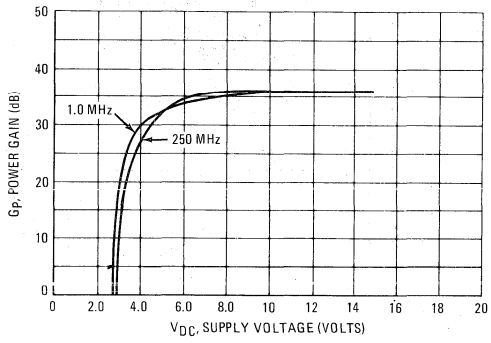


FIGURE 4 – NOISE FIGURE versus SUPPLY VOLTAGE

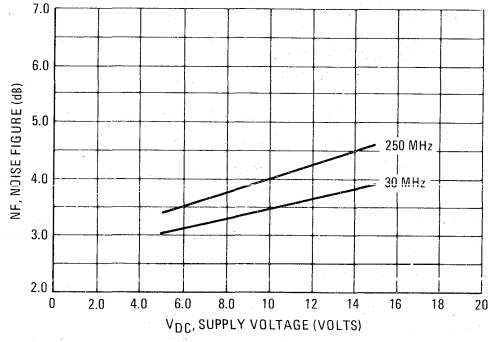


FIGURE 5 – OUTPUT POWER versus INPUT POWER

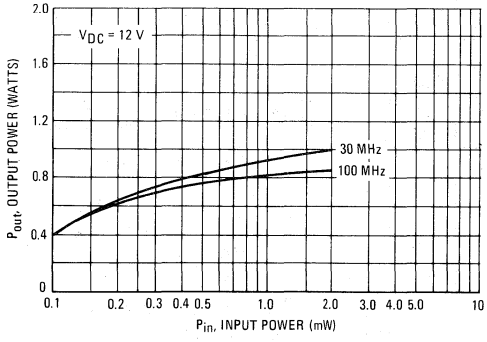
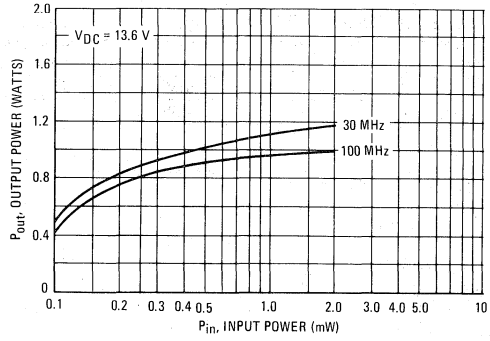


FIGURE 6 – OUTPUT POWER versus INPUT POWER



4

FIGURE 7 – INTERMODULATION DISTORTION versus OUTPUT POWER

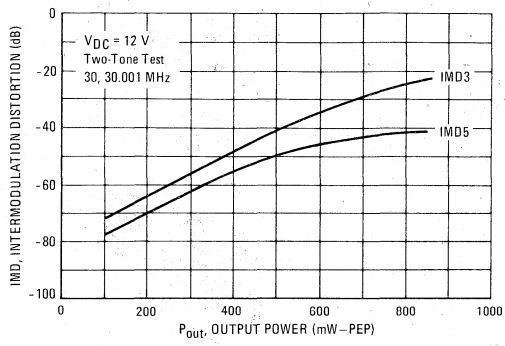


FIGURE 8 – INTERMODULATION DISTORTION versus OUTPUT POWER

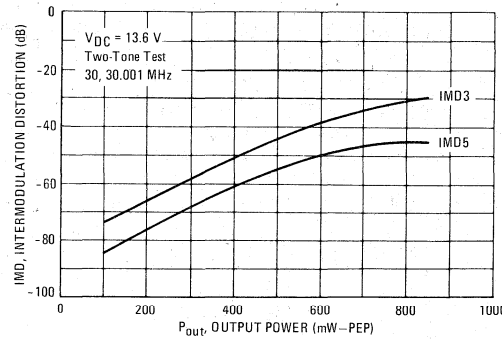
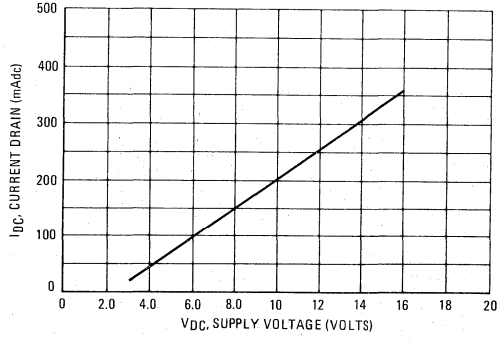


FIGURE 9 – DC CURRENT DRAIN versus SUPPLY VOLTAGE



4

MHW592

The RF Line

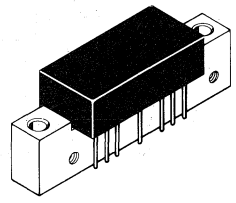
LOW DISTORTION WIDEBAND AMPLIFIER MODULE

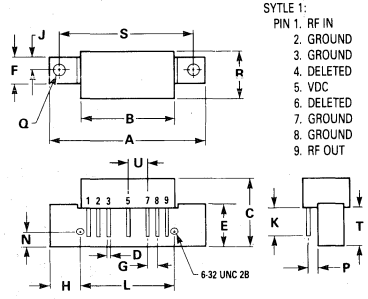
. . . low-noise, high-gain, ultra-linear, thin-film hybrid. Designed for multi-purpose broadband 50 to 100 ohm system applications requiring superior gain and current stability with temperature.

- Supply Voltage = 24 V Nominal
- Broadband Power Gain — G_p = 35 dB (Typ) @ f = 1-250 MHz
- Broadband Noise Figure — NF = 3.6 dB (Typ) @ f = 30 MHz
- Ideal for Low Level Wideband Linear Amplifiers and AM Modulators in HF/SSB, VHF Communications Equipment and RF Instrumentation Applications

1.0–250 MHz

HIGH GAIN AMPLIFIER





SYTLE 1:
PIN 1. RF IN
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUT

NOTE:
1. MOUNTING HOLES WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.41	2.67	0.095	0.105
H	9.65	9.78	0.380	0.385
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.335
L	25.40 BSC		1.000 BSC	
N	4.06	4.32	0.160	0.170
P	2.16	2.92	0.085	0.115
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
T	11.05	11.43	0.435	0.450
U	4.95	5.21	0.195	0.205

CASE 714-03

4

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{DC}	28	Vdc
Input Power	P_{in}	5.0	dBm
Operating Case Temperature Range	T_C	-20 to +90	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{DC} = 24 Vdc, Z_o = 50 Ω, T_C = 25°C. All characteristics guaranteed over bandwidth listed under "Frequency Range", unless specified otherwise.)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	1.0	—	250	MHz
Power Gain	G_p	33.5	35	36.5	dB
Gain Flatness	F	—	—	±1.0	dB
Voltage Standing Wave Ratio, In/Out	VSWR				
(f = 1.0-30 MHz)		—	1.5:1	—	
(f = 30-250 MHz)		—	2:1	—	
1 dB Compression	P1				mW
(f = 30 MHz)		750	900	—	
(f = 100 MHz)		—	900	—	
(f = 250 MHz)		—	750	—	
Peak Envelope Power	PEP				mW
(IMD3 = -30 dB, f = 30 MHz)		700	850	—	
(IMD3 = -30 dB, f = 100 MHz)		—	850	—	
(IMD3 = -30 dB, f = 250 MHz)		—	600	—	
Noise Figure	NF				dB
(f = 30 MHz)		—	3.6	5.0	
(f = 100 MHz)		—	3.7	—	
(f = 250 MHz)		—	3.9	—	
DC Voltage	V_{DC}	—	24	28	V
DC Current	I_{DC}	—	300	340	mA

FIGURE 1 – POWER GAIN versus FREQUENCY

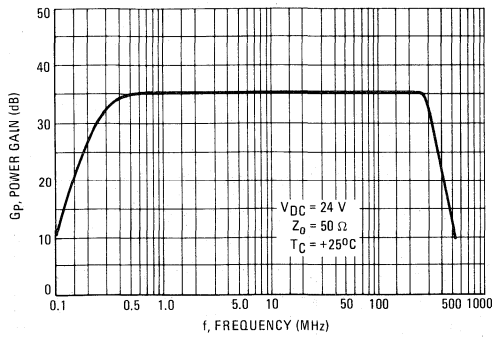


FIGURE 2 – POWER GAIN versus FREQUENCY

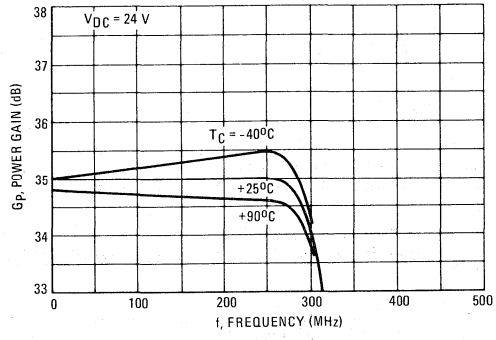


FIGURE 3 – POWER GAIN versus SUPPLY VOLTAGE

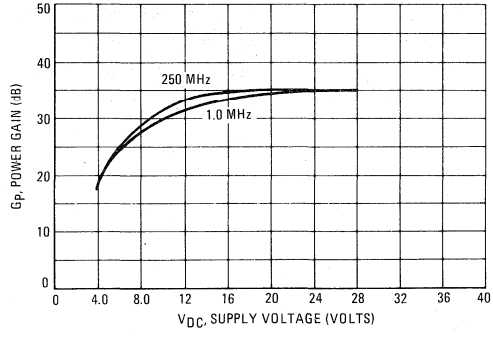


FIGURE 4 – NOISE FIGURE versus SUPPLY VOLTAGE

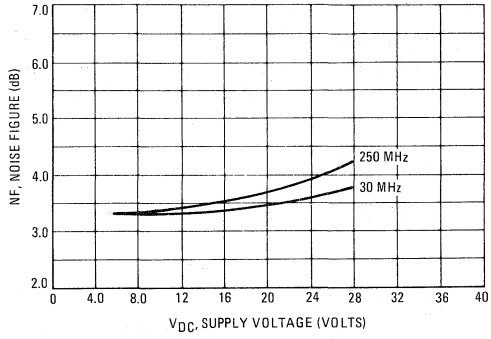


FIGURE 5 – OUTPUT POWER versus INPUT POWER

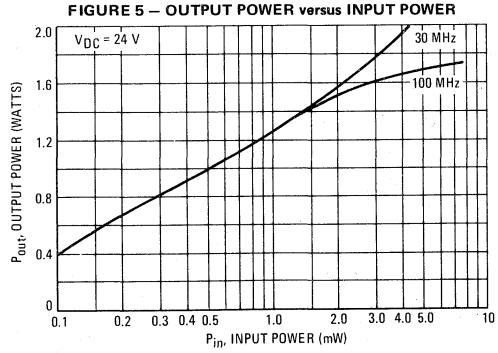
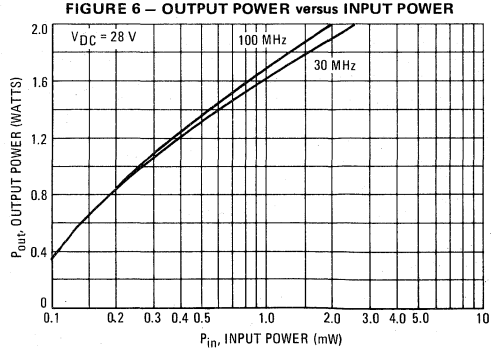


FIGURE 6 – OUTPUT POWER versus INPUT POWER



4

FIGURE 7 – INTERMODULATION DISTORTION versus OUTPUT POWER

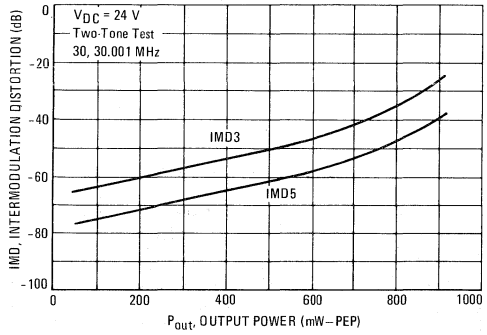


FIGURE 8 – INTERMODULATION DISTORTION versus OUTPUT POWER

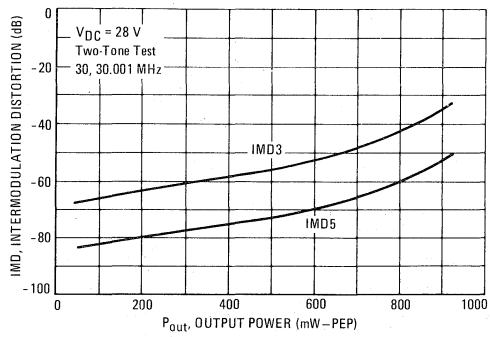
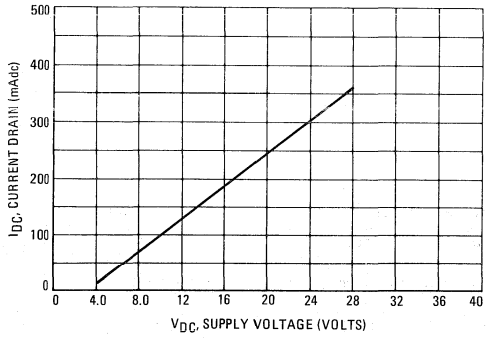


FIGURE 9 – DC CURRENT DRAIN versus SUPPLY VOLTAGE



4

MHW593

The RF Line

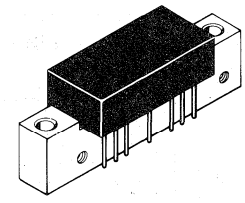
LOW DISTORTION WIDEBAND AMPLIFIER MODULE

. . . low-noise, high-gain, ultra-linear, thin-film hybrid. Designed for multi-purpose broadband 50 to 100 ohm system applications requiring superior gain and current stability with temperature.

- Supply Voltage = 13.6 V Nominal
- Broadband Power Gain — G_p = 34.5 dB (Typ) @ f = 10-400 MHz
- Broadband Noise Figure — NF = 4.0 dB (Typ) @ f = 300 MHz
- Ideal for Low Level Wideband Linear Amplifiers and AM Modulators in VHF/UHF Communications Equipment and RF Instrumentation Applications

10–400 MHz

HIGH GAIN AMPLIFIER

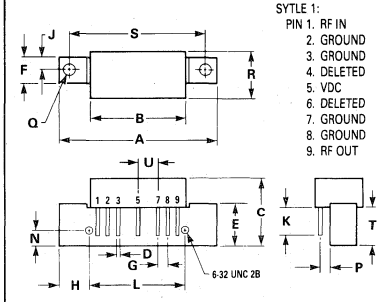


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{DC}	16	Vdc
Input Power	P_{in}	3.0	dBm
Operating Case Temperature Range	T_C	-20 to +90	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{DC} = 13.6 Vdc, Z_o = 50 Ω, T_C = 25°C. All characteristics guaranteed over bandwidth listed under "Frequency Range", unless specified otherwise.)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	10	—	400	MHz
Power Gain	G_p	33	34.5	36	dB
Gain Flatness	F	—	—	±1.0	dB
Voltage Standing Wave Ratio, In/Out (f = 10-300 MHz) (f = 300-400 MHz)	VSWR	 — —	 1.5:1 2:1	 — —	
1 dB Compression (f = 10 MHz) (f = 200 MHz) (f = 400 MHz)	P1	 — 500 —	 600 600 200	 — — —	mW
Reverse Isolation	P_{RI}	45	50	—	dB
2nd Harmonic (P_{out} = 10 mW)	d_{so}	—	-55	—	dB
Third Order Intercept	I_{TO}	—	38	—	dBm
Peak Envelope Power for -32 dB Distortion	PEP	—	300	—	mW
Noise Figure (f = 60 MHz) (f = 300 MHz)	NF	 — —	 3.7 4.0	 — 5.5	dB
DC Voltage	V_{DC}	—	13.6	16	V
DC Current	I_{DC}	—	300	340	mA



SYTLE 1:
PIN 1. RF IN
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUT

NOTE:
1. MOUNTING HOLES WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.41	2.67	0.095	0.105
H	9.65	9.78	0.380	0.385
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.335
L	25.40 BSC		1.000 BSC	
N	4.06	4.32	0.160	0.170
P	2.16	2.92	0.085	0.115
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
T	11.05	11.43	0.435	0.450
U	4.95	5.21	0.195	0.205

CASE 714-03

4

FIGURE 1 – POWER GAIN AND RETURN LOSS versus FREQUENCY

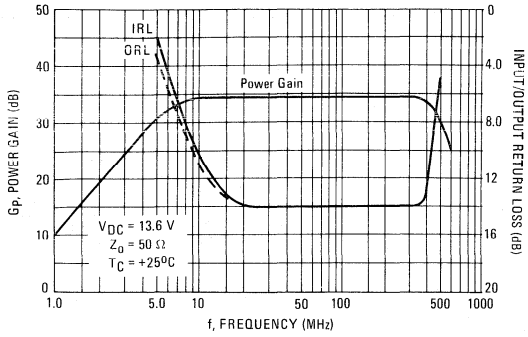


FIGURE 2 – POWER GAIN versus FREQUENCY

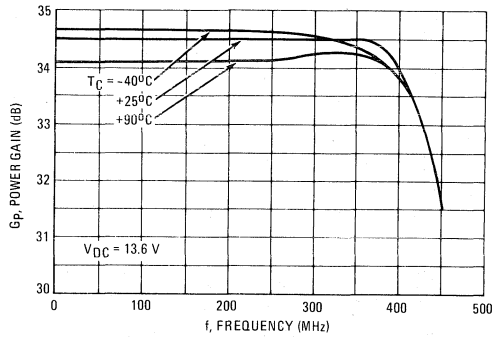


FIGURE 3 – POWER GAIN versus SUPPLY VOLTAGE

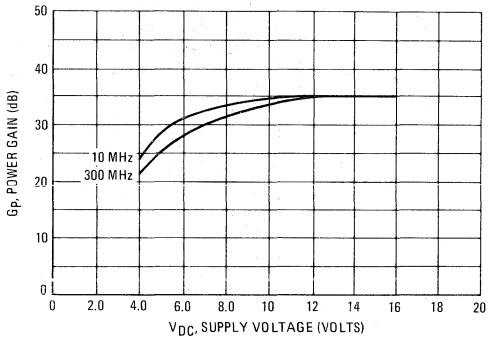


FIGURE 4 – NOISE FIGURE versus SUPPLY VOLTAGE

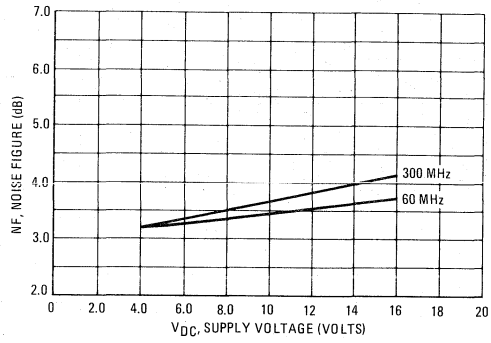


FIGURE 5 – OUTPUT POWER versus INPUT POWER

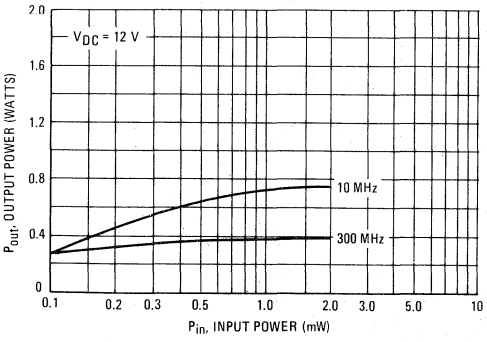
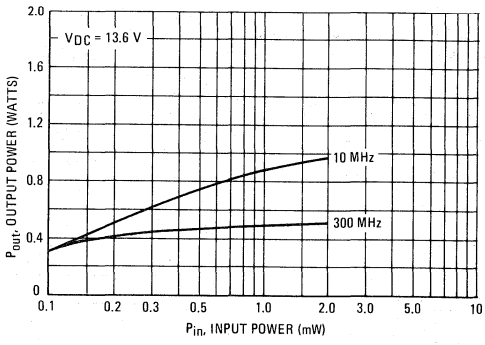


FIGURE 6 – OUTPUT POWER versus INPUT POWER



4

FIGURE 7 – INTERMODULATION DISTORTION – THIRD ORDER versus OUTPUT POWER

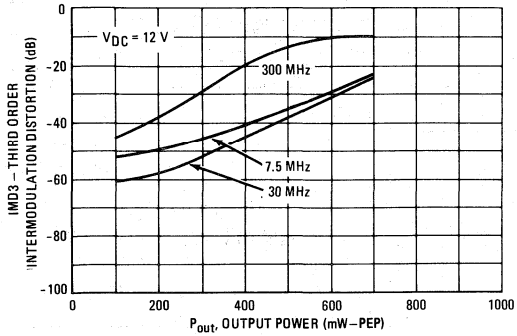


FIGURE 8 – INTERMODULATION DISTORTION – FIFTH ORDER versus OUTPUT POWER

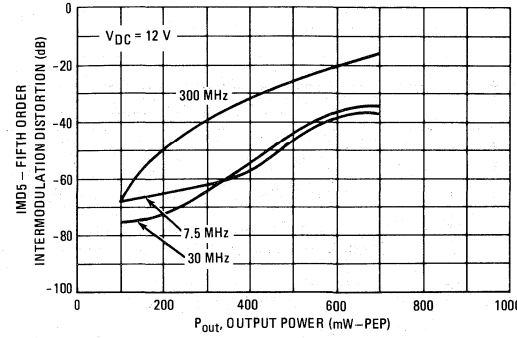


FIGURE 9 – INTERMODULATION DISTORTION – THIRD ORDER versus OUTPUT POWER

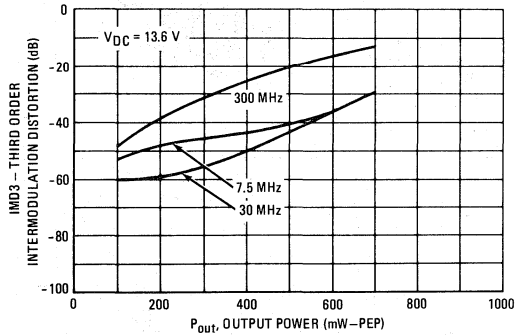


FIGURE 10 – INTERMODULATION DISTORTION – FIFTH ORDER versus OUTPUT POWER

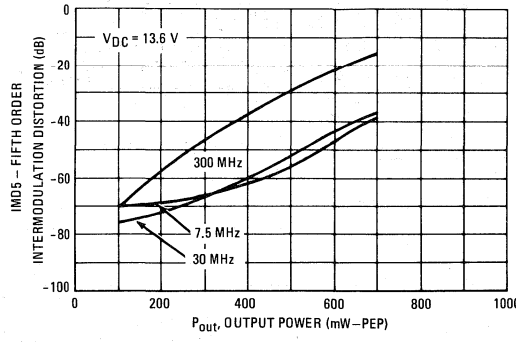
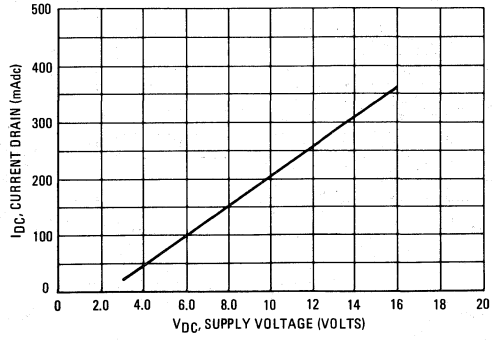


FIGURE 11 – DC CURRENT DRAIN versus SUPPLY VOLTAGE



MHW709-1
MHW709-2
MHW709-3

The RF Line

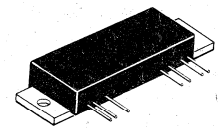
UHF POWER AMPLIFIER MODULE

. . . designed for 12.5 volt UHF power amplifier applications in industrial and commercial FM equipment operating from 400 to 512 MHz.

- Specified 12.5 Volt, UHF Characteristics —
  Output Power = 7.5 Watts
  Minimum Gain = 18.8 dB
  Harmonics = 40 dB
- 50 Ω Input/Output Impedance
- Guaranteed Stability and Ruggedness
- Gain Control Pin for Manual or Automatic Output Level Control
- Thin-Film Hybrid Construction Gives Consistent Performance and Reliability

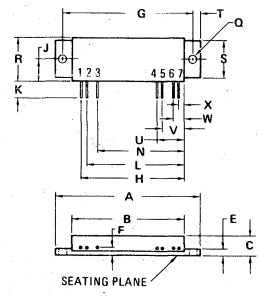
7.5 W — 400-512 MHz

RF POWER AMPLIFIER MODULE



MAXIMUM RATINGS (Flange Temperature = 25°C)

Rating	Symbol	Value	Unit
DC Supply Voltages	V_S, V_{SC}	15.5	Vdc
RF Input Power	P_{in}	250	mW
RF Output Power(@ $V_S = V_{SC} = 12.5$ V)	P_{out}	10	W
Operating Case Temperature Range	T_C	-30 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C



NOTE:
1. MOUNTING HOLES WITHIN 0.13 mm (0.005) DIA OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

STYLE 1:
PIN 1. RF OUTPUT
2. GROUND
3. D.C. TERMINAL
4. GROUND
5. D.C. GAIN
6. GROUND
7. RF INPUT

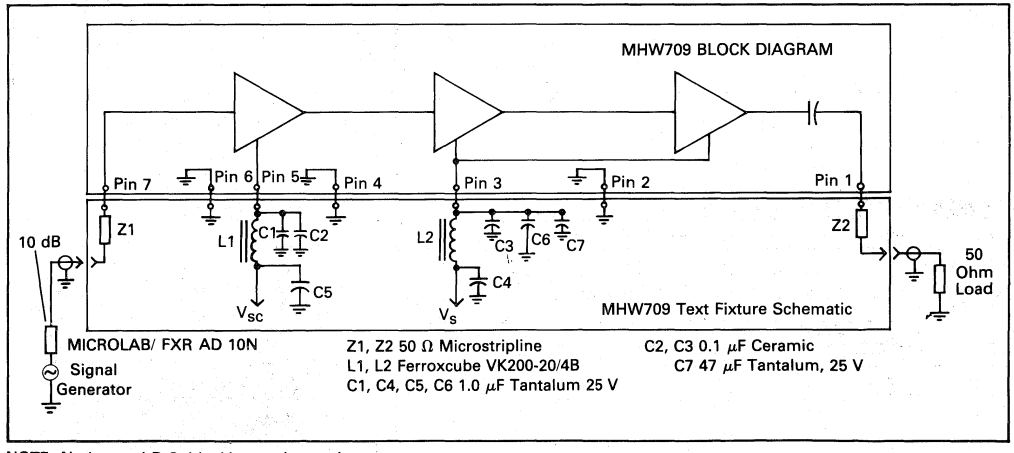
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	67.06	67.56	2.640	2.660
B	51.82	52.96	2.040	2.085
C	8.51	9.14	0.335	0.360
E	2.54	2.92	0.100	0.115
F	2.67	2.92	0.105	0.115
G	61.09 BSC		2.405 BSC	
H	47.88	48.64	1.885	1.915
J	10.16	11.18	0.400	0.440
K	5.84	7.62	0.230	0.300
L	45.34	46.10	1.785	1.815
N	40.26	41.02	1.585	1.615
Q	3.45	3.71	0.136	0.146
R	20.32	20.83	0.800	0.820
S	17.02	17.53	0.670	0.690
T	2.98	3.24	0.1175	0.1275
U	12.32	13.08	0.485	0.515
V	9.78	10.54	0.385	0.415
W	4.70	5.46	0.185	0.215
X	2.16	2.92	0.085	0.115

CASE 700-03

ELECTRICAL CHARACTERISTICS (V_S and V_{SC} set at 12.5 Vdc, T_A = 25°C, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Frequency Range MHW709-1 MHW709-2 MHW709-3	—	400 440 470	440 470 512	MHz
Input Power (P_{out} = 7.5 W)	P_{in}	—	100	mW
Power Gain	G_p	18.8	—	dB
Efficiency (P_{out} = 7.5 W)	η	35	—	%
Harmonics (P_{out} = 7.5 W, Reference)	—	—	−40	dB
Input Impedance (P_{out} = 7.5 W, 50 Ω Reference)	Z_{in}	—	2:1	VSWR
Power Degradation (P_{out} = 7.5 W, T_C = 25°C, Reference) (T_C = 0°C to 60°C) (T_C = −30°C to 80°C)	—	 — —	 0.3 0.7	dB
Load Mismatch (VSWR = ∞, V_S = V_{SC} = 15.5 Vdc, P_{out} = 10 W)	—	No degradation in P_{out}		
Stability 1. (P_{in} = 30 to 150 mW, Load Mismatch = 2:1, 50 Ω Reference, V_S = V_{SC} = 3.0 to 15.5 Vdc) 2. (V_S = 12.5 Vdc, V_{SC} adjusted for P_{out} = 5.0 to 10 W, P_{in} = 100 mW, Load Mismatch = 4:1, 50 Ω Reference, note $V_{SC} \leq V_S$)	—	All spurious outputs more than 70 dB below desired signal		
Standby Current (P_{in} = 0)	$I_{SC(Q)}$	—	10	mA

FIGURE 1 — UHF POWER MODULE TEST SETUP



NOTE: No Internal D.C. blocking on input pin.

TYPICAL PERFORMANCE CURVES

(MHW709-2)

FIGURE 2 – INPUT POWER, EFFICIENCY, AND VSWR versus FREQUENCY

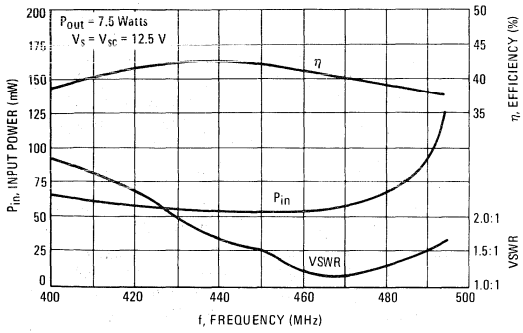


FIGURE 3 – OUTPUT POWER versus INPUT POWER

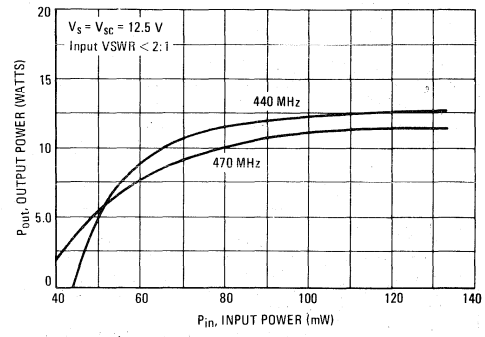


FIGURE 4 – OUTPUT POWER versus VOLTAGE

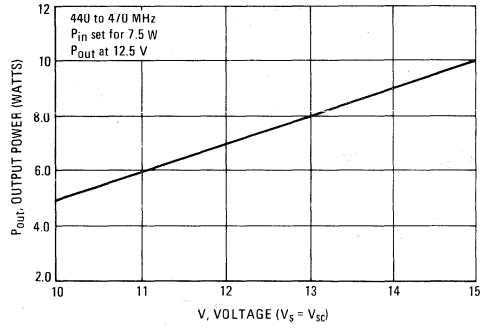


FIGURE 5 – OUTPUT POWER versus GAIN CONTROL VOLTAGE

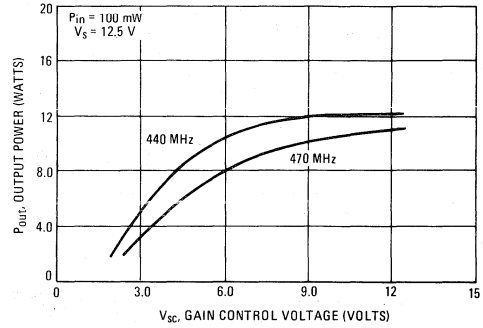


FIGURE 6 – GAIN CONTROL CURRENT versus VOLTAGE

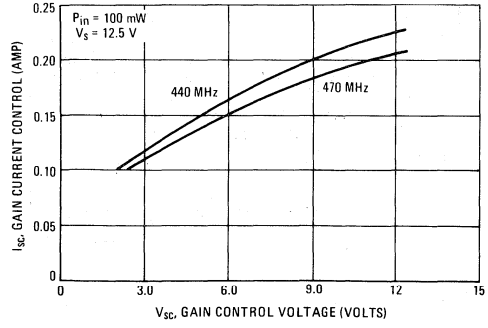
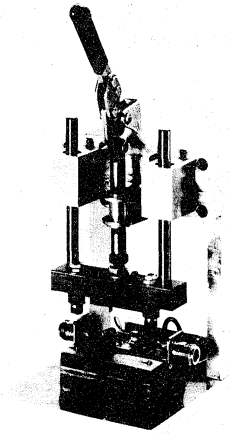


FIGURE 7 — TEST CIRCUIT



APPLICATIONS INFORMATION

Nominal Operation

All electrical specifications are based on the nominal conditions of V_{SC} (Pin 5) and V_S (Pin 3) equal to 12.5 Vdc and with output power equaling 7.5 watts. With these conditions, maximum current density on any device is 1.5×10^5 A/cm^2 and maximum die temperature with 100° base plate temperature is 165°. While the modules are designed to have excess gain margin with ruggedness, operation of these units outside the limits of published specifications is not recommended unless prior communications regarding intended use has been made with the factory representative.

Gain Control

The intent of these gain control methods is to set the nominal P_{out}. Do not use them for wide range gain control.

In general, the module output power should be limited to 10 watts. The preferred method of power output control is to fix both V_{SC} and V_S at 12.5 Vdc and vary the input RF drive level at Pin 7. The next method is to control V_{SC} through a stiff voltage source.

A third method of power output control is to control V_{SC} through a current source or voltage source with series resistance. This mode of control creates a region of negative slope on the power gain profile curve and aggravates output power slump with temperature.

Decoupling

Due to the high gain of the three stages and the module size limitation, external decoupling network requires careful consideration. Both Pins 3 and 5 are internally bypassed with a 0.018 μF chip capacitor effective for frequencies from 5 through 512 MHz. For bypassing frequencies below 5 MHz, networks equivalent to that shown in the test figure schematic are recommended. Inadequate decoupling will result in spurious outputs at certain operating frequencies and certain phase angles of input and output VSWR less than 3:1.

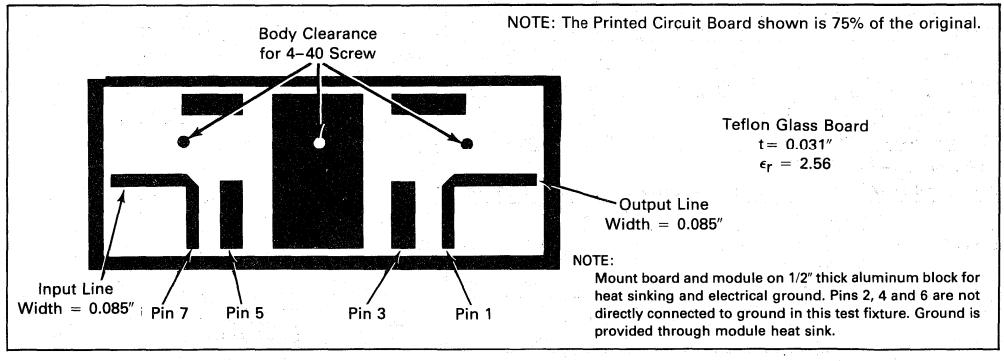
Load Pull

During final test, each module is "load pull" tested in a fixture having the identical decoupling network described in Figure 1. Electrical conditions are V_S and V_{SC} equal 15.5 V output, VSWR infinite, output power equal to 10 watts.

Mounting Considerations

To insure optimum heat transfer from the flange to heatsink, use standard 6–32 mounting screws and an adequate quantity of silicon thermal compound (e.g., Dow Corning 340). With both mounting screws finger tight, alternately torque down the screws to 4–6 inch pounds. The heatsink mounting surface directly beneath the module flange should be flat to within 0.005 inch to prevent fracturing of ceramic substrate material. For more information on module mounting, see EB-107.

FIGURE 8 — UHF POWER MODULE TEST FIXTURE PRINTED CIRCUIT BOARD



MHW710-1
MHW710-2
MHW710-3

The RF Line

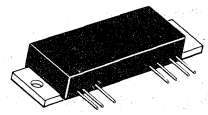
13 W 400–512 MHz

RF POWER
AMPLIFIER MODULE

UHF POWER AMPLIFIER MODULE

. . . designed for 12.5 volt UHF power amplifier applications in industrial and commercial FM equipment operating from 400 to 512 MHz.

- Specified 12.5 Volt, UHF Characteristics –
  Output Power = 13 Watts
  Minimum Gain = 19.4 dB
  Harmonics = 40 dB
- 50 Ω Input/Output Impedance
- Guaranteed Stability and Ruggedness
- Gain Control Pin for Manual or Automatic Output Level Control
- Thin Film Hybrid Construction Gives Consistent Performance and Reliability

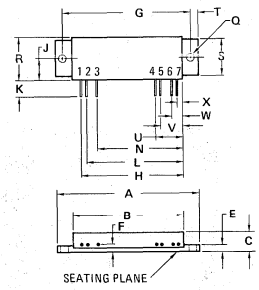


MAXIMUM RATINGS (Flange Temperature = 25°C)

Rating	Symbol	Value	Unit
DC Supply Voltages	V_s,V_{sc}	15.5	Vdc
RF Input Power	P_{in}	250	mW
RF Output Power (@ V_s = V_{sc} = 12.5 V)	P_{out}	15	W
Operating Case Temperature Range	T_C	−30 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS
(V_s and V_{sc} set at 12.5 Vdc, T_A = 25°C, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Frequency Range MHW710-1 MHW710-2 MHW710-3	—	400 440 470	440 470 512	MHz
Input Power (P_{out} = 13 W)	P_{in}	—	150	mW
Power Gain	G_p	19.4	—	dB
Efficiency (P_{out} = 13 W)	η	35	—	%
Harmonics (P_{out} = 13 W, Reference)	—	—	−40	dB
Input Impedance (P_{out} = 13 W, 50 Ω Reference)	Z_{in}	—	2:1	VSWR
Power Degradation (P_{out} = 13 W, T_C = 25°C, Reference) (T_C = 0°C to 60°C) (T_C = −30°C to 80°C)	—	 — —	 0.3 0.7	dB
Load Mismatch (VSWR = ∞, V_s = 15.5 Vdc, P_{out} = 16.5 W)	—	No degradation in P_{out}		
Stability 1. (P_{in} = 50 to 200 mW, Load Mismatch = 4:1, 50 Ω reference, V_s = V_{sc} = 8.0 to 15.5 Vdc) 2. (V_s = 12.5 Vdc, V_{sc} adjusted for P_{out} = 5.0 to 15 W, P_{in} = 150 mW, Load Mismatch = 4:1, 50 Ω reference, note $V_{sc} \leq V_s$)	—	All spurious outputs more than 70 dB below desired signal		



NOTE:
1. MOUNTING HOLES WITHIN 0.13 mm (0.005) DIA OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

STYLE 1:
PIN 1. RF OUTPUT
2. GROUND
3. D.C. TERMINAL
4. GROUND
5. D.C. GAIN
6. GROUND
7. RF INPUT

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	67.06	67.56	2.640	2.660
B	51.82	52.96	2.040	2.085
C	8.51	9.14	0.335	0.360
E	2.54	2.92	0.100	0.115
F	2.67	2.92	0.105	0.115
G	61.09 BSC		2.405 BSC	
H	47.88	48.64	1.885	1.915
J	10.16	11.18	0.400	0.440
K	5.84	7.62	0.230	0.300
L	45.34	46.10	1.785	1.815
N	40.26	41.02	1.585	1.615
Q	3.45	3.71	0.136	0.146
R	20.32	20.83	0.800	0.820
S	17.02	17.53	0.670	0.690
T	2.98	3.24	0.1175	0.1275
U	12.32	13.08	0.485	0.515
V	9.78	10.54	0.385	0.415
W	4.70	5.46	0.185	0.215
X	2.16	2.92	0.085	0.115

CASE 709-03

APPLICATIONS INFORMATION

Nominal Operation

All electrical specifications are based on the nominal conditions of V_{sc} (Pin 5) and V_s (Pin 3) equal to 12.5 Vdc and with output power equaling 13 watts. With these conditions, maximum current density on any device is 1.5×10^5 A/cm^2 and maximum die temperature with 100° base plate temperature is 165°. While the modules are designed to have excess gain margin with ruggedness, operation of these units outside the limits of published specifications is not recommended unless prior communications regarding intended use has been made with the factory representative.

Gain Control

The intent of these gain control methods is to set the nominal P_{out}. Do not use them for wide range gain control.

In general, the module output power should be limited to 10 watts. The preferred method of power output control is to fix both V_{sc} and V_s at 12.5 Vdc and vary the input RF drive level at Pin 7. The next method is to control V_{sc} through a stiff voltage source.

A third method of power output control is to control V_{sc} through a current source or voltage source with series resistance. This mode of control creates a region of negative slope on the power gain profile curve and aggravates output power slump with temperature.

Decoupling

Due to the high gain of the three stages and the module size limitation, external decoupling network requires careful consideration. Both Pins 3 and 5 are internally bypassed with a 0.018 μF chip capacitor effective for frequencies from 5 through 512 MHz. For bypassing frequencies below 5 MHz, networks equivalent to that shown in the test figure schematic are recommended. Inadequate decoupling will result in spurious outputs at certain operating frequencies and certain phase angles of input and output VSWR less than 3:1.

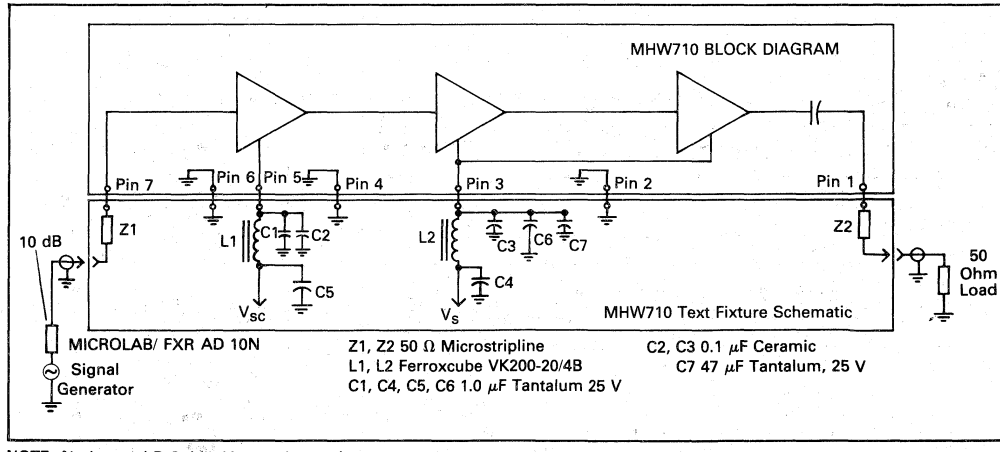
Load Pull

During final test, each module is "load pull" tested in a fixture having the identical decoupling network described in Figure 1. Electrical conditions are V_s and V_{sc} equal 15.5 V output, VSWR infinite, output power equal to 16.5 watts.

Mounting Considerations

To insure optimum heat transfer from the flange to heatsink, use standard 6–32 mounting screws and an adequate quantity of silicon thermal compound (e.g., Dow Corning 340). With both mounting screws finger tight, alternately torque down the screws to 4–6 inch pounds. The heatsink mounting surface directly beneath the module flange should be flat to within 0.005 inch to prevent fracturing of ceramic substrate material. For more information on module mounting, see EB-107.

FIGURE 1 — UHF POWER MODULE TEST SETUP



NOTE: No Internal D.C. blocking on input pin.

TYPICAL PERFORMANCE CURVES
(MHW710-2)

FIGURE 2 – INPUT POWER, EFFICIENCY, AND VSWR versus FREQUENCY

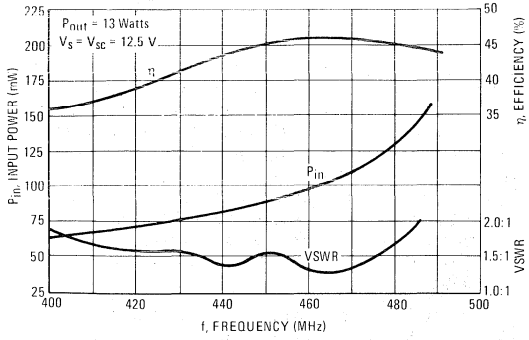


FIGURE 3 – OUTPUT POWER versus INPUT POWER

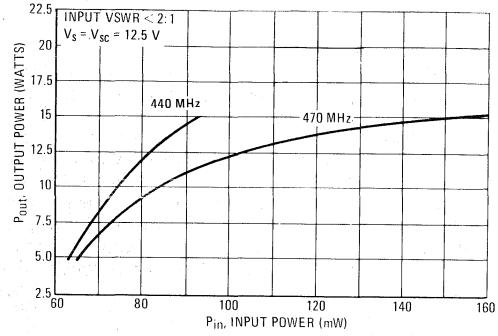


FIGURE 4 – OUTPUT POWER versus VOLTAGE

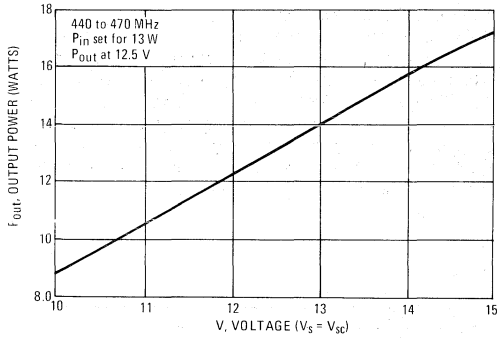


FIGURE 5 – OUTPUT POWER versus GAIN CONTROL VOLTAGE

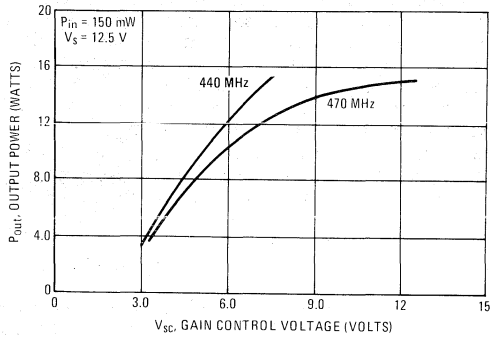


FIGURE 6 – GAIN CONTROL CURRENT versus VOLTAGE

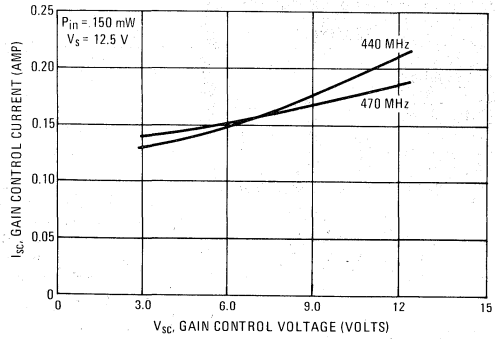


FIGURE 7 — TEST CIRCUIT

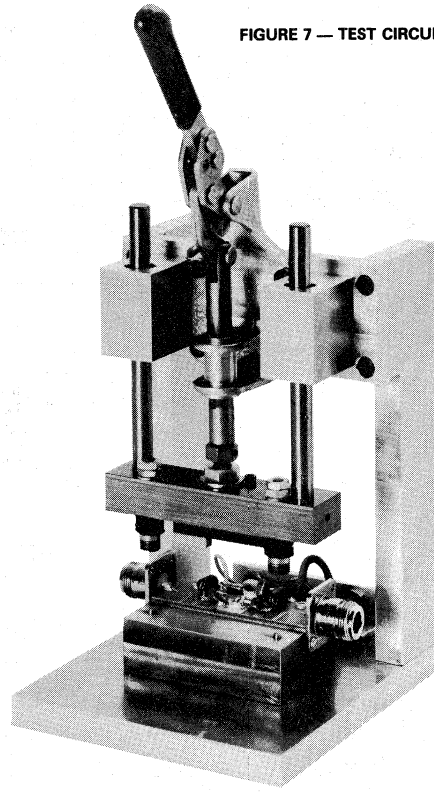
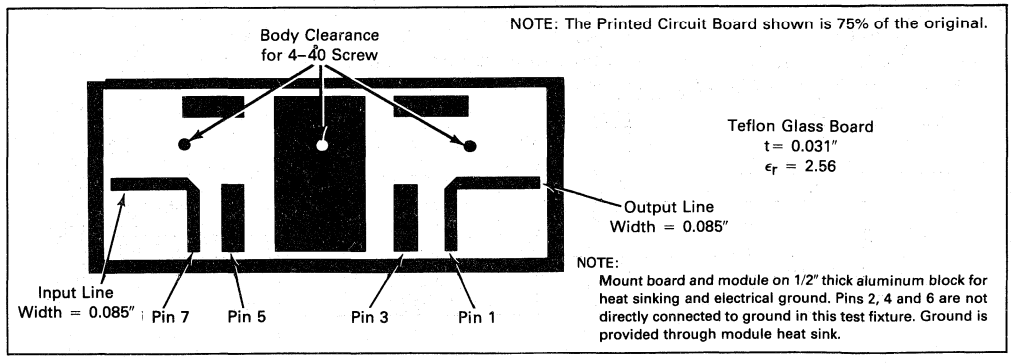


FIGURE 8 — UHF POWER MODULE TEST FIXTURE
PRINTED CIRCUIT BOARD



MHW720-1
MHW720-2

The RF Line

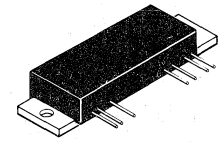
20 W 400–470 MHz

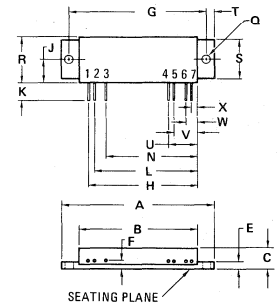
RF POWER AMPLIFIER MODULES

UHF POWER AMPLIFIER MODULES

. . . designed for 12.5 volt UHF power amplifier applications in industrial and commercial FM equipment operating from 400 to 470 MHz.

- Specified 12.5 Volt, UHF Characteristics –
  Output Power = 20 Watts
  Minimum Gain = 21 dB
  Harmonics = 40 dB
- 50 Ω Input/Output Impedance
- Guaranteed Stability and Ruggedness
- Gain Control Pin for Manual or Automatic Output Level Control
- Thin Film Hybrid Construction Gives Consistent Performance and Reliability





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	67.06	67.56	2.640	2.660
B	51.82	52.96	2.040	2.085
C	8.51	9.14	0.335	0.360
E	2.54	2.92	0.100	0.115
F	2.67	2.92	0.105	0.115
G	61.09 BSC		2.405 BSC	
H	47.88	48.64	1.885	1.915
J	10.16	11.18	0.400	0.440
K	5.84	7.62	0.230	0.300
L	45.34	46.10	1.785	1.815
N	40.26	41.02	1.585	1.615
Q	3.45	3.71	0.136	0.146
R	20.32	20.83	0.800	0.820
S	17.02	17.53	0.670	0.690
T	2.98	3.24	0.1175	0.1275
U	12.32	13.08	0.485	0.515
V	9.78	10.54	0.385	0.415
W	4.70	5.46	0.185	0.215
X	2.16	2.92	0.085	0.115

NOTE:
1. MOUNTING HOLES WITHIN 0.13 mm (0.005) DIA OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

STYLE 1:
PIN 1. RF OUTPUT
2. GROUND
3. D.C. TERMINAL
4. GROUND
5. D.C. GAIN
6. GROUND
7. RF INPUT

CASE 700-03

MAXIMUM RATINGS (Flange Temperature = 25°C)

Rating	Symbol	Value	Unit
DC Supply Voltages	V_s,V_{sc}	15.5	Vdc
RF Input Power	P_{in}	250	mW
RF Output Power (@ V_s = V_{sc} = 12.5 V)	P_{out}	25	W
Operating Case Temperature Range	T_C	−30 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS
(V_s and V_{sc} set at 12.5 Vdc, T_A = 25°C, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Frequency Range MHW720-1 MHW720-2	—	400 440	440 470	MHz
Input Power (P_{out} = 20 W)	P_{in}	—	150	mW
Power Gain	G_p	21	—	dB
Efficiency (P_{out} = 20 W)	η	35	—	%
Harmonics (P_{out} = 20 W, Reference)	—	—	−40	dB
Input Impedance (P_{out} = 20 W, 50 Ω Reference)	Z_{in}	—	2:1	VSWR
Power Degradation (P_{out} = 20 W, T_C = 25°C, Reference) (T_C = 0°C to 60°C) (T_C = −30°C to 80°C)	—	 — —	 0.3 0.7	dB
Load Mismatch (VSWR = ∞, V_s = 15.5 Vdc, P_{out} = 30 W)	—	No degradation in P_{out}		
Stability 1. (P_{in} = 50 to 200 mW, Load Mismatch = 2:1, 50 Ω reference, V_s = V_{sc} = 8.0 to 15.5 Vdc) 2. (V_s = 12.5 Vdc, V_{sc} adjusted for P_{out} = 5.0 to 20 W, P_{in} = 150 mW, Load Mismatch = 2:1, 50 Ω reference, note $V_{sc} \leq V_s$)	—	All spurious outputs more than 70 dB below desired signal		

4

APPLICATIONS INFORMATION

Nominal Operation

All electrical specifications are based on the nominal conditions of V_{SC} (Pin 5) and V_S (Pin 3) equal to 12.5 Vdc and with output power equaling 20 watts. With these conditions, maximum current density on any device is 1.5×10^5 A/cm^2 and maximum die temperature with 100° base plate temperature is 165°. While the modules are designed to have excess gain margin with ruggedness, operation of these units outside the limits of published specifications is not recommended unless prior communications regarding intended use has been made with the factory representative.

Gain Control

The intent of these gain control methods is to set the nominal P_{out}. Do not use them for wide range gain control.

In general, the module output power should be limited to 20 watts. The preferred method of power output control is to fix both V_{SC} and V_S at 12.5 Vdc and vary the input RF drive level at Pin 7. The next method is to control V_{SC} through a stiff voltage source.

A third method of power output control is to control V_{SC} through a current source or voltage source with series resistance. This mode of control creates a region of negative slope on the power gain profile curve and aggravates output power slump with temperature.

Decoupling

Due to the high gain of the three stages and the module size limitation, external decoupling network requires careful consideration. Both Pins 3 and 5 are internally bypassed with a 0.018 μF chip capacitor effective for frequencies from 5 through 512 MHz. For bypassing frequencies below 5 MHz, networks equivalent to that shown in the test figure schematic are recommended. Inadequate decoupling will result in spurious outputs at certain operating frequencies and certain phase angles of input and output VSWR less than 3:1.

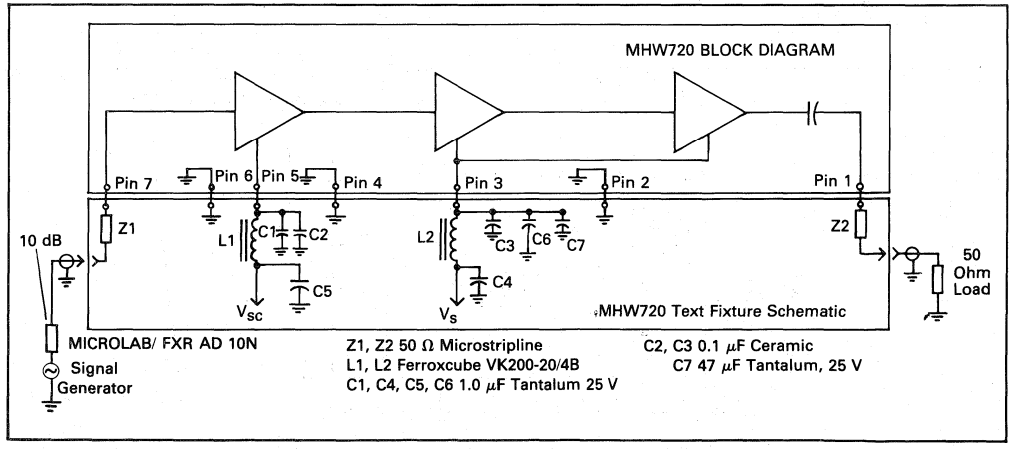
Load Pull

During final test, each module is "load pull" tested in a fixture having the identical decoupling network described in Figure 1. Electrical conditions are V_S and V_{SC} equal 15.5 V output, VSWR infinite, output power equal to 30 watts.

Mounting Considerations

To insure optimum heat transfer from the flange to heatsink, use standard 6–32 mounting screws and an adequate quantity of silicon thermal compound (e.g., Dow Corning 340). With both mounting screws finger tight, alternately torque down the screws to 4–6 inch pounds. The heatsink mounting surface directly beneath the module flange should be flat to within 0.005 inch to prevent fracturing of ceramic substrate material. For more information on module mounting, see EB-107.

FIGURE 1 — UHF POWER MODULE TEST SETUP



NOTE: No Internal D.C. blocking on input pin.

TYPICAL PERFORMANCE CURVES
(MHW720-2)

FIGURE 2 – INPUT POWER, EFFICIENCY, AND VSWR versus FREQUENCY

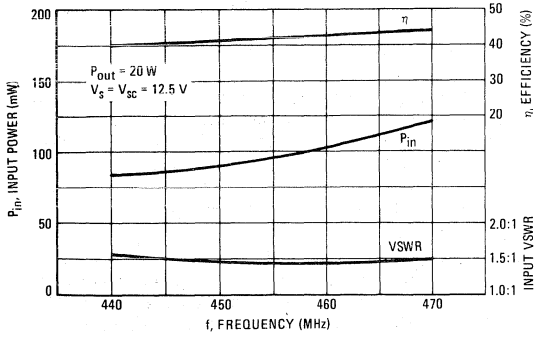


FIGURE 3 – OUTPUT POWER versus INPUT POWER

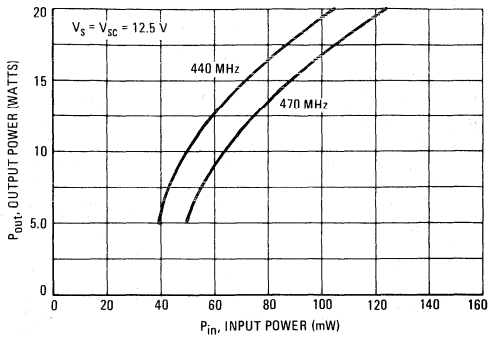


FIGURE 4 – OUTPUT POWER versus VOLTAGE

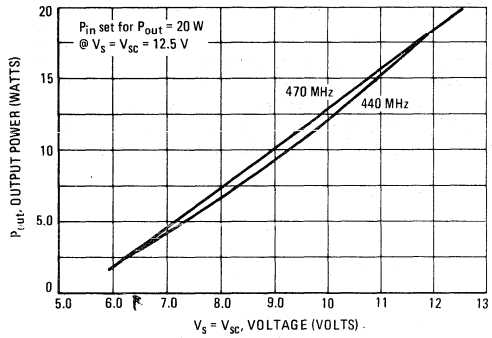


FIGURE 5 – OUTPUT POWER versus GAIN CONTROL VOLTAGE

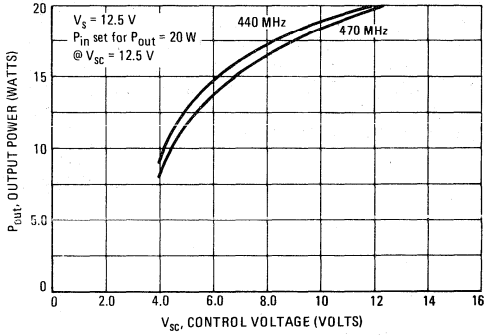


FIGURE 6 – GAIN CONTROL CURRENT versus VOLTAGE

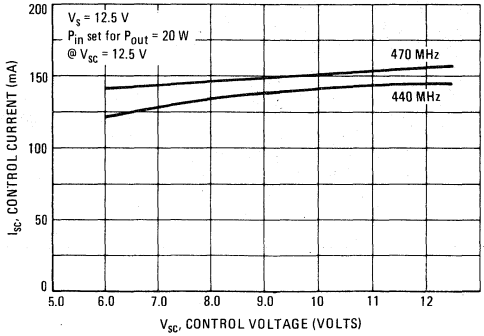


FIGURE 7 — TEST CIRCUIT

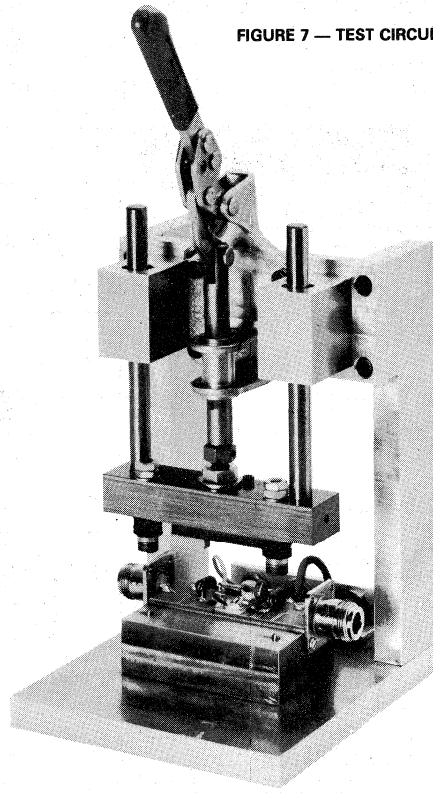
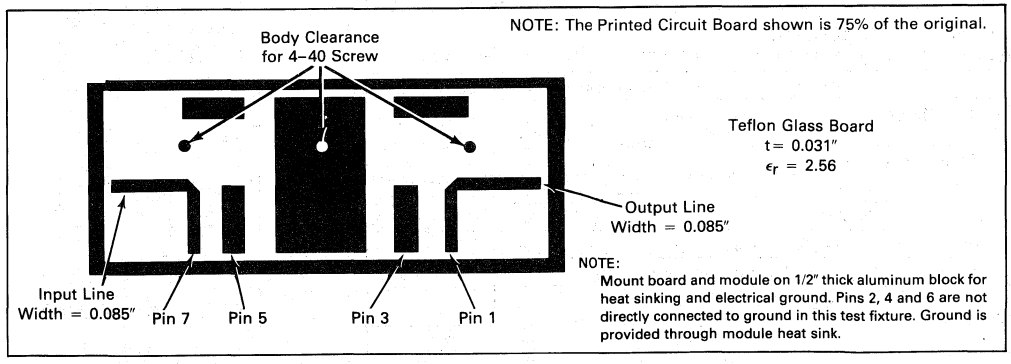


FIGURE 8 — UHF POWER MODULE TEST FIXTURE
PRINTED CIRCUIT BOARD



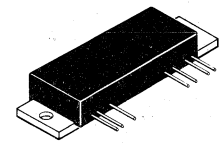
MHW720A1
MHW720A2

Designers Data Sheet

The RF Line

20 W 400–470 MHz

RF POWER AMPLIFIER MODULES



UHF POWER AMPLIFIER MODULES

. . . capable of wide power range control as encountered in UHF cellular telephone applications.

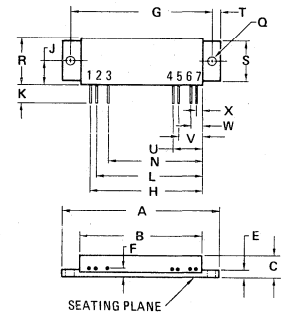
- MHW720A1 400–440 MHz
- MHW720A2 440–470 MHz
- Specified 12.5 Volt, UHF Characteristics —
  Output Power = 20 Watts
  Minimum Gain = 21 dB
  Harmonics = −40 dB (Max)
- 50 Ω Input/Output Impedance
- Guaranteed Stability and Ruggedness
- Thin Film Hybrid Construction Gives Consistent Performance and Reliability

MAXIMUM RATINGS (Flange Temperature = 25°C)

Rating	Symbol	Value	Unit
DC Supply Voltages	V_{s1}, V_{s2}	15.5	Vdc
RF Input Power	P_{in}	250	mW
RF Output Power (@ V_{s1} = V_{s2} = 12.5 V)	P_{out}	25	W
Operating Case Temperature Range	T_C	−30 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS
(V_{s1} and V_{s2} set at 12.5 Vdc, T_C = 25°C, 50 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Frequency Range	MHW720A1 MHW720A2	—	400 440	440 470	MHz
Input Power (P_{out} = 20 W)		P_{in}	—	150	mW
Power Gain (P_{out} = 20 W)		G_p	21	—	dB
Efficiency (P_{out} = 20 W)		η	35	—	%
Harmonics (P_{out} = 20 W, Reference)		—	—	−40	dB
Input Impedance (P_{out} = 20 W, 50 Ω Reference)		Z_{in}	—	2:1	VSWR
Gain Degradation (2) (P_{out} = 20 W, Reference Gain @ T_C = + 25°C)	T_C = −30°C T_C = + 80°C	—	— —	−0.7 −0.7	dB
Load Mismatch (VSWR = ∞, V_{s1} = V_{s2} = 15.5 Vdc, P_{out} = 30 W)		—	No degradation in P_{out}		
Stability (P_{in} = 0 to 250 mW, V_{s1} = V_{s2} = 10 to 15.5 Vdc) 1. Load VSWR = 4:1, 50 Ω Reference 2. Source VSWR = 2:1, 50 Ω Reference		—	All spurious outputs more than 60 dB below desired signal		
Quiescent Current (I_{s1} No RF Drive Applied)		I_{s1} (q)	—	200	mA
(2) See Figure 5, Input Power versus Case Temperature					



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	67.06	67.56	2.640	2.660
B	51.82	52.96	2.040	2.085
C	8.51	9.14	0.335	0.360
E	2.54	2.92	0.100	0.115
F	2.67	2.92	0.105	0.115
G	61.09 BSC		2.405 BSC	
H	47.88	48.64	1.885	1.915
J	10.16	11.18	0.400	0.440
K	5.84	7.62	0.230	0.300
L	45.34	46.10	1.785	1.815
N	40.26	41.02	1.585	1.615
Q	3.45	3.71	0.136	0.146
R	20.32	20.83	0.800	0.820
S	17.02	17.53	0.670	0.690
T	2.98	3.24	0.1175	0.1275
U	12.32	13.08	0.485	0.515
V	9.78	10.54	0.385	0.415
W	4.70	5.46	0.185	0.215
X	2.16	2.92	0.085	0.115

NOTE:
1. MOUNTING HOLES WITHIN 0.13 mm (0.005) DIA OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

STYLE 2:
PIN 1. RF OUTPUT
2. GROUND
3. VS2
4. GROUND
5. VS1
6. GROUND
7. RF INPUT

CASE 700-03

APPLICATIONS INFORMATION

Nominal Operation

All electrical specifications are based on the nominal conditions of V_{S1} (Pin 5) and V_{S2} (Pin 3) equal to 12.5 Vdc and with output power equaling 20 watts. With these conditions, maximum current density on any device is 1.5×10^5 A/cm^2 and maximum die temperature with 100° base plate temperature is 165°. While the modules are designed to have excess gain margin with ruggedness, operation of these units outside the limits of published specifications is not recommended unless prior communications regarding intended use has been made with the factory representative.

Gain Control

This module is designed for wide range P_{out} level control. The recommended method of power output control, as shown in Figure 3, is to fix V_{S1} and V_{S2} at 12.5 Vdc and vary the input RF drive level at Pin 7.

In all applications, the module output power should be limited to 20 watts.

Decoupling

Due to the high gain of the three stages and the module size limitation, the external decoupling network requires careful consideration. Both Pins 3 and 5 are internally bypassed with a 0.018 μF chip capacitor effective for frequencies from 5 through 470 MHz. For bypassing frequencies below 5 MHz, networks equivalent to that shown in the test fixture schematic are recommended. Inadequate decoupling will result in spurious outputs at certain operating frequencies and certain phase angles of input and output VSWR less than 4:1.

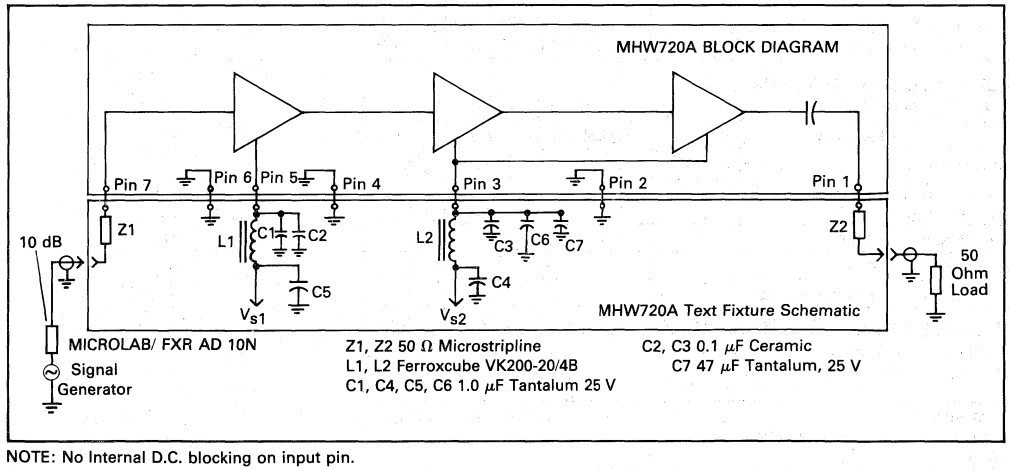
Load Mismatch

During final test, each module is load mismatch tested in a fixture having the identical decoupling network described in Figure 1. Electrical conditions are V_{S1} and V_{S2} equal 15.5 V, load VSWR infinite, and output power equal to 30 watts.

Mounting Considerations

To insure optimum heat transfer from the flange to heatsink, use standard 6–32 mounting screws and an adequate quantity of silicon thermal compound (e.g., Dow Corning 340). With both mounting screws finger tight, alternately torque down the screws to 4–6 inch pounds. The heatsink mounting surface directly beneath the module flange should be flat to within 0.005 inch to prevent fracturing of ceramic substrate material. For more information on module mounting, see EB-107.

FIGURE 1 — UHF POWER MODULE TEST SETUP



NOTE: No Internal D.C. blocking on input pin.

FIGURE 2 — INPUT POWER, EFFICIENCY, AND VSWR versus FREQUENCY

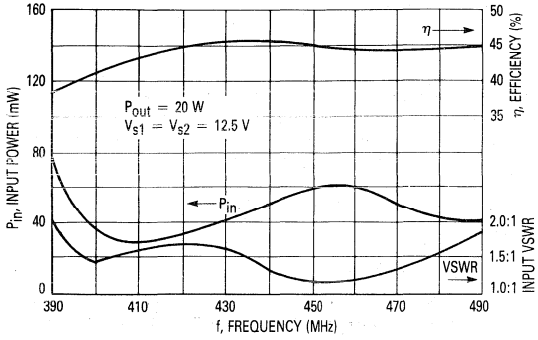


FIGURE 3 — OUTPUT POWER versus INPUT POWER

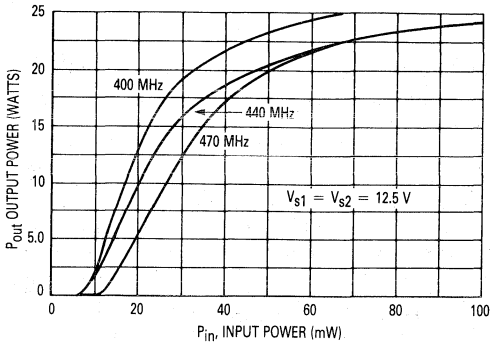


FIGURE 4 — OUTPUT POWER versus VOLTAGE

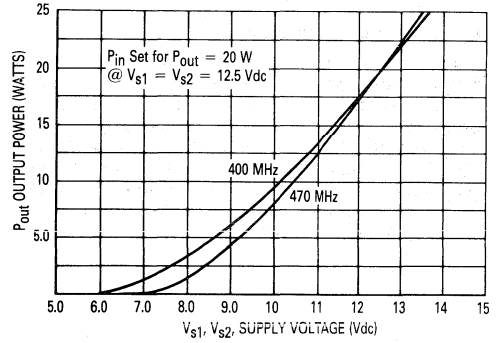


FIGURE 5 — INPUT POWER versus CASE TEMPERATURE

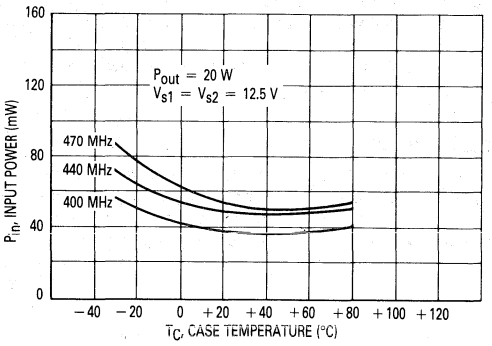


FIGURE 6 — OUTPUT POWER versus CASE TEMPERATURE @ 10.8 V SUPPLY

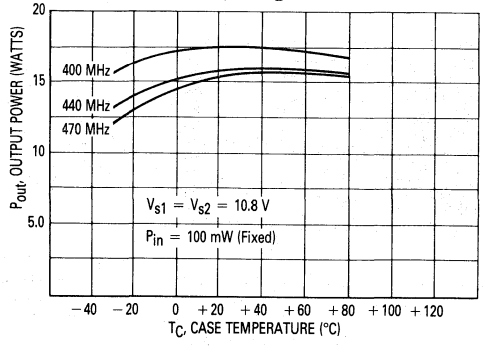


FIGURE 7 — TEST CIRCUIT

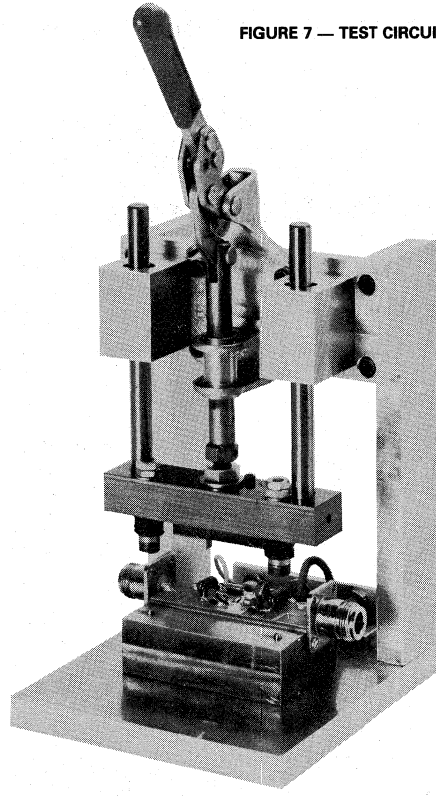
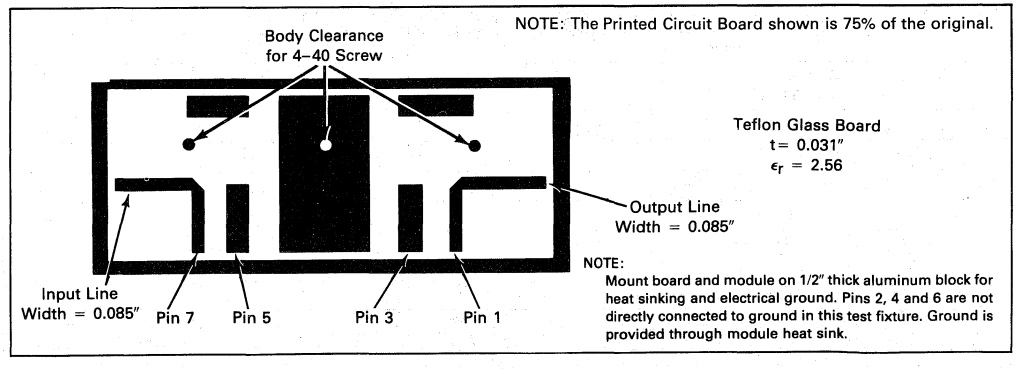


FIGURE 8 — UHF POWER MODULE TEST FIXTURE
PRINTED CIRCUIT BOARD



4

MHW802-1
MHW802-2

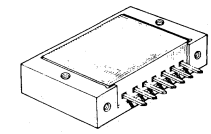
2.2 W — 825–915 MHz
RF POWER
AMPLIFIER MODULE

The RF Line

UHF Power Amplifier Modules

. . . capable of wide power range control as encountered in portable cellular radio applications (20 dB typical).

- MHW802-1 825–845 MHz
- MHW802-2 890–915 MHz
- Specified 9.5 Volt Characteristics
  - Output Power = 2.2 Watts
  - Minimum Gain ($V_{Control}$ = 9 V) = 20.4 dB
  - Harmonics = −25 dB (Max 2 fo)
- 50 Ω Input/Output Impedance
- Guaranteed Stability and Ruggedness
- Thin Film Hybrid Construction Gives Consistent Performance and Reliability



CASE 784-01

MAXIMUM RATINGS (Flange Temperature = 25°C)

Rating	Symbol	Value	Unit
DC Supply Voltage (Pins 3,4,5)	V_{CC}, V_T	12.5	Vdc
DC Control Voltage (Pin 2)	V_{cont}	9	Vdc
RF Input Power	P_{in}	50	mW
RF Output Power (V_{CC} = V_T = 12.5 V)	P_{out}	3	W
Operating Case Temperature Range	T_C	−30 to +100	°C
Storage Temperature Range	T_{stg}	−65 to +125	°C

4

ELECTRICAL CHARACTERISTICS (V_{CC} (Pins 3,5) = 9.5 V, V_T (Pin 4) = 9 V, T_C = 25°C, 50 Ω System

Characteristic	Symbol	Min	Max	Unit
Frequency Range MHW802-1 MHW802-2	—	825 890	845 915	MHz
Control Voltage (P_{out} = 2.2 W, P_{in} = 20 mW)(1)	V_{cont}	0.5	9	Vdc
Trickle Current (V_T, Pin 4 = 9 Vdc)	I_T	—	60	mA
Power Gain (P_{out} = 2.2 W, V_{cont} = 9 Vdc)	G_p	20.4	—	dB
Efficiency (P_{out} = 2.2 W, P_{in} = 20 mW)(1)	η	35	—	%
Harmonics (P_{out} = 2.2 W)(1) 2 fo (P_{in} = 20 mW) 3 fo	—	— —	−25 −35	dB
Input VSWR (P_{out} = 2.2 W, P_{in} = 20 mW), 50 Ω Ref. (1)	—	—	1.67:1	—
Noise power 30 kHz Bandwidth, 45 MHz, above fo (P_{out} = 2.2 W(1) T_C = +25°C (P_{in} = 20 mW) T_C = +100°C	— —	— —	−88 −85	dBm dBm
Load Mismatch (V_{CC} Pins 3,5 = V_T Pin 4 = 12.5 Vdc, VSWR = 3:1, P_{out} = 3 W, P_{in} = 50 mW)(1)		No Degradation in Power Output		
Stability (P_{in} = 20 mW, V_{CC} = V_T = 7.9 Vdc to 9.5 Vdc, P_{out} between 20 mW and 2.2 W(1) Load VSWR = 3:1, Source VSWR = 3:1)		All spurious outputs more than 60 dB below desired signal		

(1) Adjust V_{cont} for specified P_{out}.

TYPICAL PERFORMANCE CURVES

MHW802-1

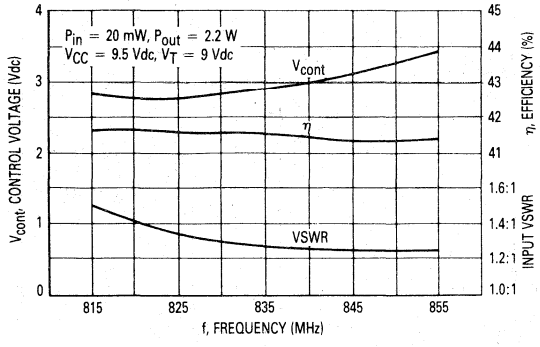


Figure 1. Control Voltage, Efficiency, and VSWR versus Frequency

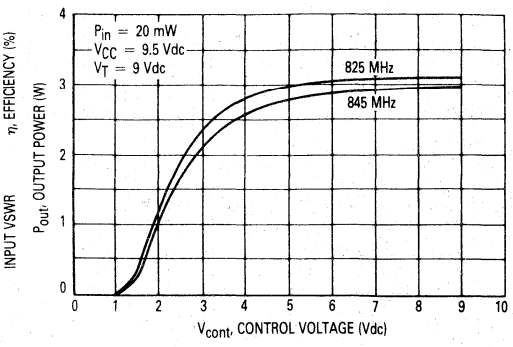


Figure 2. Output Power versus Control Voltage

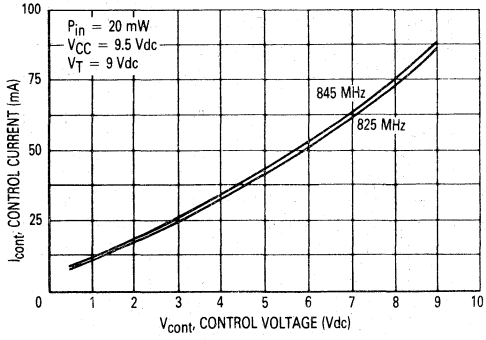


Figure 3. Control Current versus Control Voltage

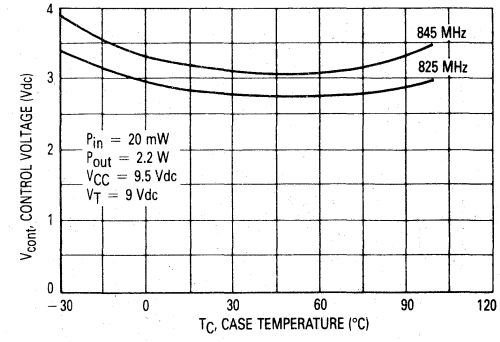


Figure 4. Control Voltage versus Case Temperature

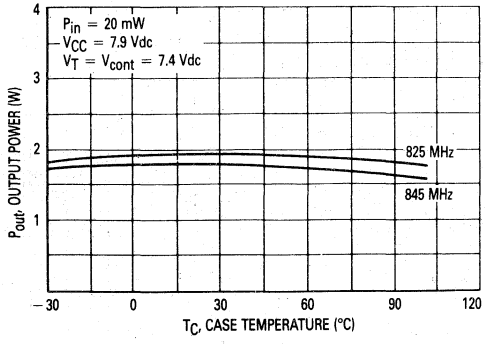


Figure 5. Output Power versus Case Temperature

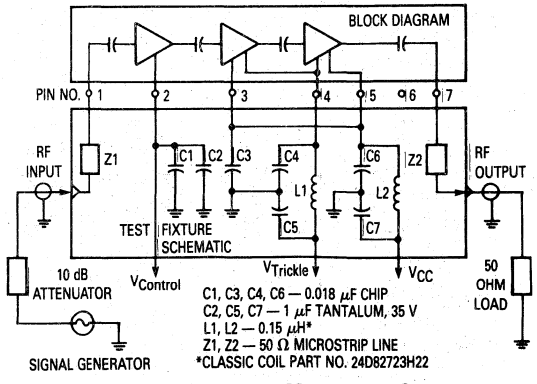


Figure 6. UHF Power Module Test Setup

MHW802-2

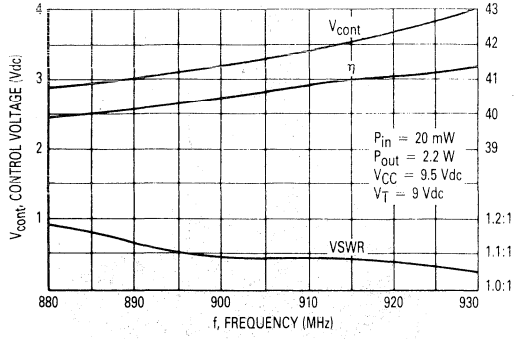


Figure 7. Control Voltage, Efficiency, and VSWR versus Frequency

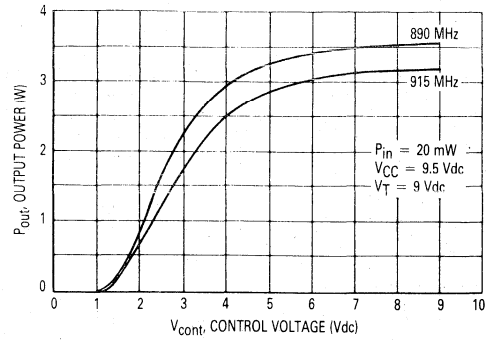


Figure 8. Output Power versus Control Voltage

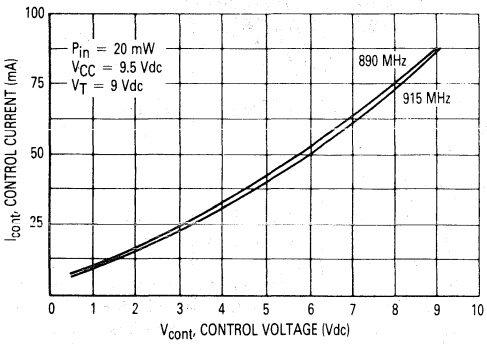


Figure 9. Control Current versus Control Voltage

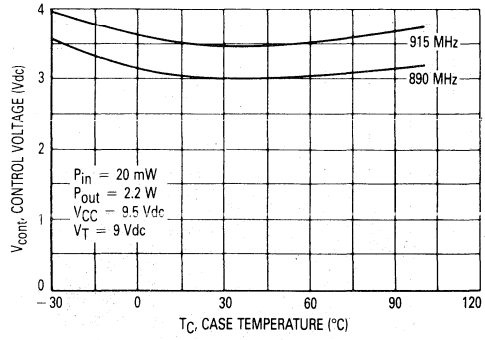
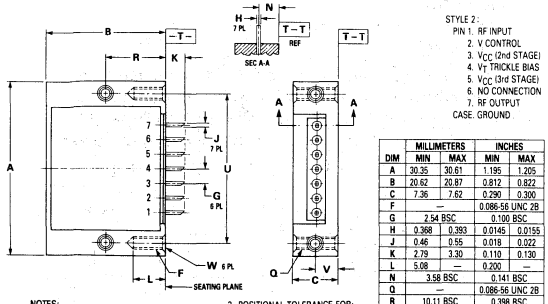


Figure 10. Control Voltage versus Case Temperature



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	30.35	30.61	1.195	1.205
B	20.62	20.87	0.812	0.822
C	7.36	7.62	0.290	0.300
F	—		0.086-56 UNC 2B	
G	2.54 BSC		0.100 BSC	
H	0.368	0.393	0.0145	0.0155
J	0.46	0.55	0.018	0.022
K	2.79	3.30	0.110	0.130
L	5.08	—	0.200	—
N	3.58 BSC		0.141 BSC	
Q	—		0.086-56 UNC 2B	
R	10.11 BSC		0.398 BSC	
U	26.16 BSC		1.030 BSC	
V	3.81 BSC		0.150 BSC	
W	82° x 2.54 ϕ		Cham. 82° x 100 ϕ	

NOTES:
1. DIMENSION A IS A DATUM. T AND T-T ARE BOTH DATUM PLANES.
2. POSITIONAL TOLERANCE FOR:
F HOLES
ϕ 0.036 (0.014) M T T-T A M
Q HOLES
ϕ 0.036 (0.014) M T-T T A M
3. POSITIONAL TOLERANCE FOR:
LEADS, J DIM (7 PL)
ϕ 0.13 (0.005) M T A M
LEADS, H DIM (7 PL)
ϕ 0.13 (0.005) M T T-T
4. DIMENSIONING AND TOLERANCING PER Y14.5, 1982.
5. CONTROLLING DIM: INCH

CASE 784-01

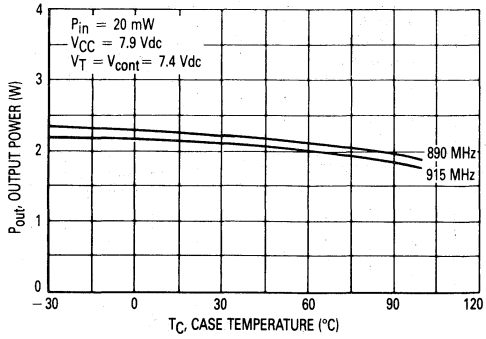


Figure 11. Output Power versus Case Temperature

APPLICATIONS INFORMATION

NOMINAL OPERATION

All electrical specifications are based on the nominal conditions of V_{CC} (Pins 3 and 5) equal to 9.5 Vdc, V_T (Pin 4) equal to 9 Vdc, and P_{out} equal to 2.2 watts. With these conditions, maximum current density on any device is 1.5×10^5 A/cm^2 and maximum die temperature with 100°C case operating temperature is 165°C. While the modules are designed to have excess gain margin with ruggedness, operation of these units outside the limits of published specifications is not recommended unless prior communication regarding intended use has been made with the factory representative.

GAIN CONTROL

The module output should be limited to 2.2 watts. The preferred method of power output control is to fix V_{CC} (Pins 3 and 5) at 9.5 Vdc, V_T (Pin 4) at 9 Vdc, P_{in} (Pin 1) at 20 mW, and vary V_{cont} (Pin 2) voltage.

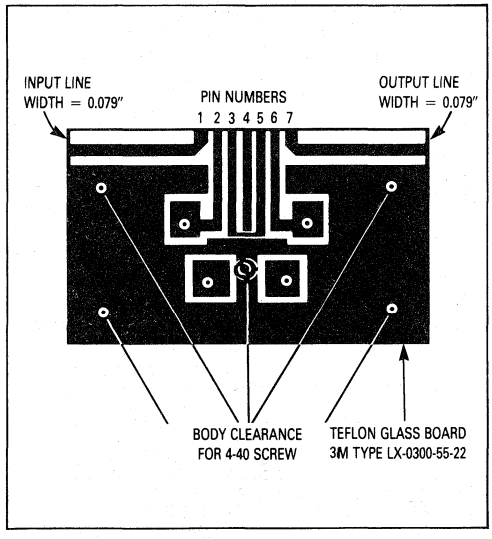


Figure 13. UHF Printed Circuit Board

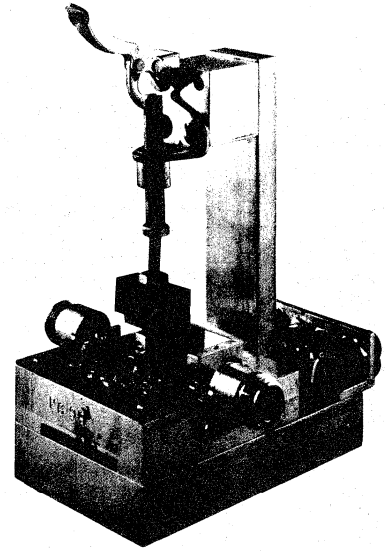


Figure 12. Test Fixture Assembly

DECOUPLING

Due to the high gain of the three stages and the module size limitation, external decoupling networks require careful consideration. Pins 2, 3 and 5 are internally bypassed with a 0.018 μF chip capacitor which is effective for frequencies from 5 MHz through 915 MHz. For bypassing frequencies below 5 MHz, networks equivalent to that shown in Figure 6 are recommended. Inadequate decoupling will result in spurious outputs at certain operating frequencies and certain phase angles of input and output VSWR.

LOAD MISMATCH

During final test, each module is load mismatch tested in a fixture having the identical decoupling networks described in Figure 6. Electrical conditions are V_{CC} and V_T equal to 12.5 Vdc, VSWR equal to 3:1, and output power equal to 3 watts.

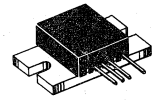
4

MHW806-1
MHW806-2
MHW806-3
MHW806-4

The RF Line

6.0 W — 806–960 MHz

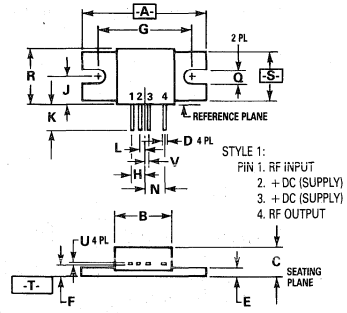
RF POWER AMPLIFIER MODULE



UHF POWER AMPLIFIER MODULE

. . . designed for 12.5 volt UHF power amplifier applications in industrial and commercial FM equipment operating from 806 to 960 MHz.

- MHW806-1 820–850 MHz
  MHW806-2 806–870 MHz
  MHW806-3 890–915 MHz
  MHW806-4 870–960 MHz
- Specified 12.5 Volt, UHF Characteristics
  Output Power = 6 Watts
  Minimum Gain = 13.8 dB (MHW806-1,2)
  = 12.3 dB (MHW806-3,4)
  Harmonics = −45 dBc Max
- 50 Ω Input/Output Impedances
- Guaranteed Stability and Ruggedness
- Features Two Common-Emitter Gain Stages
- Thin-Film Hybrid Construction Gives Consistent Performance and Reliability
- Gold-Metallized and Silicon Nitride-Passivated Transistor Chips
- Controllable, Stable Performance Over More Than 30 dB Range in Output Power



NOTES:
1. DIMENSIONS A AND S ARE DATUMS.
2. -T- IS A DATUM AND SEATING PLANE.
3. POSITIONAL TOLERANCE FOR DIMENSION B:
   ⌖ | 0.25 (0.010) Ⓜ | A Ⓜ | S Ⓜ
4. POSITIONAL TOLERANCE FOR DIMENSION D (4 PLACES):
   ⌖ | 0.25 (0.010) Ⓜ | T | A Ⓜ | S Ⓜ
5. POSITIONAL TOLERANCE FOR DIMENSION Q (2 PLACES):
   ⌖ | ϕ 0.25 (0.010) Ⓜ | T | S Ⓜ | A Ⓜ
6. POSITIONAL TOLERANCE FOR DIMENSION U (4 PLACES):
   ⌖ | 0.25 (0.010) Ⓜ | T | A Ⓜ | S Ⓜ
7. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
8. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	37.85	38.35	1.490	1.510
B	17.78	18.28	0.700	0.720
C	8.89	9.55	0.350	0.376
D	0.36	0.66	0.014	0.026
E	3.05	3.42	0.120	0.135
F	3.79	4.34	0.149	0.171
G	29.72 BSC		1.170 BSC	
H	3.81 BSC		0.150 BSC	
J	9.25 BSC		0.364 BSC	
K	5.72	—	0.225	—
L	1.27 BSC		0.050 BSC	
N	6.35 BSC		0.250 BSC	
Q	3.81	4.06	0.150	0.160
R	17.40	19.55	0.685	0.770
S	15.12	15.62	0.595	0.615
U	0.20	0.30	0.008	0.012
V	1.27 BSC		0.050 BSC	

CASE 297B-01

MAXIMUM RATINGS (Flange Temperature = 25°C)

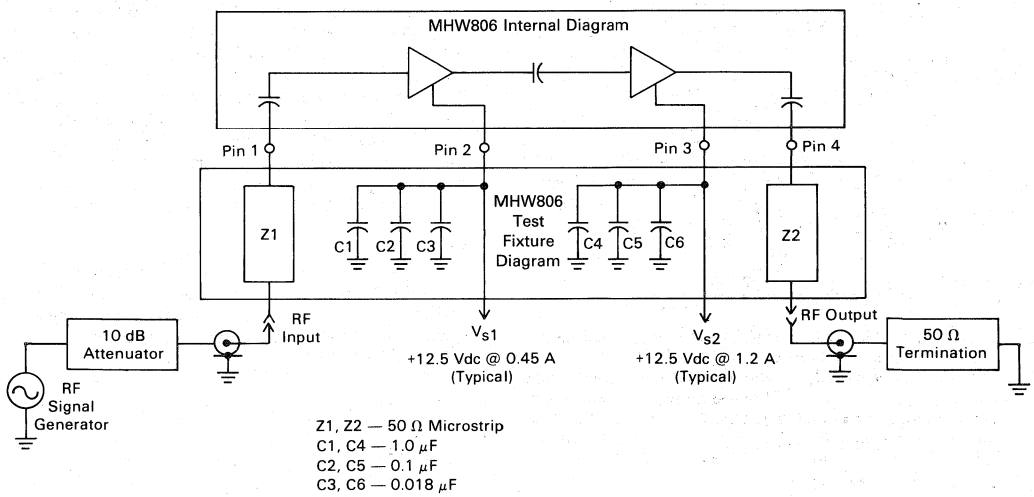
Rating	Symbol	Value	Unit
DC Supply Voltages	V_{S1}, V_{S2}	16	Vdc
RF Input Power ($P_{out} \leq 9.0$ W)	P_{in}	400	mW
RF Output Power ($V_{S1} = V_{S2} = 12.5$ V)	P_{out}	9.0	W
Storage Temperature Range	T_{stg}	−30 to +100	°C
Operating Case Temperature Range	T_C	−40 to +100	°C

4

ELECTRICAL CHARACTERISTICS (Flange Temperature = 25°C, 50 Ω system, and V_{s1} = V_{s2} = 12.5 V unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range	MHW806-1 MHW806-2 MHW806-3 MHW806-4	BW	820 806 890 870	— — — —	850 870 915 960	MHz
Input Power (P_{out} = 6.0 W)	MHW806-1,2 MHW806-3,4	P_{in}	— —	200 300	250 350	mW
Power Gain (P_{out} = 6.0 W)	MHW806-1,2 MHW806-3,4	G_p	13.8 12.3	14.7 13	— —	dB
Efficiency (P_{out} = 6.0 W)		η	30	38	—	%
Harmonic Output (P_{out} = 6.0 W Reference)		—	—	—	−45	dB
Input VSWR (P_{out} = 6.0 W, 50 Ω Reference)		—	—	—	2:1	—
Power Degradation (−30 to +80°C) (Reference P_{out} = 6.0 W @ T_C = 25°C)		—	—	—	1.2	dB
Load Mismatch Stress (V_{s1} = V_{s2} = 16 Vdc, P_{out} = 7.5 W, VSWR = 30:1, all phase angles)		—	No degradation in Power Output			
Stability (P_{in} = 0 to 250 mW, [MHW806-1,2] or 0–350 mW (MHW806-3] consistent with max. P_{out} = 7.5 W, V_{s1} = V_{s2} = V_{s3} = 10 to 16 Vdc, Load VSWR = 4:1)		All spurious outputs ≥70 dB below the desired output signal level				
Quiescent Current (I_{s1} with no RF drive applied)		$I_{s1(q)}$	—	—	125	mA

FIGURE 1 — UHF POWER MODULE TEST SYSTEM DIAGRAM



Z1, Z2 — 50 Ω Microstrip
C1, C4 — 1.0 μF
C2, C5 — 0.1 μF
C3, C6 — 0.018 μF

4

APPLICATIONS INFORMATION

Nominal Operation

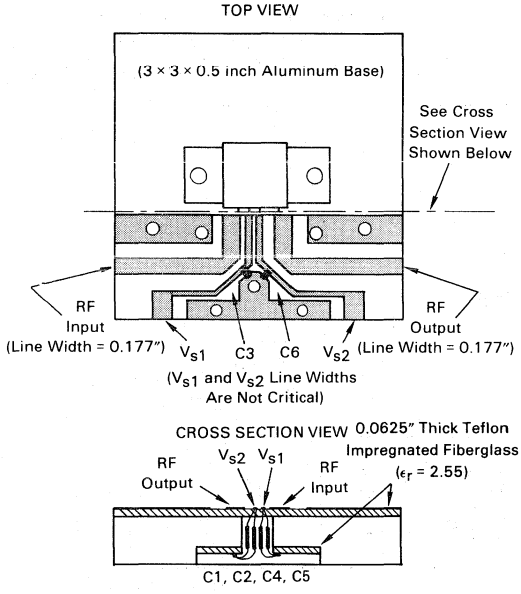
All electrical specifications are based on the following nominal conditions: (P_{out} = 6.0 W, V_{S1} = 12.5 Vdc). This module is designed to have excess gain margin with ruggedness, but operation outside the limits of the published specifications is not recommended unless prior communications regarding the intended use have been made with a factory representative.

Gain Control

In general, the module output power should be limited to 7.5 watts. The preferred method of power output control is to fix both V_{S1} and V_{S2} at 12.5 volts and to vary the input RF drive level at Pin 1.

A second method of output power control is to adjust the supply voltages (V_{S1} independently or V_{S1} and V_{S2} simultaneously).

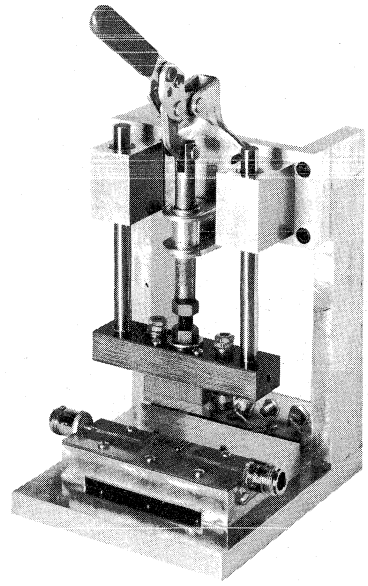
FIGURE 3 — TEST FIXTURE CONSTRUCTION



Bring capacitor leads through fiberglass board and solder to V_{S1} and V_{S2} lines as close to module as possible.

To insure optimum heat transfer from flange to heatsink, use standard 6–32 mounting screws and an adequate quantity of silicon thermal compound (e.g., Dow Corning 340). With both mounting screws finger tight, alternately torque down the screws to 4–6 inch pounds.

FIGURE 2 — TEST FIXTURE ASSEMBLY



Decoupling

Due to the high gain of each of the three stages and the module size limitation, external decoupling networks require careful consideration. Pins 2, 3 and 4 are internally bypassed with a 0.018 μF chip capacitor which is effective for frequencies from 5.0 MHz through 960 MHz. For bypassing frequencies below 5.0 MHz, networks equivalent to that shown in the text fixture schematic are recommended. Inadequate decoupling will result in spurious outputs at specific operating frequencies and phase angles of input and output VSWR.

Load Pull

During final test, each module is load mismatch stress tested in a fixture having the identical decoupling network described in Figure 1. Electrical conditions are V_{S1} equal to 16 volts, load VSWR 30:1 and output power equal to 7.5 watts.

4

MHW806A1 thru MHW806A8

The RF Line

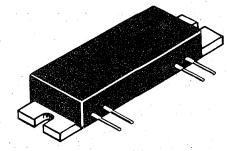
6.0 W — 806–960 MHz

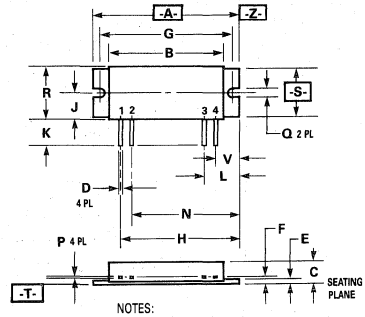
HIGH GAIN RF POWER AMPLIFIER MODULE

UHF POWER AMPLIFIER MODULE

. . . designed for 12.5 volt UHF power amplifier applications in industrial and commercial FM equipment operating from 806 to 950 MHz.

- MHW806A1,A5 820–850 MHz
  MHW806A2,A6 806–870 MHz
  MHW806A3,A7 890–915 MHz
  MHW806A4,A8 870–960 MHz
- Specified 12.5 Volt, UHF Characteristics
  Output Power = 6.0 Watts
  Minimum Gain = 23 dB (MHW806A1,2,3,4)
  = 17.8 dB (MHW806A5,6,7,8)
  Harmonics = −42 dBc Max ($2f_o$)
  = −60 dBc Max ($3f_o$ and Higher)
- 50 Ω Input/Output Impedances
- Guaranteed Stability and Ruggedness
- Features Three Common-Emitter Gain Stages
- Thin-Film Hybrid Construction Gives Consistent Performance and Reliability
- Gold-Metallized and Silicon Nitride-Passivated Transistor Chips
- Controllable, Stable Performance Over More Than 35 dB Range in Output Power





NOTES:
1. POSITIONAL TOLERANCE FOR D DIMENSION (5 PL): ⌖ | 0.25 (0.010) Ⓜ | T | Z
2. POSITIONAL TOLERANCE FOR G DIMENSION: ⌖ | ϕ 0.13 (0.005) Ⓜ | T | A Ⓜ
3. POSITIONAL TOLERANCE FOR P DIMENSION (5 PL): ⌖ | ϕ 0.25 (0.010) Ⓜ | T
4. POSITIONAL TOLERANCE FOR Q DIMENSION (2 PL): ⌖ | ϕ 0.13 (0.005) Ⓜ | T | S Ⓜ
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.

STYLE 1:
PIN 1. RF INPUT
2. + DC
3. + DC
4. + DC
5. RF OUTPUT

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	48.01	48.51	1.890	1.910
B	29.72	30.22	1.170	1.190
C	8.89	9.55	0.350	0.376
D	0.46	0.55	0.018	0.022
E	3.05	3.42	0.120	0.135
F	3.79	4.34	0.149	0.171
G	40.64 BSC		1.600 BSC	
H	35.56 BSC		1.400 BSC	
J	8.77	9.77	0.345	0.385
K	5.72	—	0.225	—
L	17.78 BSC		0.700 BSC	
N	33.02 BSC		1.300 BSC	
P	0.21	0.30	0.008	0.012
Q	3.81	4.06	0.150	0.160
R	17.40	19.55	0.685	0.770
S	15.12	15.49	0.595	0.610
V	12.70 BSC		0.500 BSC	

CASE 301H-01

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltages	V_{s1}	16	Vdc
RF Input Power	P_{in}	80	mW
RF Output Power	P_{out}	9.0	W
Storage Temperature Range	T_{stg}	-30 to +100	°C
Operating Case Temperature Range	T_C	-30 to +100	°C
DC Control Voltage	V_{Cont}	12.5	Vdc

4

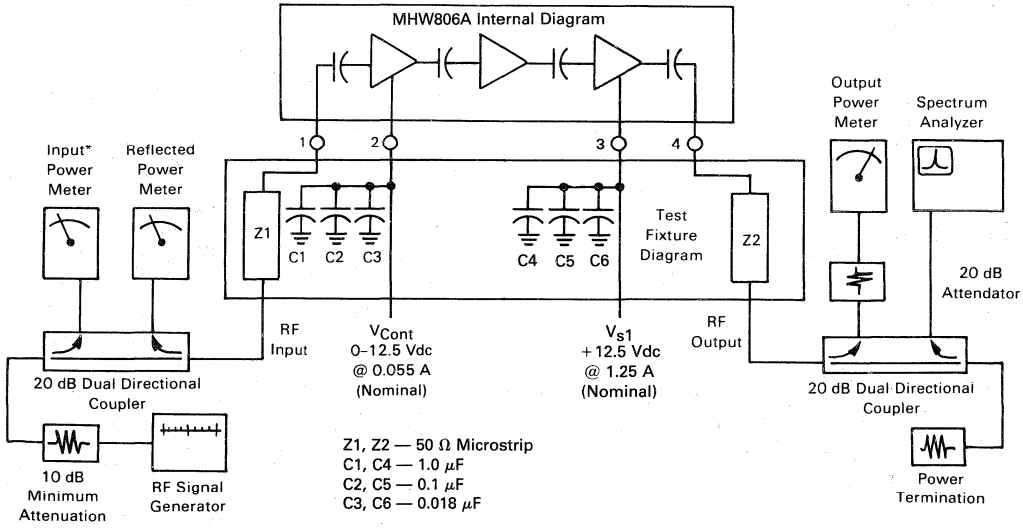
ELECTRICAL CHARACTERISTICS (Flange Temperature = 25°C, 50 Ω system, and V_{s1} = 12.5 V unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range	MHW806A1,A5 MHW806A2,A6 MHW806A3,A7 MHW806A4,A8	BW	820 806 890 870	— — — —	850 870 915 960	MHz
Power Gain (V_{Cont} = 12.5 Vdc, P_{out} = 7.5 W)	MHW806A1,2 MHW806A3	G_p	23 17.8	24 18.3	— —	dB
Efficiency (1) (P_{out} = 6.0 W)		η	30	35	—	%
Harmonic Output (1) (P_{out} = 6.0 W Reference)	$2f_o$ $3f_o$ and Higher	—	— —	— —	−42 −60	dBc
Input VSWR (1) (P_{out} = 6.0 W, 50 Ω Reference, Reflected Signal Filtered to Eliminate Harmonic Content)		—	—	—	2:1	—
Power Degradation (−30 to +80°C) (1) (Reference P_{out} = 6.0 W @ T_C = 25°C)		—	—	—	1.7	dB
Load Mismatch Stress (1) (V_{s1} = 16 Vdc, P_{out} = 7.5 W, VSWR = 30:1, all phase angles)		—	No degradation in Power Output			
Stability (P_{in} = 0 to 30 mW, [MHW808A1,2] or 0–40 mW (MHW808A3], V_{s1} = 10 to 16 Vdc, V_{Cont} = 0 to 12.5 Vdc, Load VSWR = 4:1, P_{out} Max = 7.5 W) (2)			All spurious outputs ≥70 dB below desired output signal level			
Quiescent Current (I_{s1} with no RF drive applied)		$I_{s1(q)}$	—	—	125	mA
Control Voltage	P_{in} = 30 mW (MHW806A1,2), P_{in} = 100 mW (MHW806A3,A4) P_{out} = 6.0 W	V_{Cont}	0	9.0	12.5	Vdc
Control Current		I_{Cont}	0	55	100	mA

(1) P_{in} = 30 mW (MHW806A1,2) or P_{in} = 100 mW (MHW806A3,A4), adjust V_{Cont} for specified P_{out}.
(2) Combination of P_{in}, V_{s1}, and V_{Cont} can not exceed max P_{out} = 7.5 W.

4

FIGURE 1 — UHF POWER MODULE TEST SYSTEM DIAGRAM



*Module input power is forward power as sampled by the directional coupler and read on the input power meter.

APPLICATIONS INFORMATION

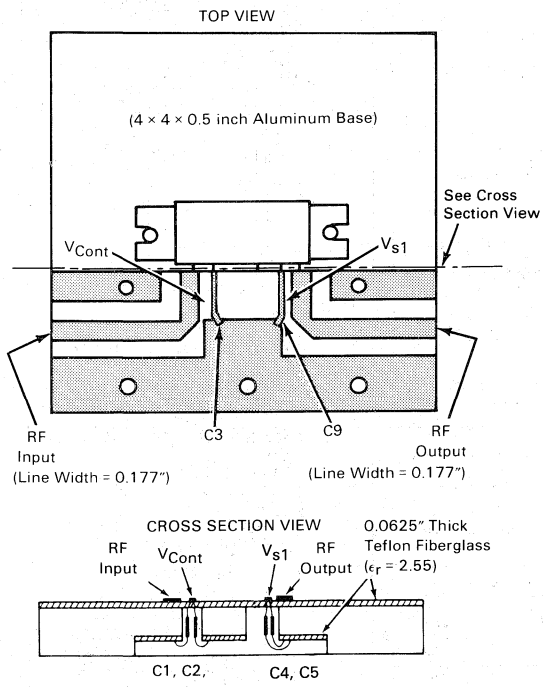
Nominal Operation

All electrical specifications are based on the following nominal conditions: (P_{out} = 6.0 W, V_{s1} = 12.5 Vdc). This module is designed to have excess gain margin with ruggedness, but operation outside the limits of the published specifications is not recommended unless prior communications regarding the intended use has been made with a factory representative.

Gain Control

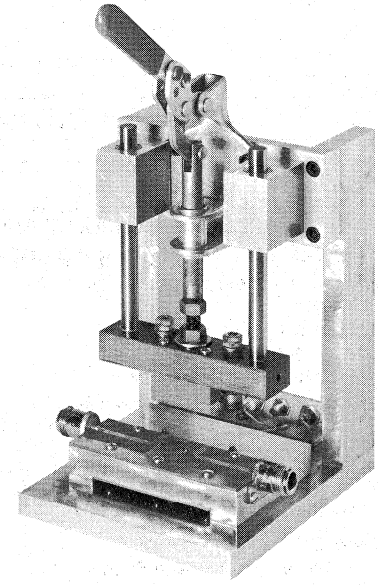
In general, the module output power should be limited to 7.5 watts. The preferred method of power output control is to fix V_{s1} and at 12.5 volts, set RF drive level, and vary the control voltage from 0 to 12.5 Volts. As designed, the module exhibits a gain control range greater than 35 dB using the method described above.

FIGURE 3 — TEST FIXTURE CONSTRUCTION



Bring capacitor leads through fiberglass board and solder to V_{s1}, V_{s2}, and V_{Cont} lines as close to module as possible.

FIGURE 2 — TEST FIXTURE ASSEMBLY



Decoupling

Due to the high gain of each of the three stages and the module size limitation, external decoupling networks require careful consideration. Pins 2, 3 and 4 are internally bypassed with a 0.018 μF chip capacitor which is effective for frequencies from 5.0 MHz through 960 MHz. For bypassing frequencies below 5.0 MHz, networks equivalent to that shown in the text fixture schematic are recommended. Inadequate decoupling will result in spurious outputs at specific operating frequencies and phase angles of input and output VSWR.

Load Mismatch Stress

During final test, each module is load mismatch stress tested in a fixture having the identical decoupling network described in Figure 1. Electrical conditions are V_{s1} equal to 16 volts, load VSWR 30:1 and output power equal to 7.5 watts.

Mounting Considerations

To insure optimum heat transfer from the flange to heatsink, use standard 6–32 mounting screws and an adequate quantity of silicon thermal compound (e.g., Dow Corning 340). With both mounting screws finger tight, alternately torque down the screws to 4–6 inch pounds. The heatsink mounting surface directly beneath the module flange should be flat to within 0.0015 inch to prevent fracturing of ceramic substrate material. For more information on module mounting, see EB-107.

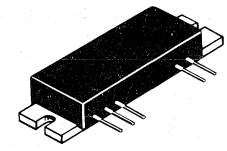
4

MHW820-1
MHW820-2
MHW820-3

The RF Line

18/20 W — 806–950 MHz

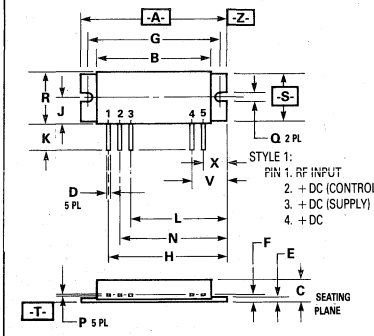
RF POWER
AMPLIFIER MODULE



UHF POWER AMPLIFIER MODULE

. . . designed for 12.5 volt UHF power amplifier applications in industrial and commercial FM equipment operating from 806 to 950 MHz.

- MHW820-1 806–870 MHz
  MHW820-2 806–890 MHz
  MHW820-3 870–950 MHz
- Specified 12.5 Volt, UHF Characteristics
  Output Power = 20 Watts (MHW820-1,2)
  = 18 Watts (MHW820-3)
  Minimum Gain = 19 dB (MHW820-1,2)
  = 17.1 dB (MHW820-3)
  Harmonics = −58 dBc Max
- 50 Ω Input/Output Impedances
- Guaranteed Stability and Ruggedness
- Features Three Common-Emitter Gain Stages
- Thin-Film Hybrid Construction Gives Consistent Performance and Reliability
- Gold-Metallized and Silicon Nitride-Passivated Transistor Chips
- Controllable, Stable Performance Over More Than 30 dB Range in Output Power



NOTES:
1. POSITIONAL TOLERANCE FOR D DIMENSION (4 PL):
   ⌖ | 0.25 (0.010) Ⓜ | T | Z
2. POSITIONAL TOLERANCE FOR G DIMENSION:
   ⌖ | ϕ 0.13 (0.005) Ⓜ | T | A Ⓜ
3. POSITIONAL TOLERANCE FOR P DIMENSION (4 PL):
   ⌖ | 0.25 (0.010) Ⓜ | T
4. POSITIONAL TOLERANCE FOR Q DIMENSION (2 PL):
   ⌖ | ϕ 0.13 (0.005) Ⓜ | T | S Ⓜ
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	55.63	56.13	2.190	2.210
B	35.44	35.94	1.395	1.415
C	8.89	9.55	0.350	0.376
D	0.46	0.55	0.018	0.022
E	3.05	3.42	0.120	0.135
F	3.79	4.34	0.149	0.171
G	48.26 BSC		1.900 BSC	
H	40.64 BSC		1.600 BSC	
J	8.77	9.77	0.345	0.385
K	5.72	—	0.225	—
L	35.56 BSC		1.400 BSC	
N	38.10 BSC		1.500 BSC	
P	0.21	0.30	0.008	0.012
Q	3.81	4.06	0.150	0.160
R	17.53	19.55	0.690	0.770
S	15.12	15.49	0.595	0.610
V	17.78 BSC		0.700 BSC	
X	12.70 BSC		0.500 BSC	

CASE 301G-01

MAXIMUM RATINGS (Flange Temperature = 25°C)

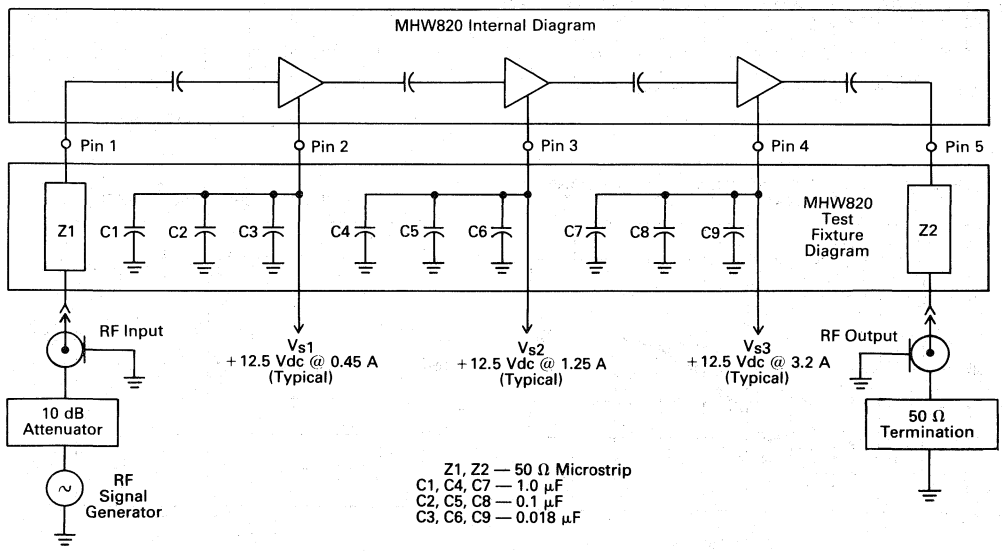
Rating	Symbol	Value	Unit
DC Supply Voltages	V_{S1}, V_{S2}, V_{S3}	16	Vdc
RF Input Power ($P_{out} \leq 25$ W)	P_{in}	400	mW
RF Output Power ($P_{in} \leq 400$ mW)	P_{out}	25	W
Storage Temperature Range	T_{stg}	-30 to +100	°C
Operating Case Temperature Range	T_C	-40 to +100	°C

4

ELECTRICAL CHARACTERISTICS (Flange Temperature = 25°C, 50 Ω system, and $V_{s1} = V_{s2} = 12.5$ V unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range	MHW820-1 MHW820-2 MHW820-3	BW	806 806 870	— — —	870 890 950	MHz
Input Power (P_{out} = 20 W) (P_{out} = 18 W)	MHW820-1, 2 MHW820-3	P_{in}	— —	200 300	250 350	mW
Power Gain (P_{out} = 20 W) (P_{out} = 18 W)	MHW820-1, 2 MHW820-3	G_p	19 17.1	20 17.8	— —	dB
Efficiency (P_{out} = 20 W) (P_{out} = 18 W)	MHW820-1, 2 MHW820-3	η	28 26	32 30	—	%
Harmonic Output (P_{out} Reference = Rated P_{out})		—	—	—	−58	dBc
Input VSWR (P_{out} = Rated P_{out}, 50 Ω Reference)		—	—	—	2:1	—
Power Degradation (−30 to +80°C) (Reference P_{out} = Rated P_{out} @ T_C = 25°C)		—	—	1.2	1.7	dB
Load Mismatch Stress ($V_{s1} = V_{s2} = V_{s3}$ = 16 Vdc, P_{out} = 25 W, VSWR = 30:1, all phase angles)		—	No degradation in Power Output			
Stability (P_{in} = 0 to 250 mW, [MHW820-1, 2] or 350 mW [MHW820-3] consistent with max, P_{out} = 25 W, $V_{s1} = V_{s2} = V_{s3}$ = 10 to 16 Vdc, Load VSWR = 4:1)		All non-harmonic related spurious outputs ≥ 70 dB below the desired output signal level				
Quiescent Current (I_{s1} with no RF drive applied)		$I_{s1(q)}$	—	—	125	mA

FIGURE 1 — 806-950 MHz TEST SYSTEM DIAGRAM



TYPICAL PERFORMANCE CURVES
(MHW820-1, 2)

FIGURE 2 — INPUT POWER, EFFICIENCY AND VSWR versus FREQUENCY

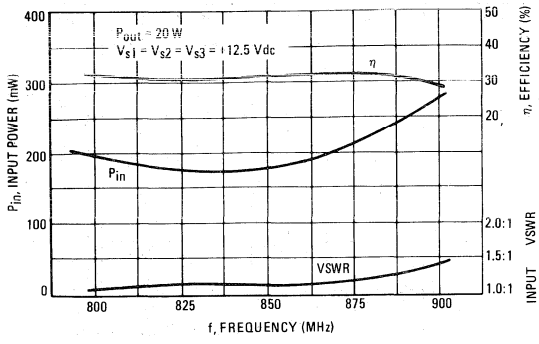


FIGURE 3 — OUTPUT POWER versus INPUT POWER

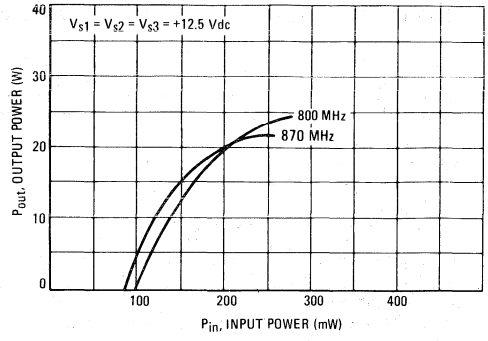


FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE

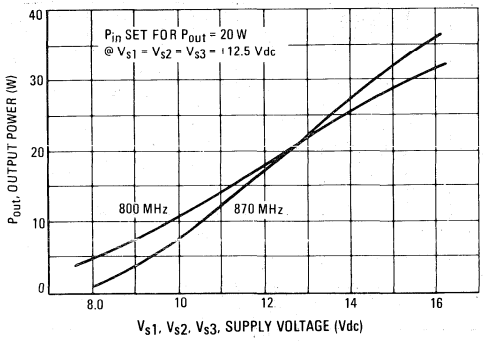


FIGURE 5 — EFFICIENCY versus SUPPLY VOLTAGE

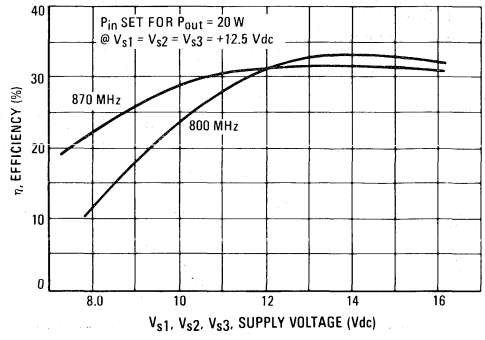


FIGURE 6 — OUTPUT POWER versus SUPPLY VOLTAGE TO FIRST STAGE (V_{s1})

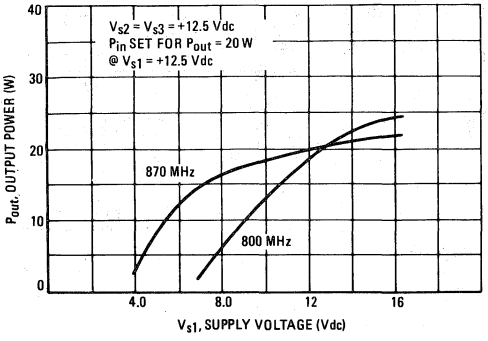
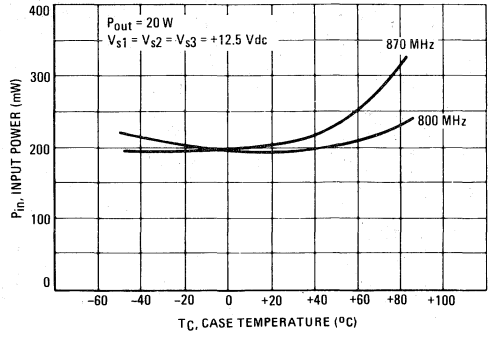


FIGURE 7 — INPUT POWER versus CASE TEMPERATURE



4

TYPICAL PERFORMANCE CURVES
(MHW820-3)

FIGURE 8 — INPUT POWER, EFFICIENCY AND VSWR versus FREQUENCY

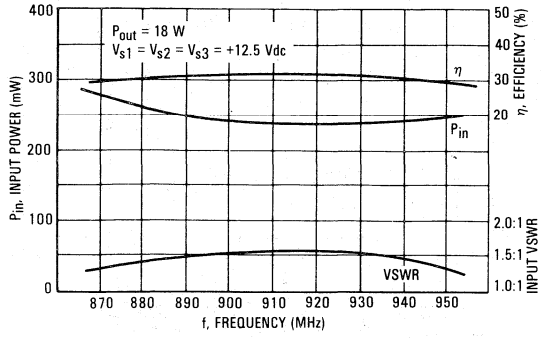


FIGURE 9 — OUTPUT POWER versus INPUT POWER

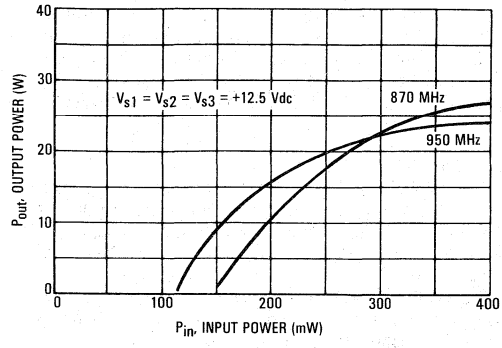


FIGURE 10 — OUTPUT POWER versus SUPPLY VOLTAGE

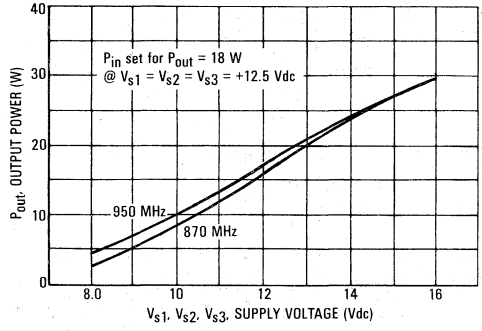
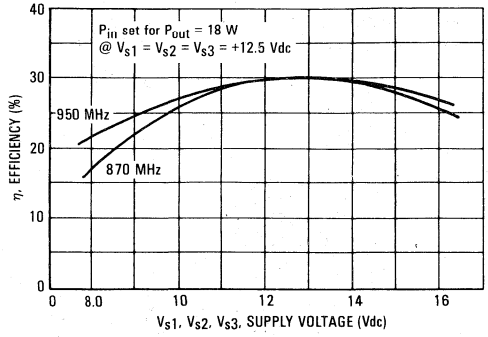


FIGURE 11 — EFFICIENCY versus SUPPLY VOLTAGE



APPLICATIONS INFORMATION

Nominal Operation

All electrical specifications are based on the following nominal conditions: (P_{out} = Rated, V_{s1} = V_{s2} = V_{s3} = 12.5 Vdc). This module is designed to have excess gain margin with ruggedness, but operation outside the limits of the published specifications is not recommended unless prior communications regarding the intended use has been made with a factory representative.

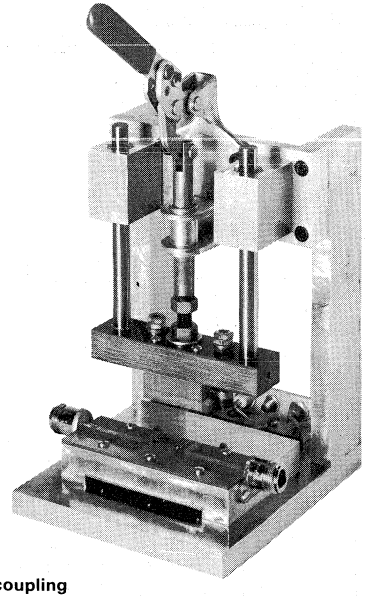
Gain Control

This module is designed for wide range P_{out} level control. The recommended method of power output control, as shown in Figure 3 and 9, is to fix V_{s1}, V_{s2}, and V_{s3} at 12.5 Vdc and vary the input RF drive level at Pin 1.

A second method of output control is to adjust the supply voltage (V_{s1} independently or V_{s1}, V_{s2}, and V_{s3} simultaneously). However, if any of these voltages fall out of the range from 10 to 16 volts module stability cannot be guaranteed. Typical ranges of power output control using this method are shown in Figures 4, 6, and 10.

In all applications, the module output power should be limited to 25 watts.

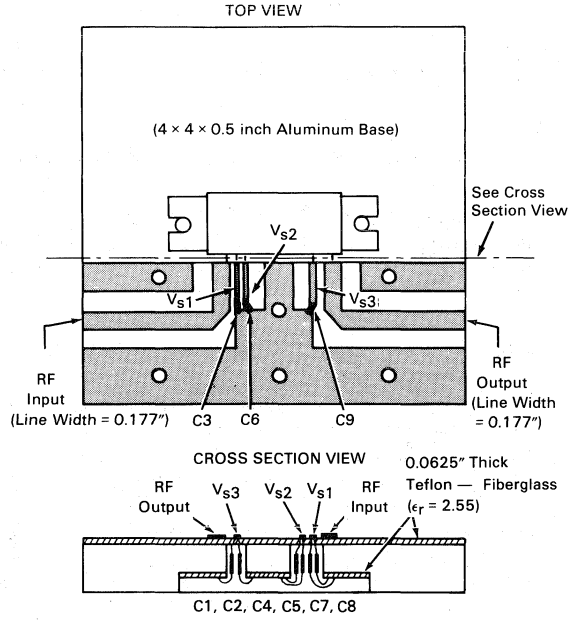
FIGURE 12 — TEST FIXTURE ASSEMBLY



Decoupling

Due to the high gain of each of the two stages and the module size limitation, external decoupling networks require careful consideration. Pins 2, 3 and 4 are internally bypassed with 0.018 μF chip capacitors which are effective for frequencies from 5 MHz through 950 MHz. For bypassing frequencies below 5 MHz, networks equivalent to that shown in the test fixture schematic are recommended. Inadequate decoupling will result in spurious outputs at specific operating frequencies and phase angles of input and output VSWR.

FIGURE 13 — TEST FIXTURE CONSTRUCTION



Bring capacitor leads through fiberglass board and solder to V_{s1}, V_{s2}, and V_{s3} lines as close to module as possible.

To insure optimum heat transfer from flange to heatsink, use standard 6–32 mounting screws and an adequate quantity of silicon thermal compound (e.g., Dow Corning 340). With both mounting screws finger tight, alternately torque down the screws to 4–6 inch pounds.

Load Pull

During final test, each module is "load pull" tested in a fixture having the identical decoupling network described in Figure 1. Electrical conditions are V_{s1}, V_{s2} and V_{s3} equal to 16 volts output, VSWR 30:1 and output power equal to 25 watts.

Mounting Considerations

To insure optimum heat transfer from the flange to heatsink, use standard 6–32 mounting screws and an adequate quantity of silicon thermal compound (e.g., Dow Corning 340). With both mounting screws finger tight, alternately torque down the screws to 4–6 inch pounds. The heatsink mounting surface directly beneath the module flange should be flat to within 0.002 inch to prevent fracturing of ceramic substrate material. For more information on module mounting, see EB-107.

MHW1134
MHW1184
MHW1224
MHW1244

The RF Line

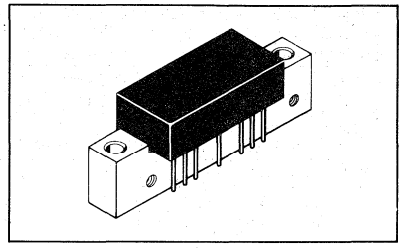
13.0 dB
18.5 dB
22.0 dB
24.0 dB

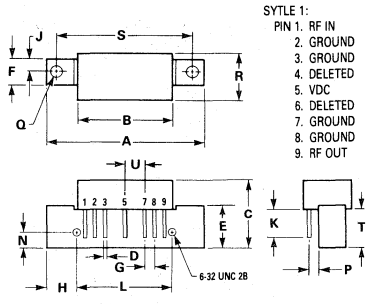
5.0–200 MHz
CATV HIGH-SPLIT
REVERSE AMPLIFIERS

LOW DISTORTION WIDEBAND AMPLIFIER MODULE

. . . designed specifically for broadband applications requiring low distortion characteristics. Specified for use as return amplifiers for mid-split and high-split 2-way cable TV systems. Features all gold metallization system.

- Guaranteed Broadband Power Gain @ f = 5.0–200 MHz
- Guaranteed Broadband Noise Figure @ f = 5.0–175 MHz
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- All Ion-Implanted Arsenic Emitter Transistor Chips with 7.0 GHz f_T's
- Circuit Design Optimized for Good RF Stability Under High VSWR Load Conditions
- Transformers Designed to Insure Good Low Frequency Gain Stability versus Temperature





SYTLE 1:
PIN 1. RF IN
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUT

NOTE:
1. MOUNTING HOLES WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.41	2.67	0.095	0.105
H	9.65	9.78	0.380	0.385
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.335
L	25.40 BSC		1.000 BSC	
N	4.06	4.32	0.160	0.170
P	2.16	2.92	0.085	0.115
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
T	11.05	11.43	0.435	0.450
U	4.95	5.21	0.195	0.205

CASE 714-03

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+65	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

4

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_A = +25°C, 75 Ω system)

Characteristic	Symbol	MHW1134	MHW1184	MHW1224	MHW1244	Units
Power Gain @ 10 MHz	G_P	13.0±0.5	18.5±0.5	22.0±0.5	24.0±0.5	dB
Frequency Range (Response/Return Loss) Note 1	BW	5.0–200				MHz
Cable Slope Equivalent (5.0–200 MHz)	S	−0.2 Min/+0.8 Max				dB
Gain Flatness (5.0–200 MHz)	F	±0.2 Max				dB
Input/Output Return Loss (5.0–200 MHz) Note 1	IRL/ORL	18.0 Min				dB
Cross Modulation Distortion @ +50 dBmV per ch. 12-Channel FLAT (5.0–120 MHz) 22-Channel FLAT (5.0–175 MHz) Notes 2 and 3 26-Channel FLAT (5.0–200 MHz)	 XM_{12} XM_{22} XM_{26}	 −70 Typ −65 Max −65 Typ	 −68 Typ −64 Max −64 Typ	 −67 Typ −62 Max −62 Typ	 −66 Typ −61 Max −61 Typ	 dB dB dB
Composite Triple Beat Distortion @ +50 dBmV per ch. 22-Channel FLAT (5.0–175 MHz) Notes 2 and 3 26-Channel FLAT (5.0–200 MHz)	 CTB_{22} CTB_{26}	 −73 Max −71 Typ	 −72 Max −70 Typ	 −71 Max −68.5 Typ	 −70 Max −67.5 Typ	 dB dB
Individual Triple Beat Distortion @ +50 dBmV per ch. Mid-Split (5.0–120 MHz) T11, T12 and CH2 @ 123.25 MHz High-Split (5.0–175 MHz) T13, CH2 and CH5 @ 175.5 MHz	 TB_3 TB_3	 −90 Typ −87 Typ	 −88 Typ −85 Typ	 −88 Typ −85 Typ	 −87 Typ −84 Typ	 dB dB
Second Order Distortion @ +50 dBmV per ch. High-Split (5.0–175 MHz) CH2, CHA @ 176.5 MHz	IMD	−72 Max	−72 Max	−72 Max	−72 Max	dB
Noise Figure High-Split (5.0–175 MHz) Note 2	NF	7.0 Max	5.5 Max	5.5 Max	5.0 Max	dB
DC Current (V_{DC} = 24 ±0.5 Vdc, T_C = 30°C)	I_{DC}	210 Typ/240 Max				mAdc

1. Response and return loss characteristics are tested and guaranteed for the full 5.0–200 MHz frequency range.
2. Motorola 100% distortion and noise figure testing is performed over the 5.0–175 MHz frequency range. Cross modulation and composite triple beat testing are with 22-channel loading; Video carriers used are:

T7–T13	7.0–43.0 MHz	7-Channels
2–6	55.25–83.25 MHz	5-Channels
A–7	121.25–175.25 MHz	10-Channels

3. Video carriers used for 12-Channel typical performances are T7–6; For 26-Channel typical performance, Channels 8, 9, 10 and 11 are added to the 22-Channel carriers listed above.

MHW1171R
MHW1172R

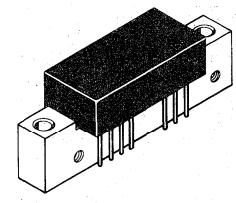
The RF Line

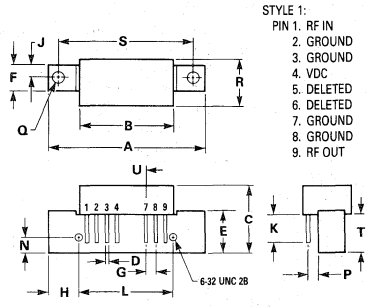
LOW DISTORTION WIDEBAND AMPLIFIER MODULE

. . . designed specifically for broadband applications requiring low distortion characteristics. Specified for use as CATV trunk-line amplifier operating from a −24 Vdc supply. Features all gold metallization system.

- Broadband Power Gain — @ f = 40–300 MHz
  G_p = 17 dB (Typ)
- Broadband Noise Figure — @ f = 300 MHz
  NF = 6.5 dB (Typ)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization

NEGATIVE SUPPLY VOLTAGE CATV TRUNK AMPLIFIER





STYLE 1:
PIN 1. RF IN
2. GROUND
3. GROUND
4. VDC
5. DELETED
6. DELETED
7. GROUND
8. GROUND
9. RF OUT

NOTE:
1. MOUNTING HOLES WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.41	2.67	0.095	0.105
H	9.65	9.78	0.380	0.385
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.335
L	25.40 BSC		1.000 BSC	
N	4.06	4.32	0.160	0.170
P	2.16	2.92	0.085	0.115
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
T	11.05	11.43	0.435	0.450
U	7.49	7.75	0.295	0.305

CASE 714C-03

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	−28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

4

ELECTRICAL CHARACTERISTICS (V_{DD} = 24 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	300	MHz
Power Gain — 50 MHz	G_p	16.6	17.0	17.4	dB
Slope	S	—	+0.5	+1.0	dB
Gain Flatness	—	—	±0.1	±0.2	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion (V_{out} = +50 dBmV per ch., Ch2, 13, R)	IMD				dB
MHW1171R		—	−72	−66	
MHW1172R		—	−74	−68	
Cross Modulation Distortion (V_{out} = +50 dBmV per ch.)					dB
MHW1171R 12 Channel FLAT	XMD_{12}	—	−65	—	
21 Channel FLAT	XMD_{21}	—	−61	—	
30 Channel FLAT	XMD_{30}	—	−58	—	
35 Channel FLAT	XMD_{35}	—	−56	−51	
MHW1172R 12 Channel FLAT	XMD_{12}	—	−69	—	
21 Channel FLAT	XMD_{21}	—	−65	—	
30 Channel FLAT	XMD_{30}	—	−62	—	
35 Channel FLAT	XMD_{35}	—	−60	−56	
Composite Triple-Beat (V_{out} = +50 dBmV per ch.)					dB
MHW1171R 12 Channel FLAT	TB_{12}	—	−71	—	
21 Channel FLAT	TB_{21}	—	−63	—	
30 Channel FLAT	TB_{30}	—	−57	—	
35 Channel FLAT	TB_{35}	—	−54	−51	
MHW1172R 12 Channel FLAT	TB_{12}	—	−75	—	
21 Channel FLAT	TB_{21}	—	−67	—	
30 Channel FLAT	TB_{30}	—	−61	—	
35 Channel FLAT	TB_{35}	—	−58	−56	
Noise Figure (f = 300 MHz)	NF				dB
MHW1171R		—	6.0	7.0	
MHW1172R		—	6.5	8.0	
DC Current (V_{DC} = 24 ±0.5 Vdc)	I_{DC}				mA
MHW1171R		—	160	200	
MHW1172R		—	200	240	

4

MHW1343
MHW1344

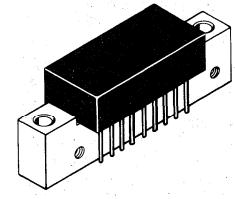
The RF Line

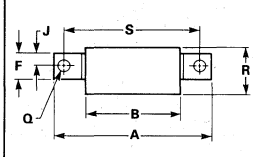
LOW DISTORTION WIDEBAND AMPLIFIER MODULE

. . . designed specifically for broadband applications requiring low distortion characteristics. Specified for use in CATV distribution equipment. Features all-gold metallization system.

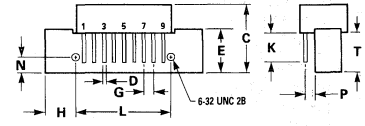
- Accessible Interstage for Gain and Tilt Control Circuitry
- Phase Inversion Possible with Dual Output Pins
- Broadband Power Gain –
  Gp = 34 dB (Typ) @ f = 40-300 MHz, 2 X 17 dB Gain Stages
- Broadband Noise Figure –
  NF = 4.0 dB (Typ) @ f = 300 MHz
- Superior Gain, Return Loss and DC Current Stability
  With Temperature
- All-Gold Metallization

34 dB GAIN
TWO-SECTION CATV
LINE-EXTENDER AMPLIFIER





STYLE 1:
PIN 1. RF IN
2. GROUND
3. GROUND
4. RF OUT
5. VDC
6. RF IN
7. GROUND
8. GROUND
9. RF OUT



NOTE:
1. MOUNTING HOLES WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.41	2.67	0.095	0.105
H	9.65	9.78	0.380	0.385
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.335
L	25.40 BSC		1.000 BSC	
N	4.06	4.32	0.160	0.170
P	2.16	2.92	0.085	0.115
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
T	11.05	11.43	0.435	0.450

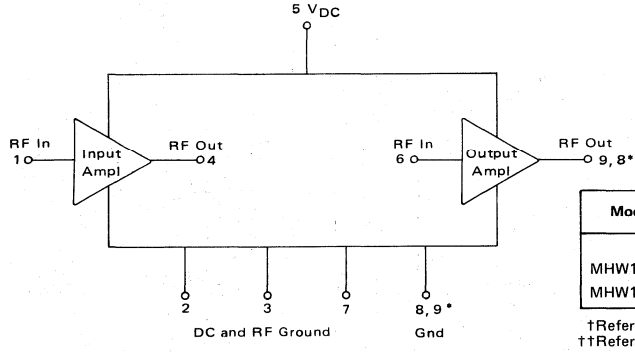
CASE 714B-03

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{DD} = 24 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	300	MHz
Power Gain — 50 MHz	G_p	33	34	35	dB
Slope	S	—	+0.8	+1.5	dB
Gain Flatness	—	—	±0.2	±0.5	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	IRL_1/ORL_2 ORL_1/IRL_2	18 16	— —	— —	dB
Second Order Intermodulation Distortion (V_{out} = +48 dBmV per ch., Ch 2, 13, R)	IMD	—	−72	−64	dB
Cross Modulation Distortion (V_{out} = +48 dBmV per ch.) 12 Channel FLAT 21 Channel FLAT 30 Channel FLAT 35 Channel FLAT	 XMD_{12} XMD_{21} XMD_{30} XMD_{35}	 — — — —	 −71 −67 −64 −62	 — — — −57	dB
Composite Triple Beat (V_{out} = +48 dBmV per ch.) 12 Channel FLAT 21 Channel FLAT 30 Channel FLAT 35 Channel FLAT	 CTB_{12} CTB_{21} CTB_{30} CTB_{35}	 — — — —	 −77 −69 −63 −60	 — — — −58	dB
Noise Figure (f = 300 MHz)	NF	—	4.0	6.0	dB
DC Current (V_{DC} = 24 ±0.5 Vdc, T_C = 30°C)	I_{DC}	—	300	340	mA



'* Pin 8 or Pin 9 must be grounded.

Module	Output Phase of First Stage	Output Phase of Second Stage	
	Pin 4†	Pin 8††	Pin 9††
MHW1343	Inverted	Inverted	In Phase
MHW1344	In Phase	Inverted	In Phase

†Reference phase is signal into Pin 1.
††Reference phase is signal into Pin 6.

MHW3171
MHW3172

The RF Line

17 dB GAIN

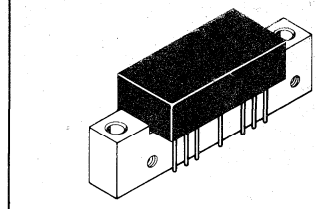
330 MHz

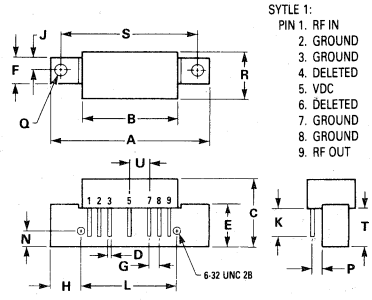
**40-CHANNEL
CATV INPUT/OUTPUT
TRUNK AMPLIFIER**

LOW DISTORTION WIDEBAND AMPLIFIER MODULE

. . . designed for broadband applications requiring low-distortion characteristics. Specifically intended for CATV market requirements. Features ion-implanted arsenic emitter transistors with 6.0 GHz f_T, and an all gold metallization system.

- Broadband Power Gain — @ f = 40–330 MHz
  G_p = 17.2 dB (Typ) @ 50 MHz
- Broadband Noise Figure — @ f = 330 MHz
  NF = 5.5 dB (Typ) MHW3171
  = 6.5 dB (Typ) MHW3172
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization





SYTLE 1:
PIN 1. RF IN
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUT

NOTE:
1. MOUNTING HOLES WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.41	2.67	0.095	0.105
H	9.65	9.78	0.380	0.385
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.335
L	25.40 BSC		1.000 BSC	
N	4.06	4.32	0.160	0.170
P	2.16	2.92	0.085	0.115
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
T	11.05	11.43	0.435	0.450
U	4.95	5.21	0.195	0.205

CASE 714-03

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

4

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_A = +25°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	MHW3171 Min	MHW3171 Typ	MHW3171 Max	MHW3172 Min	MHW3172 Typ	MHW3172 Max	Unit
Frequency Range		BW	40	—	330	40	—	330	MHz
Power Gain — 50 MHz		G_p	16.7	17.2	17.7	16.7	17.2	17.7	dB
Slope		S	—	+0.4	+1.0	—	+0.4	+1.0	dB
Gain Flatness		—	—	±0.1	±0.2	—	±0.1	±0.2	dB
Return Loss — Input/Output (Z_o = 75 Ohms)		IRL/ORL	18	—	—	18	—	—	dB
Second Order Intermodulation Distortion (V_{out} = +50 dBmV per ch.)		IMD	—	—	−68	—	—	−70	dB
Cross Modulation Distortion (V_{out} = +50 dBmV per ch.)	35-Channel FLAT	XMD_{35}	—	—	−55	—	—	−58	dB
	40-Channel FLAT	XMD_{40}	—	—	−54	—	—	−57	
Composite Triple Beat (V_{out} = +50 dBmV per ch.)	35-Channel FLAT	CTB_{35}	—	—	−56	—	—	−59	dB
	40-Channel FLAT	CTB_{40}	—	—	−54	—	—	−57	
Noise Figure (f = 330 MHz)		NF	—	5.5	6.0	—	6.5	7.0	dB
DC Current (V_{DC} = 24 ±0.5 Vdc, T_C = 30°C)		I_{DC}	—	180	200	—	210	240	mA

4

MHW3181
MHW3182

The RF Line

LOW DISTORTION WIDEBAND AMPLIFIER MODULE

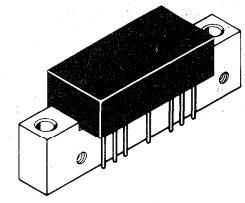
. . . designed for broadband applications requiring low-distortion characteristics. Specifically intended for CATV market requirements. Features ion-implanted arsenic emitter transistors with 6.0 GHz f_T, and an all gold metallization system.

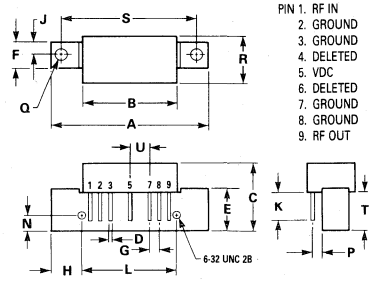
- Broadband Power Gain — @ f = 40–330 MHz
  G_p = 18.2 dB (Typ) @ 50 MHz
- Broadband Noise Figure — @ f = 330 MHz
  NF = 5.2 dB (Typ) MHW3181
  = 6.2 dB (Typ) MHW3182
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization

18 dB GAIN

330 MHz

40-CHANNEL CATV INPUT/OUTPUT TRUNK AMPLIFIER





SYTLE 1:
PIN 1. RF IN
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUT

NOTE:
1. MOUNTING HOLES WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.41	2.67	0.095	0.105
H	9.65	9.78	0.380	0.385
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.335
L	25.40 BSC		1.000 BSC	
N	4.06	4.32	0.160	0.170
P	2.16	2.92	0.085	0.115
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
T	11.05	11.43	0.435	0.450
U	4.95	5.21	0.195	0.205

CASE 714-03

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_A = +25°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	MHW3181 Min	MHW3181 Typ	MHW3181 Max	MHW3182 Min	MHW3182 Typ	MHW3182 Max	Unit
Frequency Range		BW	40	—	330	40	—	330	MHz
Power Gain — 50 MHz		G_p	17.7	18.2	18.7	17.7	18.2	18.7	dB
Slope		S	—	+0.4	+1.0	—	+0.4	+1.0	dB
Gain Flatness		—	—	±0.1	±0.2	—	±0.1	±0.2	dB
Return Loss — Input/Output (Z_o = 75 Ohms)		IRL/ORL	18	—	—	18	—	—	dB
Second Order Intermodulation Distortion (V_{out} = +50 dBmV per ch.)		IMD	—	—	−68	—	—	−68	dB
Cross Modulation Distortion (V_{out} = +50 dBmV per ch.)	35-Channel FLAT	XMD_{35}	—	—	−55	—	—	−58	dB
	40-Channel FLAT	XMD_{40}	—	—	−54	—	—	−57	
Composite Triple Beat (V_{out} = +50 dBmV per ch.)	35-Channel FLAT	CTB_{35}	—	—	−54	—	—	−57	dB
	40-Channel FLAT	CTB_{40}	—	—	−52	—	—	−55	
Noise Figure (f = 330 MHz)		NF	—	5.2	6.0	—	6.2	7.0	dB
DC Current (V_{DC} = 24 ±0.5 Vdc, T_C = 30°C)		I_{DC}	—	180	200	—	210	240	mA

4

MHW3222

The RF Line

LOW-DISTORTION WIDEBAND AMPLIFIER MODULE

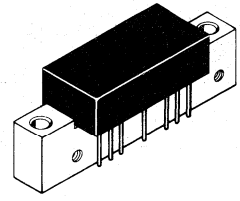
. . . designed for broadband applications requiring low-distortion characteristics. Specifically intended for CATV market requirements. Features ion-implanted arsenic emitter transistors with 6.0 GHz f_T, and an all gold metallization system.

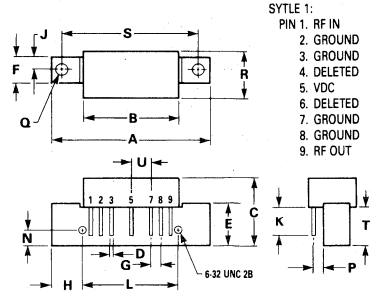
- Broadband Power Gain — @ f = 40–330 MHz
  G_p = 22 dB (Typ)
- Broadband Noise Figure — @ f = 330 MHz
  NF = 5.0 dB (Typ)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization

22 dB GAIN

330 MHz

**40-CHANNEL
CATV TRUNK AMPLIFIER**





SYTLE 1:
PIN 1. RF IN
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUT

NOTE:
1. MOUNTING HOLES WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.41	2.67	0.095	0.105
H	9.65	9.78	0.380	0.385
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.335
L	25.40 BSC		1.000 BSC	
N	4.06	4.32	0.160	0.170
P	2.16	2.92	0.085	0.115
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
T	11.05	11.43	0.435	0.450
U	4.95	5.21	0.195	0.205

CASE 714-03

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

4

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_A = +25°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	330	MHz
Power Gain — 50 MHz		G_p	21.5	22	22.5	dB
Slope		S	0	0.5	1.0	dB
Gain Flatness		—	—	—	±0.2	dB
Return Loss — Input/Output (Z_o = 75 Ohms)		IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion (V_{out} = +50 dBmV per ch.)		IMD	—	—	−65	dB
Cross Modulation Distortion (V_{out} = +50 dBmV per ch.)	35-Channel FLAT 40-Channel FLAT	XMD_{35} XMD_{40}	— —	— —	−55 −54	dB
Composite Triple Beat (V_{out} = +50 dBmV per ch.)	35-Channel FLAT 40-Channel FLAT	CTB_{35} CTB_{40}	— —	— —	−57 −55	dB
Noise Figure (f = 330 MHz)		NF	—	5.0	6.5	dB
DC Current (V_{DC} = 24 ±0.5 Vdc, T_C = 30°C)		I_{DC}	—	210	240	mA

4

MHW3342

The RF Line

330 MHz CATV AMPLIFIER MODULE

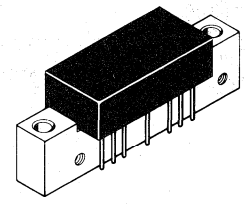
. . . designed specifically for 330 MHz CATV applications. Features ion-implanted arsenic emitter transistors with 6.0 GHz f_T and an all gold metallization system.

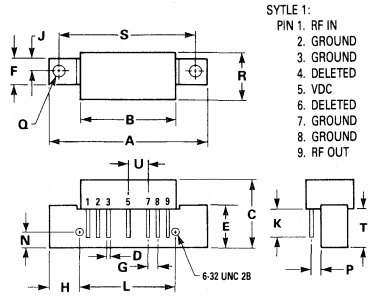
- Specified for 40-Channel Performance
- Broadband Power Gain — @ f = 40–330 MHz
  G_p = 34 dB (Typ)
- Broadband Noise Figure — @ f = 330 MHz
  NF = 4.5 dB (Typ)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 6.0 GHz Ion-Implanted Transistors

34 dB GAIN

330 MHz

40-CHANNEL CATV LINE EXTENDER AMPLIFIERS





SYTLE 1:
PIN 1. RF IN
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUT

NOTE:
1. MOUNTING HOLES WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.41	2.67	0.095	0.105
H	9.65	9.78	0.380	0.385
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.335
L	25.40 BSC		1.000 BSC	
N	4.06	4.32	0.160	0.170
P	2.16	2.92	0.085	0.115
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
T	11.05	11.43	0.435	0.450
U	4.95	5.21	0.195	0.205

CASE 714-03

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_A = +25°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	330	MHz
Power Gain — 50 MHz		G_p	33	34	35	dB
Slope		S	0	+1.0	+2.0	dB
Gain Flatness		—	—	±0.2	±0.5	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–450 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion (V_{out} = +50 dBmV per ch.)		IMD	—	—	−68	dB
Cross Modulation Distortion (V_{out} = +50 dBmV per ch.)	35-Channel FLAT 40-Channel FLAT	XMD_{35} XMD_{40}	— —	— —	−57 −55	dB
Composite Triple Beat (V_{out} = +50 dBmV per ch.)	35-Channel FLAT 40-Channel FLAT	CTB_{35} CTB_{40}	— —	— —	−57 −55	dB
Noise Figure (f = 330 MHz)		NF	—	4.5	5.5	dB
DC Current (V_{DC} = 24 ±0.5 Vdc, T_C = 30°C)		I_{DC}	—	300	340	mA

MHW4524F

The RF Line

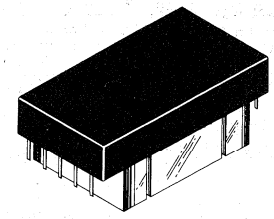
24 dB GAIN

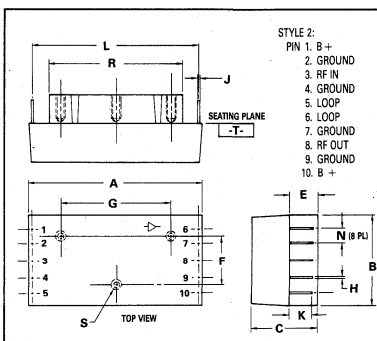
450 MHz

60-CHANNEL
CATV FEEDFORWARD AMPLIFIER

450 MHz CATV HYBRID AMPLIFIER

- Fully Integrated Feedforward Amplifier
- Specifically Designed To Provide Improved Performance in 450 MHz CATV Applications
- Distortion Components Reduced More Than 20 dB from Conventional CATV Hybrid Amplifiers
- Specified For 60-Channel Performance
- Fourth Generation CATV Transistor Technology with All Gold Metallization and 7.0 GHz f_T
- Hybrid Thin-Film Technology Used Throughout For Optimum Performance and High Reliability





STYLE 2:
PIN 1. B+
2. GROUND
3. RF IN
4. GROUND
5. LOOP
6. LOOP
7. GROUND
8. RF OUT
9. GROUND
10. B+

NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. POSITIONAL TOLERANCE FOR LEADS: H AND J DIMENSIONS
   ⌖ | .25 (0.010) Ⓜ | T | A Ⓜ | B Ⓜ
   MEASURED AT SEATING PLANE.
3. POSITIONAL TOLERANCE FOR S MINOR DIAMETERS:
   ⌖ | ϕ 0.25 (0.010) Ⓜ | T | A Ⓜ | B Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
5. CONTROLLING DIMENSION: INCH

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	52.96	53.46	2.085	2.105
B	28.32	28.70	1.115	1.130
C	21.08	21.59	0.830	0.850
E	11.18	11.43	0.440	0.450
F	15.87 BSC		0.625 BSC	
G	34.16 BSC		1.345 BSC	
H	0.46	0.55	0.018	0.022
J	0.20	0.30	0.008	0.012
K	—	7.62	—	0.300
L	50.92 BSC		2.005 BSC	
N	5.08 BSC		0.200 BSC	
R	40.64 BSC		1.600 BSC	
S	—		6-32 UNC-2B	

CASE 774-01

ABSOLUTE MAXIMUM RATINGS

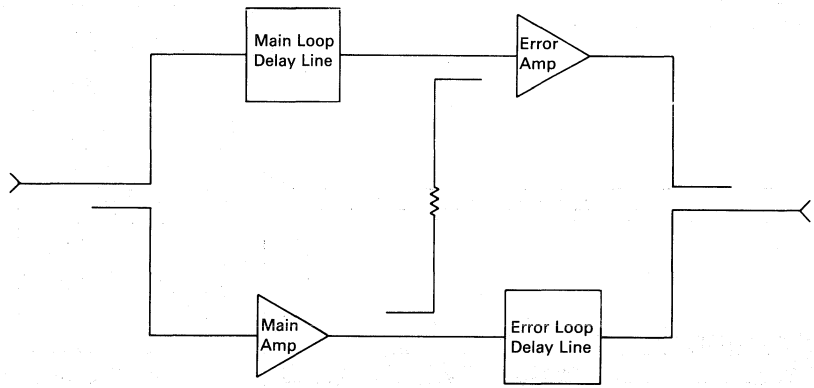
Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +90	°C
Storage Temperature Range	T_{stg}	−40 to +90	°C

NOTE: All electrical specifications listed below are design targets and subject to change.

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +35°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	450	MHz
Power Gain — 50 MHz		G_p	23.3	24	24.7	dB
Slope		S	0	—	1.5	dB
Gain Flatness		—	—	—	±0.3	dB
Return Loss — Input/Output (Z_o = 75 Ohms)		IRL/ORL	18	—	—	dB
Second Order Distortion (V_{out} = +50 dBmV)		IMD	—	—	−80	dB
Cross Modulation Distortion (V_{out} = +46 dBmV)	60-Channel FLAT	XM_{60}	—	—	−75	dB
Composite Triple Beat (60 Channel FLAT) (V_{out} = +46 dBmV)	@ + 35°C −20°C to +90°C	CTB_{60}	— —	— —	−80 −75	dB
Noise Figure (f = 450 MHz)		NF	—	8.0	8.5	dB
DC Current (V_{DC} = 24 ±0.5 Vdc, T_C = 30°C)		I_{DC}	—	—	650	mA

FIGURE 1 — MHW4524F FEEDFORWARD AMPLIFIER BLOCK DIAGRAM



MHW5122A

The RF Line

12.5 dB GAIN

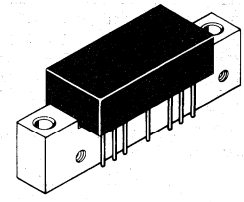
450 MHz

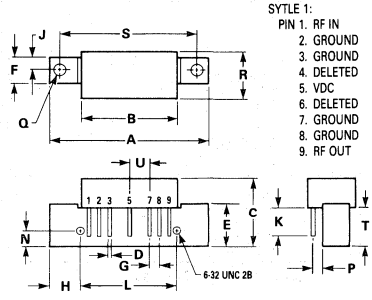
60-CHANNEL CATV TRUNK AMPLIFIERS

450 MHz CATV AMPLIFIER MODULE

. . . designed for broadband applications requiring low distortion characteristics. Specified for use as a CATV trunk-line amplifier. Features ion-implanted arsenic emitter transistors with 7.0 GHz f_T, and all an gold metallization system.

- Specified for 53- and 60-Channel Performance
- Broadband Power Gain — @ f = 40–450 MHz
  G_p = 12.5 dB (Typ)
- Broadband Noise Figure — @ f = 450 MHz
  NF = 8.0 dB (Typ)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion-Implanted Transistors





SYTLE 1:
PIN 1. RF IN
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUT

NOTE:
1. MOUNTING HOLES WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.41	2.67	0.095	0.105
H	9.65	9.78	0.380	0.385
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.335
L	25.40 BSC		1.000 BSC	
N	4.06	4.32	0.160	0.170
P	2.16	2.92	0.085	0.115
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
T	11.05	11.43	0.435	0.450
U	4.95	5.21	0.195	0.205

CASE 714-03

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_A = +25°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	450	MHz
Power Gain — 50 MHz		G_p	12	12.5	13	dB
Slope		S	+0.2	+0.7	+1.5	dB
Gain Flatness		—	—	±0.1	±0.2	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–450 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion		IMD				dB
(V_{out} = +46 dBmV per ch., Ch 2, M6, M15)			—	—	−74	
(V_{out} = +46 dBmV per ch., Ch2, M13, M22)			—	—	−72	
Cross Modulation Distortion	53-Channel FLAT	XMD_{53}	—	−63	—	dB
(V_{out} = +46 dBmV per ch.)	60-Channel FLAT	XMD_{60}	—	−63	−61	
Composite Triple Beat	53-Channel FLAT	CTB_{53}	—	−62	−61	dB
(V_{out} = +46 dBmV per ch.)	60-Channel FLAT	CTB_{60}	—	−59	−58	
DIN (European Applications Only)*						dBμV**
300 MHz — (CH V + Q − P @ W)		DIN1	—	—	125	
400 MHz — (CH M8 + M15 − M9 @ M14)		DIN2	—	—	124	
450 MHz — (CH M20 + M23 − M22 @ M21)		DIN3	—	—	123	
Noise Figure (f = 450 MHz)		NF	—	8.0	9.0	dB
DC Current (V_{DC} = 24 ±0.5 Vdc, T_C = 30°C)		I_{DC}	—	200	240	mA

***DIN (European Applications Only)**

NCTA Channel Designation	Frequency (MHz)	DIN Output Level (dBmV)**	DIN Beat Level dB Relative to Ref. Ch.
P	253.25	+59	≤ −60
Q	259.25	+59	
V	289.25	+65	
W (Ref.)	295.25	+65	
M8	361.25	+58	≤ −60
M9	367.25	+58	
M14 (Ref.)	397.25	+64	
M15	403.25	+64	
M20	433.25	+63	≤ −60
M21 (Ref.)	439.25	+63	
M22	445.25	+57	
M23	451.25	+57	

***DIN (dBμV) = Reference Channel Level (dBmV) + 60 dB

4

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MHW5141A
MHW5142A

The RF Line

14 dB GAIN

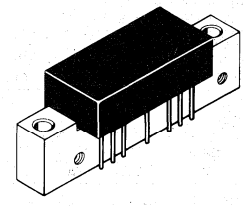
450 MHz

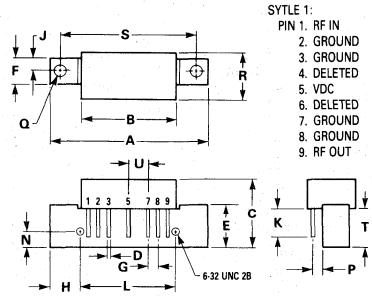
60-CHANNEL CATV INPUT/OUTPUT TRUNK AMPLIFIERS

450 MHz CATV AMPLIFIER MODULE

. . . designed specifically for 450 MHz CATV applications. Features ion-implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

- Specified for 60-Channel Performance
- Broadband Power Gain — @ f = 40–450 MHz
  G_p = 14 dB (Typ) @ 50 MHz
  14.5 dB (Min) @ 450 MHz
- Broadband Noise Figure @ 450 MHz
  NF = 7.0 dB (Max) MHW5141A
  8.0 dB (max) MHW5142A
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion-Implanted Transistors





SYTLE 1:
PIN 1. RF IN
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUT

NOTE:
1. MOUNTING HOLES WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.41	2.67	0.095	0.105
H	9.65	9.78	0.380	0.385
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.335
L	25.40 BSC		1.000 BSC	
N	4.06	4.32	0.160	0.170
P	2.16	2.92	0.085	0.115
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
T	11.05	11.43	0.435	0.450
U	4.95	5.21	0.195	0.205

CASE 714-03

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +35°C, 75 Ω system unless otherwise noted)

Characteristic	Symbol	MHW5141A Min	MHW5141A Typ	MHW5141A Max	MHW5142A Min	MHW5142A Typ	MHW5142A Max	Unit
Frequency Range	BW	40	—	450	40	—	450	MHz
Power Gain — 50 MHz	G_p	13.5	14	14.5	13.5	14	14.5	dB
Power Gain — 450 MHz	G_p	14.5	—	—	14.5	—	—	dB
Slope	S	0.2	—	1.5	0.2	—	1.5	dB
Gain Flatness	—	—	—	±0.1	±0.2	—	±0.1	±0.2	dB
Return Loss — Input/Output 40–450 MHz (Z_o = 75 Ohms)	IRL/ORL	18	—	—	18	—	—	dB
Second Order Intermodulation Distortion	IMD							dB
(V_{out} = +46 dBmV per ch., Ch 2, M6, M15)		—	—	−72	—	—	−74	
(V_{out} = +46 dBmV per ch., Ch 2, M13, M22)		—	—	−72	—	—	−74	
Cross Modulation Distortion								dB
(V_{out} = +46 dBmV per ch.) 53-Channel FLAT	XMD_{53}	—	−61	—	—	−63	—	
60-Channel FLAT	XMD_{60}	—	−59	−56	—	−62	−59	
Composite Triple Beat								dB
(V_{out} = +46 dBmV per ch.) 53-Channel FLAT	CTB_{53}	—	−61	—	—	−63	—	
60-Channel FLAT	CTB_{60}	—	−59	−56	—	−62	−59	
DIN (European Applications Only)*								dBμV**
300 MHz — (CH V + Q − P @ W)	DIN1	—	—	125	—	—	127	
400 MHz — (CH M8 + M15 − M9 @ M14)	DIN2	—	—	124	—	—	126	
450 MHz — (CH M20 + M23 − M22 @ M21)	DIN3	—	—	123	—	—	125	
Noise Figure (f = 450 MHz)	NF	—	—	7.0	—	—	8.0	dB
DC Current (V_{DC} = 24 ±0.5 Vdc, T_C = 30°C)	I_{DC}	—	180	200	—	210	240	mA

***DIN (European Applications Only)**

NCTA Channel Designation	Frequency (MHz)	DIN Output Level (dBmV)** MHW5181A	DIN Output Level (dBmV)** MHW5182A	DIN Beat Level dB Relative to Ref. Ch.
P	253.25	+59	+61	≤ −60
Q	259.25	+59	+61	
V	289.25	+65	+67	
W (Ref.)	295.25	+65	+67	
M8	361.25	+58	+60	≤ −60
M9	367.25	+58	+60	
M14 (Ref.)	397.25	+64	+66	
M15	403.25	+64	+66	
M20	433.25	+63	+65	≤ −60
M21 (Ref.)	439.25	+63	+65	
M22	445.25	+57	+59	
M23	451.25	+57	+59	

**DIN (dBμV) = Reference Channel Level (dBmV) + 60 dB

4

MHW5162A

The RF Line

16.4 dB GAIN

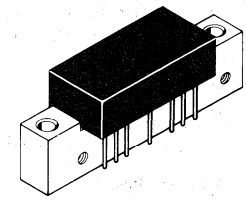
450 MHz

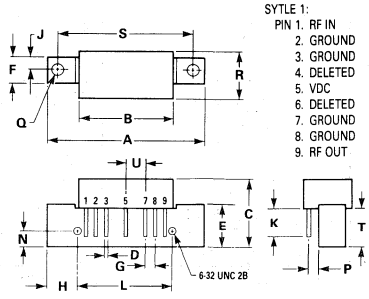
60-CHANNEL
CATV TRUNK AMPLIFIERS

450 MHz CATV AMPLIFIER MODULE

. . . designed for broadband applications requiring low-distortion characteristics. Specified for use as a CATV trunk-line amplifier. Features ion-implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

- Specified for 53- and 60-Channel Performance
- Broadband Power Gain — @ f = 40–450 MHz
  G_p = 16.4 dB (Typ)
- Broadband Noise Figure — @ f = 450 MHz
  NF = 8.0 dB (Typ)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion-Implanted Transistors





SYTLE 1:
PIN 1. RF IN
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUT

NOTE:
1. MOUNTING HOLES WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.41	2.67	0.095	0.105
H	9.65	9.78	0.380	0.385
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.335
L	25.40 BSC		1.000 BSC	
N	4.06	4.32	0.160	0.170
P	2.16	2.92	0.085	0.115
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
T	11.05	11.43	0.435	0.450
U	4.95	5.21	0.195	0.205

CASE 714-03

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_A = +25°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	450	MHz
Power Gain — 50 MHz		G_p	15.9	16.4	16.9	dB
Slope		S	+0.2	+0.7	+1.5	dB
Gain Flatness		—	—	±0.1	±0.2	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–450 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion		IMD				dB
(V_{out} = +46 dBmV per ch., Ch 2, M6, M15)			—	—	−74	
(V_{out} = +46 dBmV per ch., Ch 2, M13, M22)			—	—	−72	
Cross Modulation Distortion	53-Channel FLAT	XMD_{53}	—	−63	—	dB
(V_{out} = +46 dBmV per ch.)	60-Channel FLAT	XMD_{60}	—	−63	−61	
Composite Triple Beat	53-Channel FLAT	CTB_{53}	—	−62	−61	dB
(V_{out} = +46 dBmV per ch.)	60-Channel FLAT	CTB_{60}	—	−59	−58	
DIN (European Applications Only)*						dBμV**
300 MHz — (CH V + Q − P @ W)		DIN1	—	—	127	
400 MHz — (CH M8 + M15 − M9 @ M14)		DIN2	—	—	125	
450 MHz — (CH M20 + M23 − M22 @ M21)		DIN3	—	—	124	
Noise Figure (f = 450 MHz)		NF	—	8.0	9.0	dB
DC Current (V_{DC} = 24 ±0.5 Vdc, T_C = 30°C)		I_{DC}	—	200	220	mA

***DIN (European Applications Only)**

NCTA Channel Designation	Frequency (MHz)	DIN Output Level (dBmV)**	DIN Beat Level dB Relative to Ref. Ch.
		MHW5162A	
P	253.25	61	≤ −60
Q	259.25	61	
V	289.25	67	
W (Ref.)	295.25	67	
M8	361.25	59	≤ −60
M9	367.25	59	
M14 (Ref.)	397.25	65	
M15	403.25	65	
M20	433.25	64	≤ −60
M21 (Ref.)	439.25	64	
M22	445.25	58	
M23	451.25	58	

**DIN (dBμV) = Reference Channel Level (dBmV) + 60 dB

4

MHW5171A
MHW5172A

The RF Line

17 dB GAIN

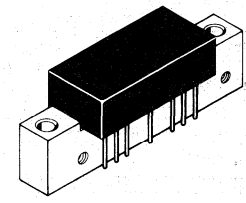
450 MHz

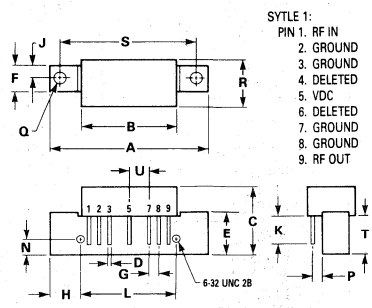
60-CHANNEL
CATV INPUT/OUTPUT
TRUNK AMPLIFIERS

450 MHz CATV AMPLIFIER MODULE

. . . designed specifically for 450 MHz CATV applications. Features ion-implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

- Specified for 53- and 60-Channel Performance
- Broadband Power Gain — @ f = 40–450 MHz
  G_p = 17.4 dB (Typ)
- Broadband Noise Figure
  NF = 7.0 dB (Max) MHW5171A
  8.0 dB (Max) MHW5172A
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion-Implanted Transistors





SYTLE 1:
PIN 1. RF IN
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUT

NOTE:
1. MOUNTING HOLES WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.41	2.67	0.095	0.105
H	9.65	9.78	0.380	0.385
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.335
L	25.40 BSC		1.000 BSC	
N	4.06	4.32	0.160	0.170
P	2.16	2.92	0.085	0.115
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
T	11.05	11.43	0.435	0.450
U	4.95	5.21	0.195	0.205

CASE 714-03

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_A = +25°C, 75 Ω system unless otherwise noted)

Characteristic	Symbol	MHW5171A			MHW5172A			Unit
		Min	Typ	Max	Min	Typ	Max	
Frequency Range	BW	40	—	450	40	—	450	MHz
Power Gain — 50 MHz	G_p	16.9	17.4	17.9	16.9	17.4	17.9	dB
Slope	S	0	0.5	1.5	0	0.5	1.5	dB
Gain Flatness	—	—	±0.1	±0.2	—	±0.1	±0.2	dB
Return Loss — Input/Output 40–450 MHz (Z_o = 75 Ohms)	IRL/ORL	18	—	—	18	—	—	dB
Second Order Intermodulation Distortion	IMD							dB
(V_{out} = +46 dBmV per ch., Ch 2, M6, M15)		—	—	−72	—	—	−74	
(V_{out} = +46 dBmV per ch., Ch 2, M13, M22)		—	—	−72	—	—	−74	
Cross Modulation Distortion 53-Channel FLAT	XMD_{53}	—	−60	−58	—	−63	−61	dB
(V_{out} = +46 dBmV per ch.) 60-Channel FLAT	XMD_{60}	—	−59	−56	—	−62	−59	
Composite Triple Beat 53-Channel FLAT	CTB_{53}	—	−61	−58	—	−63	−61	dB
(V_{out} = +46 dBmV per ch.) 60-Channel FLAT	CTB_{60}	—	−58	−56	—	−60	−59	
DIN (European Applications Only)*								dBμV**
300 MHz — (CH V + Q − P @ W)	DIN1	—	—	125	—	—	127	
400 MHz — (CH M8 + M15 − M9 @ M14)	DIN2	—	—	124	—	—	126	
450 MHz — (CH M20 + M23 − M22 @ M21)	DIN3	—	—	123	—	—	125	
Noise Figure (f = 450 MHz)	NF	—	—	7.0	—	—	8.0	dB
DC Current (V_{DC} = 24 ±0.5 Vdc, T_C = 30°C)	I_{DC}	—	180	200	—	210	240	mA

***DIN (European Applications Only)**

NCTA Channel Designation	Frequency (MHz)	DIN Output Level (dBmV)**		DIN Beat Level dB Relative to Ref. Ch.
		MHW5171A	MHW5172A	
P	253.25	+59	+61	≤ −60
Q	259.25	+59	+61	
V	289.25	+65	+67	
W (Ref.)	295.25	+65	+67	
M8	361.25	+58	+60	≤ −60
M9	367.25	+58	+60	
M14 (Ref.)	397.25	+64	+66	
M15	403.25	+64	+66	
M20	433.25	+63	+65	≤ −60
M21 (Ref.)	439.25	+63	+65	
M22	445.25	+57	+59	
M23	451.25	+57	+59	

**DIN (dBμV) = Reference Channel Level (dBmV) + 60 dB

4

MHW5181A
MHW5182A

The RF Line

18 dB GAIN

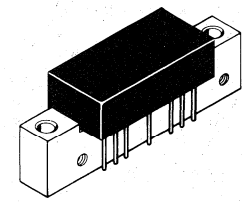
450 MHz

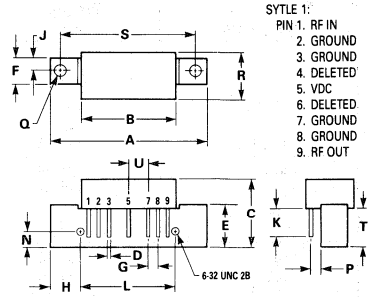
60-CHANNEL
CATV INPUT/OUTPUT
TRUNK AMPLIFIERS

450 MHz CATV AMPLIFIER MODULE

. . . designed specifically for 450 MHz CATV applications. Features ion-implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

- Specified for 53- and 60-Channel Performance
- Broadband Power Gain — @ f = 40–450 MHz
  G_p = 18.2 dB (Typ) @ 50 MHz
  19.0 dB (Typ) @ 450 MHz
- Broadband Noise Figure
  NF = 6.0 dB (Max) MHW5181A
  7.0 dB (Max) MHW5182A
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion-Implanted Transistors





SYTLE 1:
PIN 1. RF IN
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUT

NOTE:
1. MOUNTING HOLES WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.41	2.67	0.095	0.105
H	9.65	9.78	0.380	0.385
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.335
L	25.40 BSC		1.000 BSC	
N	4.06	4.32	0.160	0.170
P	2.16	2.92	0.085	0.115
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
T	11.05	11.43	0.435	0.450
U	4.95	5.21	0.195	0.205

CASE 714-03

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_A = +25°C, 75 Ω system unless otherwise noted)

Characteristic	Symbol	MHW5181A			MHW5182A			Unit
		Min	Typ	Max	Min	Typ	Max	
Frequency Range	BW	40	—	450	40	—	450	MHz
Power Gain — 50 MHz	G_p	17.8	18.2	18.6	17.8	18.2	18.6	dB
Power Gain — 450 MHz	G_p	18.5	19	20	18.5	19	20	dB
Slope	S	0.3	—	1.5	0.3	—	1.5	dB
Gain Flatness	—	—	±0.1	±0.2	—	±0.1	±0.2	dB
Return Loss — Input/Output 40–450 MHz (Z_o = 75 Ohms)	IRL/ORL	18	—	—	18	—	—	dB
Second Order Intermodulation Distortion	IMD							dB
(V_{out} = +46 dBmV per ch., Ch 2, M6, M15)		—	−80	—	—	−80	—	
(V_{out} = +46 dBmV per ch., Ch 2, M13, M22)		—	−76	−72	—	−76	−72	
Cross Modulation Distortion 53-Channel FLAT	XMD_{53}	—	−59	−56	—	−62	−59	dB
(V_{out} = +46 dBmV per ch.) 60-Channel FLAT	XMD_{60}	—	−58	−56	—	−61	−59	
Composite Triple Beat 53-Channel FLAT	CTB_{53}	—	−61	−59	—	−64	−63	dB
(V_{out} = +46 dBmV per ch.) 60-Channel FLAT	CTB_{60}	—	−58	−57	—	−62	−61	
DIN (European Applications Only)*								dBμV**
300 MHz — (CH V + Q − P @ W)	DIN1	—	—	124	—	—	126	
400 MHz — (CH M8 + M15 − M9 @ M14)	DIN2	—	—	124	—	—	126	
450 MHz — (CH M20 + M23 − M22 @ M21)	DIN3	—	—	123	—	—	125	
Noise Figure (f = 450 MHz)	NF	—	—	6.0	—	—	7.0	dB
DC Current (V_{DC} = 24 ±0.5 Vdc, T_C = 30°C)	I_{DC}	—	180	200	—	210	240	mA

*DIN (European Applications Only)

NCTA Channel Designation	Frequency (MHz)	DIN Output Level (dBmV)**		DIN Beat Level dB Relative to Ref. Ch.
		MHW5181A	MHW5182A	
P	253.25	+58	+60	≤ −60
Q	259.25	+58	+60	
V	289.25	+64	+66	
W (Ref.)	295.25	+64	+66	
M8	361.25	+58	+60	≤ −60
M9	367.25	+58	+60	
M14 (Ref.)	397.25	+64	+66	
M15	403.25	+64	+66	
M20	433.25	+63	+65	≤ −60
M21 (Ref.)	439.25	+63	+65	
M22	445.25	+57	+59	
M23	451.25	+57	+59	

**DIN (dBμV) = Reference Channel Level (dBmV) + 60 dB

4

MHW5185
MHW6185

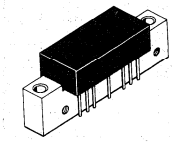
18 dB GAIN
450/550 MHz
60/77-CHANNEL
CATV AMPLIFIERS

The RF Line

High Output Doubler 450/550 MHz CATV Amplifier Modules

. . . designed specifically for 450/550 MHz CATV applications. Features ion-implanted arsenic emitter transistors with 6 to 8 GHz f_T and an all gold metallization system.

- 4th Generation Die Technology
- Specified for 60/77-Channel Performance
- Broadband Power Gain — @ f = 40–550 MHz
  G_p = 18.5 dB (Typ) @ 50 MHz
  19.0 dB (Typ) @ 450 MHz
  19.5 dB (Typ) @ 550 MHz
- Broadband Noise Figure
  NF = 5 dB (Typ) — MHW5185
  = 6 dB (Typ) — MHW6185
- Improvement in Distortion Over Conventional Hybrids
- Allows Higher Output Level Operation



CASE 714-03

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_A = +25°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range	MHW5185 MHW6185	BW	40 40	— —	450 550	MHz
Power Gain	50 MHz 450 MHz 550 MHz	G_p	18 18.5 18.8	— — —	19 19.7 20	dB
Slope		S	0.5	—	2.0	dB
Gain Flatness		—	—	±0.1	±0.2	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–550 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion (V_{out} = +46 dBmV per ch., Ch 2, M13, M22) (V_{out} = +46 dBmV per ch., Ch 2, M30, M39)	 MHW5185 MHW6185	IMD	 — —	 — —	 −74 −71	dB
Cross Modulation Distortion (V_{out} = +46 dBmV per ch.) (V_{out} = +44 dBmV per ch.)	 60-Channel FLAT 77-Channel FLAT	 XMD_{60} XMD_{77}	 — —	 −68 −66	 −66 −63	dB
Composite Triple Beat (V_{out} = +46 dBmV per ch.) (V_{out} = +44 dBmV per ch.)	 60-Channel FLAT 77-Channel FLAT	 CTB_{60} CTB_{77}	 — —	 −66 −63	 −65 −62	dB
DIN (European Applications Only)* 300 MHz — (CH V + Q − P @ W) 400 MHz — (CH M8 + M15 − M9 @ M14) 450 MHz — (CH M20 + M23 − M22 @ M21)	MHW5185	 DIN1 DIN2 DIN3	 — — —	 — — —	 129 128 126	dBμV**
Noise Figure	450 MHz 550 MHz	NF	— 8	5.0 6.0	7.0 8.0	dB
DC Current (V_{DC} = 24 ±0.5 Vdc, T_C = 30°C)		I_{DC}	—	385	435	mA

*DIN (European Applications Only)

NCTA Channel Designation	Frequency (MHz)	DIN Output Level (dBmV)** MHW5185	DIN Beat Level dB Relative to Ref. Ch.
P	253.25	+63	≤ −60
Q	259.25	+63	
V	289.25	+69	
W (Ref.)	295.25	+69	
M8	361.25	+62	≤ −60
M9	367.25	+62	
M14 (Ref.)	397.25	+68	
M15	403.25	+68	
M20	433.25	+66	≤ −60
M21 (Ref.)	439.25	+66	
M22	445.25	+60	
M23	451.25	+60	

**DIN (dBμV) = Reference Channel Level (dBmV) + 60 dB

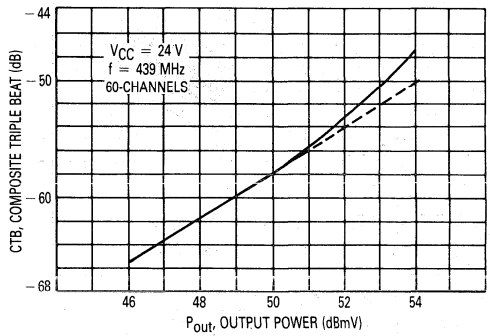


Figure 1. CTB versus Output Power

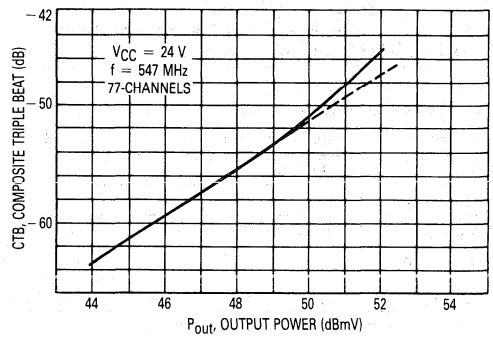


Figure 2. CTB versus Output Power

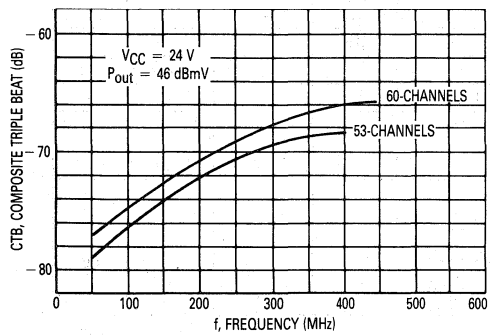


Figure 3. CTB versus Frequency/Channels

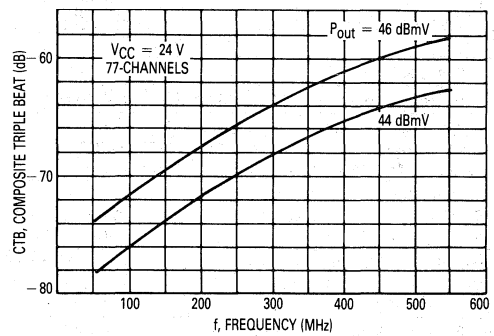


Figure 4. CTB versus Frequency/Output Power

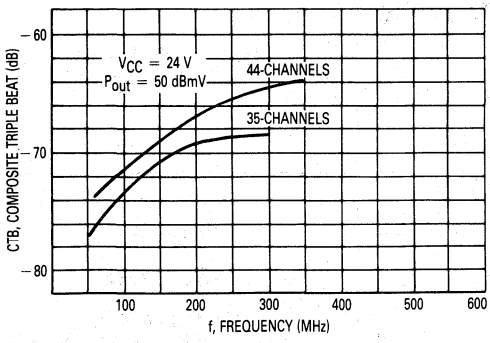


Figure 5. CTB versus Frequency/Channels

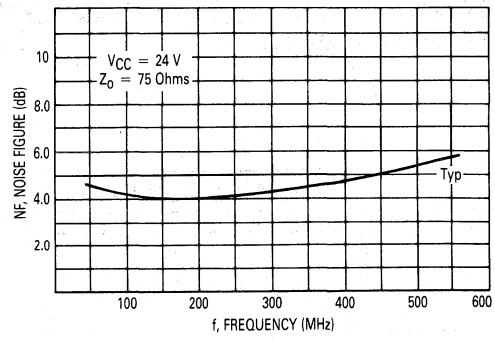


Figure 6. NF versus Frequency

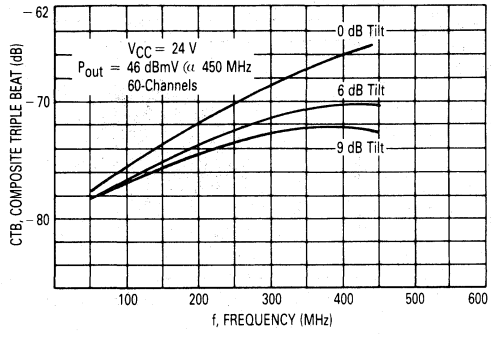


Figure 7. CTB versus Frequency/Tilt

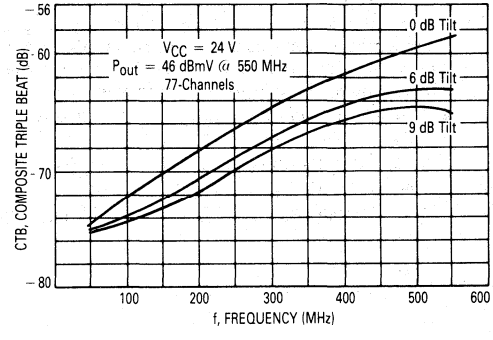


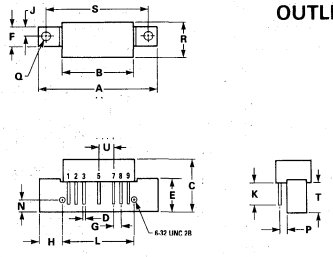
Figure 8. CTB versus Frequency/Tilt

Table 1. Functional Performance versus Temperature*

Parameter	Condition	Symbol	T1 –20°C	T2 35°C	T3 80°C	Units
Power Gain	50 MHz	G_{p1}	17.70	17.63	17.54	dB
Power Gain	450 MHz	G_{p2}	18.34	18.22	18.14	dB
Power Gain	550 MHz	G_{p3}	18.63	18.40	18.24	dB
Composite Triple Beat	V_{out} = +46 dBmV 60-Ch FLAT	CTB_{60}	– 66.1	– 64.9	– 62.9	dB
Composite Triple Beat	V_{out} = +46 dBmV 77-Ch FLAT	CTB_{77}	– 59.3	– 57.7	– 56.5	dB
DC Current	V_{DC} = 24 V	I_{DC}	370	401	419	mA

*Data in Table 1 is the average value of several parts and is only intended to show typical trends in performance as a function of temperature. Absolute values of specific parameters will comply with limits specified under "ELECTRICAL CHARACTERISTICS."

OUTLINE DIMENSION



SYTLE 1:
PIN 1. RF IN
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUT

NOTE:
1. MOUNTING HOLES WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.41	2.67	0.095	0.105
H	9.65	9.78	0.380	0.385
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.335
L	25.40 BSC		1.000 BSC	
N	4.06	4.32	0.160	0.170
P	2.16	2.92	0.085	0.115
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
T	11.05	11.43	0.435	0.450
U	4.95	5.21	0.195	0.205

CASE 714-03

MHW5222A

The RF Line

22 dB GAIN

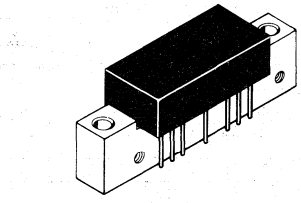
450 MHz

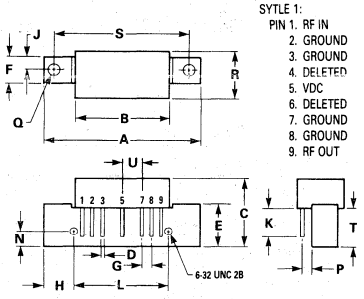
60-CHANNEL
CATV TRUNK AMPLIFIER

450 MHz CATV AMPLIFIER MODULE

. . . designed for broadband applications requiring low distortion characteristics. Specifically intended for CATV market requirements. Features ion-implanted arsenic emitter transistors with 7.0 GHz f_T, and all an gold metallization system.

- Broadband Power Gain — @ f = 40–450 MHz
  G_p = 22 dB (Typ)
- Broadband Noise Figure — @ f = 450 MHz
  NF = 6.5 dB (Typ)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion-Implanted Transistors





SYTLE 1:
PIN 1. RF IN
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUT

NOTE:
1. MOUNTING HOLES WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.41	2.67	0.095	0.105
H	9.65	9.78	0.380	0.385
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.335
L	25.40 BSC		1.000 BSC	
N	4.06	4.32	0.160	0.170
P	2.16	2.92	0.085	0.115
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
T	11.05	11.43	0.435	0.450
U	4.95	5.21	0.195	0.205

CASE 714-03

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

4

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_A = +25°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	450	MHz
Power Gain — 50 MHz		G_p	21.5	22	22.5	dB
Slope		S	0	0.5	1.5	dB
Gain Flatness		—	—	±0.1	±0.2	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–450 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion		IMD				dB
(V_{out} = +46 dBmV per ch., Ch 2, M6, M15)			—	—	−72	
(V_{out} = +46 dBmV per ch., Ch 2, M13, M22)			—	—	−72	
Cross Modulation Distortion	53-Channel FLAT	XMD_{53}	—	−59	−56	dB
(V_{out} = +46 dBmV per ch.)	60-Channel FLAT	XMD_{60}		−58	−55	
Composite Triple Beat	53-Channel FLAT	CTB_{53}	—	−62	−60	dB
(V_{out} = +46 dBmV per ch.)	60-Channel FLAT	CTB_{60}	—	−60	−58	
DIN (European Applications Only)*						dBμV**
300 MHz — (CH V + Q − P @ W)		DIN1	—	—	125.5	
400 MHz — (CH M8 + M15 − M9 @ M14)		DIN2	—	—	125	
450 MHz — (CH M20 + M23 − M22 @ M21)		DIN3	—	—	124	
Noise Figure (f = 450 MHz)		NF	—	6.5	8.0	dB
DC Current (V_{DC} = 24 ±0.5 Vdc, T_C = 30°C)		I_{DC}	—	210	240	mA

***DIN (European Applications Only)**

NCTA Channel Designation	Frequency (MHz)	DIN Output Level (dBmV)**	DIN Beat Level dB Relative to Ref. Ch.
P	253.25	+59.5	≤ −60
Q	259.25	+59.5	
V	289.25	+65.5	
W (Ref.)	295.25	+65.5	
M8	361.25	+59	≤ −60
M9	367.25	+59	
M14 (Ref.)	397.25	+65	
M15	403.25	+65	
M20	433.25	+64	≤ −60
M21 (Ref.)	439.25	+64	
M22	445.25	+58	
M23	451.25	+58	

**DIN (dBμV) = Reference Channel Level (dBmV) + 60 dB

MHW5272A

The RF Line

27 dB GAIN

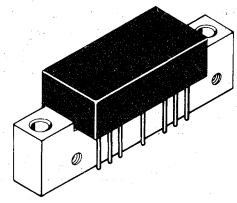
450 MHz

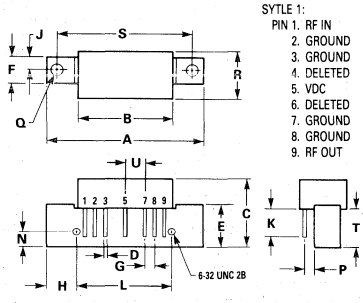
60-CHANNEL
CATV LINE EXTENDER
AMPLIFIERS

450 MHz CATV AMPLIFIER MODULE

. . . designed specifically for 450 MHz CATV applications. Features ion-implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

- Specified for 53- and 60-Channel Performance
- Broadband Power Gain — @ f = 40–450 MHz
  G_p = 27 dB (Typ)
- Broadband Noise Figure
  NF = 5.0 dB (Typ)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion-Implanted Transistors





SYTLE 1:
PIN 1. RF IN
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUT

NOTE:
1. MOUNTING HOLES WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.41	2.67	0.095	0.105
H	9.65	9.78	0.380	0.385
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.335
L	25.40 BSC		1.000 BSC	
N	4.06	4.32	0.160	0.170
P	2.16	2.92	0.085	0.115
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
T	11.05	11.43	0.435	0.450
U	4.95	5.21	0.195	0.205

CASE 714-03

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

4

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_A = +25°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	450	MHz
Power Gain — 50 MHz		G_p	26.2	27	27.8	dB
Slope		S	0	+1.0	+2.5	dB
Gain Flatness		—	—	±0.2	±0.4	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–450 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion (V_{out} = +48 dBmV per ch., Ch 2, 13, R) (V_{out} = +46 dBmV per ch., Ch 2, M6, M15)		IMD	 — —	 −80 −78	— −70	dB
Cross Modulation Distortion (V_{out} = +46 dBmV per ch.)	53-Channel FLAT 60-Channel FLAT	XMD_{53} XMD_{60}	— —	−63 −61	−62 −60	dB
Composite Triple Beat (V_{out} = +46 dBmV per ch.)	53-Channel FLAT 60-Channel FLAT	CTB_{53} CTB_{60}	— —	−63 −61	−62 −60	dB
DIN (European Applications Only)* 300 MHz — (CH V + Q − P @ W) 400 MHz — (CH M8 + M15 − M9 @ M14) 450 MHz — (CH M20 + M23 − M22 @ M21)		 DIN1 DIN2 DIN3	 — — —	 — — —	 126 125 124	dBμV**
Noise Figure (f = 450 MHz)		NF	—	5.0	6.0	dB
DC Current (V_{DC} = 24 ±0.5 Vdc, T_C = 30°C)		I_{DC}	—	310	340	mA

***DIN (European Applications Only)**

NCTA Channel Designation	Frequency (MHz)	DIN Output Level (dBmV)**	DIN Beat Level dB Relative to Ref. Ch.
P	253.25	+60	≤−60
Q	259.25	+60	
V	289.25	+66	
W (Ref.)	295.25	+66	
M8	361.25	+59	≤−60
M9	367.25	+59	
M14 (Ref.)	397.25	+65	
M15	403.25	+65	
M20	433.25	+64	≤−60
M21 (Ref.)	439.25	+64	
M22	445.25	+58	
M23	451.25	+58	

**DIN (dBμV) = Reference Channel Level (dBmV) + 60 dB

4

MHW5332A

The RF Line

33 dB GAIN

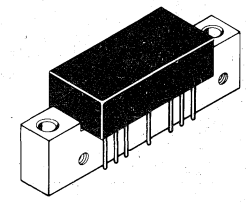
450 MHz

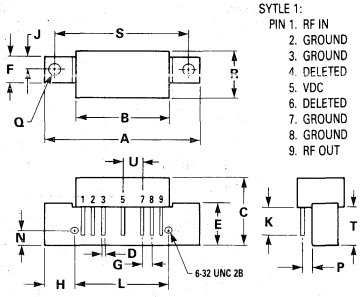
60-CHANNEL
CATV LINE EXTENDER
AMPLIFIERS

450 MHz CATV AMPLIFIER MODULE

. . . designed specifically for 450 MHz CATV applications. Features ion-implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

- Specified for 53- and 60-Channel Performance
- Broadband Power Gain — @ f = 40–450 MHz
  G_p = 33 dB (Typ)
- Broadband Noise Figure
  NF = 5.0 dB (Typ)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion-Implanted Transistors





SYTLE 1:
PIN 1. RF IN
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUT

NOTE:
1. MOUNTING HOLES WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.41	2.67	0.095	0.105
H	9.65	9.78	0.380	0.38b
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.335
L	25.40 BSC		1.000 BSC	
N	4.06	4.32	0.160	0.170
P	2.16	2.92	0.085	0.115
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
T	11.05	11.43	0.435	0.450
U	4.95	5.21	0.195	0.205

CASE 714-03

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

4

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +25°C, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	450	MHz
Power Gain — 50 MHz	G_p	32	33	34	dB
Slope	S	0	+1.0	2.0	dB
Gain Flatness	—	—	±0.2	±0.4	dB
Return Loss — Input/Output 40–450 MHz (Z_o = 75 Ohms)	IRL/ORL	20	—	—	dB
Second Order Intermodulation Distortion	IMD				dB
(V_{out} = +46 dBmV, Ch 2, M6, M15)		—	−80	−72	
(V_{out} = +46 dBmV, Ch 2, M13, M22)		—	−78	−70	
Cross Modulation Distortion 53-Channel FLAT	XMD_{53}	—	−63	−61	dB
(V_{out} = +46 dBmV) 60-Channel FLAT	XMD_{60}	—	−61	−59	
Composite Triple Beat 53-Channel FLAT	CTB_{53}	—	−63	−62	dB
(V_{out} = +46 dBmV) 60-Channel FLAT	CTB_{60}	—	−61	−60	
DIN (European Applications Only)*					dBμV**
300 MHz — (CH V + Q − P @ W)	DIN1	—	—	126	
400 MHz — (CH M8 + M15 − M9 @ M14)	DIN2	—	—	125	
450 MHz — (CH M20 + M23 − M22 @ M21)	DIN3	—	—	124	
Noise Figure (f = 450 MHz)	NF	—	5.0	6.0	dB
DC Current (V_{DC} = 24 ±0.5 Vdc, T_C = 30°C)	I_{DC}	—	310	340	mA

***DIN (European Applications Only)**

NCTA Channel Designation	Frequency (MHz)	DIN Output Level (dBmV)**	DIN Beat Level dB Relative to Ref. Ch.
P	253.25	+60	≤ −60
Q	259.25	+60	
V	289.25	+66	
W (Ref.)	295.25	+66	
M8	361.25	+59	≤ −60
M9	367.25	+59	
M14 (Ref.)	397.25	+65	
M15	403.25	+65	
M20	433.25	+64	≤ −60
M21 (Ref.)	439.25	+64	
M22	445.25	+58	
M23	451.25	+58	

**DIN (dBμV) = Reference Channel Level (dBmV) + 60 dB

4

MHW5342A

The RF Line

34 dB GAIN

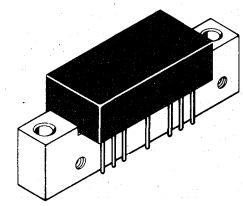
450 MHz

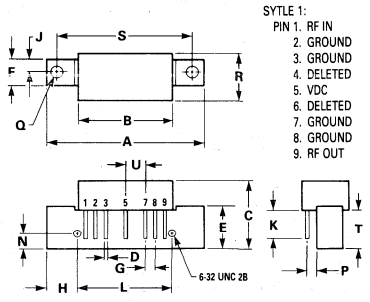
60-CHANNEL
CATV LINE EXTENDER
AMPLIFIERS

450 MHz CATV AMPLIFIER MODULE

. . . designed specifically for 450 MHz CATV applications. Features ion-implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

- Specified for 53- and 60-Channel Performance
- Broadband Power Gain — @ f = 40–450 MHz
  G_p = 34 dB (Typ)
- Broadband Noise Figure
  NF = 5.0 dB (Typ)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion-Implanted Transistors





SYTLE 1:
PIN 1. RF IN
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUT

NOTE:
1. MOUNTING HOLES WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.41	2.67	0.095	0.105
H	9.65	9.78	0.380	0.385
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.335
L	25.40 BSC		1.000 BSC	
N	4.06	4.32	0.160	0.170
P	2.16	2.92	0.085	0.115
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
T	11.05	11.43	0.435	0.450
U	4.95	5.21	0.195	0.205

CASE 714-03

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

4

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_A = +25°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	450	MHz
Power Gain — 50 MHz		G_p	33	34	35	dB
Slope		S	0	+1.0	+2.5	dB
Gain Flatness		—	—	±0.2	±0.4	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–450 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion (V_{out} = +48 dBmV per ch., Ch 2, 13, R) (V_{out} = +46 dBmV per ch., Ch 2, M6, M15)		IMD	 — —	 −80 −78	— −70	dB
Cross Modulation Distortion (V_{out} = +46 dBmV per ch.)	53-Channel FLAT 60-Channel FLAT	XMD_{53} XMD_{60}	— —	−63 −61	−61 −59	dB
Composite Triple Beat (V_{out} = +46 dBmV per ch.)	53-Channel FLAT 60-Channel FLAT	CTB_{53} CTB_{60}	— —	−63 −60	−61 −59	dB
DIN (European Applications Only)* 300 MHz — (CH V + Q − P @ W) 400 MHz — (CH M8 + M15 − M9 @ M14) 450 MHz — (CH M20 + M23 − M22 @ M21)		 DIN1 DIN2 DIN3	 — — —	 — — —	 126 125 124	dBμV**
Noise Figure (f = 450 MHz)		NF	—	5.0	5.5	dB
DC Current (V_{DC} = 24 ±0.5 Vdc, T_C = 30°C)		I_{DC}	—	310	340	mA

***DIN (European Applications Only)**

NCTA Channel Designation	Frequency (MHz)	DIN Output Level (dBmV)**	DIN Beat Level dB Relative to Ref. Ch.
P	253.25	+60	≤ −60
Q	259.25	+60	
V	289.25	+66	
W (Ref.)	295.25	+66	
M8	361.25	+59	≤ −60
M9	367.25	+59	
M14 (Ref.)	397.25	+65	
M15	403.25	+65	
M20	433.25	+64	≤ −60
M21 (Ref.)	439.25	+64	
M22	445.25	+58	
M23	451.25	+58	

**DIN (dBμV) = Reference Channel Level (dBmV) + 60 dB

4

MHW5382A

The RF Line

38 dB GAIN

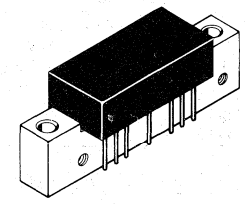
450 MHz

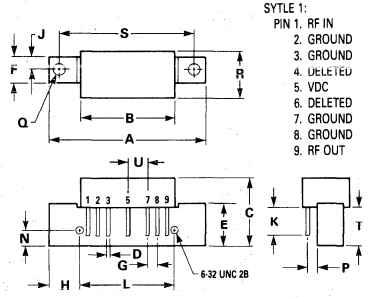
60-CHANNEL
CATV LINE EXTENDER
AMPLIFIERS

450 MHz CATV AMPLIFIER MODULE

. . . designed specifically for 450 MHz CATV applications. Features ion-implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

- Specified for 53- and 60-Channel Performance
- Broadband Power Gain — @ f = 40–450 MHz
  G_p = 38 dB (Typ)
- Broadband Noise Figure
  NF = 5.0 dB (Typ)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion-Implanted Transistors





SYTLE 1:
PIN 1. RF IN
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUT

NOTE:
1. MOUNTING HOLES WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.41	2.67	0.095	0.105
H	9.65	9.78	0.380	0.385
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.335
L	25.40 BSC		1.000 BSC	
N	4.06	4.32	0.160	0.170
P	2.16	2.92	0.085	0.115
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
T	11.05	11.43	0.435	0.450
U	4.95	5.21	0.195	0.205

CASE 714-03

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

4

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_A = +25°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	450	MHz
Power Gain — 50 MHz		G_p	37	38	39	dB
Slope		S	0	+1.0	+2.5	dB
Gain Flatness		—	—	±0.2	±0.4	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–450 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion		IMD			—	dB
(V_{out} = +48 dBmV per ch., Ch 2, 13, R)			—	−80	−70	
(V_{out} = +46 dBmV per ch., Ch 2, M6, M15)			—	−78		
Cross Modulation Distortion	53-Channel FLAT	XMD_{53}	—	−63	−61	dB
(V_{out} = +46 dBmV per ch.)	60-Channel FLAT	XMD_{60}	—	−61	−59	
Composite Triple Beat	53-Channel FLAT	CTB_{53}	—	−63	−61	dB
(V_{out} = +46 dBmV per ch.)	60-Channel FLAT	CTB_{60}	—	−60	−59	
DIN (European Applications Only)*						dBμV**
300 MHz — (CH V + Q − P @ W)		DIN1	—	—	125	
400 MHz — (CH M8 + M15 − M9 @ M14)		DIN2	—	—	124	
450 MHz — (CH M20 + M23 − M22 @ M21)		DIN3	—	—	123	
Noise Figure (f = 450 MHz)		NF	—	5.0	5.5	dB
DC Current (V_{DC} = 24 ±0.5 Vdc, T_C = 30°C)		I_{DC}	—	310	340	mA

***DIN (European Applications Only)**

NCTA Channel Designation	Frequency (MHz)	DIN Output Level (dBmV)**	DIN Beat Level dB Relative to Ref. Ch.
P	253.25	+59	≤ −60
Q	259.25	+59	
V	289.25	+65	
W (Ref.)	295.25	+65	
M8	361.25	+58	≤ −60
M9	367.25	+58	
M14 (Ref.)	397.25	+64	
M15	403.25	+64	
M20	433.25	+57	≤ −60
M21 (Ref.)	439.25	+57	
M22	445.25	+63	
M23	451.25	+63	

**DIN (dBμV) = Reference Channel Level (dBmV) + 60 dB

4

MHW6122

The RF Line

12 dB GAIN

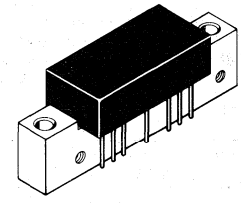
550 MHz

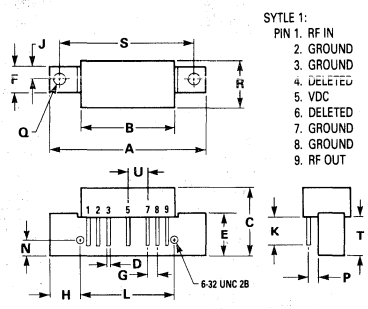
77-CHANNEL CATV INPUT/OUTPUT TRUNK AMPLIFIER

550 MHz CATV AMPLIFIER MODULE

. . . designed specifically for 550 MHz CATV applications. Features ion-implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

- Specified for 77-Channel Performance
- Broadband Power Gain — @ f = 40–550 MHz
  G_p = 12.5 dB (Typ) @ 50 MHz
  13 dB (Min) @ 550 MHz
- Broadband Noise Figure @ 550 MHz
  NF = 8.5 dB (Max) MHW6122
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion-Implanted Transistors





SYTLE 1:
PIN 1. RF IN
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUT

NOTE:
1. MOUNTING HOLES WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.41	2.67	0.095	0.105
H	9.65	9.78	0.380	0.385
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.335
L	25.40 BSC		1.000 BSC	
N	4.06	4.32	0.160	0.170
P	2.16	2.92	0.085	0.115
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
T	11.05	11.43	0.435	0.450
U	4.95	5.21	0.195	0.205

CASE 714-03

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

4

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_A = +35°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	550	MHz
Power Gain — 50 MHz		G_p	12	12.5	13	dB
Power Gain — 550 MHz		G_p	14.5	—	—	dB
Slope		S	0.2	—	1.5	dB
Gain Flatness		—	—	±0.1	±0.2	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–550 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion		IMD				dB
(V_{out} = +46 dBmV per ch., Ch 2, M13, M22)			—	—	−72	
(V_{out} = +46 dBmV per ch., Ch 2, M30, M39)			—	—	−72	
Cross Modulation Distortion						dB
(V_{out} = +46 dBmV per ch.)	60-Channel FLAT	XMD_{60}	—	−63	—	
(V_{out} = +44 dBmV per ch.)	77-Channel FLAT	XMD_{77}	—	−65	−62	
Composite Triple Beat						dB
(V_{out} = +46 dBmV per ch.)	60-Channel FLAT	CTB_{60}	—	−59	—	
(V_{out} = +44 dBmV per ch.)	77-Channel FLAT	CTB_{77}	—	−57	−56	
Noise Figure (f = 550 MHz)		NF	—	—	8.5	dB
DC Current (V_{DC} = 24 ±0.5 Vdc, T_C = 30°C)		I_{DC}	—	210	240	mA

4

MHW6141
MHW6142

The RF Line

550 MHz CATV AMPLIFIER MODULE

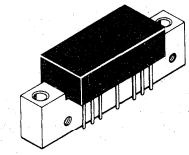
. . . designed specifically for 550 MHz CATV applications. Features ion-implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

- Specified for >77 Channel Performance
- Broadband Power Gain — @ f = 40–550 MHz
  G_p = 14 dB (Typ) @ 50 MHz
  14.5 dB (Min) @ 550 MHz
- Broadband Noise Figure
  NF = 7.5 dB (Max) MHW6141
  8.5 dB (Max) MHW6142
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion-Implanted Transistors

14 dB GAIN

550 MHz

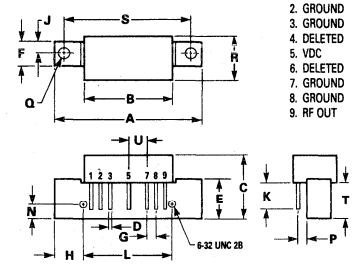
77-CHANNEL CATV INPUT/OUTPUT TRUNK AMPLIFIERS



4

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C



SYTLE 1:
PIN 1. RF IN
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUT

NOTE:
1. MOUNTING HOLES WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.41	2.67	0.095	0.105
H	9.65	9.78	0.380	0.385
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.335
L	25.40 BSC		1.000 BSC	
N	4.06	4.32	0.160	0.170
P	2.16	2.92	0.085	0.115
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
T	11.05	11.43	0.435	0.450
U	4.95	5.21	0.195	0.205

CASE 714-03

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +35°C, 75 Ω system unless otherwise noted)

Characteristic	Symbol	MHW6141			MHW6142			Unit
		Min	Typ	Max	Min	Typ	Max	
Frequency Range	BW	40	—	550	40	—	550	MHz
Power Gain — 50 MHz	G_p	13.5	14	14.5	13.5	14	14.5	dB
Power Gain — 550 MHz	G_p	14.5	—	—	14.5	—	—	dB
Slope	S	0.2	—	1.5	0.2	—	1.5	dB
Gain Flatness	—	—	±0.1	±0.2	—	±0.1	±0.2	dB
Return Loss — Input/Output 40–550 MHz (Z_o = 75 Ohms)	IRL/ORL	18	—	—	18	—	—	dB
Second Order Intermodulation Distortion	IMD							dB
(V_{out} = +46 dBmV per ch., Ch 2, M13, M22)		—	—	−70	—	—	−72	
(V_{out} = +46 dBmV per ch., Ch 2, M30, M39)		—	—	−70	—	—	−72	
Cross Modulation Distortion								dB
(V_{out} = +46 dBmV per ch.) 60-Channel FLAT	XMD_{60}	—	−61	—	—	−64	—	
(V_{out} = +44 dBmV per ch.) 77-Channel FLAT	XMD_{77}	—	−62	−59	—	−65	−62	
Composite Triple Beat								dB
(V_{out} = +46 dBmV per ch.) 60-Channel FLAT	CTB_{60}	—	−59	—	—	−61	—	
(V_{out} = +44 dBmV per ch.) 77-Channel FLAT	CTB_{77}	—	−58	−56	—	−60	−59	
Noise Figure (f = 550 MHz)	NF	—	—	7.5	—	—	8.5	dB
DC Current (V_{DC} = 24 ±0.5 Vdc, T_C = 30°C)	I_{DC}	—	180	200	—	210	240	mA

4

MHW6171
MHW6172

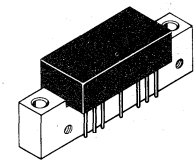
17 dB GAIN
550 MHz
77-CHANNEL
CATV AMPLIFIERS

The RF Line

77-Channel (550 MHz) CATV Input/Output Trunk Amplifiers

. . . designed specifically for 550 MHz CATV applications. Features ion-implanted arsenic emitter transistors with 7 GHz f_T and an all gold metallization system.

- Specified for 77-Channel Performance
- Broadband Power Gain — @ f = 40–550 MHz
  G_p = 17.2 dB (Typ)
- Broadband Noise Figure — @ f = 550 MHz
  NF = 5.5 dB (Typ) MHW6171
  6 dB (Typ) MHW6172
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz Ion-Implanted Transistors



CASE 714-03

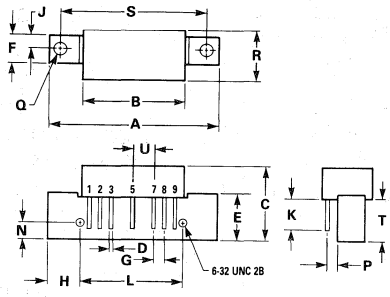
ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−60 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_A = +25°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	MHW6171			MHW6172			Unit
			Min	Typ	Max	Min	Typ	Max	
Frequency Range		BW	40	—	550	40	—	550	MHz
Power Gain	50 MHz	G_p	16.7	17.2	17.6	16.7	17.2	17.6	dB
Slope		S	0	+0.5	+1.5	0	+0.5	+1.5	dB
Gain Flatness		—	—	±0.1	±0.2	—	±0.1	±0.2	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–550 MHz	IRL/ORL	18	—	—	18	—	—	dB
Second Order Intermodulation		IMD							dB
(V_{out} = +46 dBmV per ch., Ch 2, M13, M22)			—	—	−70	—	—	−72	
(V_{out} = +44 dBmV per ch., Ch 2, M30, M39)			—	—	−68	—	—	−70	
Cross Modulation Distortion									dB
(V_{out} = +46 dBmV per ch.)	60-Channel FLAT	XMD_{60}	—	−60	—	—	−63	—	
(V_{out} = +44 dBmV per ch.)	77-Channel FLAT	XMD_{77}	—	−62	−59	—	−65	−62	
Composite Triple Beat Noise									dB
(V_{out} = +46 dBmV per ch.)	60-Channel FLAT	CTB_{60}	—	−60	—	—	−62	—	
(V_{out} = +44 dBmV per ch.)	77-Channel FLAT	CTB_{77}	—	−58	−56	—	−60	−59	
Noise Figure		NF							dB
	400 MHz		—	5.5	—	—	6	—	
	450 MHz		8	6	7	—	6.5	8	
DC Current (V_{DC} = 24 ±0.5 Vdc, T_C = 30°C)		I_{DC}	—	180	200	—	210	240	mA

OUTLINE DIMENSIONS



SYTLE 1:
PIN 1. RF IN
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUT

NOTE:
1. MOUNTING HOLES WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.41	2.67	0.095	0.105
H	9.65	9.78	0.380	0.385
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.335
L	25.40 BSC		1.000 BSC	
N	4.06	4.32	0.160	0.170
P	2.16	2.92	0.085	0.115
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
T	11.05	11.43	0.435	0.450
U	4.95	5.21	0.195	0.205

CASE 714-03

4

MHW6181
MHW6182

The RF Line

550 MHz CATV AMPLIFIER MODULE

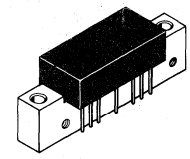
. . . designed specifically for 550 MHz CATV applications. Features ion-implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

- Specified for >77 Channel Performance
- Broadband Power Gain — @ f = 40–550 MHz
  G_p = 18.2 dB (Typ) @ 50 MHz
  G_p = 18.8 dB (Min) @ 550 MHz
- Broadband Noise Figure @ 550 MHz
  NF = 7.0 dB (Max) MHW6181
  8.0 dB (Max) MHW6182
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion-Implanted Transistors

18 dB GAIN

550 MHz

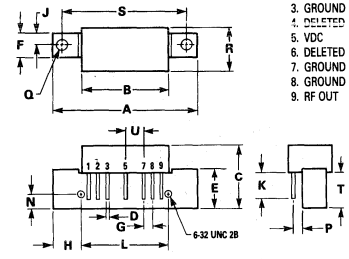
77-CHANNEL CATV INPUT/OUTPUT TRUNK AMPLIFIERS



4

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C



SYTLE 1:
PIN 1. RF IN
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUT

NOTE:
1. MOUNTING HOLES WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.41	2.67	0.095	0.105
H	9.65	9.78	0.380	0.385
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.335
L	25.40 BSC		1.000 BSC	
N	4.06	4.32	0.160	0.170
P	2.16	2.92	0.085	0.115
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
T	11.05	11.43	0.435	0.450
U	4.95	5.21	0.195	0.205

CASE 714-03

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +35°C, 75 Ω system unless otherwise noted)

Characteristic	Symbol	MHW6181			MHW6182			Unit
		Min	Typ	Max	Min	Typ	Max	
Frequency Range	BW	40	—	550	40	—	550	MHz
Power Gain — 50 MHz	G_p	17.7	18.2	18.7	17.7	18.2	18.7	dB
Power Gain — 550 MHz	G_p	18.8	19.2	20	18.8	19.2	20	dB
Slope	S	0.5	—	2.0	0.5	—	2.0	dB
Gain Flatness	—	—	±0.1	±0.2	—	±0.1	±0.2	dB
Return Loss — Input/Output 40–550 MHz (Z_o = 75 Ohms)	IRL/ORL	18	—	—	18	—	—	dB
Second Order Intermodulation Distortion	IMD							dB
(V_{out} = +46 dBmV per ch., Ch 2, M13, M22)		—	—	−72	—	—	−72	
(V_{out} = +46 dBmV per ch., Ch 2, M30, M39)		—	—	−70	—	—	−72	
Cross Modulation Distortion								dB
(V_{out} = +46 dBmV per ch.) 60-Channel FLAT	XMD_{60}	—	−58	—	—	−61	—	
(V_{out} = +44 dBmV per ch.) 77-Channel FLAT	XMD_{77}	—	−62	−59	—	−65	−62	
Composite Triple Beat								dB
(V_{out} = +46 dBmV per ch.) 60-Channel FLAT	CTB_{60}	—	−58	—	—	−61	—	
(V_{out} = +44 dBmV per ch.) 77-Channel FLAT	CTB_{77}	—	−58	−56	—	−60	−58	
Noise Figure (f = 550 MHz)	NF	—	—	7.0	—	—	8.0	dB
DC Current (V_{DC} = 24 ±0.5 Vdc, T_C = 30°C)	I_{DC}	—	180	200	—	210	240	mA

4

MHW6222

The RF Line

22 dB GAIN

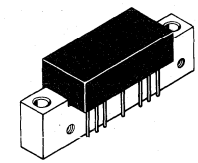
550 MHz

77-CHANNEL
CATV INPUT/OUTPUT
TRUNK AMPLIFIERS

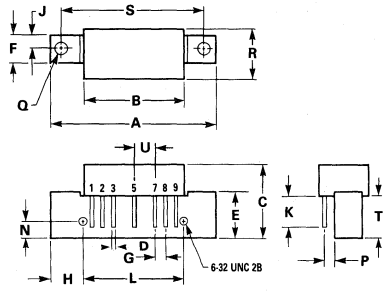
550 MHz CATV AMPLIFIER MODULE

. . . designed specifically for 550 MHz CATV applications. Features ion-implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

- Specified for 77-Channel Performance
- Broadband Power Gain — @ f = 40–550 MHz
  G_p = 22 dB (Typ) @ 50 MHz
  22 dB (Min) @ 550 MHz
- Broadband Noise Figure @ 550 MHz
  NF = 7.0 dB (Max)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion-Implanted Transistors



CASE 714-03



SYTLE 1:
PIN 1. RF IN
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUT

NOTE:
1. MOUNTING HOLES WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.41	2.67	0.095	0.105
H	9.65	9.78	0.380	0.385
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.335
L	25.40 BSC		1.000 BSC	
N	4.06	4.32	0.160	0.170
P	2.16	2.92	0.085	0.115
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
T	11.05	11.43	0.435	0.450
U	4.95	5.21	0.195	0.205

CASE 714-03

4

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+60	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +35°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	550	MHz
Power Gain — 50 MHz		G_p	21.5	22	22.5	dB
Power Gain — 550 MHz		G_p	22	—	—	dB
Slope		S	0.2	—	1.5	dB
Gain Flatness		—	—	±0.15	±0.2	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–550 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion		IMD				dB
(V_{out} = +46 dBmV per ch., Ch 2, M13, M22)			—	—	−68	
(V_{out} = +44 dBmV per ch., Ch 2, M30, M39)			—	—	−64	
Cross Modulation Distortion						dB
(V_{out} = +46 dBmV per ch.)	60-Channel FLAT	XMD_{60}	—	−62	—	
(V_{out} = +44 dBmV per ch.)	77-Channel FLAT	XMD_{77}	—	−58	−57	
Composite Triple Beat						dB
(V_{out} = +46 dBmV per ch.)	60-Channel FLAT	CTB_{60}	—	−62	—	
(V_{out} = +44 dBmV per ch.)	77-Channel FLAT	CTB_{77}	—	−59	−57	
Noise Figure (f = 550 MHz)		NF	—	—	7.0	dB
DC Current (V_{DC} = 24 ±0.5 Vdc, T_C = 30°C)		I_{DC}	—	210	240	mA

4

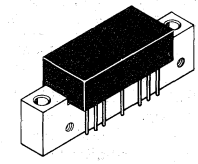
MHW6272

27 dB GAIN
550 MHz
77-CHANNEL
CATV AMPLIFIER

The RF Line

77-Channel (550 MHz) CATV Line Extender Amplifier

- Specified for 60- and 77-Channel Performance
- Broadband Power Gain — @ f = 40–550 MHz
  G_p = 27 dB (Typ)
- Broadband Noise Figure
  NF = 6 dB (Typ) @ 550 MHz
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz f_T Ion-Implanted Transistors



CASE 714-03

ABSOLUTE MAXIMUM RATINGS

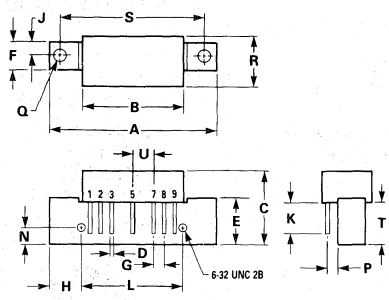
Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_A = +25°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	550	MHz
Power Gain	50 MHz 550 MHz	G_p	26.2 27	27 —	27.8 —	dB
Slope		S	0	+1	2	dB
Gain Flatness		—	—	±0.2	±0.4	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–550 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion (V_{out} = +48 dBmV per ch., Ch 2, 13, R) (V_{out} = +46 dBmV per ch., Ch 2, M6, M15) (V_{out} = +46 dBmV per ch., Ch 2, M13, M22) (V_{out} = +44 dBmV per ch., Ch 2, M30, M39)		IMD	 — — — —	 −80 −78 — —	 — — −68 −68	dB
Cross Modulation Distortion (V_{out} = +46 dBmV per ch.) (V_{out} = +44 dBmV per ch.)	 53-Channel FLAT 60-Channel FLAT 70-Channel FLAT 77-Channel FLAT	 XMD_{53} XMD_{60} XMD_{70} XMD_{77}	 — — — —	 −63 −61 −61 −59	 — −60 — −57	dB
Composite Triple Beat (V_{out} = +46 dBmV per ch.) (V_{out} = +44 dBmV per ch.)	 53-Channel FLAT 60-Channel FLAT 70-Channel FLAT 77-Channel FLAT	 TB_{53} TB_{60} TB_{70} TB_{77}	 — — — —	 −63 −61 −61 −59	 — −60 — −57	dB
Noise Figure	550 MHz	NF	—	6.0	6.5	dB
DC Current (V_{DC} = 24 ±0.5 Vdc, T_C = 30°C)		I_{DC}	—	310	340	mA

4

OUTLINE DIMENSIONS



SYTLE 1:
PIN 1. RF IN
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUT

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.41	2.67	0.095	0.105
H	9.65	9.78	0.380	0.385
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.335
L	25.40 BSC		1.000 BSC	
N	4.06	4.32	0.160	0.170
P	2.16	2.92	0.085	0.115
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
T	11.05	11.43	0.435	0.450
U	4.95	5.21	0.195	0.205

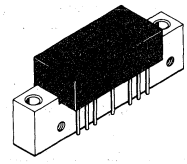
NOTE:
1. MOUNTING HOLES WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

CASE 714-03

4

MHW6342

**34 dB GAIN
550 MHz
77-CHANNEL
CATV AMPLIFIER**



CASE 714-03

The RF Line

77-Channel (550 MHz) CATV Amplifier Module

. . . designed specifically for 550 MHz CATV applications. Features ion-implanted arsenic emitter transistors with 7 GHz f_T and an all gold metallization system.

- Specified for 77-Channel Performance
- Broadband Power Gain — @ f = 40–550 MHz
  G_p = 34.5 dB (Typ) @ 50 MHz
  35 dB (Min) @ 550 MHz
- Broadband Noise Figure @ 550 MHz
  NF = 6 dB (Typ)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz Ion-Implanted Transistors

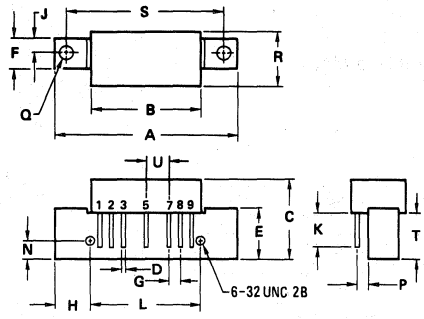
ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +35°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	550	MHz
Power Gain	50 MHz	G_p	33.5	34.5	35.5	dB
Power Gain	550 MHz	G_p	35	—	—	dB
Slope		S	0	+1	2	dB
Gain Flatness		—	—	±0.2	±0.4	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–550 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion (V_{out} = +46 dBmV per ch., Ch 2, M13, M22) (V_{out} = +44 dBmV per ch., Ch 2, M30, M39)		IMD	 — —	 — —	 −68 −68	dB
Cross Modulation Distortion (V_{out} = +46 dBmV per ch.) (V_{out} = +44 dBmV per ch.)	 60-Channel FLAT 77-Channel FLAT	 XMD_{60} XMD_{77}	 — —	 −61 −59	 60 −57	dB
Composite Triple Beat (V_{out} = +46 dBmV per ch.) (V_{out} = +44 dBmV per ch.)	 60-Channel FLAT 77-Channel FLAT	 CTB_{60} CTB_{77}	 — —	 −60 −58	 — −57	dB
Noise Figure	550 MHz	NF	—	6	6.5	dB
DC Current (V_{DC} = 24 ±0.5 Vdc, T_C = 30°C)		I_{DC}	—	310	340	mA

OUTLINE DIMENSIONS



SYTLE 1:
PIN 1. RF IN
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUT

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.41	2.67	0.095	0.105
H	9.65	9.78	0.380	0.385
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.335
L	25.40 BSC		1.000 BSC	
N	4.06	4.32	0.160	0.170
P	2.16	2.92	0.085	0.115
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
T	11.05	11.43	0.435	0.450
U	4.95	5.21	0.195	0.205

NOTE:
1. MOUNTING HOLES WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

CASE 714-03

4

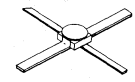
MWA0204
MWA0211,L
MWA0270

Monolithic Microwave Integrated Circuit

MONOLITHIC
MICROWAVE
INTEGRATED
CIRCUIT

. . . designed for narrow or wideband IF and RF applications in industrial and commercial systems up to 3 GHz.

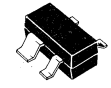
- 12 dB Gain at 500 MHz (Typ)
- Fully Cascadable
- 50 Ω Input and Output Impedance
- Choice of Package Types
  - Low Cost
  - Surface Mount
  - Hermetic
- Available In Both Standard Profile (MWA0211) and Low Profile (MWA0211L)
- Tape and Reel Packaging Options



CASE 303A-01
MWA0270



CASE 317-01
MWA0204



CASE 318B-01
MWA0211,L

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameters		Symbol	Ratings	Unit
Circuit Current		I_{CC}	40	mAdc
Input Power, RF		P_{in}	+16	dBm
Output Voltage		$V_{O(DC)}$	6	Vdc
Storage Temperature	0204/0211,L 0270	T_{stg}	−65 to +150 −65 to +200	°C

RECOMMENDED OPERATING CONDITIONS

Parameters	Symbol	Ratings	Unit
Operating Current	I_{CC}	25	mA
Source Impedance	Z_S	50 to 75	Ω
Load Impedance	Z_L	50 to 75	Ω

THERMAL CHARACTERISTICS

Thermal Resistance, Die to Case	MWA0204 MWA0211,L MWA0270	$R_{\theta JC}$	150 200 130	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C, I_{CC} = 25 mA, Z_S = Z_L = 50 Ω, unless specified otherwise)

Characteristic	Symbol	Min	Typ	Max	Unit
Gain (f = 500 MHz)	G_T	10	12	—	dB
Gain Flatness	—				dB
(f = 100 to 800 MHz — MWA0204/0211,L)		—	1	—	
(f = 100 to 1600 MHz — MWA0270)		—	1	—	
Noise Figure (f = 100–1500 MHz)	NF	—	6	—	dB
Third Order Intercept Output Power	—	—	16	—	dBm

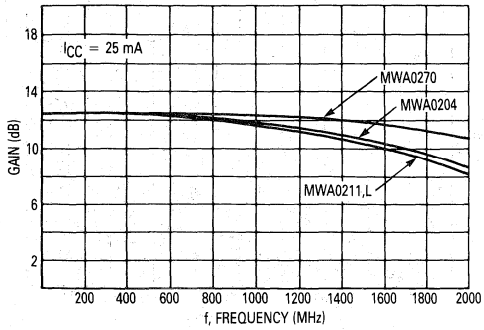


Figure 1. Gain versus Frequency

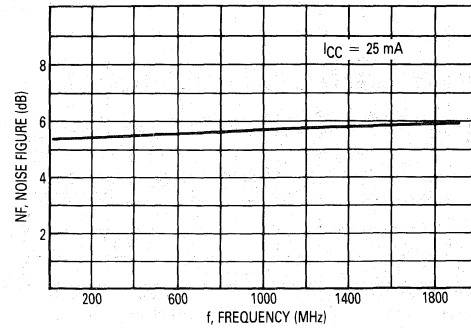


Figure 2. Noise Figure versus Frequency

TYPICAL S-PARAMETERS — MWA0204

I_{CC} (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
		$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
25	100	0.195	168	4.430	172	0.118	2	0.028	173
	200	0.197	159	4.442	166	0.119	4	0.034	−147
	300	0.192	151	4.402	161	0.119	5	0.048	−137
	400	0.191	142	4.300	155	0.121	8	0.064	−132
	500	0.191	134	4.218	148	0.124	10	0.079	−133
	600	0.190	127	4.188	141	0.126	10	0.096	−135
	700	0.192	121	4.155	136	0.129	12	0.113	−136
	800	0.183	118	4.062	131	0.130	14	0.128	−138
	900	0.174	113	3.922	126	0.135	15	0.140	−139
	1000	0.168	109	3.816	120	0.138	16	0.151	−141
	1100	0.164	105	3.727	114	0.144	17	0.161	−141
	1200	0.159	103	3.658	108	0.148	17	0.168	−143
	1300	0.155	105	3.590	103	0.153	17	0.176	−144
	1400	0.150	105	3.466	99	0.156	17	0.180	−144
	1500	0.145	108	3.318	95	0.160	16	0.181	−143
	1600	0.144	111	3.250	90	0.159	16	0.180	−143
	1700	0.143	115	3.160	85	0.165	16	0.184	−141
	1800	0.142	120	3.090	80	0.167	17	0.185	−141
	1900	0.146	123	3.026	76	0.170	17	0.187	−139
	2000	0.148	126	2.920	72	0.173	17	0.182	−136

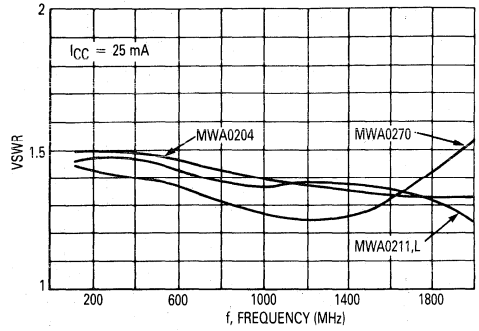


Figure 3. Input VSWR versus Frequency

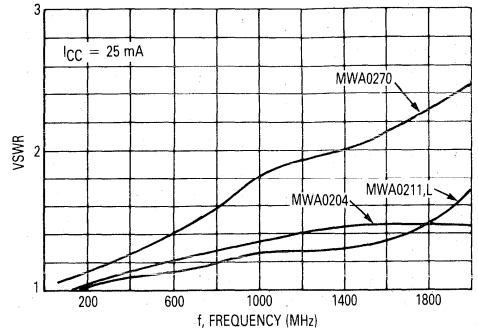


Figure 4. Output VSWR versus Frequency

TYPICAL S-PARAMETERS — MWA0211,L

I_{CC} (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
		$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
25	100	0.185	167	4.153	172	0.124	3	0.013	153
	200	0.190	156	4.145	166	0.123	6	0.016	−138
	300	0.195	149	4.102	161	0.127	10	0.024	−130
	400	0.185	143	3.987	155	0.129	12	0.035	−127
	500	0.173	132	3.920	149	0.131	15	0.045	−125
	600	0.179	119	3.856	142	0.135	18	0.062	−124
	700	0.186	116	3.816	137	0.139	21	0.076	−124
	800	0.172	112	3.670	133	0.142	23	0.090	−123
	900	0.155	103	3.534	127	0.148	25	0.097	−119
	1000	0.156	90	3.430	122	0.150	26	0.104	−117
	1100	0.166	84	3.329	117	0.157	28	0.107	−115
	1200	0.166	83	3.256	112	0.165	30	0.114	−113
	1300	0.158	80	3.160	109	0.169	32	0.118	−113
	1400	0.160	78	3.020	104	0.177	33	0.125	−113
	1500	0.157	81	2.936	100	0.181	34	0.134	−110
	1600	0.148	85	2.838	95	0.190	34	0.148	−107
	1700	0.141	89	2.795	92	0.198	35	0.156	−105
	1800	0.135	95	2.727	88	0.203	36	0.170	−101
	1900	0.116	102	2.627	85	0.205	37	0.183	−97
	2000	0.114	113	2.576	80	0.214	37	0.200	−93

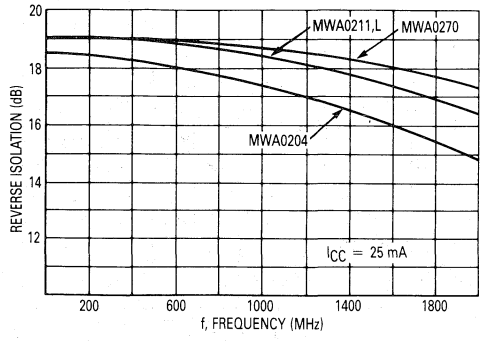


Figure 5. Reverse Isolation versus Frequency

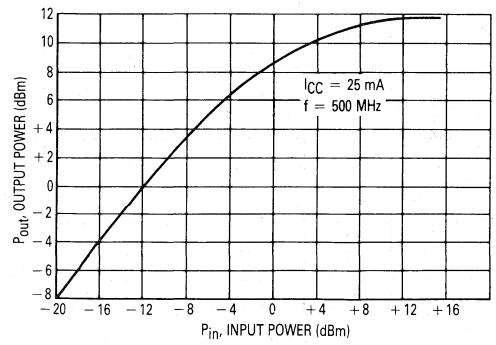


Figure 6. Output Power versus Input Power

TYPICAL S-PARAMETERS — MWA0270

I_{CC} (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
		$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
25	100	0.174	178	4.054	175	0.125	1	0.021	−63
	200	0.174	179	4.130	170	0.125	2	0.061	−84
	300	0.164	−179	4.083	167	0.125	2	0.078	−90
	400	0.157	179	4.033	164	0.127	4	0.107	−92
	500	0.158	178	4.000	158	0.129	5	0.131	−95
	600	0.158	−177	4.014	153	0.129	6	0.170	−99
	700	0.150	−171	4.065	148	0.131	7	0.207	−102
	800	0.135	−166	4.036	146	0.132	8	0.242	−105
	900	0.126	−164	3.965	141	0.135	9	0.263	−104
	1000	0.120	−160	3.930	136	0.136	9	0.288	−104
	1100	0.114	−157	3.898	131	0.139	11	0.301	−103
	1200	0.112	−153	3.899	127	0.143	11	0.325	−104
	1300	0.112	−151	3.832	124	0.146	12	0.341	−105
	1400	0.115	−151	3.735	120	0.149	12	0.350	−106
	1500	0.123	−153	3.647	115	0.151	13	0.360	−107
	1600	0.139	−156	3.621	110	0.157	13	0.373	−105
	1700	0.156	−158	3.602	106	0.162	12	0.382	−106
	1800	0.181	−159	3.567	102	0.164	12	0.401	−105
	1900	0.195	−162	3.442	97	0.168	12	0.408	−105
	2000	0.209	−162	3.392	93	0.174	12	0.415	−102

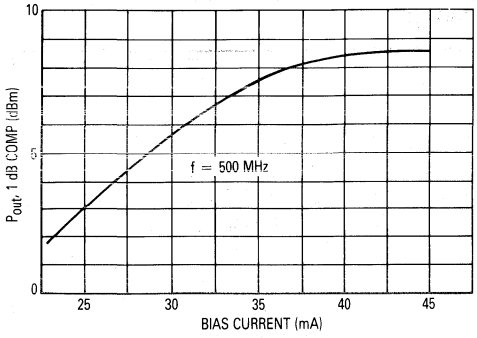


Figure 7. Output Power at 1 dB Gain Compression versus Bias Current

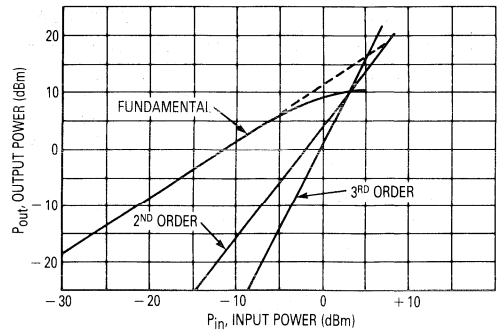


Figure 8. Second and Third Order Intercept

MMIC AMPLIFIER APPLICATIONS INFORMATION

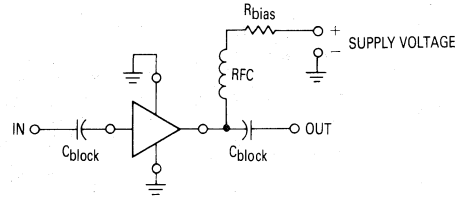


Figure 9. Typical Biasing Configuration

4

Operation

Operation of the Monolithic Microwave Integrated Circuit as an amplifier is achieved by simply connecting it to 50 ohm driving source and load impedances with dc blocking capacitors at both input and output.

DC Bias

A positive voltage must be supplied to the device output terminal. Power supply decoupling elements must include resistive current limiting. Device input voltage at the recommended operating current of 25 mA is typically 5 Vdc. R_{bias} (Figure 9) is selected to permit the device to draw 25 mA. For example, when operating with a 12 Vdc supply:

$$R_{bias} = \frac{(12-5)}{0.025} = 280 \text{ ohms}$$

The nearest standard value of 270 ohms would suffice.

External Decoupling Impedance

In all cases the external bias (decoupling elements) must present an impedance which is large compared to the 50 Ω load impedance to minimize RF gain reduction. The loss in gain due to the decoupling impedance is given by the equation:

$$\text{Loss} = 20 \text{ Log } \frac{Z_D}{Z_D + 25} \text{ dB}$$

where Z_D = decoupling impedance in ohms. For example, if Z_D = 1 kΩ, Loss = 0.214 dB.

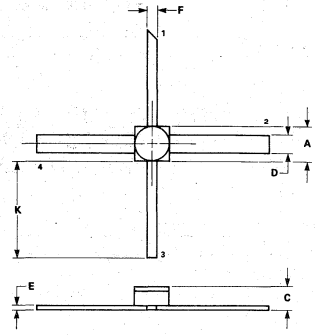
The RF choke is not mandatory, but including it improves gain by raising the dc supply voltage decoupling impedance. 4 turns of #26 AWG enameled wire wound on a ferrite bead is suggested for the choke.

Low Frequency Response

The value of the blocking capacitors determines the low frequency response of the amplifier. The following expression is used to determine the blocking capacitor value to yield a desired 3 dB low frequency corner (f_{LFC}).

$$C_{Block}(\text{Farads}) = \frac{1}{100\,\pi\, f_{LFC}(\text{Hz})}$$

OUTLINE DIMENSIONS

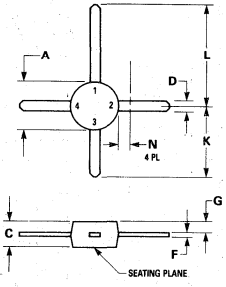


STYLE 3:
PIN 1. INPUT
2. GROUND
3. OUTPUT
4. GROUND

NOTE:
1. DIMENSION K APPLIES TO ALL LEADS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	1.58	1.98	0.062	0.078
C	0.77	1.19	0.030	0.047
D	0.84	1.19	0.033	0.047
E	0.08	0.15	0.003	0.006
F	0.41	0.60	0.016	0.024
K	5.01	5.89	0.197	0.232

CASE 303A-01
MWA0270

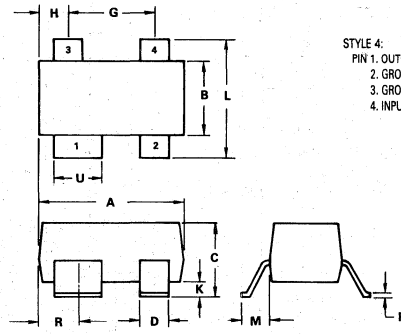


STYLE 3:
PIN 1. OUTPUT
2. GROUND
3. INPUT
4. GROUND

NOTE:
DIMENSION D NOT APPLICABLE IN ZONE N.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.44	5.21	0.175	0.205
C	1.90	2.54	0.075	0.100
D	0.84	0.99	0.033	0.039
F	0.20	0.30	0.008	0.012
G	0.76	1.14	0.030	0.045
K	7.24	8.13	0.285	0.320
L	10.54	11.43	0.415	0.450
N	—	1.65	—	0.065

CASE 317-01
MWA0204



STYLE 4:
PIN 1. OUTPUT
2. GROUND
3. GROUND
4. INPUT

	DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
	A	2.80	3.04	0.110	0.120
	B	1.20	1.39	0.047	0.055
	C	0.85	1.14	0.033	0.045
	D	0.38	0.45	0.015	0.018
	F	0.08	0.15	0.003	0.006
	G	1.78	2.03	0.070	0.080
	H	0.51	0.60	0.020	0.024
	K	0.10	0.25	0.004	0.010
	L	2.11	2.48	0.083	0.098
	M	0.46	0.60	0.018	0.024
	R	0.71	0.83	0.028	0.033
	U	0.78	0.88	0.031	0.035
*	K	0.013	0.102	0.0005	0.0040

***Low Profile = Case 318A-02**

CASE 318B-01
MWA0211,L

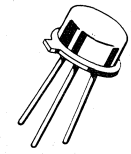
MWA110
MWA120
MWA130

WIDEBAND HYBRID AMPLIFIERS

. . . single stage amplifiers designed for broadband linear applications up to 400 MHz.

- Low-Cost TO-39 Type Package
- Gain 14 dB Typ
- 50 Ω Input and Output Impedance
- Fully Cascadable for Any Gain
- Thin Film Construction
- Hermetic Package
- Guaranteed Performance from -25°C to +125°C

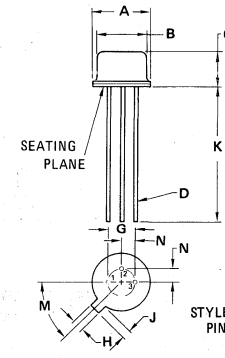
DC-400 MHz WIDEBAND GENERAL-PURPOSE HYBRID AMPLIFIERS



4

MAXIMUM RATINGS

Rating	Symbol	Value MWA110	Value MWA120	Value MWA130	Unit
RF Input Power	P_{in}	← 100 →			mW
DC Supply Current	I_D	25	55	100	mA
Maximum Case Temperature	T_C	← 125 →			°C
Storage Temperature Range	T_{stg}	← −65 to +200 →			°C
OPERATING CONDITIONS					
Device Voltage	V_D	2.9	5.0	5.5	Vdc
Device Current	I_D	10	25	60	mAdc
Decoupling Impedance	Z_D	1000	1000	330	Ω



STYLE 2:
PIN 1. INPUT
2. OUTPUT
3. GROUND

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	3.81	4.57	0.150	0.180
D	0.41	0.48	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.71	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	–	0.500	–
M	45° BSC		45° BSC	
N	2.54 BSC		0.100 BSC	

NOTE:
1. LEADS WITHIN 0.36 mm (0.014) DIA OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

CASE 31A-01

ELECTRICAL CHARACTERISTICS (T_C = -25 to +125°C, 50 Ω system and specified operating conditions)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	0.1	–	400	MHz
Power Gain	G_p	13	14	–	dB
Response Flatness	F	–	0	±1.0	dB
Input VSWR MWA110/120		–	–	2.5:1	–
MWA130		–	–	3:1	–
Output VSWR MWA110/120/130		–	–	2.5:1	–
Output @ 1 dB Gain Compression					dBm
MWA110		–	-2.5	–	
MWA120		–	+8.2	–	
MWA130		–	+18	–	
Noise Figure	NF				dB
MWA110		–	4.0	–	
MWA120		–	5.5	–	
MWA130		–	7.0	–	
Reverse Isolation	P_{RI}				dB
MWA110		–	18.8	–	
MWA120		–	19.2	–	
MWA130		–	16.8	–	
Harmonic Output	d_{so}				dB
MWA110 (P_{out} = -9 dBm)		–	-24	–	
MWA120 (P_{out} = 0 dBm)		–	-34	–	
MWA130 (P_{out} = +10 dBm)		–	-35	–	

FIGURE 1 – DEVICE VOLTAGE versus DEVICE CURRENT

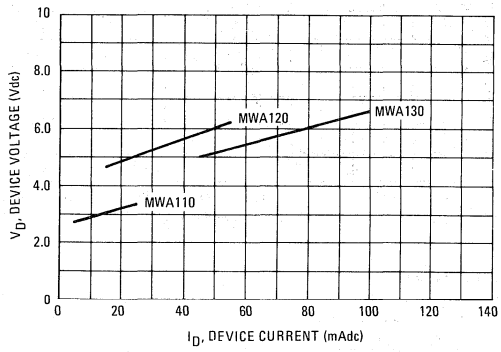


FIGURE 2 – DEVICE CURRENT versus CASE TEMPERATURE

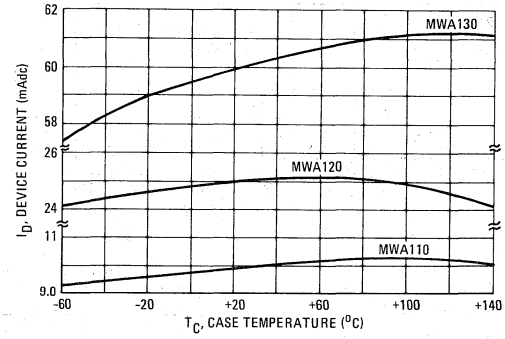


FIGURE 3 – POWER GAIN versus FREQUENCY

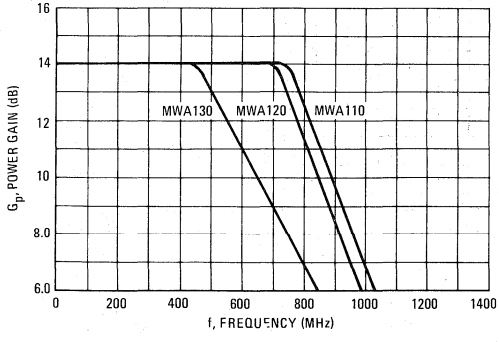
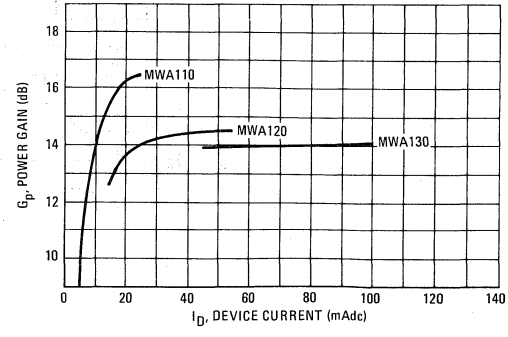


FIGURE 4 – POWER GAIN versus DEVICE CURRENT
f = 400 MHz



4

FIGURE 5 – POWER GAIN versus CASE TEMPERATURE
f = 100 MHz

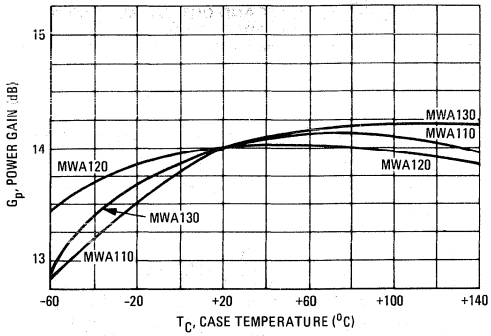


FIGURE 6 – POWER GAIN versus CASE TEMPERATURE
f = 400 MHz

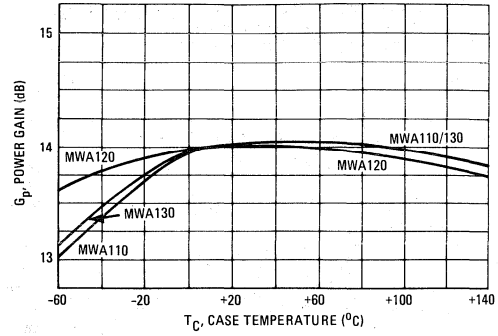


FIGURE 7 – VSWR versus FREQUENCY
MWA110

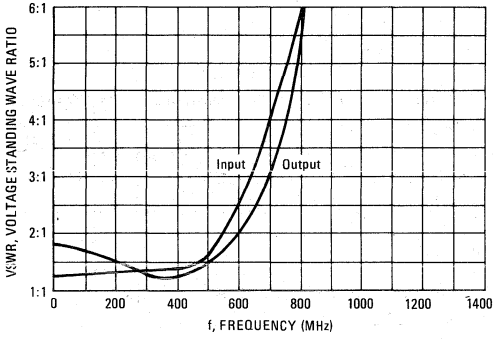


FIGURE 8 – VSWR versus FREQUENCY
MWA120

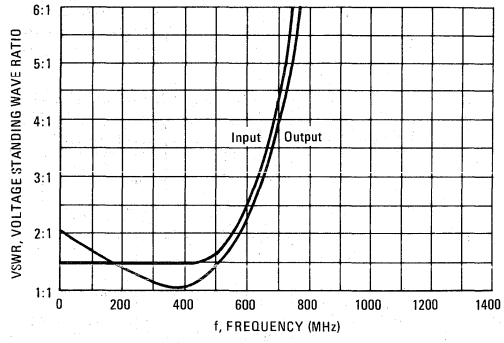


FIGURE 9 – VSWR versus FREQUENCY
MWA130

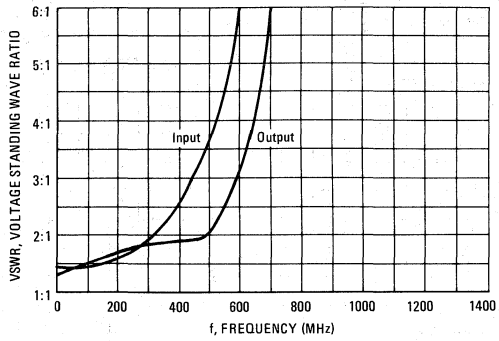
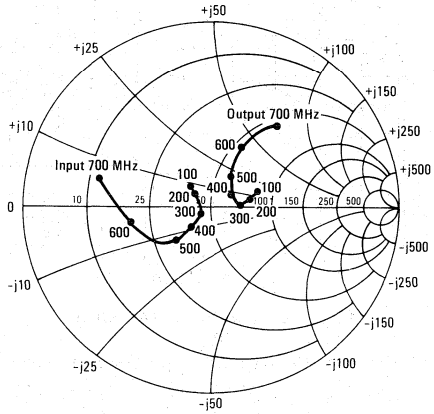
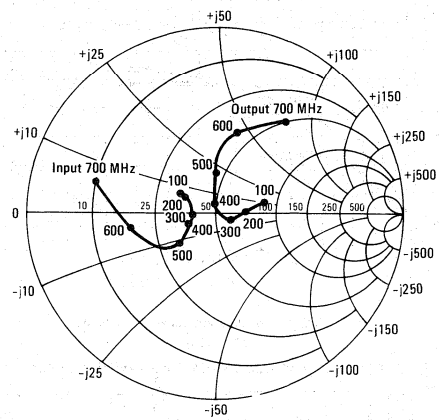


FIGURE 10 – INPUT AND OUTPUT IMPEDANCE versus FREQUENCY MWA110



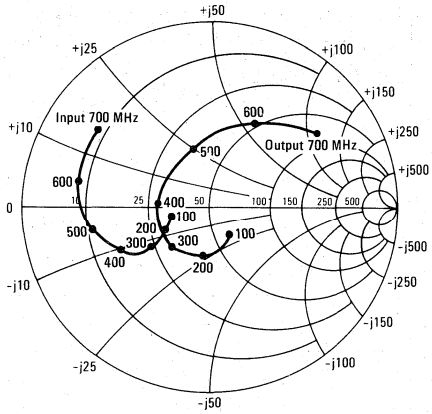
Coordinates in Ohms

FIGURE 11 – INPUT AND OUTPUT IMPEDANCE versus FREQUENCY MWA120



Coordinates in Ohms

FIGURE 12 – INPUT AND OUTPUT IMPEDANCE versus FREQUENCY MWA130



Coordinates in Ohms

FIGURE 13 – 1.0 dB GAIN COMPRESSION versus FREQUENCY

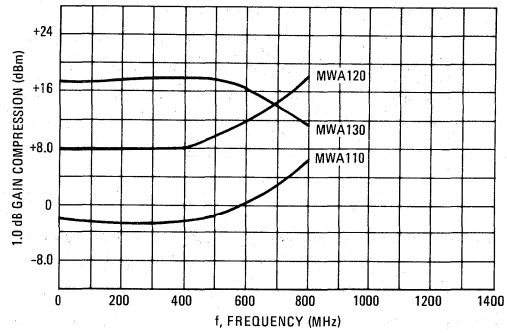


FIGURE 14 – 1.0 dB GAIN COMPRESSION versus DEVICE CURRENT f = 400 MHz

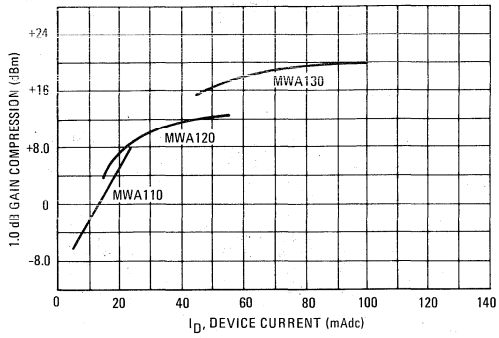


FIGURE 15 – 1.0 dB GAIN COMPRESSION versus CASE TEMPERATURE f = 400 MHz

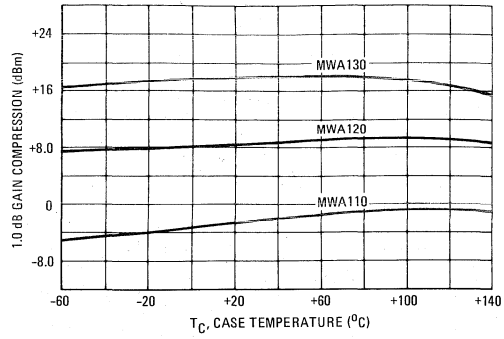


FIGURE 16 – NOISE FIGURE versus FREQUENCY

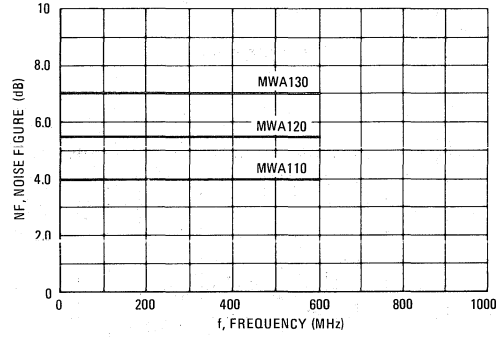


FIGURE 17 – REVERSE ISOLATION versus FREQUENCY

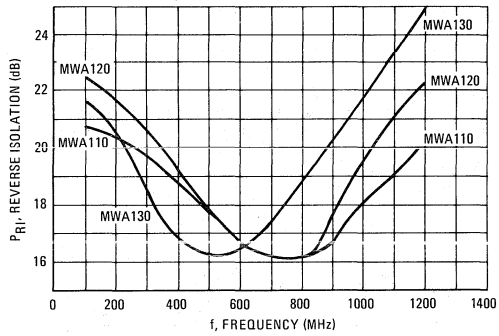


FIGURE 18 – SECOND HARMONIC OUTPUT versus FREQUENCY

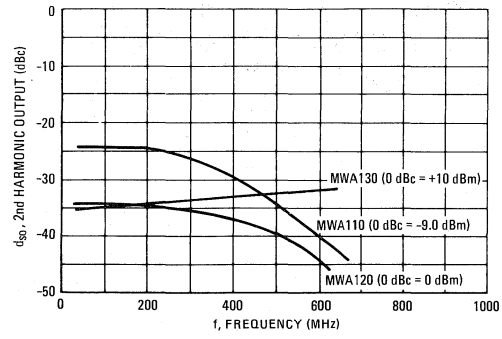
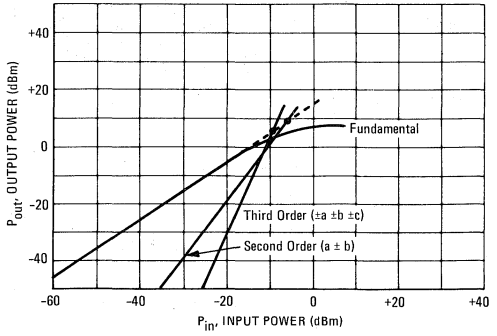


FIGURE 19 – SECOND AND THIRD ORDER INTERCEPT MWA110



4

FIGURE 20 – SECOND AND THIRD ORDER INTERCEPT
MWA120

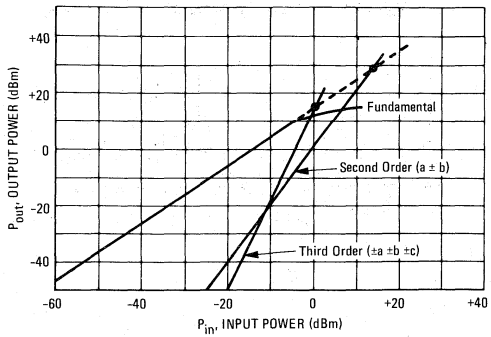


FIGURE 21 – SECOND AND THIRD ORDER INTERCEPT
MWA130

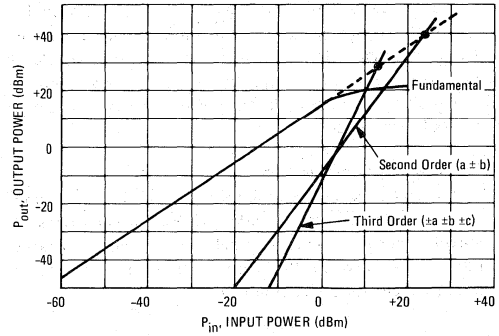


FIGURE 22 – INTERMODULATION DISTORTION
versus POWER OUTPUT
MWA110

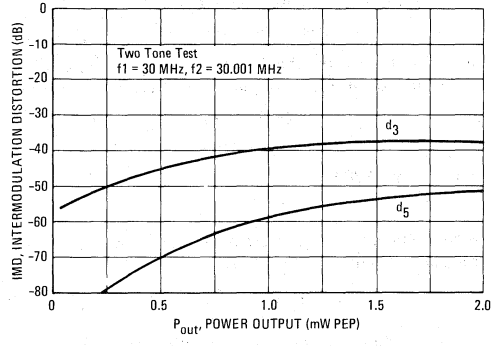


FIGURE 23 – INTERMODULATION DISTORTION
versus POWER OUTPUT
MWA120

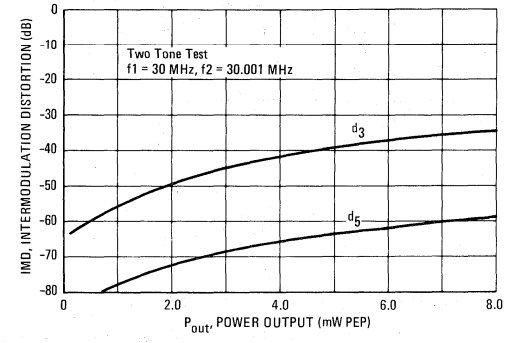


FIGURE 24 – INTERMODULATION DISTORTION
versus POWER OUTPUT
MWA130

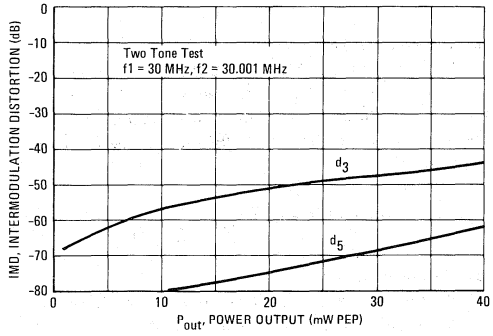
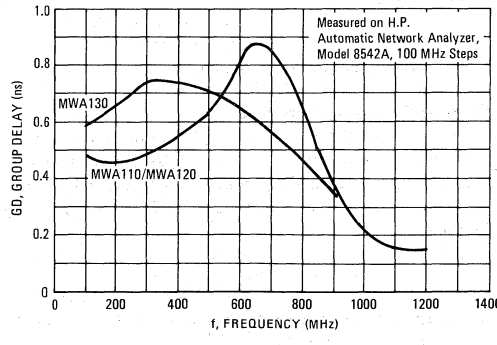


FIGURE 25 – GROUP DELAY versus FREQUENCY



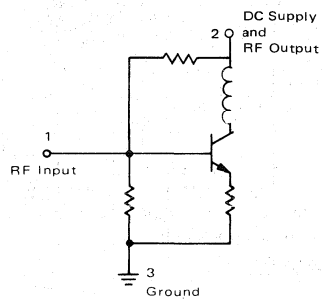
MWA SERIES HYBRID AMPLIFIER APPLICATIONS INFORMATION

The MWA series hybrid amplifiers are designed for wideband general purpose applications in 50 Ω systems. Fully cascadable for any gain combination, operable at voltages as low as 3 Vdc, and external control of the low frequency corner make the MWA amplifiers extremely versatile gain blocks.

Basic Circuit Configuration

Figure 26 shows the basic internal circuit. It is important to note that the specified operating conditions of voltage, current, and external decoupling impedance must be applied to the units in order to achieve the published electrical characteristics.

FIGURE 26 – INTERNAL CIRCUIT



Amplifier Application

The circuit schematic for a simple amplifier design is shown in Figure 27. External to the MWA hybrid amplifier the only components required are:

Decoupling elements – Bypass Capacitor
Decoupling Impedance
(resistor/inductor)
DC Blocking Capacitors at the RF input and output.

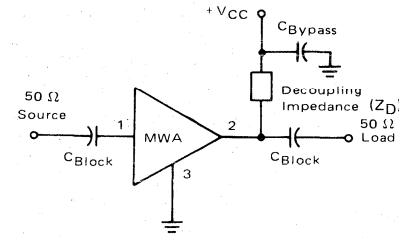
External Decoupling Impedance

In all cases the external bias (decoupling elements) must present an impedance which is large compared to the 50 Ω load impedance to minimize RF gain reduction. The loss in gain due to the decoupling impedance is given by the equation:

$$\text{Loss} = 20 \text{ Log } \frac{Z_D}{Z_D + 25} \text{ dB}$$

where Z_D = decoupling impedance in ohms. For example, if Z_D = 1 kΩ, Loss = 0.214 dB.

FIGURE 27 – AMPLIFIER SCHEMATIC DIAGRAM



Supply Voltage

The value of the external decoupling resistive impedance (R_D) determines the supply voltage ($+V_{CC}$) and is determined by the following equation:

$$V_{CC} = R_D \times I_D + V_D$$

where I_D and V_D are the device current and voltage stated in the data sheet. For example, for MWA110,

$$I_D = 10 \text{ mA}$$
$$V_D = 2.9 \text{ V}$$

and, if R_D = 330 Ω, then

$$V_{CC} = 6.2 \text{ V}$$

More commonly V_{CC} is predetermined and R_D may be calculated from:

$$R_D = \frac{V_{CC} - V_D}{I_D}$$

If an RF choke is used for decoupling, then the supply voltage (V_{CC}) required is equal to the device voltage (V_D).

Low Frequency Response

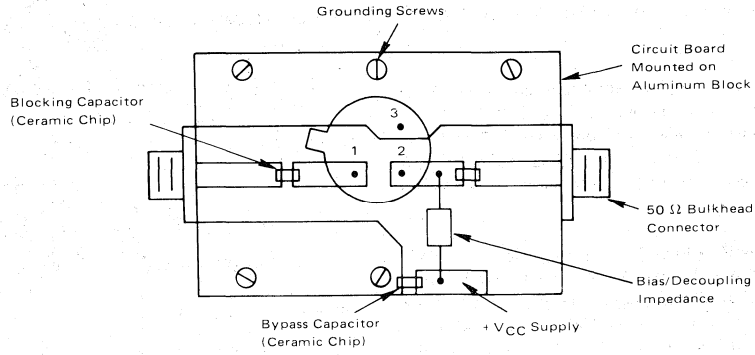
The value of the blocking capacitors determines the low frequency response of the amplifier. The following expression is used to determine the blocking capacitor value to yield a desired 3 dB low frequency corner (f_{LFC}).

$$C_{Block}(\text{Farads}) = \frac{1}{100 \pi f_{LFC}(\text{Hz})}$$

Bypass Capacitor

The reactive impedance of the bypass capacitor should be small compared to the impedance of the decoupling element at the lowest frequency of operation.

FIGURE 28 – TEST FIXTURE



Note: The circuitry indicated is on the underside of the printed circuit board with sockets for the amplifier pins. The case of the amplifier should contact the printed circuit board top surface to ensure effective RF grounding.

Text Fixture

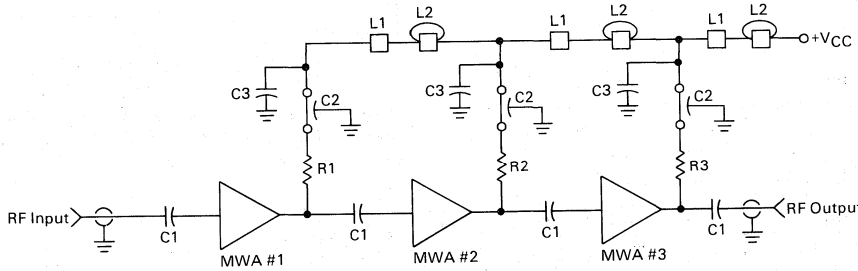
The 50 Ω input/output impedance levels of the MWA hybrids are most easily preserved on a circuit board by using 50 Ω microstrip transmission lines. Figure 28 is an example of a circuit board layout which utilizes microstrip transmission lines in conjunction with other sound RF construction techniques.

The characteristic impedance and corresponding line width of the microstrip are a function of the circuit board dielectric constant and thickness. The table lists appropriate line widths for 50 Ω microstrip lines on commonly used circuit board materials.

MATERIAL TYPE	DIELECTRIC CONSTANT	DIELECTRIC THICKNESS INCHES	LINE WIDTH INCHES
Teflon-Fiberglass	2.5	0.03125	0.090
		0.0625	0.180
Fiberglass-Epoxy	5.0	0.0625	0.100

As in all good RF circuit designs, care should be taken to minimize parasitic lead inductances and to provide adequate grounding.

FIGURE 29 – TYPICAL CASCADE



The dc isolation components shown are critical in maintaining good stability in multi-stage designs. Keep Pin #3 (Ground) as short as possible preferably soldering the case to the ground plane for best gain flatness to 1000 MHz.

C1 — For operation to 400 MHz, 1000 pF, 50 mil Chip Capacitor – ATC 50 mil Case (5.0 MHz L.F.)
C1 — For operation to 1000 MHz, 0.018 mF, Chip Capacitor for 0.25 MHz L.F. Cut-Off
C2 — Feedthru Capacitor Centralab SFT-102, 1000 pF or Metuchen 54-794002-681M, 680 pF
C3 — 0.1 μF Sprague 3CZ5U104X0050C5 – 50 Volt
L1 — Ferroxcube Shielding Bead 56-590-65/4A – Single Wire
L2 — Ferroxcube Shielding Bead 56-590-65/4A – 2 Turns #26 AWG

Cascading

The inherent stability of the MWA hybrid modules makes possible the cascading of two or more units with no oscillatory problems. Figure 29 shows a typical 3 hybrid cascade with measured data for 400 MHz and 1000 MHz hybrids.

	Cascade 1	Cascade 2
Frequency Range	0.25 to 400 MHz	5.0 to 1000 MHz
Gain	43.5 dB	20.5 dB
Gain Flatness	±1.0 dB	±0.75 dB
Input VSWR	2.0:1	2.4:1
Output VSWR	1.2:1	2.1:1
V_{CC} Supply	12 Vdc	33 Vdc
I Supply	44 mAdc	150 mAdc
MWA #1	MWA110	MWA320
MWA #2	MWA110	MWA330
MWA #3	MWA120	MWA330
R1	1000 Ω	1000 Ω
R2	1000 Ω	500 Ω
R3	300 Ω	500 Ω

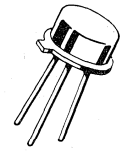
MWA210
MWA220
MWA230

DC-600 MHz WIDEBAND GENERAL-PURPOSE HYBRID AMPLIFIERS

WIDEBAND HYBRID AMPLIFIERS

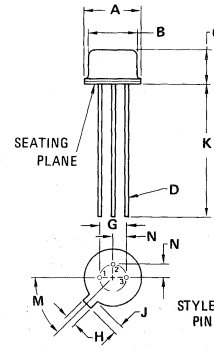
. . . single stage amplifiers designed for broadband linear applications up to 600 MHz.

- Low-Cost TO-39 Type Package
- Gain 10 dB Typ
- 50 Ω Input and Output Impedance
- Fully Cascadable for Any Gain
- Thin Film Construction
- Hermetic Package
- Guaranteed Performance from -25°C to +100°C



MAXIMUM RATINGS

Rating	Symbol	Value MWA210	Value MWA220	Value MWA230	Units
RF Input Power	P_{in}	← 100 →			mW
DC Supply Current	I_D	25	55	100	mA
Maximum Case Temperature	T_C	← 125 →			°C
Storage Temperature Range	T_{stg}	← -65 to +200 →			°C
OPERATING CONDITIONS					
Device Voltage	V_D	1.75	3.2	4.4	Vdc
Device Current	I_D	10	25	60	mAdc
Decoupling Impedance	Z_D	1000	1000	330	Ω



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	3.81	4.57	0.150	0.180
D	0.41	0.48	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.71	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	—	0.500	—
M	45° BSC		45° BSC	
N	2.54 BSC		0.100 BSC	

NOTE:
1. LEADS WITHIN 0.36 mm (0.014) DIA OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

CASE 31A-01

ELECTRICAL CHARACTERISTICS (T_C = -25 to +100°C, 50 Ω system and specified operating conditions)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	0.1	–	600	MHz
Power Gain	G_p	9.0	10	–	dB
Response Flatness	F	–	0	±1.0	dB
Input VSWR MWA210/220	–	–	–	2.5:1	–
MWA230	–	–	–	3:1	–
Output VSWR MWA210/220/230	–	–	–	2.5:1	–
Output @ 1 dB Gain Compression					dBm
MWA210		–	+1.5	–	
MWA220		–	+10.5	–	
MWA230		–	+18.5	–	
Noise Figure	NF				dB
MWA210		–	6.0	–	
MWA220		–	6.5	–	
MWA230		–	7.5	–	
Reverse Isolation	P_{RI}				dB
MWA210		–	13.5	–	
MWA220		–	14.5	–	
MWA230		–	12.9	–	
Harmonic Output	d_{so}				dB
MWA210 (P_{out} = -9.0 dBm)		–	-29	–	
MWA220 (P_{out} = 0 dBm)		–	-36	–	
MWA230 (P_{out} = +10 dBm)		–	-36	–	

FIGURE 1 – DEVICE VOLTAGE versus DEVICE CURRENT

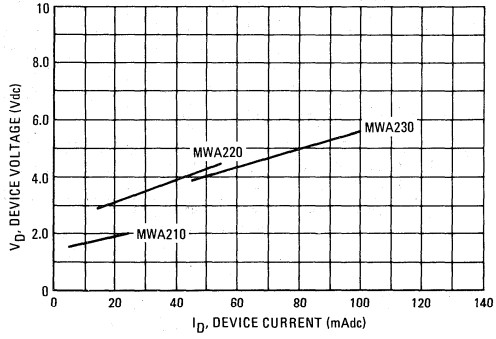


FIGURE 2 – DEVICE CURRENT versus CASE TEMPERATURE

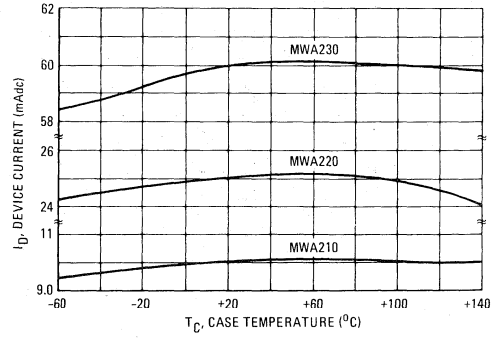


FIGURE 3 – POWER GAIN versus FREQUENCY

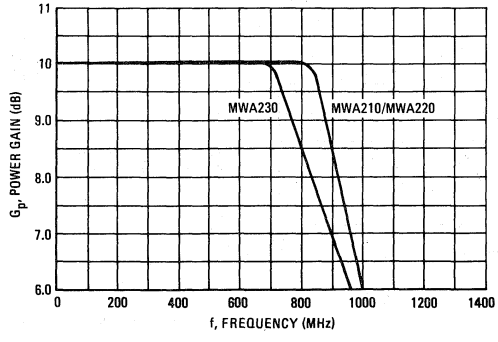


FIGURE 4 – POWER GAIN versus DEVICE CURRENT
f = 600 MHz

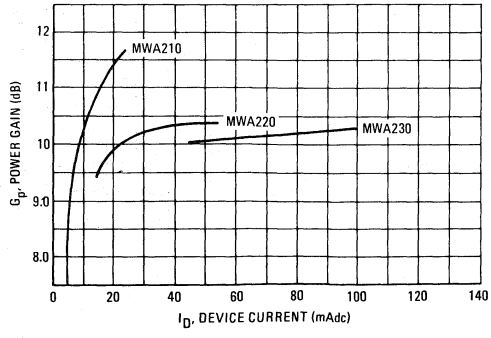


FIGURE 5 – POWER GAIN versus CASE TEMPERATURE
f = 100 MHz

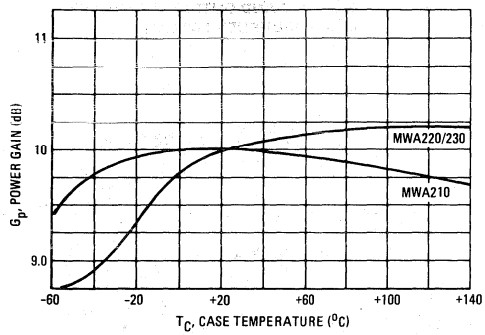


FIGURE 6 – POWER GAIN versus CASE TEMPERATURE
f = 600 MHz

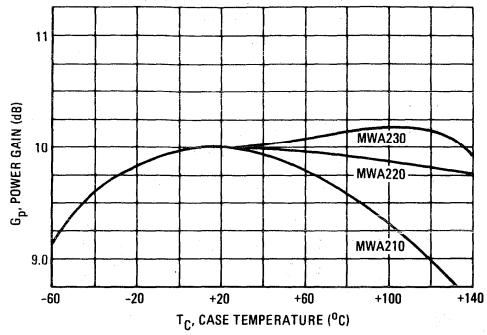


FIGURE 7 – VSWR versus FREQUENCY
MWA210

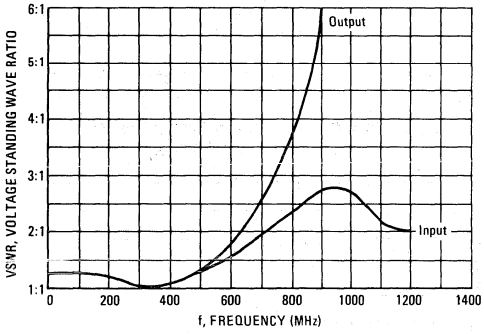


FIGURE 8 – VSWR versus FREQUENCY
MWA220

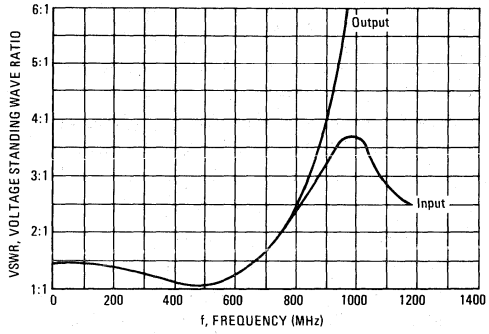


FIGURE 9 – VSWR versus FREQUENCY
MWA230

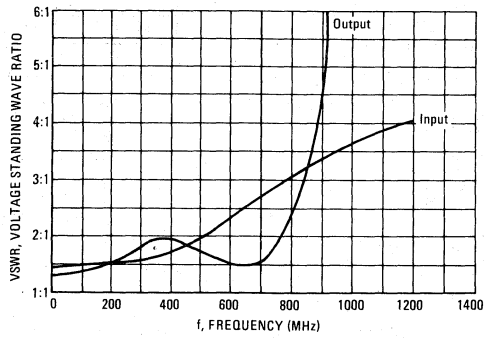


FIGURE 10 – INPUT AND OUTPUT IMPEDANCE versus FREQUENCY MWA210

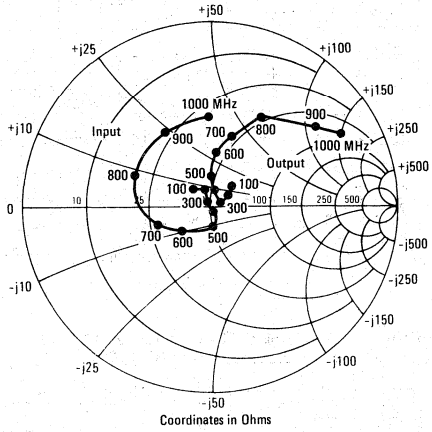


FIGURE 11 – INPUT AND OUTPUT IMPEDANCE versus FREQUENCY MWA220

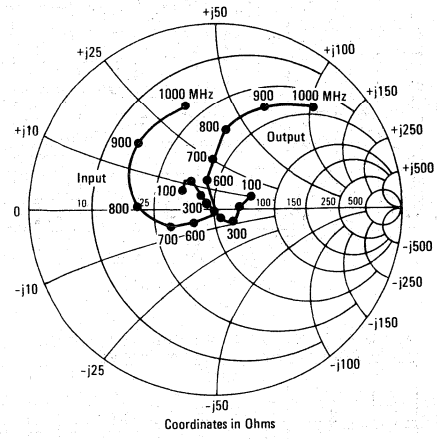


FIGURE 12 – INPUT AND OUTPUT IMPEDANCE versus FREQUENCY MWA230

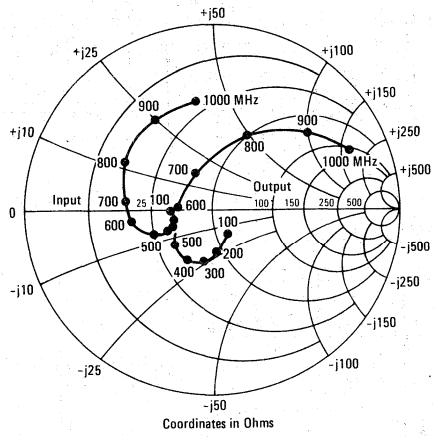


FIGURE 13 – 1.0 dB GAIN COMPRESSION versus FREQUENCY

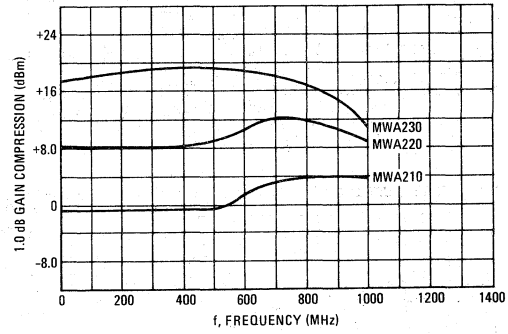


FIGURE 14 – 1.0 dB GAIN COMPRESSION versus DEVICE CURRENT f = 600 MHz

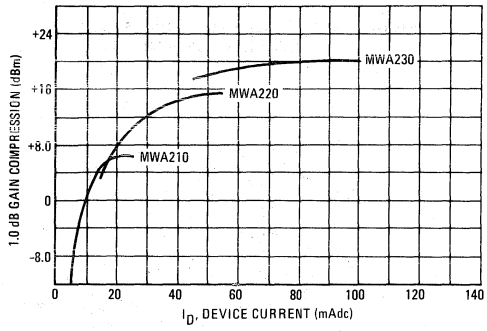


FIGURE 15 – 1.0 dB GAIN COMPRESSION versus CASE TEMPERATURE f = 600 MHz

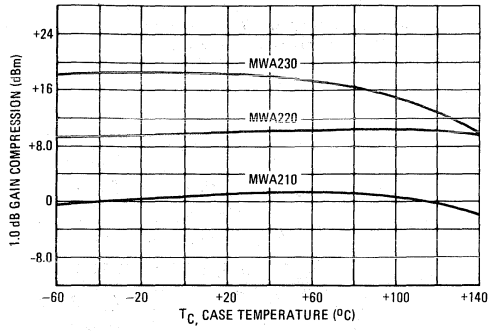


FIGURE 16 – NOISE FIGURE versus FREQUENCY

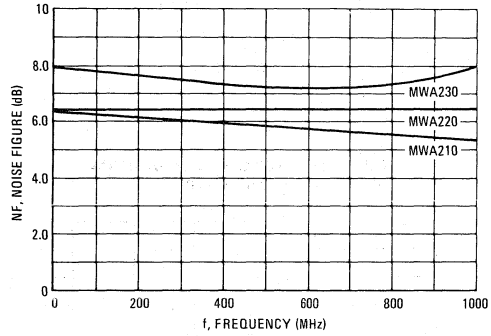


FIGURE 17 – REVERSE ISOLATION versus FREQUENCY

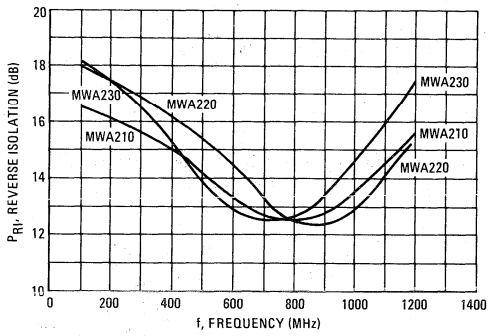


FIGURE 18 – SECOND HARMONIC OUTPUT versus FREQUENCY

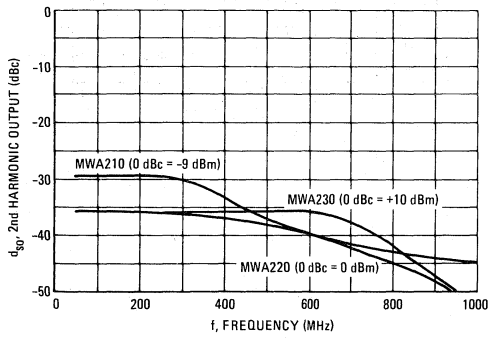


FIGURE 19 – SECOND AND THIRD ORDER INTERCEPT MWA210

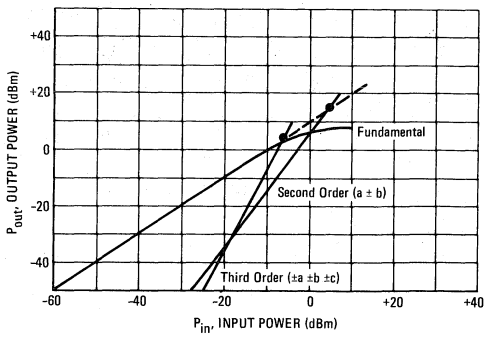


FIGURE 20 – SECOND AND THIRD ORDER INTERCEPT MWA220

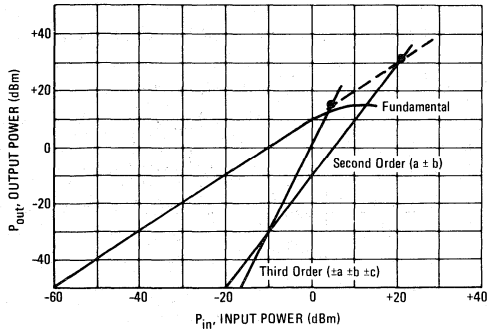


FIGURE 21 – SECOND AND THIRD ORDER INTERCEPT MWA230

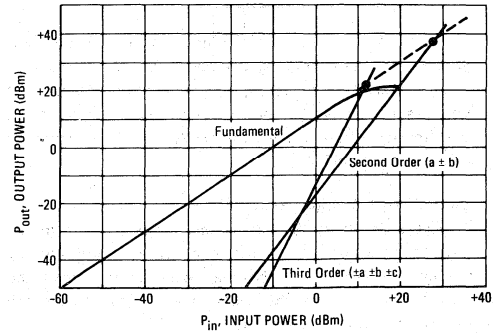


FIGURE 22 – INTERMODULATION DISTORTION versus POWER OUTPUT MWA210

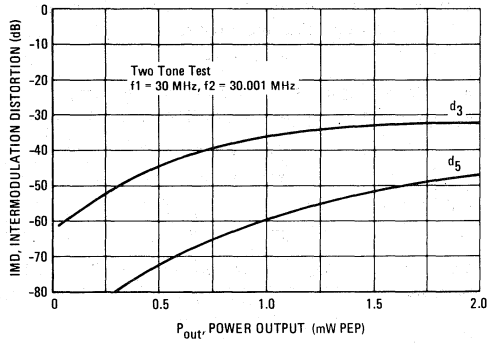


FIGURE 23 – INTERMODULATION DISTORTION versus POWER OUTPUT MWA220

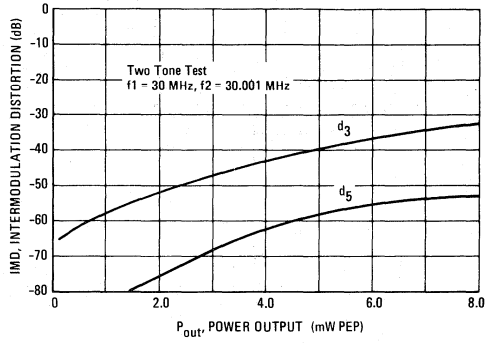


FIGURE 24 – INTERMODULATION DISTORTION versus POWER OUTPUT MWA230

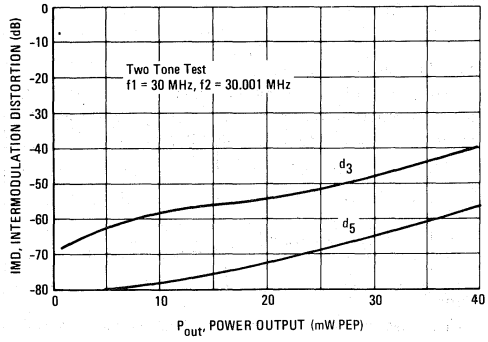
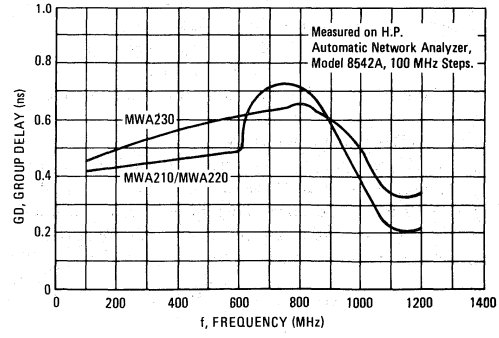


FIGURE 25 – GROUP DELAY versus FREQUENCY



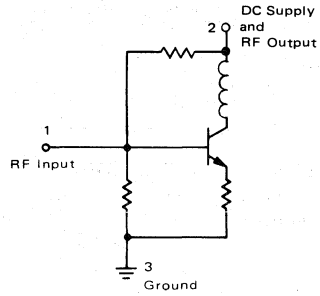
MWA SERIES HYBRID AMPLIFIER APPLICATIONS INFORMATION

The MWA series hybrid amplifiers are designed for wideband general purpose applications in 50 Ω systems. Fully cascadable for any gain combination, operable at voltages as low as 3 Vdc, and external control of the low frequency corner make the MWA amplifiers extremely versatile gain blocks.

Basic Circuit Configuration

Figure 26 shows the basic internal circuit. It is important to note that the specified operating conditions of voltage, current, and external decoupling impedance must be applied to the units in order to achieve the published electrical characteristics.

FIGURE 26 – INTERNAL CIRCUIT



Amplifier Application

The circuit schematic for a simple amplifier design is shown in Figure 27. External to the MWA hybrid amplifier the only components required are:

Decoupling elements – Bypass Capacitor
Decoupling Impedance
(resistor/inductor)

DC Blocking Capacitors at the RF input and output.

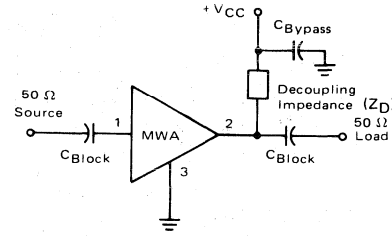
External Decoupling Impedance

In all cases the external bias (decoupling elements) must present an impedance which is large compared to the 50 Ω load impedance to minimize RF gain reduction. The loss in gain due to the decoupling impedance is given by the equation:

$$\text{Loss} = 20 \text{ Log } \frac{Z_D}{Z_D + 25} \text{ dB}$$

where Z_D = decoupling impedance in ohms. For example, if Z_D = 1 kΩ, Loss = 0.214 dB.

FIGURE 27 – AMPLIFIER SCHEMATIC DIAGRAM



Supply Voltage

The value of the external decoupling resistive impedance (R_D) determines the supply voltage ($+V_{CC}$) and is determined by the following equation:

$$V_{CC} = R_D \times I_D + V_D$$

where I_D and V_D are the device current and voltage stated in the data sheet. For example, for MWA110,

$$I_D = 10 \text{ mA}$$
$$V_D = 2.9 \text{ V}$$

and, if R_D = 330 Ω, then

$$V_{CC} = 6.2 \text{ V}$$

More commonly V_{CC} is predetermined and R_D may be calculated from:

$$R_D = \frac{V_{CC} - V_D}{I_D}$$

If an RF choke is used for decoupling, then the supply voltage (V_{CC}) required is equal to the device voltage (V_D).

Low Frequency Response

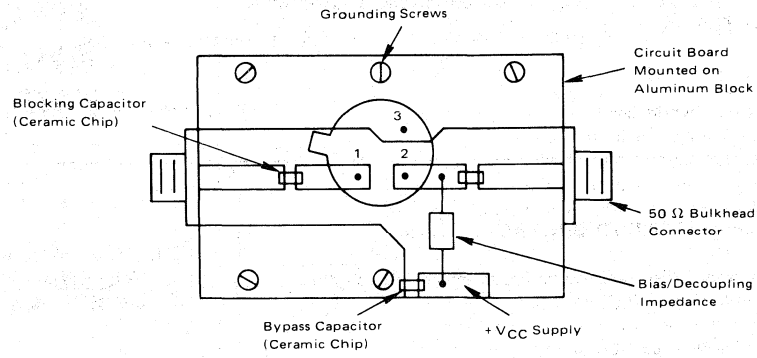
The value of the blocking capacitors determines the low frequency response of the amplifier. The following expression is used to determine the blocking capacitor value to yield a desired 3 dB low frequency corner (f_{LFC}).

$$C_{Block}(\text{Farads}) = \frac{1}{100 \pi f_{LFC}(\text{Hz})}$$

Bypass Capacitor

The reactive impedance of the bypass capacitor should be small compared to the impedance of the decoupling element at the lowest frequency of operation.

FIGURE 28 – TEST FIXTURE



Note: The circuitry indicated is on the underside of the printed circuit board with sockets for the amplifier pins. The case of the amplifier should contact the printed circuit board top surface to ensure effective RF grounding.

Text Fixture

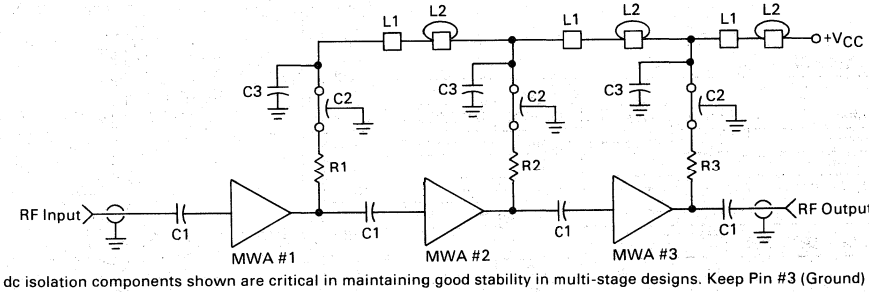
The 50 Ω input/output impedance levels of the MWA hybrids are most easily preserved on a circuit board by using 50 Ω microstrip transmission lines. Figure 28 is an example of a circuit board layout which utilizes microstrip transmission lines in conjunction with other sound RF construction techniques.

The characteristic impedance and corresponding line width of the microstrip are a function of the circuit board dielectric constant and thickness. The table lists appropriate line widths for 50 Ω microstrip lines on commonly used circuit board materials.

MATERIAL TYPE	DIELECTRIC CONSTANT	DIELECTRIC THICKNESS INCHES	LINE WIDTH INCHES
Teflon-Fiberglass	2.5	0.03125	0.090
		0.0625	0.180

As in all good RF circuit designs, care should be taken to minimize parasitic lead inductances and to provide adequate grounding.

FIGURE 29 — TYPICAL CASCADE



The dc isolation components shown are critical in maintaining good stability in multi-stage designs. Keep Pin #3 (Ground) as short as possible preferably soldering the case to the ground plane for best gain flatness to 1000 MHz.

C1 — For operation to 400 MHz, 1000 pF, 50 mil Chip Capacitor – ATC 50 mil Case (5.0 MHz L.F.)
C1 — For operation to 1000 MHz, 0.018 mF, Chip Capacitor for 0.25 MHz L.F. Cut-Off
C2 — Feedthru Capacitor Centralab SFT-102, 1000 pF or Metuchen 54-794002-681M, 680 pF
C3 — 0.1 μF Sprague 3CZ5U104X0050C5 – 50 Volt
L1 — Ferroxcube Shielding Bead 56-590-65/4A – Single Wire
L2 — Ferroxcube Shielding Bead 56-590-65/4A – 2 Turns #26 AWG

Cascading

The inherent stability of the MWA hybrid modules makes possible the cascading of two or more units with no oscillatory problems. Figure 29 shows a typical 3 hybrid cascade with measured data for 400 MHz and 1000 MHz hybrids.

	Cascade 1	Cascade 2
Frequency Range	0.25 to 400 MHz	5.0 to 1000 MHz
Gain	43.5 dB	20.5 dB
Gain Flatness	±1.0 dB	±0.75 dB
Input VSWR	2.0:1	2.4:1
Output VSWR	1.2:1	2.1:1
V_{CC} Supply	12 Vdc	33 Vdc
I Supply	44 mAdc	150 mAdc
MWA #1	MWA110	MWA320
MWA #2	MWA110	MWA330
MWA #3	MWA120	MWA330
R1	1000 Ω	1000 Ω
R2	1000 Ω	500 Ω
R3	300 Ω	500 Ω

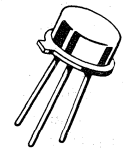
MWA310
MWA320
MWA330

WIDEBAND HYBRID AMPLIFIERS

. . . single stage amplifiers designed for broadband linear applications up to 1000 MHz.

- Low-Cost TO-39 Type Package
- Gain – 8.0 dB Typ MWA310/320
  – 6.2 dB Typ MWA330
- 50 Ω Input and Output Impedance
- Fully Cascadable for Any Gain
- Thin Film Construction
- Hermetic Package
- Guaranteed Performance from -25°C to +80°C

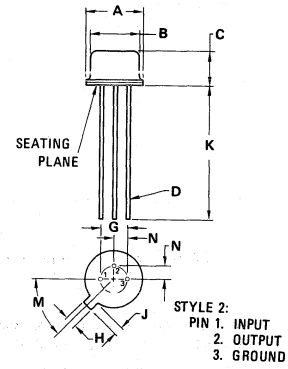
DC-1000 MHz WIDEBAND GENERAL-PURPOSE HYBRID AMPLIFIERS



4

MAXIMUM RATINGS

Rating	Symbol	Value MWA310	Value MWA320	Value MWA330	Unit
RF Input Power	P_{in}	← 100 →			mW
DC Supply Current	I_D	25	55	100	mA
Maximum Case Temperature	T_C	← 125 →			°C
Storage Temperature Range	T_{stg}	← -65 to +200 →			°C
OPERATING CONDITIONS					
Device Voltage	V_D	1.6	2.9	4.0	Vdc
Device Current	I_D	10	25	60	mAdc
Decoupling Impedance	Z_D	1000	1000	330	Ω



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	3.81	4.57	0.150	0.180
D	0.41	0.48	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.71	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	–	0.500	–
M	45° BSC		45° BSC	
N	2.54 BSC		0.100 BSC	

NOTE:
1. LEADS WITHIN 0.36 mm (0.014) DIA OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

CASE 31A-01

ELECTRICAL CHARACTERISTICS (T_C = -25 to +80°C, 50 Ω system and specified operating conditions)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	0.1	–	1000	MHz
Power Gain MWA310/320	G_p	7.0	8.0	–	dB
MWA330		–	6.2	–	
Response Flatness	F	–	0	±1.0	dB
Input VSWR	–	–	–	3:1	–
Output VSWR	–	–	–	3:1	–
Output @ 1 dB Gain Compression					dBm
MWA310		–	+3.5	–	
MWA320		–	+11.5	–	
MWA330		–	+15.2	–	
Noise Figure	NF				dB
MWA310		–	6.5	–	
MWA320		–	6.7	–	
MWA330		–	9.0	–	
Reverse Isolation	P_{RI}				dB
MWA310		–	10.4	–	
MWA320		–	10.4	–	
MWA330		–	9.0	–	
Harmonic Output	d_{so}				dB
MWA310 (P_{out} = -9 dBm)		–	-30	–	
MWA320 (P_{out} = 0 dBm)		–	-38	–	
MWA330 (P_{out} = +10 dBm)		–	-35	–	

FIGURE 1 – DEVICE VOLTAGE versus DEVICE CURRENT

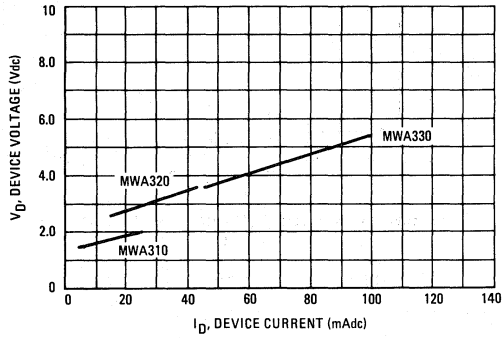


FIGURE 2 – DEVICE CURRENT versus CASE TEMPERATURE

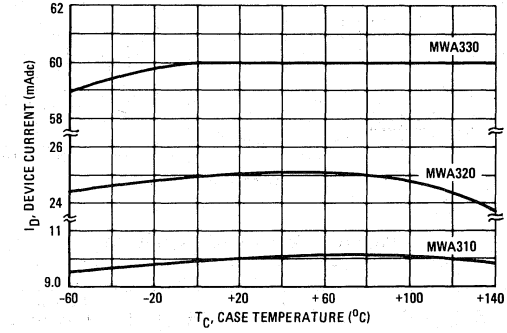


FIGURE 3 – POWER GAIN versus FREQUENCY

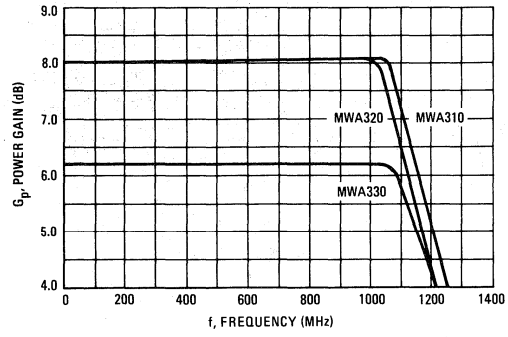


FIGURE 4 – POWER GAIN versus DEVICE CURRENT
f = 1000 MHz

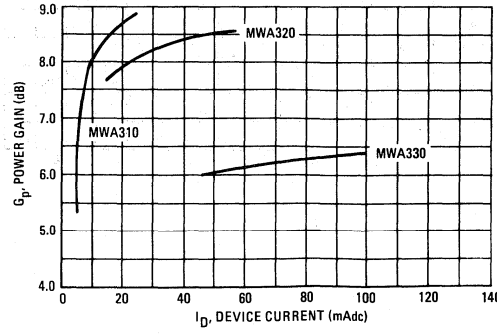


FIGURE 5 – POWER GAIN versus CASE TEMPERATURE
f = 100 MHz

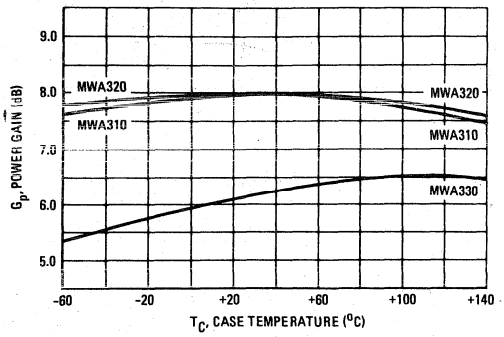


FIGURE 6 – POWER GAIN versus CASE TEMPERATURE
f = 1000 MHz

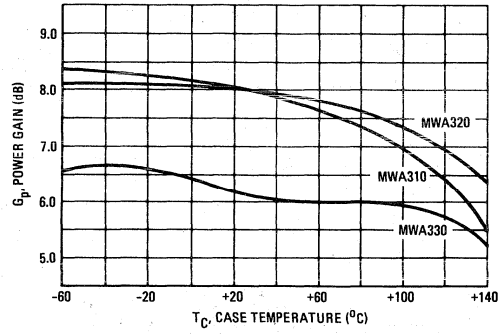


FIGURE 7 – VSWR versus FREQUENCY
MWA310

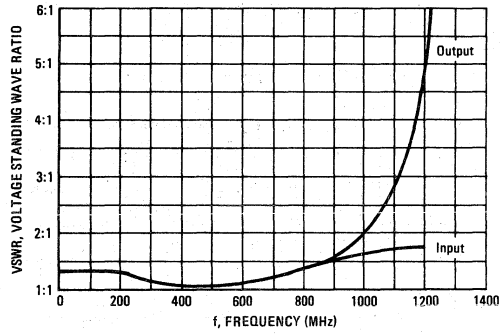


FIGURE 8 – VSWR versus FREQUENCY
MWA320

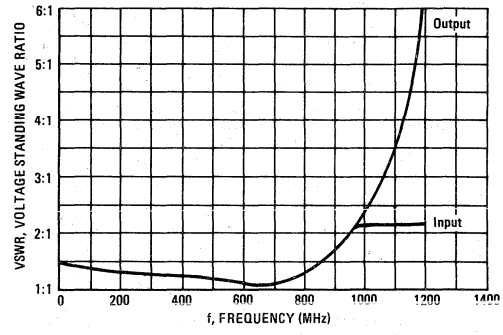


FIGURE 9 – VSWR versus FREQUENCY
MWA330

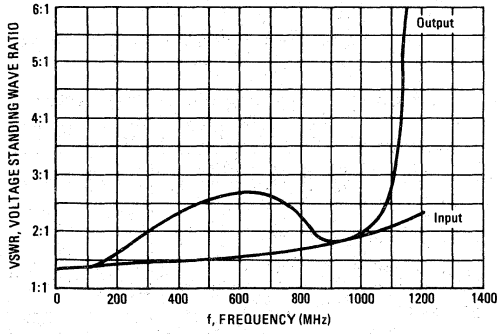


FIGURE 10 – INPUT IMPEDANCE versus FREQUENCY
MWA310

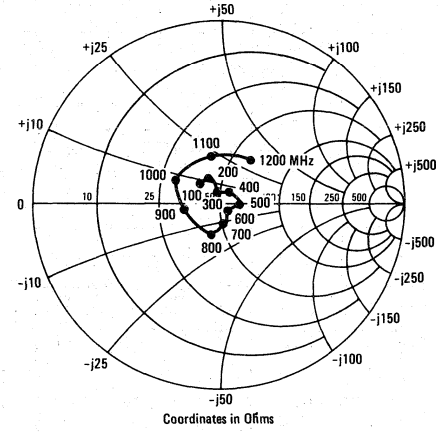


FIGURE 11 – OUTPUT IMPEDANCE versus FREQUENCY
MWA310

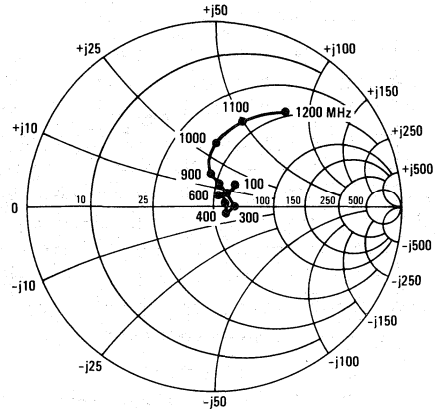


FIGURE 12 – INPUT IMPEDANCE versus FREQUENCY
MWA320

Coordinates in Ohms

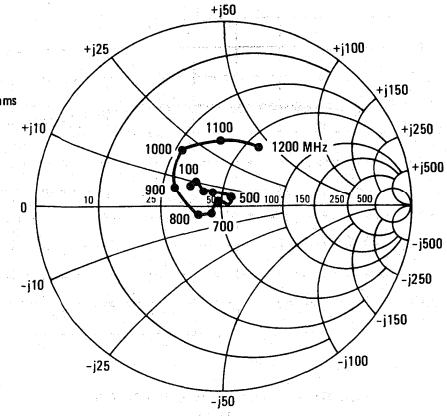


FIGURE 13 – OUTPUT IMPEDANCE versus FREQUENCY
MWA320

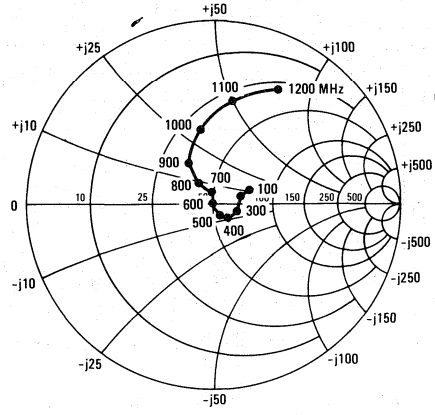


FIGURE 14 – INPUT IMPEDANCE versus FREQUENCY
MWA330

Coordinates in Ohms

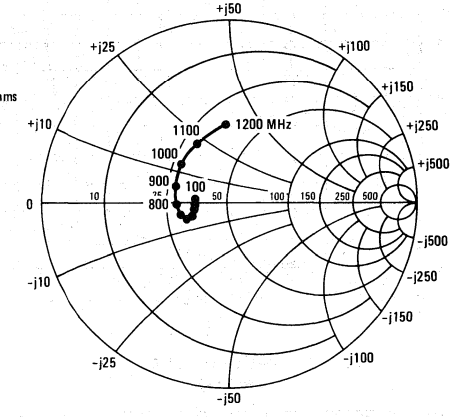


FIGURE 15 – OUTPUT IMPEDANCE versus FREQUENCY
MWA330

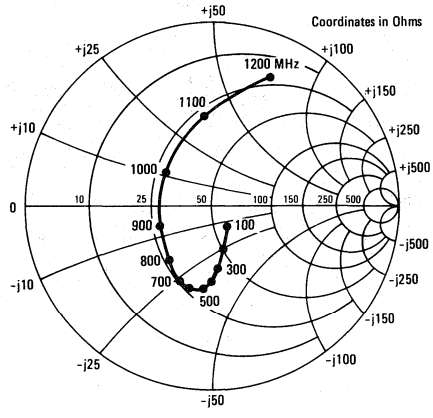
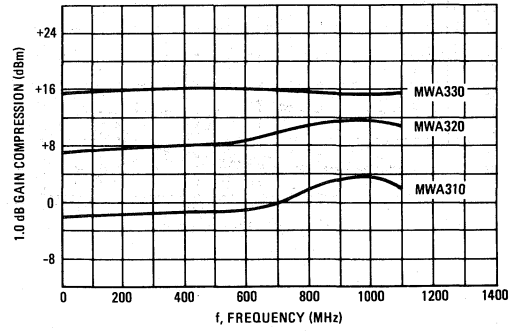


FIGURE 16 – 1.0 dB GAIN COMPRESSION versus FREQUENCY



4

FIGURE 17 – 1.0 dB GAIN COMPRESSION versus DEVICE CURRENT f = 1000 MHz

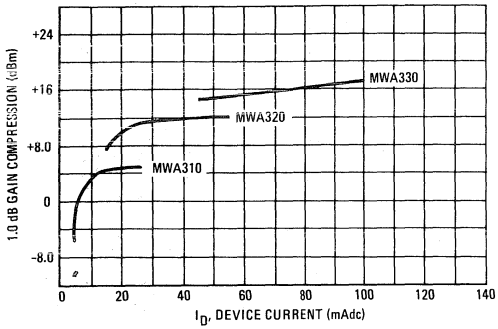


FIGURE 18 – 1.0 dB GAIN COMPRESSION versus CASE TEMPERATURE f = 1000 MHz

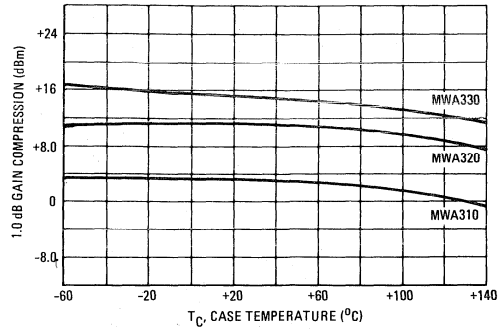


FIGURE 19 – NOISE FIGURE versus FREQUENCY

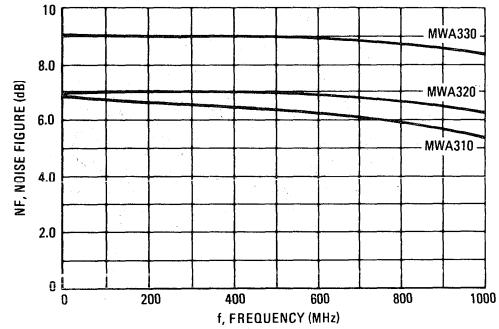


FIGURE 20 – REVERSE ISOLATION versus FREQUENCY

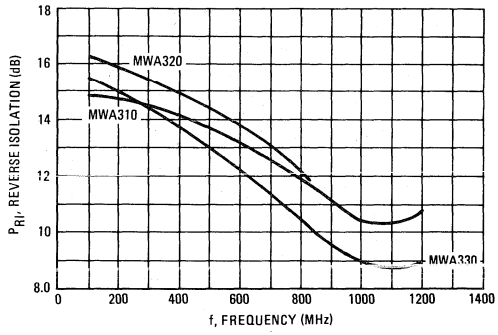


FIGURE 21 – SECOND HARMONIC OUTPUT versus FREQUENCY

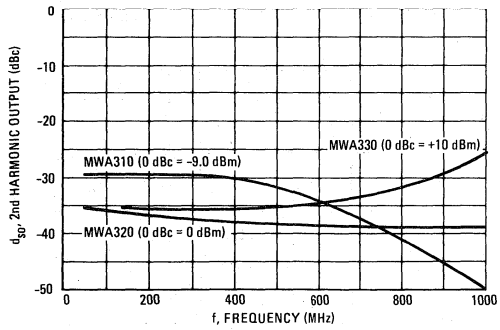


FIGURE 22 – SECOND AND THIRD ORDER INTERCEPT MWA310

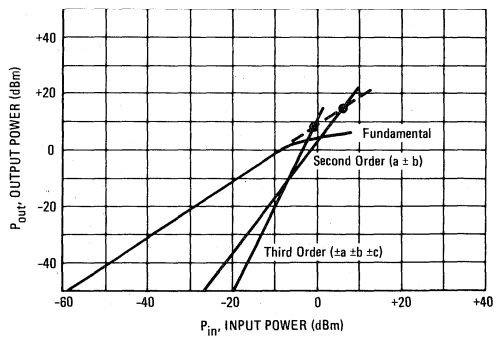


FIGURE 23 – SECOND AND THIRD ORDER INTERCEPT
MWA320

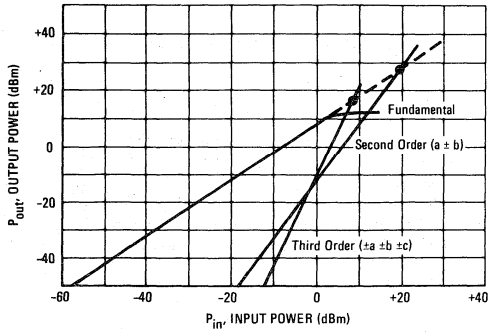


FIGURE 24 – SECOND AND THIRD ORDER INTERCEPT
MWA330

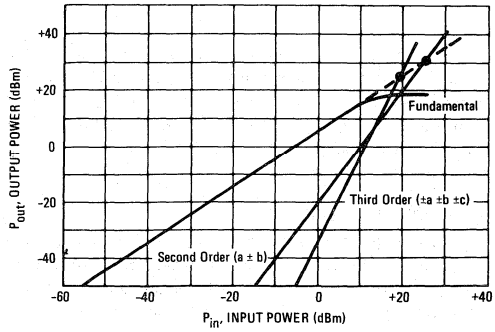


FIGURE 25 – INTERMODULATION DISTORTION
versus POWER OUTPUT
MWA310

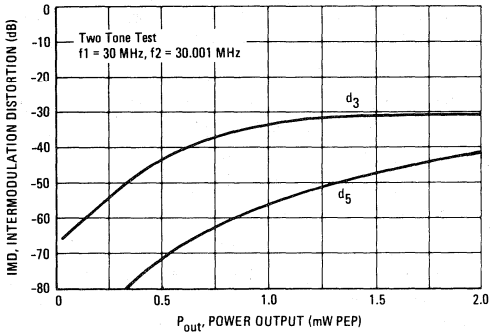


FIGURE 26 – INTERMODULATION DISTORTION
versus POWER OUTPUT
MWA320

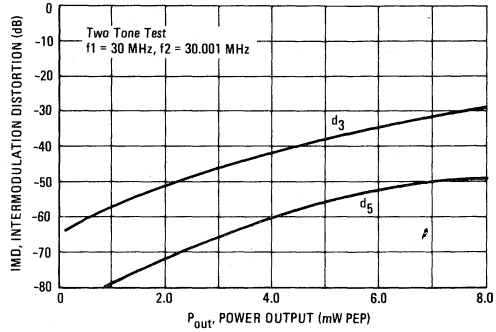


FIGURE 27 – INTERMODULATION DISTORTION
versus POWER OUTPUT
MWA330

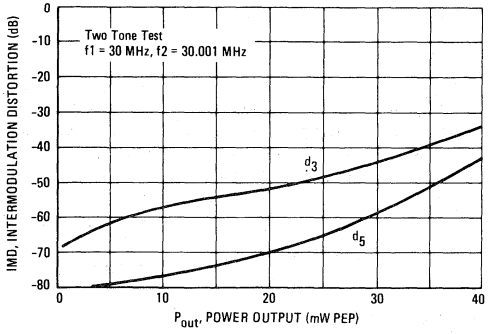
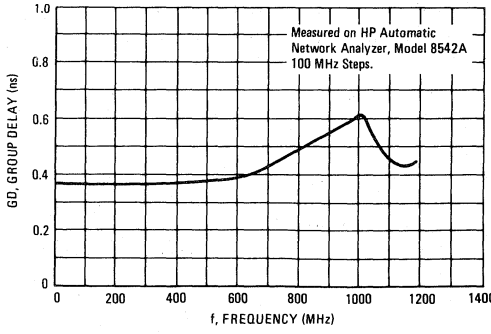


FIGURE 28 – GROUP DELAY versus FREQUENCY
MWA310/MWA320/MWA330



4

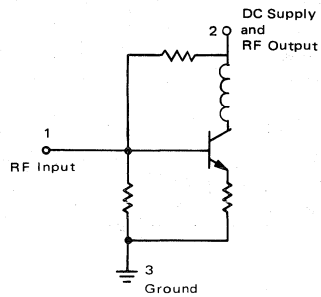
MWA SERIES HYBRID AMPLIFIER APPLICATIONS INFORMATION

The MWA series hybrid amplifiers are designed for wideband general purpose applications in 50 Ω systems. Fully cascadable for any gain combination, operable at voltages as low as 3 Vdc, and external control of the low frequency corner make the MWA amplifiers extremely versatile gain blocks.

Basic Circuit Configuration

Figure 29 shows the basic internal circuit. It is important to note that the specified operating conditions of voltage, current, and external decoupling impedance must be applied to the units in order to achieve the published electrical characteristics.

FIGURE 29 – INTERNAL CIRCUIT



Amplifier Application

The circuit schematic for a simple amplifier design is shown in Figure 30. External to the MWA hybrid amplifier the only components required are:

Decoupling elements – Bypass Capacitor
Decoupling Impedance
(resistor/inductor)
DC Blocking Capacitors at the RF input and output.

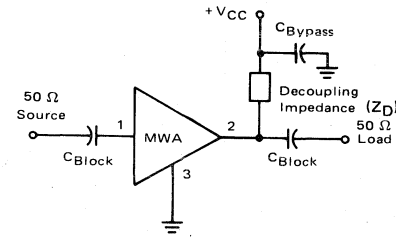
External Decoupling Impedance

In all cases the external bias (decoupling elements) must present an impedance which is large compared to the 50 Ω load impedance to minimize RF gain reduction. The loss in gain due to the decoupling impedance is given by the equation:

$$\text{Loss} = 20 \text{ Log } \frac{Z_D}{Z_D + 25} \text{ dB}$$

where Z_D = decoupling impedance in ohms. For example, if Z_D = 1 kΩ, Loss = 0.214 dB.

FIGURE 30 – AMPLIFIER SCHEMATIC DIAGRAM



Supply Voltage

The value of the external decoupling resistive impedance (R_D) determines the supply voltage ($+V_{CC}$) and is determined by the following equation:

$$V_{CC} = R_D \times I_D + V_D$$

where I_D and V_D are the device current and voltage stated in the data sheet. For example, for MWA110,

$$I_D = 10 \text{ mA}$$
$$V_D = 2.9 \text{ V}$$

and, if R_D = 330 Ω, then

$$V_{CC} = 6.2 \text{ V}$$

More commonly V_{CC} is predetermined and R_D may be calculated from:

$$R_D = \frac{V_{CC} - V_D}{I_D}$$

If an RF choke is used for decoupling, then the supply voltage (V_{CC}) required is equal to the device voltage (V_D).

Low Frequency Response

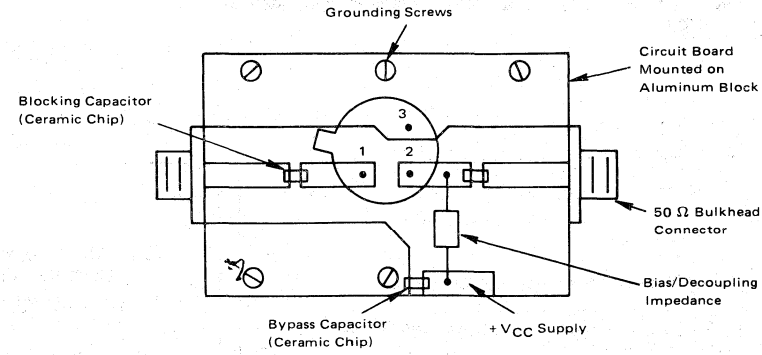
The value of the blocking capacitors determines the low frequency response of the amplifier. The following expression is used to determine the blocking capacitor value to yield a desired 3 dB low frequency corner (f_{LFC}).

$$C_{Block}(\text{Farads}) = \frac{1}{100\,\pi\, f_{LFC}(\text{Hz})}$$

Bypass Capacitor

The reactive impedance of the bypass capacitor should be small compared to the impedance of the decoupling element at the lowest frequency of operation.

FIGURE 31 – TEST FIXTURE



Note: The circuitry indicated is on the underside of the printed circuit board with sockets for the amplifier pins. The case of the amplifier should contact the printed circuit board top surface to ensure effective RF grounding.

Text Fixture

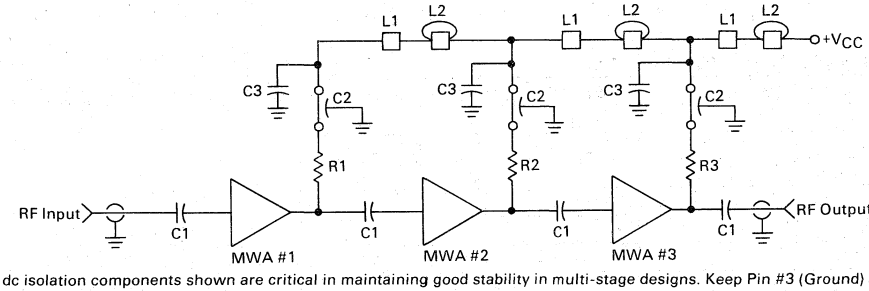
The 50 Ω input/output impedance levels of the MWA hybrids are most easily preserved on a circuit board by using 50 Ω microstrip transmission lines. Figure 31 is an example of a circuit board layout which utilizes microstrip transmission lines in conjunction with other sound RF construction techniques.

The characteristic impedance and corresponding line width of the microstrip are a function of the circuit board dielectric constant and thickness. The table lists appropriate line widths for 50 Ω microstrip lines on commonly used circuit board materials.

MATERIAL TYPE	DIELECTRIC CONSTANT	DIELECTRIC THICKNESS INCHES	LINE WIDTH INCHES
Teflon-Fiberglass	2.5	0.03125 0.0625	0.090 0.180

As in all good RF circuit designs, care should be taken to minimize parasitic lead inductances and to provide adequate grounding.

FIGURE 32 — TYPICAL CASCADE



The dc isolation components shown are critical in maintaining good stability in multi-stage designs. Keep Pin #3 (Ground) as short as possible preferably soldering the case to the ground plane for best gain flatness to 1000 MHz.

C1 — For operation to 400 MHz, 1000 pF, 50 mil Chip Capacitor – ATC 50 mil Case (5.0 MHz L.F.)
C1 — For operation to 1000 MHz, 0.018 mF, Chip Capacitor for 0.25 MHz L.F. Cut-Off
C2 — Feedthru Capacitor Centralab SFT-102, 1000 pF or Metuchen 54-794002-681M, 680 pF
C3 — 0.1 μF Sprague 3CZ5U104X0050C5 – 50 Volt
L1 — Ferroxcube Shielding Bead 56-590-65/4A – Single Wire
L2 — Ferroxcube Shielding Bead 56-590-65/4A – 2 Turns #26 AWG

	Cascade 1	Cascade 2
Frequency Range	0.25 to 400 MHz	5.0 to 1000 MHz
Gain	43.5 dB	20.5 dB
Gain Flatness	±1.0 dB	±0.75 dB
Input VSWR	2.0:1	2.4:1
Output VSWR	1.2:1	2.1:1
V_{CC} Supply	12 Vdc	33 Vdc
I Supply	44 mAdc	150 mAdc
MWA #1	MWA110	MWA320
MWA #2	MWA110	MWA330
MWA #3	MWA120	MWA330
R1	1000 Ω	1000 Ω
R2	1000 Ω	500 Ω
R3	300 Ω	500 Ω

Cascading

The inherent stability of the MWA hybrid modules makes possible the cascading of two or more units with no oscillatory problems. Figure 32 shows a typical 3 hybrid cascade with measured data for 400 MHz and 1000 MHz hybrids.

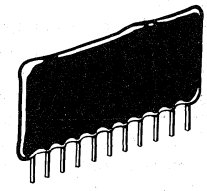
MWA5121

WIDEBAND HYBRID AMPLIFIER

. . . Three stage amplifier designed for broadband linear applications up to 900 MHz.

- Gain 27 dB Typ
- Complete Gain Block; Requires No External Components
- Thick Film Construction
- Low Noise Figure 4.0 dB Typ
- Low Intermodulation Distortion $IM_2 = -45$ dB, $IM_3 = -59$ dB

30–890 MHz WIDEBAND GENERAL-PURPOSE HYBRID AMPLIFIER



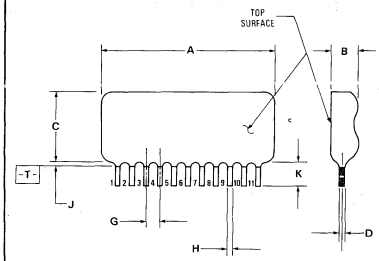
4

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameters	Symbol	Ratings	Unit
Supply Voltage	V_{CC}	24	Vdc
Circuit Current	I_{CC}	50	mAdc
Input Voltage	$V_{I(RF)}$	0.5	Vdc
Input Voltage	$V_{I(DC)}$	±25	Vdc
Output Voltage	$V_{O(DC)}$	±25	Vdc
Total Dissipation	P_T	1.2	W
Operating Temperature	T_{op}	−30 to +65	°C
Storage Temperature	T_{stg}	−30 to +85	°C

RECOMMENDED OPERATING CONDITIONS

Parameters	Symbol	Ratings	Unit
Supply Voltage	V_{CC}	+18 to +22	V
Source Impedance	Z_S	50 to 75	Ω
Load Impedance	Z_L	50 to 75	Ω
Operating Temperature	T_{op}	−10 to +40	°C



Pin 11: IN
Pin 1: OUT
Pin 7: B+
All Others
Gnd

NOTES:
1. -T- IS BOTH A SEATING PLANE AND DATUM SURFACE.
2. POSITIONAL TOLERANCE FOR LEADS (H DIMENSION):
⌖ | 0.15 (0.006) Ⓜ | T |
POSITIONAL TOLERANCE FOR LEADS (D DIMENSION):
⌖ | 0.25 (0.010) Ⓜ | T |
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.99	32.00	1.102	1.260
B	2.54	5.00	0.100	0.197
C	15.49	18.99	0.610	0.748
D	0.12	0.38	0.005	0.015
G	2.54 BSC		0.100 BSC	
H	0.38	0.63	0.015	0.025
J	–	0.99	–	0.039
K	3.99	5.06	0.157	0.200

CASE 790-01

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 20 V, Z_S = Z_L = 50 Ω)

Characteristic		Symbol	Min	Typ	Max	Unit
Operating Current		I_{CC}	35	40	45	mA
Gain (f = 100 MHz)		G	25	27	30	dB
Gain Flatness	(f = 30 to 890 MHz, Z_S = Z_L = 50 Ω) (f = 30 to 890 MHz, Z_S = Z_L = 75 Ω)	—	— —	2.0 2.0	5.0 5.0	dB
Input VSWR	(f = 30 to 890 MHz, Z_S = Z_L = 50 Ω) (f = 30 to 890 MHz, Z_S = Z_L = 75 Ω)	VSWRI	— —	2.1 2.0	3.0 3.0	— —
Output VSWR	(f = 30 to 890 MHz, Z_S = Z_L = 50 Ω) (f = 30 to 890 MHz, Z_S = Z_L = 75 Ω)	VSWRO	— —	1.5 2.0	3.0 3.0	—
Isolation	(f = 30 to 890 MHz)	I_{SO}	—	50	—	dB
Noise Figure	(f = 30 to 300 MHz) (f = 300 to 890 MHz)	NF	— —	3.5 4.0	7.0 8.0	dB

FIGURE 1 — GAIN AND NOISE FIGURE versus FREQUENCY

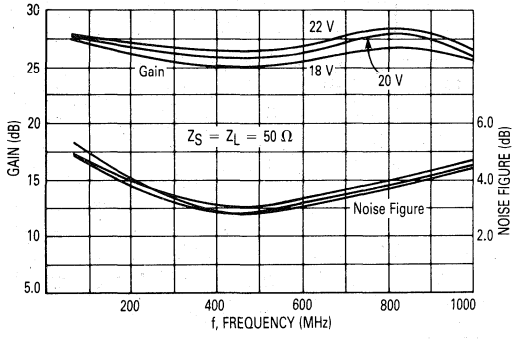


FIGURE 2 — GAIN AND NOISE FIGURE versus FREQUENCY

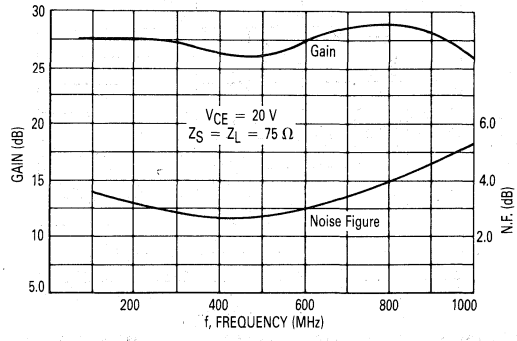


FIGURE 3 — OUTPUT POWER AT 1.0 dB GAIN COMPRESSION versus FREQUENCY

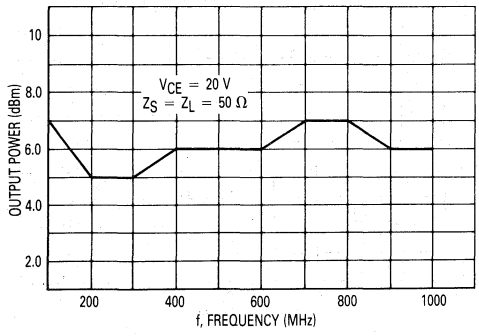


FIGURE 4 — OUTPUT POWER AT 1.0 dB GAIN COMPRESSION versus SUPPLY VOLTAGE

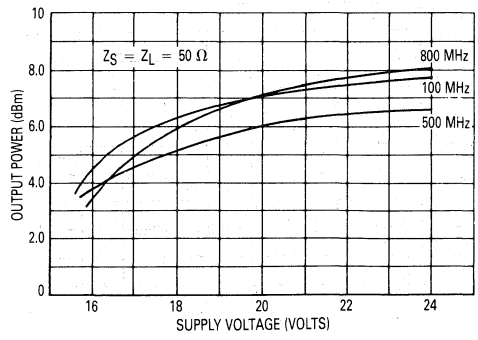


FIGURE 5 — GAIN versus SUPPLY VOLTAGE

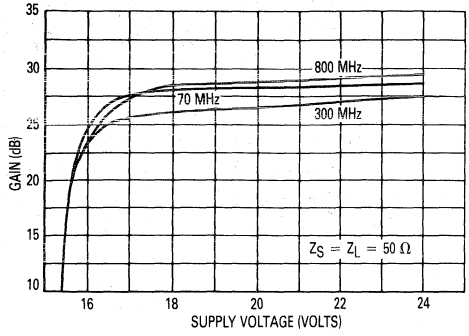


FIGURE 6 — CURRENT DRAIN versus SUPPLY VOLTAGE

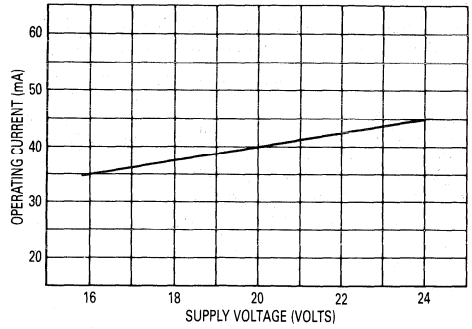


FIGURE 7 — INPUT AND OUTPUT VSWR versus FREQUENCY

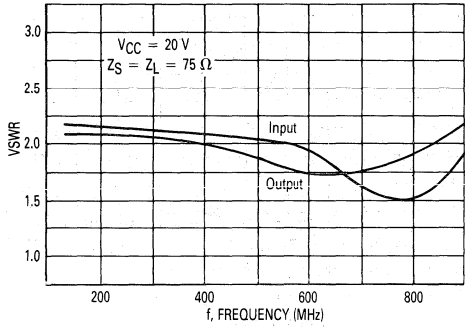


FIGURE 8 — TYPICAL INPUT AND OUTPUT VSWR CHARACTERISTICS

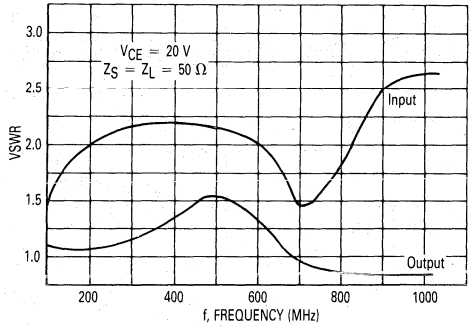


FIGURE 9 — SECOND ORDER INTERMODULATION DISTORTION
f_1 = 55.25 MHz (CH 2)
f_2 = 211.25 MHz (CH 13)
Dist = $f_1 + f_2$

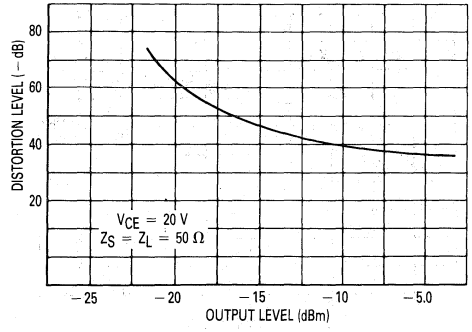
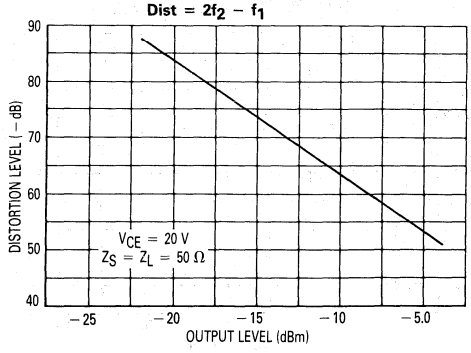


FIGURE 10 — THIRD ORDER INTERMODULATION DISTORTION
f_1 = 199.25 MHz (CH 11)
f_2 = 211.25 MHz (CH 13)
Dist = $2f_2 - f_1$



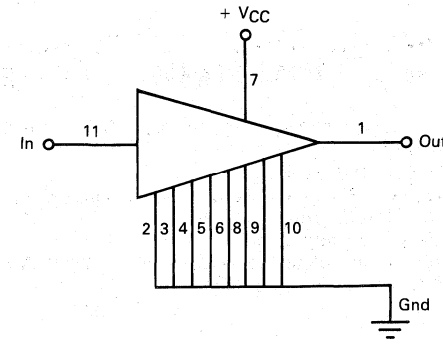
DESCRIPTION AND APPLICATIONS

The MWA5121 is a thick-film hybrid circuit designed for general purpose amplifier applications in the 30 to 890 MHz band. Features are low-noise, flat-gain and low-distortion. The MWA5121 is designed to serve as a broadband, linear gain block with excellent performance in both 50 and 75 ohm systems. The MWA5121 is a complete circuit that requires no additional components or adjustments. Reliability and performance uniformity are assured by gold metallized transistors and stringent quality control procedures.

THERMAL DESIGN CONSIDERATIONS

The MWA5121 does not require a thermal radiator; however, it is necessary to keep the ambient temperature between −30 to +85°C.

FIGURE 11 — AMPLIFIER CONFIGURATION



HANDLING PRECAUTIONS

Soldering must be performed under the following conditions:

- Hand soldering: 2.4 mm minimum from the root of the leads at 260°C maximum for 2 seconds (per line) maximum.
- Solder dip: 2.5 mm minimum from the root of the leads at 260°C maximum for 5 seconds (total) maximum.

If an unknown impedance is connected, caution should be exercised against oscillations. Be sure to isolate the input and output and adequate grounding must be provided. Remember, the MWA5121 is packaged in resin and unnecessary problems may occur when other circuit elements are allowed to couple through the unshielded IC.

4

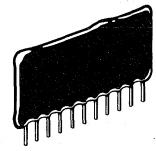
Wideband Hybrid Amplifier

MWA5157

. . . three stage amplifier designed for broadband linear applications up to 900 MHz.

- Gain 24 dB Typical
- Complete Gain Block; Requires No External Components
- Thick Film Construction
- Low Noise Figure 5 dB Typical
- Low Intermodulation Distortion IM_2 = −45 dB, IM_3 = −59 dB
- Supply Voltage = 12 V Nominal

30–890 MHz WIDEBAND GENERAL-PURPOSE HYBRID AMPLIFIER



CASE 790-01
PLASTIC

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameters	Symbol	Ratings	Unit
Supply Voltage	V_{CC}	16	Vdc
Circuit Current	I_{CC}	65	mAdc
Input Voltage	$V_{I(RF)}$	0.5	V
Input Voltage	$V_{I(DC)}$	±25	Vdc
Output Voltage	$V_{O(DC)}$	±25	Vdc
Total Dissipation	P_T	1.2	W
Operating Temperature	T_{op}	−30 to +65	°C
Storage Temperature	T_{stg}	−30 to +85	°C

RECOMMENDED OPERATING CONDITIONS

Parameters	Symbol	Ratings	Unit
Supply Voltage	V_{CC}	10 to 14	V
Source Impedance	Z_S	50 to 75	Ω
Load Impedance	Z_L	50 to 75	Ω
Operating Temperature	T_{op}	−10 to +40	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12 V, Z_S = Z_L = 50 Ω, unless specified otherwise)

Characteristic		Symbol	Min	Typ	Max	Unit
Operating Current		I_{CC}	33	43	53	mA
Gain (f = 100 MHz)		G	22	24	26	dB
Gain Flatness	(f = 30 to 890 MHz, Z_S = Z_L = 50 Ω) (f = 30 to 890 MHz, Z_S = Z_L = 75 Ω)	—	— —	2 2	5 5	dB
Input VSWR	(f = 30 to 890 MHz, Z_S = Z_L = 50 Ω) (f = 30 to 890 MHz, Z_S = Z_L = 75 Ω)	VSWRI	— —	1.5 1.75	3 3	— —
Output VSWR	(f = 30 to 890 MHz, Z_S = Z_L = 50 Ω) (f = 30 to 890 MHz, Z_S = Z_L = 75 Ω)	VSWRO	— —	1.5 1.75	3 3	—
Isolation	(f = 30 to 890 MHz)	I_{SO}	—	50	—	dB
Noise Figure	(f = 30 to 300 MHz) (f = 300 to 890 MHz)	NF	— —	4.5 5	7 8	dB

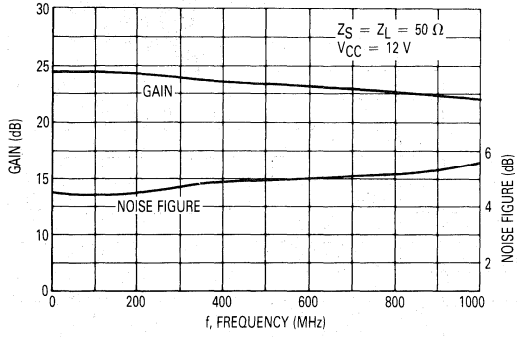


Figure 1. Gain and Noise Figure versus Frequency

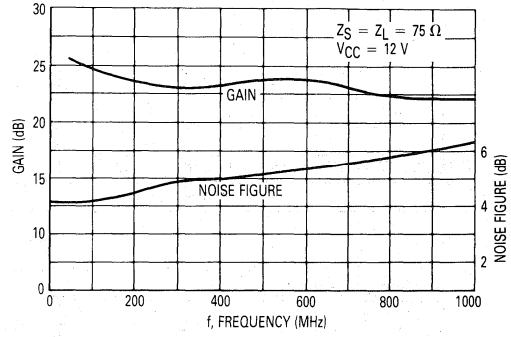


Figure 2. Gain and Noise Figure versus Frequency

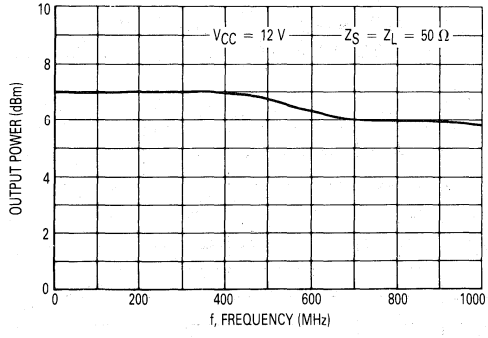


Figure 3. Output Power at 1 dB Gain Compression versus Frequency

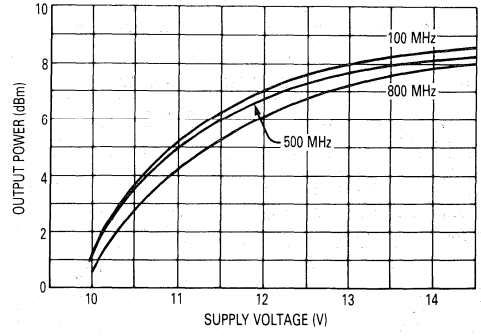


Figure 4. Output Power at 1 dB Gain Compression versus Supply Voltage

4

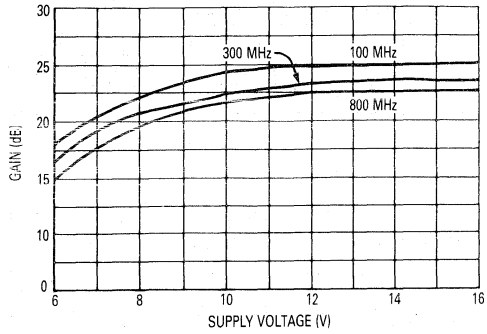


Figure 5. Gain versus Supply Voltage

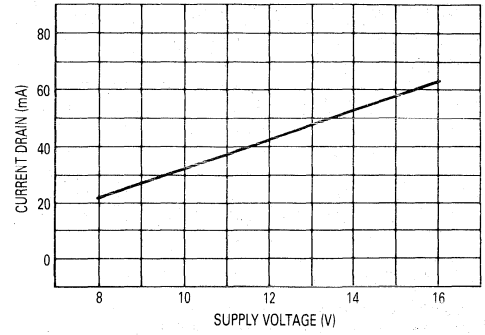


Figure 6. Current Drain versus Supply Voltage

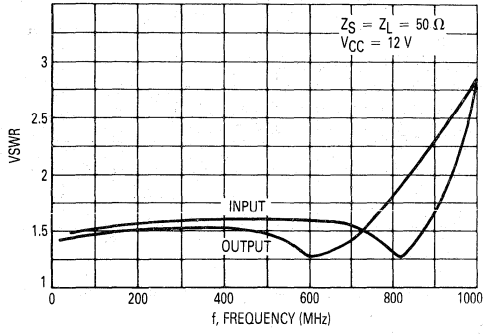


Figure 7. Input and Output VSWR versus Frequency

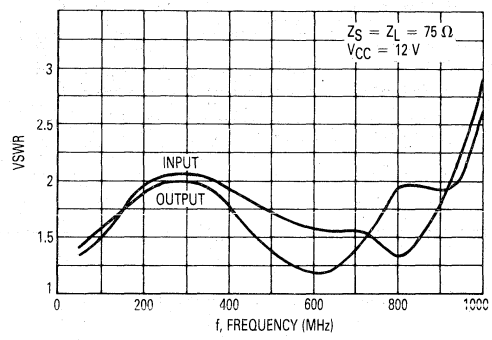


Figure 8. Input and Output VSWR versus Frequency

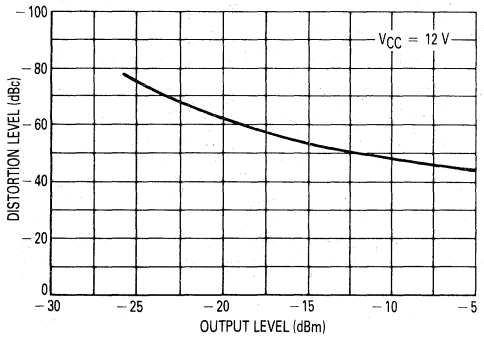


Figure 9. Second Order Intermodulation Distortion
f_1 = 55.25 MHz (CH 2)
f_2 = 211.25 MHz (CH 13)
Dist = $f_1 + f_2$

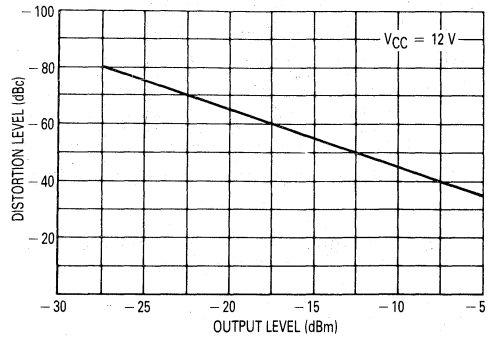


Figure 10. Third Order Intermodulation Distortion
f_1 = 199.25 MHz (CH 11)
f_2 = 211.25 MHz (CH 13)
Dist = $2f_2 - f_1$

DESCRIPTION AND APPLICATIONS

The MWA5157 is a thick-film hybrid circuit designed for general purpose amplifier applications in the 30 to 890 MHz band. Features are low-noise, flat-gain and low-distortion. The MWA5157 is designed to serve as a broadband, linear gain block with excellent performance in both 50 and 75 ohm systems. The MWA5157 is a complete circuit that requires no additional components or adjustments. Reliability and performance uniformity are assured by gold metallized transistors and stringent quality control procedures.

THERMAL DESIGN CONSIDERATIONS

The MWA5157 does not require a thermal radiator; however, it is necessary to keep the ambient temperature between −30 to +85°C.

HANDLING PRECAUTIONS

Soldering must be performed under the following conditions:

- Hand soldering: 2.4 mm minimum from the root of the leads at 260°C maximum for 2 seconds (per line) maximum.
- Solder dip: 2.5 mm minimum from the root of the leads at 260°C maximum for 5 seconds (total) maximum.

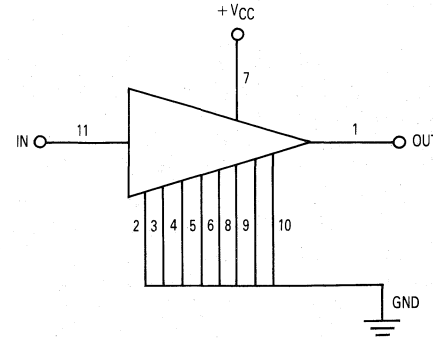
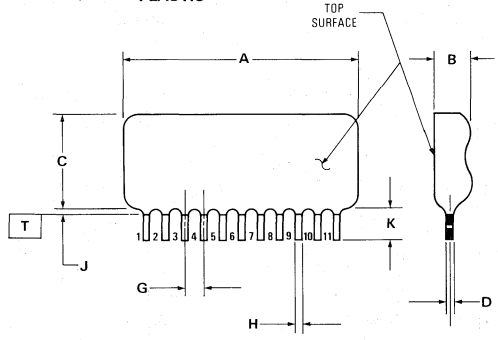


Figure 11. Amplifier Configuration

If an unknown impedance is connected, caution should be exercised against oscillations. Be sure to isolate the input and output and adequate grounding must be provided. Remember, the MWA5157 is packaged in resin and unnecessary problems may occur when other circuit elements are allowed to couple through the unshielded IC.

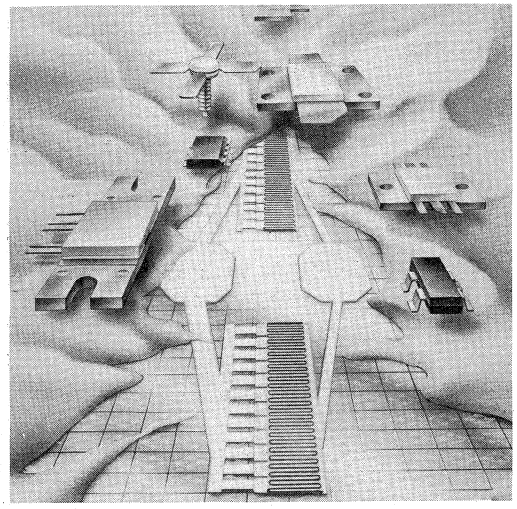
OUTLINE DIMENSIONS

CASE 790-01
PLASTIC



NOTES:
1. T IS BOTH A-SEATING PLANE AND DATUM SURFACE.
2. POSITIONAL TOLERANCE FOR LEADS (H DIMENSION):
   ⌖ | 0.15 (0.006) Ⓜ | T
   POSITIONAL TOLERANCE FOR LEADS (D DIMENSION):
   ⌖ | 0.25 (0.010) Ⓜ | T
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.99	32.00	1.102	1.260
B	2.54	5.00	0.100	0.197
C	15.49	18.99	0.610	0.748
D	0.12	0.38	0.005	0.015
G	2.54 BSC		0.100 BSC	
H	0.38	0.63	0.015	0.025
J	–	0.99	–	0.039
K	3.99	5.06	0.157	0.200



Tuning, Hot Carrier and PIN Diodes

5

1N5139 thru 1N5148
1N5139A thru 1N5148A

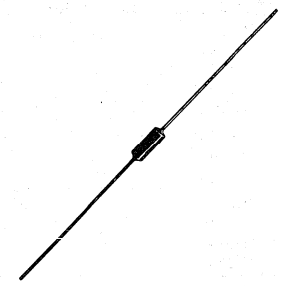
SILICON EPICAP DIODES

. . . designed for electronic tuning and harmonic-generation applications, and providing solid-state reliability to replace mechanical tuning methods.

- Guaranteed High-Frequency Q
- Guaranteed Wide Tuning Range
- Guaranteed Temperature Coefficient
- Standard 10% Capacitance Tolerance
- Complete Typical Design Curves

6.8-47 pF EPICAP VOLTAGE-VARIABLE CAPACITANCE DIODES

SILICON
EPITAXIAL PASSIVATED

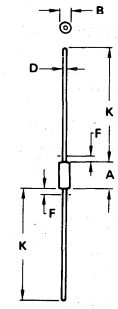


MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	60	Volts
Forward Current	I_F	250	mA
RF Power Input†	P_{in}	5	Watts
Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	400 2.67	mW mW/°C
Device Dissipation @ T_C = 25°C Derate above 25°C	P_C	2.0 13.3	Watts mW/°C
Junction Temperature	T_J	+175	°C
Storage Temperature Range	T_{stg}	−65 to +200	°C

†The RF power input rating assumes that an adequate heat sink is provided.

NOTES:
1. PACKAGE CONTOUR OPTIONAL WITHIN DIA B AND LENGTH A. HEAT SLUGS, IF ANY, SHALL BE INCLUDED WITHIN THIS CYLINDER, BUT SHALL NOT BE SUBJECT TO THE MIN LIMIT OF DIA B.
2. LEAD DIA NOT CONTROLLED IN ZONES F, TO ALLOW FOR FLASH, LEAD FINISH BUILDUP, AND MINOR IRREGULARITIES OTHER THAN HEAT SLUGS.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.84	7.62	0.230	0.300
B	2.16	2.72	0.085	0.107
D	0.46	0.56	0.018	0.022
F	–	1.27	–	0.050
K	25.40	38.10	1.000	1.500

All JEDEC dimensions and notes apply

CASE 51-02
DO-204AA

5

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic — All Types	Test Conditions	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage	I_R = 10 μAdc	BV_R	60	70	—	Vdc
Reverse Voltage Leakage Current	V_R = 55 Vdc, T_A = 25°C V_R = 55 Vdc, T_A = 150°C	I_R	— —	— —	0.02 20	μAdc
Series Inductance	f = 250 MHz, L ≈ 1/16"	L_S	—	5	—	nH
Case Capacitance	f = 1 MHz, L ≈ 1/16"	C_C	—	0.25	—	pF
Diode Capacitance Temperature Coefficient	V_R = 4 Vdc, f = 1 MHz	TC_C	—	200	300	ppm/°C

	C_T, Diode Capacitance V_R = 4 Vdc, f = 1 MHz pF			Q, Figure of Merit V_R = 4 Vdc, f = 50 MHz	α V_R = 4 Vdc, f = 1 MHz		TR, Tuning Ratio C_4/C_{60} f = 1 MHz	
Device	Min	Typ	Max	Min	Min	Typ	Min	Typ
1N5139	6.1	6.8	7.5	350	0.37	0.40	2.7	2.9
1N5139A	6.5	6.8	7.1	350	0.37	0.40	2.7	2.9
1N5140	9.0	10.0	11.0	300	0.38	0.41	2.8	3.0
1N5140A	9.5	10.0	10.5	300	0.38	0.41	2.8	3.0
1N5141	10.8	12.0	13.2	300	0.38	0.41	2.8	3.0
1N5141A	11.4	12.0	12.6	300	0.38	0.41	2.8	3.0
1N5142	13.5	15.0	16.5	250	0.38	0.41	2.8	3.0
1N5142A	14.3	15.0	15.7	250	0.38	0.41	2.8	3.0
1N5143	16.2	18.0	19.8	250	0.38	0.41	2.8	3.0
1N5143A	17.1	18.0	18.9	250	0.38	0.41	2.8	3.0
1N5144	19.8	22.0	24.2	200	0.43	0.45	3.2	3.4
1N5144A	20.9	22.0	23.1	200	0.43	0.45	3.2	3.4
1N5145	24.3	27.0	29.7	200	0.43	0.45	3.2	3.4
1N5145A	25.7	27.0	28.3	200	0.43	0.45	3.2	3.4
1N5146	29.7	33.0	36.3	200	0.43	0.45	3.2	3.4
1N5146A	31.4	33.0	34.6	200	0.43	0.45	3.2	3.4
1N5147	36.1	39.0	42.9	200	0.43	0.45	3.2	3.4
1N5147A	37.1	39.0	40.9	200	0.43	0.45	3.2	3.4
1N5148	42.3	47.0	51.7	200	0.43	0.45	3.2	3.4
1N5148A	44.7	47.0	49.3	200	0.43	0.45	3.2	3.4

PARAMETER TEST METHODS

1. L_S, SERIES INDUCTANCE
L_S is measured on a shorted package at 250 MHz using an impedance bridge (Boonton Radio Model 250A RX Meter). L = lead length.

2. C_C, CASE CAPACITANCE
C_C is measured on an open package at 1 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).

3. C_T, DIODE CAPACITANCE
($C_T = C_C + C_J$). C_T is measured at 1 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).

4. TR, TUNING RATIO
TR is the ratio of C_T measured at 4 Vdc divided by C_T measured at 60 Vdc.

5. Q, FIGURE OF MERIT
Q is calculated by taking the G and C readings of an admittance bridge at the specified frequency and substituting in the following equations:

$$Q = \frac{2\pi fC}{G}$$

(Boonton Electronics Model 33AS8).

6. α, DIODE CAPACITANCE REVERSE VOLTAGE SLOPE
The diode capacitance, C_T (as measured at V_R = 4 Vdc, f = 1 MHz) is compared to C_T (as measured at V_R = 60 Vdc, f = 1 MHz) by the following equation which defines α.

$$\alpha = \frac{\log C_T(4) - \log C_T(60)}{\log 60 - \log 4}$$

Note that a C_T versus V_R law is assumed as shown in the following equation where C_C is included.

$$C_T = \frac{K}{V^\alpha}$$

7. TC_C, DIODE CAPACITANCE TEMPERATURE COEFFICIENT
TC_C is guaranteed by comparing C_T at V_R = 4 Vdc, f = 1 MHz, T_A = −65°C with C_T at V_R = 4 Vdc, f = 1 MHz, T_A = +85°C in the following equation which defines TC_C:

$$TC_C = \left|\frac{C_T(+85°C) - C_T(-65°C)}{85 + 65}\right| \cdot \frac{10^6}{C_T(25°C)}$$

FIGURE 1 — DIODE CAPACITANCE versus REVERSE VOLTAGE

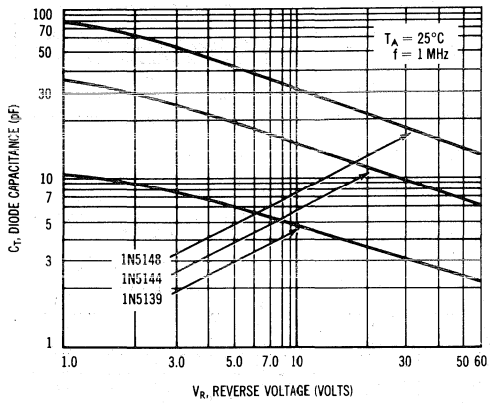


FIGURE 2 — FIGURE OF MERIT versus REVERSE VOLTAGE

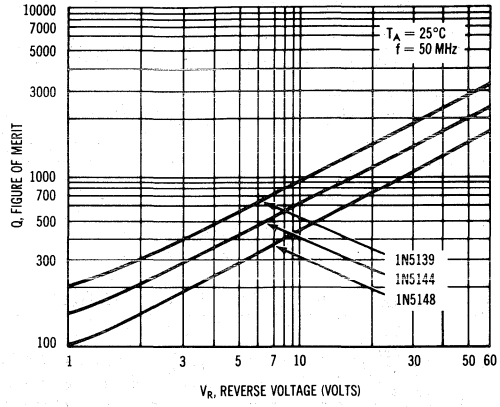


FIGURE 3 — NORMALIZED DIODE CAPACITANCE versus JUNCTION TEMPERATURE

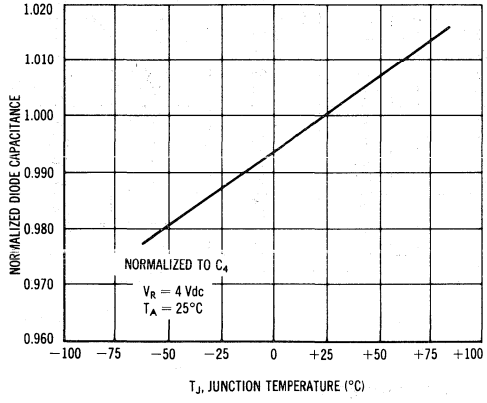


FIGURE 4 — NORMALIZED FIGURE OF MERIT versus JUNCTION TEMPERATURE

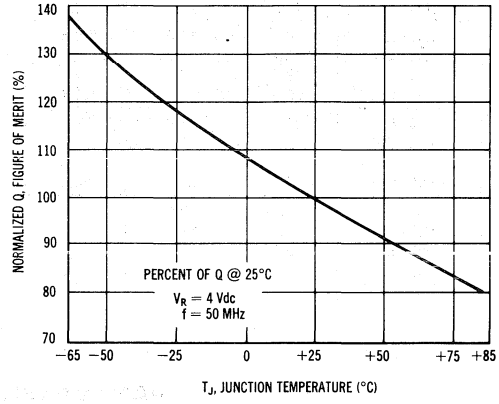


FIGURE 5 — REVERSE CURRENT versus REVERSE BIAS VOLTAGE

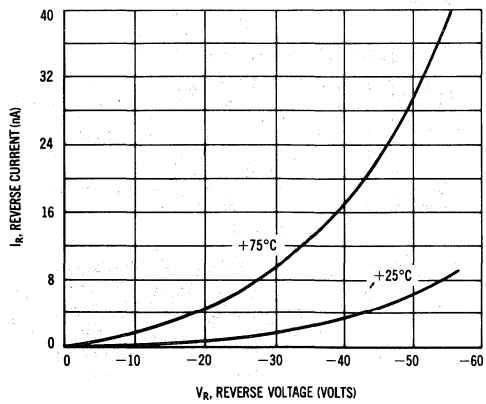
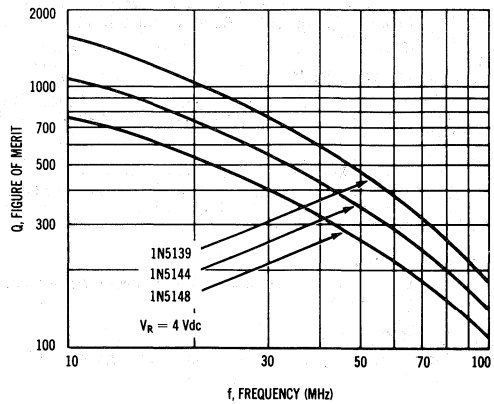


FIGURE 6 — FIGURE OF MERIT versus FREQUENCY



5

1N5441A,B thru 1N5456A,B

VVC

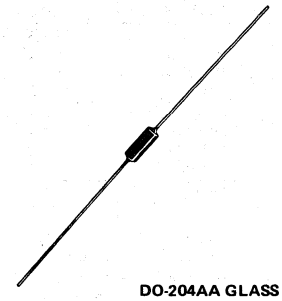
SILICON EPICAP DIODES

. . . epitaxial passivated abrupt junction tuning diodes designed for electronic tuning, FM, AFC and harmonic-generation applications in AM through UHF ranges, providing solid-state reliability to replace mechanical tuning methods.

- Excellent Q Factor at High Frequencies
- Guaranteed Capacitance Change — 2.0 to 30 V
- Guaranteed Temperature Coefficient
- Capacitance Tolerance — 10% and 5.0%
- Complete Typical Design Curves

VOLTAGE-VARIABLE CAPACITANCE DIODES

6.8 – 100 pF
30 VOLTS

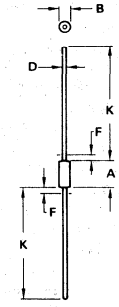


DO-204AA GLASS

* MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	30	Volts
Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	400 2.67	mW mW/°C
Operating Junction Temperature Range	T_J	+175	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.84	7.62	0.230	0.300
B	2.16	2.72	0.085	0.107
D	0.46	0.56	0.018	0.022
F	–	1.27	–	0.050
K	25.40	38.10	1.000	1.500

All JEDEC dimensions and notes apply

CASE 51-02
DO-204AA

5

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic—All Types	Test Conditions	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage	I_R = 10 μAdc	$V_{(BR)R}$	30	–	–	Vdc
Reverse Voltage Leakage Current	V_R = 25 Vdc, T_A = 25°C V_R = 25 Vdc, T_A = 150°C	I_R	– –	– –	0.02 20	μAdc
Series Inductance	f = 250 MHz, lead length≈1/16"	L_S	–	4.0	10	nH
Case Capacitance	f = 1.0 MHz, lead length≈1/16"	C_C	0.1	0.17	0.25	pF
Diode Capacitance Temperature Coefficient (Note 6)	V_R = 4.0 Vdc, f = 1.0 MHz	TC_C	–	300	400	ppm/°C

Device	C_T, Diode Capacitance (1) V_R = 4.0 Vdc, f = 1.0 MHz pF			TR, Tuning Ratio C_2/C_{30} f = 1.0 MHz		Q, Figure of Merit V_R = 4.0 Vdc f = 50 MHz
	Min (Nom -10%)	Nom	Max (Nom +10%)	Min	Max	Min
1N5441A	6.1	6.8	7.5	2.5	3.1	450
1N5442A	7.4	8.2	9.0	2.5	3.1	450
1N5443A	9.0	10.0	11.0	2.6	3.1	400
1N5444A	10.8	12.0	13.2	2.6	3.1	400
1N5445A	13.5	15.0	16.5	2.6	3.1	400
1N5446A	16.2	18.0	19.8	2.6	3.1	350
1N5447A	18.0	20.0	22.0	2.6	3.1	350
1N5448A	19.8	22.0	24.2	2.6	3.2	350
1N5449A	24.3	27.0	29.7	2.6	3.2	350
1N5450A	29.7	33.0	36.3	2.6	3.2	350
1N5451A	35.1	39.0	42.9	2.6	3.2	300
1N5452A	42.3	47.0	51.7	2.6	3.2	250
1N5453A	50.4	56.0	61.6	2.6	3.3	200
1N5454A	61.2	68.0	74.8	2.7	3.3	175
1N5455A	73.8	82.0	90.2	2.7	3.3	175
1N5456A	90.0	100.0	110.0	2.7	3.3	175

(1) To order devices with C_T Nom ±5.0% add Suffix B.
*Indicates JEDEC Registered Data.

PARAMETER TEST METHODS

1. **L_S, Series Inductance**
   L_S is measured on a shorted package at 250 MHz using an impedance bridge (Boonton Radio Model 250A RX Meter or equivalent).
2. **C_C, Case Capacitance**
   C_C is measured on an open package at 1.0 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).
3. **C_T, Diode Capacitance**
   ($C_T = C_C + C_J$). C_T is measured at 1.0 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).
4. **TR, Tuning Ratio**
   TR is the ratio of C_T measured at 2.0 Vdc divided by C_T measured at 30 Vdc.
5. **Q, Figure of Merit**
   Q is calculated by taking the G and C readings of an admittance bridge at the specified frequency and substituting in the following equations:

$$Q = \frac{2\pi fC}{G}$$

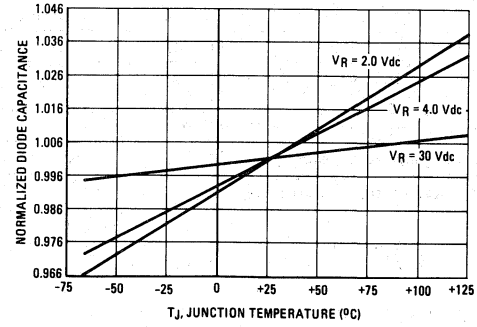
(Boonton Electronics Model 33AS8 or equivalent).

6. **TC_C, Diode Capacitance Temperature Coefficient**
   TC_C is guaranteed by comparing C_T at V_R = 4.0 Vdc, f = 1.0 MHz, T_A = -65°C with C_T at V_R = 4.0 Vdc, f = 1.0 MHz, T_A = +85°C in the following equation, which defines TC_C:

$$TC_C = \left| \frac{C_T(+85^\circ C) - C_T(-65^\circ C)}{85 + 65} \right| \frac{10^6}{C_T(25^\circ C)}$$

Accuracy limited by C_T measurement to ±0.1 pF.

FIGURE 1 – NORMALIZED DIODE CAPACITANCE versus JUNCTION TEMPERATURE



TYPICAL DEVICE PERFORMANCE

FIGURE 2 – DIODE CAPACITANCE versus REVERSE VOLTAGE

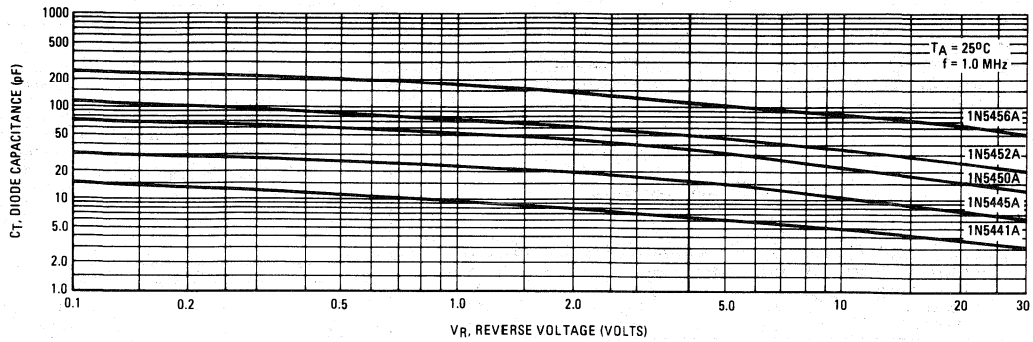


FIGURE 3 – FIGURE OF MERIT versus REVERSE VOLTAGE

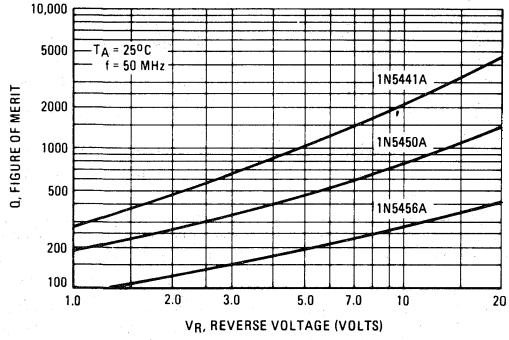


FIGURE 4 – FIGURE OF MERIT versus FREQUENCY

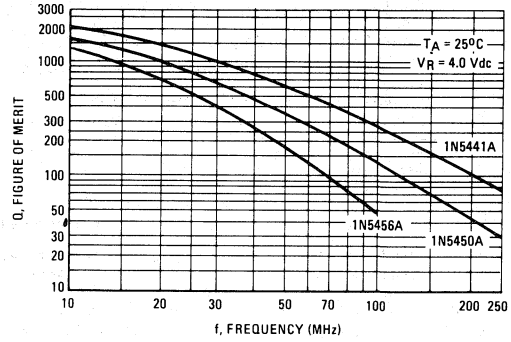


FIGURE 5 – REVERSE CURRENT versus REVERSE BIAS VOLTAGE

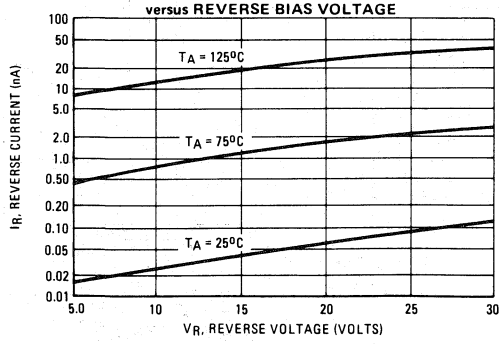
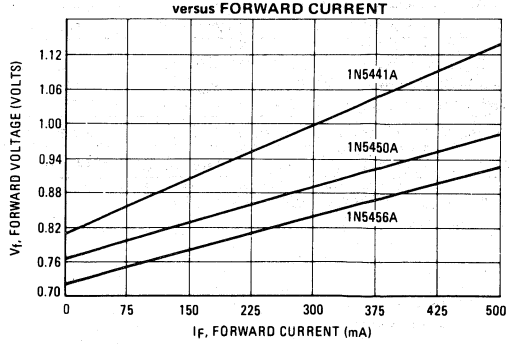


FIGURE 6 – FORWARD VOLTAGE versus FORWARD CURRENT



5

1N5461A,B thru 1N5476A,B

VVC

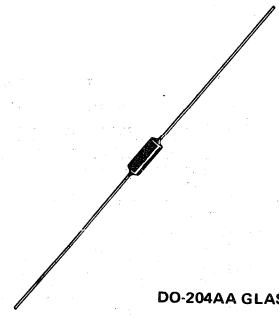
SILICON EPICAP DIODES

. . . a PREMIUM line of epitaxial, passivated, abrupt-junction tuning diodes for critical and sophisticated frequency control applications through the UHF range.

- High Q at High Frequencies
- Guaranteed High Capacitance Tuning Range
- Excellent Unit-to-Unit Uniformity
- Guaranteed Temperature Coefficient
- Capacitance Tolerances — 10% and 5.0%
- Complete Typical Design Curves

VOLTAGE-VARIABLE CAPACITANCE DIODES

6.8 – 100 pF
30 VOLTS



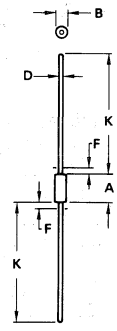
DO-204AA GLASS

5

***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	30	Volts
Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	400 2.67	mW mW/°C
Operating Junction Temperature Range	T_J	+175	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.84	7.62	0.230	0.300
B	2.16	2.72	0.085	0.107
D	0.46	0.56	0.018	0.022
F	–	1.27	–	0.050
K	25.40	38.10	1.000	1.500

All JEDEC dimensions and notes apply

CASE 51-02
DO-204AA

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic—All Types	Test Conditions	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage	I_R = 10 μAdc	$V_{(BR)R}$	30	–	–	Vdc
Reverse Voltage Leakage Current	V_R = 25 Vdc, T_A = 25°C V_R = 25 Vdc, T_A = 150°C	I_R	– –	– –	0.02 20	μAdc
Series Inductance	f = 250 MHz, lead length ≈1/16"	L_S	–	4.0	10	nH
Case Capacitance	f = 1.0 MHz, lead length ≈ 1/16"	C_C	0.1	0.17	0.25	pF
Diode Capacitance Temperature Coefficient (Note 6)	V_R = 4.0 Vdc, f = 1.0 MHz	TC_C	–	300	400	ppm/°C

Device	C_T, Diode Capacitance (1) V_R = 4.0 Vdc, f = 1.0 MHz pF			TR, Tuning Ratio C_2/C_{30} f = 1.0 MHz		Q, Figure of Merit V_R = 4.0 Vdc f = 50 MHz
	Min (Nom -10%)	Nom	Max (Nom +10%)	Min	Max	Min
1N5461A	6.1	6.8	7.5	2.7	3.1	600
1N5462A	7.4	8.2	9.0	2.8	3.1	600
1N5463A	9.0	10.0	11.0	2.8	3.1	550
1N5464A	10.8	12.0	13.2	2.8	3.1	550
1N5465A	13.5	15.0	16.5	2.8	3.1	550
1N5466A	16.2	18.0	19.8	2.9	3.1	500
1N5467A	18.0	20.0	22.0	2.9	3.1	500
1N5468A	19.8	22.0	24.2	2.9	3.2	500
1N5469A	24.3	27.0	29.7	2.9	3.2	500
1N5470A	29.7	33.0	36.3	2.9	3.2	500
1N5471A	35.1	39.0	42.9	2.9	3.2	450
1N5472A	42.3	47.0	51.7	2.9	3.2	400
1N5473A	50.4	56.0	61.6	2.9	3.3	300
1N5474A	61.2	68.0	74.8	2.9	3.3	250
1N5475A	73.8	82.0	90.2	2.9	3.3	225
1N5476A	90.0	100.0	110.0	2.9	3.3	200

(1) To order devices with C_T Nom ±5.0% add Suffix B.
*Indicates JEDEC Registered Data.

PARAMETER TEST METHODS

1. **L_S, Series Inductance**
   L_S is measured on a shorted package at 250 MHz using an impedance bridge (Boonton Radio Model 250A RX Meter or equivalent).
2. **C_C, Case Capacitance**
   C_C is measured on an open package at 1.0 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).
3. **C_T, Diode Capacitance**
   ($C_T = C_C + C_J$). C_T is measured at 1.0 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).
4. **TR, Tuning Ratio**
   TR is the ratio of C_T measured at 2.0 Vdc divided by C_T measured at 30 Vdc.
5. **Q, Figure of Merit**
   Q is calculated by taking the G and C readings of an admittance bridge at the specified frequency and substituting in the following equations:

$$Q = \frac{2\pi fC}{G}$$

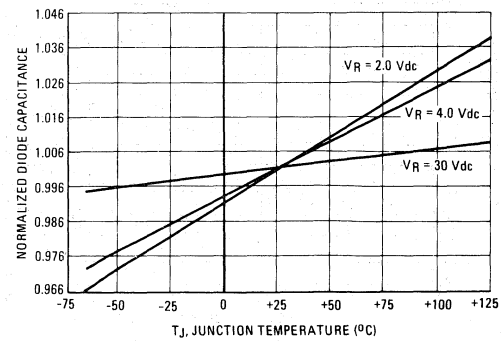
(Boonton Electronics Model 33AS8 or equivalent).

6. **TC_C, Diode Capacitance Temperature Coefficient**
   TC_C is guaranteed by comparing C_T at V_R = 4.0 Vdc, f = 1.0 MHz, T_A = -65°C with C_T at V_R = 4.0 Vdc, f = 1.0 MHz, T_A = +85°C in the following equation, which defines TC_C:

$$TC_C = \left| \frac{C_T(+85^\circ C) - C_T(-65^\circ C)}{85 + 65} \right| \frac{10^6}{C_T(25^\circ C)}$$

Accuracy limited by C_T measurement to ±0.1 pF.

FIGURE 1 — NORMALIZED DIODE CAPACITANCE versus JUNCTION TEMPERATURE



5

TYPICAL DEVICE PERFORMANCE

FIGURE 2 – DIODE CAPACITANCE versus REVERSE VOLTAGE

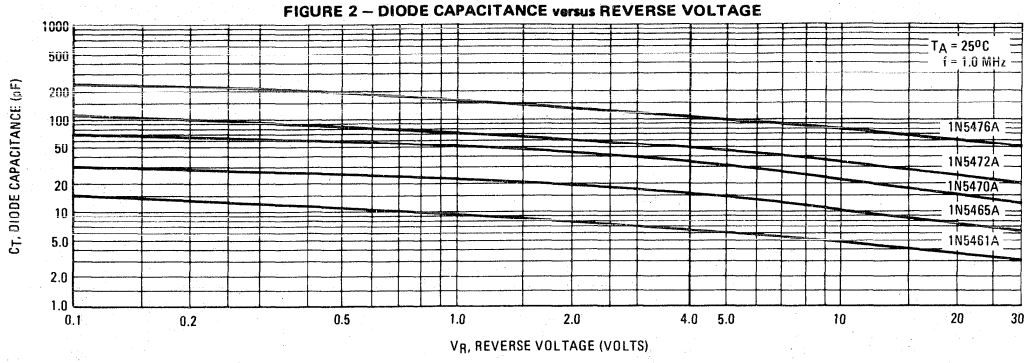


FIGURE 3 – FIGURE OF MERIT versus REVERSE VOLTAGE

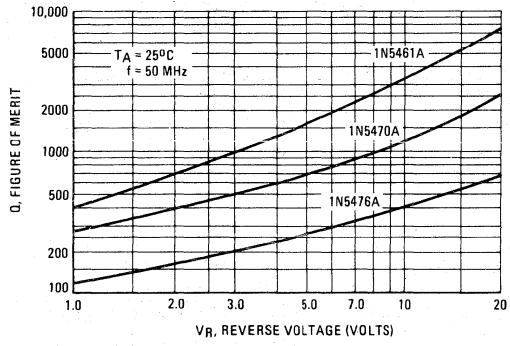


FIGURE 4 – FIGURE OF MERIT versus FREQUENCY

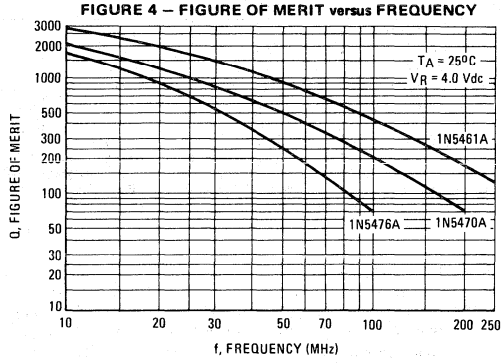


FIGURE 5 – REVERSE CURRENT versus REVERSE BIAS VOLTAGE

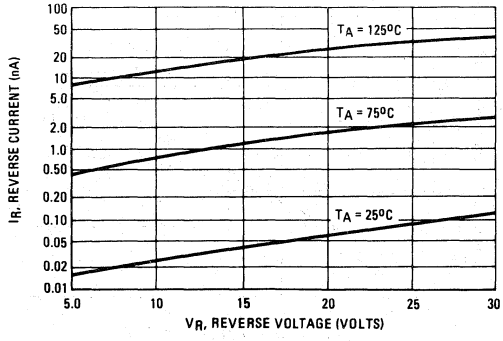
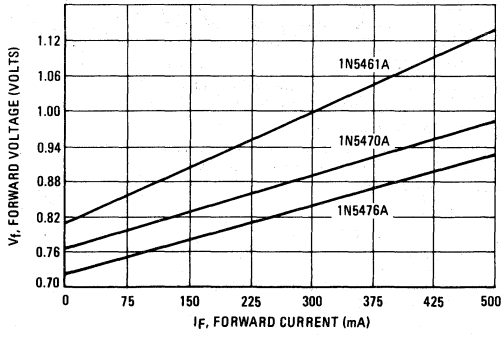


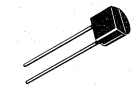
FIGURE 6 – FORWARD VOLTAGE versus FORWARD CURRENT



5

MBD101
MMBD101
MMBD101L

SILICON HOT-CARRIER UHF MIXER DIODE



CASE 182-02
TO-226AC



CASE 318-02
TO-236AA
SOT-23

SILICON HOT-CARRIER DIODE (SCHOTTKY BARRIER DIODE)

. . . designed primarily for UHF mixer applications but suitable also for use in detector and ultra-fast switching circuits. Supplied in an inexpensive plastic package for low-cost, high-volume consumer requirements. Also available in Surface Mount package.

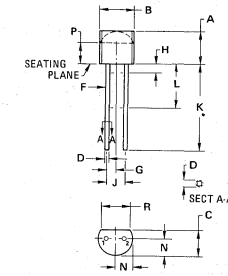
- The Rugged Schottky Barrier Construction Provides Stable Characteristics by Eliminating the "Cat-Whisker" Contact
- Low Noise Figure — 6.0 dB Typ @ 1.0 GHz
- Very Low Capacitance — Less Than 1.0 pF @ Zero Volts
- High Forward Conductance — 0.50 Volts (Typ) @ I_F = 10 mA

MAXIMUM RATINGS

		MBD101	MMBD101,L	
Rating	**Symbol**	**Value**		**Unit**
Reverse Voltage	V_R	4.0		Volts
Forward Power Dissipation @ T_A = 25°C Derate above 25°C	P_F	280 2.8	200 2.0	mW mW/°C
Junction Temperature	T_J	+125		°C
Storage Temperature Range	T_{stg}	−65 to +150		°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μA)	$V_{(BR)R}$	4.0	5.0	–	Volts
Diode Capacitance (V_R = 0, f = 1.0 MHz, Note 1)	C_T	–	0.88	1.0	pF
Forward Voltage (1) (I_F = 10 mA)	V_F	–	0.50	0.60	Volts
Noise Figure (f = 1.0 GHz, Note 2)	NF	–	6.0	—	dB
Reverse Leakage (V_R = 3.0 V)	I_R	–	0.02	0.25	μA

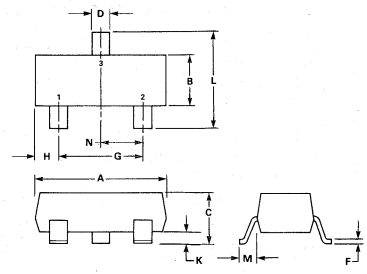


STYLE 1:
PIN 1. ANODE
2. CATHODE

CASE 182-02
TO-226AC

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.356	0.533	0.014	0.021
F	0.407	0.482	0.016	0.019
G	1.27 BSC		0.050 BSC	
H	–	1.27	–	0.050
J	2.54 BSC		0.100 BSC	
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.66	0.080	0.105
P	2.93	–	0.115	–
R	3.43	–	0.135	–

All JEDEC dimensions and notes apply



STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

CASE 318-02
TO-236AA
SOT-23

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.85	1.20	0.033	0.0472
D	0.37	0.50	0.0150	0.020
F	0.085	0.130	0.0034	0.0051
G	1.78	2.04	0.0701	0.0807
H	0.45	0.60	0.0177	0.0236
K	0.10	0.25	0.0040	0.0098
L	2.10	2.50	0.0830	0.0984
M	0.45	0.60	0.0180	0.0236
N	0.89	1.02	0.0350	0.0401
K	0.013	0.10	0.0005	0.0040

*Low Profile = CASE 318-03 TO-236AB

5

TYPICAL CHARACTERISTICS
(T_A = 25°C unless noted)

FIGURE 1 – REVERSE LEAKAGE

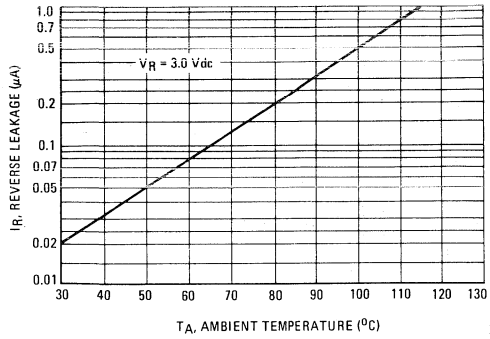


FIGURE 2 – FORWARD VOLTAGE

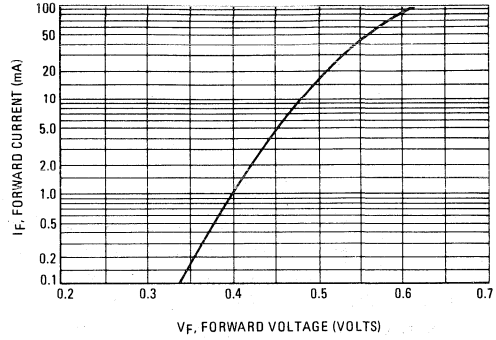


FIGURE 3 – CAPACITANCE

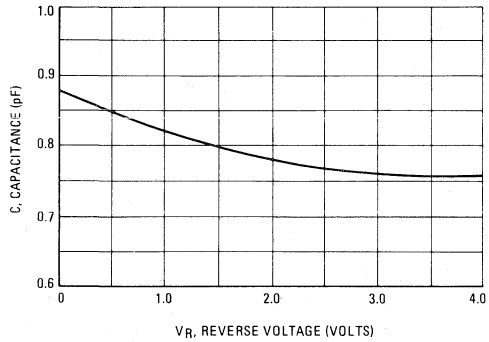
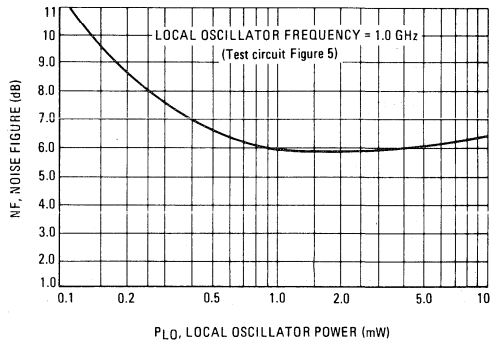
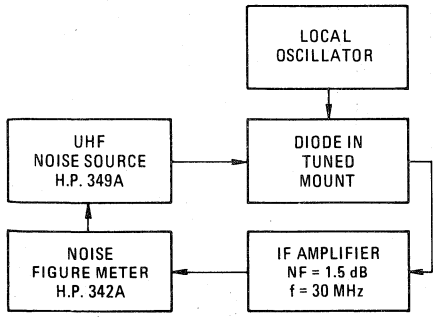


FIGURE 4 – NOISE FIGURE



5

FIGURE 5 – NOISE FIGURE TEST CIRCUIT



NOTES ON TESTING AND SPECIFICATIONS

Note 1 – C_C and C_T are measured using a capacitance bridge (Boonton Electronics Model 75A or equivalent).

Note 2 – Noise figure measured with diode under test in tuned diode mount using UHF noise source and local oscillator (LO) frequency of 1.0 GHz. The LO power is adjusted for 1.0 mW. IF amplifier NF = 1.5 dB, f = 30 MHz, see Figure 5.

Note 3 – L_S is measured on a package having a short instead of a die, using an impedance bridge (Boonton Radio Model 250A RX Meter).

MBD201 MMBD201, L
MBD301 MMBD301, L



SILICON HOT-CARRIER DIODE (SCHOTTKY BARRIER DIODE)

. . . designed primarily for high-efficiency UHF and VHF detector applications. Readily adaptable to many other fast switching RF and digital applications. Supplied in an inexpensive plastic package for low-cost, high-volume consumer and industrial/commercial requirements. Also available in Surface Mount package.

- The Schottky Barrier Construction Provides Ultra-Stable Characteristics By Eliminating the "Cat-Whisker" or "S-Bend" Contact
- Extremely Low Minority Carrier Lifetime — 15 ps (Typ)
- Very Low Capacitance — 1.5pF (Max) @ V_R = 15 V
- Two Voltage Ranges — 20 V — MBD201,MMBD201,L
  — 30 V — MBD301,MMBD301,L
- Low Reverse Leakage — I_R = 10 nAdc (Typ) MBD201, MMBD201,L
  = 13 nAdc (Typ) MBD301, MMBD301,L

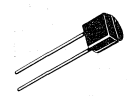
MAXIMUM RATING (T_J = 125°C unless otherwise noted)

		MBD201 MBD301	MMBD201,L MMBD301,L	
Rating	**Symbol**	**Value**		**Unit**
Reverse Voltage MBD201 MBD301	V_R	20 30		Volts
Forward Power Dissipation @ T_A = 25°C Derate above 25°C	P_F	280 2.8	200 2.0	mW mW/°C
Operating Junction Temperature Range	T_J	−55 to +125		°C
Storage Temperature Range	T_{stg}	−65 to +150		°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc) MBD201, MMBD201, L MBD301, MMBD301, L	$V_{(BR)R}$	 20 30	 — —	 — —	Volts
Total Capacitance, Figure 1 (V_R = 15 Volts, f = 1.0 MHz)	C_T	—	0.9	1.5	pF
Minority Carrier Lifetime, Figure 2 (I_F = 5.0 mA, Krakauer Method)	τ	—	15	—	ps
Reverse Leakage, Figure 3 (V_R = 15 V) MBD201, MMBD201, L (V_R = 25 V) MBD301, MMBD301, L	I_R	 — —	 10 13	 200 200	nAdc
Forward Voltage, Figure 4 (I_F = 10 mAdc)	V_F	—	0.5	0.6	Vdc

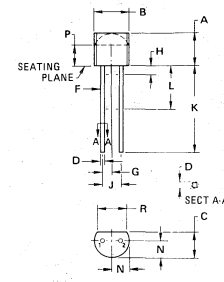
SILICON HOT-CARRIER DETECTOR AND SWITCHING DIODES
20-30 VOLTS



CASE 182-02
TO-226AC



CASE 318-02
TO-236AA
SOT-23

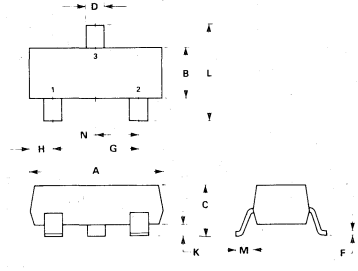


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.356	0.533	0.014	0.021
F	0.407	0.482	0.016	0.019
G	1.27 BSC		0.050 BSC	
H	—	1.27	—	0.050
J	2.54 BSC		0.100 BSC	
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.03	2.66	0.080	0.105
P	2.93	—	0.115	—
R	3.43	—	0.135	—

STYLE 1:
PIN 1. ANODE
2. CATHODE

CASE 182-02
TO-226AC

All JEDEC dimensions and notes apply



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.85	1.20	0.033	0.0472
D	0.37	0.50	0.0150	0.020
F	0.085	0.130	0.0034	0.0051
G	1.78	2.04	0.0701	0.0807
H	0.45	0.60	0.0177	0.0236
K	0.10	0.25	0.0040	0.0098
L	2.10	2.50	0.0830	0.0984
M	0.45	0.60	0.0180	0.0236
N	0.89	1.02	0.0350	0.0401
K	0.013	0.10	0.0005	0.0040

*Low Profile = CASE 318-03

TO-236AB

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

CASE 318-02
TO-236AA
SOT-23

5

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 – TOTAL CAPACITANCE

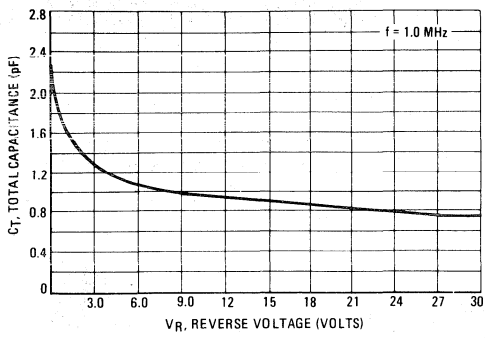


FIGURE 2 – MINORITY CARRIER LIFETIME

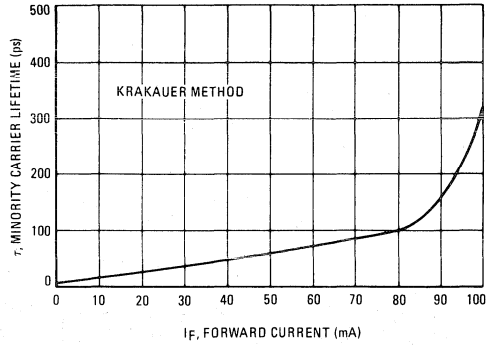


FIGURE 3 – REVERSE LEAKAGE

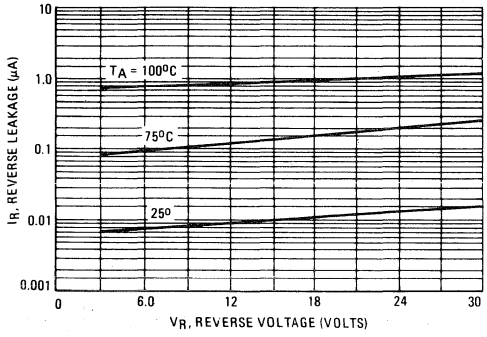
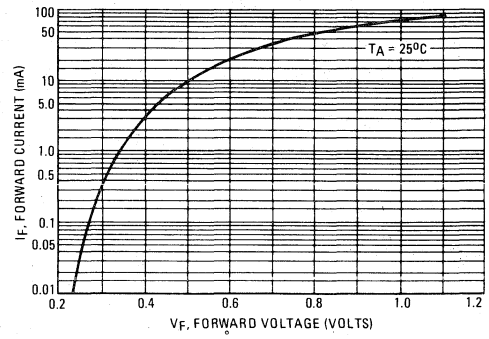
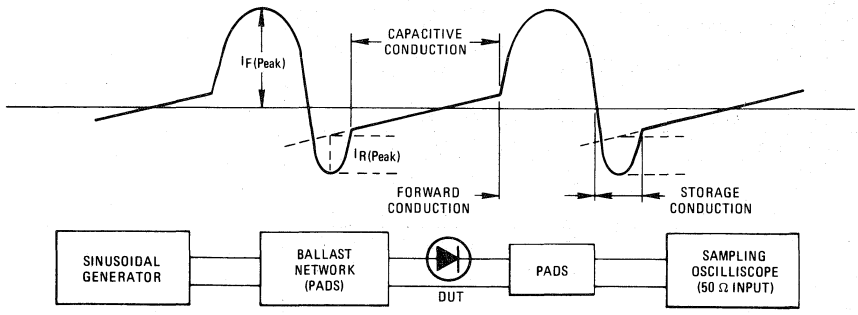


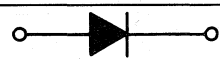
FIGURE 4 – FORWARD VOLTAGE



KRAKAUER METHOD OF MEASURING LIFE TIME



MBD501 MMBD501, L
MBD701 MMBD701, L

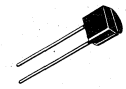


SILICON HOT-CARRIER DIODE (SCHOTTKY BARRIER DIODE)

. . . designed primarily for high-efficiency UHF and VHF detector applications. Readily adaptable to many other fast switching RF and digital applications. Supplied in an inexpensive plastic package for low-cost, high-volume consumer and industrial/commercial requirements. Also available in Surface Mount package.

- The Schottky Barrier Construction Provides Ultra-Stable Characteristics by Eliminating the "Cat-Whisker" or "S-Bend" Contact
- Extremely Low Minority Carrier Lifetime — 15 ps (Typ)
- Very Low Capacitance — 1.0 pF @ V_R = 20 V
- High Reverse Voltage — to 70 Volts
- Low Reverse Leakage — 200 nA (Max)

HIGH-VOLTAGE SILICON HOT-CARRIER DETECTOR AND SWITCHING DIODES
50-70 VOLTS



CASE 182-02
TO-226AC



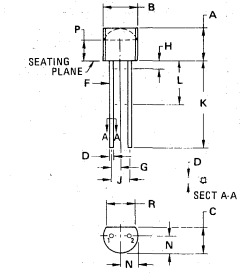
CASE 318-02
TO-236AA
SOT-23

MAXIMUM RATING (T_J = 125°C unless otherwise noted)

		MBD501 MBD701	MMBD501,L MMBD701,L	
Rating	**Symbol**	**Value**		**Unit**
Reverse Voltage MBD501 MBD701	V_R	50 70		Volts
Forward Power Dissipation @ T_A = 25°C Derate above 25°C	P_F	280 2.8	200 2.0	mW mW/°C
Operating Junction Temperature Range	T_J	−55 to +125		°C
Storage Temperature Range	T_{stg}	−65 to +150		°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc) MBD501, MMBD501, L MBD701, MMBD701, L	$V_{(BR)R}$	50 70	— —	— —	Volts
Total Capacitance, Figure 1 (V_R = 20 Volts, f = 1.0 MHz)	C_T	—	0.5	1.0	pF
Minority Carrier Lifetime, Figure 2 (I_F = 5.0 mA, Krakauer Method)	τ	—	15	—	ps
Reverse Leakage, Figure 3 (V_R = 25 V) MBD501, MMBD501, L (V_R = 35 V) MBD701, MMBD701, L	I_R	— —	7.0 9.0	200 200	nAdc
Forward Voltage, Figure 4 (I_F = 10 mAdc)	V_F	—	1.0	1.2	Vdc

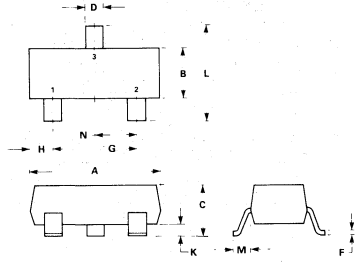


STYLE 1:
PIN 1. ANODE
2. CATHODE

CASE 182-02
TO-226AC

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.356	0.533	0.014	0.021
F	0.407	0.482	0.016	0.019
G	1.27 BSC		0.050 BSC	
H	–	1.27	–	0.050
J	2.54 BSC		0.100 BSC	
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.66	0.080	0.105
P	2.93	–	0.115	–
R	3.43	–	0.135	–

All JEDEC dimensions and notes apply



STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

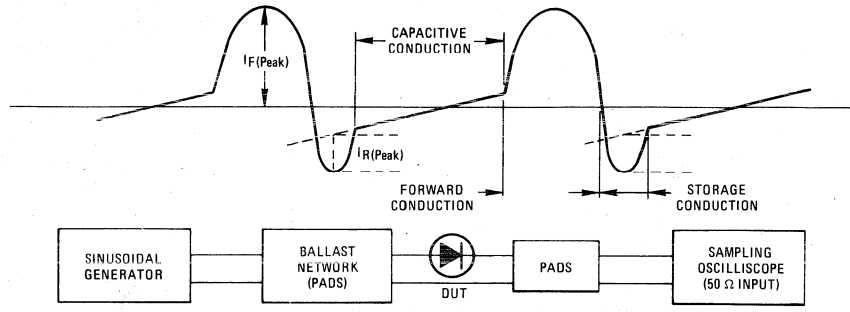
CASE 318-02
TO-236AA
SOT-23

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.85	1.20	0.033	0.0472
D	0.37	0.50	0.0150	0.020
F	0.085	0.130	0.0034	0.0051
G	1.78	2.04	0.0701	0.0807
H	0.45	0.60	0.0177	0.0236
K	0.10	0.25	0.0040	0.0098
L	2.10	2.50	0.0830	0.0984
M	0.45	0.60	0.0180	0.0236
N	0.89	1.02	0.0350	0.0401
K	0.013	0.10	0.0005	0.0040

*Low Profile = CASE 318-03 TO-236AB

5

KRAKAUER METHOD OF MEASURING LIFE TIME



TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 – TOTAL CAPACITANCE

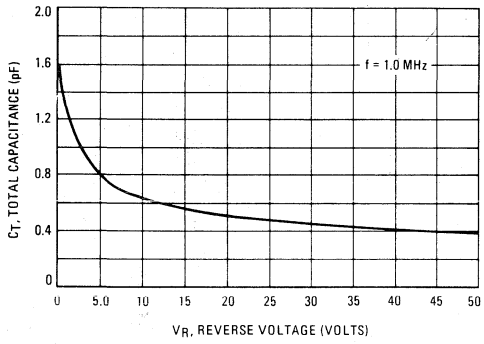


FIGURE 2 – MINORITY CARRIER LIFETIME

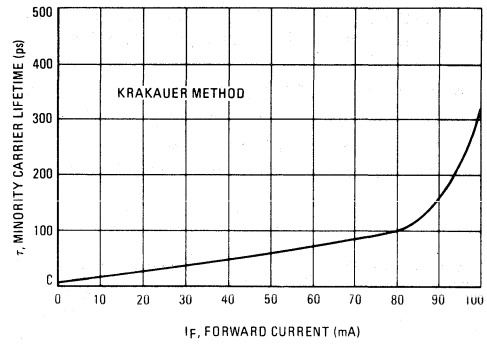


FIGURE 3 – REVERSE LEAKAGE

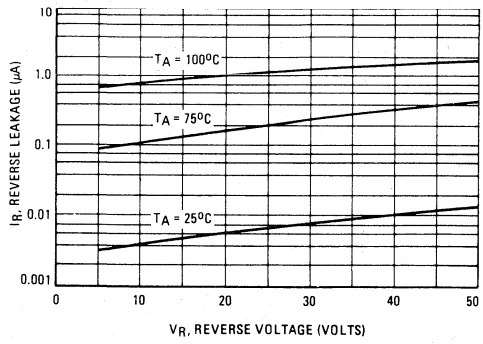
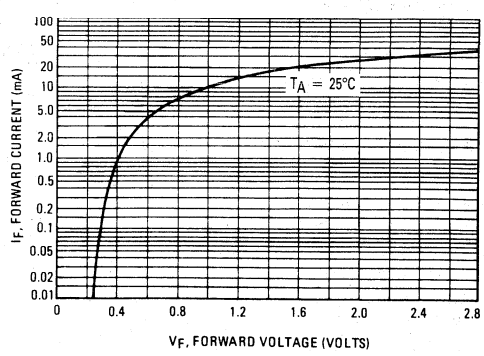


FIGURE 4 – FORWARD VOLTAGE



5

MMBV105G
MMBV105GL
MV105G

VVC

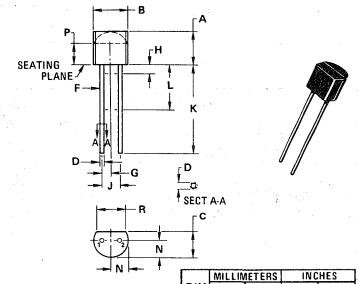
SILICON EPICAP DIODES

. . . designed in the Surface Mount package for general frequency control and tuning applications; providing solid-state reliability in replacement of mechanical tuning methods.

- Controlled and Uniform Tuning Ratio

VOLTAGE VARIABLE CAPACITANCE DIODES

30 VOLTS

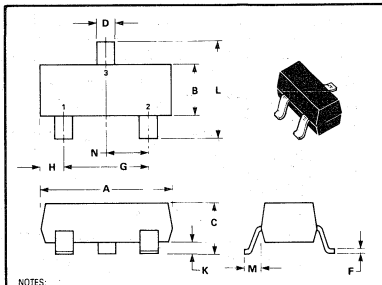


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.356	0.533	0.014	0.021
F	0.407	0.482	0.016	0.019
G	1.27 BSC		0.050 BSC	
H	–	1.27	–	0.050
J	2.54 BSC		0.100 BSC	
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.66	0.080	0.105
P	2.93	–	0.115	–
R	3.43	–	0.135	–

All JEDEC dimensions and notes apply

STYLE 1:
PIN 1. ANODE
2. CATHODE

CASE 182-02
TO-226AC



NOTES:
1. DIMENSIONING AND TOLERANCING PER Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.85	1.20	0.033	0.0472
D	0.37	0.50	0.0150	0.020
F	0.085	0.130	0.0034	0.0051
G	1.78	2.04	0.0701	0.0807
H	0.45	0.60	0.0177	0.0236
K	0.10	0.25	0.0040	0.0098
L	2.10	2.50	0.0830	0.0984
M	0.45	0.60	0.0180	0.0236
N	0.89	1.02	0.0350	0.0401
* K	0.013	0.10	0.0005	0.0040

*Low Profile = CASE 318-03 TO-236AB

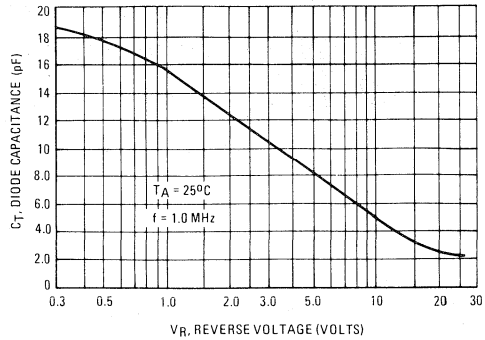
STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

CASE 318-02
TO-236AA

MAXIMUM RATINGS

Rating	Symbol	MV105G	MMBV105G,L	Unit
Reverse Voltage	V_R	30		Volts
Forward Current	I_F	200		mA
Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	280 2.8	200 2.0	mW mW/°C
Junction Temperature	T_J	+125		°C
Storage Temperature Range	T_{stg}	−65 to +150		°C

FIGURE 1 – DIODE CAPACITANCE



5

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic-All Types	Symbol	Min	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	$V_{(BR)R}$	30	–	Vdc
Reverse Voltage Leakage Current (VR = 28 V)	I_R	–	50.0	nAdc

Device Type	C_T V_R = 25 Vdc pF		Q f = 100 MHz V_R = 3.0V	C_3/C_{25}	
	Min	Max	Typ	Min	Max
MMBV105G	1.8	2.8	150	4.0	6

FIGURE 2 – FIGURE OF MERIT

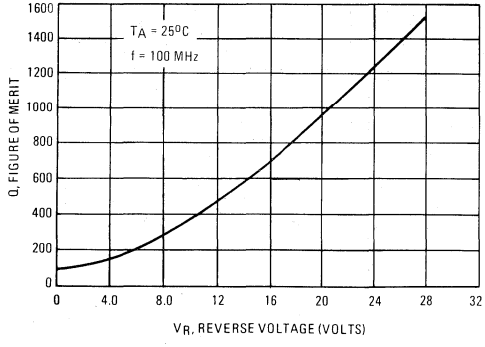
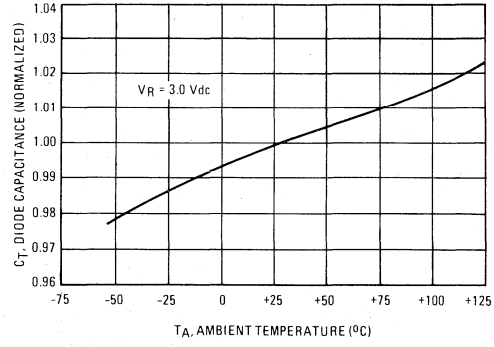


FIGURE 3 – DIODE CAPACITANCE



5

MMBV109
MMBV109L
MV209

VOLTAGE VARIABLE
CAPACITANCE DIODE

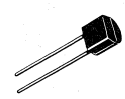
26–32 pF

VVC

SILICON EPICAP DIODE

. . . designed for general frequency control and tuning applications; providing solid-state reliability in replacement of mechanical tuning methods.

- High Q with Guaranteed Minimum Values at VHF Frequencies
- Controlled and Uniform Tuning Ratio
- Available in Surface Mount Package



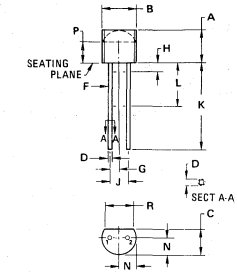
CASE 182-02
TO-226AC



CASE 318-02
TO-236AA
SOT-23

MAXIMUM RATINGS

Rating	Symbol	MV209 Value	MMBV209,L Value	Unit
Reverse Voltage	V_R	30		Volts
Forward Current	I_F	200		mA
Forward Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	280 2.8	200 2.0	mW mW/°C
Junction Temperature	T_J	+125		°C
Storage Temperature Range	T_{stg}	−65 to +150		°C

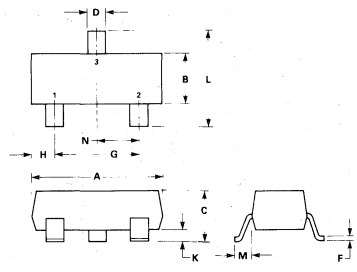


DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.356	0.533	0.014	0.021
F	0.407	0.482	0.016	0.019
G	1.27 BSC		0.050 BSC	
H	–	1.27	–	0.050
J	2.54 BSC		0.100 BSC	
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.66	0.080	0.105
P	2.93	–	0.115	–
R	3.43	–	0.135	–

All JEDEC dimensions and notes apply

STYLE 1:
PIN 1. ANODE
2. CATHODE

CASE 182-02
TO-226AC



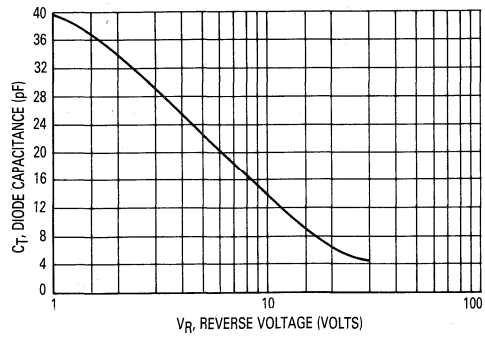
DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.85	1.20	0.033	0.0472
D	0.37	0.50	0.0150	0.020
F	0.085	0.130	0.0034	0.0051
G	1.78	2.04	0.0701	0.0807
H	0.45	0.60	0.0177	0.0236
K	0.10	0.25	0.0040	0.0098
L	2.10	2.50	0.0830	0.0984
M	0.45	0.60	0.0180	0.0236
N	0.89	1.02	0.0350	0.0401
* K	0.013	0.10	0.0005	0.0040

*Low Profile = CASE 318-03 TO-236AB

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

CASE 318-02
TO-236AA
SOT-23

FIGURE 1 — DIODE CAPACITANCE



5

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic – All Types	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	$V_{(BR)R}$	30	–	–	Vdc
Reverse Voltage Leakage Current (V_R = 25 Vdc)	I_R	–	–	0.1	μAdc
Diode Capacitance Temperature Coefficient (V_R = 3.0 Vdc, f = 1.0 MHz)	TC_C	–	300	—	ppm/°C

	C_t, Diode Capacitance V_R = 3.0 Vdc, f = 1.0 MHz pF			Q, Figure of Merit V_R = 3.0 Vdc f = 50 MHz (Note 1)	C_R, Capacitance Ratio C_3/C_{25} f = 1.0 MHz (Note 2)	
Device	Min	Nom	Max	Min	Min	Max
MMBV109,L/MV209	26	29	32	200	5.0	6.5

FIGURE 2 – FIGURE OF MERIT

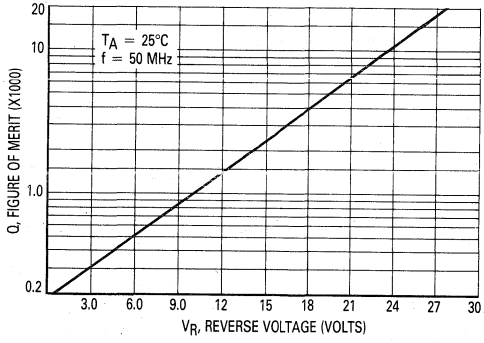


FIGURE 3 – LEAKAGE CURRENT

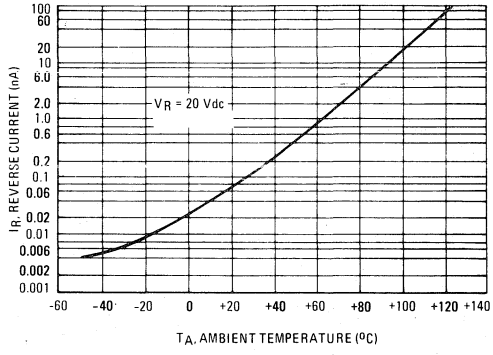
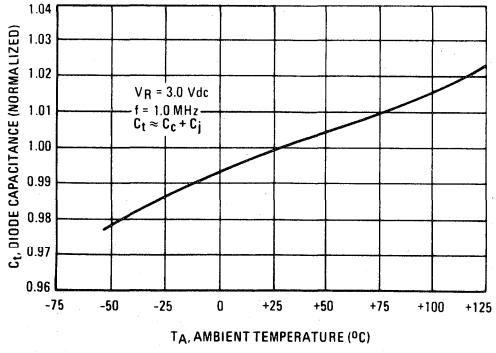


FIGURE 4 – DIODE CAPACITANCE



NOTES ON TESTING AND SPECIFICATIONS

1. Q is calculated by taking the G and C readings of an admittance bridge, such as Boonton Electronics Model 33AS8, at the specified frequency and substituting in the following equation:

$$Q = \frac{2\pi fC}{G}$$

2. C_R is the ratio of C_t measured at 3.0 Vdc divided by C_t measured at 25 Vdc.

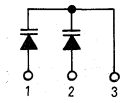
Silicon Epicap Diodes

MMBV432L

DUAL VOLTAGE-VARIABLE CAPACITANCE DIODE

. . . designed for FM tuning, general frequency control and tuning, or any top-of-the-line application requiring back-to-back diode configuration for minimum signal distortion and detuning. This device is supplied in the SOT-23 plastic package for high volume, pick and place assembly requirements.

- High Figure of Merit — Q = 100 (Typ) @ V_R = 2 Vdc, f = 100 MHz
- Guaranteed Capacitance Range
- Dual Diodes — Save Space and Reduce Cost
- Surface Mount Package
- Available in 8 mm Tape and Reel
- Monolithic Chip Provides Improved Matching — Guaranteed ±1% (Max) Over Specified Tuning Range





CASE 318-03
(TO-236AB)
Low-Profile

MAXIMUM RATINGS (Each Diode)

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	14	Volts
Forward Current	I_F	200	mA
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	−65 to +125	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	$V_{(BR)R}$	14	—	—	Vdc
Reverse Voltage Leakage Current (V_R = 30 Vdc)	I_R	—	—	100	nAdc
Diode Capacitance (V_R = 2 Vdc, f = 1 MHz)	C_T	43	—	48.1	pF
Capacitance Ratio C3/C8 (f = 1 MHz)	C_R	1.5	—	2	—
Figure of Merit* (V_R = 2 Vdc, f = 100 MHz)	Q	75	100	—	—

* $Q = \frac{1}{2\pi f C_T R_S}$

5

TYPICAL CHARACTERISTICS (Each Diode)

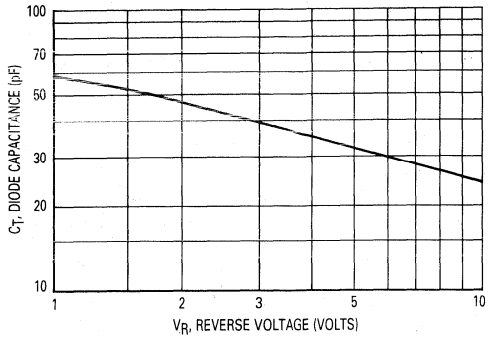


Figure 1. Diode Capacitance (Each Diode)

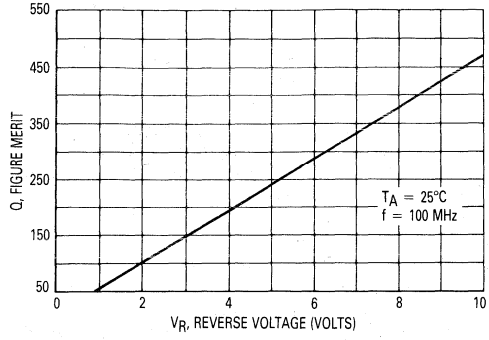


Figure 2. Figure of Merit versus Voltage

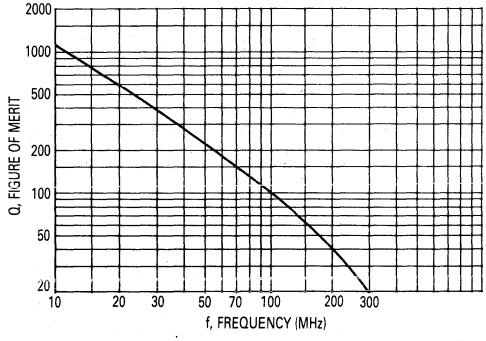


Figure 3. Figure of Merit versus Frequency

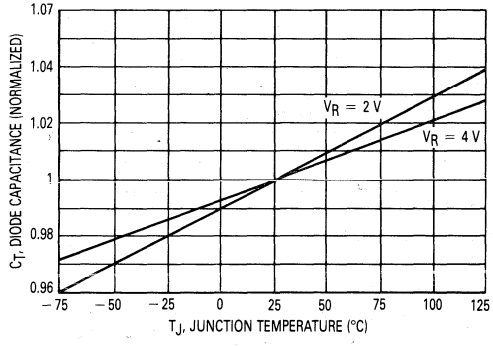


Figure 4. Diode Capacitance versus Temperature

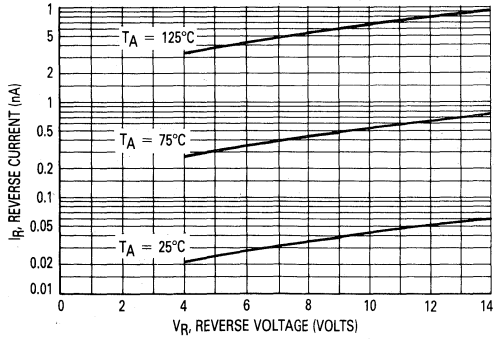
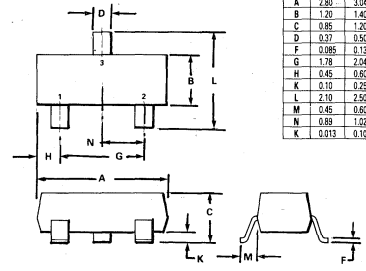


Figure 5. Reverse Current versus Reverse Voltage

OUTLINE DIMENSIONS

CASE 318-03
(TO-236AB)
Low-Profile



NOTES:
1. DIMENSIONING AND TOLERANCING PER Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.85	1.20	0.033	0.0472
D	0.37	0.50	0.0150	0.020
F	0.085	0.130	0.0034	0.0051
G	1.78	2.04	0.0701	0.0807
H	0.45	0.60	0.0177	0.0236
K	0.10	0.25	0.0040	0.0098
L	2.10	2.50	0.0830	0.0984
M	0.45	0.60	0.0180	0.0236
N	0.89	1.02	0.0350	0.0401
K	0.013	0.10	0.0005	0.0040

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

5

MMBV2101, L thru MMBV2109, L
MV2101 thru MV2115

VVC

VOLTAGE-VARIABLE CAPACITANCE DIODES

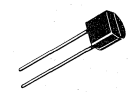
6.8–100 pF
30 VOLTS

SILICON EPICAP DIODES

. . . designed in the popular PLASTIC PACKAGE for high volume requirements of FM Radio and TV tuning and AFC, general frequency control and tuning applications; providing solid-state reliability in replacement of mechanical tuning methods.

Also available in Surface Mount package up to 33 pF.

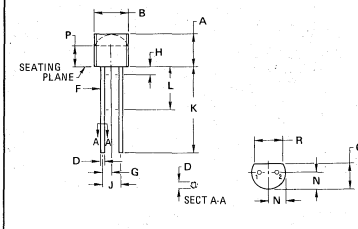
- High Q with Guaranteed Minimum Values
- Controlled and Uniform Tuning Ratio
- Standard Capacitance Tolerance — 10%
- Complete Typical Design Curves



CASE 182-02



CASE 318-02
TO-236AA
SOT-23

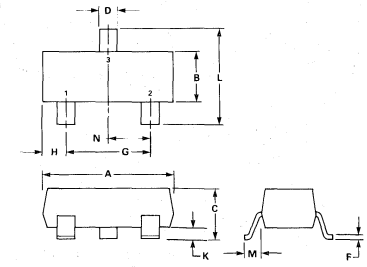


STYLE 1:
PIN 1. ANODE
2. CATHODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.356	0.533	0.014	0.021
F	0.407	0.482	0.016	0.019
G	1.27 BSC		0.050 BSC	
H	–	1.27	–	0.050
J	2.54 BSC		0.100 BSC	
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.66	0.080	0.105
P	2.93	–	0.115	–
R	3.43	–	0.135	–

CASE 182-02

All JEDEC dimensions and notes apply



STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

CASE 318-02
TO-236AA
SOT-23

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.85	1.20	0.033	0.0472
D	0.37	0.50	0.0150	0.020
F	0.085	0.130	0.0034	0.0051
G	1.78	2.04	0.0701	0.0807
H	0.45	0.60	0.0177	0.0236
K	0.10	0.25	0.0040	0.0098
L	2.10	2.50	0.0830	0.0984
M	0.45	0.60	0.0180	0.0236
N	0.89	1.02	0.0350	0.0401
K	0.013	0.10	0.0005	0.0040

*Low Profile = CASE 318-03 TO-236AB

MAXIMUM RATINGS

Rating	Symbol	MV2101 thru MV2115	MMBV2101,L thru MMBV2109,L	Unit
Reverse Voltage	V_R	30		Volts
Forward Current	I_F	200		mA
Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	280 2.8	200 2.0	mW mW/°C
Junction Temperature	T_J	+125		°C
Storage Temperature Range	T_{stg}	−65 to +150		°C

5

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic—All Types	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	$V_{(BR)R}$	30	–	–	Vdc
Reverse Voltage Leakage Current (V_R = 25 Vdc, T_A = 25°C)	I_R	–	–	0.10	μAdc
Diode Capacitance Temperature Coefficient (V_R = 4.0 Vdc, f = 1.0 MHz)	TC_C	–	280	—	ppm/°C

	C_T, Diode Capacitance V_R = 4.0 Vdc, f = 1.0 MHz pF			Q, Figure of Merit V_R = 4.0 Vdc, f = 50 MHz	TR, Tuning Ratio C_2/C_{30} f = 1.0 MHz		
Device	Min	Nom	Max	Typ	Min	Typ	Max
MMBV2101, L/MV2101	6.1	6.8	7.5	450	2.5	2.7	3.2
MMBV2102, L/MV2102	7.4	8.2	9.0	450	2.5	2.8	3.2
MMBV2103, L/MV2103	9.0	10.0	11.0	400	2.5	2.9	3.2
MMBV2104, L/MV2104	10.8	12.0	13.2	400	2.5	2.9	3.2
MMBV2105, L/MV2105	13.5	15.0	16.5	400	2.5	2.9	3.2
MMBV2106, L/MV2106	16.2	18.0	19.8	350	2.5	2.9	3.2
MMBV2107, L/MV2107	19.8	22.0	24.2	350	2.5	2.9	3.2
MMBV2108, L/MV2108	24.3	27.0	29.7	300	2.5	3.0	3.2
MMBV2109, L/MV2109	29.7	33.0	36.3	200	2.5	3.0	3.2
MV2110	35.1	39.0	42.9	150	2.5	3.0	3.2
MV2111	42.3	47.0	51.7	150	2.5	3.0	3.2
MV2112	50.4	56.0	61.6	150	2.6	3.0	3.3
MV2113	61.2	68.0	74.8	150	2.6	3.0	3.3
MV2114	73.8	82.0	90.2	100	2.6	3.0	3.3
MV2115	90.0	100.0	110.0	100	2.6	3.0	3.3

PARAMETER TEST METHODS

5

1. C_T, DIODE CAPACITANCE

($C_T = C_C + C_J$). C_T is measured at 1.0 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).

2. TR, TUNING RATIO

TR is the ratio of C_T measured at 2.0 Vdc divided by C_T measured at 30 Vdc.

3. Q, FIGURE OF MERIT

Q is calculated by taking the G and C readings of an admittance bridge at the specified frequency and substituting in the following equations:

$$Q = \frac{2\pi fC}{G}$$

(Boonton Electronics Model 33AS8). Use Lead Length ≈1/16".

4. TC_C, DIODE CAPACITANCE TEMPERATURE COEFFICIENT

TC_C is guaranteed by comparing C_T at V_R = 4.0 Vdc, f = 1.0 MHz, T_A = -65°C with C_T at V_R = 4.0 Vdc, f = 1.0 MHz, T_A = +85°C in the following equation which defines TC_C:

$$TC_C = \frac{C_T(+85^\circ C) - C_T(-65^\circ C)}{85 + 65} \cdot \frac{10^6}{C_R(25^\circ C)}$$

Accuracy limited by measurement of C_T to ± 0.1 pF.

TYPICAL DEVICE PERFORMANCE

FIGURE 1 – DIODE CAPACITANCE versus REVERSE VOLTAGE

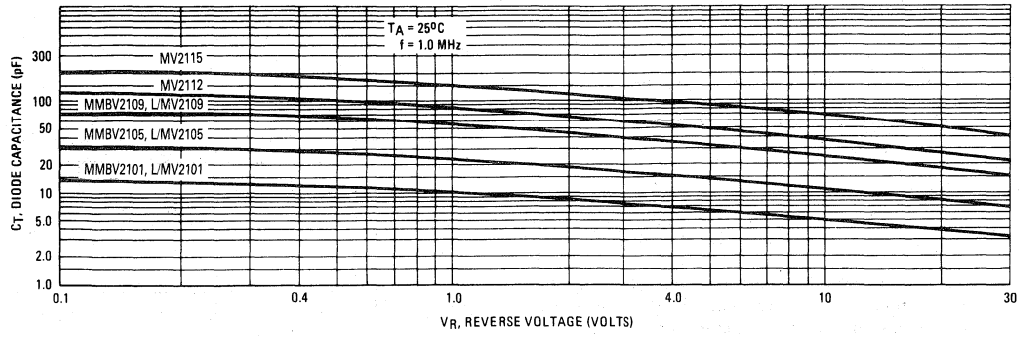


FIGURE 2 – NORMALIZED DIODE CAPACITANCE versus JUNCTION TEMPERATURE

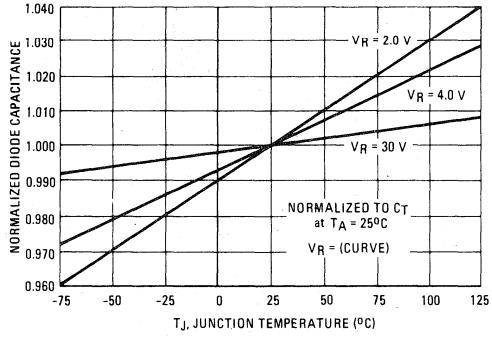


FIGURE 3 – REVERSE CURRENT versus REVERSE BIAS VOLTAGE

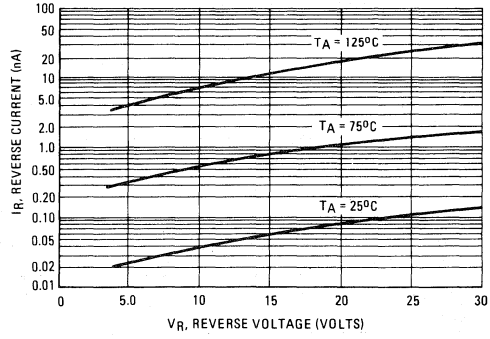


FIGURE 4 – FIGURE OF MERIT versus REVERSE VOLTAGE

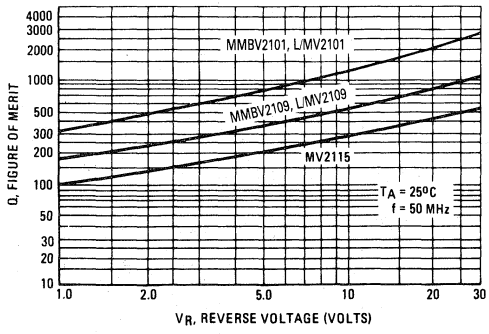
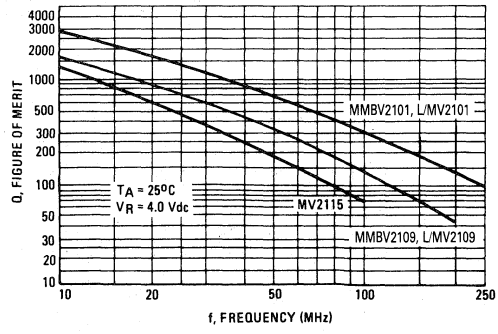


FIGURE 5 – FIGURE OF MERIT versus FREQUENCY



5

MMBV3102
MMBV3102L

VVC

SILICON EPICAP DIODES

. . . designed in the Surface Mount package for general frequency control and tuning applications; providing solid-state reliability in replacement of mechanical tuning methods.

- High Q with Guaranteed Minimum Values at VHF Frequencies
- Controlled and Uniform Tuning Ratio

VOLTAGE VARIABLE CAPACITANCE DIODES

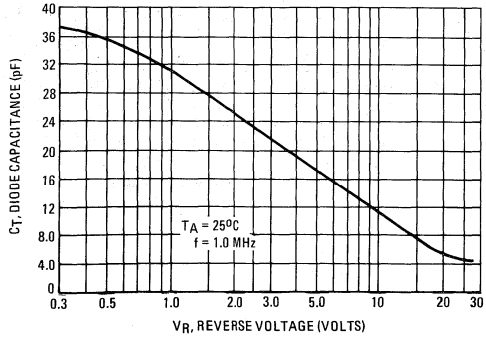
22 pF (Nominal)
30 VOLTS

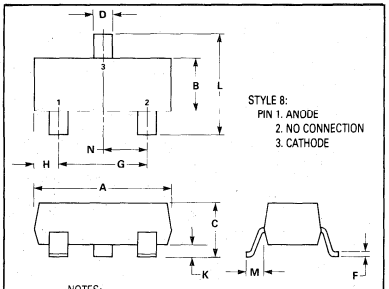


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	30	Volts
Forward Current	I_F	200	mA
Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	200 2.0	mW mW/°C
Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 1 — DIODE CAPACITANCE





NOTES:
1. DIMENSIONING AND TOLERANCING PER Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.85	1.20	0.033	0.0472
D	0.37	0.50	0.0150	0.020
F	0.085	0.130	0.0034	0.0051
G	1.78	2.04	0.0701	0.0807
H	0.45	0.60	0.0177	0.0236
K	0.10	0.25	0.0040	0.0098
L	2.10	2.50	0.0830	0.0984
M	0.45	0.60	0.0180	0.0236
N	0.89	1.02	0.0350	0.0401
* K	0.013	0.10	0.0005	0.0040

*Low Profile = CASE 318-03 TO-236AB

CASE 318-02
TO-236AA

5

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic—All Types	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	$V_{(BR)R}$	30	–	–	Vdc
Reverse Voltage Leakage Current (V_R = 25 Vdc, T_A = 25°C)	I_R	–	–	0.1	μAdc
Diode Capacitance Temperature Coefficient (V_R = 3.0 Vdc, f = 1.0 MHz)	TC_C	–	300	–	ppm/°C

	C_T, Diode Capacitance V_R = 3.0 Vdc, f = 1.0 MHz pF			Q, Figure of Merit V_R = 3.0 Vdc f = 50 MHz	C_R, Capacitance Ratio C_3/C_{25} f = 1.0 MHz	
Device	Min	Nom	Max	Min	Min	Typ
MV3102	20	22	25	200	4.5	4.8

FIGURE 2 – FIGURE OF MERIT

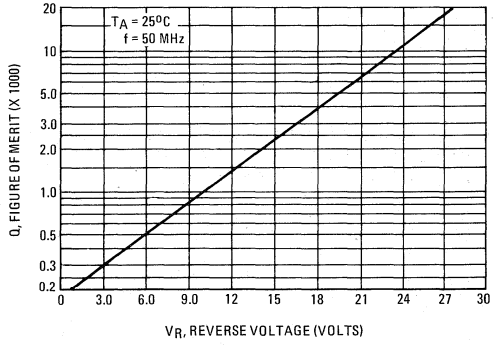


FIGURE 3 – LEAKAGE CURRENT

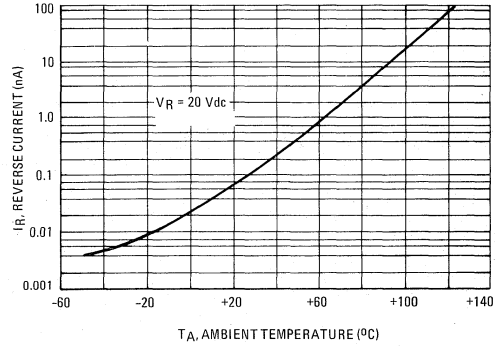
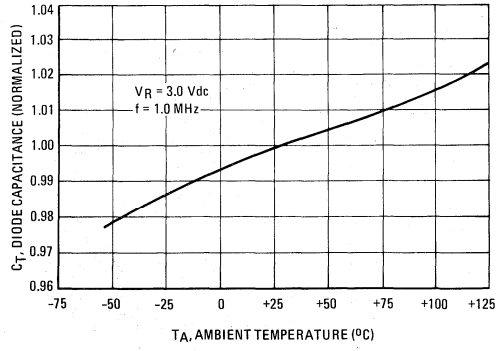


FIGURE 4 – DIODE CAPACITANCE



NOTES ON TESTING AND SPECIFICATIONS

1. L_S is measured on a package having a short instead of a die, using an impedance bridge (Boonton Radio Model 250A RX Meter).
2. C_C is measured on a package without a die, using a capacitance bridge (Boonton Electronics Model 75A or equivalent).
3. Q is calculated by taking the G and C readings of an admittance bridge, such as Boonton Electronics Model 33AS8, at the specified frequency and substituting in the following equation:

$$Q = \frac{2\pi fC}{G}$$

4. C_R is the ratio of C_T measured at 3.0 Vdc divided by C_T measured at 25 Vdc.

5

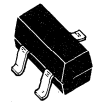
MMBV3401
MMBV3401L

SILICON PIN DIODE

. . . designed primarily for VHF band switching applications but also suitable for use in general-purpose switching and attenuator circuits. Supplied in a Surface Mount package.

- Rugged PIN Structure Coupled with Wirebond Construction for Optimum Reliability
- Low Capacitance — 0.7 pF Typ at V_R = 20 V
- Very Low Series Resistance at 100 MHz — 0.34 Ohms (Typ) @ I_F = 10 mAdc

SILICON PIN SWITCHING DIODE

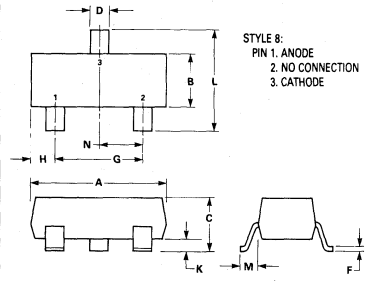


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	20	Volts
Forward Power Dissipation @ T_A = 25°C Derate above 25°C	P_F	200 2.8	mW mW/°C
Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μA)	$V_{(BR)R}$	35	—	—	Volts
Diode Capacitance V_R = 20 V	C_T	—	—	1.0	pF
Series Resistance (Figure 5) (I_F = 10 mA) f = 100 MHz	R_S	—	—	0.7	Ohms
Reverse Leakage Current (V_R = 25 V)	I_R	—	—	0.1	μA



STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

NOTES:
1. DIMENSIONING AND TOLERANCING PER Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.85	1.20	0.033	0.0472
D	0.37	0.50	0.0150	0.020
F	0.085	0.130	0.0034	0.0051
G	1.78	2.04	0.0701	0.0807
H	0.45	0.60	0.0177	0.0236
K	0.10	0.25	0.0040	0.0098
L	2.10	2.50	0.0830	0.0984
M	0.45	0.60	0.0180	0.0236
N	0.89	1.02	0.0350	0.0401
* K	0.013	0.10	0.0005	0.0040

*Low Profile = CASE 318-03 TO-236AB

CASE 318-02
TO-236AA

5

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 – SERIES RESISTANCE

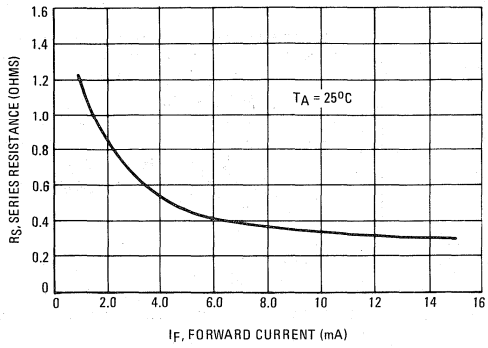


FIGURE 2 – FORWARD VOLTAGE

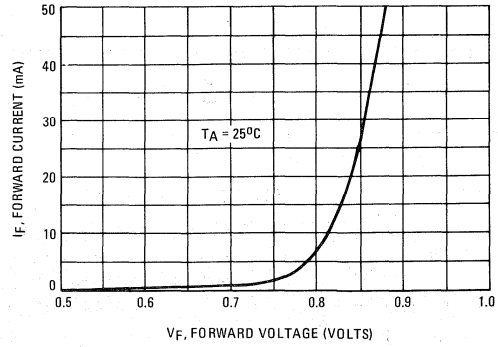


FIGURE 3 – DIODE CAPACITANCE

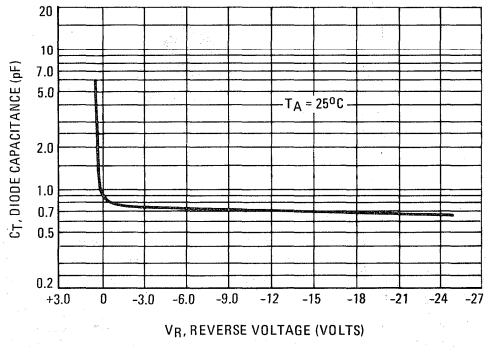


FIGURE 4 – LEAKAGE CURRENT

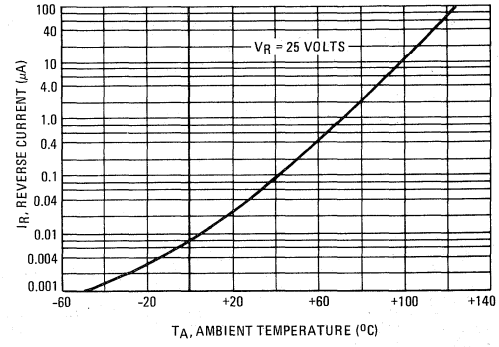
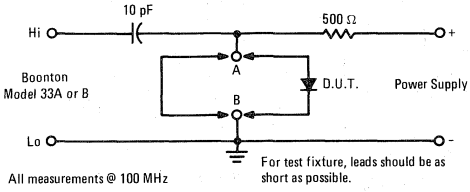


FIGURE 5 – FORWARD SERIES RESISTANCE TEST METHOD



To measure series resistance, a 10 pF capacitor is used to reduce the forward capacitance of the circuit and to prevent shorting of the external power supply through the bridge. The small signal from the bridge is prevented from shorting through the power supply by the 500-ohm resistor. The resistance of the 10 pF capacitor can be considered negligible for this measurement.

1. The RF Admittance Bridge (Boonton 33A or B) must be initially balanced, with the test circuit connected to the bridge test terminals. The conductance scale will be set at zero and the capacitance scale will be set at 120 pF, as required when using the 100 MHz test coil.
2. Use a short length of wire to short the test circuit from point "A" to "B". Then connect the power supply providing 10 mA of bias current to the test circuit.
3. Adjust the capacitance scale arm of the bridge and the "G" zero control for a minimum null on the "null meter". The null occurs at approximately 130 pF.
4. Replace the wire short with the device to be tested. Bias the device to a forward conductance state of 10 mA.
5. Obtain a minimum null on the "null meter", with the capacitance and conductance scale adjustment arms.
6. Read conductance (G) direct from the scale. Now read the capacitance value from the scale (≈ 130 pF) and subtract 120 pF which yields capacitance (C). The forward resistance (R_S) can now be calculated from:

$$R_S = \frac{2.533\,G}{C^2}$$

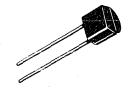
Where:
G – in micromhos,
C – in pF,
R_S – in ohms

5

MMBV3700
MMBV3700L
MPN3700

SILICON PIN
SWITCHING DIODE





CASE 182-02
TO-226AC

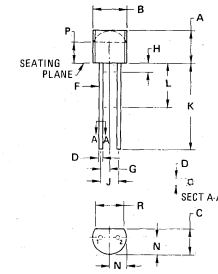


CASE 318-02
TO-236AA
SOT-23

HIGH VOLTAGE SILICON PIN DIODE

. . . designed primarily for VHF band switching applications but also suitable for use in general-purpose switching and attenuator circuits. Supplied in a cost effective plastic package for economical, high-volume consumer and industrial requirements.

- Long Reverse Recovery Time
  t_{rr} = 300 ns (Typ)
- Rugged PIN Structure Coupled with Wirebond Construction for Optimum Reliability
- Low Series Resistance @ 100 MHz —
  R_S = 0.7 Ohms (Typ) @ I_F = 10 mAdc
- Reverse Breakdown Voltage = 200 V (Min)

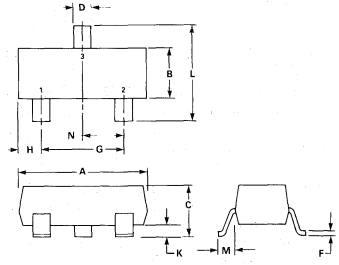


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.356	0.533	0.014	0.021
F	0.407	0.482	0.016	0.019
G	1.27 BSC		0.050 BSC	
H	—	1.27	—	0.050
J	2.54 BSC		0.100 BSC	
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.03	2.66	0.080	0.105
P	2.93	—	0.115	—
R	3.43	—	0.135	—

STYLE 1:
PIN 1. ANODE
2. CATHODE

CASE 182-02
TO-226AC

All JEDEC dimensions and notes apply



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.85	1.20	0.033	0.0472
D	0.37	0.50	0.0150	0.020
F	0.085	0.130	0.0034	0.0051
G	1.78	2.04	0.0701	0.0807
H	0.45	0.60	0.0177	0.0236
K	0.10	0.25	0.0040	0.0098
L	2.10	2.50	0.0830	0.0984
M	0.45	0.60	0.0180	0.0236
N	0.89	1.02	0.0350	0.0401
K	0.013	0.10	0.0005	0.0040

*Low Profile = CASE 318-03 TO-236AB

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

CASE 318-02
TO-236AA
SOT-23

MAXIMUM RATINGS

Rating	Symbol	MPN3700	MMBV3700,L	Unit
Reverse Voltage	V_R	200		Volts
Total Device Dissipation @ T_A = 25°C	P_D	280	200	mW
Derate above 25°C		2.8	2.0	mW/°C
Junction Temperature	T_J	+125		°C
Storage Temperature Range	T_{stg}	−65 to +150		°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μA)	$V_{(BR)R}$	200	—	—	Volts
Diode Capacitance (V_R = 20 Vdc, f = 1.0 MHz)	C_T	—	—	1.0	pF
Series Resistance (Figure 5) (I_F = 10 mA)	R_S	—	0.7	1.0	Ohms
Reverse Leakage Current (V_R = 150 Vdc)	I_R	—	—	0.1	μA
Reverse Recovery Time (I_F = I_R = 10 mA)	t_{rr}	—	300	—	ns

5

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — SERIES RESISTANCE

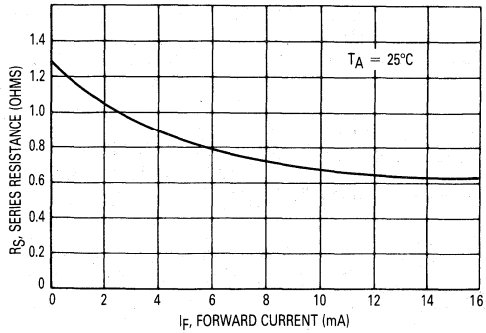


FIGURE 2 — FORWARD VOLTAGE

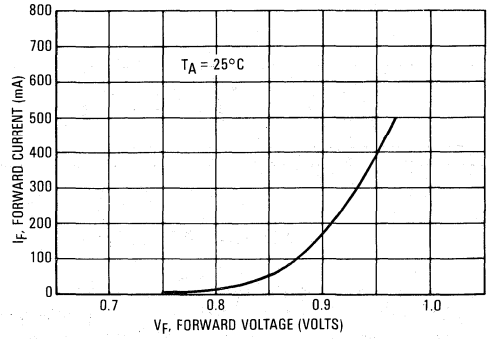


FIGURE 3 — DIODE CAPACITANCE

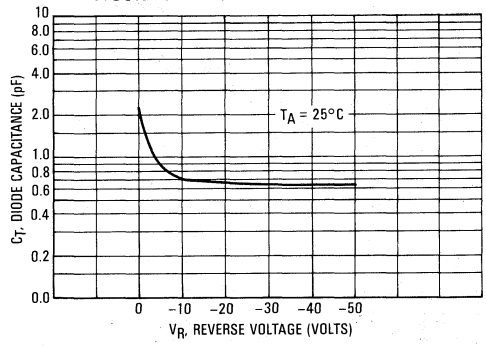


FIGURE 4 — LEAKAGE CURRENT

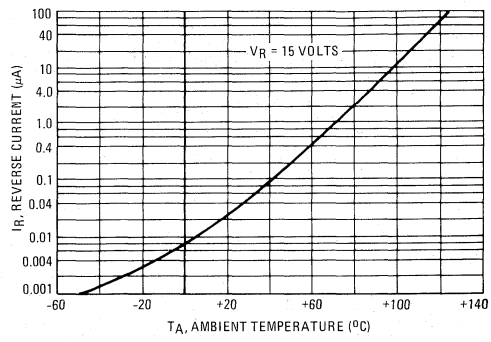
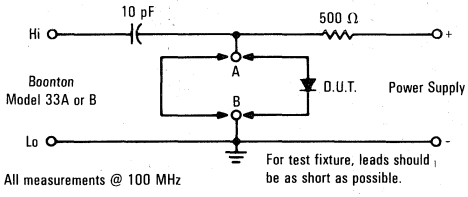


FIGURE 5 — FORWARD SERIES RESISTANCE TEST METHOD



To measure series resistance, a 10 pF capacitor is used to reduce the forward capacitance of the circuit and to prevent shorting of the external power supply through the bridge. The small signal from the bridge is prevented from shorting through the power supply by the 500-ohm resistor. The resistance of the 10 pF capacitor can be considered negligible for this measurement.

1. The RF Admittance Bridge (Boonton 33A or B) must be initially balanced, with the test circuit connected to the bridge test terminals. The conductance scale will be set at zero and the capacitance scale will be set at 120 pF, as required when using the 100 MHz test coil.
2. Use a short length of wire to short the test circuit from point "A" to "B". Then connect the power supply providing 10 mA of bias current to the test circuit.
3. Adjust the capacitance scale arm of the bridge and the "G" zero control for a minimum null on the "null meter". The null occurs at approximately 130 pF.
4. Replace the wire short with the device to be tested. Bias the device to a forward conductance state of 10 mA.
5. Obtain a minimum null on the "null meter", with the capacitance and conductance scale adjustment arms.
6. Read conductance (G) direct from the scale. Now read the capacitance value from the scale (≈130 pF) and subtract 120 pF which yields capacitance (C). The forward resistance (R_S) can now be calculated from:

$$R_S = \frac{2.533\ G}{C^2}$$

Where:
G — in micromhos,
C — in pF,
R_S — in ohms

5

MPN3404

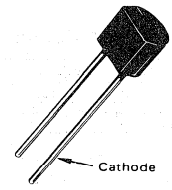


SILICON PIN SWITCHING DIODE

SILICON PIN DIODE

. . . designed primarily for VHF band switching applications but also suitable for use in general-purpose switching and attenuator circuits. Supplied in a cost effective TO-92 type plastic package for economical, high-volume consumer and industrial requirements.

- Rugged PIN Structure Coupled with Wirebond Construction for Optimum Reliability
- Low Series Resistance @ 100 MHz – R_S = 0.7 Ohms (Typ) @ I_F = 10 mAdc
- Sturdy TO-92 Style Package for Handling Ease

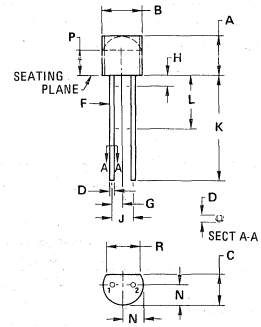


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	20	Volts
Forward Power Dissipation @ T_A = 25°C Derate above 25°C	P_F	400 4.0	mW mW/°C
Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μA)	$V_{(BR)R}$	20	–	–	Volts
Diode Capacitance (V_R = 15 Vdc, f = 1.0 MHz)	C_T	–	1.3	2.0	pF
Series Resistance (Figure 5) (I_F = 10 mA)	R_S	–	0.7	0.85	Ohms
Reverse Leakage Current (V_R = 15 Vdc)	I_R	–	–	0.1	μA



STYLE 1:
PIN 1. ANODE
2. CATHODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.356	0.533	0.014	0.021
F	0.407	0.482	0.016	0.019
G	1.27 BSC		0.050 BSC	
H	–	1.27	–	0.050
J	2.54 BSC		0.100 BSC	
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.66	0.080	0.105
P	2.93	–	0.115	–
R	3.43	–	0.135	–

All JEDEC dimensions and notes apply

CASE 182-02

5

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 – SERIES RESISTANCE

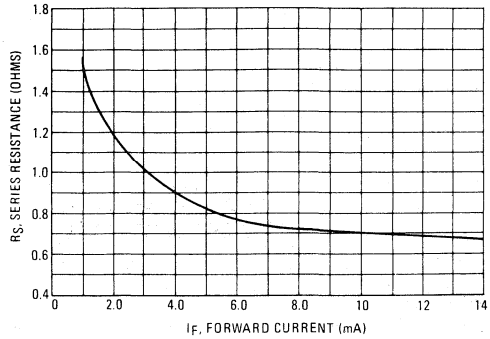


FIGURE 2 – FORWARD VOLTAGE

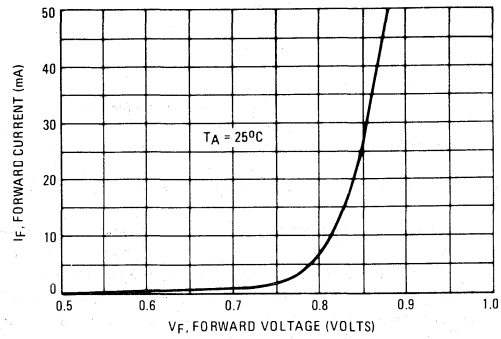


FIGURE 3 – DIODE CAPACITANCE

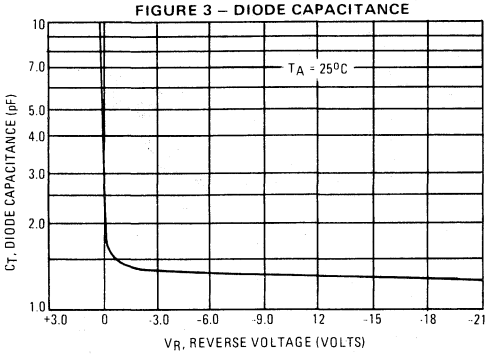


FIGURE 4 – LEAKAGE CURRENT

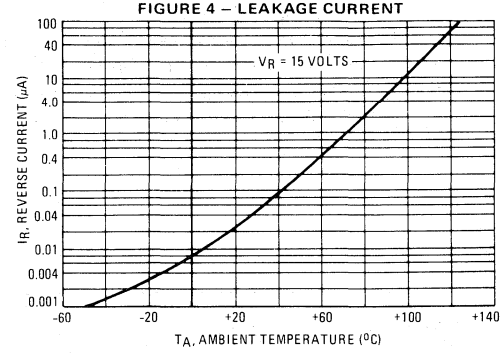
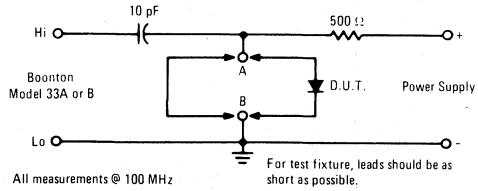


FIGURE 5 – FORWARD SERIES RESISTANCE TEST METHOD



To measure series resistance, a 10 pF capacitor is used to reduce the forward capacitance of the circuit and to prevent shorting of the external power supply through the bridge. The small signal from the bridge is prevented from shorting through the power supply by the 500-ohm resistor. The resistance of the 10 pF capacitor can be considered negligible for this measurement.

1. The RF Admittance Bridge (Boonton 33A or B) must be initially balanced, with the test circuit connected to the bridge test terminals. The conductance scale will be set at zero and the capacitance scale will be set at 120 pF, as required when using the 100 MHz test coil.
2. Use a short length of wire to short the test circuit from point "A" to "B". Then connect the power supply providing 10 mA of bias current to the test circuit.
3. Adjust the capacitance scale arm of the bridge and the "G" zero control for a minimum null on the "null meter". The null occurs at approximately 130 pF.
4. Replace the wire short with the device to be tested. Bias the device to a forward conductance state of 10 mA.
5. Obtain a minimum null on the "null meter", with the capacitance and conductance scale adjustment arms.
6. Read conductance (G) direct from the scale. Now read the capacitance value from the scale (≈ 130 pF) and subtract 120 pF which yields capacitance (C). The forward resistance (R_S) can now be calculated from:

$$R_S = \frac{2.533\,G}{C^2}$$

Where:
G – in micromhos,
C – in pF,
R_S – in ohms

5

MV104

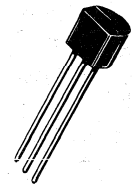
VVC

SILICON EPICAP DIODES

. . . designed for FM tuning, general frequency control and tuning, or any top-of-the-line application requiring back-to-back diode configurations for minimum signal distortion and detuning. This device is supplied in the popular TO-92 plastic package for high volume, economical requirements of consumer and industrial applications.

- High Figure of Merit — Q = 140 (Typ) @ V_R = 3.0 Vdc, f = 100 MHz
- Guaranteed Capacitance Range 37–42 pF @ V_R = 3.0 Vdc (MV104)
- Dual Diodes — Save Space and Reduce Cost
- TO-92 Package for Easy Handling and Mounting
- Monolithic Chip Provides Near Perfect Matching — Guaranteed ±1% (Max) Over Specified Tuning Range.

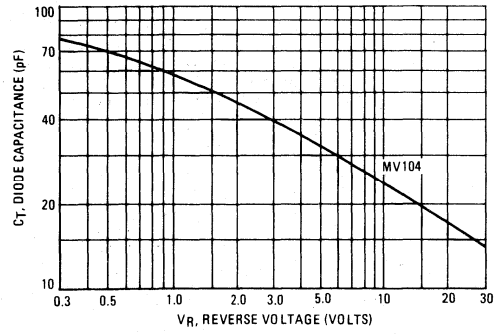
DUAL VOLTAGE-VARIABLE CAPACITANCE DIODES

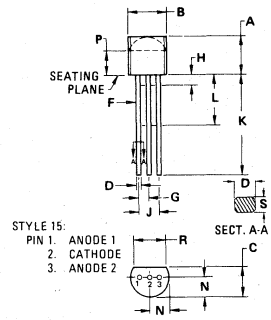


MAXIMUM RATINGS (Each Device)

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	32	Volts
Forward Current	I_F	200	mA
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	280 2.8	mW mW/°C
Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 1 — DIODE CAPACITANCE (Each Device)





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	—	2.64	—	0.100
J	2.41	2.67	0.095	0.105
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.03	2.92	0.080	0.115
P	2.92	—	0.115	—
R	3.43	—	0.135	—
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.

CASE 29-02
TO-226AA

5

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted, Each Device)

Characteristic—All Types	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	$V_{(BR)R}$	32	–	–	Vdc
Reverse Voltage Leakage Current (V_R = 30 Vdc) T_A = 25°C T_A = 60°C	I_R	– –	– –	50 500	nAdc
Diode Capacitance Temperature Coefficient (V_R = 4.0 Vdc, f = 1.0 MHz)	TC_C	–	280	—	ppm/°C

	C_T, Diode Capacitance V_R = 3.0 Vdc, f = 1.0 MHz pF		Q, Figure of Merit V_R = 3.0 Vdc f = 100 MHz		C_R, Capacitance Ratio C_3/C_{30} f = 1.0 MHz	
Device	Min	Max	Min	Typ	Min	Max
MV104	37	42	100	140	2.5	2.8

TYPICAL CHARACTERISTICS (Each Device)

FIGURE 2 – FIGURE OF MERIT versus VOLTAGE

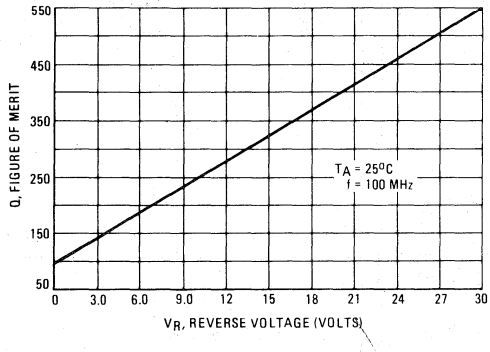


FIGURE 3 – FIGURE OF MERIT versus FREQUENCY

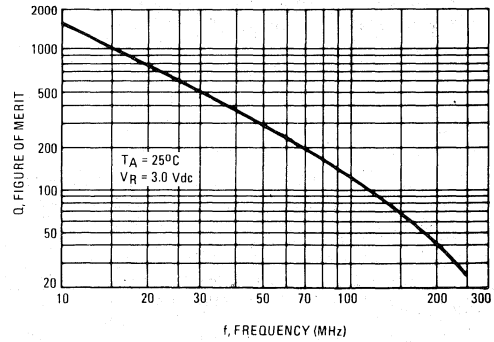


FIGURE 4 – DIODE CAPACITANCE versus TEMPERATURE

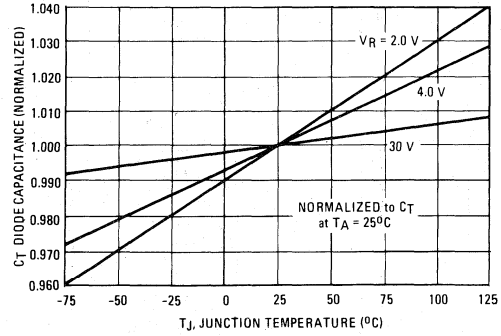
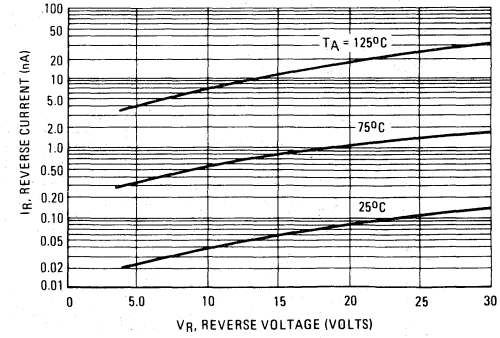


FIGURE 5 – REVERSE CURRENT versus REVERSE VOLTAGE



5

MV1401, H
MV1403, H
MV1404, H
MV1405, H

Tuning Diodes

SILICON HYPER-ABRUPT TUNING DIODES

. . . designed with high capacitance and a capacitance change of greater than TEN TIMES for a bias change from 2 to 10 volts. Provides tuning over broad frequency ranges; tunes AM radio broadcast band, general AFC and tuning applications in lower RF frequencies.

- High Capacitance: 120–550 pF
- Large Capacitance Change with Small Bias Change
- Guaranteed High Q
- Available in Standard Axial Glass Packages
- H Suffix Devices with 100% Screening

HIGH TUNING RATIO VOLTAGE-VARIABLE CAPACITANCE DIODES

120-550 pF
12 VOLTS

MV1403
MV1404
MV1405



CASE 51
DO-204AA
(DO-7)

MV1401



CASE 146
DO-204AB
(DO-14)

100% SCREENING FOR HIGH RELIABILITY

MV1401H, MV1403H, MV1404H, MV1405H are screened with the following tests:

Internal Visual Inspection
per 12M53957B (MIL-STD-750 METHOD 2072 PARAGRAPH 3.3 AND METHOD 2074 PARAGRAPH 3.1.3)

High Temperature Storage
T_A = 200°C, t ≥ 48 hours

Thermal Shock (Temperature Cycling)
MIL-STD-202, Method 107, Condition C except 10 cycles continuously performed
t(extremes) = 15 minutes

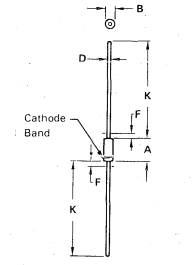
Constant Acceleration
MIL-STD-750, Method 2006
20,000 G's (Y1 axis only)

Hermetic Seal
MIL-STD-750, Method 1071
Fine Leak - Condition G
Gross Leak - Condition C, Step 1

Electrical Test
I_R and C_T

High Temperature Reverse Bias
T_A = 120°C ± 5°C, t ≥ 96 hours
V_R = 80% of $V_{(BR)R}$ MIN
Lower temperature till T_A = 30 ± 5°C.
Maintain this temperature prior to removal of Reverse Bias Voltage. Perform Electrical Test within 24 hours following bias removal.

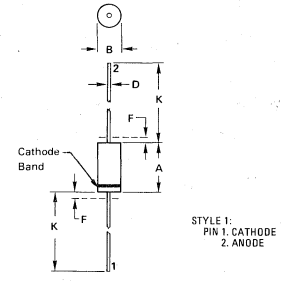
Electrical Test
I_R and C_T



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.84	7.62	0.230	0.300
B	2.16	2.72	0.085	0.107
D	0.46	0.56	0.018	0.022
F	–	1.27	–	0.050
K	25.40	38.10	1.000	1.500

All JEDEC dimensions and notes apply

CASE 51-02



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.84	7.62	0.230	0.300
B	2.74	3.56	0.108	0.140
D	0.46	0.56	0.018	0.022
F	–	1.27	–	0.050
K	25.40	–	1.000	–

All JEDEC dimensions and notes apply.

CASE 146-01

5

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	12	Volts
Forward Current	I_F	250	mA
Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	400 2.67	mW mW/°C
Junction Temperature	T_J	+175	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic — All Types	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	$V_{(BR)R}$	12	—	—	Vdc
Leakage Current at Reverse Voltage (V_R = 10 Vdc, T_A = 25°C)	I_R	—	—	0.10	μAdc
Series Inductance (f = 250 MHz, Lead Length ≈ 1/16")	L_S	—	5.0	—	nH
Case Capacitance (f = 1.0 MHz, Lead Length ≈ 1/16")	C_C	—	0.25	—	pF

	C_T, Diode Capacitance						Q, Figure of Merit	TR, Tuning Ratio	
	V_R = 1.0 Vdc, f = 1.0 MHz pF			V_R = 2.0 Vdc, f = 1.0 MHz pF			V_R = 2.0 Vdc, f = 1.0 MHz	C_1/C_{10} f = 1.0 MHz	C_2/C_{10} f = 1.0 MHz
Device	Min	Nom	Max	Min	Nom	Max	Min	Min	Min
MV1401, H	468	550	633	—	—	—	200	14	—
MV1403, H	—	—	—	140	175	210	200	—	10
MV1404, H	—	—	—	96	120	144	200	—	10
MV1405, H	—	—	—	200	250	300	200	—	10

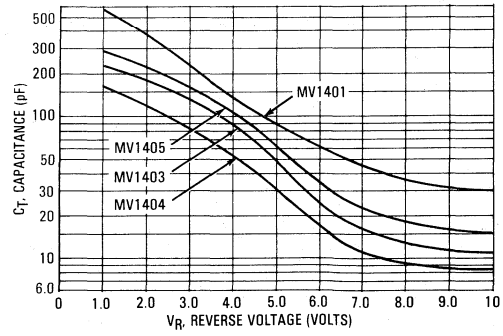
PARAMETER TEST METHODS

1. **L_S, SERIES INDUCTANCE**
   L_S is measured on a shorted package at 250 MHz using an impedance bridge (Boonton Radio Model 250A RX Meter).
2. **C_C, CASE CAPACITANCE**
   C_C is measured on an open package at 1.0 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).
3. **C_T, DIODE CAPACITANCE**
   ($C_T = C_C + C_J$) C_T is measured at 1.0 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).
4. **TR, TUNING RATIO**
   TR is the ratio of C_T measured at 2.0 Vdc (1.0 Vdc for MV1401) divided by C_T measured at 10 Vdc.
5. **Q, FIGURE OF MERIT**
   Q is calculated by taking the G and C readings of an admittance bridge at the specified frequency and substituting in the following equation:

$$Q = \frac{2\pi fC}{G}$$

(Boonton Electronics Model 33AS8). Use Lead Length ≈ 1/16".

FIGURE 1 — DIODE CAPACITANCE versus REVERSE VOLTAGE



MVAM108
MVAM109
MVAM115
MVAM125

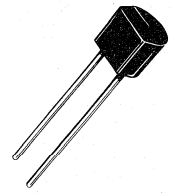
VVC

SILICON TUNING DIODE

. . . designed for electronic tuning of AM receivers and high capacitance, high tuning ratio applications.

- High Capacitance Ratio — C_R = 15 (Min), MVAM 108, 115, 125
- Guaranteed Diode Capacitance — C_t = 440 pF (Min) — 560 pF (Max) @ V_R = 1.0 Vdc, f = 1.0 MHz, MVAM108, MVAM115, MVAM125
- Guaranteed Figure of Merit — Q = 150 (Min) @ V_R = 1.0 Vdc, f = 1.0 MHz.

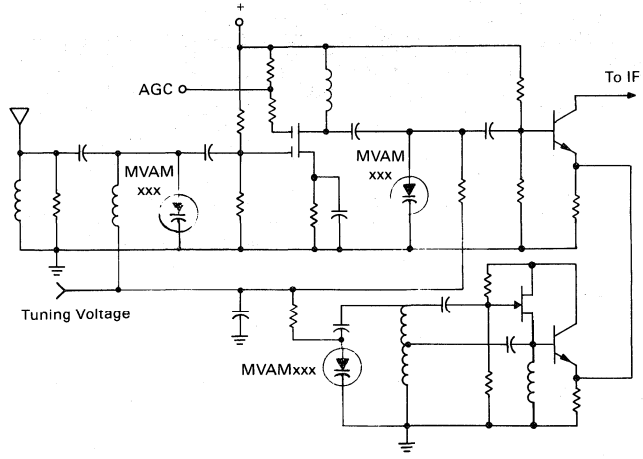
TUNING DIODES WITH VERY HIGH CAPACITANCE RATIO

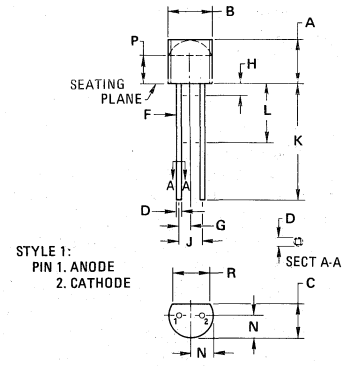


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage MVAM108 MVAM109 MVAM115 MVAM125	V_R	 12 15 18 28	Volts
Forward Current	I_F	50	mA
Power Dissipation @ T_A = 25°C Derate Above 25°C	P_D	280 2.8	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +125	°C

FIGURE 1 — TYPICAL AM RADIO APPLICATION





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.356	0.533	0.014	0.021
F	0.407	0.482	0.016	0.019
G	1.27 BSC		0.050 BSC	
H	–	1.27	–	0.050
J	2.54 BSC		0.100 BSC	
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.66	0.080	0.105
P	2.93	–	0.115	–
R	3.43	–	0.135	–

All JEDEC dimensions and notes apply

CASE 182-02

5

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted, Each Device)

Characteristic — All Types		Symbol	Min	Typ	Max	Unit
Breakdown Voltage		$V_{(BR)R}$				Vdc
(I_R = 10 μAdc)	MVAM108		12	—	—	
	MVAM109		15	—	—	
	MVAM115		18	—	—	
	MVAM125		28	—	—	
Reverse Current		I_R				nAdc
(V_R = 8.0 V)	MVAM108		—	—	100	
(V_R = 9.0 V)	MVAM109		—	—	100	
(V_R = 15 V)	MVAM115		—	—	100	
(V_R = 25 V)	MVAM125		—	—	100	
Diode Capacitance Temperature Coefficient (1) (V_R = 1.0 Vdc, f = 1.0 MHz, T_A = −40°C to +85°)		TC_C	—	435	—	ppm/°C
Case Capacitance (f = 1.0 MHz, Lead Length 1/16")		C_C	—	0.18	—	pF
Diode Capacitance (2)		C_t				pF
(V_R = 1.0 Vdc, f = 1.0 MHz)	MVAM108, 115, 125		440	500	560	
	MVAM109		400	460	520	
Figure of Merit (f = 1.0 MHz, Lead Length 1/16")		Q	150	—	—	—
Capacitance Ratio						—
(f = 1.0 MHz)	MVAM108	C1/C8	15	—	—	
	MVAM109	C1/C9	12	—	—	
	MVAM115	C1/C15	15	—	—	
	MVAM125	C1/C25	15	—	—	

Notes:
(1) The effect of increasing temperature 1.0°C, at any operating point, is equivalent to lowering the effective tuning voltage 1.25 mV. The percent change of capacitance per °C is nearly constant from −40°C to +100°C.
(2) Upon request, diodes are available in matched sets. All diodes in a set can be matched for capacitance to 3% or 2.0 pF (whichever is greater) at all points along the specified tuning range.

FIGURE 2 — CAPACITANCE versus REVERSE VOLTAGE

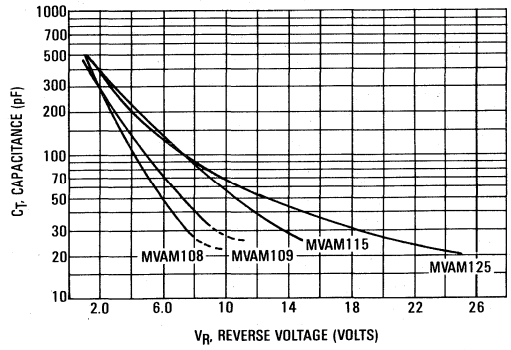
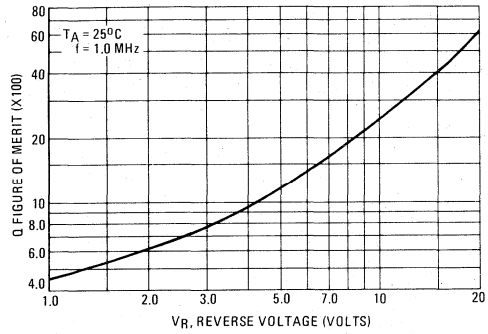
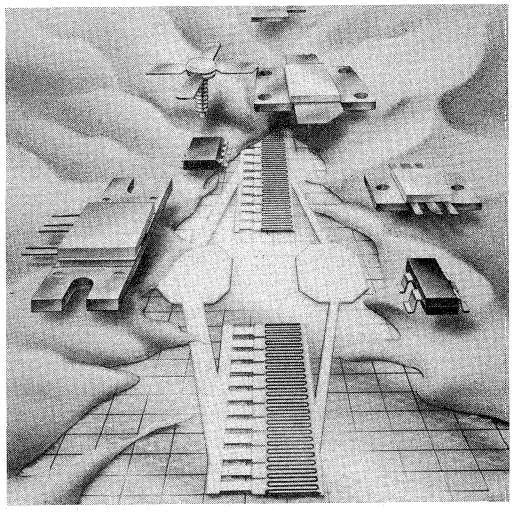


FIGURE 3 — FIGURE OF MERIT





Technical Information

Transistor Design

Application Notes

Reliability and Quality Assurance

Class C Power

The primary concern of the RF transistor designer is meeting the requirements for output power, gain, and ruggedness at the specified frequency and supply voltage.

Most RF applications typically require 12.5 or 28 volt operation of a power device in a mobile transmitter, base station, or avionics application. This choice dictates the epitaxial layer resistivity. Low resistivity, about 1 ohm/cm, is used for mobile devices, while 28 V base station and avionics devices are usually built using epi with 2 ohm/cm resistivity. Epi resistivity controls collector breakdown voltage, since the resistivity value determines the maximum possible breakdown voltage. Typically, a particular device rarely achieves this bulk breakdown value because of junction curvature and surface effects. When high voltages are present in an amplifier, high breakdown voltages are needed if the transistor is to survive. High voltage breakdowns are usually obtained by such added features as collector depletion rings, or by a high voltage diffusion surrounding the relatively shallow RF base diffusion. Voltages in excess of 150 volts are easily obtained this way.

Output power is determined primarily by the "electrical size" of the chip. Two common methods of sizing are emitter diffusion periphery and base diffusion area. Emitter periphery sizing is based on the premise that there is some optimum current which should be injected for each mil of emitter periphery. The base area sizing is based on an optimum power density. Both of these techniques are oversimplifications which make it impossible to apply them to widely varying device geometries and applications. Motorola uses a different method of sizing based on each geometry's Current Factor. Current Factor values are obtained by considering both emitter periphery effects and power density. Proper weighting of both factors makes this technique of sizing widely applicable. No matter what sizing technique is chosen, the end result is that greater power-handling capability requires larger chips. Small-signal devices, with only a few milliwatts of output power, and large devices with 100 watts output, range from current factors of only 1 to nearly 2000.

An alternative approach to high output power is to use several smaller chips in parallel. Unless extreme care is taken, this approach can result in unequal current and power sharing. Single large chips are also susceptible to this sharing problem unless specific steps are taken to ensure even current distribution. The primary method of handling this problem is by the use of well-designed emitter resistor layouts. The lowest value of emitter resistance on a chip is chosen to prevent thermal runaway up to the highest temperatures the device may encounter, possibly up to 300°C during output impedance mismatch conditions. An appropriate matrix of emitter resistance values is constructed so that the overall current distribution among the many parallel emitter sites results in an even thermal distribution. Verification of thermal balance is obtained by precise infrared microscope measurements across the entire chip.

The thermal balance of larger chips is also improved considerably by "cell spreading." In this techique the base diffusion area is broken up into smaller areas, or cells, and each cell is sufficiently removed from those adjacent to eliminate thermal interaction. The net effect is to achieve lower thermal resistance. This is exceedingly important in large devices where high power dissipation levels can cause excessive junction temperature when thermal resistance is not minimized. Some symptoms of excessively high temperature operation are low efficiency, power slump, and, frequently, total device failure.

The overall ruggedness of a transistor is enhanced by many techniques. All of them are aimed at preventing two things: junction breakdown due to excessive voltages and failure due to hot-spotting. Here again, epitaxial layer resistivity and thickness are used to alter breakdown voltages and saturated output power. Thermal balancing by base cell spreading and using emitter resistors also has a strong effect on ruggedness. These techniques are commonly referred to as collector and emitter ballasting. Ballasting of either type can improve ruggedness for a fixed geometry size (current factor), but there is a definite trade-off with gain. Usually increasing ruggedness requires decreasing gain unless one is willing to pay the penalty of the cost of larger die.

Large die can also adversely affect gain, since it is a practical fact that gain decreases by 2 dB for each doubling in current factor. To offset this gain decrease, the designer has another technique available—increase the packing denisty within the chip. The most common method of measuring packing density is with the figure of merit obtained

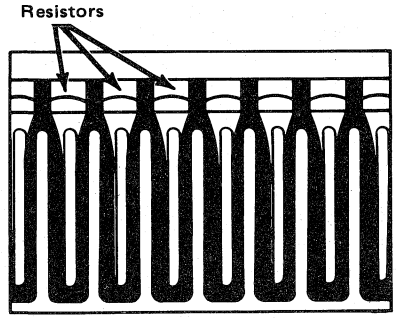
from the ratio of emitter periphery (E_P) to base area (B_A) of the chip. Higher E_P/B_A ratios result in higher gain. Typically, E_P/B_A ratios are as shown in the table.

E_P/B_A	FREQUENCY	GEOMETRY TYPE
0.5–1.5	3–30 MHz	Interdigitated
1.5–3.5	VHF	Interdigitated or Spine (Overlay)
3.5–4.5	UHF	Spine (Overlay) or Mesh (Network)
5.5–6.5	800–900 MHz	Mesh

Higher E_P/B_A ratios generally mean greater processing difficulties. These difficulties are somewhat offset by the choice of geometry type. Fundamentally, the interdigitated geometry requires narrow spacing between emitter and base fingers and narrow finger widths. The maximum E_P/B_A ratio obtainable with an interdigitated structure of uniform spacing "S" is given by

$$(E_P/B_A)\ MAX = \frac{0.45}{S}.$$

Spacings of 0.08 mil are the minimum easily obtainable with current technology, giving a maximum figure of merit of 5.6. Actual devices with this spacing are usually about 4.5. Building a large power device using this geometry calls for a great many narrow metallization fingers.



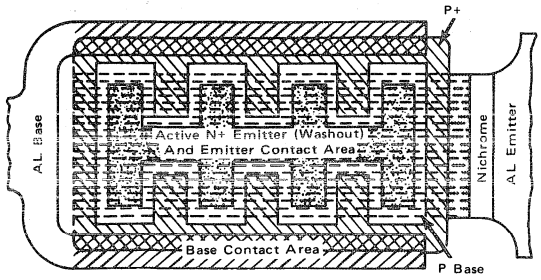
Enlargement of this "interdigitated" geometry shows emitter resistors that have been added to balance the current throughout the chip.

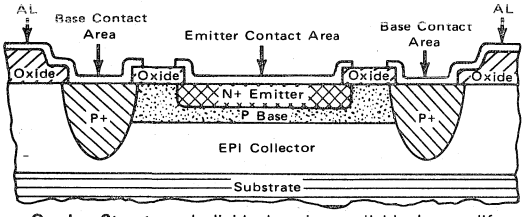
This approach increases the probability of a metallization defect linking adjoining fingers and enhances failures due to metal migration. The spine or mesh geometries used for higher figure of merit do not completely relieve the tight spacing requirements. In both cases, tight metal spacing is relieved while diffusion spacings are not. For example, 4.5 is the maximum E_P/B_A ratio for a 0.1 mil spacing with an interdigitated device. Motorola's family of UHF power devices MRF641 (15 watt), MRF644 (25 watt), MRF646 (45 watt), and MRF648 (60 watt) are constructed using a split mesh (adjoining emitter fingers are not interconnected). All four devices have an E_P/B_A ratio of 4 and are built with a 0.1 mil spacing between adjacent emitter and P+ diffusion areas. Similar tight spacing is required in the mesh geometry used for the 800–900 MHz 7, 20, 30, and 40 watt devices. Here the spacing is reduced to 0.06 mil, using a mesh geometry. Without tight spacing of emitter to P+ such as these devices have, high E_P/B_A ratios will not produce good gain. The introduction of the P+ is required to maintain full utilization of all elements of the emitter periphery. Introducing undulations in the shape of the emitter to increase the periphery without a closely spaced P+ will cause some elements of the periphery to be debiased due to uneven base voltage drops.

The metal migration failure rate as measured by MTBF (Mean Time Before Failure) depends on current density, metallization cross-sectional area, and activation energy. Activation energy may be varied by the choice of metallization with gold and aluminum being the two most common choices. Motorola uses gold metallization for both avionics and 28 volt base station devices where continuous operation is anticipated. Mobile devices are usually constructed of aluminum. In either case, devices are designed for a minimum of 10 years MTBF.

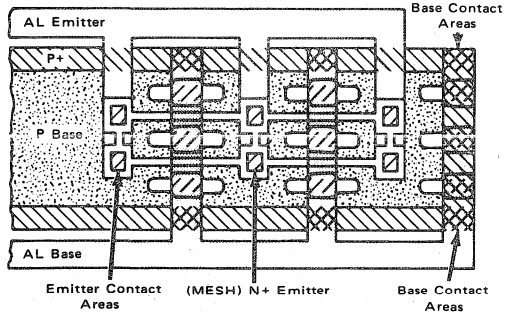
Linear Power

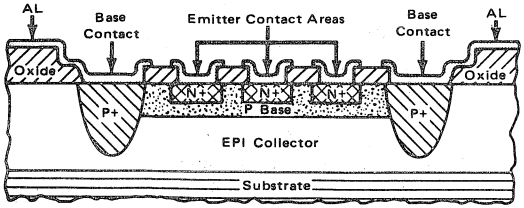
Linear operation is usually accomplished by building the same type of transistor structure as used in Class C operation. The major difference is the linearity requirements force the use of devices with larger current factors. They are also usually fabricated with slightly lower collector resistivity. The combination of these factors allows the device to maintain good linearity with high power output levels. Motorola has led the industry with its family of SSB large-chip transistors, MRF421, MRF422, MRF428. These chips are large, 140 X 250 mils, and have Current Factors approaching 2000. The higher voltage devices are built using a combination of both depletion rings and deep P+ high voltage diffusions. All feature thermal ballasting through emitter resistor matrices.





Overlay Structure. Individual emitter cell blocks are diffused into a common base region. Emitter interconnection runs are made over a passivating silicon dioxide layer, reducing the need for critically thin interdigitated metal fingers.





Network Emitter Structure. This structure maximizes emitter periphery to base area ratio but pays for it with increased production difficulty and increased contact resistance.

Motorola employs a thin nichrome barrier (not shown) between the silicon and the aluminum metalization in most network emitter and overlay devices to prevent aluminum metal migration thus improving long-term reliability.

Small Signal

Small-signal devices are constructed from the same types of geometries as used for power devices except on a much smaller scale of Current Factor. The small geometries do not suffer from the gain reduction due to size, allowing the use of lower E_P/B_A ratios for equivalent gain.

Quite commonly, small-signal transistors are not only required to have a minimum gain, but also a minimum f_t. This parameter is a measure of the total emitter-to-collector transit time. As the collector current is increased, the value of f_t increases initially, peaks, and then finally decreases. The peak value is determined by the base and emitter region transit times. This parameter is controlled by both the base junction depth and the emitter doping species. Using conventional diffusion processes with a single base and emitter diffusion, maximum achievable f_t for NPN transistors is about 3-4 GHz without severely degrading the normally desirable dc characteristics, namely BV_{CEO} and h_{FE}.

The logical solution is to use arsenic as the emitter dopant species. Arsenic has an advantage over the more commonly used phosphorus diffusion source. The concentration dependent diffusivity of arsenic causes a very abrupt emitter profile. The increased profile gradient reduces the storage of free carriers in the emitter space charge layer, reducing the layer transit time, and increasing f_t. Unfortunately, arsenic diffusion technology is difficult at best.

The simplest method for using arsenic as a dopant species is to implant it. Motorola has recently introduced transistors with implanted arsenic emitters. These devices have typical f_t of 8 GHz without sacrificing dc characteristics.

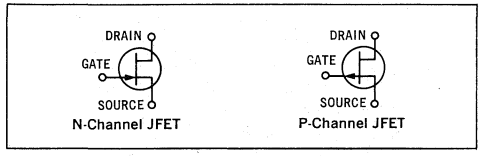
A family of low noise devices has also been fabricated using similar processes. Low noise figure (NF) places additional requirements on both f_t, the doping density of the base under the emitter, and the emitter diffusion width. Through special controlled processing, excellent NF values are obtained in the 1 to 2 GHz region. This performance requires high f_t, low base spreading resistance, and 0.05 mil wide arsenic implanted emitters.

6

FIELD EFFECT TRANSISTORS IN THEORY AND PRACTICE

INTRODUCTION

There are two types of field-effect transistors, the Junction Field-Effect Transistor (JFET) and the "Metal-Oxide Semiconductor" Field-Effect Transistor (MOSFET), or Insulated-Gate Field-Effect Transistor (IGFET). The principles on which these devices operate (current controlled by an electric field) are very similar – the primary difference being in the methods by which the control element is made. This difference, however, results in a considerable difference in device characteristics and necessitates variances in circuit design, which are discussed in this note.



JUNCTION FIELD-EFFECT TRANSISTOR (JFET)

In its simplest form the junction field-effect transistor starts with nothing more than a bar of doped silicon that behaves as a resistor (Figure 1a). By convention, the terminal into which current is injected is called the source terminal, since, as far as the FET is concerned, current originates from this terminal. The other terminal is called the drain terminal. Current flow between source and drain is related to the drain-source voltage by the resistance of the intervening material. In Figure 1b, p-type regions have been diffused into the n-type substrate of Figure 1a leaving an n-type channel between the source and drain. (A complementary p-type device is made by reversing all of the material types.) These p-type regions will be used to control the current flow between the source and the drain and are thus called gate regions.

As with any p-n junction, a depletion region surrounds the p-n junctions when the junctions are reverse biased (Figure 1c). As the reverse voltage is increased, the depletion regions spread into the channel until they meet, creating an almost infinite resistance between the source and the drain.

If an external voltage is applied between source and drain (Figure 1d) with zero gate voltage, drain current flow in the channel sets up a reverse bias along the surface of the gate, parallel to the channel. As the drain-source voltage increases, the depletion regions again spread into the channel because of the voltage drop in the channel which reverse biases the junctions. As V_{DS} is increased, the depletion regions grow until they meet, whereby any further increase in voltage is counterbalanced by an increase in the depletion region toward the drain. There is an effective increase in channel resistance that prevents any further increase in drain current. The drain-source voltage that causes this current limiting condition is called the "pinch-off" voltage (V_p). A further increase in drain-source voltage produces only a slight increase in drain current.

The variation in drain current (I_D) with drain-source voltage (V_{DS}) at zero gate-source voltage (V_{GS}) is shown in Figure 2a. In the low-current region, the drain current is linearly related to V_{DS}. As I_D increases, the "channel" begins to deplete and the slope of the I_D curve decreases. When the V_{DS} is equal to V_p, I_D "saturates" and stays relatively constant until drain-to-gate avalanche, $V_{BR(DSS)}$ is reached. If a reverse voltage is applied to the gates, channel pinch-off occurs at a lower I_D level (Figure 2b) because the depletion region spread caused by the reverse-

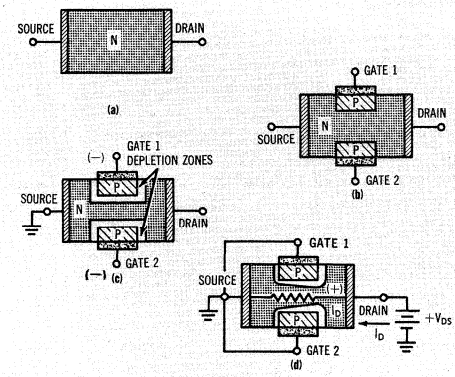


FIGURE 1 – Development of Junction Field-Effect Transistors

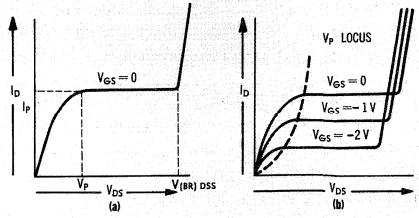
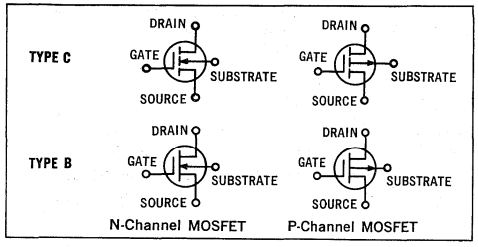


FIGURE 2 – Drain Current Characteristics

biased gates adds to that produced by V_{DS}. Thus reducing the maximum current for any value of V_{DS}.

Due to the difficulty of diffusing impurities into both sides of a semiconductor wafer, a single ended geometry is normally used instead of the two-sided structure discussed above. Diffusion for this geometry (Figure 3) is from one side only. The substrate is of p-type material onto which an n-type channel is grown epitaxially. A p-type gate is then diffused into the n-type epitaxial channel. Contact metalization completes the structure.

The substrate, which functions as Gate 2 of Figure 1, is of relatively low resistivity material to maximize gain. For the same purpose, Gate 1 is of very low resistivity material, allowing the depletion region to spread mostly into the n-type channel. In most cases the gates are internally connected together. A tetrode device can be realized by not making this internal connection.



MOS FIELD-EFFECT TRANSISTORS (MOSFET)

The metal-oxide-semiconductor (MOSFET) operates with a slightly different control mechanism than the JFET. Figure 4 shows the development. The substrate may be high resistivity p-type material, as for the 2N4351. This time two separate low-resistivity n-type regions (source and drain) are diffused into the substrate as shown in Figure 4b. Next, the surface of the structure is covered with an insulating oxide layer and a nitride layer. The oxide layer serves as a protective coating for the FET surface and to insulate the channel from the gate. However the oxide is subject to contamination by sodium ions which are found in varying quantities in all environments. Such contamination results in long term instability and changes in device characteristics. Silicon nitride is impervious to sodium ions and thus is used to shield the oxide layer from contamination. Holes are cut into the oxide and nitride layers allowing metallic contact to the source and drain. Then, the gate metal area is overlayed on the insulation, covering the entire channel region and, simultaneously, metal contacts to the drain and source are made as shown in Figure 4d. The contact to the metal area covering the channel is the gate terminal. Note that there is no physical penetration of the metal through the oxide and nitride into the substrate. Since the drain and source are isolated by the substrate, any drain-to-source current in the absence of gate voltage is extremely low because the structure is analogous to two diodes connected back to back.

The metal area of the gate forms a capacitor with the insulating layers and the semiconductor channel. The metal area is the top plate; the substrate material and channel are the bottom plate.

For the structure of Figure 4, consider a positive gate potential (see Figure 5). Positive charges at the metal side of the metal-oxide capacitor induce a corresponding negative charge at the semiconductor side. As the positive charge at the gate is increased, the negative charge "induced" in the semiconductor increases until the region beneath the oxide effectively becomes an n-type semiconductor region, and current can flow between drain and source through the "induced" channel. In other words, drain current flow is "enhanced" by the gate potential. Thus drain current flow can be modulated by the gate voltage; i.e. the channel resistance is directly related to the gate voltage. The n-channel structure may be changed to a p-channel device by reversing the material types.

An equivalent circuit for the MOSFET is shown in Figure 6. Here, $C_{g(ch)}$ is the distributed gate-to-channel

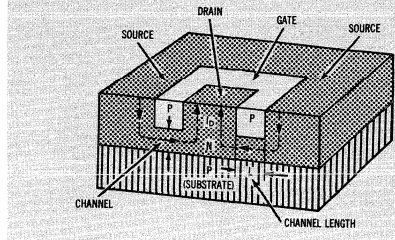


FIGURE 3 – Junction FET with Single-Ended Geometry

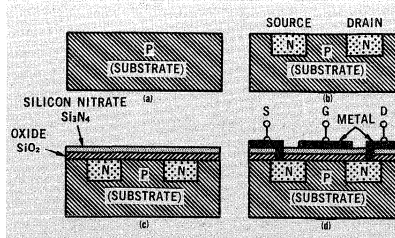


FIGURE 4 – Development of Enhancement-Mode N-Channel MOSFET

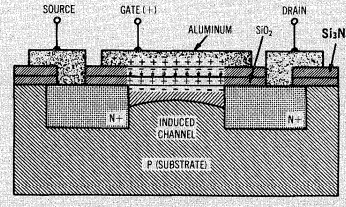


FIGURE 5 – Channel Enhancement. Application of Positive Gate Voltage Causes Redistribution of Minority Carriers in the Substrate and Results in the Formation of a Conductive Channel Between Source and Drain

capacitance representing the nitride-oxide capacitance. C_{gs} is the gate-source capacitance of the metal gate area overlapping the source, while C_{gd} is the gate-drain capacitance of the metal gate area overlapping the drain. $C_{d(sub)}$ and $C_{s(sub)}$ are junction capacitances from drain to substrate and source to substrate. Y_{fs} is the transadmittance between drain current and gate-source voltage. The modulated channel resistance is r_{ds}. R_D and R_S are the bulk resistances of the drain and source.

The input resistance of the MOSFET is exceptionally high because the gate behaves as a capacitor with very low leakage ($r_{in} \approx 10^{14}\ \Omega$). The output impedance is a function of r_{ds} (which is related to the gate voltage) and the drain and source bulk resistances (R_D and R_S).

To turn the MOSFET "on", the gate-channel capacitance, $C_{g(ch)}$, and the Miller capacitance, C_{gd}, must be charged. In turning "on", the drain-substrate capacitance, $C_{d(sub)}$, must be discharged. The resistance of the substrate determines the peak discharge current for this capacitance.

The FET just described is called an enhancement-type MOSFET. A depletion-type MOSFET can be made in the following manner: Starting with the basic structure of Figure 4, a moderate resistivity n-channel is diffused between the source and drain so that drain current can flow when the gate potential is at zero volts (Figure 7). In this manner, the MOSFET can be made to exhibit depletion characteristics. For positive gate voltages, the structure enhances in the same manner as the device of Figure 4. With negative gate voltage, the enhancement process is reversed and the channel begins to deplete of carriers as seen in Figure 8. As with the JFET, drain-current flow depletes the channel area nearest the drain first.

The structure of Figure 7, therefore, is both a depletion-mode and an enhancement-mode device.

MODES OF OPERATION

There are two basic modes of operation of FET's – depletion and enhancement. Depletion mode, as previously mentioned, refers to the decrease of carriers in the channel due to variation in gate voltage. Enhancement mode refers to the increase of carriers in the channel due to application of gate voltage. A third type of FET that can operate in both the depletion and the enhancement modes has also been described.

The basic differences between these modes can most easily be understood by examining the transfer characteristics of Figure 9. The depletion-mode device has considerable drain-current flow for zero gate voltage. Drain current is reduced by applying a reverse voltage to the gate terminal. The depletion-type FET is not characterized with forward gate voltage.

The depletion/enhancement mode type device also has considerable drain current with zero gate voltage. This type device is defined in the forward region and may have usable forward characteristics for quite large gate voltages. Notice that for the junction FET, drain current may be enhanced by forward gate voltage only until the gate-source p-n junction becomes forward biased.

The third type of FET operates only in the enhancement mode. This FET has extremely low drain current flow for zero gate-source voltage. Drain current conduction occurs for a V_{GS} greater than some threshold value, $V_{GS(th)}$. For gate voltages greater than the threshold, the transfer characteristics are similar to the depletion/enhancement mode FET.

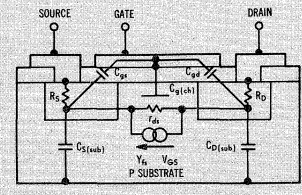


FIGURE 6 – Equivalent Circuit of Enhancement-Mode MOSFET

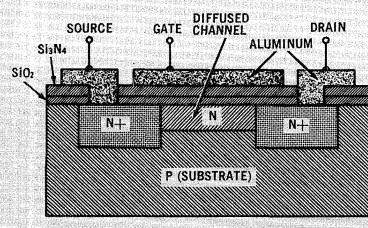


FIGURE 7 – Depletion Mode MOSFET Structure. This Type of Device may be Designed to Operate in Both the Enhancement and Depletion Modes

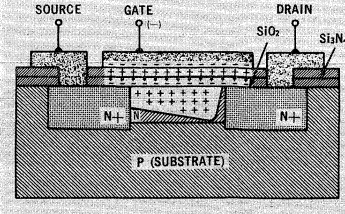


FIGURE 8 – Channel Depletion Phenomenon. Application of Negative Gate Voltage Causes Redistribution of Minority Carriers in Diffused Channel and Reduces Effective Channel Thickness. This Results in Increased Channel Resistance

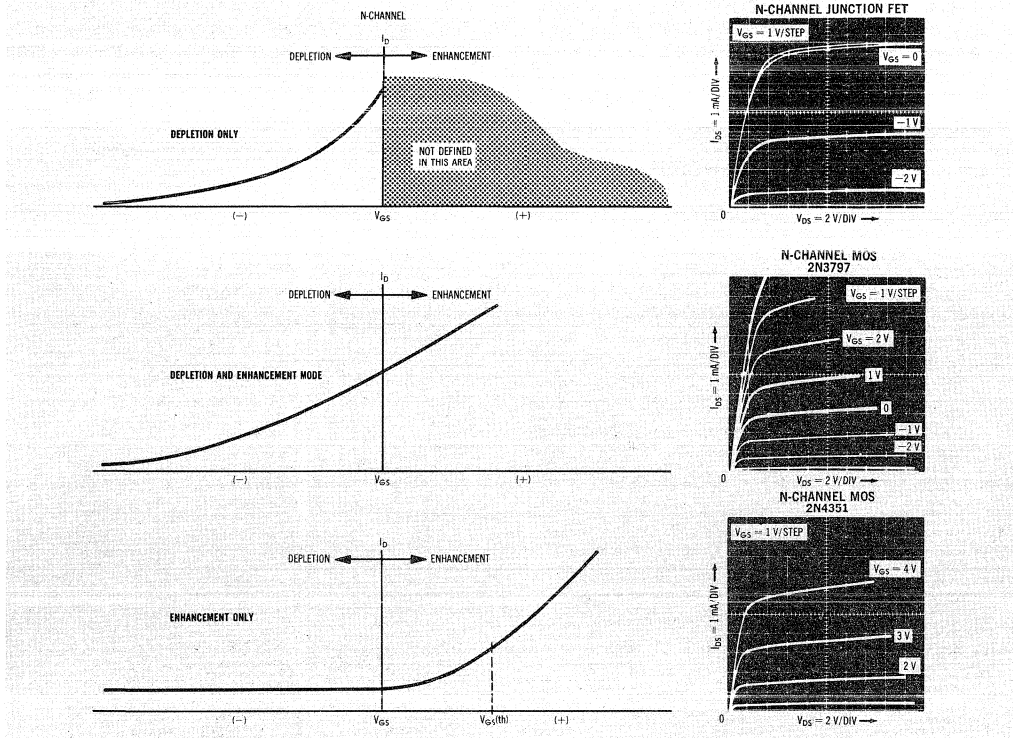


FIGURE 9 — Transfer Characteristics and Associated Scope Traces for the Three FET Types

ELECTRICAL CHARACTERISTICS

Because the basic mode of operation for field-effect devices differs greatly from that of conventional junction transistors, the terminology and specifications are necessarily different. An understanding of FET terminology and characteristics are necessary to evaluate their comparative merits from data-sheet specifications.

Static Characteristics

Static characteristics define the operation of an active device under the influence of applied dc operating conditions. Of primary interest are those specifications that indicate the effect of a control signal on the output current. The V_{GS}–I_D transfer characteristics curves are illustrated in Figure 9 for the three types of FETs. Figure 10 lists the data-sheet specifications normally employed to describe these curves, as well as the test circuits that yield the indicated specifications.

Of additional interest is the special case of tetrode-connected devices in which the two gates are separately accessible for the application of a control signal. The pertinent specifications for a junction tetrode are those which define drain-current cutoff when one of the gates is connected to the source and the bias voltage is applied to the second gate. These are usually specified as $V_{G1S(off)}$, Gate 1 – source cutoff voltage (with Gate 2 connected to source), and $V_{G2S(off)}$, Gate 2 – source cutoff voltage (with Gate 1 connected to source). The gate voltage required for drain current cutoff with one of the gates connected to the source is always higher than that for the triode-connected case where both gates are tied together.

Reach-through voltage is another specification uniquely applicable to tetrode-connected devices. This defines the amount of difference voltage that may be applied to the two gates before the depletion region of one spreads into the junction of the other – causing an increase in gate current to some small specified value. Obviously, reach-through is an undesirable condition since it causes a decrease in input resistance as a result of an increased gate current, and large amounts of reach-through current can destroy the FET.

Gate Leakage Current

Of interest to circuit designers is the input resistance of an active component. For FETs, this characteristic is specified in the form of I_{GSS} – the reverse-bias gate-to-source current with the drain shorted to the source (Figure 11). As might be expected, because the leakage current across a reverse-biased p-n junction (in the case of a JFET) and across a capacitor (in the case of a MOSFET) is very small, the input resistance is extremely high. At a temperature of 25°C, the JFET input resistance is hundreds of megohms while that of a MOSFET is even greater. For junction devices, however, input resistance may decrease by several orders of magnitude as temperature is raised to 150°C. Such devices, therefore, have gate-leakage current specified at two temperatures. Insulated-gate FETs are not drastically affected by temperature, and their input resistance remains extremely high even at elevated temperatures.

Gate leakage current may also be specified as I_{GDO} (leakage between gate and drain with the source open), or as I_{GSO} (leakage between gate and source with the drain open). These usually result in lower values of leakage current and do not represent worst-case conditions. The I_{GSS} specification, therefore, is usually preferred by the user.

Voltage Breakdown

A variety of specifications can be used to indicate the maximum voltage that may be applied to various elements of a FET. Among those in common use are the following:

$V_{(BR)GSS}$ = Gate-to-source breakdown voltage

$V_{(BR)DGO}$ = Drain-to-gate breakdown voltage

$V_{(BR)DSX}$ = Drain-to-source breakdown voltage (normally used only for MOSFETs)

In addition, there may be ratings and specifications indicating the maximum voltages that may be applied between the individual gates and the drain and source (for tetrode-connected devices). Obviously, not all of these specifications are found on every data sheet since some of them provide the same information in somewhat different form. By understanding the various breakdown mechanisms, however, the reader should be able to interpret the intent of each specification and rating. For example:

In junction FETs, the maximum voltage that may be applied between any two terminals is the lowest voltage that will lead to breakdown or avalanche of the gate junction. To measure $V_{(BR)GSS}$ (Figure 12a), an increasingly higher reverse voltage is applied between the gate and the source. Junction breakdown is indicated by an increase in gate current (beyond I_{GSS}) which signals the beginning of avalanche.

Some reflection will reveal that for junction FETs, the $V_{(BR)DGO}$ specification really provides the same information as $V_{(BR)GSS}$. For this measurement, an increasing voltage is applied between drain and gate. When this applied voltage becomes high enough, the drain-gate junction will go into avalanche, indicated either by a significant increase in drain current or by an increase in gate current (beyond I_{DGO}). For both $V_{(BR)DGO}$ and $V_{(BR)GSS}$ specifications, breakdown should normally occur at the same voltage value.

From Figure 2 it is seen that avalanche occurs at a lower value of V_{DS} when the gate is reverse biased than for the zero-bias condition. This is caused by the fact that the reverse-bias gate voltage adds to the drain voltage, thereby increasing the effective voltage across the junction. The maximum amount of drain-source voltage that may be applied $V_{DS(max)}$ is, therefore, equal to $V_{(BR)DGO}$ minus V_{GS}, which indicates avalanche with reverse bias gate voltage applied.

For MOSFETs, the breakdown mechanism is somewhat different. Consider, for example, the enhancement-mode structure of Figure 5. Here, the gate is completely insulated from the drain, source, and channel by an oxide-nitride layer. The breakdown voltage between the gate and any of the other elements, therefore, is dependent on the thickness and purity of this insulating layer, and represents the voltage that will physically puncture the layer. Consequently, the voltage must be specified separately.

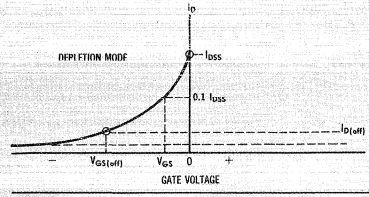
The drain-to-source breakdown is a different matter. For enhancement mode devices, with the gate connected to the source (the cutoff condition) and the substrate floating, there is no effective channel between drain and source and the applied drain-source voltage appears across two opposed series diodes, represented by the source-to-substrate and substrate-to-drain junctions. Drain current remains at a very low level (picoamperes) as drain voltage is increased until the drain voltage reaches a value that causes reverse (avalanche) breakdown of the diodes. This particular condition, represented by $V_{(BR)DSS}$, is indicated by an increase in I_D above the I_{DSS} level, as shown in Figure 12b.

For depletion/enhancement mode devices, the $V_{(BR)DSS}$ symbol is sometimes replaced by $V_{(BR)DSX}$. Note that the principal difference between the two symbols is the replacement of the last subscript s with the subscript x. Whereas the s normally indicates that the gate is shorted to the source, the x indicates that the gate is biased to cutoff or beyond. To achieve cutoff in these devices, a depleting bias voltage must be applied to the gate, Figure 12b.

An important static characteristic for switching FETs is the "on" drain-source voltage $V_{DS(on)}$. This characteristic for the MOSFETs is a function of V_{GS}, and resembles the $V_{CE(sat)}$ versus I_B characteristics of junction transistors. The curve for these characteristics can be used as a design guide to determine the minimum gate voltage necessary to achieve a specified output logic level.

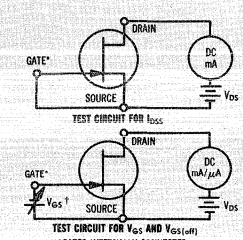
Dynamic Characteristics

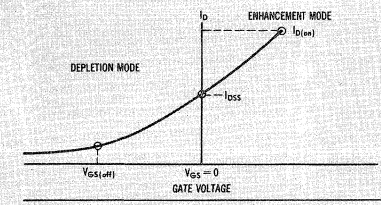
Unlike the static characteristics, the dynamic characteristics of field-effect transistors apply equally to all FETs. The conditions and presentation of the dynamic characteristics, however, depend largely upon the intended application. For example, the following table indicates the dynamic characteristics needed to adequately describe



DEPLETION MODE JFETs

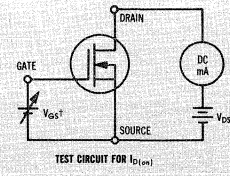
CHARACTERISTIC	DESCRIPTION
I_{DSS} @ $V_{GS} = 0$, $V_P < V_{DS} < V_{(BR)\,DSS}$	Zero-gate-voltage drain current. Represents maximum drain current.
$V_{GS(off)}$ @ $I_D = 0.001\ I_{DSS}$, $V_P < V_{DS} < V_{(BR)\,DSS}$	Gate voltage necessary to reduce I_D to some specified negligible value at the recommended V_{DS}, i.e. cutoff.
V_{GS} @ $I_D = 0.1\ I_{DSS}$, $V_P < V_{DS} < V_{(BR)\,DSS}$	Gate voltage for a specified value of I_D between I_{DSS} and I_{DS} at cutoff — normally 0.1 I_{DSS}.

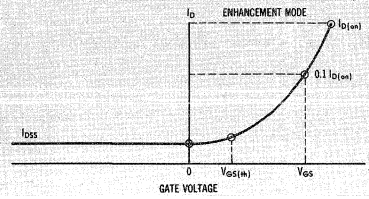




DEPLETION/ENHANCEMENT MODE MOSFETs

CHARACTERISTIC	DESCRIPTION
$I_{D(on)}$ @ $V_{GS} > 0$, $V_P < V_{DS} < V_{(BR)\,DSS}$	An arbitrary current value (usually near max rated current) that locates a point in the enhancement operating mode.
I_{DSS} @ $V_{GS} = 0$, $V_P < V_{DS} < V_{(BR)\,DSS}$	Zero-gate-voltage drain current.
$V_{GS(off)}$ @ $I_D = 0.001\ I_{DSS}$,	Voltage necessary to reduce I_D to some specified negligible value at the recommended V_{DS}, i.e. cutoff.





ENHANCEMENT MODE MOSFETs

CHARACTERISTIC	DESCRIPTION
$I_{D(on)}$ @ $V_{GS} > 0$, $V_P < V_{DS} < V_{(BR)\,DSS}$	An arbitrary current value (usually near max rated current) that locates a point in the enhancement operating mode.
V_{GS} @ 0.1 $I_{D(on)}$	Gate-source voltage for a specified drain current of 0.1 $I_{D(on)}$.
$V_{GS(th)}$ @ $I_D = 0.001\ I_{D(on)}$ or less	Gate cutoff or turn-on voltage.
I_{DSS} @ $V_{GS} = 0$, $V_P < V_{DS} < V_{(BR)\,DSS}$	Leakage drain current.

$I_{D(on)}$ **TEST CIRCUIT**
SAME AS FOR DEPLETION/ENHANCEMENT

V_{GS} **TEST CIRCUIT**
SAME AS FOR $I_{D(on)}$

$V_{GS(th)}$ **TEST CIRCUIT**
SAME AS $V_{GS(off)}$ FOR JFET
EXCEPT REVERSE V_{GS} BATTERY POLARITY

I_{DSS} **TEST CIRCUIT**
SAME AS FOR JFET

FIGURE 10 — Static Characteristics for the Three FET Types are Defined by the Above Curves, Tables, and Test Circuits

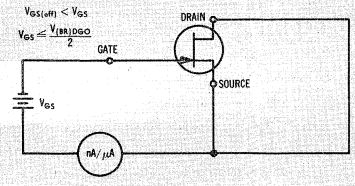


FIGURE 11 — Test Circuit for Leakage Current

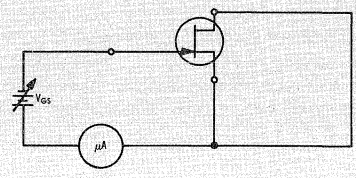


Figure 12a — $V_{(BR)GSS}$ Test Circuit

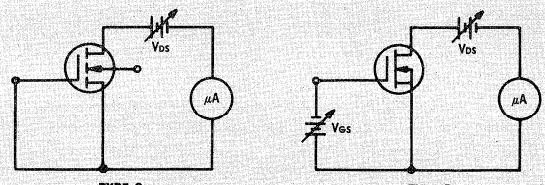


FIGURE 12b — $V_{(BR)DSS}$ and $V_{(BR)DSX}$ Test Circuit (Usually Used for MOSFETs Only).

Audio	RF-IF	Switching	Chopper
y_{fs} (1 kHz)	y_{fs} (1 kHz)		
C_{iss}	C_{iss}	C_{iss}	C_{iss}
C_{rss}	C_{rss}	C_{rss}	C_{rss}
y_{os} (1 kHz)	GP	$Cd_{(sub)}$	$Cd_{(sub)}$
NF	$Re(y_{is})$ (HF)	$r_{ds(on)}$	$r_{ds(on)}$
	$Re(y_{os})$ (HF)	t_{d1}, t_{d2}	
	NF	t_r, t_f	

a FET for various applications.

y_{fs} The forward transadmittance is a key dynamic characteristic for field-effect transistors. It serves as a basic design parameter in audio and rf circuits and is a widely accepted figure of merit for devices.

Because field-effect transistors have many characteristics similar to those of vacuum tubes, and because many engineers still are more comfortable with tube parameters, the symbol g_m used for tube transconductance is often specified instead of y_{fs}. To further confuse things, the "g" school also uses a variety of subscripts. In addition to g_m, some data sheets show g_{fs} while others even show g_{21}.

Regardless of the symbol used, y_{fs} defines the relation between an input signal voltage and an output signal current:

$$y_{fs} = \Delta I_D/\Delta V_{GS} \Big|_{V_{DS} = K}$$

The unit is the mho – current divided by voltage. Figure 13 is a typical y_{fs} test circuit for a junction FET.

As a characteristic of all field-effect devices, y_{fs} is specified at 1 kHz with a V_{DS} the same as that for which $I_{D(on)}$ or I_{DSS} is characterized. Since y_{fs} has both real and imaginary components, but is dominated by the real component at low frequency, the 1 kHz characteristic is given as an absolute magnitude and indicated as $|y_{fs}|$.

It is interesting to note that y_{fs} varies considerably with I_D due to nonlinearity in the I_D–V_{GS} characteristics. This variation, for a typical n-channel, JFET is illustrated in Figure 14. Obviously, the operating point must be carefully selected to provide the desired y_{fs} and signal swing.

For tetrode-connected FETs, three y_{fs} measurements are usually specified on data-sheet tables. One of these, with the two gates tied together, provides a y_{fs} value for the condition where a signal is applied to both gates simultaneously; the others provide the y_{fs} for the two gates individually. Generally, with the two gates tied together, y_{fs} is higher and more gain may be realized in a given circuit. Because of the increased capacitance, however, gain-bandwidth product is much lower.

For rf field-effect transistors, an additional value of y_{fs} is sometimes specified at or near the highest frequency of operation. This value should also be measured at the same voltage conditions as those used for $I_{D(on)}$ or I_{DSS}. Because of the importance of the imaginary component at radio frequencies, the high-frequency y_{fs} specification should be a complex representation, and should be given either in the specifications table or by means of curves showing typical variations, as in Figure 15 for the MPF102 JFET.

The real portion of this high-frequency y_{fs}, Re (y_{fs}) or G_{21}, is usually considered a significant figure of merit.

y_{os} Another FET parameter that offers a direct vacuum tube analogy is y_{os}, the output admittance:

$$y_{os} = \Delta I_D/\Delta V_{DS} \Big|_{V_{GS} = K}$$

In this case, the analogous tube parameter is r_p – i.e., $y_{os} = 1/r_p$. For depletion mode devices, y_{os} is measured with gate and source grounded (see Figure 16). For enhancement mode units, it is measured at some specified V_{GS} that permits substantial drain-current flow.

As with y_{fs}, many expressions are used for y_{os}. In

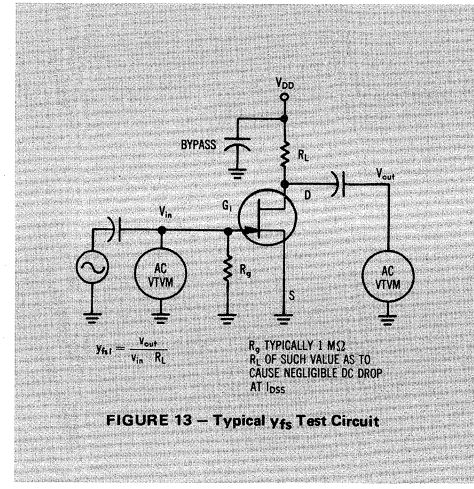


FIGURE 13 – Typical y_{fs} Test Circuit

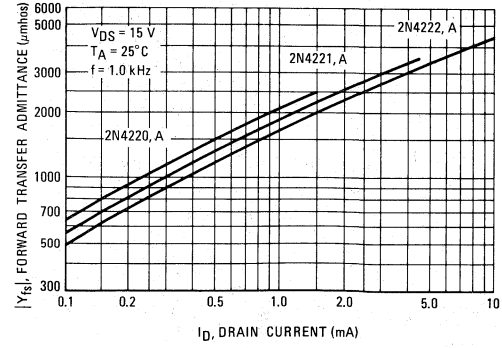


FIGURE 14 – Forward Transfer Admittance versus Drain Current for Typical JFETs

addition to the obvious parallels such as y_{22}, g_{os}, and g_{22}, it is also sometimes specified as r_d, where $r_d = 1/y_{os}$.

Voltages and frequencies for measuring y_{os} should be exactly the same as those for measuring y_{fs}. Like y_{fs}, it is a complex number and should be specified as a magnitude at 1 kHz and in complex form at high frequencies.

μ Closely related to y_{os} and y_{fs} is the amplification factor, μ:

$$\mu = \Delta V_{DS}/\Delta V_{GS} \Big|_{I_D = K}$$

The amplification factor does not appear on the field-effect transistor registration format but can be calculated as y_{fs}/y_{os}. For most small-signal applications, μ has little circuit significance. It does, however, serve as a general indication of the quality of the field-effect manufacturing process.

C_{iss} The common-source-circuit input capacitance, C_{iss}, takes the place of y_{is} in low-frequency field-effect transistors. This is because y_{is} is entirely capacitive at low frequencies. C_{iss} is conveniently measured in the circuit of Figure 17 for the tetrode JFET. As with y_{fs}, two measurements are necessary for tetrode-connected devices.

At very high frequencies, the real component of y_{is} becomes important so that rf field-effect transistors should have y_{is} specified as a complex number at the same conditions as other high-frequency parameters. For tetrode-connected rf FETs, reading of both Gate 2 to source and Gate 1 tied to Gate 2 are necessary.

In switching applications C_{iss} is of major importance since a large voltage swing at the gate must appear across C_{iss}. Thus, C_{iss} must be charged by the input voltage before turn-on effectively begins.

C_{rss} Reverse transfer admittance (y_{rs}) does not appear on FET data sheets. Instead C_{rss}, the reverse transfer capacitance, is specified at low frequency. Since y_{rs} for a field-effect transistor remains almost completely capacitive and relatively constant over the entire usable FET frequency spectrum, the low-frequency capacitance is an adequate specification. C_{rss} is measured by the circuit of Figure 18. For tetrode FETs, values should be specified for Gate 1 and for both gates tied together.

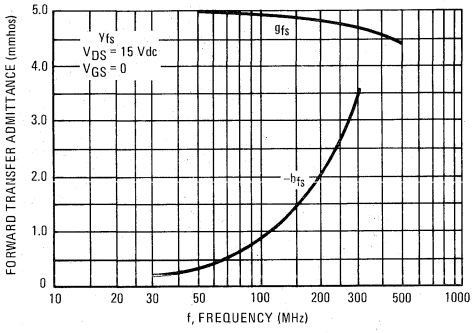


FIGURE 15 – Forward Transfer Admittance versus Frequency

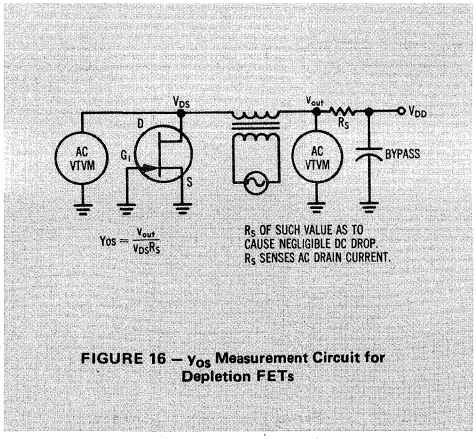


FIGURE 16 – y_{os} Measurement Circuit for Depletion FETs

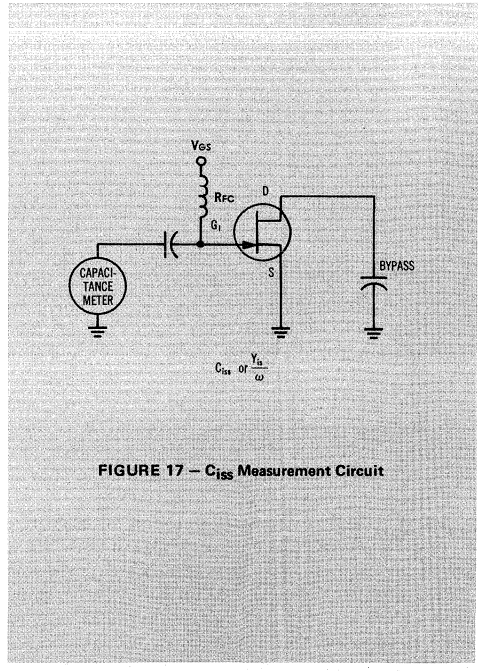


FIGURE 17 – C_{iss} Measurement Circuit

Again, for switching applications C_{rss} is a critical characteristic. Similar to the C_{ob} of a junction transistor, C_{rss} must be charged and discharged during the switching interval. For a chopper application, C_{rss} is the feedthrough capacitance for the chopper drive.

$C_{d(sub)}$ For the MOSFET, the drain-substrate junction capacitance becomes an important characteristic affecting the switching behavior. $C_{d(sub)}$ appears in parallel with the load in a switching circuit and must be charged and discharged between the two logic levels during the switching interval.

Noise Figure (NF) Like all other active components, field-effect transistors generate a certain amount of noise. The noise figure for field-effect transistors is normally specified on the data sheet as "spot noise", referring to the noise at a particular frequency. The noise figure will vary with frequency and also with the resistance at the input of the device. Typical graphs of such variations are illustrated in Figure 19 for the 2N5458. From graphs of this kind the designer can anticipate the noise level inherent in his design.

$r_{ds(on)}$ Channel resistance describes the bulk resistance of the channel in series with the drain and source. From an applications standpoint, it is important primarily for switching and chopper circuits since it affects the switching speed and determines the output level. To complete the confusion of multiple symbols for FET parameters, channel resistance is sometimes indicated as $r_{d(on)}$ and also as r_{DS} and r_{ds}. In either case, however, it is measured, for JFETs, by tying the gates to the source, setting all terminals equal to 0 Vdc, and applying an ac voltage from drain to source (see Figure 20). The magnitude of the ac voltage should be kept low so that there will be no pinch-off in the channel. Insulated-gate FETs may be measured with dc gate bias in the enhancement mode.

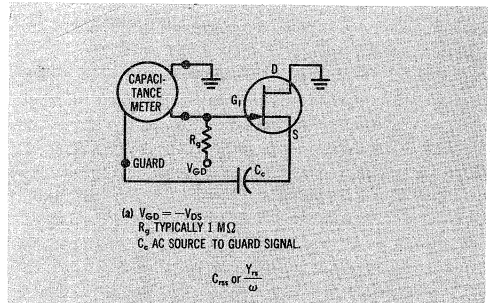


FIGURE 18 – Recommended C_{rss} Test Circuit

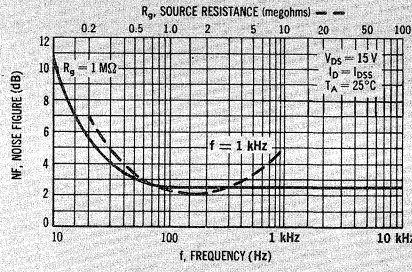


FIGURE 19 – Typical Variations of FET Noise Figure with Frequency and Source Resistance

APPLICATIONS

Device Selection

Obviously, different applications call for special emphasis on specific characteristics so that a simple figure of merit that compares devices for all potential uses would be hard to formulate. Nevertheless, an attempt to pinpoint the characteristics that are most significant for various applications has been made* to permit a rapid, first-order evaluation of competitive devices.

The most important single FET parameter, one that applies for any amplifier application, is y_{fs}. This parameter, or one of its many variations, is specified on most data

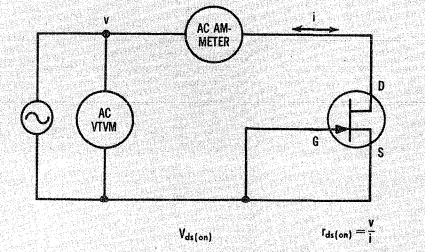


FIGURE 20 – Circuit for Measuring JFET Channel Resistance

*Christiansen, Donald, "Semiconductors: The New Figures of Merit," EEE, October, 1965.

sheets, yet some evaluation is required to come up with a reasonable comparison. For example, in the table of electrical characteristics on most JFET data sheets, y_{fs} is specified at I_{DSS} (V_{GS} = 0) where, for JFETs devices, y_{fs} is maximum. This is illustrated in Figure 14, where typical variations of y_{fs} as a function of I_D are plotted. For some small-signal applications, the I_{DSS} (V_{GS} = 0) point can actually be used as a dc operating point because small-signal excursions into the forward bias region will not actually cause the gate-source junction to become forward-biased. However, in most practical uses, some bias is necessary to allow for the anticipated signal swing; and it must be recognized the y_{fs} goes down as the bias is increased.

It is seen, also, that maximum y_{fs} increases as I_{DSS} increases so that, where maximum y_{fs} is important, a device with a high I_{DSS} specification is normally desirable.

On the other hand, where power dissipation is a factor to be considered, the figure of merit $y_{fs}/V_{GS(off)}$ I_{DSS} has been proposed. This term factors in not only I_{DSS}, which should be low if power dissipation is to be low, but also $V_{GS(off)}$, which indicates maximum input voltage swing. Since the signal peaks are represented by V_{GS} = $V_{GS(off)}$ and V_{GS} = 0, the lower $V_{GS(off)}$, the higher the figure of merit. And, for amplifier applications requiring a large signal swing, $V_{(BR)GSS}/V_{GS(off)}$ (assuming that $V_{GS(off)}$ is the "pinch-off" voltage) is a satisfactory merit figure because it indicates the ratio of maximum and minimum drain voltages.

For high-frequency circuits, the input capacitance (C_{iss}) and the Miller-effect capacitance (C_{rss}) become important, so $y_{fs}/(C_{iss} + C_{rss})$ indicates a relative measure of device performance. For switching and chopper circuits, a figure of merit is not often useful. Here the magnitudes of C_{iss}, C_{rss}, $C_{d(sub)}$ and r_{ds} are of primary interest.

Circuits

The types of circuits that can utilize FETs are practically unlimited. In fact, many circuits designed to utilize small-signal pentode tubes can utilize FETs with only minor modifications. For example, the circuit in Figure 21 shows a typical rf stage for a broadcast-band auto radio. In this circuit, a MPF102 n-channel JFET has replaced the 12BL6 pentode normally employed. The specifications for the two devices, including the AGC characteristics, are similar enough to perform adequately in the circuit of Figure 21.

In an audio application, a field-effect transistor such as the 2N5460 can be combined with a high voltage bipolar transistor to make a simple line-operated phonograph amplifier such as that shown in Figure 22. The ceramic pickup is connected through a potentiometer volume control to the field-effect transistor. Collector current of the transistor, in turn, is set by the potentiometer in the source of the FET. With the proper bipolar output transistor, the circuit can be driven directly from the rectified line voltage, while the low voltage for the FET can be derived from a voltage divider in the power supply line.

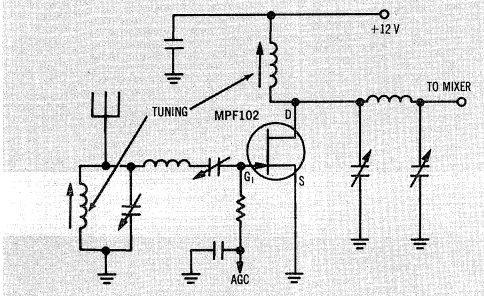


FIGURE 21 – RF Stage of Broadcast Auto Radio

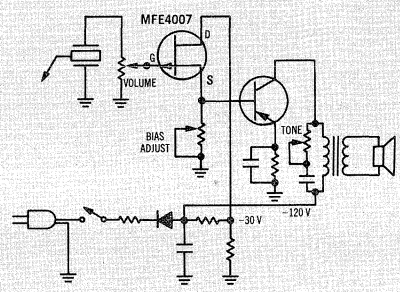


FIGURE 22 – Line Operated Phono Amplifiers

Figure 23 shows three basic chopper circuits. The advantage of the more complex series-shunt circuit (24c) is that it balances out the leakage currents of the FETs in order to reduce voltage error and is used to attain high chopping frequencies. From an applications standpoint, the FET circuit is superior to a junction transistor circuit in that there is no offset voltage with the FET turned on. On the minus side, however, the field-effect-transistor chopper generally has a higher series resistance ($r_{ds(on)}$) than the junction transistor.

As newer and better FETs are introduced and as a larger number of designers learn to use them, the range of applications of FETs should broaden considerably.

With its high input impedance, the field-effect transistor will play an important role in input circuitry for instrumentation and audio applications where low-impedance junction transistors have generally been least successful.

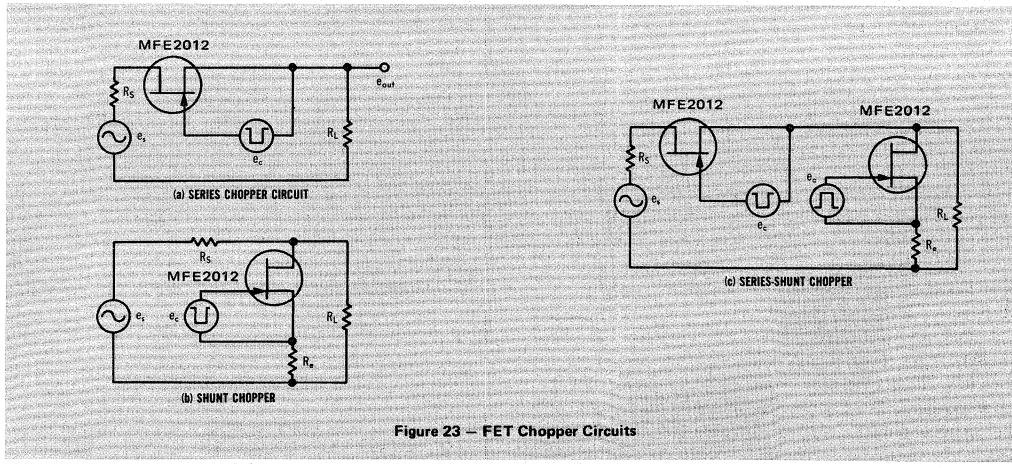


Figure 23 – FET Chopper Circuits

6

Circuit diagrams external to Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information in this Application Note has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

RF SMALL SIGNAL DESIGN USING TWO-PORT PARAMETERS

Prepared by:
Roy Hejhall

INTRODUCTION

Design of the solid-state, small-signal RF amplifier using two-port parameters is a systematic, mathematical procedure, with an exact solution (free from approximation) available for the complete design problem. The only sources of error in the final design are parameter variations resulting from transistor parameter distributions and strays in the physical circuit. Parameter distributions result from limits in measurement and random variations among identically designed transistors.

The purpose of this paper is to provide, in a single working reference, the important relationships necessary for the complete solution of the RF small-signal design problem using two-port parameters.

The major portion of the report presents design equations in terms of admittance parameters. A section on design with scattering parameters is also included.

This paper is based on work by Linvill[1], Stern[2], and others. Those who may wish to consider the derivations of some of the expressions should refer to the bibliography.

This report assumes that the reader is familiar with the two-port parameter method of describing a linear active network. Several references are available on this subject.[1,2,6,8,11,12]

It has also been assumed that a suitable transistor or other active device for the task at hand has been selected, and that two-port parameters are available for the frequency and bias point which will be used. Device selection will not be covered as a separate topic in this report; rather, a thorough understanding of the material in the report should provide the designer with the tools he needs to select transistors for a particular small-signal application.

The equations given in the text of this report are applicable to the common-emitter, common-base, or common-collector configuration, if the applicable set of parameters (common-emitter, common-base, or common-collector parameters) is used. Equations for the conversion of the admittance or hybrid parameters of any configuration to either of the other two configurations of the same parameter set are given in the appendix.

While directed primarily toward circuit design with conventional bipolar transistors, two-port network theory has the advantage of being applicable to any linear active network (LAN). The same design approach and equations may therefore be used with field effect transistors[7,9], integrated circuits[10], or any other device which may be described as a linear active two-port network.

Finally, various parameter interrelationships and other data are given in the Appendix.

GENERAL DESIGN CONSIDERATIONS

Design of the RF small-signal tuned amplifier is usually based on a requirement for a specified power gain at a given frequency. Other design goals may include bandwidth, stability, input-output isolation, and low noise performance. After a basic circuit type is selected, the applicable design equations can be solved.

Circuits may be categorized according to feedback (neutralization, unilateralization, or no feedback), and matching at transistor terminals (circuit admittances either matched or mismatched to transistor input and output admittances). Each of these circuit categories will be discussed, including the applicable design equations and the considerations leading to the selection of a particular configuration.

STABILITY

A major factor in the overall design is the potential stability of the transistor. This may be determined by computing the Linvill stability factor[1] C using the following expression:†

$$C = \frac{|y_{12}\, y_{21}|}{2g_{11}\, g_{22} - \mathrm{Re}\,(y_{12}y_{21})} \qquad (1)$$

When C is less than 1, the transistor is unconditionally stable. When C is greater than 1, the transistor is potentially unstable.

The C factor is a test for stability under a hypothetical worst case condition; that is, with both input and output transistor terminals open circuited. With no external feedback, an unconditionally stable transistor will not oscillate with any combination of source and load. If a transistor is potentially unstable, certain source and load combinations will produce oscillations.

Although the C factor may be used to determine the potential stability of a transistor, the conditions of open circuited source and load which are assumed in the C factor test are not applicable to a practical amplifier.

†Re ($Y_{12}Y_{21}$) = Real part of ($Y_{12}Y_{21}$)

Consequently it is also desirable to compute the relative stability of actual amplifier circuits, and Stern[2] has defined a stability factor k for this purpose. The k factor is similar to the C factor except that it also takes into account finite source and load admittances connected to the transistor. The expression for k is:

$$k = \frac{2\,(g_{11} + G_s)\,(g_{22} + G_L)}{\left|y_{12}y_{21}\right| + \mathrm{Re}\,(y_{12}y_{21})} \qquad (2)$$

If k is greater than one, the circuit will be stable. If k is less than one, the circuit will be potentially unstable and will very likely oscillate at some frequency.

Note that the C factor simply predicts potential stability of a transistor with an open circuited source and load, while the k factor provides a stability computation for a specific circuit.

Stability considerations will be discussed further in the descriptions of each basic circuit type to follow.

GENERAL DESIGN EQUATIONS

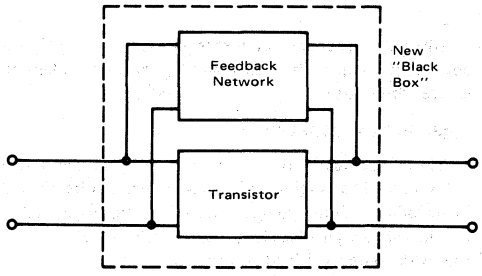
There are a number of design equations which are applicable to most types of amplifiers. These equations will be discussed first. Descriptions of specific amplifier types will then follow, and each will contain additional design equations applicable to that particular amplifier.

POWER GAIN

The general expression for power gain is:

$$G = \frac{\left|y_{21}\right|^2 \mathrm{Re}\,(Y_L)}{\left|Y_L + y_{22}\right|^2 \mathrm{Re}\left(y_{11} - \frac{y_{12}y_{21}}{y_{22} + Y_L}\right)} \qquad (3)$$

Equation 3 applies to circuits with no external feedback. It can also be used with circuits which have external feedback if the composite y parameters of both the transistor and the feedback network are substituted for the transistor y parameters in the equation. The composite y parameters are determined by considering the transistor and the feedback network to be two "black boxes" in parallel:



For example, the above combination of transistor and feedback network may be characterized as a single "black box" by the following equations:†

$$\begin{aligned} y_{11c} &= y_{11t} + y_{11f} \\ y_{12c} &= y_{12t} + y_{12f} \\ y_{21c} &= y_{21t} + y_{21f} \\ y_{22c} &= y_{22t} + y_{22f} \end{aligned} \qquad (4)$$

Where:

$y_{11c}, y_{12c}, y_{21c}, y_{22c}$ are the composite y parameters of the parallel combination of transistor and feedback network.

$y_{11t}, y_{12t}, y_{21t}, y_{22t}$ are the y parameters of the transistor.

$y_{11f}, y_{12f}, y_{21f}, y_{22f}$ are the y parameters of the feedback network.

Note that, since this approach treats the transistor and feedback network combination as a single "black box" with $y_{11c}, y_{12c}, y_{21c}$, and y_{22c} as its y parameters, the composite y parameters may therefore be substituted in any of the design equations applicable to a linear, active two-port analysis.

The neutralized and unilateralized amplifiers are special cases of this general concept, and equations associated with those special cases will be given later.

Equation 3 provides a solution for power gain of the linear active network (transistor) only. Input and output networks are considered to be part of the source and load, respectively. Two important points should therefore be kept in mind:

(1) Power gain computed from equation 3 will not take into account network losses. Input network loss reduces power delivered to the transistor. Power lost in the output network is computed as useful power output, since the load admittance Y_L is the combination of the output network and its load.

(2) Power gain is independent of source admittance. An input mismatch results in less input power being delivered to the transistor. Accordingly, note that equation 3 does not contain the term Y_S.

The power gain of a transistor together with its associated input and output networks may be computed by measuring the input and output network losses, and subtracting them from the power gain computed with equation 3.

In some cases it may be desirable to include the effects of input matching in power gain computations. A convenient term is transducer gain G_T, defined as output power delivered to a load by the transistor, divided by the

†Refer to Seshu and Balabanian, "Linear Network Analysis," John Wiley and Sons, 1959, P321

maximum input power available from the source.

The equation for transducer gain is:

$$G_T = \frac{4\ \mathrm{Re}\ (Y_s)\ \mathrm{Re}\ (Y_t)\ |y_{21}|^2}{|(y_{11} + Y_s)\ (y_{22} + Y_L) - y_{12}y_{21}|^2} \qquad (5)$$

In this equation, Y_L is the composite transistor load admittance-composed of both output network and its load, and Y_S is the composite transistor source admittance composed of both input network and its source. Therefore, transducer gain includes the effects of the degree of admittance match at the transistor input terminals but does not take into account input and output network losses.

As in equation 3, the composite y parameters of a transistor feedback network combination may be substituted for the transistor y parameters when such a combination is used.

The Maximum Available Gain MAG is an often used transistor figure-of-merit. The MAG is the theoretical power gain of a transistor with its reverse transfer admittance y_{12} set equal to zero, and its source and load admittances conjugately matched to y_{11} and y_{22}, respectively.

If $y_{12} = 0$, the transistor exhibits an input admittance equal to y_{11} and an output admittance equal to y_{22}.† The equation for MAG is, therefore, obtained by solving the general power gain expression, equation 3, with the conditions

$$y_{12} = 0$$

$$y_L = y_{22}^*$$

$$\text{and } y_s = y_{11}^*$$

where * denotes conjugate

which yields:

$$\mathrm{MAG} = \frac{|y_{21}|^2}{4\ \mathrm{Re}\ (y_{11})\ \mathrm{Re}\ (y_{22})} \qquad (6)$$

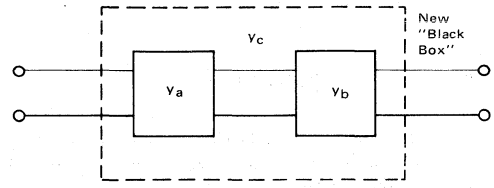
MAG is a figure of merit only, since it is physically impossible to reduce y_{12} to zero without changing the other parameters of the transistor. An external feedback network may be used to achieve a composite y_{12} of zero, but then the other composite parameters will also be modified according to the relationships given in the discussion of the composite transistor – feedback network "black box."

†Obtained by solving the equations for transistor Y_{IN} and Y_{OUT} with y_{12} equal to zero. These equations are given later in the report.

CASCADED LAN'S

Design calculations for cascaded LAN's may be performed by first computing composite two-port parameters as was done in the case of the parallel LAN's.

For the following cascaded LAN's



The composite y parameters are:

$$y_{11c} = y_{11a} - \frac{y_{12a}\,y_{21a}}{y_{22a} + y_{11b}}$$

$$y_{22c} = y_{22b} - \frac{y_{12b}\,y_{21b}}{y_{22a} + y_{11b}} \qquad (7)$$

$$y_{21c} = -\frac{y_{21a}\,y_{21b}}{y_{22a} + y_{11b}}$$

$$y_{12c} = -\frac{y_{12a}\,y_{12b}}{y_{22a} + y_{11b}}$$

where y_{11c}, y_{22c}, y_{21c}, y_{12c} are the composite y parameters of the cascaded LAN's.

TRANSISTOR INPUT AND OUTPUT ADMITTANCES

The expression for the input admittance of a transistor is:

$$Y_{IN} = y_{11} - \frac{y_{12}\,y_{21}}{y_{22} + Y_L} \qquad (8)$$

The expression for the output admittance of a transistor is:

$$Y_{OUT} = y_{22} - \frac{y_{12}\,y_{21}}{y_{11} + Y_s} \qquad (9)$$

When the feedback parameter y_{12} is not zero, Y_{IN} is dependent on load admittance and Y_{OUT} is dependent on source admittance.

AMPLIFIER STABILITY

One of the major considerations in RF amplifier design is stability. The stability of a final design can be assured by including stability computations and considering stability in all design decisions relating to feedback and transistor source and load admittances.

The potential stability of the transistor should first be computed using equation 1.

The various alternatives concerning input – output matching and neutralization – unilateralization will now be discussed for both the unconditionally stable transistor and the potentially unstable transistor.

THE UNCONDITIONALLY STABLE TRANSISTOR

When the Linvill stability factor of the transistor as determined by equation 1 is less than one, the transistor is unconditionally stable. Oscillations will not occur using any combination of source and load admittances without external feedback. Stability is therefore eliminated as a factor in the remainder of the design, and complete freedom is possible with regard to matching and neutralization to optimize the amplifier for other performance requirements.

AMPLIFIERS WITHOUT FEEDBACK

The amplifier with no feedback is a logical choice for the unconditionally stable transistor in many applications since it may offer the advantages of fewer components and a simple tuning procedure.

Source and load admittances may be selected for maximum gain and/or any number of other requirements. Power gain and transducer gain may be computed using equations 3 and 5, respectively; input and output admittances may be computed using equations 8 and 9, respectively.

The amplifier stability factor may be computed using equation 2. While amplifier stability was assured from the beginning by the use of an unconditionally stable transistor, the designer may still wish to perform this computation to provide some insight into danger of instability under adverse environmental conditions, source and load variations, etc.

G_{max}

G_{max}, the highest transducer gain possible without external feedback, forms a special case of the no feedback amplifier.

The source and load admittances required to achieve G_{max} may be computed from the following:

$$G_S = \frac{1}{2\ \mathrm{Re}(y_{22})} \left\{ \left[2\ \mathrm{Re}(y_{11})\ \mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}y_{21}) \right]^2 - \left| y_{12}y_{21} \right|^2 \right\}^{\frac{1}{2}} \quad (10)$$

$$B_S = -\ \mathrm{Im}(y_{11}) + \frac{\mathrm{Im}(y_{21}y_{12})}{2\ \mathrm{Re}(y_{22})} \quad (11)$$

$$G_L = \frac{1}{2\ \mathrm{Re}(y_{11})} \left\{ \left[2\ \mathrm{Re}(y_{11})\ \mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}y_{21}) \right]^2 - \left| y_{12}y_{21} \right|^2 \right\}^{\frac{1}{2}} \quad (12)$$

$$B_L = -\ \mathrm{Im}(y_{22}) + \frac{\mathrm{Im}(y_{21}y_{12})}{2\ \mathrm{Re}(y_{11})} \quad (13)$$

Therefore, if the maximum possible power gain without feedback is desired for an amplifier, equations 10, 11 12, and 13 are used to compute Y_S and Y_L.

The magnitude of G_{max} may be computed from the following expressions:

$$G_{max} = \frac{\left| y_{21} \right|^2}{2\ \mathrm{Re}(y_{11})\ \mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}y_{21}) + \left\{ \left| 2\ \mathrm{Re}(y_{11})\ \mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}y_{21}) \right|^2 - \left| y_{12}y_{21} \right|^2 \right\}^{\frac{1}{2}}} \quad (14)$$

Equations 10, 11, 12, and 13 can be obtained by differentiating equation 5 with respect to G_S, B_S, G_L, and B_L, and setting the four derivatives equal to zero. The G_S, B_S, G_L, and B_L thus computed can then be substituted in equation 5 to obtain the expression for G_{max}, equation 14.

THE LINVILL METHOD

The amplifier without feedback design problem may also be solved graphically using a technique developed by J. G. Linvill.† Linvill's technique is very useful for a certain class of problems. Since it is so fully discussed in many good references, we will not go into it further here. An advantage of the Linvill technique is that it provides a reasonably rapid graphic solution relating gain, bandwidth, and stability. A disadvantage is its scope of usefulness, since the standard Linvill solution applies only to an amplifier with no external feedback and the Y_S conjugately matched to the transistor input admittance, Y_{IN}.

THE UNILATERALIZED AMPLIFIER

Unilateralization consists of employing an external feedback network to achieve a composite y_{12} of zero.

While unilateralization is perhaps most often used to achieve stability with a potentially unstable transistor, other circuit considerations may also warrant the use of unilateralization with the unconditionally stable transistor. For example, the input-output isolation afforded by unilateralization may be desirable in a particular design.

Design equations for the unilateralized case are obtained by first computing the composite y parameters of the transistor – feedback network combination and then substituting the composite parameters in the general equations.

Referring to the discussion on composite y parameters and setting up the basic condition that y_{12c} must equal zero, the other composite y parameters can be computed. Assuming that a passive feedback network is being used, then

$$y_{11f} = y_{22f} = -y_{12f} = -y_{21f},$$

$$\text{and since } y_{12c} = 0,\ y_{12t} + y_{12f} = 0$$

$$\text{then } y_{12t} = -y_{12f},$$

$$\text{and } y_{12t} = -y_{12f} = y_{11f} = y_{22f} = -y_{21f}$$

†Application Note AN166 Motorola Semiconductor Products, Inc. Dept. TIC, 5005 E. McDowell Road, Phoenix, Arizona. See also reference 5 in the bibliography.

6

Substituting the above results in equations 4 yields the following:

$$y_{11c} = y_{11t} + y_{12t}$$

$$y_{22c} = y_{22t} + y_{12t}$$

$$y_{12c} = y_{12t} - y_{12t} = 0$$

$$y_{21c} = y_{21t} - y_{12t}$$

Substituting these complete y parameters in equations 8, 9, 3, 7, and 5 respectively, yields equations 15, 16, 17 18, and 19 respectively for the unilateralized case.

Unilateralized input admittance

$$Y_{IN} = y_{11} + y_{12} \qquad (15)$$

Unilateralized output admittance

$$Y_{OUT} = y_{22} + y_{12} \qquad (16)$$

Unilateralized power gain, general expression:

$$G_{PU} = \frac{\left|y_{21} - y_{12}\right|^2 \, Re\,(Y_L)}{\left|Y_L + y_{22} + y_{12}\right|^2 \, Re(y_{11})} \qquad (17)$$

Unilateralized power gain with Y_L conjugately matched to Y_{OUT}:

$$G_U = \frac{\left|y_{21} - y_{12}\right|^2}{4\,Re(y_{11} + y_{12})\,Re(y_{22} + y_{12})} \qquad (18)$$

Unilateralized transducer gain:

$$G_{TU} = \frac{4\,Re(Y_S)\,Re(Y_L)\,\left|y_{21} - y_{12}\right|^2}{\left|(y_{11} + y_{12} + Y_S)\,(y_{22} + y_{12} + Y_L)\right|^2} \qquad (19)$$

Note that equations 15, 16, 17, 18 and 19, are given entirely in terms of the transistor y parameters, not those of the feedback network or the composite.

Another benefit of unilateralization is input – output isolation. As can be seen in equations 15 and 16, Y_{IN} is completely independent of Y_L, and Y_{OUT} is similarly independent of Y_S. In a practical sense, this means that in a single or multi-stage amplifier using unilateralized stages, tuning of any one network will not affect tuning in other parts of the circuit. Thus, the troublesome task of having to re-peak an entire amplifier following a change in tuning at a single point can be eliminated.

NEUTRALIZATION

Neutralization consists of employing a feedback network to reduce y_{12} to some value other than zero. Neutralization is generally used for the same purposes as unilateralization, but provides something less than the ideal cancellation of the transistor feedback parameter which unilateralization achieves. A typical example of neutralization might be a feedback network which provides a composite b_{12} of zero while having only a negligible effect on the transistor g_{12}.

The equations for a particular neutralized case would be developed in the same manner as those for the unilateralized case. Since there are an infinite number of possibilities, no specific equations will be given here.

This completes the discussion of design with the unconditionally stable transistor. The potentially unstable transistor will now be considered.

THE POTENTIALLY UNSTABLE TRANSISTOR

When the Linvill stability factor of the transistor as determined by equation 1 is greater than one, the transistor is potentially unstable. Certain combinations of source and load admittances will cause oscillations if no feedback is used. In designing with the potentially unstable transistor, steps must be taken to insure that the amplifier will be stable.

Stability is usually achieved by one or both of two methods:

(1) Using a feedback network which reduces the composite y_{12} to a value which insures stability.

(2) Choosing a source and load admittance combination which provides stability.

A discussion of these basic methods is given below.

USING FEEDBACK TO ACHIEVE STABILITY

Either unilateralization or neutralization may be used to achieve stability. If unilateralization is used, the transistor-feedback network combination will be unconditionally stable. This may be verified by computing the Linvill stability factor of the combination. Since $y_{12c} = 0$, the numerator in equation 1 would be zero.

With stability thus assured, the remainder of the design may then be done to satisfy other requirements placed on the amplifier. After unilateralization has converted the potentially unstable transistor to an unconditionally stable combination, all other aspects of the design are identical to the unilateralized case with the unconditionally stable transistor. Power gains and input and output admittances may be computed using equations 15 through 19.

If neutralization is used to achieve stability, the Linvill stability factor can be used to compute the potential stability of any transistor – neutralization network combination. Since in this case $y_{12c} \neq 0$, C will have a value other than zero.

After unconditional stability of the transistor-neutralization network combination has been achieved, the design may then be completed by treating the combination as an unconditionally stable transistor, and proceeding with the case of the unconditionally stable transistor in an amplifier without feedback. Power gains, input and output admittances, and the circuit stability factor may be computed by using the composite parameters of the combination in equations 2, 3, 5, 8, and 9.

STABILITY WITHOUT FEEDBACK

A stable design with the potentially unstable transistor is possible without external feedback by proper choice of

souce and load admittances. This can be seen by inspection of equation 2; G_S and/or G_L can be made large enough to yield a stable circuit regardless of the degree of potential instability of the transistor.

This suggests a relatively simple way to achieve a stable design with a potentially unstable transistor. A circuit stability factor k is selected, and equation 2 is used to arrive at values of G_S and G_L which will provide the desired k. In achieving a particular circuit stability factor, the designer may choose any of the following combinations of matching or mismatching of G_S and G_L to the transistor input and output conductances, respectively:

(1) G_S matched and G_L mismatched
(2) G_L matched and G_S mismatched
(3) Both G_S and G_L mismatched

Often a decision on which combination to use will be dictated by other performance requirements or practical considerations.

Once G_S and G_L have been chosen, the remainder of the design may be completed using the relationships which apply to the amplifier without feedback. Power gain and input and output admittances may be computed using equations 3, 5, 8, and 9.

Although the above procedure may be adequate in many cases, a more systematic method of source and load admittance determination is desirable for designs which demand maximum power gain per degree of circuit stability. Stern has analyzed this problem and developed equations for computing the conductance and susceptance of both Y_S and Y_L for maximum power gain for a particular circuit stability factor.[2,4] These equations are given here:

$$G_s = \sqrt{\frac{k\left[\left|y_{12}y_{21}\right| + \mathrm{Re}(y_{12}y_{21})\right]}{2}} \cdot \sqrt{\frac{g_{11}}{g_{22}}} - g_{11} \tag{20}$$

$$G_L = \sqrt{\frac{k\left[\left|y_{12}y_{21}\right| + \mathrm{Re}(y_{12}y_{21})\right]}{2}} \cdot \sqrt{\frac{g_{22}}{g_{11}}} - g_{22} \tag{21}$$

$$B_s = \frac{(G_s + g_{11})\ Z_o}{\sqrt{k\left[\left|y_{12}y_{21}\right| + \mathrm{Re}(y_{12}y_{21})\right]}} - b_{11} \tag{22}$$

$$B_L = \frac{(G_L + g_{22})\ Z_o}{\sqrt{k\left[\left|y_{12}y_{21}\right| + \mathrm{Re}(y_{12}y_{21})\right]}} - b_{22} \tag{23}$$

Where,

$$Z = \frac{(B_s + b_{11})(G_L + g_{22}) + (B_L + b_{22})\,k(L + M)/2(G_L + g_{22})}{\sqrt{k\ (L + M)}} \tag{24}$$

$$L = \left|y_{12}y_{21}\right| \tag{25}$$

$$M = \mathrm{Re}(y_{12}y_{21}) \tag{26}$$

Defining D as the demoninator in equation 5 yields:

$$D = \frac{Z^4}{4} + \frac{\left[k(L + M) + 2M\right] Z^2}{2} - 2NZ\sqrt{k(L + M)} + A^2 + N^2 \tag{27}$$

where,

$$A = \frac{k(L + M)}{2} - M, \tag{28}$$

$$N = \mathrm{Im}(y_{12}y_{21}), \tag{29}$$

and,

Z_O = that real value of Z which results in the smallest minimum of D, found by setting,

$$\frac{dD}{dZ} = Z^3 + \left[k(L + M) + 2M\right] Z - 2N\sqrt{k(L + M)} \tag{30}$$

equal to zero.

Computation of Y_S and Y_L using equations 20 through 30 is a bit tedious to be done very frequently, and this may have discouraged wide usage of the complete Stern solution. However, examination of Stern's work suggests some interesting shortcuts:

(A) COMPUTATION OF G_S AND G_L ONLY, USING EQUATIONS 20 AND 21. If a value equal to $-b_{22}$ is then chosen for B_L, the resulting Y_L will be very close to the true Y_L for maximum gain. The transistor Y_{IN} can then be computed from Y_L using equation 8, and B_S can be set equal to $-\mathrm{Im}(Y_{IN})$.

Computation of B_S and B_L comprise by far the more complex portion of the Stern solution. This alternate method therefore permits the designer to closely approximate the exact Stern solution for Y_S and Y_L while avoiding that portion of the computations which are the most complex and time consuming. Further, the circuit can be designed with tuning adjustments for varying B_S and B_L, thereby creating the possibility of experimentally achieving the true B_S and B_L for maximum gain as accurately as if all the Stern equations had been solved.

(B) MISMATCHING G_S TO g_{11} AND G_L TO g_{22} BY AN EQUAL RATIO YIELDS A TRUE STERN SOLUTION FOR G_S AND G_L. This can be derived from equations 20 and 21, which lead to the following result:

$$\frac{G_L}{g_{22}} = \frac{G_s}{g_{11}} \tag{31}$$

If a mismatch ratio, R, is defined as follows,

$$R = \frac{\frac{G_L}{g_{22}}}{\frac{G_s}{g_{11}}} \tag{32}$$

then R may be computed for any particular circuit stability factor using the equation:

$$(1 + R)^2 = k\left[\frac{\left|y_{21}y_{12}\right| + \mathrm{Re}(y_{12}y_{21})}{2\ g_{11}\ g_{22}}\right] \tag{33}$$

Equation 33 was derived from equation 2 and 32. Having thus determined R, G_S and G_L can be quickly found using equation 32.

B_S and B_L can then be determined in the

manner described above in alternate method (A).

This alternate method may be advantageous if source and load admittances and power gains for several different values of k are desired. Once the R for a particular k has been determined, the R for any other k may be quickly found from the equation

$$\frac{(1 + R_1)^2}{(1 + R_2)^2} = \frac{k_1}{k_2} \tag{34}$$

where R_1 and R_2 are values of R corresponding to k_1 and k_2, respectively.

(C) COMPUTER DESIGN. The complete Stern design problem may be programmed into a computer. Power gain, circuit stability factor, Y_S and Y_L can be obtained from the computer for any value of k. MAG, G_U, and the Linvill stability factor of the transistor may also be included in the program.

After employing either the complete Stern solution or an alternate method to obtain Y_S and Y_L for the potentially unstable transistor in an amplifier without feedback, power gains and input and output admittances may be obtained using equations 3, 5, 8, and 9.

SENSITIVITY

In all but the unilateralized amplifier, Y_{IN} is a function of load admittance. Thus Y_{IN} changes with output circuit tuning, and this can be troublesome. Consequently, it is sometimes desirable to compute the extent of variation of Y_{IN} with changes in Y_L. A term, sensitivity δ, has been defined to provide a measure of this characteristic, and is equal to per cent change in Y_{IN} divided by per cent change in Y_L. The equation for sensitivity is:

$$\delta = \left|\frac{Y_L}{y_{22} + Y_L}\right| \cdot \left|\frac{g_{11}}{y_{11}}\right| \cdot \frac{K}{\left|\frac{y_{22} + Y_L}{g_{22}} + \frac{g_{11}}{y_{11}} K e^{j\Theta}\right|} \tag{35}$$

where,

$$K = \left|\frac{y_{21}\, y_{12}}{g_{11}\, g_{22}}\right|$$

$$\Theta = \arg(-y_{12}y_{21}) *$$

$$K e^{j\Theta} = K(\cos\Theta + j \sin\Theta)$$

A more complete discussion of sensitivity is given in reference 6.

DESIGN WITH SCATTERING PARAMETERS

Scattering, or s parameters have greatly increased in popularity since the late 1960's, largely due to the appearance of sophisticated new equipment for performing s parameter measurements.

A summary of s parameter design equations is given below.

Power gain:

$$G = \frac{|S_{21}|^2 (1 - |\Gamma_L|^2)}{(1 - |S_{11}|^2) + |\Gamma_L|^2 (|S_{22}|^2 - |\Delta S|^2) - 2\,\mathrm{Re}(\Gamma_L N)} \tag{36}$$

$$\Delta S = S_{11}S_{22} - S_{12}S_{21}$$

$$N = S_{22} - D S^*_{11}$$

Transducer gain:

$$G_T = \frac{|S_{21}|^2 (1 - |\Gamma_S|^2)(1 - |\Gamma_L|^2)}{|(1 - S_{11}\Gamma_S)(1 - S_{22}\Gamma_L) - S_{12}S_{21}\Gamma_L\Gamma_S|^2} \tag{37}$$

Input reflection coefficient:

$$S'_{11} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{38}$$

Output reflection coefficient:

$$S'_{22} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \tag{39}$$

Linvill stability factor:

$$C = K^{-1}$$

$$K = \frac{1 + |\Delta S|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}S_{21}|} \tag{40}$$

$$\Delta S = S_{11}S_{22} - S_{12}S_{21}$$

Equation 40 which gives K, the reciprocal of C, is presented in this form because it is the s parameter stability expression most often seen in the literature. K in equation 40 must not be confused with Stern stability factor k given in equation 2.

Maximum unneutralized transducer gain, unconditionally stable LAN:

$$G_{max} = \left|\frac{S_{21}}{S_{12}}(K \pm \sqrt{K^2 - 1})\right| \tag{41}$$

$$K = C^{-1}$$

C = Linvill Stability Factor

Source and load reflection coefficients for a conjugate match of the unconditionally stable LAN in an amplifier without feedback:

$$\Gamma_{mS} = M^* \left[\frac{B_1 \pm \sqrt{B_1^2 - 4|M|^2}}{2|M|^2}\right] \tag{42}$$

$$\Gamma_{mL} = N^* \left[\frac{B_2 \pm \sqrt{B_2^2 - 4|N|^2}}{2|N|^2}\right] \tag{43}$$

Where $B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta S|^2$

$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta S|^2$

$M = S_{11} - (\Delta S)(S_{22}^*)$

$N = S_{22} - (\Delta S)(S_{11}^*)$

A more comprehensive treatment of amplifier design with s parameters is given in references 8, 11, and 12.

One cautionary note is in order.

Several papers have been published on the subject of simplifying the s parameter design procedure by making the assumption that the reverse transfer parameter, s_{12}, is equal to zero. This procedure totally ignores the entire

problem of amplifier stability.

Modern high gain solid-state RF devices will readily oscillate under a wide variety of circuit conditions. Stability problems are encountered even with extremely low feedback devices such as Linear IC's and dual gate MOSFETS. Therefore, amplifier design calculations which do not include device and circuit feedback are only an approximation which will yield either an inaccurate solution or possibly even an oscillator when the design is tested in the laboratory. Reference 13 provides more detail on the shortcomings of this procedure, including an amplifier design example which did turn out to be an oscillator.

SUMMARY OF DESIGN PROCEDURE

A summary of the amplifier design procedure using two-port parameters is given below.

1. Determine the potential instability of the active device.
2. If the device is not unconditionally stable, decide on a course of action to insure circuit stability.
3. Determine whether or not feedback is to be used.
4. Determine source and load admittances.
5. Design appropriate networks to provide the desired source and load admittances.

Stability (Steps 1 and 2 above)

A stability computation for the worst case conditions of open circuit source and load is provided by Linvill's stability factor C. If the C factor indicates unconditional stability, no combination of passive terminations can cause oscillations.

Stability calculations should include the total feedback of the amplifier. In the case of extremely low feedback devices such as dual gate MOSFET's and Linear IC's, external circuit feedback often eclipses the internal device feedback. In such a case, the designer should measure the external circuit feedback and include it in the design calculations. To accomplish this, see the earlier section of this note on the composite parameters of two-port LAN's in parallel.

If the device is unconditionally stable, the design may proceed to fulfill other objectives without fear of oscillations. If the device is potentially unstable, steps must be taken to prevent oscillations in the final design. Stability is achieved by proper selection of source and load admittances, by the use of feedback, or both.

Feedback (Step 3)

Feedback may be employed in the tuned high frequency amplifier to achieve stability, input-output isolation, or to alter the gain and terminal admittances of the active device. A decision to employ feedback would be based on whether or not its use was the optimum way to accomplish one of the foregoing objectives in a particular application.

If feedback is employed, the device parameters may be modified to include the feedback network in accordance with standard two-port network theory. The remainder of the design may then proceed by treating the transistor-feedback network combination as a single, new two-port linear active network.

Source and Load Admittances (Step 4)

Source and load admittance determination is dependent upon gain and stability considerations, together with practical circuit limitations.

If the device is either unconditionally stable itself or has been made stable with feedback, stability need not be a major factor in the determination of source and load. If the device is potentially unstable and feedback is not employed, then a source and load which will guarantee a certain degree of circuit stability must be used. Also, it is a good idea to check the circuit stability factor during this step even when an unconditionally stable device is used.

Finally, practical limitations in matching networks and components may also play an important part of source and load admittance determination.

Network Design (Step 5)

The final step consists of network synthesis to achieve the desired source and load admittances computed in step 4.

Sometimes, it will be difficult to achieve a desired source and load due to tuning range limitations, excess network losses, component limitations, etc. In such cases, the source and load admittances will be a compromise between desired performance and practical limitations.

SUMMARY

The small signal amplifier performance of a transistor is completely described by two-port admittance parameters. Based on these parameters, equations for computing the stability, gain, and optimum source and load admittances for the unilateralized, neutralized, and no-feedback amplifier cases have been discussed.

The unconditionally stable transistor will not oscillate with any combination of source and load admittances, and circuits using a stable transistor may be optimized for other performance requirements without fear of oscillations.

The potentially unstable transistor requires that steps be taken to guarantee a stable design. Stability is usually achieved by unilateralization, neutralization, or selection of source and load admittances which result in a stable amplifier.

Unilateralization and neutralization reduce the composite reverse transfer admittance. They may be used to achieve stability, input – output isolation, or both.

Maximum power gain per degree of circuit stability without feedback may be achieved using Stern's equations.

The degree of input – output isolation is described by the term sensitivity, which makes it possible to compute changes in input admittance for any change in load admittance.

The theory and design equations in this report are applicable to any linear active device which may be characterized as a two-port network. Therefore, the term "transistor" used herein refers generally to all such devices, including FETs and integrated circuits.

BIBLIOGRAPHY

1. "Transistors and Active Circuits," by Linvill and Gibbons, McGraw-Hill, 1961.
2. "Stability and Power Gain of Tuned Transistor Amplifiers," by Arthur P. Stern, Proc. IRE, March, 1957.
3. "Using Linvill Techniques for R. F. Amplifiers," Motorola Semiconductor Products, Inc., Application Note 166.
4. "High-Gain, High-Frequency Amplifiers," by Peter M. Norris, Electro-Technology, January, 1966.
5. "Linvill Technique Speeds High Frequency Amplifier Design," by John Lauchner and Marvin Silverstein, Electronic Design, April, 12, 1966.
6. "The Design of Alignable Transistor Amplifiers," by J. F. Gibbons, Stanford University Technical Report No. 106, May 7, 1956.
7. "Field Effect Transistor R. F. Amplifier Design Techniques," Motorola Semiconductor Products Inc., Application Note 423.
8. "Circuit Design and Characterization of Transistors by Means of Three-Part Scattering Parameters" by George E. Bodway, the Microwave Journal, May, 1968.
9. "Small-Signal RF Design with Dual-Gate MOSFET's" Motorola Semiconductor Products, Inc. Application Note 478A.
10. "A High Gain Integrated Circuit RF-IF Amplifier with Wide Range AGC", Motorola Semiconductor Products, Inc. Application Note 513.
11. "S Parameter Design", Hewlett-Packard Company, Palo Alto, California, Application Note 154.
12. "S Parameters", Hewlett-Packard Company, Palo Alto, California, Application Note 95.
13. "Staying Stable with S Parameters", by Roy Hejhall, Motorola Monitor, Vol. 7, No. 2.

GLOSSARY

- C = Linvill's stability factor
- k = Stern's stability factor
- G_S = Real part of the source admittance
- G_L = Real part of the load admittance
- B_S = Imaginary part of the source admittance
- B_L = Imaginary part of the load admittance
- g_{11} = Real part of y_{11}
- g_{22} = Real part of y_{22}
- G = Generalized power gain
- Y_L = Complex load admittance
- Y_S = Complex source admittance
- G_T = Transducer gain
- MAG = Maximum available gain
- $*$ = Conjugate
- Y_{IN} = Input admittance
- Y_{OUT} = Output admittance
- G_{max} = Maximum gain without feedback
- G_U = Unilateralized gain
- G_{TU} = Unilateralized transducer gain
- δ = Sensitivity
- s'_{11} = Input reflection coefficient
- s'_{22} = Output reflection coefficient
- Γ_L = Load reflection coefficient
- Γ_S = Source reflection coefficient
- K = Scattering parameter stability factor

APPENDIX I

A. Conversions among parameter types for y, z, h, and g parameters.

h to y

$$y_{11} = \frac{1}{h_{11}} \qquad y_{12} = \frac{-h_{12}}{h_{11}} \qquad y_{21} = \frac{h_{21}}{h_{11}} \qquad y_{22} = \frac{\Delta h}{h_{11}}$$

where $\Delta h = h_{11} h_{22} - h_{12} h_{21}$

y to h

$$h_{11} = \frac{1}{y_{11}} \qquad h_{12} = \frac{-y_{12}}{y_{11}} \qquad h_{21} = \frac{y_{21}}{y_{11}} \qquad h_{22} = \frac{\Delta y}{y_{11}}$$

where $\Delta y = y_{11} y_{22} - y_{12} y_{21}$

h to z

$$z_{11} = \frac{\Delta h}{h_{22}} \qquad z_{12} = \frac{h_{12}}{h_{22}} \qquad z_{21} = \frac{-h_{21}}{h_{22}} \qquad z_{22} = \frac{1}{h_{22}}$$

z to h

$$h_{11} = \frac{\Delta z}{z_{22}} \qquad h_{12} = \frac{z_{12}}{z_{22}} \qquad h_{21} = \frac{-z_{21}}{z_{22}} \qquad h_{22} = \frac{1}{z_{22}}$$

where $\Delta z = z_{11} z_{22} - z_{12} z_{21}$

h to g

$$g_{11} = \frac{h_{22}}{\Delta h} \qquad g_{12} = \frac{-h_{12}}{\Delta h} \qquad g_{21} = \frac{-h_{21}}{\Delta h} \qquad g_{22} = \frac{h_{11}}{\Delta h}$$

where $\Delta h = h_{11} h_{22} - h_{12} h_{21}$

g to h

$$h_{11} = \frac{g_{22}}{\Delta g} \qquad h_{12} = \frac{-g_{12}}{\Delta g} \qquad h_{21} = \frac{-g_{21}}{\Delta g} \qquad h_{22} = \frac{g_{11}}{\Delta g}$$

where $\Delta g = g_{11} g_{22} - g_{12} g_{21}$

z to y

$$y_{11} = \frac{z_{22}}{\Delta z} \qquad y_{12} = \frac{-z_{12}}{\Delta z} \qquad y_{21} = \frac{-z_{21}}{\Delta z} \qquad y_{22} = \frac{z_{11}}{\Delta z}$$

where $\Delta z = z_{11} z_{22} - z_{12} z_{21}$

y to z

$$z_{11} = \frac{y_{22}}{\Delta y} \qquad z_{12} = \frac{-y_{12}}{\Delta y} \qquad z_{21} = \frac{-y_{21}}{\Delta y} \qquad z_{22} = \frac{y_{11}}{\Delta y}$$

where $\Delta y = y_{11} y_{22} - y_{12} y_{21}$

z to g

$$g_{11} = \frac{1}{z_{11}} \qquad g_{12} = \frac{-z_{12}}{z_{11}} \qquad g_{21} = \frac{z_{21}}{z_{11}} \qquad g_{22} = \frac{\Delta z}{z_{11}}$$

where $\Delta z = z_{11} z_{22} - z_{12} z_{21}$

g to z

$$z_{11} = \frac{1}{g_{11}} \qquad z_{12} = \frac{-g_{12}}{g_{11}} \qquad z_{21} = \frac{g_{21}}{g_{11}} \qquad z_{22} = \frac{\Delta g}{g_{11}}$$

where $\Delta g = g_{11} g_{22} - g_{12} g_{21}$

g to y

$$y_{11} = \frac{\Delta g}{g_{22}} \qquad y_{12} = \frac{g_{12}}{g_{22}} \qquad y_{21} = \frac{-g_{21}}{g_{22}} \qquad y_{22} = \frac{1}{g_{22}}$$

where $\Delta g = g_{11} g_{22} - g_{12} g_{21}$

y to g

$$g_{11} = \frac{\Delta y}{y_{22}} \qquad g_{12} = \frac{y_{12}}{y_{22}} \qquad g_{21} = \frac{-y_{21}}{y_{22}} \qquad g_{22} = \frac{1}{y_{22}}$$

where $\Delta y = y_{11} y_{22} - y_{12} y_{21}$

B. Conversions among common emitter, common base, and common collector parameters of the same type for y, and h parameters.

Common emitter y parameters in terms of common base and common collector y parameters.

$$y_{11e} = y_{11b} + y_{12b} + y_{21b} + y_{22b} = y_{11c}$$

$$y_{12e} = -(y_{12b} + y_{22b}) = -(y_{11c} + y_{12c})$$

$$y_{21e} = -(y_{21b} + y_{22b}) = -(y_{11c} + y_{21c})$$

$$y_{22e} = y_{22b} = y_{11c} + y_{12c} + y_{21c} + y_{22c}$$

Common base y parameters in terms of common emitter and common collector y parameters.

$$y_{11b} = y_{11e} + y_{12e} + y_{21e} + y_{22e} = y_{22c}$$

$$y_{12b} = -(y_{12e} + y_{22e}) = -(y_{21c} + y_{22c})$$

$$y_{21b} = -(y_{21e} + y_{22e}) = -(y_{12c} + y_{22c})$$

$$y_{22b} = y_{22e} = y_{11c} + y_{12c} + y_{21c} + y_{22c}$$

Common collector y parameters in terms of common emitter and common base y parameters.

$$y_{11c} = y_{11e} = y_{11b} + y_{12b} + y_{21b} + y_{22b}$$

$$y_{12c} = -(y_{11e} + y_{12e}) = -(y_{11b} + y_{21b})$$

$$y_{21c} = -(y_{11e} + y_{21e}) = -(y_{11b} + y_{12b})$$

$$y_{22c} = y_{11e} + y_{12e} + y_{21e} + y_{22e} = y_{11b}$$

Common emitter h parameters in terms of common base and common collector h parameters.

$$h_{11e} = \frac{h_{11b}}{(1 + h_{21b})(1-h_{12b}) + h_{22b} h_{11b}} \approx \frac{h_{11b}}{1 + h_{21b}} = h_{11c}$$

$$h_{12e} = \frac{h_{11b} h_{22b} - h_{12b}(1+h_{21b})}{(1 + h_{21b})(1-h_{12b}) + h_{22b} h_{11b}} \approx \frac{h_{11b} h_{22b}}{1 + h_{21b}} - h_{12b} = 1-h_{12c}$$

$$h_{21e} = \frac{-h_{21b}(1-h_{12b}) - h_{22b} h_{11b}}{(1 + h_{21b})(1-h_{12b}) + h_{22b} h_{11b}} \approx \frac{-h_{21b}}{1 + h_{21b}} = -(1 + h_{21c})$$

$$h_{22e} = \frac{h_{22b}}{(1 + h_{21b})(1-h_{12b}) + h_{22b} h_{11b}} \approx \frac{h_{22b}}{1 + h_{21b}} = h_{22c}$$

Common has h parameters in terms of common emitter and common collector h parameters.

$$h_{11b} = \frac{h_{11e}}{(1 + h_{21e})(1-h_{12e}) + h_{11e} h_{22e}} \approx \frac{h_{11e}}{1 + h_{21e}}$$

$$= \frac{h_{11c}}{h_{11c} h_{22c} - h_{21c} h_{12c}} \approx \frac{-h_{11c}}{h_{21c}}$$

6

$$h_{12b} = \frac{h_{11e}\,h_{22e} - h_{12e}(1 + h_{21e})}{(1 + h_{21e})(1-h_{12e}) + h_{11e}\,h_{22e}} \approx \frac{h_{11e}\,h_{22e}}{1 + h_{21e}} - h_{12e}$$

$$= \frac{h_{21c}(1-h_{12c}) + h_{11c}\,h_{22c}}{h_{11c}\,h_{22c} - h_{21c}\,h_{12c}} \approx (h_{12c} - 1) - \frac{h_{11c}\,h_{22c}}{h_{21c}}$$

$$h_{21b} = \frac{-h_{21e}(1-h_{12e}) - h_{11e}\,h_{22e}}{(1 + h_{21e})(1-h_{12e}) + h_{11e}\,h_{22e}} \approx \frac{-h_{21e}}{1 + h_{21e}}$$

$$= \frac{h_{12c}(1 + h_{21c}) - h_{11c}\,h_{22c}}{h_{11c}\,h_{22c} - h_{21c}\,h_{12c}} \approx \frac{-(1 + h_{21c})}{h_{21c}}$$

$$h_{22b} = \frac{h_{22e}}{(1 + h_{21e})(1-h_{12e}) + h_{11e}\,h_{22e}} \approx \frac{h_{22e}}{1 + h_{21e}}$$

$$= \frac{h_{22c}}{h_{11c}\,h_{22c} - h_{21c}\,h_{12c}} \approx \frac{h_{22c}}{h_{21c}}$$

Common collector h parameters in terms of common base and common emitter h parameters.

$$h_{11c} = \frac{h_{11b}}{(1 + h_{21b})(1-h_{12b}) + h_{22b}\,h_{11b}} \approx \frac{h_{11b}}{1 + h_{21b}} = h_{11e}$$

$$h_{12c} = \frac{1 + h_{21b}}{(1 + h_{21b})(1-h_{12b}) + h_{22b}\,h_{11b}} \approx 1 = 1-h_{12e}$$

$$h_{21c} = \frac{h_{12b} - 1}{(1 + h_{21b})(1-h_{12b}) + h_{22b}\,h_{11b}} \approx \frac{-1}{1 + h_{21b}} = -(1 + h_{21e})$$

$$h_{22c} = \frac{h_{22b}}{(1 + h_{21b})(1-h_{12b}) + h_{22b}\,h_{11b}} \approx \frac{h_{22b}}{1 + h_{21b}} = h_{22e}$$

Expressions for voltage gain, current gain, input impedance, and output impedance in terms of y, z, h, and g parameters.

Voltage Gain

$$A_V = \frac{z_{21}\,Z_L}{\Delta z + z_{11}\,Z_L} = \frac{-y_{21}}{y_{22} + Y_L} = \frac{-h_{21}\,Z_L}{h_{11} + \Delta h Z_L} = \frac{g_{21}\,Z_L}{g_{22} + Z_L}$$

$$= \frac{S_{21}(1 + \Gamma_L)}{(1 - S_{22}\Gamma_L)(1 + S_{11})}$$

Current Gain

$$A_I = \frac{-z_{21}}{z_{22} + Z_L} = \frac{-y_{21}\,Y_L}{\Delta y + y_{11}\,Y_L} = \frac{h_{21}\,Y_L}{h_{22} + Y_L} = \frac{-g_{21}}{\Delta g + g_{11}\,Z_L}$$

Input Impedance

$$Z_{IN} = \frac{\Delta z + z_{11}\,Z_L}{z_{22} + Z_L} = \frac{y_{22} + Y_L}{\Delta y + y_{11}\,Y_L} = \frac{\Delta h + h_{11}\,Y_L}{h_{22} + Y_L}$$

$$= \frac{g_{22} + Z_L}{\Delta g + g_{11}\,Z_L}$$

Output Impedance

$$Z_{OUT} = \frac{\Delta z + z_{22}\,Z_s}{z_{11} + Z_s} = \frac{y_{11} + Y_s}{\Delta y + y_{22}\,Y_s} = \frac{h_{11} + Z_s}{\Delta h + h_{22}\,Z_s}$$

$$= \frac{\Delta g + g_{22}\,Y_s}{g_{11} + Y_s}$$

Conversion between y parameters and s (scattering) parameters:

$$s_{11} = \frac{(1-y_{11})(1+y_{22}) + y_{12}\,y_{21}}{(1+y_{11})(1+y_{22}) - y_{12}\,y_{21}} \dagger$$

$$s_{12} = \frac{-2y_{12}}{(1+y_{11})(1+y_{22}) - y_{12}\,y_{21}} \dagger$$

$$s_{21} = \frac{-2y_{21}}{(1+y_{11})(1+y_{22}) - y_{12}\,y_{21}} \dagger$$

$$s_{22} = \frac{(1+y_{11})(1-y_{22}) + y_{21}\,y_{12}}{(1+y_{11})(1+y_{22}) - y_{12}\,y_{21}} \dagger$$

$$y_{11} = \left[\frac{(1+s_{22})(1-s_{11}) + s_{12}\,s_{21}}{(1+s_{11})(1+s_{22}) - s_{12}\,s_{21}}\right] \frac{1}{Z_o}$$

$$y_{12} = \left[\frac{-2s_{12}}{(1+s_{11})(1+s_{22}) - s_{12}\,s_{21}}\right] \frac{1}{Z_o}$$

$$y_{21} = \left[\frac{-2s_{21}}{(1+s_{11})(1+s_{22}) - s_{12}\,s_{21}}\right] \frac{1}{Z_o}$$

$$y_{22} = \left[\frac{(1+s_{11})(1-s_{22}) + s_{12}\,s_{21}}{(1+s_{22})(1+s_{11}) - s_{12}\,s_{21}}\right] \frac{1}{Z_o}$$

where Z_O= the characteristic impedance of the transmission lines used in the scattering parameter system, usually 50 ohms.

Conversion between h parameters and s parameters:

$$s_{11} = \frac{(h_{11}-1)(h_{22}+1) - h_{12}\,h_{21}}{(h_{11}+1)(h_{22}+1) - h_{12}\,h_{21}} \dagger\dagger$$

$$s_{12} = \frac{2h_{12}}{(h_{11}+1)(h_{22}+1) - h_{12}\,h_{21}} \dagger\dagger$$

$$s_{21} = \frac{-2h_{21}}{(h_{11}+1)(h_{22}+1) - h_{12}\,h_{21}} \dagger\dagger$$

$$s_{22} = \frac{(1+h_{11})(1-h_{22}) + h_{12}\,h_{21}}{(h_{11}+1)(h_{22}+1) - h_{12}\,h_{21}} \dagger\dagger$$

$$h_{11} = \left[\frac{(1+s_{11})(1+s_{22}) - s_{12}\,s_{21}}{(1-s_{11})(1+s_{22}) + s_{12}\,s_{21}}\right] Z_o$$

6

$$h_{12} = \frac{2s_{12}}{(1-s_{11})(1+s_{22}) + s_{12}\,s_{21}}$$

$$h_{21} = \frac{-2s_{21}}{(1-s_{11})(1+s_{22}) + s_{12}\,s_{21}}$$

$$h_{22} = \left[\frac{(1-s_{22})(1-s_{11}) - s_{12}\,s_{21}}{(1-s_{11})(1+s_{22}) + s_{12}\,s_{21}}\right] \frac{1}{Z_o}$$

---

†In converting from y to s parameters, the y parameters must first be multiplied by Z_O, and then substituted in the equations for conversion to s parameters.

††In converting from h to s parameters, the h parameters must first be normalized to Z_O in the following manner and then substituted in the equations for conversion to s parameters:

Parameter	To Normalize
h_{11}	divide by Z_O
h_{12}	use as is
h_{21}	use as is
h_{22}	multiply by Z_O

Conversion between z parameters and s parameters:

$$Z_{11} = \left[\frac{(1+S_{11})(1-S_{22}) + S_{12}S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}\right] Z_o$$

$$Z_{12} = \left[\frac{2S_{12}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}\right] Z_o$$

$$Z_{21} = \left[\frac{2S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}\right] Z_o$$

$$Z_{22} = \left[\frac{(1+S_{22})(1-S_{11}) + S_{12}S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}\right] Z_o$$

$$S_{11} = \frac{(Z_{11}-1)(Z_{22}+1) - Z_{12}Z_{21}}{(Z_{11}+1)(Z_{22}+1) - Z_{12}Z_{21}} \quad \dagger\dagger\dagger$$

$$S_{12} = \frac{2Z_{12}}{(Z_{11}+1)(Z_{22}+1) - Z_{12}Z_{21}} \quad \dagger\dagger\dagger$$

$$S_{21} = \frac{2Z_{21}}{(Z_{11}+1)(Z_{22}+1) - Z_{12}Z_{21}} \quad \dagger\dagger\dagger$$

$$S_{22} = \frac{(Z_{11}+1)(Z_{22}-1) - Z_{12}Z_{21}}{(Z_{11}+1)(Z_{22}+1) - Z_{12}Z_{21}} \quad \dagger\dagger\dagger$$

---

†††In converting from z to s parameters, the z parameters must first be divided by Z_O, and then substituted in the equations for conversion to s parameters.

MATCHING NETWORK DESIGNS WITH COMPUTER SOLUTIONS

Prepared by:
Frank Davis

INTRODUCTION

One of the problems facing the circuit design engineer is the design of high-frequency matching networks. Careful design of a network that will accomplish the required matching, harmonic attenuation, bandwidth, etc., and yield components of practical size can result in many hours spent with pencil and slide rule.

The design of matching networks for high frequency circuits involves an infinite number of possibilities, and a complete tabulation of possible network solutions would be virtually impossible. However, it is often necessary to design matching networks with a 50 + j 0 ohm impedance at one port. This, combined with a restricted range of impedance values to be matched, imposed by network and device limitations, makes practical a tabulation of some of the more commonly used networks. These design solutions are given in this report.

The network solutions included in this report have the limitation that one terminating impedance must be 50 + j 0 ohms. These networks are often used for matching in transistor RF power amplifier circuits that have a 50-ohm source or load. When the network does not have a 50-ohm termination at either port, the mathematical procedure given for each network in Appendix I can be used for the solution.

COMPONENT CONSIDERATIONS

Four networks are presented in this report with solutions in the form of computer tabulations. Each network has its own limitations. Although the network configuration is normally up to the discretion of the design engineer, it is sometimes necessary to use one configuration in preference to another in order to obtain component values that are more realistic from a practical standpoint.

Component selection in the UHF and VHF frequency ranges becomes a major problem, and the network configuration to obtain realistic component values is of vital importance to the design engineer. Design calculations for matching networks can become completely meaningless unless the components for the network are measured at the operating frequency.

For example, a 100 pF silver mica capacitor that meets all specifications at 1 MHz can have as much capacitance as 300 pF at 100 MHz. At some frequency, the capacitor's series lead inductance will finally tune out the capacitance, thus leaving the capacitor net inductive.

Values of inductance in the low nanohenry range are also difficult to obtain, since the inductance of a one-inch straight piece of #20 solid tinned wire is approximately 20 nH.

Component tolerances have no meaning at VHF frequencies and above unless they are specified at the operating frequency. It cannot be over-emphasized that components must be measured at the operating frequency.

NETWORK SOLUTIONS

The resistor and capacitor shown in the box labeled "device to be matched" represent the complex input or output impedance of a transistor. These complex impedances have been represented in series form in some cases and parallel form in others, depending on which form is most convenient for network calculation. The resultant impedance of the network, when terminated with 50 + j 0 ohms, must be equal to the conjugate of the impedance in the box. The computer tabulations provide this solution.

Network A (see Figure 1) is applicable only when the "device to be matched" has a series real part of less than 50 ohms. As we can see from the computer tabulation, as the series real part approaches 50 ohms, the reactance of C_1 approaches infinity. However, in RF power amplifiers, we normally find that the series real part of both the input and the output is less than 50 ohms, making this matching network applicable to most RF power amplifier stages. Where the terminating impedance is other than 50 ohms, the mathematical procedure for the network solution is given in Appendix I.

Network B (see Figure 2) is the Pi network widely used in vacuum tube transmitters. As is apparent from the computer tabulation, this network is often impractical for use where R_1 is small. For values of R_1 less than 50 ohms, the inductance of L becomes impractically small while the capacitance of both C_1 and C_2 become very large. Where the Pi network configuration must be used to match low values of impedance, a double Pi network, in which the Q of the first section is very low, can be utilized to yield practical components.

Network C has been solved in two forms (see Figure 3). Both of these networks have the limitation that R_1 must be less than 50 ohms. However, it must be stressed that this network configuration quite often yields the most practical components where low values of R_1 must be matched.

Network D (see Figure 4) is a "Tee" network. This network is useful for matching impedance less than or greater than 50 ohms. It has been observed in laboratory tests that this network configuration also yields very high collector efficiencies when used for output matching in transistor RF power amplifier stages.

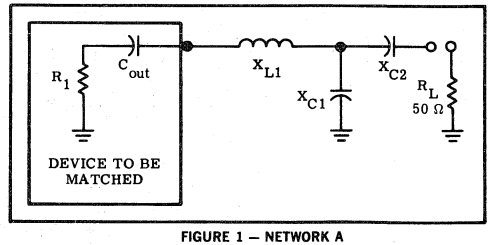


FIGURE 1 — NETWORK A

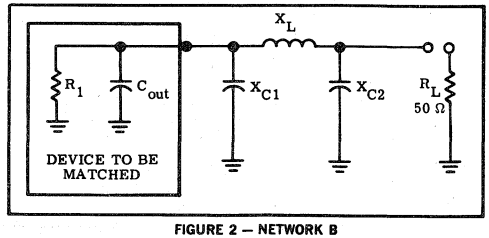


FIGURE 2 — NETWORK B

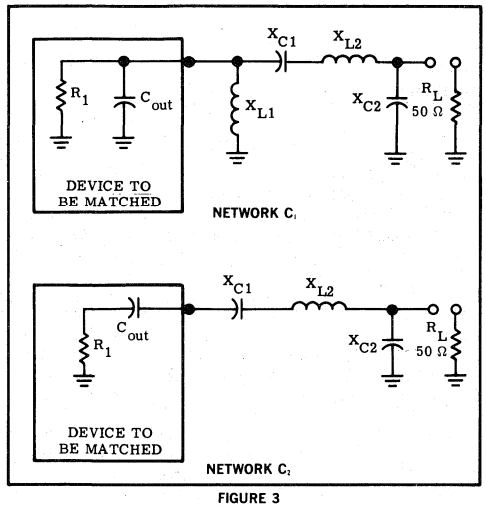


FIGURE 3

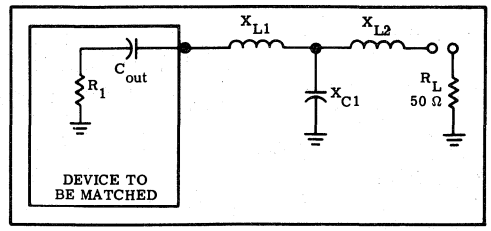


FIGURE 4 — NETWORK D

SUMMARY

Four computer-solved networks have been presented. The mathematical procedure for the solution of each network has been given in Appendix I.* Although the networks have found major use in matching solid-state RF power amplifier stages, they are also applicable to any circuit where the individual network's limitations are fulfilled.

*For the derivation of the equations used, refer to Electronic Circuit Analysis, Volume 1, "Passive Networks," Philip Cutler.

APPENDIX I

To convert a parallel resistance and reactance combination to series:

$$R_S = \frac{R_P}{1 + (R_P/X_P)^2}$$

$$X_S = R_S \frac{R_P}{X_P}$$

To convert a series resistance and reactance combination to parallel:

$$R_P = R_S[1 + (X_S/R_S)^2]$$

$$X_P = \frac{R_P}{X_S/R_S}$$

To solve network A:

1. Select a Q

$$X_{L1} = QR_1 + X_{C\,out}$$

$$X_{C2} = A R_L$$

$$X_{C1} = \frac{(B/A)(B/Q)}{(B/A)-(B/Q)} = \frac{B}{Q - A}$$

where $A = \sqrt{\left[\frac{R_1(1+Q^2)}{R_L}\right] - 1}$

$$B = R_1(1 + Q^2)$$

To solve network B:

1. Select a Q

$$X_{C1} = R_1/Q$$

$$X_{C2} = R_L\sqrt{\frac{R_1/R_L}{(Q^2+1)-(R_1/R_L)}}$$

$$X_L = \frac{QR_1 + (R_1R_L/X_{C2})}{Q^2 + 1}$$

To solve network C_1:

1. Select a Q

$$X_{L1} = X_{C\,out}$$

$$X_{C1} = QR_1$$

$$X_{C2} = R_L\sqrt{\frac{R_1}{R_L - R_1}}$$

$$X_{L2} = X_{C1} + \left(\frac{R_1R_L}{X_{C2}}\right)$$

To solve network C_2:

1. Select a Q
2. L_1 is not used in this network

$$X_{C1} = QR_1$$

$$X_{C2} = R_L\sqrt{\frac{R_1}{R_L - R_1}}$$

$$X_{L2} = X_{C1} + \left(\frac{R_1R_L}{X_{C2}}\right) + X_{C\,out}$$

To solve network D:

1. Select a Q

$$X_{L1} = (R_1Q) + X_{C\,out}$$

$$X_{L2} = R_L B$$

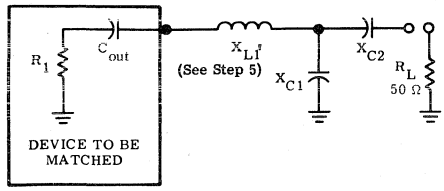
$$X_{C1} = \frac{(A/Q)(A/B)}{(A/Q) + (A/B)} = \frac{A}{Q + B}$$

where $A = R_1(1 + Q^2)$

$$B = \sqrt{\left(\frac{A}{R_L}\right) - 1}$$

6

NETWORK A



TO DESIGN A NETWORK USING THE TABLES

1. Transform the parallel impedance of the device to be matched to series form ($R_1 + jX_{C_{out}}$).
2. Define Q, in column one, as X_{L1}/R_1.
3. Choose a Q.
4. For a Q, find the R_s to be matched in the R column and read the reactive value of the components.
5. X_{L1}' is equal to the quantity X_{L1} obtained from the tables plus $|X_{C_{out}}|$.
6. This completes the network.

Q	X_{L1}	X_{C1}	X_{C2}	R_1
1	26	65	10	26
1	27	75.3	14.14	27
1	28	85.68	17.32	28
1	29	96.66	20	29
1	30	108.5	22.36	30
1	32	136	26.46	32
1	34	170	30	34
1	36	213.8	33.16	36
1	38	272.5	36.05	38
1	40	355	38.7	40
1	42	479	41.23	42
1	44	686.32	43.59	44
1	46	1102	45.83	46
1	48	2351	48	48
2	22	32.7	15.8	11
2	24	38.6	22.4	12
2	26	45	27.4	13
2	28	51.2	31.6	14
2	30	58	35.4	15
2	32	65.3	38.7	16
2	34	73.1	41.8	17
2	36	81.4	44.7	18
2	38	90.3	47.4	19
2	40	100	50	20
2	42	110.4	52.4	21
2	44	122	55	22
2	46	134	57	23
2	48	147	59	24
2	50	161	61	25
2	52	177	63	26
2	54	194	65	27
2	56	213	67	28
2	58	233	69	29
2	60	256	71	30
2	64	310	74	32
2	68	377	77	34
2	72	464	81	36
2	76	582	84	38
2	80	746	87	40
2	84	995	89	42
2	88	1409	92	44
2	92	2241	95	46
2	96	4739	97	48
3	18	23.5	22.3	6
3	21	29.6	31.6	7
3	24	35.9	38.7	8
3	27	42.7	44.7	9
3	30	50	50	10
3	33	57.8	54.8	11
3	36	66	59	12
3	39	75	63.2	13

Q	X_{L1}	X_{C1}	X_{C2}	R_1
3	42	84	67	14
3	45	95	71	15
3	48	105	74	16
3	51	117	77	17
3	54	130	81	18
3	57	143	84	19
3	60	158	87	20
3	63	173	89	21
3	66	190	92	22
3	69	209	95	23
3	72	228	97	24
3	75	250	100	25
3	78	274	102	26
3	81	299	105	27
3	84	327	107	28
3	87	358	110	29
3	90	393	112	30
3	96	473	116	32
3	102	575	120	34
3	108	706	124	36
3	114	882	128	38
3	120	1129	132	40
3	126	1502	136	42
3	132	2124	140	44
3	138	3372	143	46
3	144	7119	146	48
4	12	13.2	7.1	3
4	16	20	30	4
4	20	26.9	41.8	5
4	24	34.2	51	6
4	28	42.1	58.7	7
4	32	50.6	66	8
4	36	60	72	9
4	40	69	77	10
4	44	80	83	11
4	48	91	88	12
4	52	103	92	13
4	56	115	97	14
4	60	129	101	15
4	64	144	105	16
4	68	159	109	17
4	72	176	113	18
4	76	194	117	19
4	80	214	120	20
4	84	235	124	21
4	88	257	127	22
4	92	282	131	23
4	96	308	134	24
4	100	337	137	25
4	104	368	140	26
4	108	403	143	27

Q	X_{L1}	X_{C1}	X_{C2}	R_1
4	112	440	146	28
4	116	482	149	29
4	120	527	152	30
4	128	635	157	32
4	136	770	162	34
4	144	945	168	36
4	152	1180	173	38
4	160	1510	177	40
4	168	2007	182	42
4	176	2837	187	44
4	184	4500	191	46
4	192	9497	196	48
5	10	10.8	10	2
5	15	18.3	37.4	3
5	20	26.3	52	4
5	25	34.8	63.2	5
5	30	44	73	6
5	35	54	81	7
5	40	65	89	8
5	45	76	96	9
5	50	88	102	10
5	55	101	108	11
5	60	115	114	12
5	65	130	120	13
5	70	146	125	14
5	75	163	130	15
5	80	181	135	16
5	85	201	140	17
5	90	222	145	18
5	95	245	149	19
5	100	269	153	20
5	105	295	157	21
5	110	323	162	22
5	115	354	166	23
5	120	387	169	24
5	125	423	173	25
5	130	462	177	26
5	135	505	181	27
5	140	553	184	28
5	145	604	188	29
5	150	662	191	30
5	160	796	198	32
5	170	965	204	34
5	180	1184	210	36
5	190	1477	217	38
5	200	1890	222	40
5	210	2510	228	42
5	220	3548	234	44
5	230	5628	239	46
5	240	11874	245	48

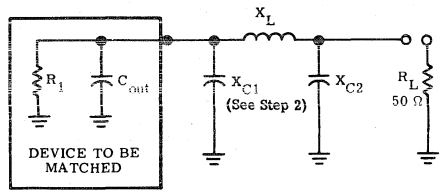
Q	X_{L1}	X_{C1}	X_{C2}	R_1
6	12	13.9	34.6	2
6	18	22.7	55.2	3
6	24	32.2	70	4
6	30	42.5	82	5
6	36	53.6	93	6
6	42	65.5	102	7
6	48	78	110	8
6	54	92	119	9
6	60	107	126	10
6	66	122	133	11
6	72	139	140	12
6	78	157	147	13
6	84	176	153	14
6	90	197	159	15
6	96	219	165	16
6	102	242	170	17
6	108	267	175	18
6	114	295	181	19
6	120	324	186	20
6	126	355	191	21
6	132	389	195	22
6	138	426	200	23
6	144	466	205	24
6	150	509	209	25
6	156	556	214	26
6	162	608	218	27
6	168	664	222	28
6	174	727	226	29
6	180	795	230	30
6	192	957	238	32
6	204	1160	246	34
6	216	1422	253	36
6	228	1775	260	38
6	240	2270	267	40
6	252	3015	274	42
6	264	4260	281	44
6	276	6755	287	46
6	288	14250	294	48
7	14	16.7	50	2
7	21	26.8	71	3
7	28	38	87	4
7	35	50	100	5
7	42	63	112	6
7	49	77	122	7
7	56	92	132	8
7	63	108	141	9
7	70	125	150	10
7	77	143	158	11
7	84	163	166	12
7	91	184	173	13
7	98	206	180	14
7	105	230	187	15
7	112	256	193	16
7	119	283	200	17
7	126	313	206	18
7	133	344	212	19
7	140	379	218	20
7	147	415	224	21
7	154	455	229	22
7	161	498	234	23
7	168	544	239	24
7	175	595	245	25
7	182	650	250	26

Q	X_{L1}	X_{C1}	X_{C2}	R_1
7	189	710	255	27
7	196	776	260	28
7	203	849	265	29
7	210	929	269	30
7	224	1117	278	32
7	238	1354	287	34
7	252	1661	296	36
7	266	2071	304	38
7	280	2649	312	40
7	294	3518	320	42
7	308	4971	328	44
7	322	7882	335	46
7	336	16626	343	48
8	8	8.7	27.4	1
8	16	19.3	63.2	2
8	24	31	85	3
8	32	43.6	102	4
8	40	57.4	117	5
8	48	72	130	6
8	56	88	142	7
8	64	105	153	8
8	72	124	164	9
8	80	143	173	10
8	88	164	182	11
8	96	187	191	12
8	104	211	199	13
8	112	236	207	14
8	120	264	215	15
8	128	293	222	16
8	136	324	230	17
8	144	358	237	18
8	152	394	243	19
8	160	433	250	20
8	168	475	256	21
8	176	521	263	22
8	184	570	269	23
8	192	623	275	24
8	200	681	281	25
8	208	744	286	26
8	216	812	292	27
8	224	888	297	28
8	232	971	303	29
8	240	1062	308	30
8	256	1277	318	32
8	272	1548	329	34
8	288	1899	338	36
8	304	2368	348	38
8	320	3028	357	40
8	336	4022	366	42
8	352	5682	375	44
8	368	9009	383	46
9	9	10	40	1
9	18	21.9	76	2
9	27	35	99	3
9	36	49.4	118	4
9	45	65	134	5
9	54	82	149	6
9	63	100	162	7
9	72	119	174	8
9	81	139	185	9
9	90	162	196	10
9	99	185	206	11

Q	X_{L1}	X_{C1}	X_{C2}	R_1
9	108	210	216	12
9	117	237	225	13
9	126	266	234	14
9	135	297	243	15
9	144	330	251	16
9	153	365	259	17
9	162	403	267	18
9	171	444	275	19
9	180	488	282	20
9	189	535	289	21
9	198	586	296	22
9	207	641	303	23
9	216	701	310	24
9	225	766	316	25
9	234	837	323	26
9	243	914	329	27
9	252	999	335	28
9	261	1092	341	29
9	270	1196	347	30
9	288	1438	359	32
9	306	1743	370	34
9	324	2137	381	36
9	342	2665	391	38
9	360	3407	402	40
9	378	4525	412	42
9	396	6393	422	44
10	10	11.2	50.5	1
10	20	24.5	87	2
10	30	39	112	3
10	40	55	133	4
10	50	72	151	5
10	60	91	167	6
10	70	111	181	7
10	80	132	195	8
10	90	155	207	9
10	100	180	219	10
10	110	206	230	11
10	120	234	241	12
10	130	264	251	13
10	140	296	261	14
10	150	330	271	15
10	160	367	280	16
10	170	406	289	17
10	180	448	297	18
10	190	494	306	19
10	200	543	314	20
10	210	595	322	21
10	220	652	330	22
10	230	713	337	23
10	240	780	345	24
10	250	852	352	25
10	260	930	359	26
10	270	1016	366	27
10	280	1111	373	28
10	290	1214	379	29
10	300	1329	383	30
10	320	1598	399	32
10	340	1937	411	34
10	360	2375	423	36
10	380	2961	435	38
10	400	3787	446	40
10	420	5029	458	42
10	440	7104	469	44

NETWORK B

The following is a computer solution for the Pi network when R_L equals 50 ohms.



TO DESIGN A NETWORK USING THE TABLES

1. Define Q, in column one, as R_1/X_{C1}.
2. C_1 actual is equal to C_1 – parallel C_{out} of device to be matched.
3. This completes the network.

Q	X_{C1}	X_{C2}	X_L	R_1
1	1	5.03	5.47	1
1	2	7.14	8	2
1	3	8.79	10.03	3
1	4	10.21	11.8	4
1	5	11.47	13.4	5
1	10	16.67	20	10
1	15	21	25.35	15
1	20	25	30	20
1	25	28.87	34.15	25
1	30	32.73	37.91	30
1	35	36.69	41.35	35
1	40	40.82	44.49	40
1	45	45.23	47.37	45
1	50	50	50	50
1	55	55.28	52.37	55
1	60	61.24	54.49	60
1	65	68.14	56.35	65
1	70	76.38	57.91	70
1	75	86.6	59.15	75
1	80	100	60	80
1	85	119.02	60.35	85
1	90	150	60	90
2	0.5	3.17	3.56	1
2	1	4.49	5.25	2
2	1.5	5.51	6.64	3
2	2	6.38	7.87	4
2	2.5	7.14	9	5
2	5	10.21	13.8	10
2	7.5	12.63	17.87	15
2	10	14.74	21.56	20
2	12.5	16.67	25	25
2	15	18.46	28.25	30
2	17.5	20.17	31.35	35
2	20	21.82	34.33	40
2	22.5	23.43	37.21	45
2	25	25	40	50
2	27.5	26.55	42.71	55
2	30	28.1	45.35	60
2	32.5	29.64	47.93	65
2	35	31.18	50.45	70
2	37.5	32.73	52.91	75
2	40	34.3	55.32	80
2	42.5	35.89	57.69	85
2	45	37.5	60	90
2	47.5	39.14	62.27	95
2	50	40.82	64.49	100
2	62.5	50	75	125
2	75	61.24	84.49	150
2	87.5	76.38	92.91	175
2	100	100	100	200
2	112.5	150	105	225

Q	X_{C1}	X_{C2}	X_L	R_1
3	0.33	2.24	2.53	1
3	0.67	3.17	3.76	2
3	1	3.88	4.76	3
3	1.33	4.49	5.65	4
3	1.67	5.03	6.47	5
3	3.33	7.14	10	10
3	5	8.79	13.03	15
3	6.67	10.21	15.8	20
3	8.33	11.47	18.4	25
3	10	12.63	20.87	30
3	11.67	13.72	23.26	35
3	13.33	14.74	25.56	40
3	15	15.72	27.81	45
3	16.67	16.67	30	50
3	18.33	17.58	32.14	55
3	20	18.46	34.25	60
3	21.67	19.33	36.32	65
3	23.33	20.17	38.35	70
3	25	21	40.35	75
3	26.67	21.82	42.33	80
3	28.33	22.63	44.28	85
3	30	23.43	46.21	90
3	31.67	24.22	48.12	95
3	33.33	25	50	100
3	41.67	28.87	59.12	125
3	50	32.73	67.91	150
3	58.33	36.69	76.35	175
3	66.67	40.82	84.49	200
3	75	45.23	92.37	225
3	83.33	50	100	250
4	6.25	8.7	14.33	25
4	12.5	12.5	23.53	50
4	18.75	15.55	31.83	75
4	25	18.26	39.64	100
4	31.25	20.76	47.12	125
4	37.5	23.15	54.36	150
4	43.75	25.46	61.39	175
4	50	27.74	68.27	200
4	56.25	30	75	225
4	62.5	32.27	81.61	250
4	75	36.93	94.48	300
4	100	47.14	119.07	400
4	125	59.76	142.25	500
4	150	77.46	163.96	600
4	175	108.01	183.77	700
4	200	200	200	800
5	0.2	1.39	1.58	1
5	5	7	11.67	25
5	10	10	19.23	50
5	15	12.37	26.08	75

Q	X_{C1}	X_{C2}	X_L	R_1
5	20	14.43	32.55	100
5	25	16.31	38.78	125
5	30	18.06	44.82	150
5	35	19.72	50.72	175
5	40	21.32	56.5	200
5	45	22.87	62.18	225
5	50	24.4	67.78	250
5	60	27.39	78.76	300
5	80	33.33	100	400
5	100	39.53	120.48	500
5	120	46.29	140.31	600
5	140	54.01	159.54	700
5	160	63.25	178.17	800
5	180	75	196.15	900
5	200	91.29	213.37	1000
5	220	117.26	229.58	1100
5	240	173.21	244.09	1200
6	0.17	1.16	1.32	1
6	4.17	5.85	9.83	25
6	8.33	8.33	16.22	50
6	12.5	10.28	22.02	75
6	16.67	11.95	27.52	100
6	20.83	13.46	32.82	125
6	25	14.85	37.97	150
6	29.17	16.16	43.01	175
6	33.33	17.41	47.96	200
6	37.5	18.61	52.83	225
6	41.67	19.76	57.63	250
6	50	22	67.08	300
6	66.67	26.26	85.45	400
6	83.33	30.43	103.29	500
6	100	34.64	120.7	600
6	116.67	39.01	137.76	700
6	133.33	43.64	154.5	800
6	150	48.67	170.94	900
6	166.67	54.23	187.08	1000
6	183.33	60.55	202.93	1100
6	200	67.94	218.46	1200
6	216.67	76.87	233.66	1300
6	233.33	88.19	248.48	1400
6	250	103.51	262.83	1500
6	266.67	126.49	276.55	1600
6	283.33	168.33	289.32	1700
6	300	300	300	1800
7	0.14	1	1.14	1
7	3.57	5.03	8.47	25
7	7.14	7.14	14	50
7	10.71	8.79	19.03	75
7	14.29	10.21	23.8	100
7	17.86	11.47	28.4	125

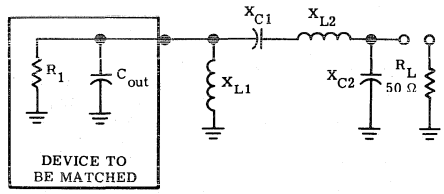
Q	X_{C1}	X_{C2}	X_L	R_1
7	21.43	12.63	32.87	150
7	25	13.72	37.26	175
7	28.57	14.74	41.56	200
7	32.14	15.72	45.81	225
7	35.71	16.67	50	250
7	42.86	18.46	58.25	300
7	57.14	21.82	74.33	400
7	71.43	25	90	500
7	85.71	28.1	105.35	600
7	100	31.18	120.45	700
7	114.29	34.3	135.32	800
7	128.57	37.5	150	900
7	142.86	40.82	164.49	1000
7	171.43	48.04	192.98	1200
7	200	56.41	220.82	1400
7	228.57	66.67	248	1600
7	257.14	80.18	274.45	1800
7	285.71	100	300	2000
7	314.29	135.4	324.25	2200
7	342.86	244.95	345.8	2400
8	0.13	0.88	1	1
8	3.13	4.4	7.45	25
8	6.25	6.25	12.31	50
8	9.38	7.68	16.74	75
8	12.5	8.91	20.94	100
8	15.63	10	25	125
8	18.75	11	28.95	150
8	21.88	11.93	32.82	175
8	25	12.8	36.63	200
8	28.13	13.64	40.38	225
8	31.25	14.43	44.09	250
8	37.5	15.94	51.4	300
8	50	18.73	65.66	400
8	62.5	21.32	79.58	500
8	75	23.79	93.25	600
8	87.5	26.2	106.71	700
8	100	28.57	120	800
8	112.5	30.94	133.14	900
8	125	33.33	146.15	1000
8	150	38.25	171.82	1200
8	175	43.5	197.07	1400
8	200	49.24	221.92	1600
8	225	55.71	246.39	1800
8	250	63.25	270.48	2000
8	275	72.37	294.15	2200
8	300	84.02	317.36	2400
9	8.33	6.83	14.93	75
9	11.11	7.91	18.69	100
9	13.89	8.87	22.32	125
9	16.67	9.74	25.85	150
9	19.44	10.56	29.31	175
9	22.22	11.32	32.72	200
9	25	12.05	36.08	225
9	27.78	12.74	39.4	250
9	33.33	14.05	45.95	300
9	44.44	16.44	58.74	400
9	55.56	18.63	71.24	500
9	66.67	20.7	83.53	600
9	77.78	22.69	95.64	700
9	88.89	24.62	107.62	800
9	100	26.52	119.48	900
9	111.11	28.4	131.23	1000
9	133.33	32.16	154.46	1200
9	155.56	36	177.37	1400
9	177.78	40	200	1600
9	200	44.23	222.37	1800
9	222.22	48.8	244.5	2000
9	244.44	53.8	266.4	2200
9	266.67	59.41	288.05	2400

Q	X_{C1}	X_{C2}	X_L	R_1
10	0.1	0.7	0.8	1
10	5	5	9.9	50
10	10	7.11	16.87	100
10	15	8.75	23.34	150
10	20	10.15	29.55	200
10	25	11.41	35.6	250
10	30	12.57	41.52	300
10	40	14.66	53.11	400
10	50	16.57	64.44	500
10	60	18.36	75.58	600
10	70	20.06	86.58	700
10	80	21.69	97.46	800
10	90	23.28	108.24	900
10	100	24.85	118.94	1000
10	120	27.91	140.09	1200
10	140	30.97	161	1400
10	160	34.05	181.68	1600
10	180	37.21	202.17	1800
10	200	40.49	222.47	2000
10	220	43.93	242.61	2200
10	240	47.58	262.59	2400
12	25	10.39	34.79	300
12	33.33	12.08	44.52	400
12	41.67	13.61	54.05	500
12	50	15.02	63.43	600
12	58.33	16.35	72.7	700
12	66.67	17.61	81.87	800
12	75	18.82	90.97	900
12	83.33	20	100	1000
12	100	22.27	117.89	1200
12	116.67	24.46	135.6	1400
12	133.33	26.61	153.15	1600
12	150	28.73	170.57	1800
12	166.67	30.86	187.86	2000
12	183.33	33	205.06	2200
12	200	35.17	222.15	2400
12	216.67	37.39	239.16	2600
12	233.33	39.66	256.07	2800
12	250	42.01	272.9	3000
12	291.67	48.3	314.64	3500
12	333.33	55.47	355.9	4000
12	375	63.96	396.67	4500
12	416.67	74.54	436.92	5000
12	458.33	88.64	476.57	5500
12	500	109.54	515.44	6000
14	21.43	8.86	29.91	300
14	28.57	10.29	38.3	400
14	35.71	11.56	46.51	500
14	42.86	12.73	54.6	600
14	50	13.83	62.59	700
14	57.14	14.87	70.51	800
14	64.29	15.86	78.37	900
14	71.43	16.81	86.17	1000
14	85.71	18.62	101.63	1200
14	100	20.35	116.95	1400
14	114.29	22.02	132.15	1600
14	128.57	23.64	147.24	1800
14	142.86	25.24	162.25	2000
14	157.14	26.81	177.17	2200
14	171.43	28.38	192.02	2400
14	185.71	29.94	206.81	2600
14	200	31.51	221.54	2800
14	214.29	33.09	236.21	3000
14	250	37.12	272.66	3500
14	285.71	41.34	308.82	4000
14	321.43	45.86	344.7	4500
14	357.14	50.77	380.33	5000
14	392.86	56.22	415.69	5500
14	428.57	62.42	450.79	6000

Q	X_{C1}	X_{C2}	X_L	R_1
16	18.75	7.73	26.23	300
16	25	8.96	33.59	400
16	31.25	10.06	40.8	500
16	37.5	11.07	47.9	600
16	43.75	12	54.93	700
16	50	12.88	61.89	800
16	56.25	13.72	68.79	900
16	62.5	14.52	75.65	1000
16	75	16.05	89.26	1200
16	87.5	17.48	102.74	1400
16	100	18.86	116.12	1600
16	112.5	20.18	129.42	1800
16	125	21.47	142.64	2000
16	137.5	22.73	155.8	2200
16	150	23.96	168.9	2400
16	162.5	25.18	181.95	2600
16	175	26.39	194.96	2800
16	187.5	27.59	207.92	3000
16	218.75	30.59	240.16	3500
16	250	33.61	272.18	4000
16	281.25	36.71	304.01	4500
16	312.5	39.9	335.66	5000
16	343.75	43.25	367.15	5500
16	375	46.8	398.49	6000
18	16.67	6.86	23.35	300
18	22.22	7.94	29.9	400
18	27.78	8.91	36.33	500
18	33.33	9.79	42.66	600
18	38.89	10.61	48.92	700
18	44.44	11.38	55.13	800
18	50	12.11	61.28	900
18	55.56	12.8	67.4	1000
18	66.67	14.12	79.54	1200
18	77.78	15.35	91.57	1400
18	88.89	16.52	103.51	1600
18	100	17.65	115.38	1800
18	111.11	18.73	127.2	2000
18	122.22	19.79	138.95	2200
18	133.33	20.81	150.66	2400
18	144.44	21.82	162.33	2600
18	155.56	22.81	173.96	2800
18	166.67	23.79	185.55	3000
18	194.44	26.2	214.4	3500
18	222.22	28.57	243.08	4000
18	250	30.94	271.6	4500
18	277.78	33.33	300	5000
18	305.56	35.76	328.27	5500
18	333.33	38.25	356.44	6000
20	15	6.16	21.03	300
20	20	7.13	26.94	400
20	25	8	32.73	500
20	30	8.78	38.44	600
20	35	9.51	44.09	700
20	40	10.19	49.69	800
20	45	10.84	55.24	900
20	50	11.46	60.76	1000
20	60	12.62	71.71	1200
20	70	13.7	82.57	1400
20	80	14.72	93.35	1600
20	90	15.7	104.07	1800
20	100	16.64	114.73	2000
20	110	17.55	125.35	2200
20	120	18.44	135.93	2400
20	130	19.3	146.47	2600
20	140	20.14	156.98	2800
20	150	20.97	167.46	3000
20	175	22.99	193.54	3500
20	200	24.96	219.48	4000
20	225	26.9	245.3	4500
20	250	28.82	271.01	5000
20	275	30.74	296.62	5500
20	300	32.67	322.15	6000

NETWORK C_1

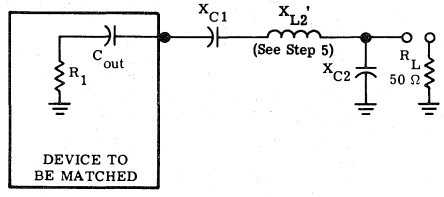
The following is a computer solution for an RF matching network. This computer solution is applicable for two forms of matching networks.



TO DESIGN A NETWORK USING THE TABLES

1. $X_{L1} = X_{C\,out}$.
2. Define Q, in column one, as X_{C1}/R_1.
3. All network values can now be read from the charts in terms of reactance.
4. This completes network C_1.

NETWORK C_2



TO DESIGN A NETWORK USING THE TABLES

1. L_1 is not used in this network.
2. Transform the impedance of the device to be matched to series form ($R_1 + jX_{C\,out}$).
3. Define Q, in column one, as X_{C1}/R_1.
4. For a desired Q, find the R_S to be matched in the R_1 column and read the reactive value of the components.
5. X_{L2}' is equal to the quantity X_{L2} obtained from the tables plus $|X_{C_{out}}|$.
6. This completes network C_2.

Q	X_{C1}	X_{C2}	X_{L2}	R_1
1	1	7.14	8	1
1	2	10.21	11.8	2
1	3	12.63	14.87	3
1	4	14.74	17.56	4
1	5	16.67	20	5
1	6	18.46	22.25	6
1	7	20.17	24.35	7
1	8	21.82	26.33	8
1	9	23.43	28.21	9
1	10	25	30	10
1	11	26.55	31.81	11
1	12	28.1	33.35	12
1	13	29.64	34.93	13
1	14	31.13	36.45	14
1	15	32.73	37.91	15
1	16	34.3	39.32	16
1	17	35.89	40.69	17
1	18	37.5	42	18
1	19	39.14	43.27	19
1	20	40.82	44.49	20
1	21	42.55	45.68	21
1	22	44.32	46.82	22
1	23	46.15	47.92	23
1	24	48.04	48.98	24
1	25	50	50	25
1	26	52.04	50.98	26
1	27	54.17	51.92	27
1	28	56.41	52.82	28
1	29	58.76	53.68	29
1	30	61.24	54.49	30
1	32	66.67	56	32
1	34	72.89	57.32	34
1	36	80.18	58.45	36
1	38	88.98	59.35	38
1	40	100	60	40
1	42	114.56	60.33	42
1	44	135.4	60.25	44
1	46	169.56	59.56	46
1	48	244.95	57.8	48
2	2	7.14	9	1
2	4	10.21	13.8	2
2	6	12.63	17.87	3
2	8	14.74	21.56	4
2	10	16.67	25	5
2	12	18.46	28.25	6
2	14	20.17	31.35	7
2	16	21.82	34.33	8
2	18	23.43	37.21	9
2	20	25	40	10
2	22	26.55	42.71	11
2	24	28.1	45.35	12
2	26	29.64	47.93	13
2	28	31.18	50.45	14
2	30	32.73	52.91	15
2	32	34.3	55.32	16
2	34	35.89	57.69	17
2	36	37.5	60	18
2	38	39.14	62.27	19
2	40	40.82	64.49	20
2	42	42.55	66.68	21
2	44	44.32	68.82	22
2	46	46.15	70.92	23
2	48	48.04	72.98	24
2	50	50	75	25
2	52	52.04	76.98	26
2	54	54.17	78.92	27
2	56	56.41	80.82	28
2	58	58.76	82.68	29
2	60	61.24	84.49	30
2	64	66.67	88	32
2	68	72.89	91.32	34
2	72	80.18	94.45	36
2	76	88.98	97.35	38
2	80	100	100	40
2	84	114.56	102.33	42
2	88	135.4	104.25	44
2	92	169.56	105.56	46
2	96	244.95	105.8	48
3	3	7.14	10	1
3	6	10.21	15.8	2
3	9	12.63	20.87	3
3	12	14.74	25.56	4
3	15	16.67	30	5
3	18	18.46	34.25	6
3	21	20.17	38.35	7
3	24	21.82	42.33	8
3	27	23.43	46.21	9
3	30	25	50	10
3	33	26.55	53.71	11
3	36	28.1	57.35	12
3	39	29.64	60.98	13
3	42	31.18	64.45	14
3	45	32.73	67.91	15
3	48	34.3	71.32	16
3	51	35.89	74.69	17
3	54	37.5	78	18
3	57	39.14	81.27	19

Q	X_{C1}	X_{C2}	X_{L2}	R_1
3	60	40.82	84.49	20
3	63	42.55	87.68	21
3	66	44.32	90.82	22
3	69	46.15	93.93	23
3	72	48.04	96.98	24
3	75	50	100	25
3	78	52.04	102.98	26
3	81	54.17	105.92	27
3	84	56.41	108.82	28
3	87	58.76	111.68	29
3	90	61.24	114.49	30
3	96	66.67	120	32
3	102	72.89	125.32	34
3	108	80.18	130.45	36
3	114	88.98	135.35	38
3	120	100	140	40
3	126	114.56	144.33	42
3	132	135.4	148.25	44
3	138	169.56	151.56	46
3	144	244.95	153.8	48
4	4	7.14	11	1
4	8	10.21	17.8	2
4	12	12.63	23.87	3
4	16	14.74	29.56	4
4	20	16.67	35	5
4	24	18.46	40.25	6
4	28	20.17	45.35	7
4	32	21.82	50.33	8
4	36	23.43	55.21	9
4	40	25	60	10
4	44	26.55	64.71	11
4	48	28.1	69.35	12
4	52	29.64	73.93	13
4	56	31.18	78.45	14
4	60	32.73	82.91	15
4	64	34.3	87.32	16
4	68	35.89	91.69	17
4	72	37.5	96	18
4	76	39.14	100.27	19
4	80	40.82	104.49	20
4	84	42.55	108.68	21
4	88	44.32	112.82	22
4	92	46.15	116.92	23
4	96	48.04	120.98	24
4	100	50	125	25
4	104	52.04	128.98	26
4	108	54.17	132.92	27
4	112	56.41	136.82	28
4	116	58.76	140.68	29
4	120	61.24	144.49	30
4	128	66.67	152	32
4	136	72.89	159.32	34
4	144	80.18	166.45	36
4	152	88.98	173.35	38
4	160	100	180	40
4	168	114.56	186.33	42
4	176	135.4	192.25	44
4	184	169.56	197.56	46
4	192	244.95	201.8	48
5	5	7.14	12	1
5	10	10.21	19.8	2
5	15	12.63	26.87	3
5	20	14.74	33.56	4
5	25	16.67	40	5
5	30	18.46	46.25	6
5	35	20.17	52.35	7
5	40	21.82	58.33	8
5	45	23.43	64.21	9
5	50	25	70	10
5	55	26.55	75.71	11

Q	X_{C1}	X_{C2}	X_{L2}	R_1
5	60	28.1	81.35	12
5	65	29.64	86.93	13
5	70	31.18	92.45	14
5	75	32.73	97.91	15
5	80	34.3	103.32	16
5	85	35.89	108.69	17
5	90	37.5	114	18
5	95	39.14	119.27	19
5	100	40.82	124.49	20
5	105	42.55	129.68	21
5	110	44.32	134.82	22
5	115	46.15	139.92	23
5	120	48.04	144.98	24
5	125	50	150	25
5	130	52.04	154.98	26
5	135	54.17	159.92	27
5	140	56.41	164.82	28
5	145	58.76	169.68	29
5	150	61.24	174.49	30
5	160	66.67	184	32
5	170	72.89	193.32	34
5	180	80.18	202.45	36
5	190	88.98	211.35	38
5	200	100	220	40
5	210	114.56	228.33	42
5	220	135.4	236.25	44
5	230	169.56	243.56	46
5	240	244.95	249.8	48
6	6	7.14	13	1
6	12	10.21	21.8	2
6	18	12.63	29.87	3
6	24	14.74	37.56	4
6	30	16.67	45	5
6	36	18.46	52.25	6
6	42	20.17	59.35	7
6	48	21.82	66.33	8
6	54	23.43	73.21	9
6	60	25	80	10
6	66	26.55	86.71	11
6	72	28.1	93.35	12
6	78	29.64	99.93	13
6	84	31.18	106.45	14
6	90	32.73	112.91	15
6	96	34.3	119.32	16
6	102	35.89	125.69	17
6	108	37.5	132	18
6	114	39.14	138.27	19
6	120	40.82	144.49	20
6	126	42.55	150.68	21
6	132	44.32	156.82	22
6	138	46.15	162.92	23
6	144	48.04	168.98	24
6	150	50	175	25
6	156	52.04	180.98	26
6	162	54.17	186.92	27
6	168	56.41	192.82	28
6	174	58.76	198.68	29
6	180	61.24	204.49	30
6	192	66.67	216	32
6	204	72.89	227.32	34
6	216	80.18	238.45	36
6	228	88.98	249.35	38
6	240	100	260	40
6	252	114.56	270.33	42
6	264	135.4	280.25	44
6	276	169.56	289.56	46
6	288	244.95	297.8	48
7	7	7.14	14	1
7	14	10.21	23.8	2
7	21	12.63	32.87	3

Q	X_{C1}	X_{C2}	X_{L2}	R_1
7	28	14.74	41.56	4
7	35	16.67	50	5
7	42	18.46	58.25	6
7	49	20.17	66.35	7
7	56	21.82	74.33	8
7	63	23.43	82.21	9
7	70	25	90	10
7	77	26.55	97.71	11
7	84	28.1	105.35	12
7	91	29.64	112.93	13
7	98	31.18	120.45	14
7	105	32.73	127.91	15
7	112	34.3	135.32	16
7	119	35.89	142.69	17
7	126	37.5	150	18
7	133	39.14	157.27	19
7	140	40.82	164.49	20
7	147	42.55	171.68	21
7	154	44.32	178.82	22
7	161	46.15	185.92	23
7	168	48.04	192.98	24
7	175	50	200	25
7	182	52.04	206.98	26
7	189	54.17	213.92	27
7	196	56.41	220.82	28
7	203	58.76	227.68	29
7	210	61.24	234.49	30
7	224	66.67	248	32
7	238	72.89	261.32	34
7	252	80.18	274.45	36
7	266	88.98	287.35	38
7	280	100	300	40
7	294	114.56	312.33	42
7	308	135.4	324.25	44
7	322	169.56	335.56	46
7	336	244.95	345.8	48
8	8	7.14	15	1
8	16	10.21	25.8	2
8	24	12.63	35.87	3
8	32	14.74	45.56	4
8	40	16.67	55	5
8	48	18.46	64.25	6
8	56	20.17	73.35	7
8	64	21.82	82.33	8
8	72	23.43	91.21	9
8	80	25	100	10
8	88	26.55	108.71	11
8	96	28.1	117.35	12
8	104	29.64	125.93	13
8	112	31.18	134.45	14
8	120	32.73	142.91	15
8	128	34.3	151.32	16
8	136	35.89	159.69	17
8	144	37.5	168	18
8	152	39.14	176.27	19
8	160	40.82	184.49	20
8	168	42.55	192.68	21
8	176	44.32	200.82	22
8	184	46.15	208.92	23
8	192	48.04	216.98	24
8	200	50	225	25
8	208	52.04	232.98	26
8	216	54.17	240.92	27
8	224	56.41	248.82	28
8	232	58.76	256.68	29
8	240	61.24	264.49	30
8	256	66.67	280	32
8	272	72.89	295.32	34
8	288	80.18	310.45	36
8	304	88.98	325.35	38

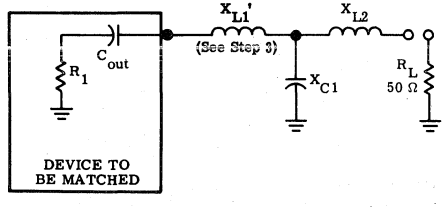
Q	X_{C1}	X_{C2}	X_{L2}	R_1
8	320	100	340	40
8	336	114.56	354.33	42
8	352	135.4	368.25	44
8	368	169.56	381.56	46
8	384	244.95	393.8	48
9	9	7.14	16	1
9	18	10.21	27.8	2
9	27	12.63	38.87	3
9	36	14.74	49.56	4
9	45	16.67	60	5
9	54	18.46	70.25	6
9	63	20.17	80.35	7
9	72	21.82	90.33	8
9	81	23.43	100.21	9
9	90	25	110	10
9	99	26.55	119.71	11
9	108	28.1	129.35	12
9	117	29.64	138.93	13
9	126	31.18	148.45	14
9	135	32.73	157.91	15
9	144	34.3	167.32	16
9	153	35.89	176.69	17
9	162	37.5	186	18
9	171	39.17	195.27	19
9	180	40.82	204.49	20
9	189	42.55	213.68	21
9	198	44.32	222.82	22
9	207	46.15	231.92	23

Q	X_{C1}	X_{C2}	X_{L2}	R_1
9	414	169.56	427.56	46
9	432	244.95	441.8	48
9	216	48.04	240.98	24
9	225	50	250	25
9	234	52.04	258.98	26
9	243	54.17	267.92	27
9	252	56.41	276.82	28
9	261	58.76	285.88	29
9	270	61.24	294.49	30
9	288	66.67	312	32
9	306	72.89	329.32	34
9	324	80.18	346.45	36
9	342	88.98	363.35	38
9	360	100	380	40
9	378	114.56	396.33	42
9	396	135.4	412.25	44
10	10	7.14	17	1
10	20	10.21	29.8	2
10	30	12.63	41.87	3
10	40	14.74	53.56	4
10	50	16.67	65	5
10	60	18.46	76.25	6
10	70	20.17	87.35	7
10	80	21.82	98.33	8
10	90	23.43	109.21	9
10	100	25	120	10
10	110	26.55	130.71	11

Q	X_{C1}	X_{C2}	X_{L2}	R_1
10	120	28.1	141.35	12
10	130	29.64	151.93	13
10	140	31.18	162.45	14
10	150	32.73	172.91	15
10	160	34.3	183.32	16
10	170	35.89	193.69	17
10	180	37.5	204	18
10	190	39.14	214.27	19
10	200	40.82	224.49	20
10	210	42.55	234.68	21
10	220	44.32	244.82	22
10	230	46.15	254.92	23
10	240	48.04	264.98	24
10	250	50	275	25
10	260	52.04	284.98	26
10	270	54.17	294.92	27
10	280	56.41	304.82	28
10	290	58.76	314.68	29
10	300	61.24	324.49	30
10	320	66.67	344	32
10	340	72.89	363.32	34
10	360	80.18	382.45	36
10	380	88.98	401.35	38
10	400	100	420	40
10	420	114.56	438.33	42
10	440	135.4	456.25	44
10	460	169.56	473.56	46
10	480	244.95	489.8	48

NETWORK D

The following is a computer solution for an RF "Tee" matching network.
Tuning is accomplished by using a variable capacitor for C_1. Variable matching may also be accomplished by increasing X_{L2} and adding an equal amount of X_C in series in the form of a variable capacitor.



TO DESIGN A NETWORK USING THE TABLES

1. Define Q, in column one, as X_{L1}/R_1.
2. For an R_1 to be matched and a desired Q, read the reactances of the network components from the charts.
3. X_{L1}' is equal to the quantity X_{L1} obtained from the tables plus $|X_{C_{out}}|$.
4. This completes the network.

Q	X_{L1}	X_{L2}	X_{C1}	R_1
1	26	10	43.33	26
1	27	14.14	42.09	27
1	28	17.32	41.59	28
1	29	20	41.43	29
1	30	22.36	41.46	30
1	32	26.46	41.85	32
1	34	30	42.5	34
1	36	33.17	43.29	36
1	38	36.06	44.16	38
1	40	38.72	45.08	40
1	42	41.23	46.04	42
1	44	43.59	47.01	44
1	46	45.83	48	46
1	48	47.96	49	48
1	50	50	50	50
1	55	54.77	52.49	55
1	60	59.16	54.96	60
1	65	63.25	57.4	65
1	70	67.08	69.79	70
1	75	70.71	62.13	75
1	80	74.16	64.43	80
1	85	77.46	66.69	85
1	90	80.62	68.9	90
1	95	83.67	71.07	95
1	100	86.6	73.21	100
1	125	100	83.33	125
1	150	111.8	92.71	150

Q	X_{L1}	X_{L2}	X_{C1}	R_1
1	175	122.47	101.46	175
1	200	132.29	109.72	200
1	225	141.42	117.54	225
1	250	150	125	250
1	275	158.11	132.14	275
1	300	165.83	139	300
2	22	15.81	23.75	11
2	24	22.36	24.52	12
2	26	27.39	25.51	13
2	28	31.62	26.59	14
2	30	35.36	27.7	15
2	32	38.73	28.83	16
2	34	41.83	29.96	17
2	36	44.72	31.09	18
2	38	47.43	32.22	19
2	40	50	33.33	20
2	42	52.44	34.44	21
2	44	54.77	35.54	22
2	46	57.01	36.62	23
2	48	59.16	37.7	24
2	50	61.24	38.76	25
2	52	63.25	39.82	26
2	54	65.19	40.86	27
2	56	67.08	41.9	28
2	58	68.92	42.92	29
2	60	70.71	43.93	30
2	64	74.16	45.93	32

Q	X_{L1}	X_{L2}	X_{C1}	R_1
2	68	77.46	47.9	34
2	72	80.62	49.83	36
2	76	83.67	51.72	38
2	80	86.6	53.59	40
2	84	89.44	55.43	42
2	88	92.2	57.23	44
2	92	94.87	59.01	46
2	96	97.47	60.77	48
2	100	100	62.5	50
2	110	106.07	66.73	55
2	120	111.8	70.82	60
2	130	117.26	74.8	65
2	140	122.47	78.66	70
2	150	127.48	82.43	75
2	160	132.29	86.1	80
2	170	136.93	89.69	85
2	180	141.42	93.2	90
2	190	145.77	96.63	95
2	200	150	100	100
2	250	169.56	115.93	125
2	300	187.08	130.62	150
2	350	203.1	144.34	175
2	400	217.94	157.26	200
2	450	231.84	169.51	225
2	500	244.95	181.19	250
2	550	257.39	192.37	275
2	600	269.26	203.11	300

Q	X_{L1}	X_{L2}	X_{C1}	R_1
3	18	22.36	17.41	6
3	21	31.62	19.27	7
3	24	38.73	21.19	8
3	27	44.72	23.11	9
3	30	50	25	10
3	33	54.77	26.86	11
3	36	59.16	28.69	12
3	39	63.25	30.48	13
3	42	67.08	32.25	14
3	45	70.71	33.98	15
3	48	74.16	35.69	16
3	51	77.46	37.37	17
3	54	80.62	39.02	18
3	57	83.67	40.66	19
3	60	86.6	42.26	20
3	63	89.44	43.85	21
3	66	92.2	45.42	22
3	69	94.87	46.96	23
3	72	97.47	48.49	24
3	75	100	50	25
3	78	102.47	51.49	26
3	81	104.88	52.97	27
3	84	107.24	54.42	28
3	87	109.54	55.87	29
3	90	111.8	57.29	30
3	96	116.19	60.11	32
3	102	120.42	62.87	34
3	108	124.5	65.57	36
3	114	128.45	68.23	38
3	120	132.29	70.85	40
3	126	136.01	73.42	42
3	132	139.64	75.96	44
3	138	143.18	78.45	46
3	144	146.63	80.91	48
3	150	150	83.33	50
3	165	158.11	89.25	55
3	180	165.83	94.99	60
3	195	173.21	100.56	65
3	210	180.28	105.97	70
3	225	187.08	111.25	75
3	240	193.65	116.4	80
3	255	200	121.43	85
3	270	206.16	126.35	90
3	285	212.13	131.17	95
3	300	217.94	135.89	100
3	375	244.95	158.25	125
3	450	269.26	178.89	150
3	525	291.55	198.17	175
3	600	312.25	216.33	200
3	675	331.66	233.57	225
3	750	350	250	250
3	825	367.42	265.74	275
3	900	384.06	280.87	300
4	12	7.07	12.31	3
4	16	30	14.78	4
4	20	41.83	17.57	5
4	24	50.99	20.32	6
4	28	58.74	23	7
4	32	65.57	25.6	8
4	36	71.76	28.15	9
4	40	77.46	30.64	10
4	44	82.76	33.07	11
4	48	87.75	35.45	12
4	52	92.47	37.78	13
4	56	96.95	40.07	14
4	60	101.24	42.32	15
4	64	105.36	44.54	16
4	68	109.32	46.72	17
4	72	113.14	48.86	18
4	76	116.83	50.97	19
4	80	120.42	53.06	20
4	84	123.9	55.11	21
4	88	127.28	57.14	22
4	92	130.58	59.14	23
4	96	133.79	61.12	24
4	100	136.93	63.07	25
4	104	140	65	26
4	108	143	66.91	27
4	112	145.95	68.8	28
4	116	148.83	70.67	29
4	120	151.66	72.51	30
4	128	157.16	76.16	32
4	136	162.48	79.73	34
4	144	167.63	83.24	36
4	152	172.63	86.68	38
4	160	177.48	90.07	40
4	168	182.21	93.4	42
4	176	186.82	96.69	44
4	184	191.31	99.92	46
4	192	195.7	103.11	48
4	200	200	106.25	50
4	220	210.36	113.93	55
4	240	220.23	121.36	60
4	260	229.67	128.59	65
4	280	238.75	135.61	70
4	300	247.49	142.46	75
4	320	255.93	148.15	80
4	340	264.1	155.68	85
4	360	272.03	162.07	90
4	380	279.73	168.32	95
4	400	287.23	174.46	100
4	500	322.1	203.5	125
4	600	353.55	230.33	150
4	700	382.43	255.4	175
4	800	409.27	279.02	200
4	900	434.45	301.44	225
4	1000	458.26	322.82	250
4	1100	480.88	343.3	275
4	1200	502.49	362.99	300
5	10	10	10	2
5	15	37.42	13.57	3
5	20	51.96	17.22	4
5	25	63.25	20.75	5
5	30	72.8	24.16	6
5	35	81.24	27.47	7
5	40	88.88	30.69	8
5	45	95.92	33.82	9
5	50	102.47	36.88	10
5	55	108.63	39.87	11
5	60	114.46	42.8	12
5	65	120	45.68	13
5	70	125.3	48.49	14
5	75	130.38	51.26	15
5	80	135.28	53.99	16
5	85	140	56.67	17
5	90	144.57	59.31	18
5	95	149	61.91	19
5	100	153.3	64.47	20
5	105	157.48	67	21
5	110	161.55	69.49	22
5	115	165.53	71.96	23
5	120	169.41	74.39	24
5	125	173.21	76.79	25
5	130	176.92	79.17	26
5	135	180.55	81.52	27
5	140	184.12	83.85	28
5	145	187.62	86.15	29
5	150	191.05	88.43	30
5	160	197.74	92.91	32
5	170	204.21	97.31	34
5	180	210.48	101.63	36
5	190	216.56	105.88	38
5	200	222.49	110.06	40
5	210	228.25	114.17	42
5	220	233.88	118.21	44
5	230	239.37	122.2	46
5	240	244.74	126.13	48
5	250	260	130	50
5	275	262.68	139.46	55
5	300	274.77	148.64	60
5	325	286.36	157.54	65
5	350	297.49	166.21	70
5	375	308.22	174.66	75
5	400	318.59	182.91	80
5	425	328.63	190.97	85
5	450	338.38	198.85	90
5	475	347.85	206.57	95
5	500	357.07	214.14	100
5	625	400	250	125
5	750	438.75	283.12	150
5	875	474.34	314.08	175
5	1000	507.44	343.26	200
5	1125	538.52	670.95	225
5	1250	567.89	397.36	250
5	1375	595.82	422.67	275
5	1500	622.49	446.99	300
6	12	34.64	11.06	2
6	18	55.23	15.62	3
6	24	70	20	4
6	30	82.16	24.2	5
6	36	92.74	28.26	6
6	42	102.23	32.2	7
6	48	110.91	36.02	8
6	54	118.95	39.74	9
6	60	126.49	43.38	10
6	66	133.6	46.93	11
6	72	140.36	50.41	12
6	78	146.8	53.83	13
6	84	152.97	57.18	14
6	90	158.9	60.47	15
6	96	164.62	63.71	16
6	102	170.15	66.89	17
6	108	175.5	70.03	18
6	114	180.69	73.12	19
6	120	185.74	76.17	20
6	126	190.66	79.18	21
6	132	195.45	82.15	22
6	138	200.12	85.08	23
6	144	204.69	87.97	24
6	150	209.17	90.83	25
6	156	213.54	93.66	26
6	162	217.83	96.46	27
6	168	222.04	99.23	28
6	174	226.16	101.96	29
6	180	230.22	104.67	30
6	192	238.12	110.01	32
6	204	245.76	115.25	34
6	216	253.18	120.39	36
6	228	260.38	125.45	38
6	240	267.39	130.42	40
6	252	274.23	135.31	42
6	264	280.89	140.13	44
6	276	287.4	144.88	46
6	288	293.77	149.55	48
6	300	300	154.17	50
6	330	315.04	165.44	55
6	360	329.39	176.36	60
6	390	343.15	186.97	65
6	420	356.37	197.3	70
6	450	369.12	207.36	75
6	480	381.44	217.19	80
6	510	393.38	226.79	85
6	540	404.97	236.18	90
6	570	416.23	245.38	95
6	600	427.2	254.4	100
6	750	478.28	297.13	125
6	900	524.4	336.61	150
6	1050	566.79	373.5	175
6	1200	606.22	408.29	200
6	1350	643.23	441.3	225
6	1500	678.23	472.79	250
6	1650	711.51	502.96	275
6	1800	743.3	531.96	300
7	14	50	12.5	2
7	21	70.71	17.83	3
7	28	86.6	22.9	4
7	35	100	27.78	5
7	42	111.8	32.48	6
7	49	122.47	37.04	7
7	56	132.29	41.47	8
7	63	141.42	45.79	9
7	70	150	50	10
7	77	158.11	54.12	11
7	84	165.83	58.16	12
7	91	173.21	62.12	13
7	98	180.28	66	14
7	105	187.08	69.82	15
7	112	193.65	73.58	16

Q	X_{L1}	X_{L2}	X_{C1}	R_1
7	119	200	77.27	17
7	126	206.16	80.91	18
7	133	212.13	84.5	19
7	140	217.94	88.04	20
7	147	223.61	91.53	21
7	154	229.13	94.97	22
7	161	234.52	98.37	23
7	168	239.79	101.73	24
7	175	244.95	105.05	25
7	182	250	108.33	26
7	189	254.95	111.58	27
7	196	259.81	114.79	28
7	203	264.58	117.97	29
7	210	269.26	121.11	30
7	224	278.39	127.31	32
7	238	287.23	133.39	34
7	252	295.8	139.36	36
7	266	304.14	145.23	38
7	280	312.25	151	40
7	294	320.16	156.68	42
7	308	327.87	162.27	44
7	322	335.41	167.78	46
7	336	342.78	173.21	48
7	350	350	178.57	50
7	385	367.42	191.66	55
7	420	384.06	204.34	60
7	455	400	216.67	65
7	490	415.33	228.66	70
7	525	430.12	240.35	75
7	560	444.41	251.76	80
7	595	458.86	262.91	85
7	630	471.7	273.82	90
7	665	484.77	284.51	95
7	700	497.49	294.99	100
7	875	556.78	344.63	125
7	1050	610.33	390.49	150
7	1225	659.55	433.36	175
7	1400	705.34	473.78	200
7	1575	748.33	512.14	225
7	1750	788.99	548.73	250
7	1925	827.65	583.79	275
7	2100	864.58	617.5	300
8	8	27.39	7.6	1
8	16	63.25	14.03	2
8	24	85.15	20.1	3
8	32	102.47	25.87	4
8	40	117.26	31.42	5
8	48	130.38	36.77	6
8	56	142.3	41.95	7
8	64	153.3	46.99	8
8	72	163.55	51.9	9
8	80	173.21	56.7	10
8	88	182.35	61.39	11
8	96	191.05	65.98	12
8	104	199.37	70.49	13
8	112	207.36	74.91	14
8	120	215.06	79.26	15
8	128	222.49	83.54	16
8	136	229.67	87.74	17
8	144	236.64	91.89	18
8	152	243.41	95.97	19
8	160	250	100	20
8	168	256.42	103.97	21
8	176	262.68	107.9	22
8	184	268.79	111.77	23
8	192	274.77	115.59	24
8	200	280.62	119.38	25
8	208	286.36	123.11	26
8	216	291.98	126.81	27
8	224	297.49	130.47	28
8	232	302.9	134.09	29
8	240	308.22	137.67	30

Q	X_{L1}	X_{L2}	X_{C1}	R_1
8	256	318.59	144.73	32
8	272	328.63	151.65	34
8	288	338.38	158.46	36
8	304	347.85	165.14	38
8	320	357.07	171.71	40
8	336	366.06	178.18	42
8	352	374.83	184.56	44
8	368	383.41	190.83	46
8	384	391.79	197.02	48
8	400	400	203.13	50
8	440	419.82	218.04	55
8	480	438.75	232.49	60
8	520	456.89	246.53	65
8	560	474.34	260.2	70
8	600	491.17	273.52	75
8	640	507.44	286.52	80
8	680	523.21	299.23	85
8	720	538.52	311.66	90
8	760	553.4	323.84	95
8	800	567.89	335.78	100
8	1000	635.41	392.36	125
8	1200	696.42	444.63	150
8	1400	752.5	493.49	175
8	1600	804.67	539.57	200
8	1800	853.67	583.29	225
8	2000	900	625	250
8	2200	944.06	664.96	275
8	2400	986.15	703.38	300
9	9	40	8.37	1
9	18	75.5	15.6	2
9	27	98.99	22.4	3
9	36	117.9	28.88	4
9	45	134.16	35.09	5
9	54	148.66	41.09	6
9	63	161.86	46.91	7
9	72	174.07	52.56	8
9	81	185.47	58.07	9
9	90	196.21	63.45	10
9	99	206.4	68.71	11
9	108	216.1	73.86	12
9	117	225.39	78.92	13
9	126	234.31	83.88	14
9	135	242.9	88.76	15
9	144	251.2	93.55	16
9	153	259.23	98.28	17
9	162	267.02	102.93	18
9	171	274.59	107.51	19
9	180	281.96	112.03	20
9	189	289.14	116.49	21
9	198	296.14	120.89	22
9	207	302.99	125.23	23
9	216	309.68	129.53	24
9	225	316.23	133.77	25
9	234	322.65	137.97	26
9	243	328.94	142.12	27
9	252	335.11	146.22	28
9	261	341.17	150.28	29
9	270	347.13	154.3	30
9	288	358.75	162.23	32
9	306	370	170	34
9	324	380.92	177.63	36
9	342	391.54	185.14	38
9	360	401.87	192.52	40
9	378	411.95	199.78	42
9	396	421.78	206.93	44
9	414	431.39	213.98	46
9	432	440.79	220.93	48
9	450	450	227.78	50
9	495	472.23	244.52	55
9	540	493.46	260.74	60
9	585	513.81	276.51	65
9	630	533.39	291.85	70

Q	X_{L1}	X_{L2}	X_{C1}	R_1
9	675	552.27	306.8	75
9	720	570.53	321.4	80
9	765	588.22	335.67	85
9	810	605.39	349.63	90
9	855	622.09	363.31	95
9	900	638.36	376.71	100
9	1125	714.14	440.24	125
9	1350	782.62	498.94	150
9	1575	845.58	553.81	175
9	1800	904.16	605.54	200
9	2025	959.17	654.64	225
9	2250	1011.19	701.48	250
9	2475	1060.66	746.36	275
9	2700	1107.93	789.51	300
10	10	50.5	9.17	1
10	20	87.18	17.2	2
10	30	112.47	24.74	3
10	40	133.04	31.91	4
10	50	150.83	38.8	5
10	60	166.73	45.45	6
10	70	181.25	51.89	7
10	80	194.68	58.16	8
10	90	207.24	64.26	9
10	100	219.09	70.23	10
10	110	230.33	76.06	11
10	120	241.04	81.78	12
10	130	251.3	87.38	13
10	140	261.15	92.89	14
10	150	270.65	98.29	15
10	160	279.82	103.61	16
10	170	288.7	108.85	17
10	180	297.32	114.01	18
10	190	305.7	119.09	19
10	200	313.85	124.1	20
10	210	321.79	129.05	21
10	220	329.55	133.93	22
10	230	337.12	138.75	23
10	240	344.53	143.51	24
10	250	351.78	148.22	25
10	260	358.89	152.87	26
10	270	365.86	157.47	27
10	280	372.69	162.03	28
10	290	379.41	166.53	29
10	300	386.01	170.99	30
10	320	398.87	179.78	32
10	340	411.34	188.4	34
10	360	423.44	196.87	36
10	380	435.2	205.2	38
10	400	446.65	213.38	40
10	420	457.82	221.44	42
10	440	468.72	229.37	44
10	460	479.37	237.19	46
10	480	489.8	244.9	48
10	500	500	252.5	50
10	550	524.64	271.07	55
10	600	548.18	289.07	60
10	650	570.75	306.56	65
10	700	592.45	323.58	70
10	750	613.39	340.18	75
10	800	633.64	356.37	80
10	850	653.26	372.21	85
10	900	672.31	387.7	90
10	950	690.83	402.87	95
10	1000	708.87	417.74	100
10	1250	792.94	488.23	125
10	1500	868.91	553.36	150
10	1750	938.75	614.25	175
10	2000	1003.74	671.66	200
10	2250	1064.78	726.14	225
10	2500	1122.5	778.12	250
10	2750	1177.39	827.92	275
10	3000	1229.84	875.8	300

Prepared by:
Roy Hejhall

SYSTEMIZING RF POWER AMPLIFIER DESIGN

INTRODUCTION

Two of the most popular RF small signal design techniques are:

1) the use of two port parameters, and
2) the use of some type of equivalent circuit for the transistor.

Early attempts to adapt these techniques to power amplifier design led to poor results and frustration.

In the mid-1960's, Motorola pioneered the concept of solid state power amplifier design through the use of large signal transistor input and output impedances. This system has since achieved almost universal acceptance by solid state communications equipment manufacturers. It provides a systematic design procedure to replace what used to be a trial and error process. This note is a description of the concept and its use in transmitter design.

LIMITATIONS OF SMALL-SIGNAL PARAMETERS

As a vivid example to show the short-comings of trying to adapt small-signal parameters to power amplifier design, the 2N3948 transistor was considered. A performance comparison was made of the 2N3948 operating at 300 MHz as a Class A small-signal amplifier, and as a Class C* power amplifier delivering a power output of 1 W. Table I shows the results of this comparison.

	CLASS A Small-signal amplifier V_{CE} = 15 Vdc; I_C = 80 mA; 300 MHz	CLASS C Power amplifier V_{CE} = 13.6 Vdc; P_o = 1 W
Input resistance	9 Ohms	38 Ohms
Input capacitance or inductance	0.012 μH	21 pF
Transistor output resistance	199 Ohms	92 Ohms
Output capacitance	4.6 pF	5.0 pF
G_{PE}	12.4 dB	8.2 dB

Table I — Small- and large-signal performance data for the 2N3948 show the inadequacy of using small-signal characterization data for large-signal amplifier design. Resistances and reactances shown are parallel components. That is, the large-signal input impedance is 38 ohms in parallel with 21 pF, etc.

The most striking difference in this comparison is in the device input impedance. As operation is changed from small-signal to large-signal conditions, the complex input impedance of the 2N3948 undergoes a considerable change in magnitude and actually changes from inductive to capacitive reactance.

Note also that the transistor's output resistances and power gains are considerably different for the two modes of operation. This example clearly demonstrates the inaccuracies that would result in a power-amplifier design based on the small-signal parameters of this device.

IMPORTANCE OF LARGE-SIGNAL PARAMETERS

The network theory for power amplifier design is well known but is useless unless the designer has valid input and output impedance data for the transistor. The design method described in this report hinges primarily on the direct measurement of these parameters for use in network synthesis equations. Large-signal impedance data, together with power output and gain data, provide the designer with the information necessary to design his amplifier networks and to predict the performance that should be achieved when the design is completed.

A clear understanding of the test conditions and method of presentation for the large signal impedance data is important.

TEST CONDITIONS

The term "large-signal input impedance" and "large-signal output impedance" refer to the actual transistor terminal impedances when operating in a matched amplifier at the desired RF power output level and dc supply voltage.

"Matched" is defined as the condition where the input and output networks of the test amplifier provide a conjugate match to the transistor, such that the input and output impedances of the amplifier are 50 + j 0 ohms.

Large-signal impedances should not be confused with small-signal, two port parameters which are normally measured at low signal levels with Class A bias and the transistor (or IC) connected directly to a short, open, or 50 ohm termination.

Most of the data which appears on Motorola RF power transistor data sheets is measured in common emitter, Class C amplifiers; as this condition covers the majority of device applications.

One significant exception to this involves transistors characterized for Class B linear power amplifier service. Examples of such transistors are the Motorola 2N5941-2 series. Since these transistors are designed specifically for linear service, their large-signal impedances were measured in a linear power amplifier test circuit with a two tone test signal instead of the conventional single frequency signal. For further information on these transistors see the

*Class C, as used here, refers to operation with both the emitter and base at dc ground potential and with the collector supply as the only dc voltage applied, regardless of resulting device conduction angle. Usually, the emitter is connected directly to chassis ground and the base is dc grounded through an inductive network element or choke.

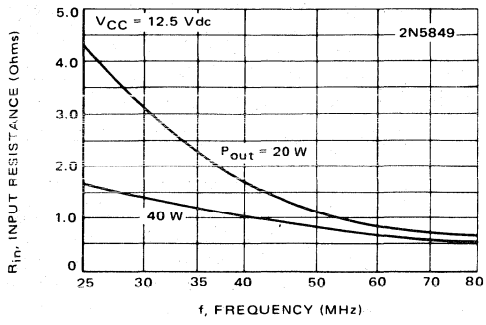


FIGURE 1 – Parallel Equivalent Input Resistance versus Frequency

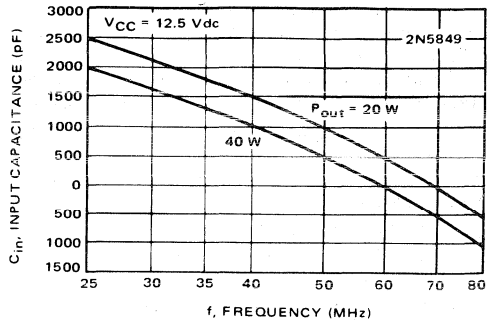


FIGURE 2 – Parallel Equivalent Input Capacitance versus Frequency

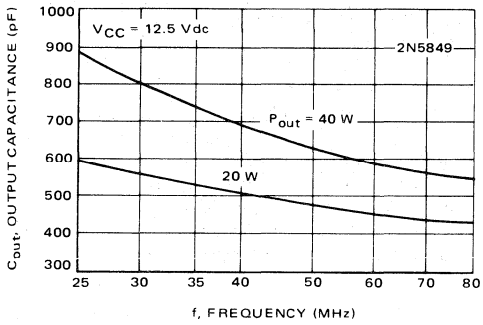


FIGURE 3 – Parallel Equivalent Output Capacitance versus Frequency

Motorola 2N5941-2 data sheet.

DATA FORMAT

Much of the information on device data sheets is presented in parallel equivalent form of resistance and capacitance. Figures 1-3 form an example of this type of presentation. The data may also be presented in series equivalent form. It makes no difference which form is used as long as the designer pays particular attention to the form and uses the data accordingly. As a convenience, the series-parallel equivalent conversion equations are given in Appendix A.

For example, reading the complex input impedance, from Figures 1 and 2 at 50 MHz with 40 W output and a 12.5 Vdc collector supply, we obtain a value of 0.8 ohms resistance in parallel with a 500 pF capacitance.

Another form of impedance data presentation uses the series equivalent form plotted on a Smith Chart. This form is popular with UHF power transistors due to the extensive use of the Smith Chart in microstrip network synthesis. Figure 4 is an example of large-signal impedances plotted on a Smith Chart plot. Note that Figure 4 includes complete complex output impedance data, not just the output capacitance. This topic is discussed more fully in the section on collector load resistance.

AMPLIFIER DESIGN

After selection of a transistor with the required performance capabilities, the next step in the design of a power amplifier is to determine the large-signal input and output impedances of the transistor. When using devices for which the data is available, this step involves nothing more than reading the complex impedance values off of the data sheet. If only output capacitance is given on the data sheet, the collector load resistance may be calculated in the manner described in the Collector Load Resistance Section of this note.

Again, the designer is cautioned to carefully determine whether the data sheet impedance curves are in parallel or series equivalent form, and to use the data accordingly. If the data is not available, a later section of this note contains information on large-signal impedance measurement.

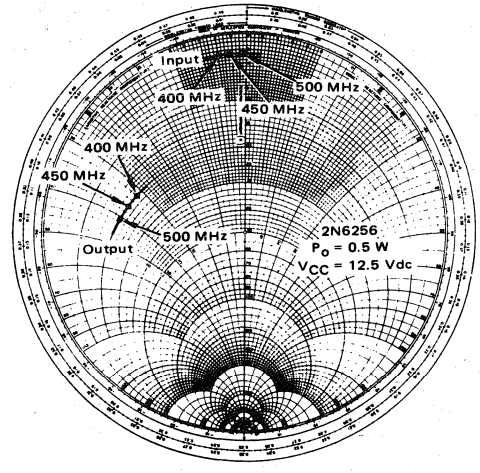


FIGURE 4 – Large Signal Input and Output Series Impedances, 2N6256

Having determined the large-signal impedances, the designer selects a suitable network configuration and proceeds with his network synthesis.

The primary purpose of this note is to describe the large-signal impedance concept. Accordingly, network selection and synthesis are beyond the scope of this discussion. For specific transmitter design examples using this concept, the reader is referred to the following Motorola Application Note: AN-548A.

COLLECTOR LOAD RESISTANCE

Large-signal impedance data at HF and VHF have for the most part been published by Motorola without collector load resistance information. The reason is that the load resistance can easily be calculated. The conditions necessary to obtain this load resistance derivation will now be discussed.

If certain simplifying assumptions are made, the theoretical collector voltage of a power amplifier with a tuned output network is a sine wave which swings from zero to 2 V_{CC}, where V_{CC} is the dc collector supply voltage. These assumptions include:

1. $V_{CE(sat)}$ is equal to zero.
2. The output network has sufficient loaded Q to produce a sine wave voltage regardless of transistor conduction angle.
3. The voltage drop in the dc collector supply feed system is zero.
4. The collector load impedance at all harmonics of the operating frequency is zero.

Obviously none of the foregoing assumptions is true, and the most serious discrepancies probably arise from assumptions 1 and 4. However, conditions are close enough to give good results.

Let us assume for a moment that this theoretical condition does exist. The parallel equivalent collector load resistance, R_L', then becomes a function of desired RF output power and V_{CC} only. The expression for R_L' given in equation 1 is readily derived.

$$R_L' = \frac{(V_{CC})^2}{2P} \qquad (1)$$

where P = RF output power

Therefore, the complex collector load impedance for an amplifier design would be the conjugate of the parallel equivalent output capacitance and collector load resistance computed with Equation 1.

Figure 5 provides a graphic solution to Equation 1 for the four popular dc supply levels of 12.5, 13.6, 24 and 28 volts.

Despite the assumptions required, experience with HF and VHF lumped-component, power amplifiers with supply voltages from 7 to 30 Vdc and power output levels from a few tenths of a watt to 300 watts have proven that the use of Equation 1 to compute R_L' for network synthesis yields good results. That is to say, the types of HF and VHF lumped component collector output networks which

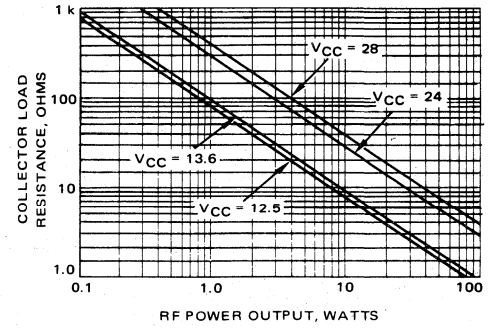


FIGURE 5 – Collector Load Resistance versus Power Output

have proved best from the standpoint of proper impedance matching with low losses and smooth tuning generally have a sufficient tuning and matching range to compensate for any errors associated with Equation 1.

Of course if the $V_{CE(sat)}$ of the transistor is accurately known for the frequency of operation and collector current swings anticipated in a particular amplifier, Equation 1 is readily modified as follows:

$$R_L' = \frac{(V_{CC}-V_{CE(sat)})^2}{2P} \qquad (2)$$

The advent of greatly increased numbers of UHF power transistors and their associated amplifier design problems brought some revisions to Motorola's methods of presenting large-signal transistor impedances for UHF devices. Among the reasons for this are the popularity of microstrip matching networks and the higher $V_{CE(sat)}$ values at UHF.

The major difference in the data format involves output impedance, which is presented in full complex form instead of plotting parallel equivalent output capacitance only and using Equation 1 to compute the load resistance. Further, the UHF devices are measured in a microstrip test amplifier for the purpose of determining the transistor impedances in an environment which is as close as possible to that of the majority of the actual applications of the device. And finally, a Smith Chart plot is used as this is more convenient to the microstrip network designer, who often makes extensive use of the Smith Chart as a design tool.

Future Motorola data sheets may also include collector load resistance data at frequencies below UHF. The information is automatically generated for the test circuit in use while measuring C_{in}, R_{in} and C_{out}.

PARAMETER MEASUREMENT

Although design engineers will find large-signal impedance characterization on Motorola data sheets for RF power transistors, it may help to know how this data is obtained. The transistor is placed in a test circuit designed to provide wide tuning capabilities. Design of the first

6

test amplifier for a new transistor type is based on estimates of input and output impedance.

Since the input and output impedances are needed to design an amplifier which is then used to measure the impedances of the device, we have a "chicken or the egg" type of problem. Wide tuning range networks help compensate for errors in the impedance estimates and they also permit the same characterization amplifier to be used at multiple power output levels.

The amplifier is tuned for a careful impedance match at both input and output. Several precautions are in order to insure that this is accomplished.

Tuning for maximum power output is valid only if the source and load impedances are an accurate 50 + j 0 ohms. Usually a good 50 ohm load is available in the laboratory. Such a load should be used, as tuning for maximum output power for a given input power is the best method to use on the amplifier output network.

The input network poses some additional problems. First, many laboratory RF power sources are not accurate 50 ohm generators. A generator impedance that is not 50 ohms can introduce errors in measuring gain as well as input impedances. In addition, a source with high harmonic levels can cause difficulties in low Q input networks.

A good solution to this problem is to use a dual directional coupler or directional power meter in the coax line between the generator and the test amplifier. The amplifier is then tuned for zero reflected power, thus indicating that the input network is really matching the transistor input impedance to 50 + j 0 ohms.

In practice, the reflected power usually will not null all the way to zero, so one should insure that the null is at least as deep as that obtained with a good 50 ohm passive termination.

In some cases, the amplifier will reflect enough harmonic power to prevent a satisfactory reflected power null from being obtained. A good solution to this problem is to place a fundamental frequency bandpass filter at the reflected power port of the dual directional coupler.

A typical test amplifier for HF and VHF measurements is shown in Figure 6. For UHF device characterization, amplifiers employing microstrip matching networks are most commonly employed.

After the test amplifier has been properly tuned, the dc power, signal source, circuit load, and test transistor are disconnected from the circuit. Then the signal source and output load circuit connections are each terminated with 50 ohms. After performing these substitutions, complex impedances are measured at the base and collector circuit connections of the test transistor (points A and B respectively in Figure 7). The desired data, the transistor input and output impedances, will be the conjugates of the base circuit connection and the collector circuit connection, impedances respectively.

By operating test amplifiers at several different frequencies with at least two power outputs, sufficient data can be obtained to characterize a transistor for the majority of its power applications.

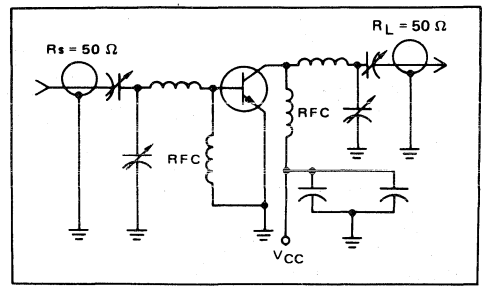


FIGURE 6 – Typical Test Amplifier Circuit

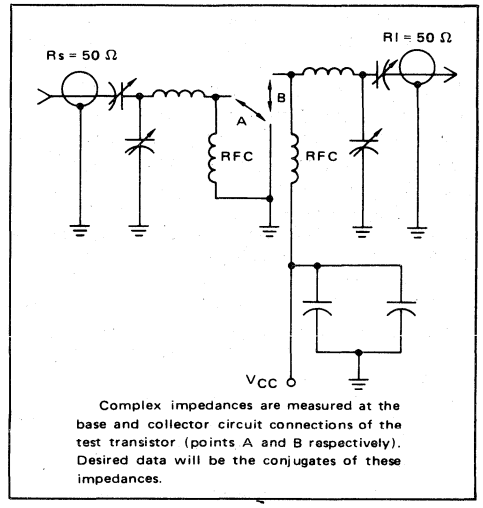


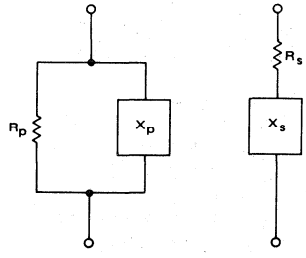
FIGURE 7 – Test Circuit with Transistor Removed

SUMMARY

The large-signal impedance characterization of RF power transistors has provided the most systematic and successful power amplifier design method the author has encountered since the concept was explored in depth in the mid 1960's.

APPENDIX A

PARALLEL-TO-SERIES AND SERIES-TO-PARALLEL IMPEDANCE CONVERSION EQUATIONS.



$$R_p = R_s \left[1 + \left(\frac{X_s}{R_s}\right)^2\right]$$

$$X_p = \frac{R_p \cdot R_s}{Xs}$$

$$R_s = \frac{R_p}{1 + \left(\frac{R_p}{X_p}\right)^2}$$

$$X_s = \frac{R_s \cdot R_p}{X_p}$$

UHF AMPLIFIER DESIGN USING DATA SHEET DESIGN CURVES

INTRODUCTION

The design of UHF amplifiers usually involves a particular set of device parameters of which h, y, and s parameters are probably the most familiar. These parameters are commonly used to determine device loading (input and output) admittances for particular gain and stability criteria. The design procedure for determining gain and stability usually involves a mathematical solution, a graphical approach, or a combination of both.

This report describes a design technique for the unneutralized case whereby the device loading admittances are taken directly from device design curves. An example is given of how these design parameters are used to design a single stage 1 GHz microstrip amplifier and predicted results are compared to actual measured values. Practical circuit construction techniques are also discussed for the benefit of readers unfamiliar with microstrip techniques.

STABILITY CONSIDERATIONS

Two very important methods[1] for expressing stability involve Linvill's stability factor "C" and Stern's stability factor "k". The first deals primarily with the device since an open termination is assumed on both the input and output and is formulated:

$$C = \frac{|y_{12}y_{12}|}{2g_{11}g_{22} - Re(y_{12}y_{21})}.$$

If "C" is greater than 1, the transistor is potentially unstable. However, if C is less than 1, the transistor is unconditionally stable. The C factor versus frequency for the common base and common emitter configurations (2N4957) are shown in Figures 10 and 17 respectively.

The second method is primarily circuit oriented and is used to compute the relative stability of an actual amplifier circuit for the particular source and load terminations used. If "k" is greater than 1, the circuit is stable. If "k" is less than 1 the circuit is potentially unstable

Stern has developed equations for calculating the input and output loading admittances for maximum power gain with a particular stability factor, k. These values of input and output admittances in conjunction with the device parameters can then be used to calculate the transducer gain.[1]

$$k = \frac{2(g_{11}+G_s)(g_{22}+G_L)}{|y_{12}y_{21}| + Re(y_{12}y_{21})}$$

$$G_s = \sqrt{\frac{k[|y_{12}y_{21}| + Re(y_{12}y_{21})]}{2}}\sqrt{\frac{g_{11}}{g_{22}}} - g_{11}$$

$$G_L = \sqrt{\frac{k[|y_{12}y_{21}| + Re(y_{12}y_{21})]}{2}}\sqrt{\frac{g_{22}}{g_{11}}} - g_{22}$$

$$B_s = \frac{(G_s+g_{11})Z_o}{\sqrt{k[|y_{12}y_{21}| + Re\ y_{12}y_{21}]}} - b_{11}$$

$$B_L = \frac{(G_L+g_{22})Z_o}{\sqrt{k[|y_{12}y_{21}| + Re(y_{12}y_{21})]}} - b_{22}$$

Where,

$$Z = \frac{(B_s+b_{11})(G_L+g_{22}) + (B_L+b_{22})k(L+M)/2(G_L+g_{22})}{\sqrt{k(L+M)}}$$

$$L = |y_{12}y_{21}|$$

$$M = Re(y_{12}y_{21})$$

Defining D as the denominator in G_T expression yields:

$$D = \frac{Z^4}{4} + \frac{[k(L+M)+2M]\ Z^2}{2} - 2NZ\sqrt{k(L+M)} + A^2 + N^2$$

where,

$$A = \frac{k(L+M)}{2} - M,$$

$$N = Im(y_{12}y_{21}),$$

and,

Z_o = that real value of Z which results in the smallest minimum of D, found by setting,

$$\frac{dD}{dZ} = Z^3 + [k(L+M)+2M]\ Z - 2N\sqrt{k(L+M)}.$$

equal to zero.

$$G_T = \frac{4\,Re(Y_s)\,Re(Y_L)\,|y_{21}|^2}{|(y_{11}+Y_s)(y_{22}+Y_L) - y_{12}y_{21}|^2}$$

k	=	Stern's stability factor
G_s	=	Real part of the source admittance
G_L	=	Real part of the load admittance
B_s	=	Imaginary part of the source admittance
B_L	=	Imaginary part of the load admittance
g_{11}	=	Real part of y_{11}
g_{22}	=	Real part of y_{22}
Y_L	=	Complex load admittance
Y_s	=	Complex source admittance
G_T	=	Transducer gain
Y_{IN}	=	Input admittance
Y_{OUT}	=	Output admittance
G_{max}	=	Maximum gain without feedback

6

Computer solutions of these equations for various values of k versus frequency have been plotted in Appendix I for the 2N4957. These curves include common-base (Figures 10 through 16) and common-emitter (Figures 17 through 22).

From these curves, the designer can determine the input and output loading admittances for maximum power gain at a particular circuit stability. In addition, the transducer power gain under these conditions can also be determined. Thus the designer, rather than reading s or y parameters from a curve and using this information to design an amplifier, has all the design equations solved and presented in convenient, computer-derived design curves.

The following example demonstrates how these curves can be utilized in the design of a 1 GHz amplifier using the 2N4957. In addition, a second example is shown to demonstrate the special case where input admittance is determined primarily by noise figure considerations rather than by maximum power gain.

1 GHz AMPLIFIER DESIGN

A preliminary investigation of stability and power gain, common-emitter and common-base, can be quickly made from the design curves. For instance, the unilateralized gain (Figure 8) at 1 GHz is approximately 15 dB for either the common-emitter or common-base configuration. Also, the C factor for the common-base configuration (Figure 10) is greater than one and indicates potential device instability. However, the C factor for the common-emitter configuration (Figure 17) is less than one and indicates unconditional device stability.

Figures 16 and 22 are key curves that show transducer power gain for the common base and common emitter configuration respectively. Assuming a circuit stability factor of 4*, power gain is approximately 15 dB, common-base. Although the common-emitter curve is not extended to 1 GHz (since this is a region of unconditional stability) power gain for k = 4 would be obviously much less than 15 dB.

Using the common base configuration with k = 4, the required input and output admittance for maximum power gain can be determined directly from Figures 11 through 16.

For instance, the real part of the output admittance can be read from either Figure 11 or 12. Figure 12 is an expanded version of Figure 11 and is intended to facilitate lower frequency use. The imaginary portion of the output admittance is shown in Figure 13. Figures 14 and 15 show the real and imaginary portions of the input admittance respectively. The resultant input and output admittances are shown in Figure 1 and are summarized:

Conditions: (2N4957)

V_{CE} = 10 V
I_C = 2 mA
f = 1 GHz
G_T = 15 dB
k = 4

Input admittance = 69.5 mmhos +j27.1 mmhos
Output admittance = 1.53 mmhos –j7.46 mmhos

It becomes apparent that the emitter must "see" an admittance of 69.5 mmhos shunted by a susceptance of +j27.1 mmhos. The latter, in terms of a lumped constant element, would be a lossless capacitor. Likewise, the collector would be required to see an admittance of 1.53 mmhos shunted by –j7.46 mmhos. The latter, in terms of a lumped-constant element, would be a lossless coil. This loading will result in a stability factor, k, of 4 and a power gain of 15 dB, the maximum power gain possible for k = 4. This loading does not include stray capacitance. If stray capacitance is assumed to be 1 pF, the actual load is 1.53 mmhos –j13.5 mmhos (see Figure 1).

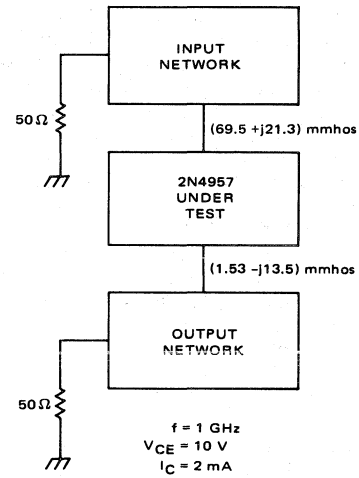


FIGURE 1 – COMMON BASE INPUT AND OUTPUT ADMITTANCES INCLUDING STRAY CAPACITANCE

To facilitate instrumentation, both the source and load impedance will be 50 ohms. This admittance level must be transformed to the required device loading admittance. Micro strip techniques provide a convenient method of achieving this transformation without circuit reproducibility and component loss problems that are common with many lumped constant circuits at this frequency.

The Smith Chart is a convenient design tool for solving transmission line problems of this type. Since space does not permit, familiarity with this chart will be assumed.

*For the purpose of this report a stability factor of 4 is chosen. Values of k less than 4 may not prove to be advantageous from the standpoint of regeneration and parameter spread.

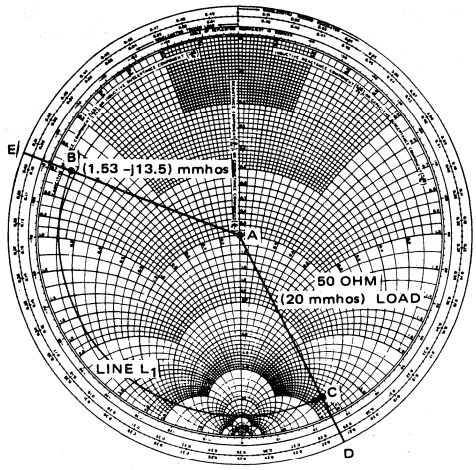


FIGURE 2 – OUTPUT NETWORK DESIGN

Starting with the output circuit, both the 50 ohm (20 mmhos) load and the desired collector admittance are plotted on the Smith Chart (see Figure 2). As a starting point, a characteristic admittance of 20 mmhos will be assumed. First, the 20 mmho load is plotted (point A, Figure 2), then point B is plotted (1.53 mmhos -j13.5 mmhos).

Although many different methods exist for transforming point A to point B (see Figure 2), a direct, and as it turns out, practical approach is that shown in Figure 3. This circuit uses C_1 in parallel with R_L to vary the SWR of point A (Figure 2) to point C. Since point C has the same SWR as point B, a line L_1 with an electrical length equal to $0.405\lambda_2$ (point E) minus 0.214λ (point D) will complete the transformation. Collector tuning is available with component C_2. This variable capacitor provides the difference between the assumed stray capacitance and the actual circuit stray capacitance.

The required SWR could have been realized by using an inductor in place of C_1. However, an inductor would have either forced the bias feed-point to be changed to the collector lead or necessitated a dc- isolated coil. Although this is readily attainable using transmission line techniques, the variable component C_1 is more convenient. A typical curve of Q versus capacitance for (C_1) is shown in Figure 4.

The output bias is fed through a 4000 ohm resistor rather than an RF choke. The resultant 8 volt drop across this resistor is easier to contend with than the circuit instabilities sometimes associated with RF chokes.

The same procedure is followed in designing the input network (see Figure 5). Again, a stray capacitance of 1 pF is assumed. Thus, the actual input loading becomes 69.5 mmhos +j21.3 mmhos. First, the 20 mmho load is plotted (see Point T, Figure 6). Next, point W is plotted (69.5 mmhos +j21.3 mmhos). Adjusting the SWR with C_3 (point V) allows a transmission line of length L_2 to transform the admittance at point V to the desired level at the base (point W).

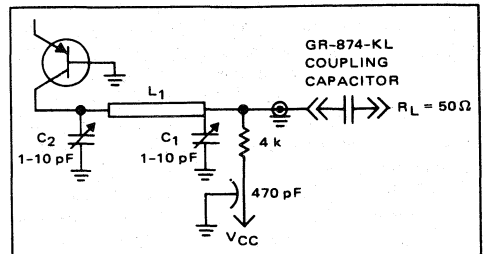


FIGURE 3 – OUTPUT NETWORK

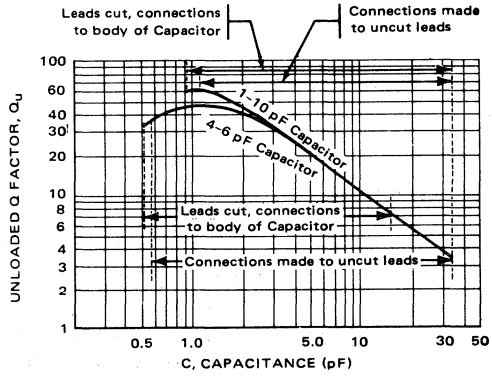


FIGURE 4 – Q versus CAPACITANCE FOR C_1 @ 1 GHz

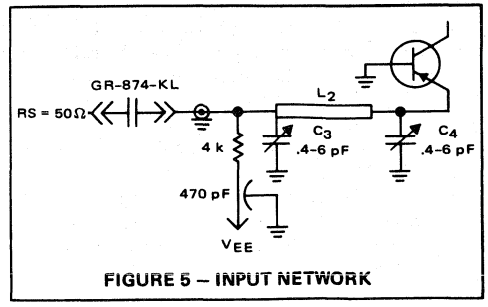


FIGURE 5 – INPUT NETWORK

CIRCUIT CONSTRUCTION

The transmission line lengths L_1 and L_2 are readily transferred to micro-strip lengths once the wavelength and line-width are known. Hopefully, this information is available from the manufacturer, but if not, it must be measured before the design can be completed. The laminate used for this application required a line-width of approximately 0.16 inches for a 20 mmho characteristic admittance. This value proved adequate both from a realizable design solution on the Smith Chart and also from a practicable circuit construction standpoint.

The actual laminate thickness depends to a large extent on the desired characteristic impedance and the frequency of operation The line thickness for a 50 ohm line is approximately 0.16 inch for a 1/16 inch laminate and approximately 0.035 inch for the same laminate 1/64 inch thick. As the intended frequency of operation is increased, the line width becomes a larger percentage of the line length.[4] Higher ratios of line width to length may result in undesirable modes of operation. Decreasing the laminate thickness results in a smaller line width for the same characteristic (assuming TEM operation) and a smaller line width to length ratio.

The dielectric constant for the material used was 2.6. The actual wavelength in the laminate is:

$$\lambda\,(\text{actual}) = \frac{\lambda\,(\text{air})}{\sqrt{2.6}} = \frac{11.8 \text{ inches}}{\sqrt{2.6}} = 7.34 \text{ inches}$$

Since $L_1 = 0.191\lambda$,

The physical length of L_1 is 1.4 inches

Correspondingly, L_2 is 0.062λ or 0.455 inches.

It should be pointed out that the actual wavelength[3] for this laminate is somewhat larger than that calculated from the dielectric constant. A careful measurement[4] of wavelength versus characteristic impedance (line width) demonstrates this phenomena. The slight increase in wavelength (6%) from that calculated using the dielectric constant was judged insignificant. However, this error increases for larger values of characteristic impedance and may prove to be quite significant for other laminates or narrower line widths. A good precaution would be to measure wavelength versus line width on each laminate used before TEM propagation is assumed.

Although the lines can be produced by a masking-etch process, adequate results can be obtained by cutting the desired strip from a thin copper sheet and glueing this strip to the teflon glass board. The latter is a convenient method for making rapid design changes.

The author observes several precautions which may or may not be necessary for all applications:

1. All breadboards have a ground strap which encompasses the outer periphery of the board. This strip is soldered to both the top and bottom copper sheets to effectively ground the outer periphery of the amplifier on all four sides. The circuit dimensions are held to a minimum to keep the ground planes as short as possible.

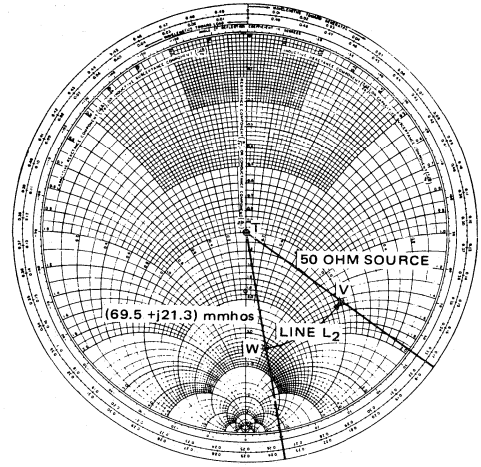


FIGURE 6 – INPUT NETWORK DESIGN

2. All RF connectors are carefully connected with grounding surfaces soldered to the ground plate. For instance, mount the connectors* perpendicularly to the board at a point where the connection to the center conductor is a minimum length. Completely solder the outer conductor to the copper sheet on the opposite side of the board. Poorly mounted connectors may result in poor transitions and unpredictable impedance transformations. For example, tacking the outer barrel of this connector to the line side of the board may seriously alter the predicted impedance level at the collector.

The amplifier was constructed as specified and the admittance levels were measured at the emitter and collector pins. These admittance levels were checked and adjusted to the original design values with C_1, C_2, C_3, and C_4

The 2N4957 was then soldered directly into the circuit with minimum lead length. The resultant power gain was 14.3 dB and the noise figure, 6.5 dB, which is within 1 dB of the original design requirements. Attempts to re-adjust the input loading and output loading for lower noise figure resulted in lower noise figure with decreased circuit stability. Although the circuit (adjusted for minimum noise figure) didn't oscillate, the calculated k factor from the resultant input and output admittances was approximately 2.

*General Radio Cable Connector 874-G58B.

LOW NOISE DESIGN

Improvement in noise figure is possible by arbitrarily adjusting the input and output loading. For the purpose of this paper, the stability factor (k = 4) will be retained.

However, the design curves represent the maximum power gain case. Although the circuit stability factor can be maintained at k = 4, varying the source loading will result in less power gain than indicated in the design curves.

The procedure for this case is as follows:

First, the optimum source resistance is calculated (see Appendix) and found to be 43Ω.* The calculated noise figure for this source is 5 dB. In addition, the source reactance was empirically determined to be inductive (j119Ω).

Second, the collector loading was calculated for a stability factor of 4. Using these values of source resistance and stability factor, the calculated gain (G_T) and collector loading is 11.8 dB and 3.41 mmhos −7.5 mmhos (neglecting stray capacitance).

The output network was readily adjusted to the desired collector loading. However, the input line was too short and required re-design (see Figure 7). The calculated value of this line length is 1.15 inches as contrasted with .46 inches used in the first example. The complete amplifier is shown in Figure 9.

The resultant power gain and noise figure was 11.8 dB and 5.5 dB. These figures compare well with the calculated design.

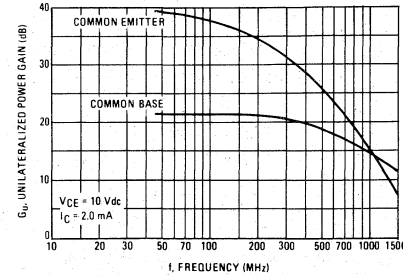


FIGURE 8 – UNILATERALIZED POWER GAIN versus FREQUENCY

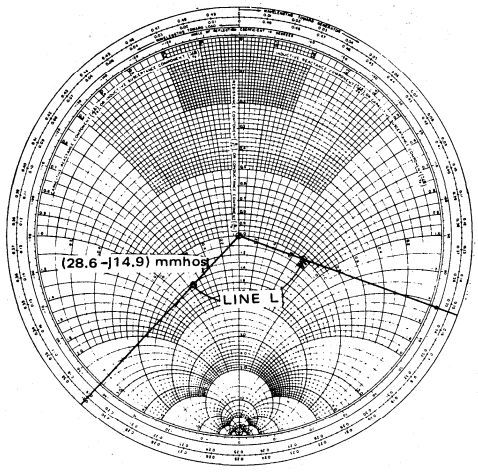


FIGURE 7 – LOW NOISE INPUT DESIGN

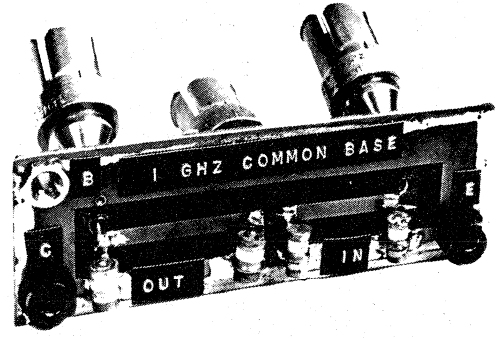


FIGURE 9 – 1 GHz AMPLIFIER

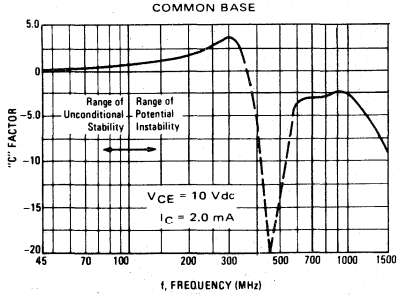


FIGURE 10 – LINVILL STABILITY FACTOR versus FREQUENCY

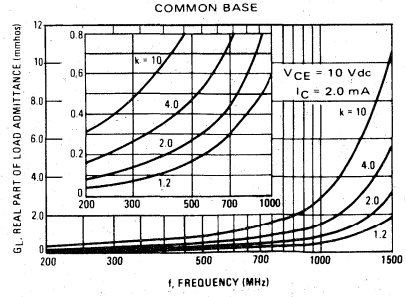


FIGURE 11 AND 12 – LOAD ADMITTANCE versus FREQUENCY (REAL)

*The actual value of optimum source resistance was empirically determined to be 35Ω. Consequently this value was used for the input circuit design rather than 43Ω.

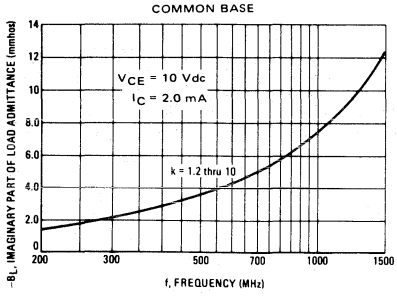


FIGURE 13 – LOAD ADMITTANCE versus FREQUENCY (IMAGINARY)

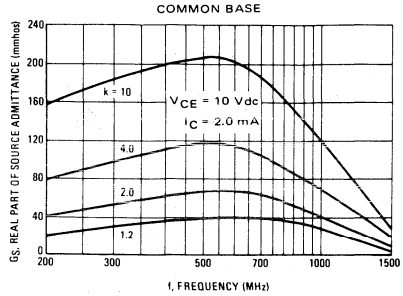


FIGURE 14 – SOURCE ADMITTANCE versus FREQUENCY (REAL)

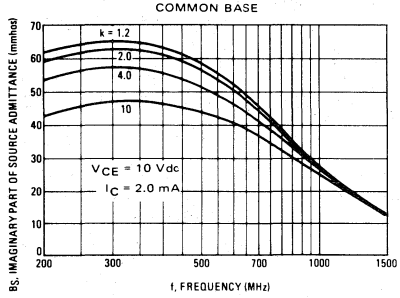


FIGURE 15 – SOURCE ADMITTANCE versus FREQUENCY (IMAGINARY)

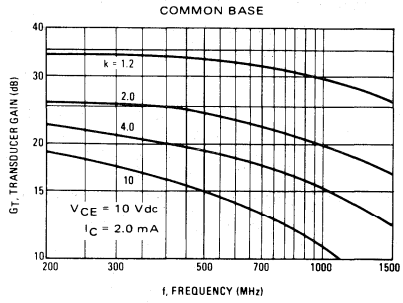


FIGURE 16 – TRANSDUCER GAIN versus FREQUENCY

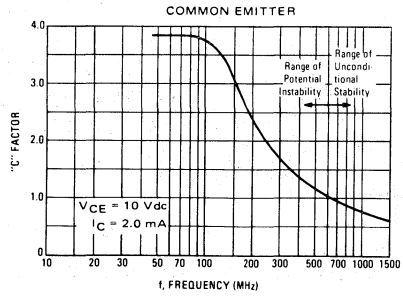


FIGURE 17 – LINVILL STABILITY FACTOR versus FREQUENCY

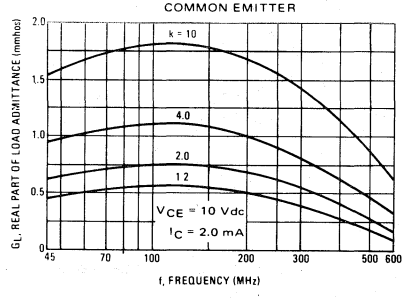


FIGURE 18 – LOAD ADMITTANCE versus FREQUENCY (REAL)

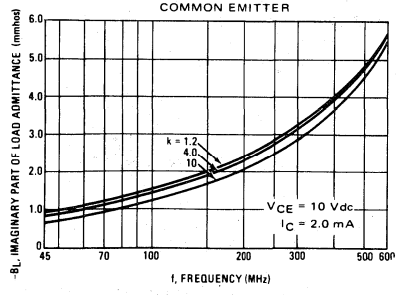


FIGURE 19 – LOAD ADMITTANCE versus FREQUENCY (IMAGINARY)

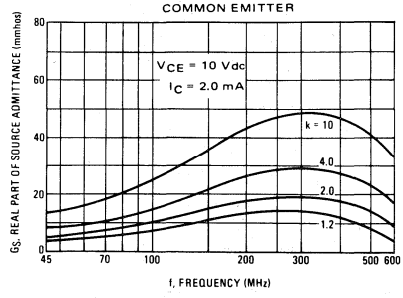


FIGURE 20 – SOURCE ADMITTANCE versus FREQUENCY (REAL

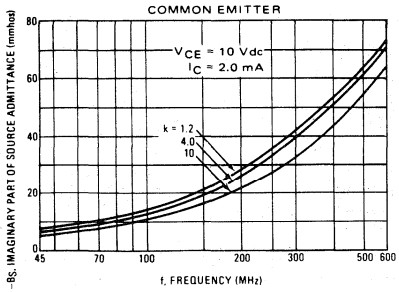


FIGURE 21 – SOURCE ADMITTANCE versus FREQUENCY (IMAGINARY)

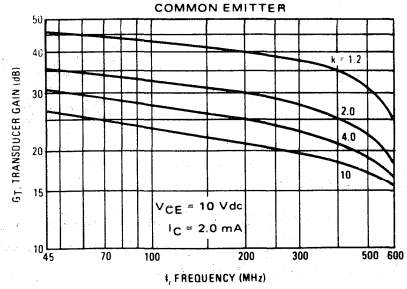


FIGURE 22 – TRANSDUCER GAIN versus FREQUENCY

APPENDIX

LOW NOISE DESIGN

The procedure followed in designing this amplifier is to first calculate the optimum source resistance for optimum noise figure and then calculate the collector loading for a required value of k.

A first approximation of optimum source resistance for optimum noise figure is:[2]

$$R_{gF(opt)} = \sqrt{k_2^2 + \frac{k_1}{k_3}}$$

$$k_1 = r_b + \frac{r_e}{2}$$

$$k_2 = r_b + r_e$$

$$k_3 = \frac{1 + (B_o + 1)\left(\frac{f}{f_{ab}}\right)^2}{2B_o r_e}$$

Assuming the above parameters for the 2N4957 are:

r_b = 12.5 ohms
r_e = 13 ohms
B_o = 40
f_{ab} = 1600 MHz,

$\therefore R_{gF(opt)}$ = 43 ohms

The noise figure using this source resistance is available from Nielsen's equation:[2]

$$NF = 1 + \frac{r_e}{2R_g} + \frac{r_b}{R_g} + \frac{(R_g + r_e + r_b)^2}{2\,B_o\,R_g\,r_e}\left[1 + (B_o + 1)\left(\frac{f}{f_{ab}}\right)^2\right]$$

Using the previous parameter values,

NF = 5 dB

Since the impedance level is different at the base, the collector loading must be re-designed.

Using Stern's stability equator for k = 4 (see Table 1):

$$k = \frac{2\,(g_{11} + G_S)(g_{22} + G_L)}{|y_{12}y_{21}| + \mathrm{Re}\,(y_{12}y_{21})}$$

and calculating G_L for G_S = 25 mmhos (40 ohms)

G_L = 3.41 mmhos

The transducer gain can be calculated from these impedance levels:

$$G_T = \frac{4\,\mathrm{Re}\,(Y_s)\,\mathrm{Re}\,(Y_L)\,|y_{21}|^2}{|(y_{11} + Y_s)(y_{22} + Y_L) - y_{12}y_{21}|^2}$$

G_T = 11.8 dB

TABLE 1
f = 1 GHz V_{CB} = 10 V I_C = 2 mA
y_{ib} = 25 –j25
y_{ob} = 0.55 +j7.54
y_{fb} = –4.99 +j41
y_{rb} = –0.01 –j1.19

REFERENCES

1. R. Hejhall, "RF Small Signal Design Using Admittance Parameters", Motorola Application Note AN-215A, Motorola Semiconductor Products, Inc., Phoenix, Arizona.
2. E. G. Nielsen, "Behavior of Noise Figure in Junction Transistors," Proc. IRE, Vol. 45, p. 957, July 1957.
3. F. Assadourian and E. Rimai, "Simplified Theory of Microstrip Transmission Systems", Proc. IRE, pp. 1651-1663, December 1953.
4. M. Arditi, "Experimental Determination of the Properties of Microstrip Components," Electrical Communication, December 1953.

SEMICONDUCTOR NOISE FIGURE CONSIDERATIONS

INTRODUCTION

The design of low noise amplifiers requires a basic working knowledge of subjects such as circuit stability, cross modulation, noise figure, etc.

The purpose of this report is to provide, in a single working reference, basic semiconductor noise figure considerations. Emphasis is on basic fundamentals rather than complex mathematical derivations. Because much of the theory, particularly with noise, is statistical and quite complicated, derivations will in fact be avoided with details available in suggested references.

NOISE SOURCES

The three types of noise sources generally associated with solid state devices are thermal noise, shot noise and excess noise.

THERMAL NOISE – Thermal noise[1,2,6,7,16] results from the random motion of free carriers in a medium caused by thermal agitation. Although the sum of all the noise currents over a long period of time is zero, at any given instant a net current in one direction may result. In an ideal resistor, the net current produces a voltage which has a constant spectral density independent of frequency. The self-generated noise voltage across a resistor is:

$$e_n = \sqrt{4\,k\,T\,R\,B},$$

where:

e_n = Johnson noise (rms volts)

k = Boltzmann's constant (1.38×10^{-23} joule/^oK)

T = Temperature (degrees Kelvin)

R = Effective Resistance (Ohms)

B = Equivalent bandwidth (Hz) of the system through which the noise is measured.

The thermal noise associated with a solid state device results from resistance within the device. Thermal noise in a transistor comes principally from the base spreading resistance (r_b').

SHOT NOISE – Shot noise[2,6,7,16], and thermal noise for that matter, depends on the nature of charge carriers for generation. The basic difference, is that thermal noise is produced by the erratic movement of free charge while shot noise is produced by the change (i.e., appearance and disappearance) of the charge carriers with respect to the circuit current.

The basic equation for full shot noise in a diode is:

$$i_n = \sqrt{2q\,I_{dc}\,B}$$

where:

i_n = shot noise (rms amps)

q = electron charge (1.59×10^{-19} coulombs)

I_{dc} = diode direct current (amps)

B = equivalent bandwidth (Hz)

Another important characteristic of both thermal and shot noise is the flat frequency spectrum. This frequency independent characteristic is an important consideration in the construction of equivalent device noise models.

Sources of shot noise in a transistor are currents within the emitter-base and collector-base diodes.[5]

EXCESS NOISE – Excess noise[2,14,16] usually occurs at low frequencies and is also known as 1/f noise. The exact mechanism producing this phenomenon is not well known. It is thought to be associated with "traps" within the emitter depletion layer which capture and release carriers at different frequency rates but with energy levels varying inversely with frequency. This noise is not only present in junction transistors and field-effect transistors, but also in certain types of resistors.[1,2] In general, the excess noise in junction transistors and field-effect transistors is negligible above 1 kHz.[4]

NOISE FIGURE

The sensitivity of an amplifier is limited by the signal-to-noise ratio available at the antenna or input. The presence of any of the previously described noise sources within the system only serves to further deteriorate this ratio. The amount of deterioration of the available input signal-to-noise ratio is called the noise figure and may be defined as:

$$F = \frac{\frac{P_{si}}{P_{ni}}}{\frac{P_{so}}{P_{no}}} = \frac{P_{no}}{P_{ni}}\,\frac{1}{G}, \qquad (1)$$

where:

F = noise figure in power ratio

P_{si} = signal input power

P_{ni} = noise input power

P_{so} = signal output power

P_{no} = noise output power

G = power gain of system

Noise figure is generally expressed in decibels, i.e.:

$$F_{(dB)} = 10 \log_{10}\left(\frac{P_{no}}{G\,P_{ni}}\right) \qquad (2)$$

From a practical standpoint, a distinction needs to be made between two types of noise figure, "Spot noise figure" [3,4] and "average noise figure."[3] Spot noise figure is the noise figure measured in a narrow frequency band, useful for specifying the noise figure at individual frequencies. Average noise figure is measured over a particular frequency spectrum such as the bandwidth of an IF amplifier and is useful when specifications approximating total system performance are required.

GENERAL CHARACTERISTICS – A discussion of noise figure variations versus frequency for all types of semiconductor devices is a complex study and actually beyond the scope of this paper. On the other hand, a preliminary study of transistor noise figure versus frequency can cover several general points which are common with other device types. A study of this type usually utilizes an equivalent circuit involving device parameters and noise sources from which noise figure is derived. The complexity of the resultant noise figure expression will vary with the complexity of the equivalent circuit used. A relatively simple yet adequate noise figure expression for this purpose is Nielsen's equation.[5,6,7,8] A modified version of this expression is:

$$F = 1 + \frac{r_e}{2R_g} + \frac{r'_b}{R_g} + \left[\frac{(R_g + r_e + r'_b)^2}{2\beta_o R_g r_e}\right]\left[1 + (\beta_o + 1)\left(\frac{f}{f_{ab}}\right)^2\right] \qquad (3)$$

where:

$$r_e = \frac{26}{I_{E\,(mA)}} \text{ (ohms)}$$

r'_b = base spreading resistance (ohms)

R_g = source resistance (ohms)

β_o = low frequency common emitter current gain

f = frequency (Hz)

f_{ab} = common base cut-off frequency (Hz)

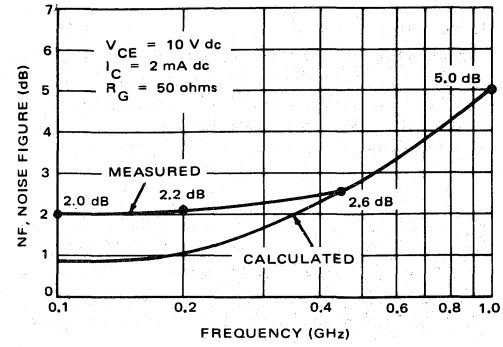


FIGURE 1 – TYPICAL SPOT NOISE FIGURE versus FREQUENCY (CALCULATED AND MEASURED) FOR 2N4957 SILICON PNP TRANSISTOR

The graph in Figure 1 gives both the measured and calculated curves of noise figure versus frequency for the 2N4957 transistor. Generally, the measured curve is flat in the mid-frequency range, increasing at approximately 6 dB per octave at higher frequencies. The descrepancy between measured and calculated values of noise figure in the mid-frequency range results from either not considering all noise sources or not properly analyzing the assumed noise sources. Regardless, the noise model used is reasonably accurate and adequate for the purpose of this paper.

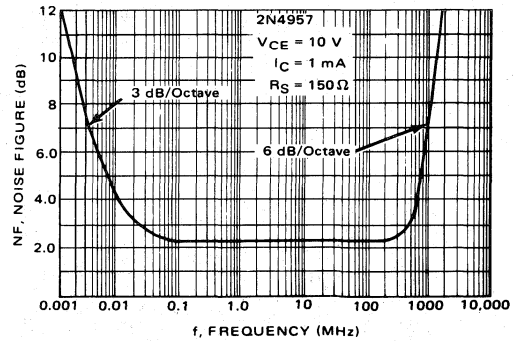


FIGURE 2 – NOISE FIGURE ASYMPTOTES

Transistor noise figure at low frequencies (1 kHz or less) is not predicted by Nielsen's equation. The major noise contributor in this region is excess noise. The slope of the curve in this lower frequency is approximately -3 dB per octave. Figure 2 shows a typical noise figure versus frequency curve for the 2N4957 which includes the region affected by excess noise.

Although equivalent noise circuits vary depending on device type (such as junction and MOS FETs) the same general characteristic noise figure versus frequency curve exists for each (see figures 3, 4, 5, 6 and 7).

Other important noise figure characteristics are evident from equation 3. For example, for a given transistor of known device parameters and operating frequency, this equation describes the relationship of noise figure versus source resistance. [5,9] Closer examination indicates that by proper selection of source resistance, noise figure can be minimized. A similar dependence may also be noted between noise figure and bias conditions–particularly emitter current.

An additional design variable of importance that is not shown by equation 3 is the source susceptance. [10] For many high frequency devices, lower noise figures are attained by mis-tuning the input circuit rather than tuning for maximum gain–that is, the base (common-emitter configuration) sees a resistance shunted by a susceptance (usually capacitive). The value of this susceptance is found by empirical methods. Again, the considerations are true with junction and MOS field-effect transistors. That is, the noise figure, in general, is optimum for a particular bias point and source admittance.

CHARACTERIZING THE DEVICE

Noise figure curves from device data sheets take several forms. One of the simplest presentations is noise figure versus frequency at a fixed bias point (see Figure 5). This bias point is usually a compromise between minimum noise figure and maximum power gain. Curves of this type, as a rule, do not provide the optimum source resistance necessary for minimum noise figure.

A convenient method of showing source resistance variations for a fixed frequency is shown in Figure 8. This figure shows at a glance the optimum source resistance for

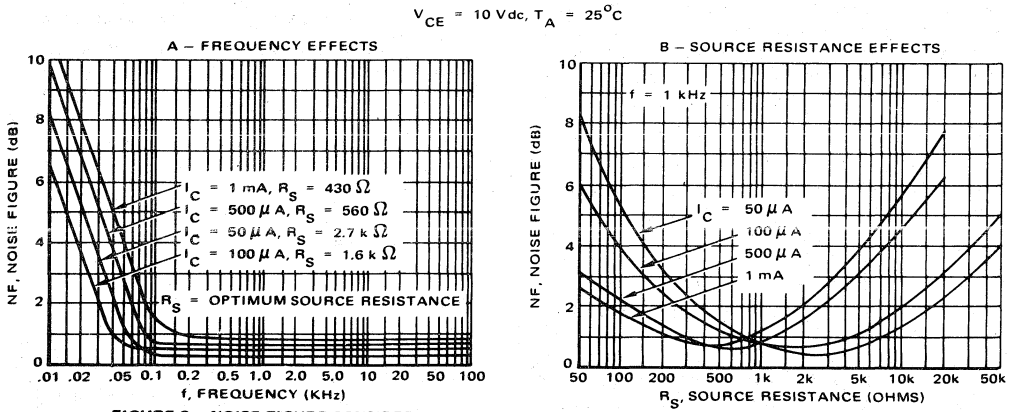


FIGURE 3 – NOISE FIGURE CONSIDERATIONS FOR THE 2N4402 AND 2N4403, SILICON PNP TRANSISTORS

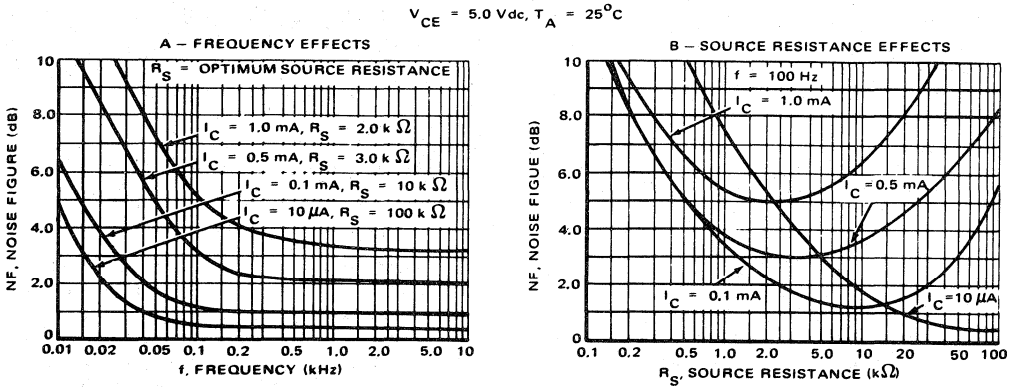


FIGURE 4 – NOISE FIGURE CONSIDERATIONS FOR THE 2N5088 AND 2N5089, SILICON NPN TRANSISTORS

various values of collector current. Similar curves (see Figure 10) at other frequencies allow a more complete picture of noise figure to be made.

Another method of demonstrating source resistance effects is shown in Figure 4B. Here the noise figure is plotted versus source resistance for several values of bias current. This presentation is common for low frequency devices. Another presentation which usually incorporates the previous curve is shown in Figure 4A. This figure shows noise figure versus frequency for several values of collector current. Each value of collector current includes the optimum source resistance for this value of current. The optimum source resistance is usually taken from a figure similar to Figure 4B.

An example of a field-effect transistor presentation similar to Figure 4 is shown in Figure 6 for a junction field-effect and Figure 7 for a tetrode connected junction field-effect transistor.

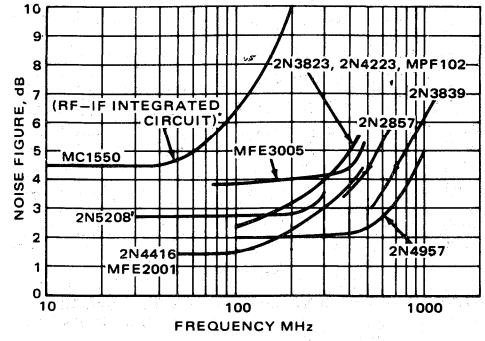


FIGURE 5 – NOISE FIGURE versus FREQUENCY FOR VARIOUS RF SEMICONDUCTOR DEVICES

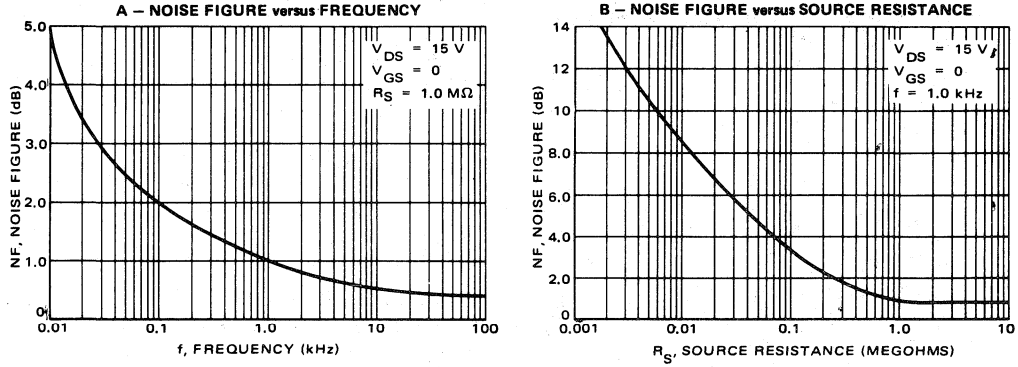


FIGURE 6 – NOISE FIGURE versus FREQUENCY FOR THE 2N4220, J-FET

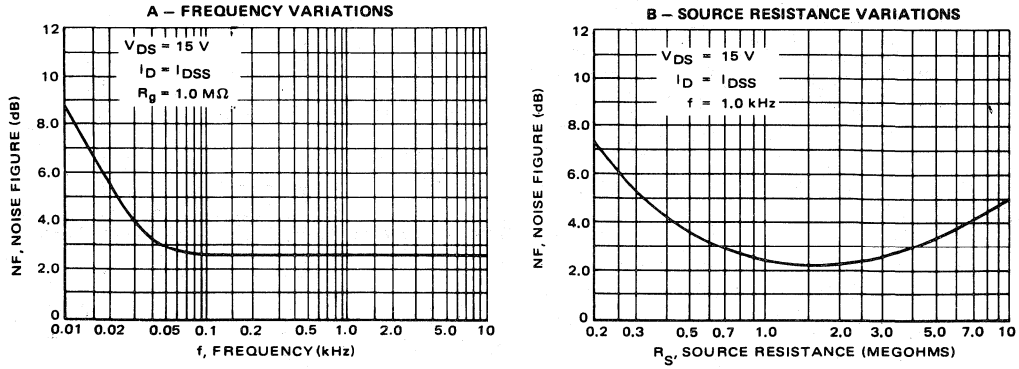


FIGURE 7 – NOISE FIGURE versus SOURCE RESISTANCE FOR THE 3N124, TETRODE J-FET

6

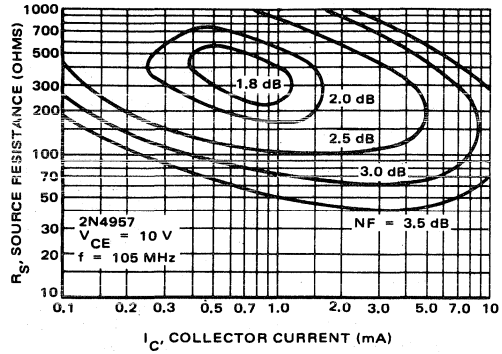


FIGURE 8 – CONTOURS OF NOISE FIGURE versus SOURCE RESISTANCE AND COLLECTOR CURRENT FOR 2N4957 AT 105 MHz

LOW FREQUENCY NOISE FIGURE MEASUREMENTS

SIGNAL GENERATOR METHOD – One of the simplest methods for measuring noise figure at low frequencies is to fix the input signal-to-noise ratio, and note the resultant output signal-to-noise ratio. The resultant degradation in the output signal-to-noise ratio (noise figure) may be expressed in the following form:

$$F_{(dB)} = 20\log_{10}\left(\frac{E_{si}}{E_{ni}}\right) - 20\log_{10}\left(\frac{E_{so}}{E_{no}}\right), \qquad (4)$$

where:

E_{si} = signal input voltage

E_{ni} = noise input voltage

E_{so} = signal output voltage

E_{no} = noise output voltage

(For measurement purposes the signal levels are expressed in terms of voltage rather than power.) If the source resistance R_s is known, E_{ni} can be calculated from equation (1) and E_{si} adjusted so the input signal to noise ratio is a convenient value such as 20 dB.

For such a case:

$$F_{1(dB)} = 20\ dB - 20\log_{10}\left(\frac{E_{so}}{E_{no}}\right) \qquad (5)$$

Since the measured output signal also includes E_{no}, the actual signal measured is:

$$\sqrt{E_{so}^2 + E_{no}^2}\ \dagger$$

Substituting the measured output signal into equation (5), the original relation becomes:

$$F_{2(dB)} = 20\ dB - 20\log_{10}\frac{\sqrt{E_{so}^2 + E_{no}^2}}{E_{no}} \qquad (6)$$

The difference between equation (5) and equation (6) represents the degree of error involved:

$$F_{1(dB)} - F_{2(dB)} = 20\log_{10}\sqrt{\frac{E_{so}^2}{E_{no}^2} + 1} - 20\log_{10}\frac{E_{so}}{E_{no}} \qquad (7)$$

† A vector sum is necessary as different frequencies are added.

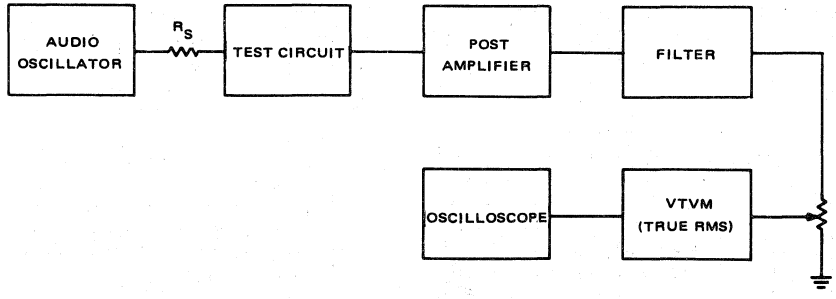


FIGURE 9 – TEST SET-UP FOR LOW FREQUENCY NOISE FIGURE MEASUREMENT–SIGNAL GENERATOR METHOD

6

As an example, this difference or error is less than 0.5 dB for a device having a noise figure up to 10 dB if the input signal to noise ratio is 20 dB.

The general procedure (see Figure 9) for utilizing this method is as follows: First, adjust the input voltage signal to noise ratio to 20 dB. Second, adjust the variable attenuator such that the voltmeter indication of E_{so} is full scale. Next, reduce the input signal to zero and note the drop in output voltage (dB). Since the output voltage without a signal is E_{no}, the actual drop in output in dB represents the ratio of E_{so} and E_{no}. This ratio, when subtracted from 20 dB, is the noise figure (without error correction).

CONSTANT-GAIN METHOD

The basis for this method involves maintaining a constant known voltage gain and measuring E_{no} (see equation 8). Knowing these terms, in addition to the bandwidth (which is determined by a band-pass filter as in the first method) and the source resistance, the noise figure can be calculated. A commercial instrument employing this operating principle is the Quan-Tech Noise Analyzer, Model 2173-2181.

$$F = \frac{P_{no}}{P_{ni}} \quad \frac{1}{G}, \quad G = \text{power gain}$$

or, in terms of voltage:

$$F = \frac{E_{no}^2}{E_{ni}^2 (G_V)^2}; \tag{8}$$

where G_V = voltage gain.

HIGH FREQUENCY NOISE FIGURE MEASUREMENTS

OUTPUT DOUBLING METHOD – Probably the simplest technique to measure noise figure at high frequencies is the noise doubling method. This involves increasing the noise generator output until the noise power in the output is doubled. The noise power produced by the noise generator under these conditions is the same as that produced by the circuit. That is:

$$P_{no} = G P_{ng},$$

where:

P_{no} = noise power out from source and device

G = power gain

P_{ng} = noise generator power output

If this term is substituted into equation (2), we have the following expression:

$$F = \frac{P_{ng}}{P_{ni}} \tag{9}$$

The actual values of both P_{ng} and P_{ni} are functions of not only source resistance but also the input impedance of the "device-under-test" circuit. A convenient method of defining P_{ng} and P_{ni} is on an available power basis, or,

$$P_{ni} = \frac{e_{ni}^2}{4 R_g}, \tag{10}$$

and

$$P_{ng} = \frac{i_{ng}^2 R_g}{4}. \tag{11}$$

For the case where the noise generator used is a temperature-limited tungsten-filament diode with a mean-square current of

$$i_{ng} = 2q I_{dc} B \text{ (see shot noise)} \tag{12}$$

$$F = \frac{q I_{dc} R_g}{2 k T_o} \tag{13}$$

Assuming the temperature of the source (T_o) is 290°K and that R_g is 50 ohms, this expression reduces to:

$$F = I_{dc} \text{ (in mA)}. \tag{14}$$

The actual technique used to double the noise output power involves more than connecting an RF voltmeter to the output of the test circuit and noting when the twice power output point is reached. First, the noise power levels are very low and a post amplifier is required to increase these levels to the capability of the RF voltmeter. In addition, this power amplifier (if spot noise is desired) must have a bandwidth less than the test amplifier and must not overload for the signal levels encountered. Finally, the actual RF voltmeter used must be linear and must respond to the RMS voltage.

The contribution of noise by the post amplifier is taken into account by the following equation:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} \cdots \frac{F_{(n-1)}}{G_1 G_2 \cdots G_{(n-1)}}, \tag{15}$$

where,

F = overall noise figure (power ratio)

F_1 = noise figure of the first stage (power ratio)

F_2 = noise figure of the second stage (power ratio)

F_3 = noise figure of the third stage (power ratio)

G_1 = power gain of the first stage (ratio)

G_2 = power gain of the second stage (ratio).

Additional considerations, such as "image response", are beyond the scope of this paper. For more information on these considerations, see references 18, 19, and 25.

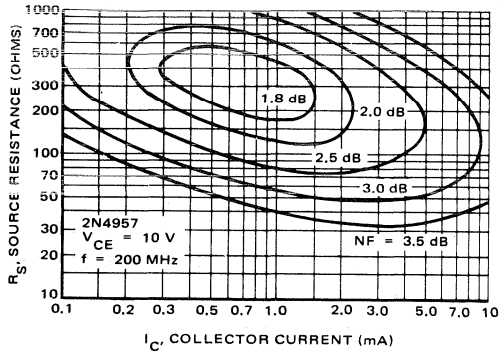


FIGURE 10 – CONTOURS OF NOISE FIGURE versus SOURCE RESISTANCE AND COLLECTOR CURRENT AT 200 MHz

COMMERCIAL EQUIPMENT TECHNIQUE – More sophisticated noise measurement techniques generally use a noise generator with two modes of operation. One mode utilizes the output power from a source such as a temperature limited diode or a gas-discharge tube. The second mode usually utilizes the noise output power of the generator source resistance at room temperature.

A noise generator of this type is connected to the input of a system under test and the two resultant output levels from the "system" are used to determine the noise figure (See Figure 12). The general equation[17] relating noise figure and the two output levels is:

$$F = 10\log_{10}\left[\frac{T_2 - T_o}{T_o}\right] - 10\log_{10}\left[\frac{P_{no2}}{P_{no1}} - 1\right] \quad (16)$$

where the expression $[(T_2 - T_o)/T_o]$ is a measure of the relative excess noise power from the noise generator and P_{no1} and P_{no2} are the two resultant power output levels. These levels correspond respectively to the "fired" and "unfired" modes of operation of the noise source.

The relative excess noise power is usually specified by the manufacturer. A typical value for an Argon gas tube is 15.2 dB. However, for accurate measurements, each source must be individually checked at each frequency of intended use.

Equation (16) is the basis for several of the most popular manual and automatic commercial noise characterization systems.[17,18,19]

A typical manual noise figure system using an IF attenuator is shown in Figure 11. The objective in using the attenuator is to determine the ratio of P_{no1} and P_{no2}. This ratio is called the "Y" factor. Initially, a convenient detector level is noted with the noise diode in the unfired mode. Next, the noise diode is fired and the attenuator readjusted to reduce the new detector level to the original level. The amount of attenuation added is the ratio of P_{no2} to P_{no1}. The resultant noise figure is calculated by substituting the excess noise power and the attenuator change in equation (16).

Automatic noise measuring equipment in general, gate the noise diode "on" and "off" at a fixed rate and continuously record the output power ratio. Methods of reducing this ratio to a continuous noise figure reading will vary with manufacturer.



FIGURE 11 – MANUAL NOISE FIGURE SYSTEM USING AN IF ATTENUATOR

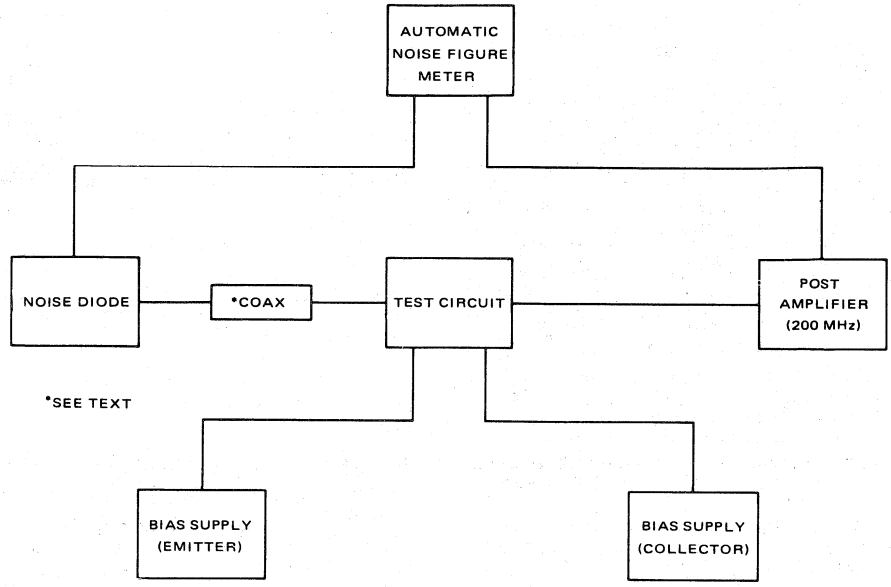


FIGURE 12 – TYPICAL TEST SET-UP FOR 200 MHz NOISE FIGURE MEASUREMENT

TYPICAL VHF NOISE FIGURE MEASUREMENTS USING AUTOMATIC EQUIPMENT

A typical 200 MHz noise figure test set-up using automatic noise measuring equipment is shown in Figure 12.

The noise diode is connected to the test circuit through a special coaxial cable which transforms the 50 ohm noise diode impedance to a higher impedance level, (such as 100 ohms) with negligible circuit loss. Input circuit losses are important since each dB of input circuit loss adds directly to the noise figure. The special coaxial cable length is trimmed to exactly one-quarter of a 200 MHz wavelength, such that when one end of the cable is terminated in 50 ohms, the resultant impedance level at the other end is the desired resistive value with minimum shunting capacitance (0.2 pF max). The cable characteristic impedance necessary to give the desired source resistance is calculated from:

$$R_o^2 = R_S R_L,$$

where

R_o = characteristic impedance of cable (ohms)

R_L = resistance of noise diode (50 ohms)

R_S = desired source resistance (ohms)

Several values of source resistance values are readily attained by using coaxial cable with standard values of characteristic impedance. Additional resistance values can be attained by varying the center-conductor wire size of the cable.

Directly following the test amplifier is the post amplifier. This amplifier provides the additional gain necessary to operate the automatic noise figure equipment. Although the required gain is also a function of the test circuit gain, a typical power gain is 50 dB.

Since system bandwidth is determined by the automatic noise equipment, no special bandwidth restrictions are required.

Any contribution of the post amplifier to the total measured noise figure may be calculated with Equation 15. A post amplifier with a noise figure low enough to avoid any significant contribution to the total noise figure is highly desirable.

The input impedance of the post amplifier should be 50 ohms since this impedance level will provide the load for the test circuit. If the device under test is mismatched at the output, the resultant source resistance seen by the post amplifier can increase to several hundred ohms and may result in instability problems with the post amplifier. Consequently, the first stage of the post amplifier should be stable regardless of the source resistance.

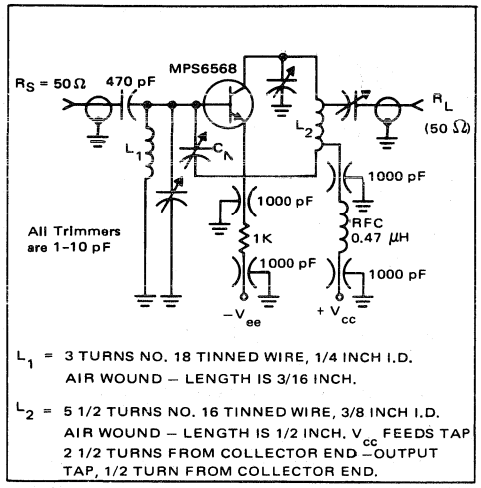


FIGURE 13 – A TYPICAL 200 MHz NOISE TEST CIRCUIT

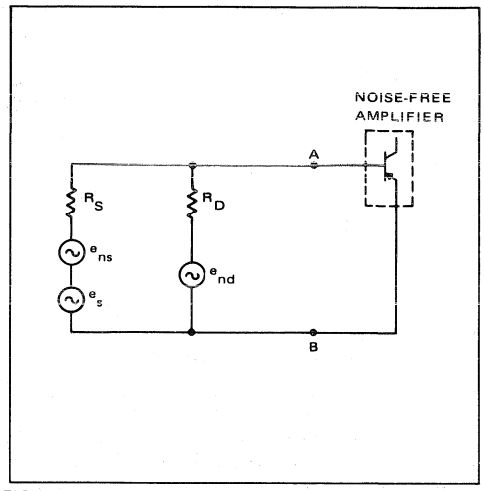


FIGURE 14 – MODEL TO DEMONSTRATE THE EFFECT OF AN EXTERNAL SHUNT RESISTANCE AT INPUT OF NOISE FIGURE TEST CIRCUIT

A typical 200 MHz noise figure test circuit is shown in Figure 13. Here a common emitter neutralized configuration is used with two bias supplies. The desired source impedance seen by the device under test is provided by the special coaxial cable previously discussed, and the input tank circuit provides the necessary tuning. The coil (L_1) must be carefully constructed to minimize input circuit loss; not only should the unloaded Q be high, but the actual inductance value should be as large as possible and still maintain tuning.

In general, all lead lengths should be minimum and circuit layout should be such that the neutralizing capacitor (C_N) is provided the shortest path between the base and L_2, through a small hole in the shield. Piston-type capacitors are recommended for C_N.

The immediate area should be carefully examined for unknown noise generators. A screen room is certainly a "must." As a general statement, each piece of equipment in the screen room must be examined as a potential noise source. For instance, it is not uncommon to find that the signal generator used to measure power gain, generates a considerable amount of noise power even with the generator output power level reduced.

DESIGN CONSIDERATIONS FOR HIGH FREQUENCY LOW NOISE AMPLIFIERS

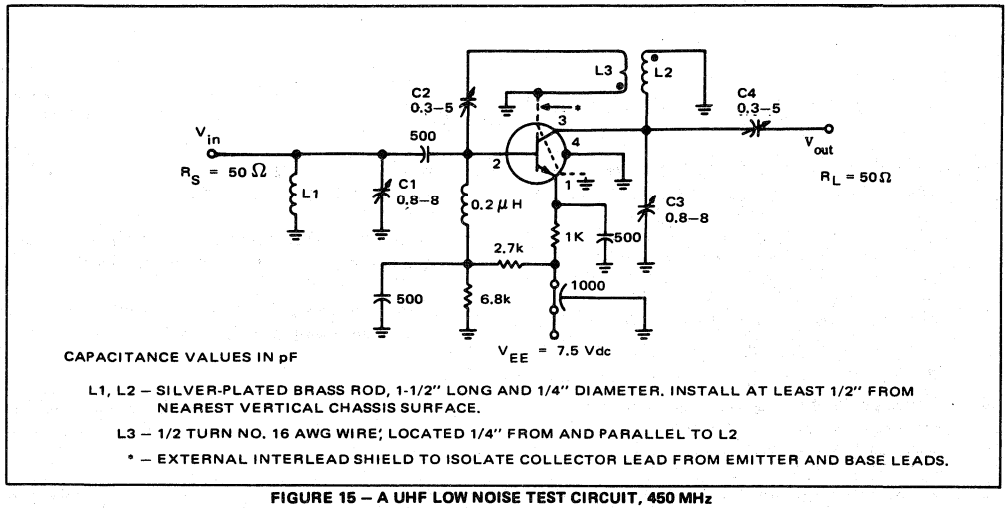
The actual design of a low noise amplifier whether intended for audio or RF applications usually involves considerations other than low noise figure. Particularly in high frequency applications, considerations such as cross-modulation, intermodulation distortion and dynamic range are of paramount importance and may often overshadow and delegate to a secondary role the overall noise figure. (The interested reader may obtain more information in references 10, 23, and 24).

As previously mentioned, the device must operate under specified bias conditions and generator source admittance to realize the optimum device noise figure. In addition to providing the device with this environment, another major noise contributor, input circuit loss, must also be considered. This circuit loss usually takes the form of an equivalent input shunting resistance resulting from coil loss, bias resistance, capacitor loss, or other component losses such as stand-offs and sockets.

An excellent method of demonstrating the effect of an external resistance shunting the input circuit is to consider the circuit in Figure 14. The amplifier is considered noise free. The calculated noise figure [15] up to point A-B is:

$$F = 1 + \frac{R_S}{R_D}$$

For the case where the shunting resistor R_D equals the source resistance, the noise figure will be degraded 3 dB before the device is even considered. The minimum noise figure occurs when $R_D \gg R_S$ which means that R_D must be large or R_S small. The former condition may be difficult to achieve since the input of the amplifier is generally a tuned circuit and the maximum value of R_D (considering the tuned circuit only) will be limited by practicable coil losses. Correspondingly, R_S may not be arbitrarily reduced since the device requires a certain source resistance for minimum noise figure.



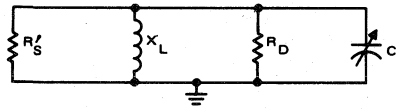
L1, L2 – SILVER-PLATED BRASS ROD, 1-1/2" LONG AND 1/4" DIAMETER. INSTALL AT LEAST 1/2" FROM NEAREST VERTICAL CHASSIS SURFACE.

L3 – 1/2 TURN NO. 16 AWG WIRE, LOCATED 1/4" FROM AND PARALLEL TO L2

* – EXTERNAL INTERLEAD SHIELD TO ISOLATE COLLECTOR LEAD FROM EMITTER AND BASE LEADS.

FIGURE 15 – A UHF LOW NOISE TEST CIRCUIT, 450 MHz

The effect of reducing the bandwidth can be seen by examining the following where tuning is shown in the input circuit:



R_D = coil loss ($R_D = Q_U X_L$)

X_L = reactance of coil

R_S' = optimum source resistance

The circuit bandwidth of this figure is described as:

$$\text{Bandwidth} \cong \frac{X_L f_o}{R'}$$

where:

f_o = center frequency

$$R' = \frac{R_D R_S'}{R_D + R_S'} \cong R_S' .$$

Thus, it can be seen that reducing the bandwidth for a fixed value of R_S' will require X_L to also decrease. Unfortunately, reducing X_L will also reduce R_D. Thus, decreasing the bandwidth of the input circuit will result in generally a higher noise figure, since the circuit loss increases.

An example of a UHF low noise test circuit is shown in Figure 15 in which noise figures as low as 2.1 dB are measured. 27,28.

The common emitter and common base configuration have approximately the same noise figure.[5] The final choice of which configuration to use is usually made by carefully considering other factors such as power gain, stability, and whether or not neutralization is acceptable.

DESIGN CONSIDERATIONS FOR LOW FREQUENCY, LOW NOISE AMPLIFIERS

Excess noise (the predominant noise contributor at low frequencies) does not fit into a convenient noise model such as proposed by Nielsen. However, empirical investigation shows a similar dependence of noise figure on bias conditions and source impedance (see Figures 3 and 4). This dependence is of considerable importance in low frequency design and may dictate the type of device used (bipolar or field effect transistor). The major difficulty concerns transforming the system source impedance to the desired value (seen by the device) necessary for optimum noise figure. At high frequencies, transformation is readily accomplished with a simple tuned circuit. At low frequencies, however, transformation is limited to a transformer. Transformers are usually avoided if possible because of bandwidth, weight, noise pickup, loss and cost considerations. Consequently, rather than transforming the required source impedance (magnetic pick-up, etc.) to the desired resistance seen by the device, the device is usually selected and biased such that the required resistance seen by the device approximates the actual source resistance.

BIBLIOGRAPHY

1. W.W. Harman and J.G. Terman, "Electronic Measurements," McGraw Hill Book Company, Inc., New York, 1952.
2. W.R. Bennett, "Electrical Noise," McGraw Hill Book Company.
3. "IRE Standards on Electron Tubes: Definition of Terms, 1957" Proc. IRE; Vol. 45, pp. 983-1010, July, 1957.
4. "Description of the Noise Performance of Amplifiers and Receiving Systems," Proceedings of the IEEE pp. 436-442, March, 1963.
5. E.G. Nielsen, "Behavior of Noise Figure in Junction Transistors," Proc. IRE, Vol. 45, p. 957, June, 1957.
6. A. van der Ziel, "Shot Noise in Junction Diodes and Transistors," Proc. IRE, Vol. 43, pp. 1639-1696, November, 1955.
7. A. van der Ziel, "Shot Noise in Transistors," Proc. IRE, Vol. 48, pp. 114-115, January, 1960.
8. H.A. Haus, et. al., "Representation of Noise in Linear Two-Ports," Proc. IRE, Vol. 48, pp. 69-74, January, 1960.
9. F.M. Gardner, "Optimum Noise Figure of Transistor Amplifiers," Proc. IRE, pp. 45-48, March, 1963.
10. W.A. Rheinfelder, "Design of Low-Noise Transistor Input Circuits." Hayden Book Company, Inc., New York, 1964.
11. J.J. Freeman, "Principles of Noise," John Wiley and Sons, Inc., 1958.
12. H.T. Friss, "Noise Figure of Radio Receivers," Proc. IRE, Vol. 32, No. 7, pp. 419-422, July, 1944.
13. W. Davenport and W. Root, "Random Signals and Noise," McGraw Hill Book Company, Inc., 1958.
14. L. Smullin and H. Haus, "Noise in Electron Devices," John Wiley and Sons, Inc., New York, 1959.
15. K. Sturley, "Radio Receiver Design," John Wiley and Sons, Inc., New York, 1953.
16. A. van der Ziel, "Noise," Prentice-Hall, Inc., 1954.
17. Hewlett Packard Application Note No. 57, Hewlett Packard, Palo Alto, California.
18. "Noise Figure Measurements," Airborne Instrument Laboratory, Deer Park, Long Island, New York.
19. "Topics in Noise Figure Measurements," Airborne Instrument Laboratory, Deer Park, Long Island, New York.
20. J. Pettit and M. McWharter, "Electronic Amplifier Circuits," McGraw Hill Book Company, Inc., New York, 1961.
21. J. Pierce, "Transistor Circuit Theory and Design," Charles E. Merrill Books, Inc., Columbus, Ohio, 1963.
22. J. Vasseur, "Properties and Applications of Transistors," The MacMillan Company, New York, 1964.
23. W. Austin, J. Dean, D. Griswold, and O. Hart, "T.V. Applications of MOS Transistors," RCA Proc. of NEC, Vol. 22, 1966, p. 1061.
24. E. McKean, F. Carlson, "Small-Signal RF Amplification of MOS Devices," RCA, Proc. of NEC, Vol. 22, p. 88, 1966.
25. G. Valley, H. Wallman, "Vacuum Tube Amplifier," p. 720, The McGraw Hill Book Company, Inc., New York, 1948.
26. R. Lane, "The Comparative Performance of FET and Bipolar Transistors at VHF," IEEE Journal of Solid-State Circuits, Vol. SC-1, No. 1, September, 1966.
27. R. Hejhall, "RF Small Signal Design Using 2-Port Parameters," Motorola Application Note AN-215A, Motorola Semiconductor Products Inc., Phoenix, Arizona.
28. "UHF Amplifier Design Using Data Sheet Design Curves," Motorola Application Note AN-419, Motorola Semiconductor Products Inc., Phoenix, Arizona.

MICROSTRIP DESIGN TECHNIQUES FOR UHF AMPLIFIERS

Prepared by:
Glenn Young

INTRODUCTION

This note uses a 25 watt UHF amplifier design as a vehicle to discuss microstrip design techniques. The design concentrates on impedance matching and microstrip construction considerations. A basic knowledge of Smith chart techniques is helpful in understanding this note. [1]

The amplifier itself, as shown in Figure 1, provides 25 watts of output power in the 450 - 512 MHz UHF band. It is designed for 12.5 volt operation which makes it useful for mobile transmitting equipment. A variety of police, taxi, trucking and utility maintenance communication systems operate in this band.

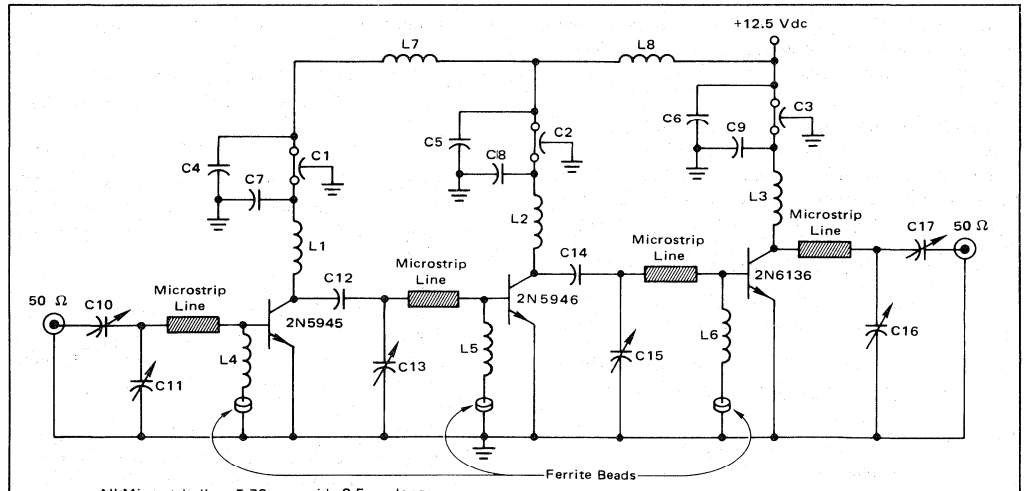
A summary of the performance of the completed amplifier operating with a 12.5 volt supply at 512 MHz indicates a power gain of 16 dB and a bandwidth (-1 dB) of 8 MHz. Overall efficiency is 48.5% and all harmonics are a minimum of 20 dB below the fundamental output.

Sections on construction and device handling considerations are also presented.

MICROSTRIP DESIGN CONSIDERATIONS

Microstrip design was used for this amplifier due to its inherent superiority over other methods at this frequency. These techniques not only offer good compatibility with the Motorola "stripline" package but they also offer very good reproducibility. Microstrip construction is more efficient than lumped constant equivalents since microstrip lines are less lossy than lumped constant components.

Microstrip board with Teflon bonded fiberglass dielectric rather than the higher dielectric constant ceramics was chosen due to the ease of working with that type of material. A substrate thickness of 1/16-inch is convenient since a line of the same width as the transistor leads (0.225 inch) produces a reasonable characteristic impedance (Z_O) of 40.65 ohms. The value of the characteristic impedance is



All Microstrip lines 5.72 mm wide 2.5 cm long

C1,2,3, 470 pf feedthru
C4,5,6 1.0 μf Tantalum
C7,8,9 0.1 μf Ceramic
C10,11,13,15,16,17 1.5-20 pf Compression Trimmer ARCO 420
C12,14 10 pf Microwave capacitor ATC type 100-B-10-M-MS or equiv.

L1, L2, L3 – 5 turns #20 Closewound 3/16" I.D.
L4, L5, L6 – 0.15 μh molded choke
L7, L8 – Ferroxcube VK 200 20/4B or equiv.
Ferrite beads are Ferroxcube 56 590 65/3B or equiv.

FIGURE 1 – Schematic Diagram of 25 W UHF Amplifier

calculated from:[4]

$$Z_O = \frac{377h}{\sqrt{\epsilon_r} \times W \left[1 + 1.735\, \epsilon_r^{-.0724} \left(\frac{W}{h}\right)^{-.836}\right]} \quad (1)$$

where ϵ_r = dielectric constant
W = width of microstrip line
h = thickness of the dielectric

The h term is equal to the total thickness of the microstrip board minus the thickness of the copper on both sides. In this design that term is equal to

$$h = 62 - (2 \times 1.4) = 59.2 \text{ mils} \quad (2)$$
1 oz. copper = 1.4 mils thick

The effective width should be used when the conductor is of finite thickness.

$$Weff = W + \frac{t}{\pi}\left(\ln \frac{2h}{t} + 1\right) \quad (3)$$

where t = thickness of the conductor

$$Weff = 225 + (1.4/\pi)\left(\ln \frac{2 \times 59.2}{1.4} + 1\right) = 227.4 \text{ mils} \quad (4)$$

therefore:

$$Z_O = \frac{377 \times .0592}{\sqrt{2.5} \times .2274 \left[1 + 1.735 \times 2.5^{-.0724} \times \left(\frac{227.4}{59.2}\right)^{-.836}\right]} = 40.65\ \Omega \quad (5)$$

THE AMPLIFIER DESIGN

The first decision in the design was determining the type of matching networks to be used. The network shown in Figure 3 was chosen because of its ability to "map" a large area of complex impedances; this allows a good tuning margin to compensate for normal variations in transistor impedances and other peripheral effects. A side benefit of this network is that the series tuning element provides the dc blocking function, eliminating the need for coupling capacitors.

The synthesis of the matching networks utilizes the large signal impedances of the transistors as specified on the data sheets. These parameters should not be confused with small signal 2-port parameters. A complete discussion of large signal characterization is given in Motorola Application note AN-282A. The impedance parameters used in this note are taken from the respective data sheets and were obtained in the manner described in AN282A.

2N5945
Z_{in} 1.3 + j1.5 ohms
Z_{out} 4.6 - j5.4 ohms
2N5946
Z_{in} 1.3 + j1.2 ohms
Z_{out} 4.2 - j0.5 ohms
2N6136
Z_{in} 1.3 + j 4.11 ohms
Z_{out} 3.2 + j 1.96 ohms

FIGURE 2 – Transistor Complex Input and Output Impedance at 470 MHz (Series Form)

Smith chart techniques are used to synthesize the matching networks in the amplifier to be described. The complex series equivalent input and output impedances as taken from the data sheets are shown in Figure 2. There are an infinite number of solutions to the required matching networks, however, once an initial choice of one of the components is made, only one solution exists. It is obvious that all components need to be kept within reasonable limits, however it would seem that the most critical parameter is the length of the microstrip line. Using this assumption, the length of the line is chosen as a starting point. The input network, shown in Figure 3 will be solved to illustrate the technique.

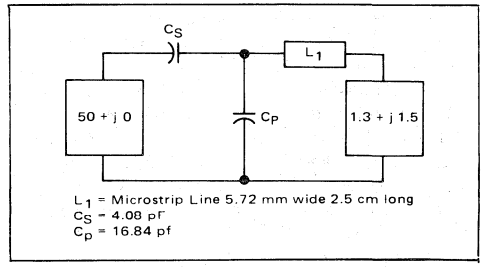


FIGURE 3 – Equivalent Circuit of Input Network

Before proceeding to determine the component values, the effective wavelength of the desired frequency in the microstrip line must be known. This is accomplished by first finding λ_O, the wavelength in free space:

$$\lambda_O = \frac{c}{freq} = \frac{3 \times 10^8}{4.7 \times 10^8} = 0.638 \text{ meters} \quad (6)$$

where c = propagation constant, free space

The TEM mode wavelength is determined:

$$\lambda_{TEM} = \lambda_O / (\epsilon_r)^{1/2} = 63.8\text{cm} / (2.5)^{1/2} = 40.37\text{cm} \quad (7)$$

Now as the propagation in microstrip line is not pure TEM mode, a correction factor must be applied to the last calculation.[4]

$$K = \left[\frac{\epsilon_r}{1 + 0.63\,(\epsilon_r - 1)\left(\frac{W}{h}\right)^{.1225}}\right]^{1/2} = \left[\frac{2.5}{1 + 0.63\,(2.5-1)\,(227.4/59.2)^{.1225}}\right]^{1/2} = 1.086 \quad (8)$$

Then:

$$\lambda' = (\lambda tem)\,(K) = (40.37)\,(1.086) = 43.85 \text{ cm} \quad (9)$$

This is the effective wavelength and will be used in all further calculations. Equation 8 is valid for width to height ratios of 0.6:1 or greater. For ratios less than 0.6:1 alter the (w/h) factor in the denominator to $(w/h)^{.0297}$

The source and load impedances must now be normalized to the 40.65Ω characteristic impedance of the line and

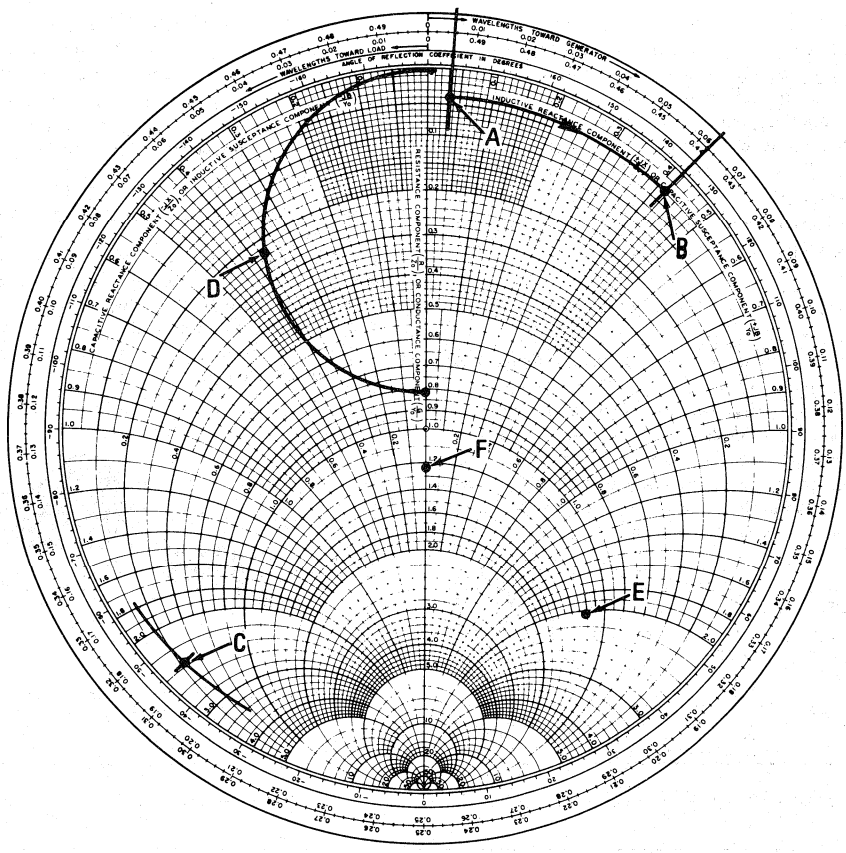


FIGURE 4 — Smith Chart Solution

plotted on the Smith chart. It should be noted that the terms "source" and "load" are used here only in reference to the Smith chart solution.

A source impedance of 50 + j0 is normalized to 1.23 + j0 and a load impedance of 1.3 + j1.5 is normalized to 0.032 + j0.0369 . The load impedance is plotted at point A in Figure 4 and the source impedance at point F. An arbitrary choice of 2.5 cm for the line length was made. This is an electrical length of:

$$\text{electrical length} = \text{line length}/\lambda' = 2.5 \text{ cm}/43.85 \text{ cm} = 0.057\ \lambda \quad (10)$$

Point A is rotated on a constant VSWR circle 0.057 λ toward the generator to point B. Reactance must now be added in parallel with the impedance presented at the end of the line just plotted. As parallel additions are more easily handled in admittance form, point B is converted to an admittance by rotating it one-quarter wavelength on the same constant VSWR circle. This results in point C in Figure 4. The constant conductance circle that point C lies on is noted to be 0.23. The problem now is to move along this circle towards the generator until the reciprocal of the constant resistance circle of the source impedance is intercepted. This circle does not exist on a standard Smith chart and must be constructed.

This is done by determining the radius of the constant resistance circle representing the real part of the source impedance and then constructing a circle of equal radius with its center on the real axis and its circumference tangent to the outer radius of the chart at zero resistance. When this is done the intercept with the 0.23 constant real circle is seen to lie at point D. The amount of parallel susceptance needed to move from point C to point D is:

$$B_{CP} = (B_C - B_D)(Y_O) = (2.4 - 0.38)(24.6) = 49.72 \text{ mmhos} \quad (11)$$

This is a parallel capacitance of:

$$C_P = B_{CP}/2\pi f = 49.72/(2\pi)(470 \times 10^6) = 16.84 \text{ pF} \quad (12)$$

6

All that remains to finish the solution is to determine the amount of reactance necessary to reach the source at point F. To do this, it is first necessary to transpose point D, which is an admittance, to an impedance. This is accomplished by rotating point D one-quarter wavelength on a constant VSWR circle. This moves point D to point E which is on the 2.04 reactance line thus representing a series reactance of:

$$X_{CS} = (X_E) \bullet (Z_O) = (2.04) \bullet (40.65) = 82.9 \text{ ohms} \quad (13)$$

A series capacitance with this reactance is:

$$C_S = \frac{1}{(2\pi)(f)(X_{CS})} = \frac{1}{(2\pi)(470 \times 10^6)(82.9)} = 4.08 \text{ pF} \quad (14)$$

This completes the solution for the input network.

The interstage networks as well as the output network are solved in similar fashion with the following differences. In the case of the interstage networks when the imaginary term of the source impedance is other than zero, point F would be plotted at the complex conjugate of the source impedance. In the output network solution the "source" is the output load of the amplifier (50 + j0) and the "load" is the collector impedance of the output device.

	450 MHz	480 MHz	512 MHz
Power Gain	18 db	17.2 db	16 db
Bandwidth (-1 db)	5 MHz	6 MHz	8 MHz
Overall Efficiency	44.5%	46.5%	48.5%
Harmonics	All Harmonics Better Than -20 db		
Stability	Amplifier Stable under all Conditions of Drive down to V_{CC} = 5.0 volts		
Power Output	25 w	25 w	25 w
Burnout	No Damage to any Transistor with Load Open & Shorted with 0 to ±180° Phase Angle		

FIGURE 5 – Typical Performance Specifications

Figure 5 gives details on the performance of the completed amplifier. The use of the porcelain dielectric chip capacitors for the series elements in the interstage networks was found to provide an additional 2.5 to 3.0 dB of gain over that obtained with compression trimmers as well as reducing the number of tuning adjustments necessary.

CONSTRUCTION CONSIDERATIONS

As in all RF power applications, solid emitter grounds are imperative. In microstrip amplifiers gain can be increased more than 1 dB by grounding both of the emitter leads to the bottom foil of the microstrip board by wraping strips of copper foil thru the transistor mounting hole as shown in Figure 6.

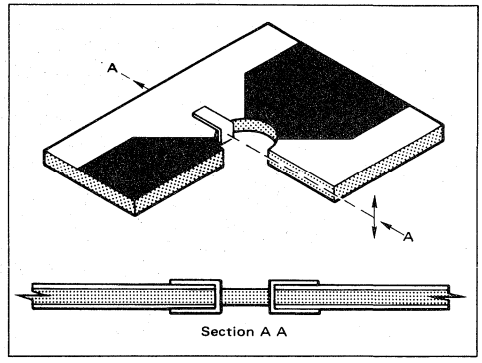


FIGURE 6 – Proper Emitter Grounding Method

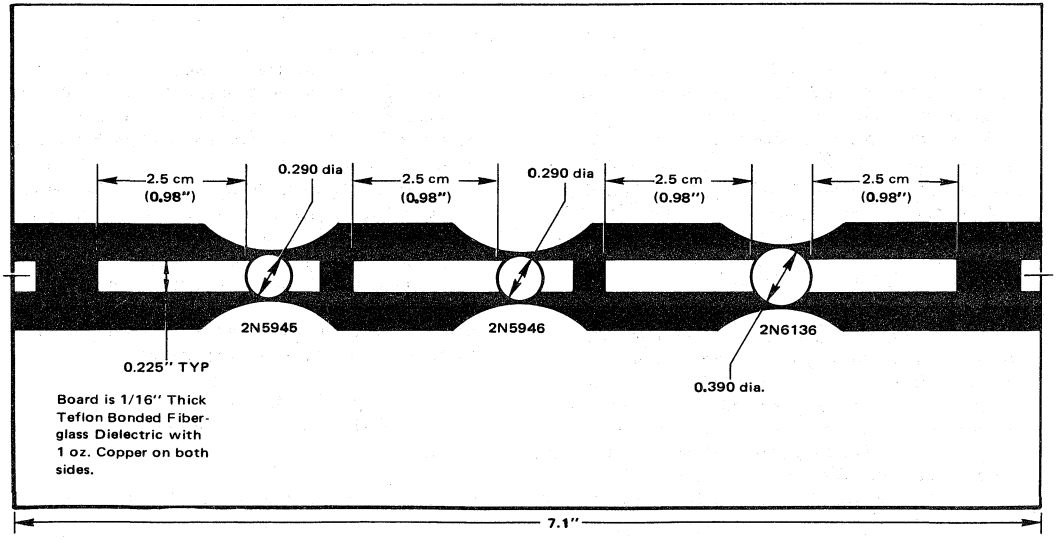


FIGURE 7a – Microstrip Board Layout

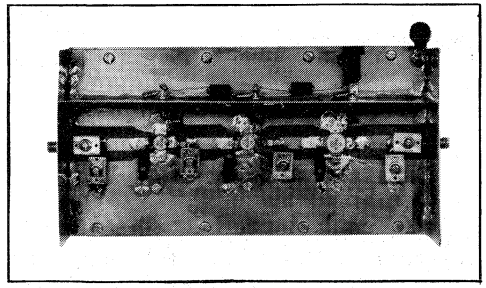


FIGURE 7b – Photograph of Amplifier

Stability under normal operating conditions is essential, however, stability should be maintained over as wide a range of supply voltage and drive levels as possible. If amplifier stability is maintained at all RF drive levels with the supply voltage reduced to between three and five volts, the designer can be practically certain that the amplifier will remain stable under all conditions of load. Maintaining stability is a key factor in protecting these transistors from damage. In a stable amplifier that has adequate heat sinking, these transistors will withstand high VSWR loads including open and shorted loads without damage. The major controlling factors in obtaining wide range stability are:

1) Mechanical layout: Good mechanical layout includes good emitter grounds (as previously described), compact layout and short ground paths.

2) Biasing: The devices are all zero biased for Class "C" operation. The use of relatively low Q base chokes with ferrite beads on the ground side will maintain good base circuit stability. In some applications, the use of a resistor in series with the ground side of the base chokes on the output and driver stages may enhance the stability. Approximate values of these resistors should be 10 ohms, 1/2 watt for the driver and 1.0 ohms, 1/2 watt for the output device. The addition of these series resistors will cause a slight loss in gain; (about 0.1 to 0.2 dB overall).

3) Collector supply feed method: The collector supply feed system is designed to provide decoupling at or near the operating frequency and a low collector load impedance at frequencies much lower than the operating frequency.

4) Heat sinking: In order to protect against burnout under all conditions of load, adequate heat-sinking must be provided. In heat sinking the device it is imperative to use a good grade of thermal compound, such as Dow-Corning 340, on the interface between the device and its heat sink.

Figure 7a shows the microstrip board layout while Figure 7b is a photo of the completed amplifier.

DEVICE HANDLING CONSIDERATIONS

Although the Motorola stripline package is a rugged assembly, some care in its handling should be observed. The most important mechanical parameter is stud-torque, specified on the data sheet at 6.5 inch-pounds maximum. This data sheet specification is an absolute maximum and should not be exceeded under any circumstances. A good limit to use in production assembly is 6 inch-pounds and if for any reason repeated assembly/dissassembly is required torque should be limited to 5 inch-pounds.

Another major precaution to observe is to avoid upward pressure on the leads near the case body. Stresses of this type can crack or dislodge the cap. This type stress sometimes occurs due to adverse tolerance build-up in dimensions when the device is mounted thru a microstrip board onto a heat sink. Many times this type of stress is applied even in the most carefully thought out designs due to solder build-up on the copper foil when a device is replaced. In device replacement care should be taken to flow all solder away from the mounting area before the stud nut is torqued. Finally, one must be sure to torque the stud nut before soldering the device leads. Refer to Motorola Application Note AN-555 for details on mounting Motorola "stripline packaged transistors.

REFERENCES

1. P. H. Smith, "Electronic Applications of the Smith Chart", McGraw-Hill, 1969.
2. H. A. Wheeler, "Transmission-Line Properties of Parallel Wide Strips by a Conformal-Mapping Approximation" IEEE Trans. Microwave Theory and Techniques Vol. MTT-12, May 1964.
3. H. A. Wheeler, "Transmission-Line Properties of Parallel Strips Separated by a Dielectric Sheet" IEEE Trans. Microwave Theory and Techniques Vol. MTT-3, March 1965.
4. H. Sobol "Extending Microwave and Technology to Microwave Equipment" Electronics, March 20, 1967.
5. Microwave Engineers Technical and Buyers Guide, Edition of the Microwave Journal, 1969.

TUNING DIODE DESIGN TECHNIQUES

Prepared by:
Doug Johnson

INTRODUCTION

Voltage variable capacitors or tuning diodes are best described as diode capacitors employing the junction capacitance of a reverse biased PN junction. There is a wide range of available capacitances and different device types. The capacitance of these devices varies inversely with the applied reverse bias voltage.

Tuning diodes or Motorola's "Epicaps*" have several advantages over the more common variable capacitor. They are much smaller in size and lend themselves to circuit board mounting. They are available in most of the same capacitance values as air variable capacitors. Tuning diodes offer the designer the unique feature of remote tuning.

Epicaps, as opposed to earlier versions of voltage variable capacitors exhibit many new improvements. Lower leakage, significantly higher Q and uniformity are just some of these advantages. However, the capacitance of all tuning diodes inherently varies with temperature and may require compensation. A simple scheme is available for compensation of the temperature drift, resulting in stabilities as good as, or better than, that of air capacitors. This note contains the details for compensating Motorola's Epicap diodes.

SIMPLIFIED THEORY

A tuning diode is a silicon diode with very uniform and stable capacitance versus voltage characteristics when operated in its reverse biased condition. In accordance with semiconductor theory, a depletion region is set up around the PN junction. The depletion layer is devoid of mobile carriers. The width of this depletion region is dependent upon doping parameters and the applied voltage. Figure 1A shows a PN junction with reverse bias applied, while Figure 1B shows the analogy, a parallel plate capacitor. The equation for the capacitance of a parallel plate capacitor given below predicts the capacitance of a tuning diode.

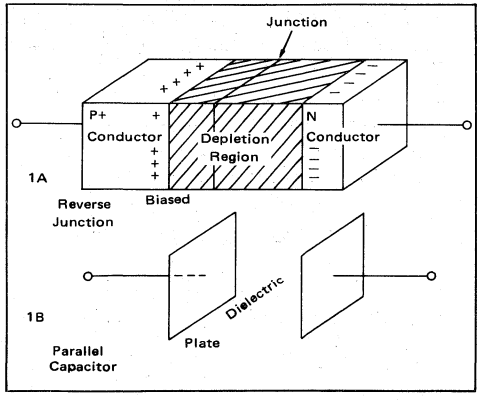


FIGURE 1 – Tuning Diode Capacitor Analogy

$$C = \frac{\epsilon A}{d} \quad (1)$$

where ϵ = dielectric constant of silicon equal to 11.8 x ϵ_0
$\epsilon_0 = 8.85 \times 10^{-12}$ F/m
A = Device cross sectional area
d = Width of the depletion layer.

The depletion layer width d may be determined from semiconductor junction theory.

The more accepted method of determining tuning diode capacitance is to use the defining formula for capacitance.

$$C = \frac{dQ}{dV} \quad (2)$$

The charge, Q per unit area, is defined as:

$$Q = \epsilon E \quad (3)$$

where E = Electric field

So we have capacitance per unit area:

$$c = \frac{C}{A} = \epsilon \frac{dE}{dV} \quad (4)$$

Norwood and Shatz[1] use these ideas to develop a general formula:

$$c = \left[\frac{q B \epsilon^{m+1}}{(m+2)(V+\phi)} \right]^{1/m+2} \quad (5)$$

m = Impurity exponent
c = Capacitance per unit area

Lumping all the constant terms together, including the area of the diode, into one constant, C_D, we arrive at:

$$C_J = \frac{C_D}{(V+\phi)^{\gamma}} \quad (6)$$

where γ = Capacitance Exponent, a function of impurity exponent
ϕ = The junction contact potential ($\approx$ 0.7 Volts)

The capacitance constant, C_D, can be shown to be a function of the capacitance at zero voltage and the contact potential. At room temperature we have:

$$C_D = C_O(\phi)^{\gamma} \quad (7)$$

C_O = Value of capacitance at zero voltage

The simple formula given in Eq. 6, very accurately predicts the voltage-capacitance relationship of Epicaps. There are many detailed derivations [1,2,3,4,5] of junction capacitance, so further explanation is not necessary in this note.

The capacitance of commercial tuning diodes must be modified by the case capacitance.

The equation then becomes:

$$C = C_C + C_J \quad (8)$$

where

C_C = Case capacitance typically 0.1 to 0.25 pF

C_J = Junction capacitance given by equation 6.

TUNING RATIOS

The tuning or capacitance ratio, TR, denotes the ratio of capacitance obtained with two values of applied bias voltage. This ratio is given by the following expression for the Epicap junction.

$$TR = \frac{C_J(V_2)}{C_J(V_1)} = \left[\frac{V_1+\phi}{V_2+\phi}\right]^{\gamma} \quad (9)$$

where $C_J(V_1)$ = Junction capacitance at V_1

$C_J(V_2)$ = Junction capacitance at V_2

where $V_1 > V_2$

In specifying TR, some Epicap data sheets use four volts for V_2. However, in order to achieve larger tuning ratios, the devices may be operated at slightly lower bias levels with some degradation in the Q specified at four volts. (See the discussion of Q versus voltage in the circuit Q section, later in this note). Furthermore, care must be taken when operating Epicaps at these low reverse bias levels to avoid swinging the diode into forward conduction upon application of large ac signals. These large signals may also produce distortion due to capacitance modulation effects.

Since the effects of ϕ and case capacitance, C_C, are usually small, Eq. 9 may be simplified to the following for most design work:

$$TR = \frac{C(V_{min})}{C(V_{max})} = \left(\frac{V_{max}}{V_{min}}\right)^{\gamma} \quad (10)$$

The frequency ratio is equal to the square root of the tuning ratio. This tunable frequency ratio assumes no stray circuit capacitance.

Another parameter of importance is γ, the capacitance exponent. Physically, γ depends on the doping geometry employed in the diode. Varactor diodes with γ values from 1/3 to 2 can be manufactured by various processing techniques. The types of junctions, their doping profiles, and resulting values of γ are shown in Figure 2. These graphs show the variation of the number of acceptors (N_A) and the number of donors (N_D) with distance from the junction.

Abrupt junctions are the easiest to manufacture and most Epicaps are of this type. This type of junction gives a γ of approximately 1/2 and a tuning ratio on the order 3 with the specified voltage range. Therefore the corresponding frequency range which may be tuned is about 1.7 to 1.0. A typical example is the MV2101:

$C(V_2) = C(30\ V) = 2.5$ pF

$C(V_1) = C(4\ V) = 6.8$ pF

TR = 2.7

$\gamma = 0.47$

The subscripts on the capacitance refer to the bias voltage applied.

In many applications, such as tuning the television channels, or the AM broadcast band, a wider frequency range is required. In this event, the designer must use a hyper-abrupt junction Epicap. The hyper-abrupt diode has a γ of 1 or 2, and much larger frequency ranges. Table I shows typical types of tuning diodes available, their tuning ratios, frequency ratios and junction types.

TABLE I SAMPLE TUNING DIODE TYPES

Device Series	Capacitances Available	Tuning Ratio	γ	Frequency Ratio	Junction Type
1N5139	47-6.8 pF	2.7-3.4	0.47	1.6-1.8	Abrupt
MV2101	100-6.8 pF	1.6-3.3	0.47	1.6-1.8	Abrupt
BB105	10 pF	4-6	1.0	2-2.4	Hyper-Abrupt
MV1400	550-120 pF	10-14	2.0	3.2-3.7	Hyper-Abrupt
MV109	30 pF	5-6.5	1.0	2.2-2.5	Hyper-Abrupt

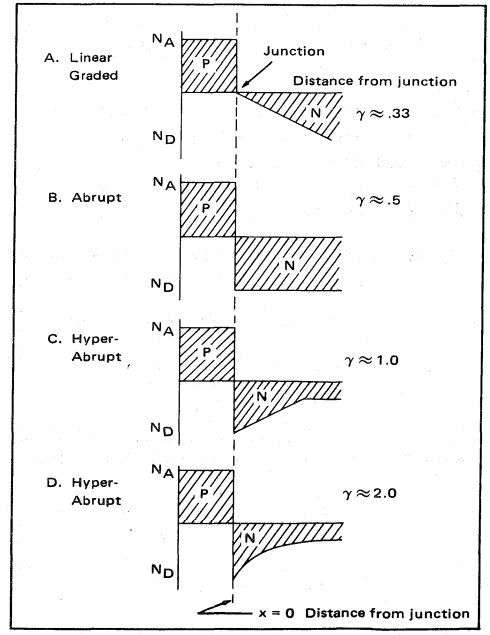


FIGURE 2 – Doping Profiles and Capacitance Exponent for Some Common Tuning Diode Types

6

The hyper-abrupt devices are constructed with special epitaxial growth and diffusion techniques, which creates a doping profile similar to that shown in Figures 2C and 2D. The Q of the BB105 and MV109 series hyper-abrupt diodes is as high as abrupt junction Epicaps. Their capacitance range is from a few picofarads to 10 or 20 pF, and their major application is in television tuners. The MV1400 series are high capacitance devices for applications below 10 MHz. They are suitable for tuning elements in AM broadcast band receivers and similar low frequency applications.

CIRCUIT Q

Popular types of mechanical tuning capacitors often have Q's on the order of a thousand or greater. The Q of tuned circuits using these capacitors is generally dependent only on the coil. When using an Epicap, however, one must be conscious of the tuning diode Q as well. The Q of the tuning diode is not constant being dependent on bias voltage and frequency. The Q of tuning diode capacitors falls off at high frequencies, because of the series bulk resistance of the silicon used in the diode. The Q also falls off at low frequencies because of the back resistance of the reverse-biased diode.

The equivalent circuit of a tuning diode is often described as shown: [7]

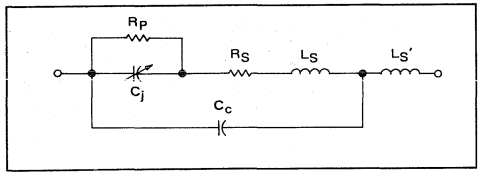


FIGURE 3 — Equivalent Circuit of Epicap Diode

where

R_p = Parallel resistance or back resistance of the diode
R_S = Bulk resistance of the silicon in the diode
L_S' = External lead inductance
L_S = Internal lead inductance
C_C = Case capacitance

Normally we may neglect the lead inductance and case capacitance. This results in the simplified circuit of Figure 4.

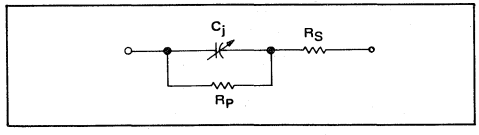


FIGURE 4 — Simplified Equivalent Circuit of Epicap Diodes

The tuning diode Q may be calculated with equation 11.

$$Q = \frac{2\pi f C R_p^2}{R_s + R_p + (2\pi f C)^2 R_s R_p^2} \qquad (11)$$

This rather complicated equation is plotted in Figure 5 for

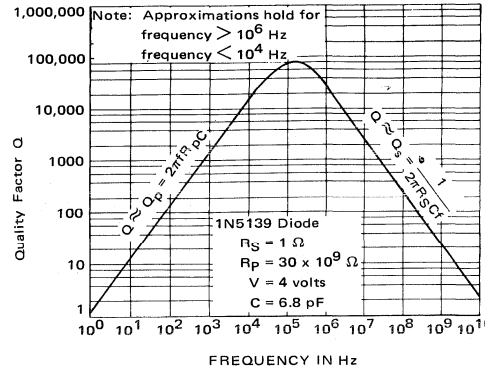


FIGURE 5 — Graph of Q versus Frequency

R_S = 1.0 ohm, R_p = 30 x 10^9 ohms, at V = 4 volts and C = 6.8 pF, typical for a 1N5139 Epicap at room temperature.

At frequencies above several MHz, the Q decreases directly with increasing frequency by the simpler formula given below:

$$Q \approx Q_S = \frac{1}{2\pi f C R_S} \quad \text{(High frequency Q)} \qquad (12)$$

The emphasis today is on decreasing R_S so better high frequency Q can be obtained. At low frequencies Q increases with frequency since only the component resulting from R_p, the back resistance of the diode, is of consequence.

$$Q \approx Q_p = 2\pi f C R_p \quad \text{(Low frequency Q)} \qquad (13)$$

Q is also dependent on voltage and temperature. Higher reverse bias voltage yields a lower value of capacitance, and also since R_S decreases with increasing bias voltage, the Q increases with increasing voltages. Similarly, low reverse bias voltages accompany larger capacitances, and lower Q's. Increasing temperature also lowers the Q of tuning diodes. As the junction temperature increases, the leakage current

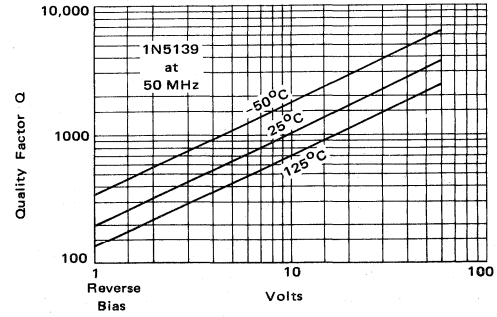


FIGURE 6 — Q versus Reverse Bias and Temperature

increases, lowering R_p. There is also a slight decrease in R_s with increasing temperature, but the effects of the decreasing R_p are greater and this causes the Q to decrease. The effects of temperature and voltage on the Q of a 1N5139 at 50 MHz are plotted in Figure 6.

TEMPERATURE

The Q and tuning ratio of Epicaps are parameters that every design engineer must be aware of in his circuits. Another equally important characteristic of tuning diodes is their temperature coefficient. A typical example of the capacitance versus temperature drift is shown in Figure 7.

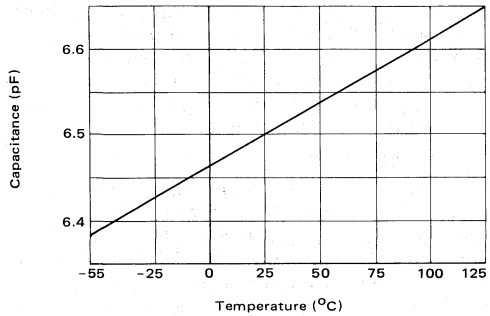


FIGURE 7 – Capacitance versus Temperature for a MV2101 Epicap Biased at 4 Volts

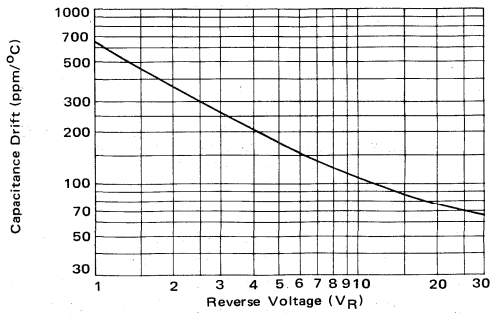


FIGURE 8 – Capacitance Drift in ppm/°C versus Voltage MV2101 Diode

The temperature constant, T_C, is a function of applied bias. Figure 8 shows T_C for a typical Motorola Epicap. Note that for low bias levels, on the order of a volt or two, the T_C is as high as +600 parts per million per degree centigrade (ppm/°C). This represents a frequency change of -300 ppm/°C which at 100 MHz means a frequency shift of 30 kHz per degree. It is obvious that a temperature compensation scheme is desirable for any frequency control not using feedback techniques.

In Figure 9, the actual capacitance drift of a MV2101 per degree centigrade is plotted. The graph illustrates that

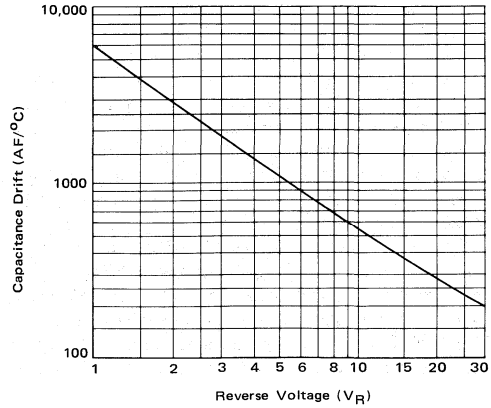


FIGURE 9 – Capacitance Drift in Attofarads/°C versus Voltage for the MV2101 Tuning Diode
Attofarads = (pF x 10^{-6})

a simple negative temperature coefficient compensating capacitor will not compensate for the tuning diode T_C because the change in capacitance is not constant with voltage.

A popular method of temperature compensating Epicaps involves the use of a forward biased diode. The voltage drop of a forward biased diode decreases as the temperature rises, thus applying a changing voltage to the Epicap. In the network shown in Figure 10, an increase in temperature

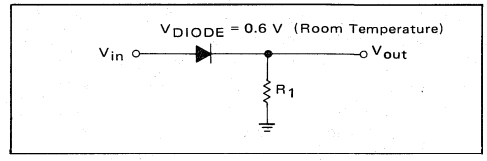


FIGURE 10 – Simple Temperature Compensating Network

will result in a decrease of the diode voltage V_{DIODE} to perhaps 0.5 V. If V_{in} is maintained constant, the available output voltage V_{out} will rise by 0.1 V. This increase in output voltage will lower the capacitance of the tuning diode and partially offset the initial capacitance increase caused by the temperature change. This method has been explored in detail and specific compensating circuits for Epicaps have been designed. The following sections describe the results of this work.

THEORY OF TEMPERATURE CHANGE

Before proceeding further with schemes to correct the temperature drift, it is informative to investigate the physical mechanisms responsible for the changing capacitance. Equations 6 and 8 may be combined to give the basic expression for capacitance below:

$$C = \frac{C_d}{(V+\phi)^{\gamma}} + C_c \qquad (14)$$

6

We can pinpoint the terms in Eq. 14 that may account for capacitance changes. The contact potential, ϕ, is a strong function of temperature, varying on the order of - 2 mV/°C. C_d is a function of geometric dimensions which can change with temperature and ϵ which changes with temperature. Case capacitance also changes with temperature. For this analysis we will assume the only terms not temperature dependent are the supply voltage V, and the capacitance exponent, which is a function only of the slope of the doping profile.

The contact potential, ϕ, is readily calculated from semiconductor theory, and the equations predict a large change with temperature. This change in ϕ will produce a much larger change in capacitance for lower voltages than for higher voltages, and therefore accounts for the majority of capacitance change in tuning diode temperature drift. See Table II.

TABLE II

Calculated capacitance change versus applied voltage in ppm/°C for:

$$\frac{d\phi}{dT} = -2 \text{ mV/°C}$$

$$C = \frac{C_d}{(V + \phi)^\gamma} + C_c$$

Applied Bias Voltage (Volts)	Capacitance Drift In (ppm/°C)
1	587
2	261
4	204
10	88.7
20	45.6
30	30.7

Comparing Table II with Figure 8, we see that a +40 to +50 ppm/°C temperature drift still remains. Therefore ϕ is not the only mechanism responsible for temperature drift and others must be sought. There is a change with temperature in physical dimensions in any material which has an affect on the order of 1 ppm/°C for a tuning diode. However, this change is too small to be of any significance. Another possibility is a change in dielectric constant. Silicon, depleted of its charge carriers, forms a dielectric layer with a relative dielectric constant of 11.8. The dielectric constant of silicon has a temperature coefficient of +35 ppm/°C. [1] These effects change the value of C_d with temperature.

Another effect which sometimes must be considered is the change in case capacitance with temperature. The case capacitance is about 0.25 pF for the plastic TO-92 case. And there is a change of +25 AF (attofarads = 10^{-6} pF) per degree centigrade. The glass DO-7 case exhibits a capacitance of about 0.20 pF and a change of +30 AF/°C. These are small changes for most low voltage capacitances, but become increasingly important as the voltage is increased and capacitance is reduced. Also these effects are only important for the low capacitance devices. For instance, consider the 1N5139 series which are packaged in the DO-7 glass case. Table III shows how large an effect case capacitance has on the capacitance drift of these diodes.

TABLE III Effect Of Case Capacitance Changes On 1N5139 And 1N5148 Epicaps

Bias Voltage (Volts)	1N5139		1N5148	
	Capacitance (pF)	Changes attributable to case capacitance (ppm/°C)	Capacitance (pF)	Changes attributable to case capacitance (ppm/°C)
2.0	8.9	3.4	61	0.5
4.0	6.4	4.7	47	0.6
10.0	4.8	6.3	32	1.0
30.0	3.0	10.0	19	1.6
60.0	2.2	14.0	13	2.3

In summary, the largest changes are caused by the change in contact potential. This effect is most noticeable at low voltage, high capacitance levels. The change in silicon dielectric is the next most important factor providing a change that is uniform for all devices and voltages. Case capacitance changes are most noticeable in the low capacitance, high voltage range, and may be neglected for all devices except those low capacitance devices.

THE POWER SUPPLY

We previously assumed that the supply voltage did not change with temperature. This is rarely the case, and special consideration must be given to this part of the design. All our efforts to temperature compensate the tuning diode may be in vain if the power supply has a large T_C or is otherwise unstable. Figure 11 shows the common method of supplying voltage to a tuning diode.

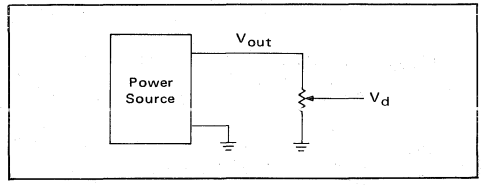


FIGURE 11 – Common Means of Supplying Bias Voltage to a Varactor Diode

POWER SOURCE

The power source is the most critical part of the circuit in Figure 11. It must be extremely stable in order to achieve good varactor tuning stability. The full drift of the power supply as expressed in ppm/°C will appear at V_d regardless of the setting of the potentiometer. For example, if V_{out} is 40 volts with a drift of 100 ppm/°C (4 mV/°C), V_d may be 10 V, but will still have a drift of 100 ppm/°C (1 mV/°C). A 50 ppm/°C stability figure in V_d translates into a 25 ppm/°C stability of capacitance, when the capacitance exponent is 0.5. For hyper-abrupt junctions we realize capacitance stabilities of 50 and 100 ppm/°C for exponents of 1 and 2 respectively.

There are many differing power supply regulators available to the designer. Zener diodes are relatively inexpensive, but have a poor temperature coefficient. Temperature compensated zeners are very expensive and have a limited voltage range. The MC1723, a monolithic integrated circuit voltage regulator, has excellent temperature characteristics, 37 volt output capability, and wide temperature range.

6

TABLE IV Summary of Power Regulators

Device	Voltage Range	Temperature Range	Voltage ppm/°C Max T_C	Voltage ppm/°C Typical T_C	Capacitance ppm/°C Typical $\gamma = 0.5$	Relative cost
1N5260 Zener	33	-65 +200°C	975	975	475	Low
1N4752 Zener	33	-65 +200°C	850	850	425	Low
1N3157 Temperature Compensated Zener	8.4	-50 +125°C	10	10	5	High
MC1723 Regulator	37	-55 +125°C	20	12	6	Medium
MFC6030 Functional Regulator	32	0° +70°C	50	15	7.5	Low
MC7800 Fixed Voltage Regulators	28	0° +125°C		40-60	20-30	Medium
MVS460 TO-92 Regulator	31 V	0 +70°C	-100 +50	-25	12	Low

Notes:
1) See Figure 12 for some typical circuit connections
2) More information on regulators is available in literature 8,9,10
3) To compute frequency change (ppm/°C), divide capacitance (ppm/°C) change by 2.

The MFC6030 Functional* integrated circuit is less costly and exhibits almost as good a temperature constant.

The MC7800 fixed output voltage regulators are extremely simple to use in that they have only input, output and ground terminals and require no external components other than possibly a high frequency bypass capacitor. (The latter item is generally required with all IC regulators to prevent high frequency oscillations).

The MVS460 is a two leaded IC regulator especially designed for use with tuning diodes. It represents a simple, inexpensive solution to the voltage regulator problem. Table IV contains a summary of available power supply regulators.

VARIABLE RESISTOR

The variable resistor is considerably less critical. Since it is being used as a voltage divider, all that is required is that the resistive material be uniform so any change in resistance is uniform throughout the potentiometer. Wire wound, and special high quality cermet film variable resistors are suitable for these applications. Generally speaking, a linear potentiometer should have a T_C of $\pm$150 ppm/°C or better. Special taper potentiometers should have a T_C of $\pm$50 ppm/°C or better.

The variable resistance cannot be made too large or there will be appreciable voltage drop as the reverse current in the diode increases. The reverse current in a silicon diode generally doubles every 10°C so this becomes an important problem at temperatures above 50°C. If the temperature is expected to run as high as 70°C, one must limit the variable resistor to 50 kΩ or the effect will be a greater than 5 ppm/°C capacitance change. If 50°C is the upper temperature limit, the resistance may be upped to 150 kΩ. These values apply to all of Motorola's Epicap series. When the tuning diodes are used in applications where temperature will greatly exceed 70°C, the divider resistance should be kept below 10 kΩ. This low value requires large power supply currents and would be undesirable in some applications. However, since the Motorola MC1723 is the recommended power source at these temperatures, voltage control may be accomplished using the regulator without relying on an external divider potentiometer, as shown in Figure 12A. The MC1723's low output impedance of 0.05 ohms will easily and reliably handle the change in current demanded by the Epicap as it heats up. Figure 12B shows another popular regulator circuit. If higher or lower voltages are needed, schemes such as voltage boost[8] and floating regulators may be used.

*Trademark of Motorola Inc.

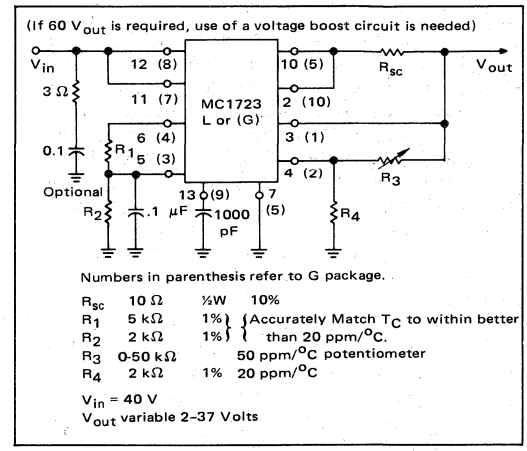


FIGURE 12A — High Stability Regulator -50 to +125°C

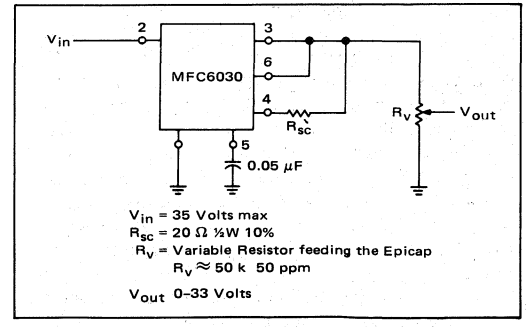


FIGURE 12 B — Regulator Using MCF6030, 0° — 70°C

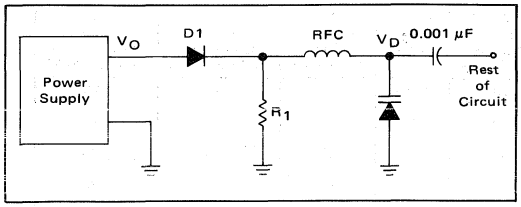


FIGURE 13 – Temperature Compensation Using A Silicon Diode

TEMPERATURE COMPENSATION

It has been previously noted that the most effective means of temperature compensation is simply to use a silicon junction biased in the forward direction. A circuit employing this technique is shown in Figure 13.

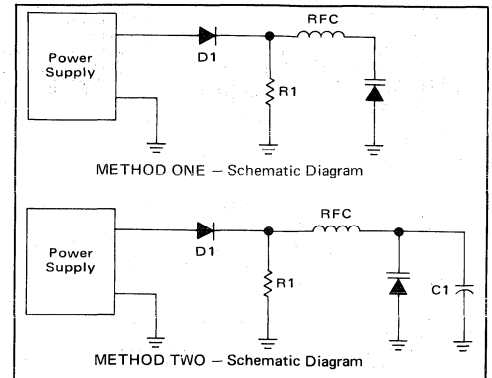
Diode D1 has a forward voltage drop on the order of 0.6 volts, and a temperature coefficient of -0.002 V/°C. Assuming a constant voltage from the supply, the reduction in diode voltage with increasing temperature, increases the voltage available to the tuning diode, V_D. The higher tuning diode voltage, V_D, lowers the capacitance enough to compensate for the increase due to temperature. However, merely using a random diode with an arbitrary value of R1 will not result in very accurate temperature compensation.

Different correction devices exhibit different T_C (changes in voltage drop with temperature) values because of differing doping schemes. For example, a typical Epicap exhibits a T_C of approximately – 1.5 mV/°C while some high current rectifier junctions measure as high as -2.6 mV/°C. So it is necessary to investigate many different junction devices in order to find a diode that adequately compensates the tuning diode drift.

The tuning diode's change with temperature must be accurately determined. Also of major importance is the value of R1. A typical junction may have a T_C of -1.5 mV/°C at 10 mA junction current, and a T_C of -2.8 mV/°C at 1 μA junction current. Thus the value of R1, the bias resistor, must be chosen to yield the optimum value of compensating diode current.

Detailed analysis was performed on 160 low cost junction devices in order to arrive at suitable compensation schemes for Motorola's Epicaps. The results appear in Table V. The correction diodes represent the devices which provided the most accurate and reliable compensation. A computer program was devised to optimize the value of R1 in each case. Two different methods of compensation were analyzed. Method one searches for the lowest ppm values without using C1, the temperature compensating capacitor. At some voltages the temperature corrected tuning diode will have a negative temperature coefficient, while at others it will be positive. In general the results are better than ±50 ppm over the entire range from 2 volts to the breakdown voltage of the Epicap diode.

Method two attempts to cluster the residual capacitance at some standard value after the diode has performed its



Note 1: To find the value of negative temperature coefficient capacitor, C1, use equation 15.

$$C_1 = \frac{C_X \cdot C_{TD}}{N} \text{ in pF} \qquad (15)$$

where

C_X = Value listed above in Table V
C_{TD} = Capacity in pF of the tuning diode at four volts
N = Temperature coefficient of capacitor.
If a N750 is used, N = 750.

Note 2: For MV2305 series, the ppm/°C drift values specified hold for 1.5 V to the breakdown voltage.

correction. This value (due to silicon dielectric change, case capacitance change, etc.) is easily "tuned out" by means of a small negative temperature coefficient capacitor.

Consideration must be given to the stability of R1. As the resistance of R1 increases with changing temperature, less current will be drawn through D1, thus decreasing its voltage drop. The result will be a rise in the voltage applied to the Epicap. Analysis of this effect is shown in Table VI.

The results of using a MV2111 in the compensation circuits are shown in Figures 14A and 14B. Only the diode,

TABLE VI

TUNING DIODE BIAS VOLTAGE

ppm Accuracy of R1	1 V	2 V	5 V	25 V	
±10 ppm	1	1	–	–	PPM CAPACITANCE CHANGE
±25 ppm	3	2	1	–	
±50 ppm	6	4	2	1	
±100 ppm	12	7	4	2	
±200 ppm	24	14	8	4	

Keeping cost in mind, ±100 ppm or ±50 ppm 1% resistors are recommended for R1.

resistor R1, tuning diode, and capacitor C1 if used were subjected to temperature changes. Thus, any effect of power supply variation and variable resistor instability were neglected.

Actual circuits constructed will not be as accurate as these test results because the power supply and variable resistor will contribute some instability. Some of the variations that will occur are shown in Table VII.

The effects of tuning diode variation and correction diode variation are accounted for in Table V. The effects

TABLE V

Tuning Diode	Correction Diode	Method One R1	Typ ppm Method One -50 to 125°C	Max ppm Method One -50 to 125°C	Method Two R1	Method Two C_X Note 1	Typ ppm Method Two -50 to 125°C	Max ppm Method Two -50 to 125°C
MV2101 Series	MSD6100	50 k to 70 k	-30 to +40	±50	8.2 k	23	±15	±25
	1N4001	20 k to 30 k	-40 to +40	±60	–	–	–	–
	*2N5221	250 k to 400 k	-30 to +40	±55	33 k	23	±15	±25
	*MPS5172	250 k to 400 k	-35 to +40	±60	47 k	23	±15	±25
	*MPS3904	–	–	–	180 k	23	±20	±30
1N5139	MSD6100	400 k to 600 k	-30 to +50	±60	120 k	16	±25	±35
Series	1N4001	400 k to 600 k	-30 to +45	±50	82 k	15	±20	±30
	MPS5172	–	–	–	600 - 800 k	15	±25	±35
MV2305 Series	MSD6100	40 k to 60 k	-40 to +50	±60	–	–	–	–
Note 2	1N4001	15 k to 25 k	±45	±65	–	–	–	–
	*2N5221	250 k tp 350 k	±45	±70	18 k	35	±15	±25
	*MPS5172							
	*MPS3904	–	–	–	100 k	34	±15	±25
MV3500 Series	MSD6100	30 k to 40 k	±40	±60	–	–	–	–
	*2N5221	120 k to 180 k	-35 to +45	±55	–	–	–	–
	*MPS5172							
	*MPS3904	–	–	–	56 k	22	±15	±25
1N5441 & 1N5461	MSD6100	400 k to 500 k	±45	±60	68 k	22	±20	±30
Series	1N4001	400 k to 500 k	±50	±60	22 k	22	±20	±30
	*2N5221	–	–	–	390 k	22	±20	±35
	*MPS5172							

*Base-Emitter junction used as a diode.

TABLE VII Other Error Contributing Factors In Temperature Compensation

	Typical ppm/°C
Power Supply Variation	±8
R1 Changes	±5
Changes in Epicap Current through Potentiometer	±5
Potentiometer Nonlinearities	±2
Tuning Diode Variation	±10
Correction Diode Variation	±15

of power supply and potentiometers must be accounted for separately and decrease the total accuracy. If a ±25 ppm/°C correction scheme is used, but the power supply has ±25 ppm/°C stability, an overall stability of ±35 ppm is obtained. This apparent error results from the fact that the error factors cannot be added directly, but must be summed as vectors in accordance to the rules of error theory. It is important to consider the whole circuit when designing for temperature compensation.

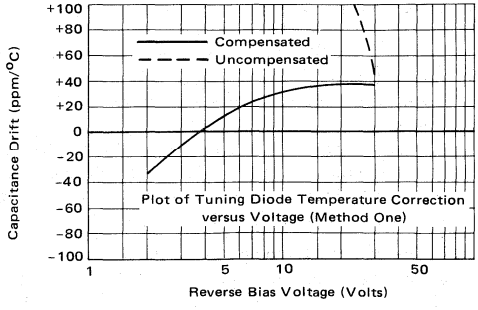


FIGURE 14A – MV2111, MSD6100 Compensation Diode
R1 = 68 k

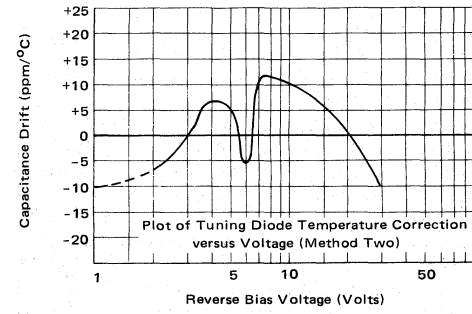


FIGURE 14B – MV2111, MSD6100 Compensating Diode
R1 = 8.2 k
C1 = 3.3 pF (N330)
0.00109 pF/°C

HYPER-ABRUPT TEMPERATURE DRIFT

The hyper-abrupt tuning diode is more sensitive than other types to temperature variations resulting in a greater need for temperature compensation. Also their drift with temperature is not as uniform as abrupt junction tuning diodes. Their drift factors expressed in ppm/°C run as high as 800 to 1200 for the units with a γ of 2. Units having a γ of 1 typically show 300 to 400 ppm/°C capacitance changes. These higher drift rates are caused by the

hyper-abrupt tuning diode's greater sensitivity to changes in voltage, and the fact that the majority of capacitance change is caused by the change in contact potential, ϕ. This greater sensitivity to voltage changes means that power supply and other instabilities will also have a larger effect than with regular abrupt junction tuning diodes.

As a first order approximation, a MPS3904 transistor's emitter-base junction with a 50 k resistor used for R1 will improve the temperature drift in capacitance to better than 200 ppm/°C. Improvement from this point can only be obtained by a trial and error method described below.

Figure 15 shows the variation in compensation as R1 is varied for the MV3142, a hyper-abrupt tuning diode. As R1 is increased in value, the ppm/°C value is made more negative. The effect of the change is greatest at lower voltages.

To completely compensate the drift factor of the MV3142 shown in Figure 15 would be very difficult due to the variation of the curve shape. However, improved compensation may be achieved by limiting the diode to an operating voltage range of 2 to 15 volts. Starting with an R1 value of 50 k, the tuning diode and compensation circuit should be varied in temperature, while measuring the capacitance change. If the drift factor is more positive than desired, R1 may be increased in value. Referring to Figure 15, a temperature drift factor of +40 ppm/°C at 2 V may be larger than can be tolerated. Substituting a 200 k resistor will reduce the value to 25 ppm/°C at 2 V. In order to accurately compensate at any voltage, it is only necessary to vary R1 while measuring the capacitance drift. If the required value for R1 becomes larger than 750 k, the compensating junction type should be switched to a MSD6100, and the bias resistor started at 50 k again.

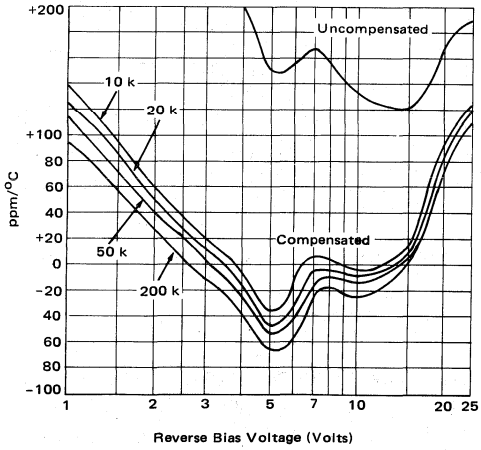


FIGURE 15 – MV3142 Tuning Diode Compensation For Differing Values of R1

SUMMARY

Voltage variable capacitors are rapidly replacing air variable capacitors in many applications. These devices offer many advantages over previous variable capacitors, such as the ability to employ remote tuning. By carefully considering the proper design conditions, such as temperature drift, and designing accordingly, Epicaps can replace air capacitors in virtually all but high power applications. The designer must be aware of the tuning range and Q limitation in order to use these devices effectively. Temperature drift should cease to be a problem when proper compensation schemes are used.

BIBLIOGRAPHY

1. Norwood, Marcus; and Shatz, Ephraim, "Voltage Variable Capacitor Tuning: A Review." IEEE, 56:5, May 1968, pp. 788-98.
2. Chang, Y.F., "Capacitance of p-n Junctions: Space Charge Capacitance." Journal of Applied Physics, 37:6, May 1966, pp. 2337-42.
3. Gimmel, H.K.; and Schauftter, D.L., "Depletion Layer Capacitance of p^+n Step Junctions." Journal of Applied Physics, 38:5, April, 1967, pp. 2148-53.
4. Gray, P.E.; DeWitt, D.; Boothroyd, A.; Gibbons, J., Physical Electronics and Circuit Models of Transistors. New York, John Wiley & Sons, 1964, pp. 8-54.
5. Warner, R.; Fordemwalt, J., Integrated Circuits, Design Principles and Fabrication, New York, McGraw-Hill, 1965, pp. 31-68.
6. John Hopkins, "A Printed Circuit VHF TV Tuner Using Tuning Diodes," Motorola Application Note AN-544A.
7. G. Schaffner, "Designing Around The Tuning Diode Inductance," Motorola Application Note AN-249.
8. Don Kesner, Marv Gienger, "Voltage and Current Boost Techniques Using The MC1560-61," Motorola Application Note AN-498.
9. Ed Renschler and Don Schrock, "Development, Analysis, and Basic Operation of The MC1560-61 Monolithic Voltage Regulators," Motorola Application Note AN-500.
10. Don Kesner, "Regulators Using Operational Amplifiers," Motorola Application Note AN-480.

MOUNTING STRIPLINE-OPPOSED-EMITTER (SOE) TRANSISTORS

Prepared by Lou Danley

INTRODUCTION

The Stripline Opposed Emitter (SOE) package presently used by Motorola for a number of rf power transistors represents a major advancement in high frequency and thermal performance. This Application Note discusses the SOE package, it advantages and limitations as well as a number of considerations to avoid improper usage.

An understanding of a few basic principles in regard to mounting and heat-sinking of this package can help avoid cases of poor performance or device damage.

Two general package types – the stud-mounted and flange-mounted SOE packages will be discussed. Each of the general types is available in a variety of sizes. Typical package outlines of the two SOE packages are shown in Figure 1.

ADVANTAGES OF THE SOE PACKAGE

The primary electrical advantages of the SOE packages are the low inductance strip line leads which interface very well with the microstrip lines often used in UHF-VHF equipment and the good collector to base isolation provided by the two emitter leads. The two emitter concept promotes symmetry in board layout when combining devices to obtain higher output power. Both emitter leads should always be used for best performance.

DESCRIPTION OF THE SOE PACKAGE

Figure 2 displays the component parts on a stud-mounted SOE package. This package will be used as an example since both the stud and flange-mounted packages are very similar in construction. The body of the package is a Berylium Oxide (BeO) disc. Berylium Oxide was chosen due to its high thermal conductivity. Attached to the bottom of the disc is a copper stud which is for heat transfer and mechanical mounting. The lead frame is attached to a metalized pattern on to the top surface of the BeO disc. The actual shape of the leads differs between the various package types. Finally an Alumina ceramic cap is attached to the top of the disc over the leads providing a protective cover for the transistor die.

An understanding of the basic structure of the SOE package is essential to proper usage of these devices in respect to heat-sinking and mechanical mounting. Since these two areas present the greatest problem to users, they will be discussed in detail.

HEAT-SINKING THE SOE PACKAGE

In order to properly understand the thermal considerations involved in mounting SOE type packages, it is necessary to lay some groundwork in the area of heat flow. Table I gives equivalent Thermal and Electrical parameters which may be used to relate Thermal properties to more familiar electrical units.

Semiconductor power devices are usually guaranteed to have a certain thermal performance as stated by the thermal resistance of the device from the junction to the case, or mounting surface – θ_{JC}. How to get the heat out of the

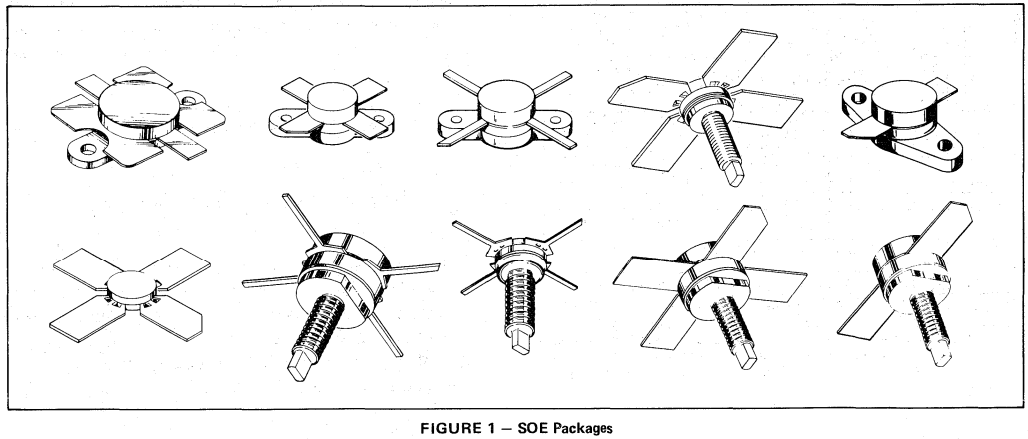


FIGURE 1 – SOE Packages

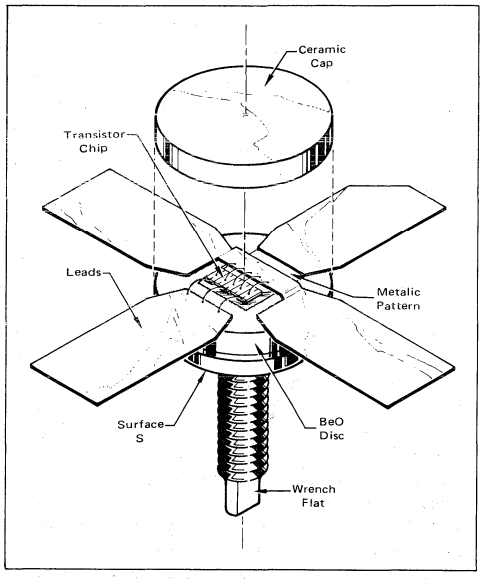


FIGURE 2 – Component Parts of SOE Package

case has generally been left to the user. In any dynamic heat flow problem, the heat must go somewhere, otherwise there will be a continuous rise in the temperature of the system. In text books, there always seems to be an "infinite heat sink" available which can absorb any amount of heat with no temperature rise whatsoever. In the practical sense, however, such a heat sink does not really exist. Practical heat sinks must be characterized by a certain temperature rise for a given ambient condition, with a known amount of heat input (power to be dissipated) after equilibrium conditions have been achieved. Characterization of heat-sink systems is best achieved by examining the complete system under controlled conditions.

TABLE I – Thermal Parameters and Their Electrical Analogs

Thermal			Electrical Analog	
Symbol	Parameter	Units*	Symbol	Parameter
ΔT	Temperature difference	^{o}C	V	Voltage
H	Heat flow	watts	I	Current
θ	Thermal resistance	^{o}C/watt	R	Resistance
γ	Heat capacity	$\frac{\text{watt-sec}}{^{o}C}$	C	Capacity
K	Thermal conductivity	$\frac{\text{cal}}{\text{sec-cm-}^{o}C}$	σ	Conductivity
Q	Quantity of heat	cal	q	Charge
t	Time	sec	t	Time
$\theta\gamma$	Thermal time constant	sec	RC	Time constant

*Note the one major difference in thermal and electrical units; Q is in units of energy, whereas q is simply a charge. Hence H is in units of power and may be equated to an electrical power dissipation.

For example, the normal environment for a land-mobile VHF transmitter might be the trunk of a taxi cab in the hot Arizona summer. In such an environment, temperatures might reach as high as 80°C (176°F). The heat-sink system for such a radio should therefore be tested at a minimum ambient temperature of 80°C. The method that should be applied in this test would utilize a fine wire thermocouple rigidly secured to the stud of the rf power transistor for which the test is being conducted. The system, which in this case would include all parts of the radio which would contribute heat, should then be operated under maximum heat generating conditions, in the high temperature environment specified. Careful measurement of the temperature of the device under test would then give the difference in temperature between the case of the transistor and the controlled ambient.

If the case and ambient temperatures are known, as well as the power levels in the transistor, the thermal resistance from the transistor case to the ambient can be calculated. The first step is to obtain the power being dissipated by the device.

$$P_d = P_1 + P_2 - P_3 \quad (1)$$

where: P_d = power being dissipated by the transistor in watts;

P_1 = dc power into the transistor in watts;

P_2 = rf power into the transistor in watts;

P_3 = rf power out of the transistor in watts.

This value of P_d is used to obtain the θ_{CA} value from the equation:

$$\theta_{CA} = \frac{T_C - T_A}{P_d} \quad (2)$$

where: θ_{CA} = thermal resistance device case to ambient;

T_C = device case temperature;

T_A = ambient temperature.

In order to determine the maximum temperature rise in the transistor element (junction temperature rise) under any given operating condition the following equation may be used.

$$T_j = (\theta_{JC} + \theta_{CA})P_d + T_A \quad (3)$$

where: T_j = junction temperature;

θ_{JC} = published thermal resistance – junction to case.

If power is dissipated in a power transistor, the case temperature will rise above the ambient temperature by an amount determined by θ_{JC} and θ_{CA}. Since the value to θ_{JC} is fixed by the transistor type being used, θ_{CA} is the only factor with which the user can control the junction temperature for a given power dissipation.

Since heat generated by the transistor must be radiated to the ambient by the heat sink, a low θ_{CA} requires an effective heat sink. In general, an efficient heat sink requires that material with high thermal conductivity and high specific heat be used. A table of thermal properties for various materials is given in the Appendix. A well-designed heat sink requires that all thermal paths be as short as possible and of maximum cross-sectional area. Examples of thermal resistance calculations for a bar and a flat disc of thermal conducting material are given in the Appendix.

The equations given in the Appendix however, assume no thermal resistance between the case and the heat sink.

The primary heat conducting surface on stud-mounted SOE packages is the flat metal surface between the actual stud and BeO case body labeled surface S in Figure 2. This surface, which has a D-flat on some case types, must make good contact with the heat sink to allow good thermal conduction. To insure good contact: a) the heat sink mounting surface must be flat, b) the mounting hole must be burr free, the proper size and perpendicular to the mounting surface, c) the proper sized nut should be used and d) the nut should be properly torqued. Recommended mounting hardware is given in the section on device mounting.

With flange-mounted devices the primary parameters affecting thermal transfer are the flatness of the heat sink surface and the flatness of the device flange. The flange-mounted package requires that good contact be made between the flange and the heat-sink surface, particularly directly beneath the BeO disc.

With either of these packages it has been found that a considerable improvement in thermal transfer can be achieved through the proper use of one of the silicone based "heat-sink compounds" which are marketed by several vendors. Dow Corning and Wakefield Engineering are both suppliers of good thermal compounds. It should be pointed out however, that these compounds have a thermal conductivity approximately equal to that of Mica (0.0018 Cal/Sec-cm-^{o}C) which is poor compared to that of Aluminum (0.49 Cal/Sec-cm-^{o}C). However by comaprison, the thermal conductivity of still air is approximately 0.000006 Cal/Sec-cm-^{o}C). The quantity of silicone grease used must be kept to the absolute minimum required to fill in any air gaps which might occur between the transistor mounting surface and the heat-sink surface. In the case of the stud-mounted package this is the gap after the transistor has been secured with the proper stud torque. Contributions of as high as 0.5^{o}C/watt to the overall thermal resistance can occur if the heat-sink compound is used in a sloppy and excessive manner.

MOUNTING SOE DEVICES

The second area demanding consideration by a user of SOE transistors is mechanical mounting. Failure to observe proper mounting procedures can result in device destruction. This section will discuss both the stud-mounted, and the flange-mounted SOE devices.

Seven general considerations for properly mounting SOE transistors are listed briefly below. More detailed discussion will follow.

A. The device should never be mounted in such a manner as to place ceramic to metal joints in tension.

B. The device should never be mounted in such a manner as to apply force on the strip leads in a vertical direction towards the cap.

C. When the device is mounted in a printed circuit board with the copper (stud or flange) and BeO portion of the header passing through a hole in the circuit board, adequate clearance must be provided for the BeO to prevent shear forces from being applied to the leads.

D. Some clearance must be allowed between the leads and the circuit board when the device is properly secured to the heat sink.

E. The device should be properly secured into the heat sinks before the device leads are attached (soldered) into the circuit.

F. The leads must not be used to prevent device rotation on stud type devices during stud torque application. A wrench flat is provided for this purpose.

G. With stud packages, maximum stud torque, as stated later in this note, and on the respective device data sheets must not be exceeded. If repeated assembly/disassembly operation is expected, a lesser torque should be used.

Most of the considerations listed above are designed to prevent tension at the metal-ceramic interfaces on the SOE package. Improper mechanical design can lead to application of stresses to these joints resulting in device destruction. Three joints are considered: The cap to the BeO disc, the leads to the disc, and the stud or flange to the disc.

The joint between the ceramic cap and the BeO ceramic disc is composed of a material which loses strength above 175°C. While the strength of the material returns upon cooling, any force applied to the cap at high temperature may result in failure of the cap to ceramic joint.

The lead frame and stud or flange attachment will be grouped together since they are very similar. Although the SOE package used by Motorola makes use of high temperature ($>$ 700°C) solder alloys for lead frame and flange or stud attachment, care should be taken to avoid the application of tensile forces to the joint in the mounting of the transistor into a system. Such forces could result if the device were mounted with improper mounting clearances.

MOUNTING THE STUD TYPE SOE TRANSISTOR

Figure 3 shows a cross-section of a printed circuit board and heat sink assembly for mounting a stud type SOE device. Let us define H as the distance from the top surface of the printed circuit board to the D-flat heat sink surface. If H is less than the minimum distance from the bottom of the lead material to the mounting surface of the SOE

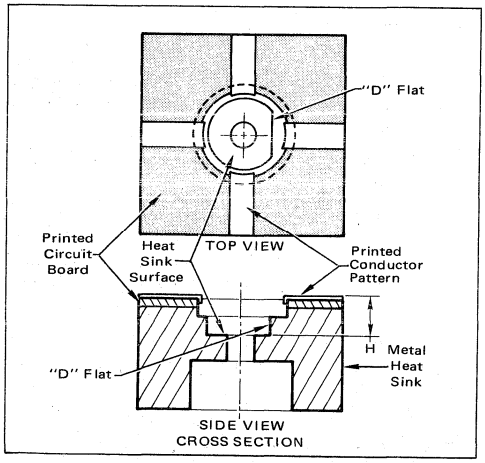


FIGURE 3 – Typical Stud-Mounting Method

package, there is no possibility of tensile forces in the copper stud – BeO ceramic joint. If, however, H is greater than the package dimension, considerable force is applied to the cap to BeO joint and the BeO to stud joint. Two occurances are possible at this point. The first is a cap joint failure when the structure is heated, as might occur during the lead soldering operation; while the second is BeO to stud failure if the force generated is high enough. Lack of contact between the device and the heat sink surface will occur as the difference between H and the package dimension becomes larger, this may result in device failure as power is applied.

Proper stud torque is an important consideration when mounting stud type SOE devices.* The stud section of the SOE package is composed of a special copper alloy chosen because of its high thermal conductivity. However when this material is used in studded semiconductor device packages, it is necessary to place severe restrictions on the amount of tightening torque which can be applied to a nut used to secure the device to a heat sink.

*The Motorola Outline Dictionary calls for Class 2A threads. The National Bureau of Standards Handbook H28 entitled Screw Thread Standards, paragraph 4.2 on page 2.17, reads in part as follows:

> "However, for threads with additive finish, the maximum diameters of Class 2A threads may be exceeded by the amount of the allowance; i.e., the 2A maximum diameters apply to an unplated part or to a part before plating whereas the basic diameters (the 2A maximum diameter plus allowance) apply to a part after plating."

Also, footnote b, page 2.37 reads:

> "For Class 2A threads having an additive finish, the maximum is increased to the basic size, the value being the same as for Class 3A."

This means that for plated parts, the no-go gauge used is the 2A minimum and the go gauge used is the 2A maximum plus the allowance or, in other words, the 3A maximum.

The recommended torque values are listed below for the two thread sizes presently being employed on Motorola rf power transistor packages.

Recommended maximum torque for stud SOE transistors follows:

	8 – 32 Threads	10 – 32 Threads
One time maximum	6.5 lb.-in.	11.0 lb.-in.
Repeated assembly–assembly maximum	5.0 lb.-in.	8.5 lb.-in.

An evaluation of the effects of measured torque on the studs under consideration requires a known set of conditions. The system used to generate the data shown in Figure 4 consisted of a 1/8 inch aluminum plate with a deburred clearance hole for the stud under test, a steel washer to be positioned between the plate and appropriate steel nut. A calibrated torque wrench was used as the driving means. On each unit under test, the spacing separating four threads positioned between the nut and heat-sink surface was measured. After mounting the device on the aluminum plate and applying a known amount of torque the spacing was again measured and the results recorded.

The results of this test show that up to the maximum torque specified, the permanent elongation of the threads increases linearly with applied torque. At the torque specified this elongation does not exceed acceptable limits.

MOUNTING THE FLANGE TYPE SOE TRANSISTOR

The mounting and heat sinking of the flange type package is similar to that of the stud type package. The main considerations with the flange package are avoiding tensile stresses at the metal-ceramic joints and providing a flat heat conducting surface beneath the flange.

Figure 5 shows a typical mounting technique for flange type SOE rf power transistors. Again H is defined as the distance from the top of the printed circuit board to the heat-sink surface. If distance H is less than the minimum distance from the bottom of transistor lead to the bottom surface of the flange, tensile forces at the various joints in the package are avoided. However, if distance H exceeds the package dimension, problems similar to those discussed for the stud type devices can occur. Because of the ability

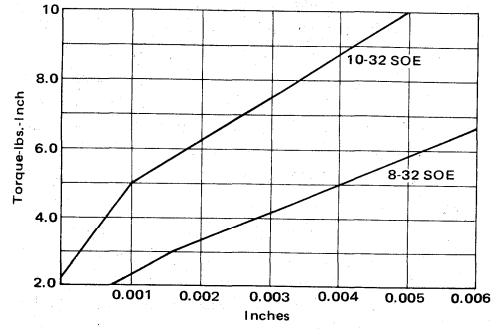


FIGURE 4 – Permanent Elongation Over a Four Tooth Length

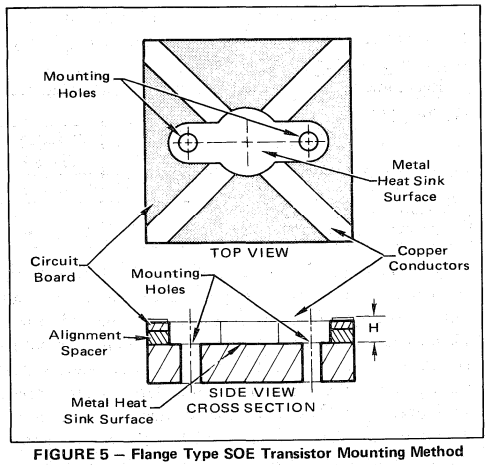


FIGURE 5 – Flange Type SOE Transistor Mounting Method

of the copper flange to bend under the types of loads encountered when the mounting screws are tightened, permanent deformation of the flange may result. Corrective action after the flange has been bent will not necessarily insure proper thermal contact with the heat sink.

The flange surface as supplied with Motorola SOE transistors is either flat or slightly convex. It is important that the mating heat-sink surface also be flat or slightly convex to provide the best contact when the device is properly secured.

The holes for the mounting screws should be deburred because any irregularity of the surface at these two points is equivalent to concavity of the heat-sink surface which will degrade thermal contact between the transistor and the heat sink.

Since the flange may be permanently deformed during mounting, the device should not be dismounted and remounted in another position.

CONCLUSION

The SOE package is an excellent rf power transistor package. However, improper heat sinking and mechanical mounting can result in device damage. A number of considerations have been presented to inform the potential user of the hazards of improper mounting. Proper usage of the SOE package requires no great difficulty if the designer is aware of the limitations and construction of the package.

A list of recommended mounting hardware and a suggested mounting procedure follows:

Table of Recommended Mounting Hardware Which Can be Supplied With Motorola Stud Type SOE Transistor

Stud Thread Size	Motorola Part Numbers		
	Nut	Flat Washer	Lock Washer
10-32	02BSB51568F044	04BSB51567F040	04BSB51566F028
8-32	02BSB51568F042	04BSB51567F038	04BSB51566F030
6-32	02BSB51568F040	04BSB51567F036	04BSB51566F032

STEPS IN A PROPER MOUNTING PROCEDURE

1. Compare the distance between the heat sink surface and the top of the printed circuit board with the minimum dimension of the transistor from the mounting surface to the bottom of the leads. The transistor dimension, as stated on the device data sheet, should be the greater distance to avoid the chance of stresses on the various joints of the SOE package.

2. Bore the proper sized mounting hole or holes for the stud or mounting screws. These holes should be perpendicular to the heat sink surface and they should be properly deburred.

3. Place a limited amount of thermal compound on the heat sink surface where it will contact the flange or mounting surface above the stud. Insert the transistor and mount with the proper hardware as suggested in the preceeding table.

   In the case of the stud device, torque the nut to the proper value.

4. Solder the leads to the printed circuit board using the minimum amount of heat and the least possible time of application. The leads should be soldered as close to the package as possible to minimize series lead inductance.

5. With the unit exposed to the highest expected ambient temperature, and power applied, measure the temperature at the stud or flange surface with a thermocouple to insure that this temperature is not excessive. Before production quantities are commited, it is suggested that a sample assembly to be tested under worst case heat generating conditions.

APPENDIX

In order to aid in heat-sink design, a table of thermal properties of common materials and a pair of thermal conductivity examples are presented.

Table AI gives three important thermal properties of common heat-sink materials. In order to evaluate materials for use in heat sinks these three thermal properties should be considered.

Thermal conductivity is a measure of the ability of a material of known cross-sectional area to transfer heat a given distance in a given time with a given temperature difference. Generally metals are good thermal conductors.

Specific heat is a measure of the amount of heat a given mass of material can accept for a given rise in temperature. The scale is normalized to the heat capacity of water ($H_2O = 1.0$).

Mass density is simply the mass per unit volume of a material. This parameter is important in heat sink design to the extent that large heat sinks of dense material carry with them a serious weight penalty.

TABLE AI – Typical Thermal Properties of Materials

Material	Thermal Conductivity K (cal/sec-cm-°C)	Specific Heat S (cal/gm-°C)	Mass Density ρ (gm/cm°C)
Silver	0.97	0.056	10.5
Copper	0.92	0.093	8.9
Gold	0.69	0.030	19.3
Beryllia-Ceramic	0.55	0.31	2.8
Aluminum	0.49	0.22	2.7
Brass	0.26	0.094	8.6
Silicon	0.20	0.18	2.4
Germanium	0.14	0.074	5.5
Steel	0.12	0.12	7.8
Solder	0.09	0.04	8.7
Kovar	0.046	0.11	8.2
Alumina-Ceramic	0.04	0.21	3.7
Plastic-Epoxy	0.0026	0.2	2.0
Glass	0.0026	0.20	2.2
Mica	0.0018	0.20	3.2
Teflon	0.00056	0.25	2.2
Air	0.000057	0.24	0.0013
Heat Sink Compound	0.0018	–	–

Example 1.

In order to present some of the important characteristics to be used in heat sink design, the examination of two admittedly simplified models is desirable. The analogy between electrical resistivity and thermal resistivity will be employed.

The first of these is shown in Figure A1.

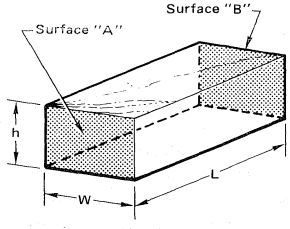


FIGURE A1 – A Bar of Thermal Conducting Material

The electrical resistance from Surface A to Surface B of this bar of conductive material is:

$$R = \frac{\rho L}{hW} \qquad (A1)$$

Using the electrical to thermal analogs:

$$\theta = \frac{L}{KhW} = \frac{L}{KA} \qquad (A2)$$

This simplified model might represent a pedestal mount or a device mount in the center of a bar connecting at either end to a housing, and demonstrates the need for thermally conducting paths of high cross-sectional area and the shortest possible length.

Example 2.

The second simple model represents the mounting of the power device on a plate of conducting material which provides the conducting path to the ambient conditions.

Consider the simple disc geometry shown in Figure A2 as a donut-shaped sheet resistor. Equation A3 represents the electrical resistance between r1 and r2,

$$R = \frac{\rho}{2\pi x} \ell n\left(n \frac{r2}{r1}\right) \qquad (A3)$$

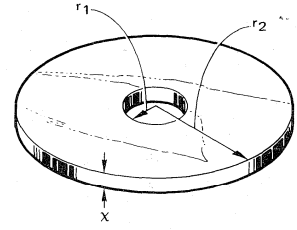


FIGURE A2 – Disc-Shaped Thermal Conductor

using the first term of the appropriate power series expansion

$$R \approx \frac{\rho}{\pi x}\left(\frac{r2 - r1}{r2 + r1}\right). \qquad (A4)$$

Where: ρ = Resistivity;

$$\rho = \frac{1}{\sigma};$$

σ = Conductivity.

Replacing the electrical terms with their thermal analogs we find:

$$\theta = \frac{1}{K\pi x}\left(\frac{r2 - r1}{r2 + r1}\right)$$

Note the inverse linear dependence of thermal resistance on the thickness of the conducting sheet.

This model demonstrates a major factor in designing heat sink structures for stud type power transistors. All other factors being equal, the thickness of the thermally conducting plate is of prime importance in the solution of heat flow problems.

BROADBAND LINEAR POWER AMPLIFIERS USING PUSH-PULL TRANSISTORS

Prepared by
Helge Granberg
RF Circuits Engineering

INTRODUCTION

Linear power amplifier operation, as used in SSB transmitters, places stringent distortion requirements on the high-power stages. To meet these distortion requirements and to attain higher power levels than can be generally achieved with a single transistor, a push-pull output configuration is often employed. Although parallel operation can often meet the power output demands, the push-pull mode offers improved even-harmonic suppression making it the better choice. The exact amount of even-harmonic suppression available with push-pull stages is highly dependent on several factors, the most significant one being the matching between the two output devices. Nevertheless, even in the worst case the suppression provided in push-pull designs is superior to that of single-ended circuits. Device matching however is not limited to push-pull circuits since it is also required to a lesser degree in parallel transistor designs.

Two linear power amplifier designs are to be discussed in this Application Note. The 80 Watt design is intended for mobile communications systems operating from a 12.5 V power sources. The other supplies 160 W when operated from a 28 V line and it is intended for fix location systems. Both designs cover the 3- 30 MHz band and utilize a driver stage to provide a total power gain of about 30 dB. Each amplifier requires some amount of heat-sinking for proper operation. The 28 V amplifier requires a heat-sink with a thermal characteristic of 0.85°C/W while the 12.5 V version uses a heat-sink with a 1.40°C/W thermal resistance. With these heat-sinks, cooling fans are not required for normal conditions, since with speech operation the average power is some 15 dB below peak levels. However, if two-tone bench testing is to exceed more than a duration of a few minutes, a cooling fan should be provided.

To assure ruggedness, engineering models of both amplifiers were subjected to open and short circuit output mismatches for several minutes at full power levels without any apparent damage to any of the transistors. This is very important in most equipment designs to avoid possible downtime for transistor replacements.

A 28 V, 160 W AMPLIFIER

An amplifier which can supply 160 watts (PEP) into a 50 Ω load with IMD performance of -30 dB or better is shown in the schematic diagram of Figure 1 and photos of Figures 2 and 3. Two 2N5942 transistors are employed in the design. These transistors are specified at 80 watts (PEP) output with intermodulation distortion products (IMD) rated at -30 dB. For broadband linear operation, a quiescent collector current of 60-80 mA for each transistor should be provided. Higher quiescent current levels will reduce fifth order IMD products, but will have little effect on third order products except at lower power levels. Generally, third order distortion is much more significant than the fifth order products.

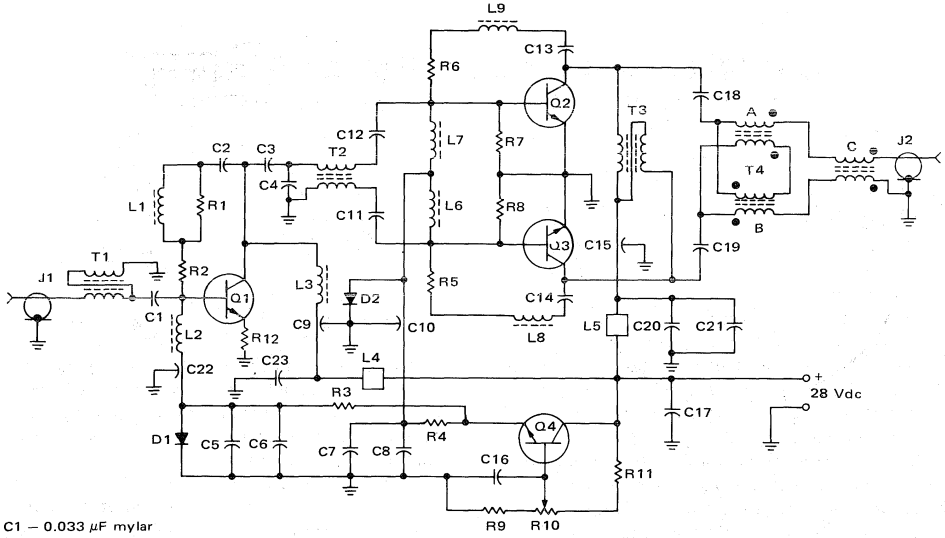
A biasing adjustment is provided in the amplifier circuit to compensate for variations in transistor current gain. This adjustment allows control of the idling current for both the output and driver devices. This control is also useful if the amplifier is operated from a supply other than 28 volts.

Even with the biasing control, it is strongly suggested that the output transistors be beta matched. As with any push-pull design, both dc current gain and power gain at a midband frequency should be matched within about 15-20%. This matching may require more stringent limits if broad-banding is necessary since broad-band operation requires more effective cancellation of even harmonics. In the engineering model used, the transistors were not perfectly matched. Four "similar" pairs were selected from a total of ten randomly chosen 2N5942 transistors. Table I shows the measured harmonic suppression which is degraded by the mismatch in the output transistor parameters. This data was taken with a single frequency test and 80 watts average output.

TABLE I – HARMONIC SUPPRESSION OF 28 V AMPLIFIER AT FULL OUTPUT POWER

Harmonic		2nd	3rd	4th	5th
Frequency	3 MHz	-16 dB	-30 dB	-22 dB	-37 dB
	6 MHz	-15 dB	-20 dB	-21 dB	-37 dB
	12 MHz	-16 dB	-24 dB	-22 dB	-34 dB
	30 MHz	-35 dB	-20 dB	-51 dB	-44 dB

A 2N6370 transistor is employed as a driver. This device is specified at -30 dB IMD when delivering 10 watts (PEP). However, at about 4.5 W (PEP) output, which is the maximum necessary to drive two 2N5942 transistors, the IMD is typically better than -40 dB with Class B biasing. A quiescent collector current level of at least 10-15 mA provides best IMD performance with the 2N6370. Higher current levels will not improve linearity, but will degrade driver efficiency.



C1 – 0.033 μF mylar
C2, C3 – 0.01 μF mylar
C4 – 620 pF dipped mica
C5, C7, C16 – 0.1 μF ceramic
C6 – 100 μF/15 V electrolytic
C8 – 500 μF/6 V electrolytic
C9, C10, C15, C22 – 1000 pF feed through
C11, C12 – 0.01 μF
C13, C14 – 0.015 μF mylar
C17 – 10 μF/35 V electrolytic
C18, C19, C21 – Two 0.068 μF mylars in parallel
C20 – 0.1 μF disc ceramic
C23 – 0.1 μF disc ceramic
R1 – 220 Ω, 1/4 W carbon
R2 – 47 Ω, 1/2 W carbon
R3 – 820 Ω, 1 W wire W
R4 – 35 Ω, 5 W wire W
R5, R6 – Two 150 Ω, 1/2 W carbon in parallel
R7, R8 – 10 Ω, 1/2 W carbon
R9, R11 – 1 k, 1/2 W carbon
R10 – 1 k, 1/2 W potentiometer
R12 – 0.85 Ω (6 5.1 Ω or 4 3.3 Ω 1/4 W resistors in parallel, divided equally between both emitter leads)

T1 – 4:1 Transformer, 6 turns, 2 twisted pairs of #26 AWG enameled wire (8 twists per inch)
T2 – 1:1 Balun, 6 turns, 2 twisted pairs of #24 AWG enameled wire (6 twists per inch)
T3 – Collector choke, 4 turns, 2 twisted pairs of #22 AWG enameled wire (6 twists per inch)
T4 – 1:4 Transformer Balun, A&B – 5 turns, 2 twisted pairs of #24, C – 8 turns, 1 twisted pair of #24 AWG enameled wire (All windings 6 twists per inch). (T4 – Indiana General F624-19Q1, – All others are Indiana General F627-8Q1 ferrite toroids or equivalent.)

PARTS LIST

L1 – .33 μH, molded choke
L2, L6, L7 – 10 μH, molded choke
L3 – 1.8 μH (Ohmite 2-144)
L4, L5 – 3 ferrite beads each
L8, L9 – .22 μH, molded choke

Q1 – 2N6370
Q2, Q3 – 2N5942
Q4 – 2N5190

D1 – 1N4001
D2 – 1N4997

J1, J2 – BNC connectors

FIGURE 1 – 160 Watt (PEP) Broadband Linear Amplifier

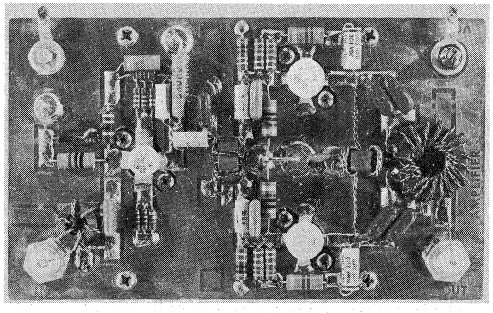


FIGURE 2 – Photo of 28 V Linear Amplifier

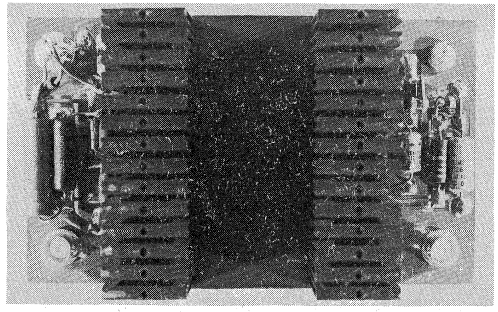


FIGURE 3 – Photo of Back Side of 28 V Linear Amplifier

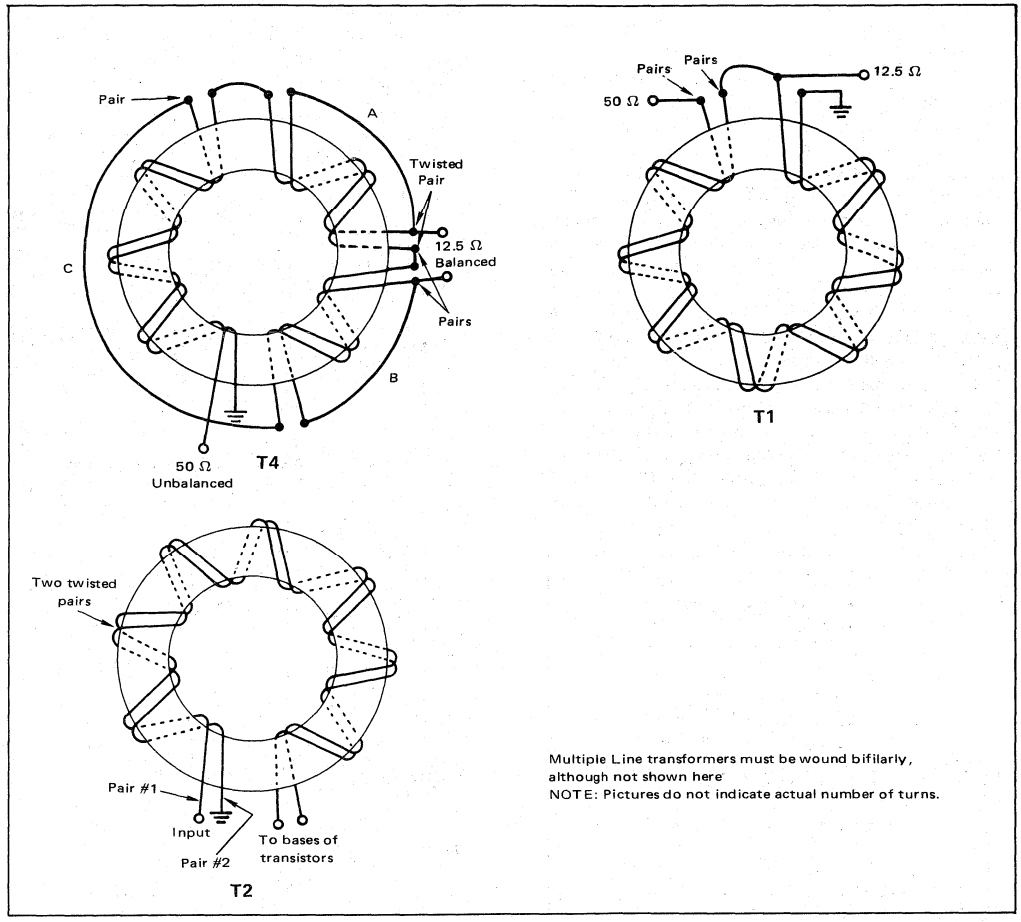


FIGURE 4 – Transformer Details for 28 V Linear Amplifier

Feedback

To compensate for variations in output with changes in operating frequency, negative voltage feedback is employed on both the final amplifier and driver stages. At the low end of the desired frequency band, approximately 4.5 dB of feedback is introduced in the final stage and 15 dB in the driver stage. With this feedback and the feedback networks shown in the schematic diagram, Figure 1, a total gain variation of 0.5 dB was measured on an engineering prototype amplifier over a 3-30 MHz range. The total gain differential in three identical amplifiers constructed for evaluation was less than 1.5 dB.

Transformers Employed

In order to achieve the desired broadband response, transmission line-type transformers were employed for coupling and signal-splitting. These transformers utilize twisted-pair windings and toroidal cores. Transformers T1, T2 and T3 have turn ratios of 4:1, 1:1 and 1:4 respectively. Additional information on these transformers can be found in the references. A short description of each of the transformers will follow.

Transformer T1 provides an impedance transformation to match the 50 Ω source to the low impedance level required at the base of Q1. This transformer consists of six turns of two twisted pairs wound on a toroidal core. The two pairs (four separate wires), are twisted together and the two wires from each original pair are soldered together at each end. Each pair thus connected is shown as a single wire in Figure 4. The pairs can easily be identified by choosing wires with two different colors of insulation.

Transformer T2 is a 1:1 Balun consisting of six turns of two-twisted pairs of wire (four wires total). As shown in Figure 4 each of the pairs is treated as a single wire.

Transformer T3 consists of four turns of two twisted pairs. Again both wires of each pair are soldered together at each end.

Transformer T4 is a 1:4 ratio unbalanced to balanced unit with three separate windings.

A lumped-constant equivalent conventional transformer diagram of transformer T4 is shown in Figure 5. The two windings in a single twisted pair are indicated by similar capital and lower case letters (i.e. windings A and a). The output line of the balun is in the same direction as windings A and B while the grounded line is in the opposite direction from the winding it is connected to. Windings A, a, B and b consist of 5 turns of two twisted pairs while C and c are formed from eight turns of a single pair. Connections are shown in Figure 4. The three windings are bifilar wound, although for simplicity the figures do not show this.

Referring to Figure 5 the equivalent connection diagram of T4, it can be seen that the sum of the voltages across c and C should be equal to the voltage across windings DE. From this, winding cC (a twisted pair) should have twice as many turns as twisted pairs aA and bB. Deviations of about 10-20% from the 2:1 ratio do not produce noticeable effects.

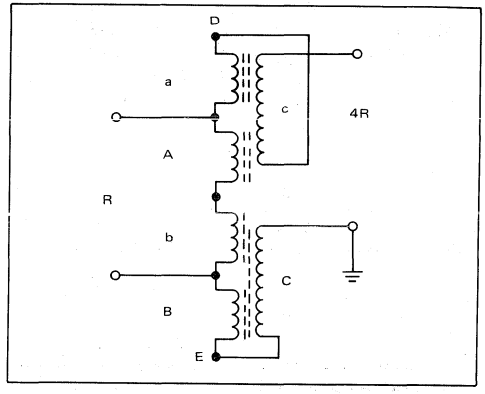


FIGURE 5 – Equivalent Lumped Element Form of T4.

The ferrite core used for T4 in the parts list of Figure 1 has a specified maximum flux density of about 100 gauss. The flux density may be computed from equation 1.

$$B_{max} = \frac{V \times 10^8}{4.44\, fnA} \quad \text{gauss} \qquad (1)$$

where:

V = RMS voltage across the winding = 89
f = frequency in Hertz = 3×10^6
n = number of turns (windings Aa and Bb only. Windings Cc cancel each other) = 20
A = cross sectional area of Toroid in Cm^2 = 0.25
$4.44 = 2\pi \times 0.707$

therefore:

$$B_{max} = \frac{89 \times 10^8}{4.44\,(3 \times 10^6)\,20\,(.25)} = 133 \text{ gauss}$$

Despite this slight overrating, this density is not excessive.

Amplifier Performance

The data shown in the following curves was obtained from measurement performed on an engineering model of the 28 V 160 Watt (PEP) amplifier.

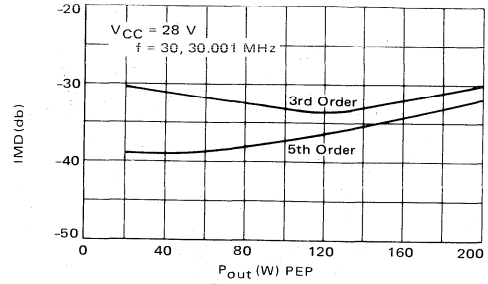


FIGURE 6 – IMD as a Function of Output Power for 28 V Amplifier

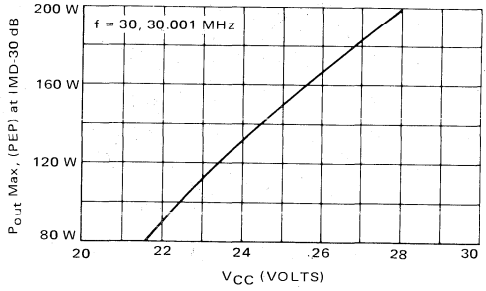


FIGURE 7 – Output Power for -30 dB IMD as a Function of V_{CC} for 28 V Amplifier

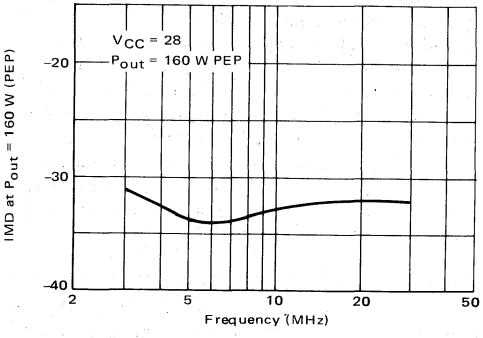


FIGURE 8 – IMD versus Frequency

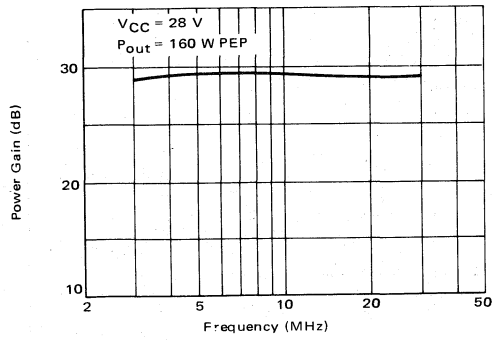


FIGURE 9 – Power Gain versus Frequency

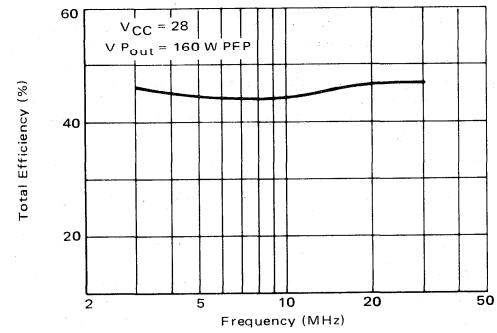


FIGURE 10 – Total Efficiency versus Frequency

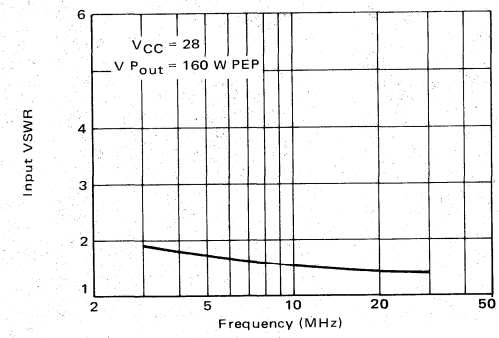


FIGURE 11 – VSWR versus Frequency

AN 80 WATT (PEP) 12.5 – 13.6 V AMPLIFIER

To complement the 28 Volt amplifier discussed previously, a second amplifier designed for 12 V operation was constructed and evaluated. This amplifier is shown in Figures 12, 13 and 14. It utilizes a 2N6367 and a pair of 2N6368 transistors. The 2N6367 transistor is employed as a driver and is specified for up to 9 watts (PEP) output. In the amplifier design the driver must supply only 5 watts (PEP) at 30 MHz with a resulting IMD performance of about -37 to -38 dB. At lower operating frequencies, drive requirements drop to the 2-3 Watt (PEP) range and IMD performance improves to better than 40 dB. The 2N6367 data sheet suggests a quiescent collector current of 35 mA, but it was found that increasing this to 40 mA yielded somewhat better linearity in broadband operation.

Two 2N6368 transistors are employed in the final stage of the transmitter design in a push-pull configuration. These devices are rated at 40 Watts (PEP) and -30 dB maximum IMD, although -35 dB performance is more typical for narrow band operation.

The 2N6368 data sheet suggests a quiescent collector current level of 50 mA, but a level of 60 mA for each transistor was used in this design for improved linearity.

Without frequency compensation, the completed amplifier can deliver 90 Watts (PEP) in the 25-30 MHz band with IMD performance down -30 dB. If only the power amplifier stage is frequency compensated, 95 Watts (PEP) can be obtained at 6-10 MHz.

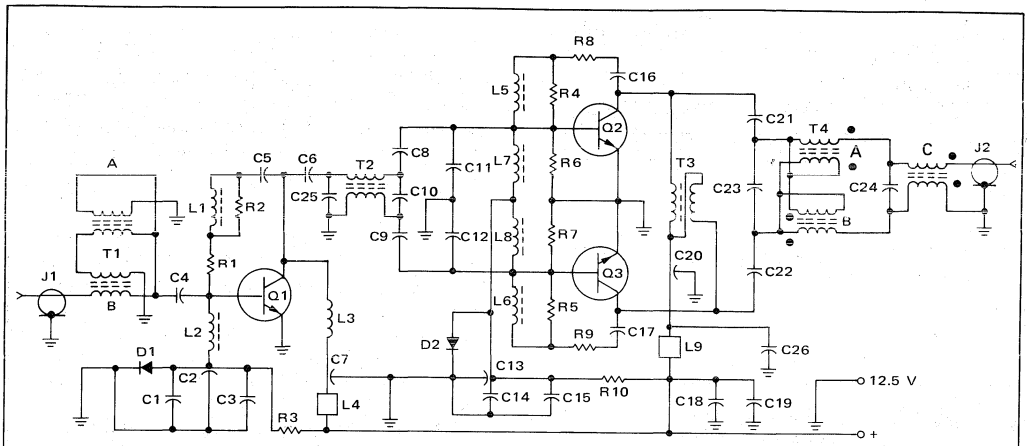
Gain Compensation

Negative collector-to-base feedback is employed in both the driver and output stages for gain compensation. The feedback networks consist of: a) a dc blocking capacitor, b) a series resistor, to limit the amount of feedback at the low frequencies and c) a series inductor with a parallel resistor to determine the feedback slope.

In general, the use of negative feedback lowers the input impedance, and reduces the gain of the amplifier. However, it also improves the linearity since some of the output signal is fed back to the input and reamplified, tending to cancel the distortion originally generated. This is only true at the low frequencies where the phase errors are small. The phase error is caused by reactive elements in the feedback path. Since the basis for the compensation is to introduce more feedback at low frequencies, it will also equalize the input impedance to some degree. This, in turn, should result in a lower VSWR over the band.

The following two tables illustrate the affect of compensation on the final amplifier stage. This data was taken with a 9:1 ratio transformer connected between 50 Ω source and the input balun to the final stage.

From this table it can be seen that efficiency is reduced by applying compensation. For this reason only 3 dB of compensation was utilized on the final stage. The driver stage, where efficiency is not of primary concern, was actually over compensated. This stage has a gain of 16 dB at 30 MHz but only 13 dB at 3 MHz.



C1, C14, C18 — 0.1 μF ceramic.
C2, C7, C13, C20 — 0.001 μF feed through.
C3 — 100 μF/3V.
C4, C6 — 0.033 μF mylar
C5 — 0.0047 μF mylar.
C8, C9 — 0.015 and 0.033 μF mylars in parallel.
C10 — 470 pF mica.
C11, C12 — 560 pF mica.
C15 — 1000 μF/3 V
C16, C17 — 0.015 μF mylar
C19 — 10 pF 15 V
C21, C22 — two 0.068 μF mylars in parallel.
C23 — 330 pF mica
C24 — 39 pF mica
C25 — 680 pF mica
C26 — .01 μF ceramic

R1, R6, R7 — 10 Ω, 1/2 W carbon.
R2 — 51 Ω, 1/2 W carbon
R3 — 240 Ω, 1 wire W
R4, R5 — 18 Ω, 1 W carbon
R8, R9 — 27 Ω, 2 W carbon
R10 — 33 Ω, 6 W wire W

L1 — 0.22 μh molded choke
L2, L7, L8 — 10 μh molded choke
L5, L6 — 0.15 μh
L3 — 25 t, #26 wire, wound on a 100 Ω, 2 W resistor. (1.0 μh)
L4, L9 — 3 ferrite beads each.

T1 — 2 twisted pairs of #26 wire, 8 twists per inch. A = 4 turns, B = 8 turns. Core - -Stackpole 57-9322-11, Indiana General F627-8Q1 or equivalent
T2 — 2 twisted pairs of #24 wire, 8 twists per inch, 6 turns. (Core as above.)
T3 — 2 twisted pairs of #20 wire, 6 twists per inch, 4 turns. (Core as above.)
T4 — A and B = 2 twisted pairs of #24 wire, 8 twists per inch. 5 turns each. C = 1 twisted pair of #24 wire, 8 turns. Core - -Stackpole 57-9074-11, Indiana General F624-19Q1 or equivalent.

Q1 — 2N6367
Q2, Q3 — 2N6368

D1 — 1N4001
D2 — 1N4997

J1, J2 — BNC connectors

FIGURE 12 — Schematic Diagram of 12.5 V Amplifier

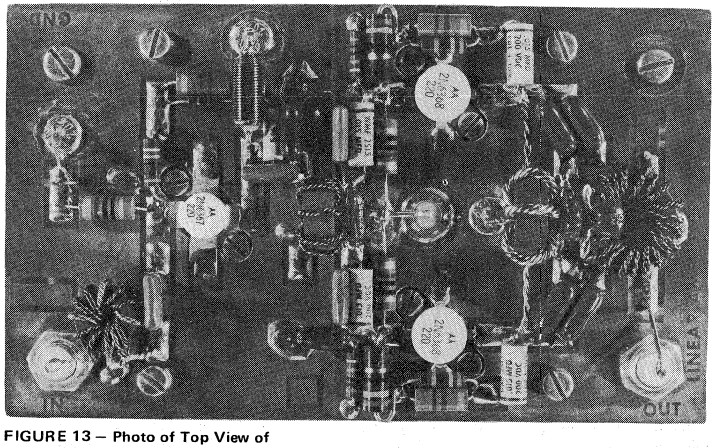


FIGURE 13 — Photo of Top View of 12.5 V Linear Amplifier

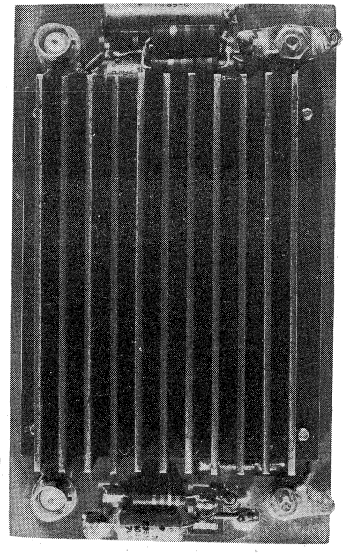


FIGURE 14 — Photo of Bottom of 12.5 V Linear Amplifier

6

TABLE II – PERFORMANCE OF 12.5 V OUTPUT STAGE WITH AND WITHOUT GAIN COMPENSATION

With Feedback	GPE	EFF.	IMD	VSWR
3 MHz	16 dB	45.5%	-30 dB	1.6
12 MHz	15.3 dB	46.5%	-31 dB	2.1
30 MHz	12 dB	43.0%	-31 dB	1.05

Without Feedback	GPE	EFF.	IMD	VSWR
3 MHz	19.2 dB	48.0%	-26 dB	6.5
12 MHz	16.2 dB	46.8%	-30 dB	2.4
30 MHz	12.5 dB	43.0%	-33 dB	1.05

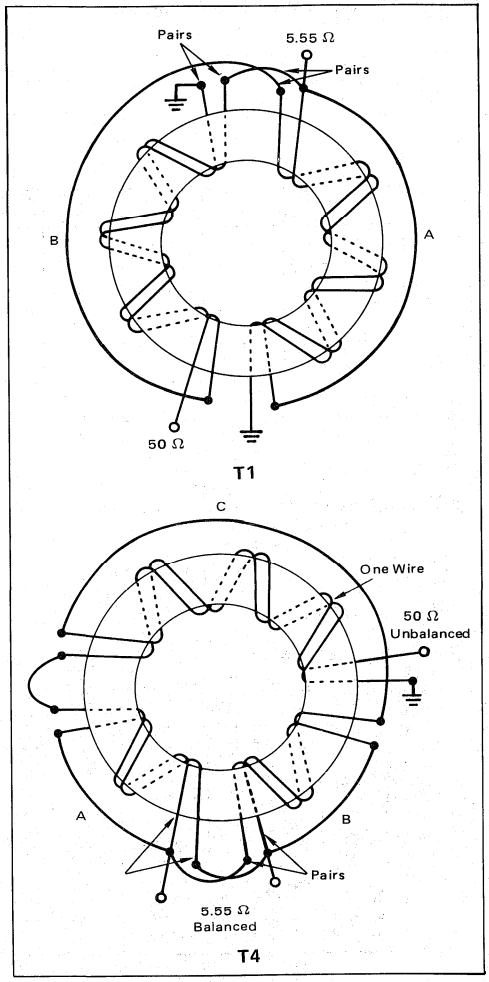


FIGURE 15 – Transformer Details for 12.5 V Linear Amplifier (See Figure 4)

Transformer T1 consists of two twisted pairs of wires which can be wound on either a single or two separate toroids. In the two core approach, both windings have an equal number of turns (four). If a single core is utilized, winding Aa uses four turns while winding Bb uses eight turns. These lines must be wound bifilar on the core. See Figure 15. The single core approach was used in the engineering model.

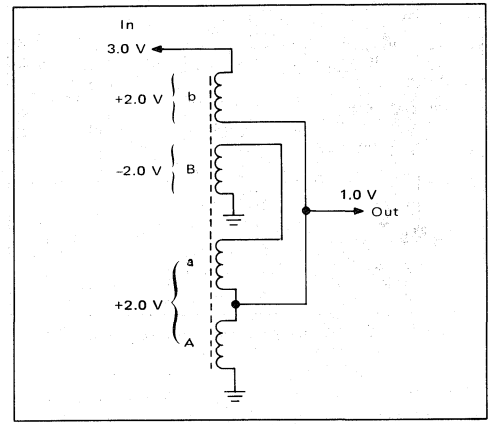


FIGURE 16 – Equivalent Lumped Element Form of T1

A lumped-constant equivalent conventional transformer diagram of transformer T1 is shown in Figure 16. Examination reveals that since winding B is directly in parallel with the series combination of aA, line Bb must have twice the number of turns as winding Aa. (The lower case and capital letters refer to the two wires in a given twisted-pair). As an example of the voltage relationships for the various windings in this transformer, an arbitrary 3 V input has been shown in the Figure. It can be seen that the voltages generated across windings b and B are out of phase and cancel each other. Therefore, the resulting output is 1 V (3 V-2 V).

This transformer may be considered as a combination of a 4:1 ratio transformer (aA) and a 1:1 balun (bB), where the balun performs the voltage subtraction.

Transformer T2 consists of two twisted pairs on a single core. Both wires of each pair are soldered together at each end. See Figure 15.

Transformer T3 also uses two twisted pairs wound on a single core. Each pair is treated as a single wire by soldering the two wires at each end.

Transformer T4 uses three separate bifilar windings on a single core. Windings aA and bB are balanced while Cc is unbalanced. Both aA and bB utilize five turns and Cc uses eight turns. This is the nearest whole number of turns possible to the desired ratio of 1:1.5 for winding Aa and

Bb to winding cC. Deviations of 10-20% of this ratio are allowable without noticeable effects.

Figure 17 shows the lumped equivalent transformer of

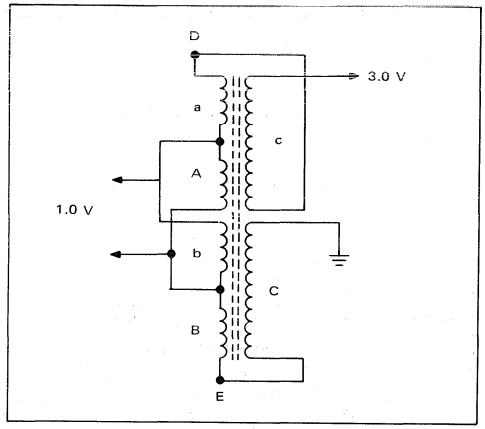


FIGURE 17 – Equivalent Lumped Element Form of T4

T4 and the ratio of voltages on the various windings if one volt is applied to the input. It can be seen that the voltage developed across c and C must equal the voltage between points D and E on the diagram. Since windings A and b are paralleled and connected to the input, they see one volt. Thus the voltage from point D to point E would be 3 V (1 V from A and b plus 1 V from winding a plus 1 V from winding B). Therefore, the output voltage is 3.0 volts and the voltage across winding c = -1.5 V and winding C = 1.5 V.

When using twisted-pair transmission line transformers, windings with four or more pairs should be avoided as it is difficult to twist such lines uniformly.

A second amplifier was evaluated with T4 replaced by a balun and an unsymmetrical 1:9 ratio transformer. Performance results were very similar to that obtained from the first version except that much more high frequency compensation was necessary. This was required because it is difficult to obtain the low characteristic impedance required for the balun. For this reason capacitors C10, C11, C12 and C25 were unusually large in value.

Performance

Typical performance of the 12.5 volt linear amplifiers is provided in the following curves. A calibration curve for use to correlate low frequency readings on a power meter is also given in Figure 24.

The harmonic suppression measurements taken at full output power levels with a single tone test are illustrated in Table II. This data suggests that a suitable low-pass filter between the amplifier output and the antenna will be required to meet harmonic suppression requirements. This filter's necessity is common to most broadband amplifier designs.

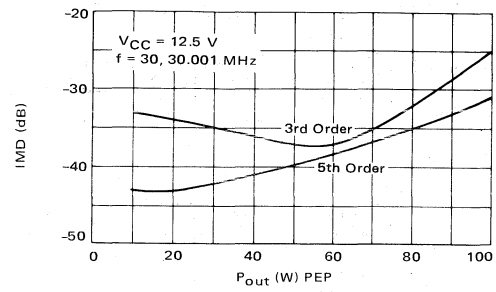


FIGURE 18 – IMD as a Function of Output Power For Push-Pull Linear Amplifier

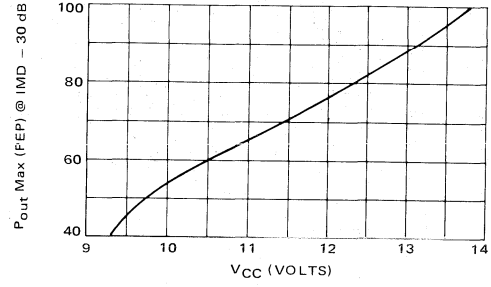


FIGURE 19 – Maximum Output Power @ -30 dB IMD versus V_{CC} for 12.5 V Power Amplifier

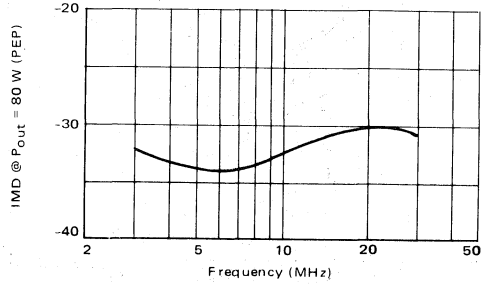


FIGURE 20 – IMD versus Frequency

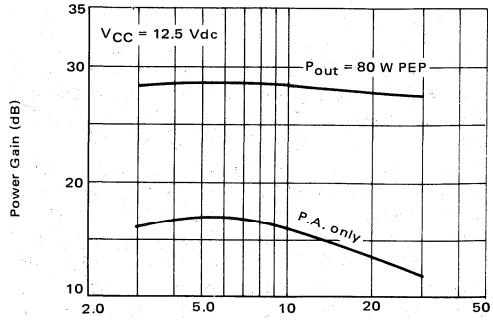


FIGURE 21 – Power Gain versus Frequency

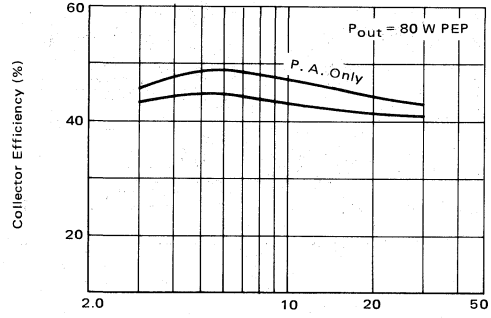


FIGURE 22 – Efficiency versus Frequency

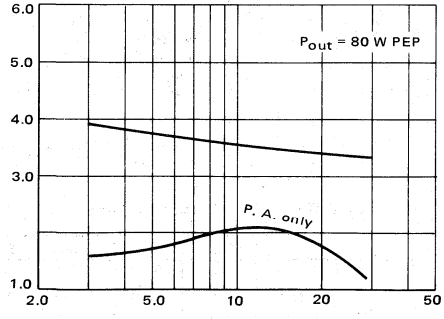


FIGURE 23 – VSWR versus Frequency

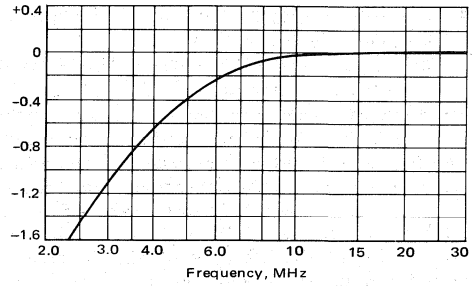


FIGURE 24 – Response of H.P. 431-432 Power Meters at Low Frequencies

Transformer Data

As with the 28 V amplifier, transmission line type transformers are employed throughout the 12 V design. Although this type of transformer does not provide optimum impedance match, it is easy to duplicate for consistant performance results. A similar amplifier was constructed with a standard 2:1 ratio coupling transformer instead of the 1:1 ratio balun (T2). This amplifier featured a 40-60% improvement in VSWR at all frequencies while gain and IMD were basically unchanged from the performance of the model using transmission line type transformers.

Splitting the compensating capacitor for transformer T2 into three parts (C10, C11 and C12) will result in considerably lower IMD at higher frequencies. Capacitors C11 and C12 should be well matched and therefore should be either ±5% or better tolerance fixed value units, or variable capacitors such as Arco 466 and 469.

Two factors must be considered in the choice of toroidal core materials. The first is core losses. The second is the power handling capability which is limited by both magnetic saturation and heat generation.

For the input transformer (T1) core losses are of primary concern. For the material chosen in this design, a loss factor of 1-2 mW/cm^3 at 3 MHz is typical. This increases to 5-10 mW/cm^3 at 30 MHz. For the size of core used in T1, a maximum core loss of 1.5-7.0 mW can be expected. While this figure seems negligible, it is advantageous to use the smallest practical sized core for the input transformer consistent with the wire size and required number of turns.

Conversely the core of the output transformer (T4) should be as large as possible to be able to handle the required power levels and remain in the linear operating region of the materials' B-H curve. If the core is operated near the saturation region of the core material, distortion will be generated on the carrier and envelope. This saturation occurs first at low frequencies. However, core heating due to losses is most prevalent at higher frequencies, being a function of flux density and operating frequency. The maximum recommended flux density for a 1/2" O.D. toroid (such as Indiana General F627-8 or Stackpole 57-9322),

is 45 to 70 gauss. From the B-H curves it can be seen that this is well into the linear region.

For the 12-volt amplifier, a flux density of roughly 180 gauss would be required for a 1/2" O.D. core. Use of a larger core reduces the density to about 130 gauss. As stated in the 28 V amplifier section, although this is in excess of the 100 gauss limit suggested for the particular core type, it was not found to be excessive. In fact, some of the 1/2" O.D. toroids were tested at three to four times the maximum recommended flux density, and then compared to a larger toroid of the same material. The distortion in each core was small enough not to be noticed in an oscilloscope. However, there was some amount of heat generated in the small toroid at the high frequencies. Excessive heating is the primary problem that one should be first concerned about.

As a rule of thumb, the required minimum transformer inductance can be determined to have at least 4-5 times the reactance of the high impedance port at the lowest operating frequency. This means that for T4, the reactance would be 250 ohms, which corresponds to roughly 14 μH at 3 MHz

Employing a different wire size or wire with a different thickness of dielectric or changing the number of twists per inch will alter the line impedance. However, this is one of the least critical points in the design of broadband linear amplifiers and will mainly affect the amount of high frequency compensation required. The variations in the transistor input and output impedance over a decade frequency range are several times larger than the changes in transformer impedance due to wire sizes or twist variations. Although compromises in matching are necessary to tune the wide frequency range, they are most serious in the output stage where a mismatch can significantly degrade total linearity.

The maximum theoretical linear output powers for the 28 V and 12.5 V amplifiers would be 120 W and 50 W respectively, when 4:1 and 9:1 output transformers are employed.

However, due to stray inductances in the circuit, and line impedances usually being higher than optimum, the actual impedance ratios of the transformers will be somewhat higher.

Thus, if the phase and even harmonic distortions are minimized it is possible to obtain higher power levels with fairly low IMD readings despite slight flat-topping of the envelope.

Construction Notes (12.5 V version)

The circuit board for both amplifier designs is made of two-sided copper-fiberglass laminate. A full sized pattern is given in Figures 25 and 26. The ground planes on each side are connected together at several points with the feed-through capacitors, the BNC connectors and the mounting screws. From experience with an earlier broadband amplifier, it was learned that a good ground plane is extremely important because of the high currents and low impedance levels involved. The power supply impedance must be as low as possible.

The ac impedance of the supply should not be higher than 0.01 ohm at the lowest envelope frequency.

All dc connections are made on the back side of the board which is separated from the heat sink by 3/32 inches. The base bias resistors (R3, R10), and all by-pass capacitors, except the feed-throughs, are on the back side of the board in each end of the heat sink. Diode D2 is press fitted into the heat sink for temperature compensation of the quiescent collector currents of the 2N6368 transistors. Ceramic capacitors have been avoided, except for certain by-pass applications, because they have spurious resonances and, their capacitance values are voltage and temperature sensitive. Parallel capacitors are employed to increase the current carrying capability and to decrease the possibility of self resonances. The peak RF current in

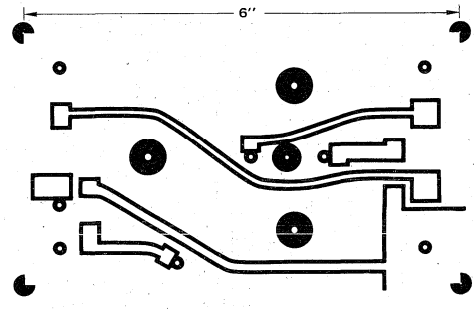


FIGURE 25 – Bottom PC Board Pattern

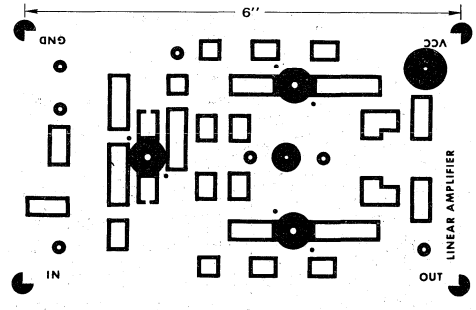


FIGURE 26 – Top Side of PC Board

TABLE III – HARMONIC SUPPRESSION versus FREQUENCY

Harmonic		2nd	3rd	4th	5th
Frequency	3 MHz	-19 dB	-15 dB	-26 dB	-29 dB
	6 MHz	-17 dB	-18 dB	-23 dB	-35 dB
	12 MHz	-30 dB	-20 dB	-28 dB	-34 dB
	30 MHz	-35 dB	-25 dB	-50 dB	-62 dB

the output transformer primary is $\sqrt{\frac{80\ W}{6.25\ \Omega}}$ = 3.54A. Half of this is supplied by each 2N6368. Thus, the collector isolation capacitors will have to handle 1.77A peak and 1.26A average currents. Even the lead sizes in most capacitors are insufficient for these current levels. In general, the low impedances involved in a 12.5 volt amplifier of this power level make the layout, construction and component selection somewhat critical compared to a higher voltage unit.

CONSTRUCTION NOTES (28 V version)

The 28 volt unit is less critical than the 12.5 V amplifier as far as the physical circuit lay-out is concerned. However, the same precautions should be taken in grounding the by-pass capacitors and the transformer high frequency-compensation capacitors. It is recommended that variable capacitors, such as the ARCO 460 line be used initially for the compensating capacitors. Then after establishing satisfactory operation of the unit, they can be changed to fixed value capacitors.

IMPROVED PERFORMANCE

Since the original work on these amplifiers, device improvements have been made. Both IMD and load mismatch ruggedness characteristics can be enhanced by substituting the MRF463 or MRF464 for the 2N5942 in the 28-Volt amplifier. The MRF460 is recommended for upgrading the 12-Volt amplifier using the 2N6368. Neither of these new devices require circuit modifications for optimum operation.

REFERENCES

1. Ruthroff: Some Broad Band Transformers, *IRE, Volume 47,* August, 1957.
2. Hilbers: Design of H. F. Wideband Power Transformers, *Philips Application Information #530.*
3. Pitzalis-Couse: Broadband Transformer Design for RF Transistor Amplifiers, *ECOM-2989,* July 1968.
4. Pappenfus; Bruene, Schoenike: Single Sideband Principles and Circuits, McGraw-Hill.
5. Granberg, H.; *Broadband Transformers and Power Combining Techniques for RF,* AN-749 Motorola Semiconductor Products Inc., June 1975.
6. Granberg, H.; *Get 300 Watts PEP Linear Across 2 to 30 MHz From This Push-Pull Amplifier,* EB-27 Motorola Semiconductor Products Inc., September 1974.
7. Granberg, H.; *A Complementary Symmetry Amplifier for 2 to 30 MHz SSB Driver Applications,* EB-32 Motorola Semiconductor Products Inc., February 1975.
8. Granberg, H.; *Measuring the Intermodulation Distortion of Linear Amplifiers,* EB-38 Motorola Semiconductor Products Inc., January 1975.

IMPEDANCE MATCHING NETWORKS APPLIED TO RF POWER TRANSISTORS

Prepared by:
B. Becciolini

1. INTRODUCTION

Some graphic and numerical methods of impedance matching will be reviewed here. The examples given will refer to high frequency power amplifiers.

Although matching networks normally take the form of filters and therefore are also useful to provide frequency discrimination, this aspect will only be considered as a corollary of the matching circuit.

Matching is necessary for the best possible energy transfer from stage to stage. In RF-power transistors the input impedance is of low value, decreasing as the power increases, or as the chip size becomes larger. This impedance must be matched either to a generator — of generally 50 ohms internal impedance — or to a preceding stage. Impedance transformation ratios of 10 or even 20 are not rare. Interstage matching has to be made between two complex impedances, which makes the design still more difficult, especially if matching must be accomplished over a wide frequency band.

2. DEVICE PARAMETERS

2.1 INPUT IMPEDANCE

The general shape of the input impedance of RF-power transistors is as shown in Figure 1. It is a large signal parameter, expressed here by the parallel combination of a resistance R_p and a reactance X_p (Ref. (1)).

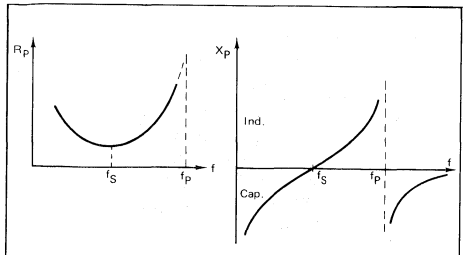


Fig. 1 — Input impedance of RF-power transistors as a function of frequency

The equivalent circuit shown in Figure 2 accounts for the behaviour illustrated in Figure 1.

With the presently used stripline or flange packaging, most of the power devices for VHF low band will have their R_p and X_p values below the series resonant point fs. The input impedance will be essentially capacitive.

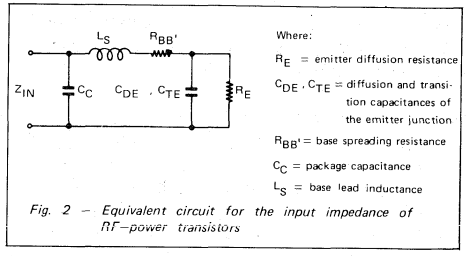


Fig. 2 — Equivalent circuit for the input impedance of RF-power transistors

Most of the VHF high band transistors will have the series resonant frequency within their operating range, i.e. be purely resistive at one single frequency f_s, while the parallel resonant frequency f_p will be outside.

Parameters for one or two gigahertz transistors will be beyond f_s and approach f_p. They show a high value of R_p and X_p with inductive character.

A parameter that is very often used to judge on the broadband capabilities of a device is the input Q or Q_{IN}, defined simply as the ratio R_p/X_p. Practically Q_{IN} ranges around 1 or less for VHF devices and around 5 or more for microwave transistors.

Q_{IN} is an important parameter to consider for broadband matching. Matching networks normally are low-pass or pseudo low-pass filters. If Q_{IN} is high, it can be necessary to use band-pass filter type matching networks and to allow insertion losses. But broadband matching is still possible. This will be discussed later.

2.2. OUTPUT IMPEDANCE

The output impedance of the RF-power transistors, as given by all manufacturers' data sheets, generally consists of only a capacitance C_{OUT}. The internal resistance of the transistor is supposed to be much higher than the load and is normally neglected. In the case of a relatively low internal resistance, the efficiency of the device would decrease by the factor:

$$1 + {}^{R}L/R_T$$

where R_L is the load resistance, seen at the collector-emitter terminals, and R_T the internal transistor resistance equal to:

$$\frac{1}{\omega_T \cdot (C_{TC} + C_{DC})},$$

defined as a small signal parameter, where:

ω_T = transit angular frequency

$C_{TC} + C_{DC}$ = transition and diffusion capacitances at the collector junction

The output capacitance C_{OUT}, which is a large signal parameter, is related to the small signal parameter C_{CB}, the collector-base transistion capacitance.

Since a junction capacitance varies with the applied voltage, C_{OUT} differs from C_{CB} in that it has to be averaged over the total voltage swing. For an abrupt junction and assuming certain simplifications, $C_{OUT} = 2\ C_{CB}$.

Figure 3 shows the variation of C_{OUT} with frequency. C_{OUT} decreases partly due to the presence of the collector lead inductance, but mainly because of the fact that the base-emitter diode does not shut off anymore when the operating frequency approaches the transit frequency f_T.

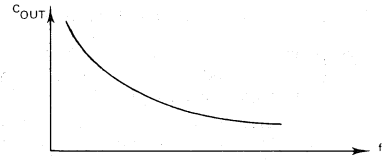


Fig. 3 – Output capacitance C_{OUT} as a function of frequency

3. OUTPUT LOAD

In the absence of a more precise indication, the output load R_L is taken equal to:

$$R_L = \frac{[V_{CC} - V_{CE\ (sat)}]^2}{2\,P_{OUT}}$$

with $V_{CE\ (sat)}$ equal to 2 or 3 volts, increasing with frequency.

The above equation just expresses a well-known relation, but also shows that the load, in first approximation, is not related to the device, except for $V_{CE\ (sat)}$. The load value is primarily dictated by the required output power and the peak voltage; it is not matched to the output impedance of the device.

At higher frequencies this approximation becomes less exact and for microwave devices the load that must be presented to the device is indicated on the data sheet. This parameter will be measured on all Motorola RF-power devices in the future.

Strictly speaking, impedance matching is accomplished only at the input. Interstage and load matching are more impedance transformations of the device input impedance and of the load into a value R_L (sometimes with additional reactive component) that depends essentially on the power demanded and the supply voltage.

4. MATCHING NETWORKS

In the following, matching networks will be described by order of complexity. These are ladder type reactance networks.

The different reactance values will be calculated and determined graphically. Increasing the number of reactances broadens the bandwidth. However, networks consisting of more than four reactances are rare. Above four reactances, the improvement is small.

4.1 NUMERICAL DESIGN

4.1.1 Two-Resistance Networks

Resistance terminations will first be considered. Figure 4 shows the reactive L-section and the terminations to be matched.

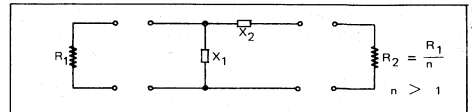


Fig. 4 – Two-Reactance Matching Network

Matching or exact transformation from R_2 into R_1 occurs at a single frequency f_o.

At f_o, X_1 and X_2 are equal to:

$$X_1 = \pm R_1 \sqrt{\frac{R_2}{R_1 - R_2}} = R_1 \frac{1}{\sqrt{n-1}}$$

$$X_2 = \mp \sqrt{R_2 (R_1 - R_2)} = R_1 \frac{\sqrt{n-1}}{n}$$

At f_o: $X_1 \cdot X_2 = R_1 \cdot R_2$

X_1 and X_2 must be of opposite sign. The shunt reactance is in parallel with the larger resistance.

The frequency response of the L-section is shown in Figure 5, where the normalized current is plotted as a function of the normalized frequency.

If X_1 is capacitive and consequently X_2 inductive, then:

$$X_1 = -\frac{fo}{f} R_1 \sqrt{\frac{R_2}{R_1 - R_2}} = -\frac{fo}{f} R_1 \frac{1}{\sqrt{n-1}}$$

and $$X_2 = \frac{f}{fo} \sqrt{R_2 (R_1 - R_2)} = \frac{f}{fo} R_1 \frac{\sqrt{n-1}}{n}$$

6

The normalized current absolute value is equal to:

$$\left|\frac{I_2}{I_0}\right| = \frac{2\sqrt{n}}{\sqrt{(n-1)^2 \cdot (\frac{f}{f_o})^4 - 2(\frac{f}{f_o})^2 + (n+1)^2}}$$

where $I_o = \frac{\sqrt{n}\,E}{2.R_1}$, and is plotted in Figure 5 (Ref. (2)).

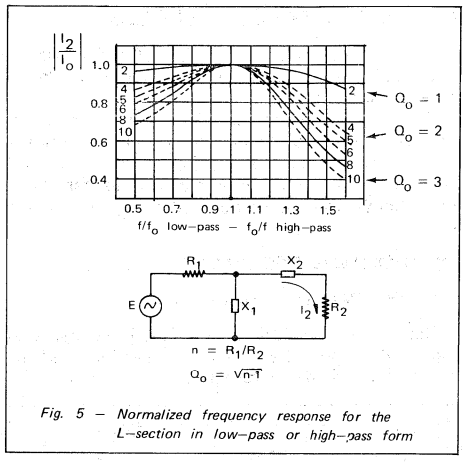


Fig. 5 – Normalized frequency response for the L-section in low-pass or high-pass form

If X_1 is inductive and consequently X_2 capacitive, the only change required is a repacement of f by f_o and vice-versa. The L-section has low pass form in the first case and high-pass form in the second case.

The Q of the circuit at f_o is equal to:

$$Q_o = \frac{X_2}{R_2} = \frac{R_1}{X_1} = \sqrt{n-1}$$

For a given transformation ratio n, there is only one possible value of Q. On the other hand, there are two symmetrical solutions for the network, that can be either a low-pass filter or a high-pass filter.

The frequency f_o does not need to be the center frequency, $\frac{f_1 + f_2}{2}$, of the desired band limited by f_1 and f_2.

In fact, as can be seen from the low-pass configuration of Figure 5, it may be interesting to shift fo toward the high band edge frequency f_2 to obtain a larger bandwidth w, where $w = \frac{2(f_1 + f_2)}{f_2 - f_1}$

This will, however, be at the expense of poorer harmonic rejection.

Example:

For a transformation ratio n = 4, it can be determined from the above relations:

Bandwidth w	0.1	0.3
Max insertion losses	0.025	0.2
X_1/R_1	1.730	1.712

If the terminations R_1 and R_2 have a reactive component X, the latter may be taken as part of the external reactance as shown in Figure 6.

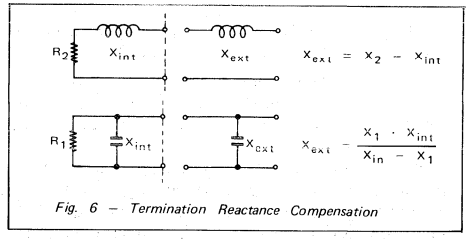


Fig. 6 – Termination Reactance Compensation

This compensation is applicable as long as

$$Q_{INT} = \frac{X_{INT}}{R_2} \text{ or } \frac{R_1}{X_{INT}} < n-1$$

Tables giving reactance values can be found in Ref. (3) and (4).

4.1.1.1 Use of transmission lines and inductors

In the preceding section, the inductance was expected to be realized by a lumped element. A transmission line can be used instead (Fig 7).

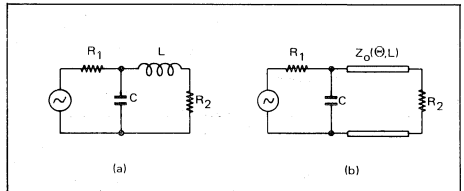


Fig. 7 – Use of a transmission line in the L-section

As can be seen from the computed selectivity curves (Fig. 8) for the two configurations, transmission lines result in a larger bandwidth. The gain is important for a transmission line having a length $L = \lambda/4$ ($\Theta = 90°$) and a characteristic impedance $Z_o = \sqrt{R_1 \cdot R_2}$. It is not significant for lines short with respect to $\lambda/4$. One will notice that there is an infinity of solutions, one for each value of C, when using transmission lines.

4.1.2 Three-reactance matching networks

The networks which will be investigated are shown in Figure 9. They are made of three reactances alternatively connected in series and shunt.

A three-reactances configuration allows to make the quality factor Q of the circuit and the transformation ratio $n = \frac{R_2}{R_1}$ independent of each other and consequently to choose the selectivity between certain limits.

For narrow band designs, one can use the following formulas (Ref. (5) AN-267, where tables are given):

Network (a):

$X_{C1} = R_1/Q$ Q must be first selected

$$X_{C2} = R_2 \sqrt{\frac{R_1 R_2}{(Q^2+1) - \frac{R_1}{R_2}}}$$

$$X_L = \frac{QR_1 + (R_1 R_2/X_{C2})}{Q^2 + 1}$$

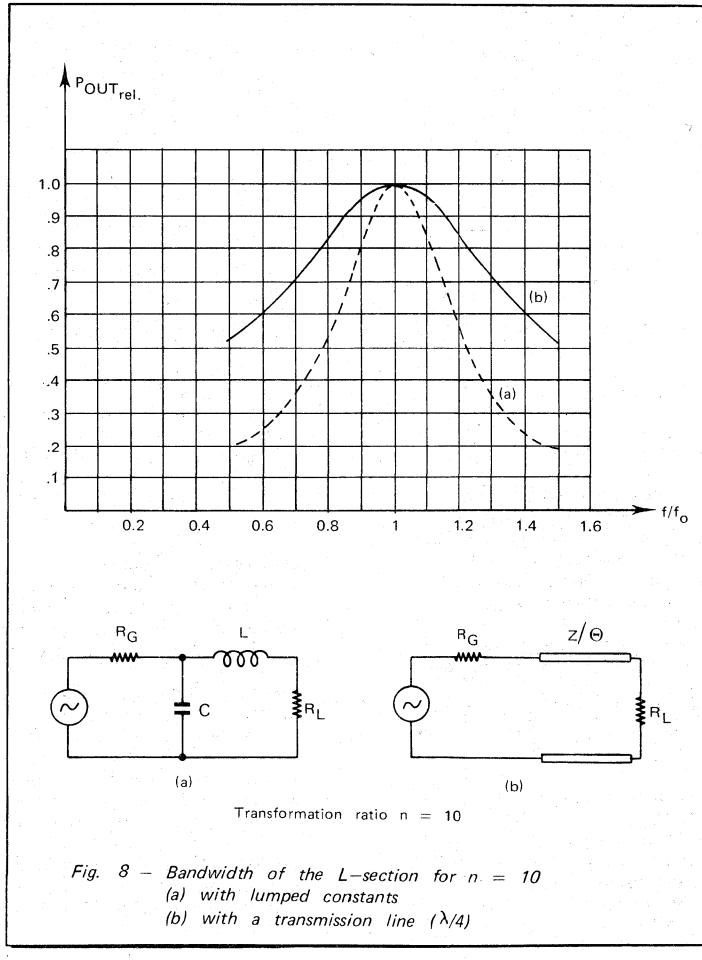


Fig. 8 – Bandwidth of the L–section for n = 10
(a) with lumped constants
(b) with a transmission line (λ/4)

6

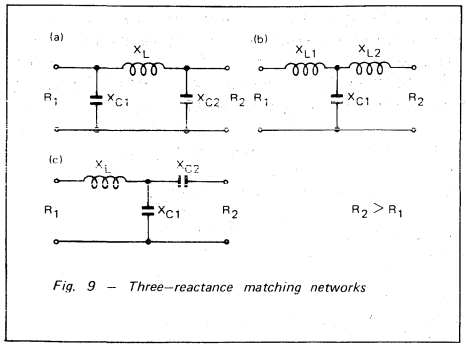


Fig. 9 – Three–reactance matching networks

Network (b) : Q must first be selected

$$X_{L1} = R_1 Q \qquad A = R_1 (1 + Q^2)$$

$$X_{L2} = R_2 . B \qquad B = \sqrt{\frac{A}{R_2} - 1}$$

$$X_{C1} = \frac{A}{Q + B}$$

Network (c) : Q must first be selected

$$X_{L1} = Q . R_1 \qquad A = \sqrt{\frac{R_1 (1+Q^2)}{R_2} - 1}$$

$$X_{C2} = A . R_2$$

$$X_{C1} = \frac{B}{Q - A} \qquad B = R_1 . (1 + Q^2)$$

The network which yields the most practical component values, should be selected for a given application.

The three-reactance networks can be thought of as being formed of a L-section (two reactances) and of a compensation reactance. The L-section essentially performs the impedance transformation, while the additional reactance compensates for the reactive part of the transformed impedance over a certain frequency band.

Figure 10 shows a representation in the Z-plane of the circuit of Figure 9 (a) split into two parts R_1-C_1-L_1 and C_2-R_2.

Exact transformation from R_1 into R_2 occurs at the points of intersection M and N. Impedances are then conjugate or $Z' = R' + jX'$ and $Z'' = R'' + jX''$ with $R' = R''$ and $X' = -X''$.

The only possible solution is obtained when X' and -X'' are tangential to each other. For the dashed curve, representing another value of L_1 or C_1, a wider frequency band could be expected at the expense of some ripple inside the band. However, this can only be reached with four reactances as will be shown in section 4.1.3.

With a three-reactance configuration, there are not enough degrees of freedom to permit $X' = -X''$ and simultaneously obtain the same variation of frequency on both curves from M' to point N'.

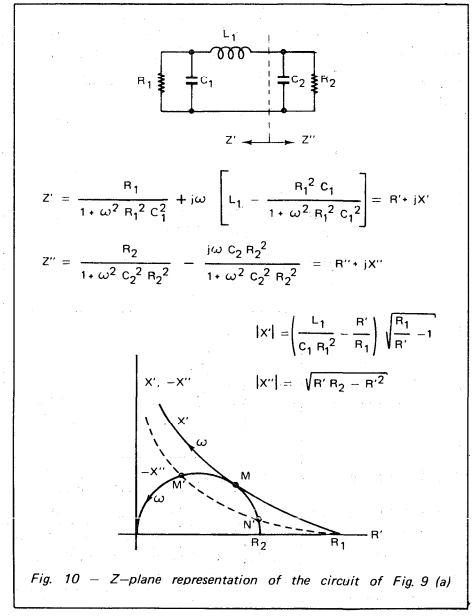


Fig. 10 – Z–plane representation of the circuit of Fig. 9 (a)

Exact transformation can, therefore, only be obtained at one frequency.

The values of the three reactances can be calculated by making $X' = -X''$, $R' = R''$ and $\frac{dX'}{dR'} = -\frac{dX''}{dR''}$.

The general solution of these equations leads to complicated calculations. Therefore, computed tables should be used.

One will note on Figure 10 that the compensation reactance contributes somewhat to impedance transformation, i.e. R' varies when going from M to R_2.

The circuit of Figure 9 (b) is dual with respect to the first one and gives exactly the same results in a Y-plane representation.

Circuit of Figure 9 (c) is somewhat different since only one intersection M exists as shown in Figure 11. Narrower frequency bands must be expected from this configuration. The widest band is obtained for $C_1 = \infty$.

Again, if one of the terminations has a reactive component, the latter can be taken as a part of the matching network, provided it is not too large (see Fig. 6).

6

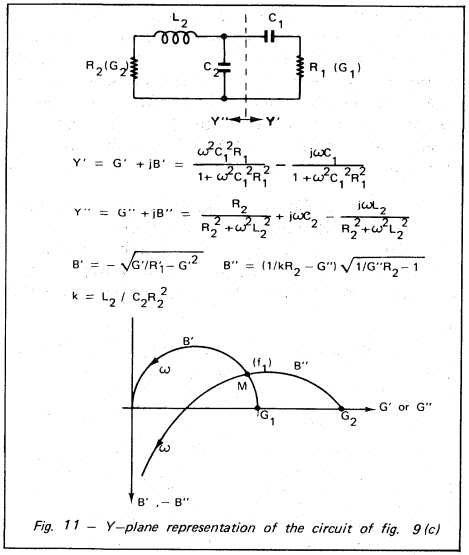


Fig. 11 – Y-plane representation of the circuit of fig. 9 (c)

4.1.3 Four-reactance networks

Four-reactance networks are used essentially for broadband matching. The networks which will be considered in the following consist of two two-reactance sections in cascade. Some networks have pseudo low-pass filter character, others band-pass filter character. In principle, the former show narrower bandwidth since they extend the impedance transformation to very low frequencies unnecessarily, while the latter insure good matching over a wide frequency band around the center frequency only (see Fig. 14).

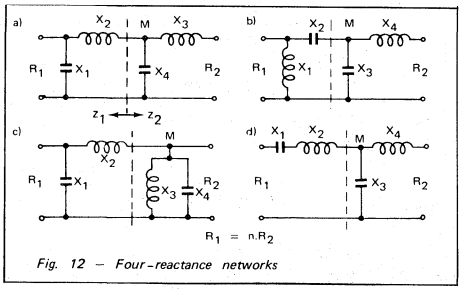


Fig. 12 – Four-reactance networks

The two-reactance sections used in above networks have either transformation properties or compensation properties. Impedance transformation is obtained with one series reactance and one shunt reactance. Compensation is made with both reactances in series or in shunt.

If two cascaded transformation networks are used, transformation is accomplished partly by each one.

With four-reactance networks there are two frequencies. f_1 and f_2, at which the transformation from R_1 into R_2 is exact. These frequencies may also coincide.

For network (b) for instance, at point M, R_1 or R_2 is transformed into $\sqrt{R_1R_2}$ when both frequencies fall together. At all points (M), Z_1 and Z_2 are conjugate if the transformation is exact.

In the case of Figure 12 (b) the reactances are easily calculated for equal frequencies:

$$X_1 = \frac{R_1}{\sqrt{\sqrt{n}-1}},\quad X_2 = R_1\sqrt{\frac{\sqrt{n}-1}{n}}$$

$$X_1.X_4 = R_1.R_2 = X_2.X_3$$

$$X_3 = \frac{R_1}{\sqrt{n(\sqrt{n}-1)}},\quad X_4 = \frac{R_1}{n}\sqrt{\sqrt{n}-1}$$

For network (a) normally, at point (M), Z_1 and Z_2 are complex. This pseudo low-pass filter has been computed elsewhere (Ref. (3)). Many tables can be found in the literature for networks of four and more reactances having Tchebyscheff character or maximally-flat response (Ref. (3), (4) and (6)).

Figure 13 shows the transformation path from R_1 to R_2 for networks (a) and (b) on a Smith-Chart (refer also to section 4.2, Graphic Design).

Case (a) has been calculated using tables mentioned in Ref. (4).

Case (b) has been obtained from the relationship given above for $X_1 \ldots X_4$. Both apply to a transformation ratio equal to 10 and for $R_1 = 1$.

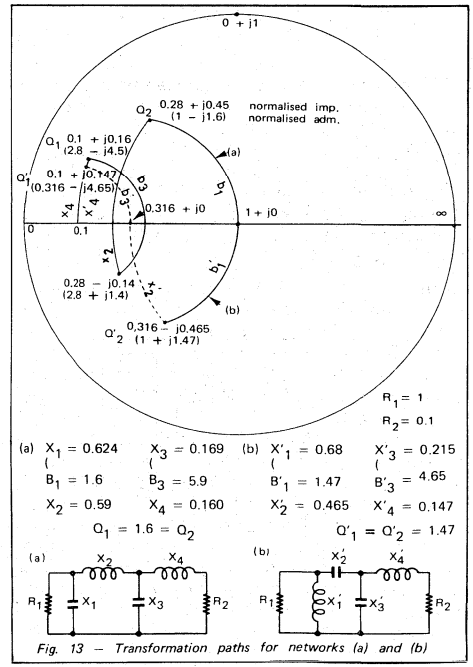


Fig. 13 – Transformation paths for networks (a) and (b)

There is no simple relationship for $X'_1 \ldots X'_4$ of network (b) if f_1 is made different from f_2 for larger bandwidth.

Figure 14 shows the respective bandwidths of network (a) and (b) for the circuits shown in Figure 13.

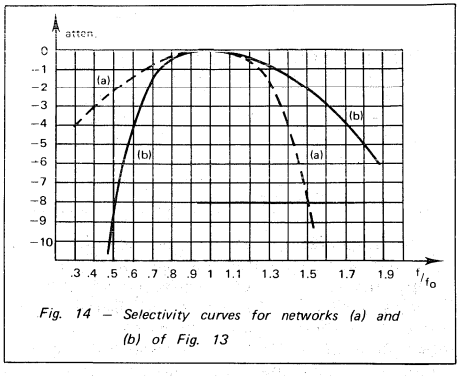


Fig. 14 – Selectivity curves for networks (a) and (b) of Fig. 13

If the terminations contain a reactive component, the computed values for X_1 or X_4 may be adjusted to compensate for this.

For configuration (a), it can be seen from Figure 13, that in the considered case the Q's are equal to 1.6.

For configuration (b) Q'_1, which is equal to Q'_2, is fixed for each transformation ratio.

n	2	4	8	10	16
$Q'_1 = Q'_2$	0.65	1	1.35	1.46	1.73

$$Q' = \sqrt{\sqrt{n} - 1}$$

The maximum value of reactance that the terminations may have for use in this configuration can be determined from the above values of Q'.

If R1 is the load resistance of a transistor, the internal transistor resistance may not be equal to R_1. In this case the selectivity curve will be different from the curves given in Figure 14. Figure 15 shows the selectivity for networks (a) and (b) when the source resistance R_1 is infinite.

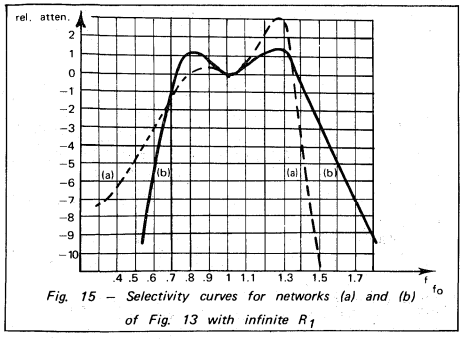


Fig. 15 – Selectivity curves for networks (a) and (b) of Fig. 13 with infinite R_1

From Figure 15 it can be seen that network (a) is more sensitve to R_1 changes than network (b).

As mentioned earlier, the four-reactance network can also be thought of as two cascaded two-reactance sections; one used for transformation, the other for compensation. Figure 16 shows commonly used compensation networks, together with the associated L-section.

The circuit of Figure 16 (a) can be compared to the three-reactance network shown in Figure 9 (c). The difference is that capacitor C_2 of that circuit has been replaced by a L-C circuit. The resulting improvement may be seen by comparing Figure 17 with Figure 11.

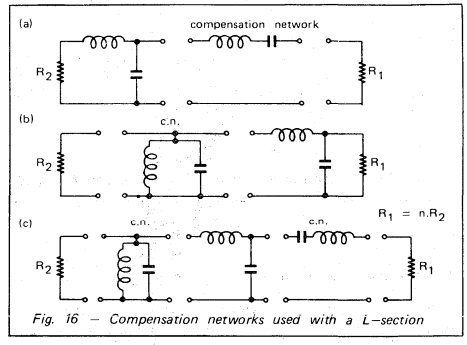
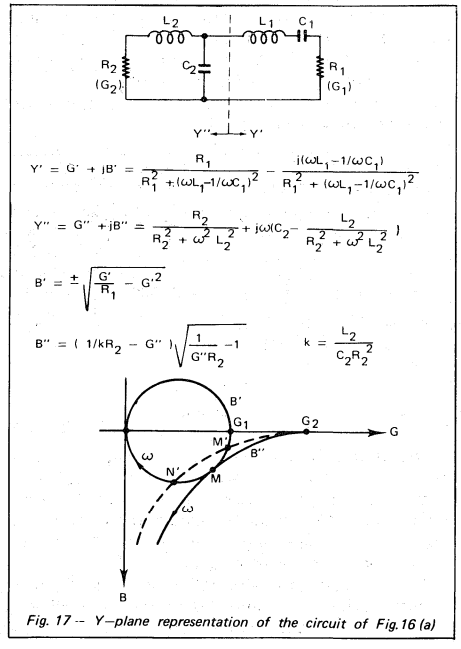


Fig. 16 – Compensation networks used with a L-section



$$Y' = G' + jB' = \frac{R_1}{R_1^2 + (\omega L_1 - 1/\omega C_1)^2} - \frac{j(\omega L_1 - 1/\omega C_1)}{R_1^2 + (\omega L_1 - 1/\omega C_1)^2}$$

$$Y'' = G'' + jB'' = \frac{R_2}{R_2^2 + \omega^2 L_2^2} + j\omega\left(C_2 - \frac{L_2}{R_2^2 + \omega^2 L_2^2}\right)$$

$$B' = \pm\sqrt{\frac{G'}{R_1} - G'^2}$$

$$B'' = (1/kR_2 - G'')\sqrt{\frac{1}{G''R_2} - 1} \qquad k = \frac{L_2}{C_2 R_2^2}$$

Fig. 17 – Y–plane representation of the circuit of Fig. 16 (a)

By adding one reactance, exact impedance transformation is achieved at two frequencies. It is now possible to choose component values such that the point of intersection M' occurs at the same frequency f_1 on both curves and simultaneously that N' occurs at the same frequency f_2 on both curves. Among the infinite number of possible intersections, only one allows to achieve this.

When M' and N' coincide in M, the new condition $\frac{dX'}{df} = \frac{dX''}{df}$ can be added to the condition $X' = -X''$ (for three-networks) and similarly $R'=R''$ and $\frac{dR'}{df} = \frac{dR''}{df}$.

If f_1 is made different from f_2, a larger bandwidth can be achieved at the expense of some ripple inside the band.

Again, a general solution of the above equations leads to still more complicated calculations than in the case of three-reactance networks. Therefore, tables are preferable (Ref. (3), (4) and (6)).

The circuit of Figure 16 (b) is dual of the circuit of of Figure 14 (a) and does not need to be treated separately. It gives exactly the same results in the Z-plane. Figure 16 (c) shows a higher order compensation requiring six reactive elements.

The above discussed matching networks employing compensation circuits result in narrower bandwidths than the former solutions (see paragraph 4.1.3) using two transformation sections. A matching with higher order compensation such as in Figure 16 (c) is not recommended. Better use can be made of the large number of reactive elements using them all for transformation.

When the above configurations are realized using short portions of transmission lines, the equations or the usual tables no longer apply. The calculations must be carried out on a computer, due to the complexity. However, a graphic method can be used (see next section) which will consist essentially in tracing a transformation path on the Z-Y-chart using the computed lumped element values and replacing it by the closest path obtained with distributed constants. The bandwidth change is not significant as long as short portions of lines are used (Ref. (13)).

4.1.4 Matching networks using quarter-wave transformers

At sufficiently high frequencies, where $\lambda/4$-long lines of practical size can be realized, broadband transformation can easily be accomplished by the use of one or more $\lambda/4$-sections.

Figure 18 summarizes the main relations for (a) one-section and (b) two-section transformation.

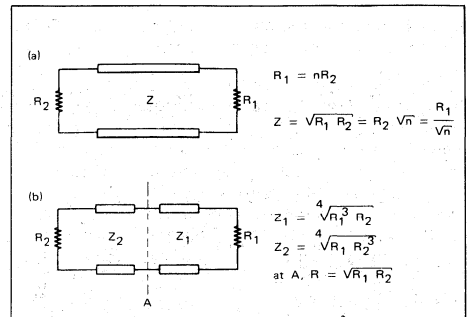


Fig. 18 – Transformation networks using $\lambda/4$-long transmission lines

A compensation network can be realized using a $\lambda/2$-long transmission line.

Figures 19 and 20 show the selectivity curves for different transformation ratios and section numbers.

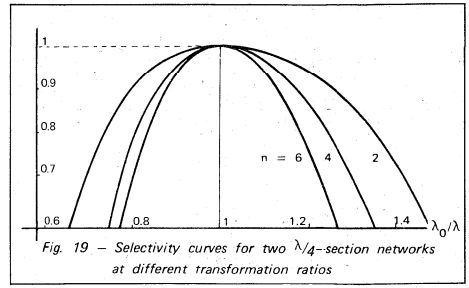


Fig. 19 – Selectivity curves for two $\lambda/4$-section networks at different transformation ratios

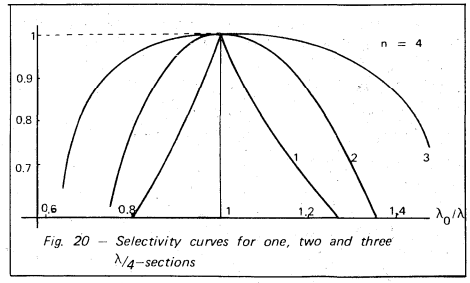


Fig. 20 – Selectivity curves for one, two and three $\lambda/4$-sections

Exponential lines

Exponential lines have largely frequency independent transformation properties.

The characteristic impedance of such lines varies exponentially with their length l:

$$Z = Z_o \cdot e^{kl}$$

where k is a constant,
but these properties are preserved only if k is small.

4.1.5 Broadband matching using band-pass filter type networks. High Q case.

The above circuits are applicable to devices having low input or output Q, if broadband matching is required. Generally, if the impedances to be matched can be represented for instance by a resistor R in series with an inductor L (sometimes a capacitor C) within the band of interest and if L is sufficiently low, the latter can be incorporated into the first inductor of the matching network. This is also valid if the representation consists of a shunt combination of a resistor and a reactance

Practically this is feasible for Q's around one or two. For higher Q's or for input impedances consisting of a series or parallel resonant circuit (see Fig. 2), as it appears to be for large bandwidths, a different treatment must be followed.

Let us first recall that, as shown by Bode and Fano (Ref. (7) and (8)), limitations exist on the impedance matching of a complex load. In the example of Figure 21, the load to be matched consists of a capacitor C and a resistor R in shunt.

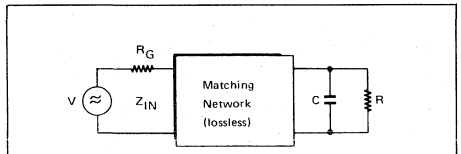


Fig. 21 – General matching conditions

The reflection coefficient between transformed load and generator is equal to:

$$\Gamma = \frac{Z_{IN} - R_g}{Z_{IN} + R_g}$$

$\Gamma = 0$, perfect matching,

$\Gamma = 1$, total reflection.

The ratio of reflected to incident power is:

$$\frac{Pr}{Pi} = |\Gamma|^2$$

The fundamental limitation on the matching takes the form:

$$\int_{\omega=0}^{\infty} \ln\left(\frac{1}{|\Gamma|}\right) d\omega \leqslant \frac{\pi}{RC}$$ Bode equation

and is represented in Figure 22.

The meaning of Bode equation is that the area S under the curve cannot be greater than $\frac{\pi}{RC}$ and therefore, if matching is required over a certain bandwidth, this can only be done at the expense of less power transfer within the band. Thus, power

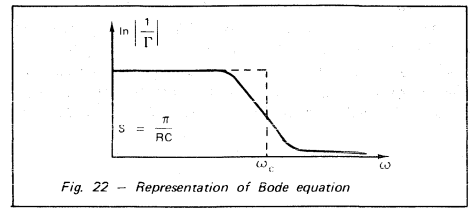


Fig. 22 – Representation of Bode equation

transfer and bandwidth appear as interchangeable quantities.

It is evident that the best utilization of the area S is obtained when $|\Gamma|$ is kept constant over the desired band ω_C and made equal to 1 over the rest of the spectrum. Then $|\Gamma| = e^{-\frac{\pi}{\omega_c RC}}$ within the band and no power transfer happens outside.

A network fulfilling this requirement cannot be obtained in practice as an infinite number of reactive elements would be necessary.

If the attenuation a is plotted versus the frequency for practical cases, one may expect to have curves like the ones shown in Figure 23 for a low-pass filter having Tchebyscheff character.

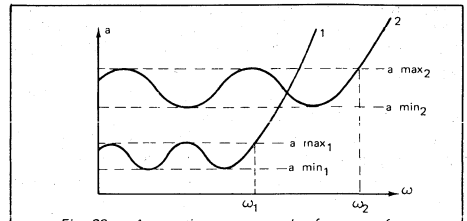


Fig. 23 – Attenuation versus angular frequency for different bandwidths with same load

For a given complex load, an extension of the bandwidth from ω_1 to ω_2, is possible only with a simultaneous increase of the attenuation a. This is especially noticeable for Q's exceeding one or two (see Figure 24).

Thus, devices having relatively high input Q's are useable for broadband operation, provided the consequent higher attenuation or reflection introduced is acceptable.

The general shape of the average insertion losses or attenuation a (neglecting the ripple) of a low-pass impedance matching network is represented in Figure 24 as a function of 1/Q for different numbers of network elements n (ref. (3)).

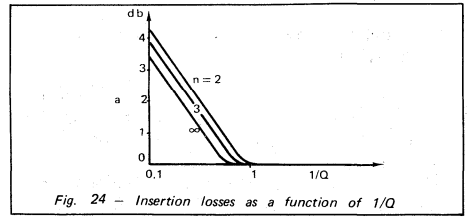


Fig. 24 – Insertion losses as a function of 1/Q

For a given Q and given ripple, the attenuation decreases if the number n of the network elements increases. But above n = 4, the improvement is small.

For a given attenuation a and bandwidth, the larger n the smaller the ripple.

For a given attenuation and ripple, the larger n the larger the bandwidth.

Computations show that for $Q < 1$ and $n \leq 3$ the attenuation is below 0.1 db approximately. The impedance transformation ratio is not free here. The network is a true low-pass filter. For a given load, the optimum generator impedance will result from the computation.

Before impedance transformation is introduced, a conversion of the low-pass prototype into a band-pass filter type network must be made. Figure 25 summarizes the main relations for this conversion.

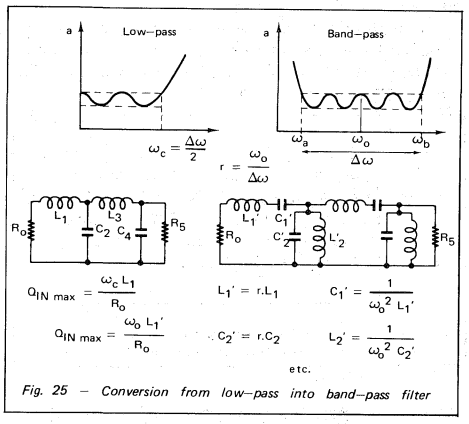


Fig. 25 – Conversion from low–pass into band–pass filter

r is the conversion factor.

For the band-pass filter, Q_{IN} max or the maximum possible input Q of a device to be matched, has been increased by the factor r (from Figure 25, $Q'_{IN\ max} = r.Q_{IN\ max}$).

Impedance inverters will be used for impedance transformation. These networks are suitable for insertion into a band-pass filter without affecting the transmission characteristics.

Figure 26 shows four impedance inverters. It will be noticed that one of the reactances is negative and must be combined in the band-pass network with a reactance of at least equal positive value. Insertion of the inverter can be made at any convenient place (Ref. (3) and (9)).

When using the band-pass filter for matching the input impedance of a transistor, reactances L'_1 C'_1 should be made to resonate at ω_o by addition of a convenient series reactance.

As stated above, the series combination of Ro, L'_1 and C'_1 normally constitutes the equivalent input network of a transistor when considered over a large bandwidth. This is a good approximation up to about 500 MHz.

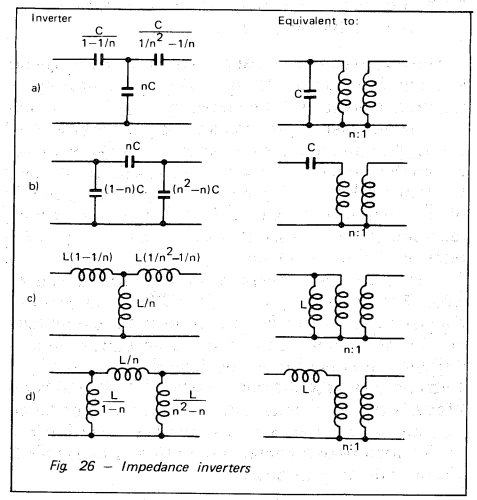


Fig. 26 – Impedance inverters

In practice the normal procedure for using a band-pass filter type matching network will be the following:

(1) For a given bandwidth, center frequency and input impedance of a device to be matched e.g. to 50 ohms, first determine Q_{IN}' from the data sheet as $\frac{\omega_o L'_1}{R_o}$ after having eventually added a series reactor for centering,

(2) Convert the equivalent circuit $R_o L_1'$ C_1' into a low-pass prototype R_o L_1 and calculate Q_{IN} using the formulas of Figure 25,

(3) Determine the other reactance values from tables (Ref. (3)) for the desired bandwidth,

(4) Convert the element values found by step (3) into series or parallel resonant circuit parameters,

(5) Insert the impedance inverter in any convenient place.

In the above discussions, the gain roll-off has not been taken into account. This is of normal use for moderate bandwidths (30% for ex.). However, several methods can be employed to obtain a constant gain within the band despite the intrinsic gain decrease of a transistor with frequency.

Tables have been computed elsewhere (Ref. (10)) for matching networks approximating 6 db/octave attenuation versus frequency.

Another method consists in using the above mentioned network and then to add a compensation circuit as shown for example in Figure 27.

6

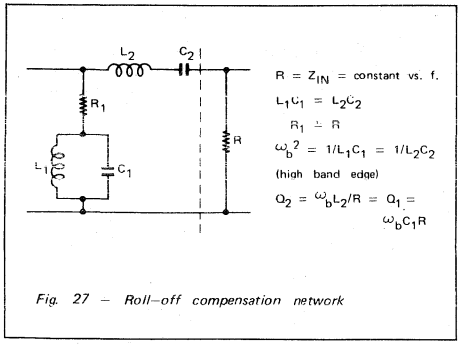


Fig. 27 – Roll-off compensation network

Resonance ω_b is placed at the high edge of the frequency band. Choosing Q correctly, roll-off can be made 6 db/octave.

The response of the circuit shown in Figure 27 is expressed by:

$$\frac{1}{1 + Q^2 \left(\frac{\omega}{\omega_b} - \frac{\omega_b}{\omega}\right)^2} \text{ where } \omega < \omega_b$$

This must be equal to $\frac{\omega}{\omega_b}$ for 6db/octave compensation.

At the other band edge a, exact compensation can be obtained if:

$$Q = \frac{\left(\frac{\omega_b}{\omega_a}\right)^2 - 1}{\frac{\omega_a}{\omega_b} - \left(\frac{\omega_b}{\omega_a}\right)^2}$$

4.1.6 Line Transformers

The broadband properties of line transformers make them very useful in the design of broadband impedance matching networks (Ref. (11) and (12)).

A very common form is shown by Figure 28. This is a 4:1 impedance transformer. Other transformation ratios like 9 : 1 or 16 : 1 are also often used but will not be considered here.

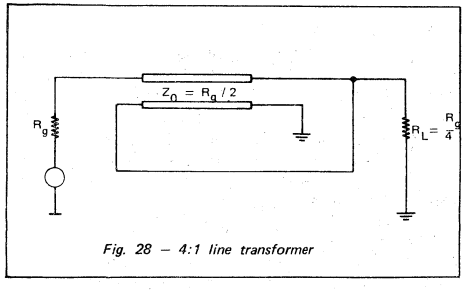


Fig. 28 – 4:1 line transformer

The high frequency cut-off is determined by the length of line which is usually chosen smaller than λ min/8. Short lines extend the high frequency performance.

The low frequency cut-off is determined first by the length of line, long lines extending the low frequency performance of the transformer. Low frequency cut-off is also improved by a high even mode impedance, which can be achieved by the use of ferrite material. With matched ends, no power is coupled through the ferrite which cannot saturate.

For matched impedances, the high frequency attenuation a of the 4 : 1 transformer is given by:

$$a = \frac{(1+3\cos 2\pi l/\lambda)^2 + 4\sin^2 2\pi l/\lambda}{4(1+\cos 2\pi l/\lambda)^2}$$

For $l = \lambda/4$, a = 1.25 or 1 db ; for $l = \lambda/2$, $a = \infty$.

The characteristic impedance of the line transformer must be equal to:

$$Zo = \sqrt{Rg.R}$$

Figures 29 and 30 show two different realizations of 4 : 1 transformers for a 50 to 12.5 ohm-transformation designed for the band 118-136 MHz.

The transformers are made of two printed circuit boards or two ribbons stuck together and connected as shown in Figures 29 and 30.

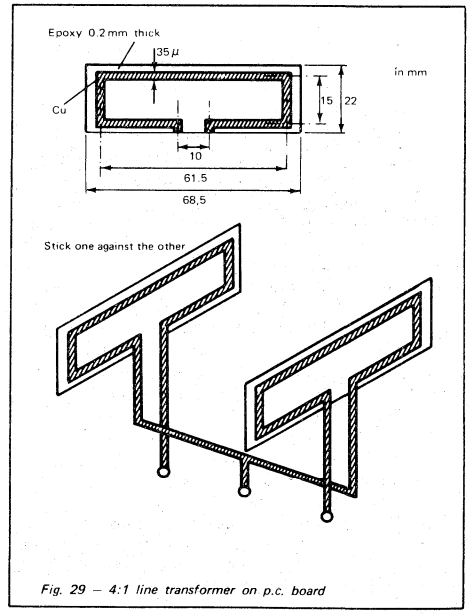
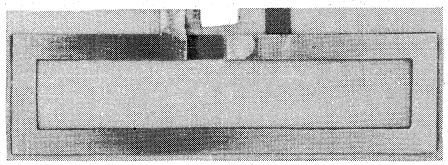
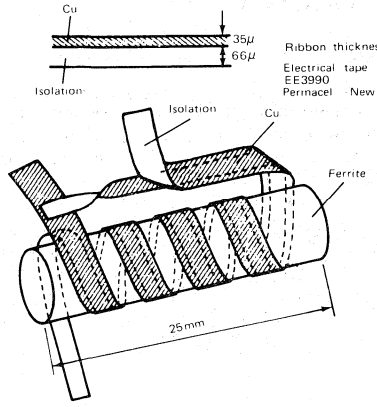


Fig. 29 – 4:1 line transformer on p.c. board

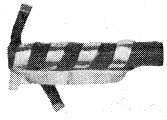


Line transformer on p.c. board (Fig. 29)



Stick one ribbon (1.5mm wide) against the other (2.5)
Total length per ribbon 9cm.
Turns 3.5

Fig. 30 – 4:1 copper ribbon line transformer with ferrite



Line transformer on ferrite (Fig. 30)

4.2 GRAPHIC DESIGN

The common method of graphic design makes use of the Impedance-Admittance Chart (Smith Chart).

It is applicable to all ladder-type networks as encountered in matching circuits.

Matching is supposed to be realized by the successive algebraic addition of reactances (or susceptances) to a given start impedance (or admittance) until another end impedance (or admittance) is reached.

Impedance chart and admittance chart can be superimposed and used alternatively due to the fact that an immittance point, defined by its reflection coefficient Γ with respect to a reference, is common to the Z-chart and the Y-chart, both being representations in the Γ-plane.

$$\Gamma = \frac{Z-R_S}{Z+R_S} = \gamma_r + j\gamma_i$$

$$\Gamma = \frac{G_S-Y}{G_S+Y} \qquad R_S = \frac{1}{G_S} = \text{Characteristic impedance of the line}$$

More precisely, the Z-chart is a plot in the Γ-plane, while the Y-chart is a plot in the $-\Gamma$-plane. The change from the Γ to $-\Gamma$-plane is accounted for in the construction rules given below.

Figure 31 and 32 show the representation of normalized Z and Y respectively, in the Γ-plane.

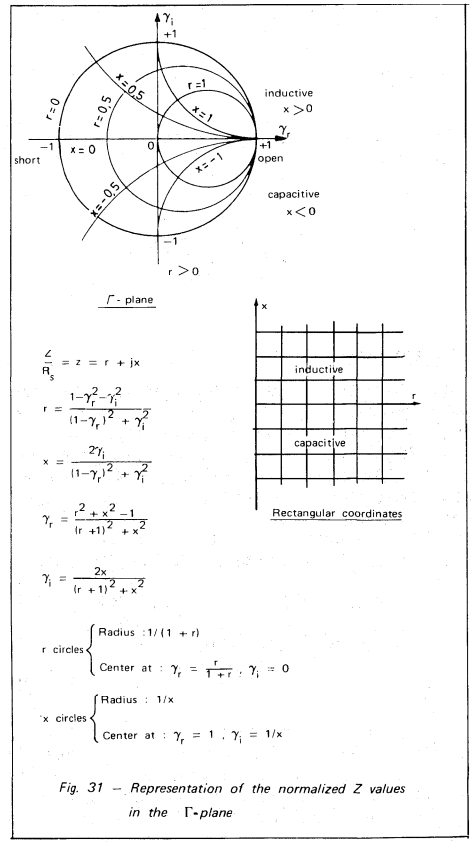
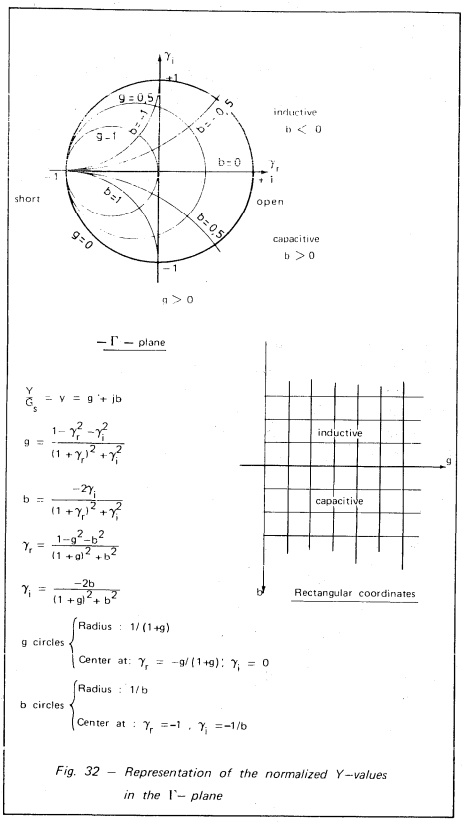


Fig. 31 – Representation of the normalized Z values in the Γ-plane



$\frac{Y}{G_s} = y = g + jb$

$g = \frac{1-\gamma_r^2-\gamma_i^2}{(1+\gamma_r)^2+\gamma_i^2}$

$b = \frac{-2\gamma_i}{(1+\gamma_r)^2+\gamma_i^2}$

$\gamma_r = \frac{1-g^2-b^2}{(1+g)^2+b^2}$

$\gamma_i = \frac{-2b}{(1+g)^2+b^2}$

g circles { Radius : 1/(1+g); Center at: $\gamma_r = -g/(1+g)$; $\gamma_i = 0$

b circles { Radius : 1/b; Center at : $\gamma_r = -1$, $\gamma_i = -1/b$

Fig. 32 – Representation of the normalized Y–values in the Γ– plane

The Z-chart is used for the algebraic addition of series reactances. The Y-chart is used for the algebraic addition of shunt reactances.

For the practical use of the charts, it is convenient to make the design on transparent paper and then place it on a usual Smith-chart of impedance type (for example). For the addition of a series reactor, the chart will be placed with "short" to the left. For the addition of a shunt reactor, it will be rotated by 180° with "short" (always in terms of impedance) to the right.

The following design rules apply. They can very easily be found by thinking of the more familiar Z and Y representation in reactangular coordinates.

For joining two impedance points, there are a infinity of solutions. Therefore, one must first decide on the number of reactances that will constitute the matching network. This number is related essentially to the desired bandwidth and the transformation ratio.

Addition of	Chart to be used	Direction	Using curve of constant
series R	Z	open (in terms of admittance)	x
series G	Y	short (in terms of admittance)	b
series C ($+\frac{1}{j\omega C}$)	Z	ccw	r
shunt C ($+j\omega C$)	Y	cw	g
series L ($+j\omega L$)	Z	cw	r
shunt L ($+\frac{1}{j\omega L}$)	Y	ccw	g

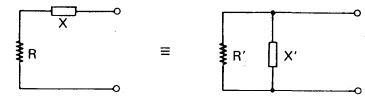
Secondly, one must choose the operating Q of the circuit, which is also related to the bandwidth. Q can be defined at each circuit node as the ratio of the reactive part to the real part of the impedance at that node. The Q of the circuit, which is normally referred to, is the highest value found along the path.

Constant Q curves can be superimposed to the charts and used in conjunction with them. In the Γ -plane, Q-curves are circles with a radius equal to $\sqrt{1+\frac{1}{Q^2}}$ and a center at the point $\pm\frac{1}{Q}$ on the imaginary axis, which is expressed by:

$$Q = \frac{x}{r} = \frac{2\gamma_i}{1-\gamma_r^2-\gamma_i^2} \qquad \gamma_r^2 + (\gamma_i + \frac{1}{Q})^2 = 1 + \frac{1}{Q^2}.$$

The use of the charts will be illustrated with the help of an example.

The following series shunt conversion rules also apply:



$$R = \frac{R'}{1+\frac{R'^2}{X'^2}} \qquad G' = \frac{1}{R'} = \frac{R}{R^2+X^2}$$

$$X = \frac{X'}{1+\frac{X'^2}{R'^2}} \qquad -B' = \frac{1}{X'} = \frac{X}{R^2+X^2}$$

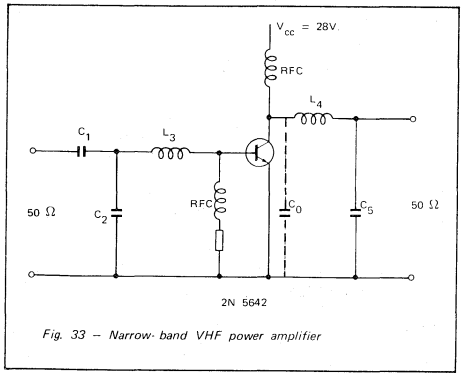


Fig. 33 – Narrow-band VHF power amplifier

Figure 33 shows the schematic of an amplifier using the 2N5642 RF power transistor. Matching has to be achieved at 175 MHz, on a narrow band basis.

The rated output power for the device in question is 20 W at 175 MHz and 28 V collector supply. The input impedance at these conditions is equal to 2.6 ohms in parallel with -200 pF (see data Sheet). This converts to a resistance of 1.94 ohms in series with a reactance of 1.1 ohm.

The collector load must be equal to:

$$\frac{[\,Vcc - Vce\,(sat)\,]^2}{2 \times P_{out}} \text{ or } \frac{(28-3)^2}{40} = 15.6 \text{ ohms.}$$

The collector capacitance given by the data sheet is 40 pF, corresponding to a capacitive reactance of 22.7 ohms.

The output impedance seen by the collector to insure the required output power and cancel out the collector capacitance must be equal to a resistance of 15.6 ohms in parallel with an inductance of 22.7 ohms. This is equivalent to a resistance of 10.6 ohms in series with an inductance of 7.3 ohms.

The input Q is equal to, 1.1/1.94 or 0.57 while the output Q is 7.3/10.6 or 0.69.

It is seen that around this frequency, the device has good broadband capabilities. Nevertheless, the matching circuit will be designed here for a narrow band application and the effective Q will be determined by the circuit itself not by the device.

Figure 34 shows the normalized impedances (to 50 ohms).

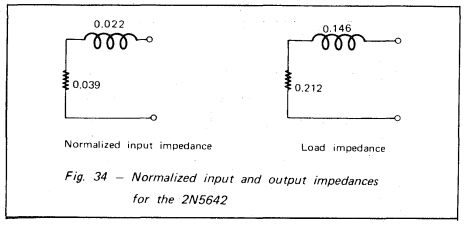


Fig. 34 – Normalized input and output impedances for the 2N5642

Figure 35 shows the diagram used for the graphic design of the input matching circuit. The circuit Q must be larger than about 5 in this case and has been chosen equal to 10. At Q = 5, C_1 would be infinite. The addition of a finite value of C_1 increases the circuit Q and therefore the selectivity. The normalized values between brackets in the Figure are admittances (g + jb).

At f = 175MHz, the following results are obtained:

$$\omega L_3 = 50x_3 = 50\,(0.39 - 0.022) = 18.5 \text{ ohms} \quad \therefore L_3 = 16.8 \text{ nH}$$

$$\omega C_2 = \frac{1}{50} b_2 = \frac{1}{50}\,(2.5 - 0.42) = 0.0416 \text{ mhos} \quad \therefore C_2 = 37.8 \text{ pF}$$

$$\frac{1}{\omega C_1} = 50x_1 = 50 \,.\, 1.75 = 87.5 \text{ ohms} \quad \therefore C_1 = 10.4 \text{ pF}$$

Figure 36 shows the diagram for the output circuit, designed in a similar way.

Here, the results are (f = 175MHz) :

$$\omega L_4 = 50.x_4 = 50\,.\,(0.4 + 0.146) = 27.3 \text{ ohms} \quad \therefore L_4 = 24.8 \text{ nH}$$

$$\omega C_5 = \frac{1}{50} b_5 = \frac{1}{50}\,.\,1.9 = 0.038 \text{ mhos} \quad \therefore C_5 = 34.5 \text{ pF}$$

The circuit Q at the output is equal to 1.9.

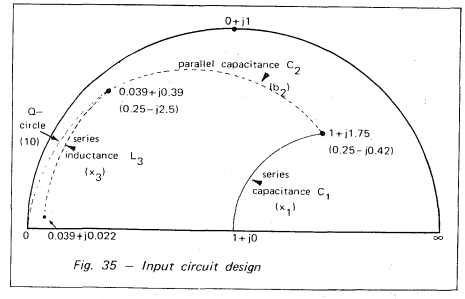


Fig. 35 – Input circuit design

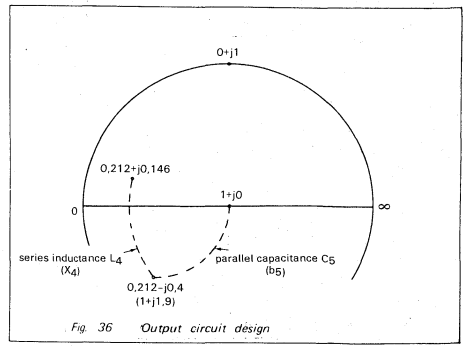


Fig. 36 Output circuit design

6

The selectivity of a matching circuit can also be determined graphically by changing the x or b values according to a chosen frequency change. The diagram will give the VSWR and the attenuation can be computed.

The graphic method is also useful for conversion from a lumped circuit design into a stripline design. The immittance circles will now have their centres on the 1 + jo point.

At low impedance levels (large circles), the difference between lumped and distributed elements is small.

5. PRACTICAL EXAMPLE

The example shown refers to a broadband amplifier stage using a 2N 6083 for operation in the VHF-band 118-136 MHz. The 2N 6083 is a 12.5 V-device and, since amplitude modulation is used at these transmission frequencies, that choice supposes low level modulation associated with a feedback system for distortion compensation.

Line transformers will be used at the input and output. Therefore the matching circuits will reduce to two-reactance networks, due to the relatively low impedance transformation ratio required.

5.1 DEVICE CHARACTERISTICS

Input impedance of the 2N 6083 at 125 MHz:

$$R_p = 0.9 \text{ ohms}$$

$$C_p = -390 \text{ pF}$$

Rated output power:

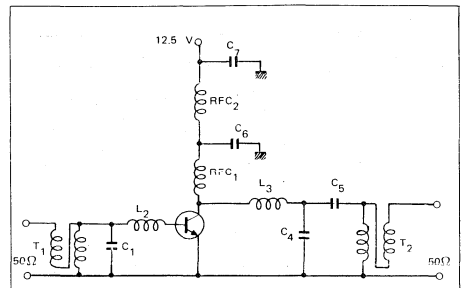
30W for 8W input at 175MHz. From the data sheet it appears that at 125MHz, 30W output will be achieved with about 4W input.

Output impedance:

$$\frac{[V_{cc} - V_{ce\,(sat)}]^2}{2 \times P_{out}} = \frac{100}{60} = 1.67 \text{ ohms}$$

$$C_{out} = 180 \text{ pF at } 125 \text{ MHz}$$

5.2 CIRCUIT SCHEMATIC



C_1 = 300 pF (chip)
L_2 = 4.2 nH (adjust)
L_3 = 8 nH (adjust)
C_4 = 130 pF (chip)
C_5 = 750 pF (chip)
C_6 = 2.2 μF

T_1, T_2 see Figure 30
RFC_1 = 7 turns
6.3 mm coil diameter
0,8 mm wire diameter
RFC_2 = 3 turns on ferrite bead
C_7 = 0.68 μF

Fig. 37 – Circuit schematic

5.3 TEST RESULTS

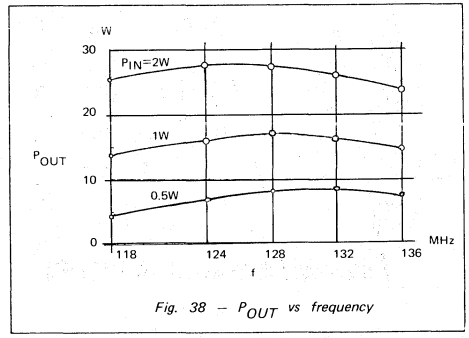


Fig. 38 – P_{OUT} vs frequency

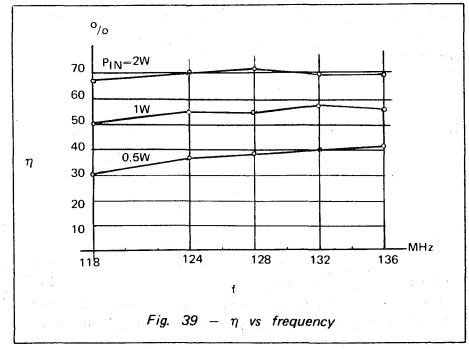


Fig. 39 – η vs frequency

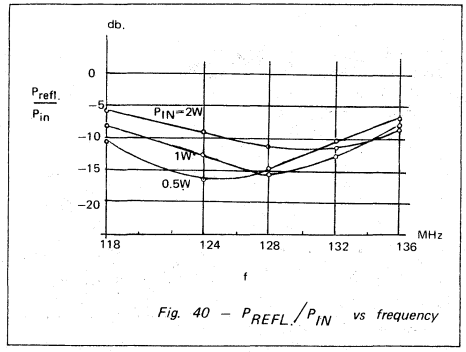
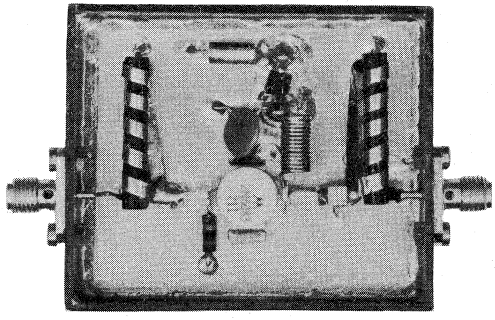


Fig. 40 – $P_{REFL.}/P_{IN}$ vs frequency



118-136 MH2 amplifier (see Fig. 37) before coil adjustment.

Acknowledgements:

The author is indebted to Mr. T. O'Neal for the fruitful discussions held with him. Mr. O'Neal designed the circuit shown in Figure 37; Mr. J. Hennet constructed and tested the lab model.

6. LITERATURE

1. Motorola Application Note AN-282 A "Systemizing RF Power Amplifier Design"

2. W. E. Everitt and G. E. Anner
"Communication Engineering"
McGraw-Hill Book Company, Inc.

3. G. L. Matthaei, L. Young, E. M. T. Jones
"Microwave Filters, Impedance-Matching Networks and Coupling Structures"
McGraw-Hill Book Company, Inc.

4. G. L. Matthaei
"Tables of Chebyshew Impedance-Transforming Networks of Low-Pass Filter Form"
Proc. IEEE, August 1964

5. Motorola Application Note AN-267
"Matching Network Designs with Computer Solutions"

6. E. G. Cristal
"Tables of Maximally Flat Impedance-Transforming Networks of Low-Pass-Filter Form"
IEEE Transactions on Microwave Theory and Techniques
Vol. MTT 13, No 5, September 1965
Correspondence

7. H. W. Bode
"Network Analysis and Feedback Amplifier Design"
D. Van Nostrand Co., N.Y.

8. R. M. Fano
"Theoretical limitations on the Broadband Matching of Arbitrary Impedances"
Journal of Franklin Institute, January-February 1950

9. J. H. Horwitz
"Design Wideband UHF-Power Amplifiers"
Electronic Design 11, May 24, 1969

10. O. Pitzalis, R. A. Gilson
"Tables of Impedance Matching Networks which Approximate Prescribed Attenuation Versus Frequency Slopes"
IEEE Transactions on Microwave Theory and Techniques
Vol. MTT-19, No 4, April 1971

11. C. L. Ruthroff
"Some Broadband Transformers"
Proc. IRE, August 1959

12. H. H. Meinke
"Theorie der H. F. Schaltungen"
München, Oldenburg 1951

BROADBAND TRANSFORMERS AND POWER COMBINING TECHNIQUES FOR RF

Prepared by
H. Granberg
RF Circuits Engineering

INTRODUCTION

The following discussion focuses on broadband transformers for RF power applications with practical examples of various types given with performance data. Detailed design formula are available in the Reference section. Power combining techniques useful in designing high power amplifiers are discussed in detail.

BROADBAND TRANSFORMERS

The input and output transformers are among the most critical components in the design of a multi-octave amplifier. The total performance of the amplifier (linearity, efficiency, VSWR, gain flatness) will depend on their quality. Transformers with high impedance ratios and for low impedances are more difficult to design in general. In the transmission line transformers very low line impedances are required, which makes them impractical for higher than 16:1 impedance ratios in a 50-Ohm system. Other type transformers require tight coupling coefficients between the primary and secondary, or excessive leakage inductances will reduce the effective bandwidth. Twisted line transformers (Figure 1C, D, F, G) are described in References 1, 2, and 4. Experiments have shown that the dielectric losses in certain types of magnet wire, employed for the twisted lines, can limit the power handling capability of such transformers. This appears as heat generated within the transformer at higher frequencies, although part of this may be caused by the losses in the magnetic core employed to improve the low frequency response. At low frequencies, magnetic coupling between the primary and secondary is predominant. At higher frequencies the leakage inductance increases and the permeability of the magnetic material decreases, limiting the bandwidth unless tight capacitive coupling is provided. In a transmission line transformer this coupling can be clearly defined in the form of a line impedance.

The required minimum inductance on the low impedance side is:

$$L = \frac{4R}{2\pi f}$$

where L = Inductance in μH
R = Impedance in Ohms
f = Frequency in MHz

This applies to all transformers described here.

Some transformers, which exhibit good broad band performance and are easy to duplicate are shown in Figure 1.

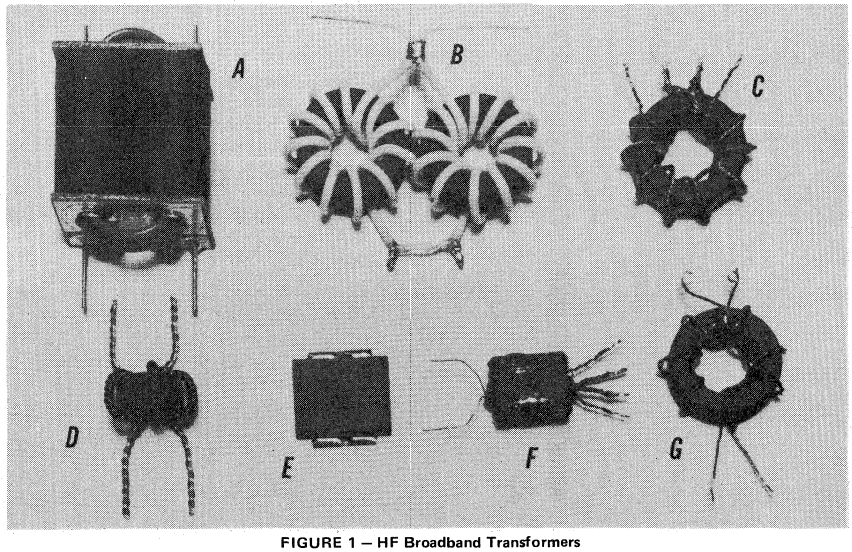


FIGURE 1 – HF Broadband Transformers

Transformers E and F are intended for input applications, although A in a smaller physical form is also suitable. In E, the windings are photo etched on double sided copper-Kapton* (or copper-fiberglass) laminate. The dielectric thickness is 3 mils, and the winding area is 0.25 in^2.

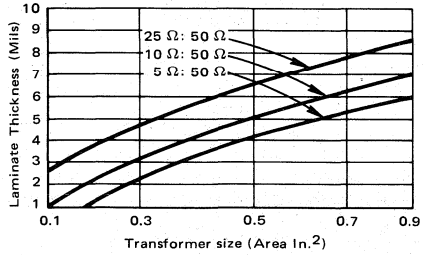


FIGURE 2 — Laminate Thickness versus Winding Area

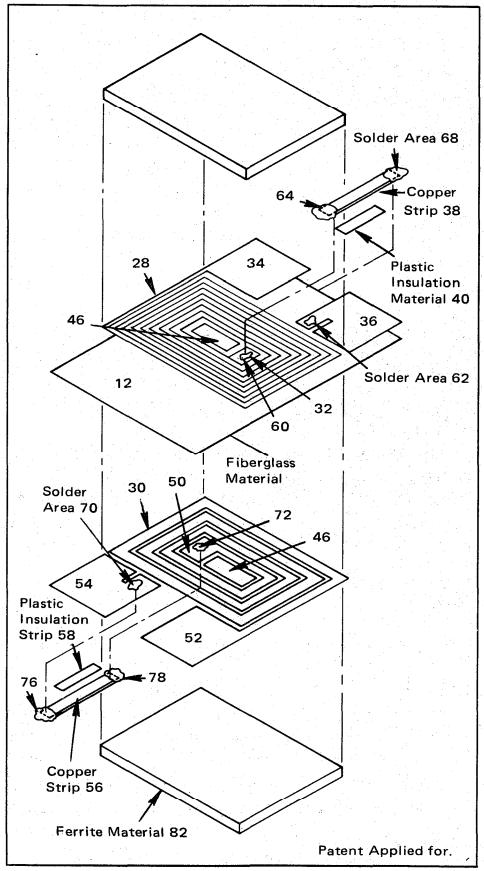


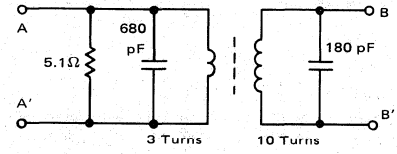
FIGURE 3 — Detailed Structure of Transformer Shown in Figure 1E

*Trademark of E. I. DuPont, De Nemours and Co., Inc.

Ferrite plates (μ_r = 2000 to 3000) are cemented on each side to improve the low frequency response. This type transformer in the size shown, can handle power levels to 10 W. Figure 2 shows curves for laminate thickness versus winding area for various impedance ratios.

Impedance ratios of this transformer are not limited to integers as 1:1, 4:1 — N:L, and the dc isolated primary and secondary have an advantage in certain circuit configurations. This design will find its applications in high volume production or where the small physical size is of main concern. Table 1 shows the winding configuration and measured data of the transformer shown in Figure 3.

TABLE 1 — Impedance at Terminals BB'
Transformer Terminated as Shown



f (MHz)	R_p (Ohms)	X_p (Ohms)
1.0	50.7	+j 81
2.0	53.0	+j 185
4.0	53.1	+j 1518
8.0	53.5	-j 214
16.0	50.5	-j 79
32.0	52.9	-j 30

In the transformer shown in Figure 1F and Table 2, a regular antenna balun core is employed (Indiana General F684-1 or equivalent). Lines A and B each consist of two twisted pairs of AWG #30 enameled wire. The line impedances are measured as 32 Ohms, which is sufficiently close to the optimum 25 Ohms calculated for 4:1 impedance ratio. ($Z_o = \sqrt{R_{in} R_L}$).

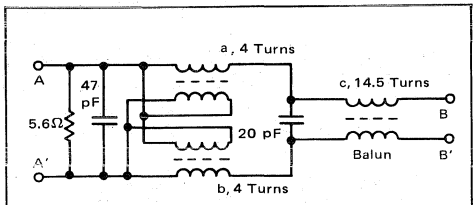
Windings a and b are wound one on top of the other, around the center section of the balun core. Line c should have an optimum Z_o of 50 Ohms. It consists of one pair of AWG #32 twisted enameled wire with the Z_o measured as 62 Ohms. The balun core has two magnetically isolated toroids on which c is wound, divided equally between each. The inductance of c should approach the combined inductance of Lines a and b (Reference 4, 6).

The reactance in the 50 Ohm port (BB') should measure a minimum of + j 200. To achieve this for a 4:1 transformer, a and b should each have three turns, and for a 9:1 transformer, four turns. When the windings are connected as a 9:1 configuration, the optimum Z_o is 16.6 Ohms, and a larger amount of high frequency compensation will be necessary. Lower impedance lines can be realized with heavier wires or by twisting more than two pairs together. (e.g., four pairs of AWG #36 enameled wire

6

would result in the Z_O of approximately 18 Ohms.) Detailed information on the manufacture of twisted wire transmission lines can be found in References 2, 4, and 8.

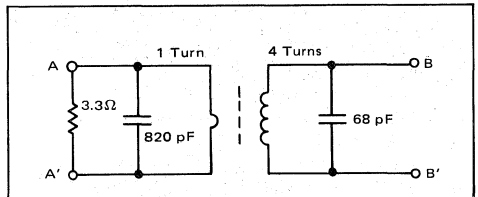
TABLE 2 – Impedance at Terminals BB'
Transformer Terminated as Shown



f (MHz)	R_p (Ohms)	X_p (Ohms)
1.0	53.0	+j 185
2.0	52.6	+j 330
4.0	52.9	+j 430
8.0	53.1	+j 600
16.0	53.2	+j 750
32.0	53.5	+j 3060

Figure 1A shows one of the most practical designs for higher impedance ratios (16 and up). The low impedance winding always consists of one turn, which limits the available ratios to integers 1, 4, 9 —— N. Data taken of this type of a 16:1 transformer is shown in Table 3, while Figure 4 illustrates the physical construction. Two tubes, 1.4" long and 1/4" in diameter – copper or brass – form the primary winding. The tubes are electrically shorted on one end by a piece of copper-clad laminate with holes for the tubes and the tube ends are soldered to the copper foil. The hole spacing should be larger than the outside diameter of the ferrite sleeves.

TABLE 3 – Impedance at Terminals BB'
Transformer Terminated as Shown



f (MHz)	R_p (Ohms)	X_p (Ohms)
1.0	54.0	+j 1030
2.0	54.0	+j 3090
4.0	54.0	+j 5800
8.0	53.9	-j 300
16.0	53.1	-j 760
32.0	53.2	-j 600

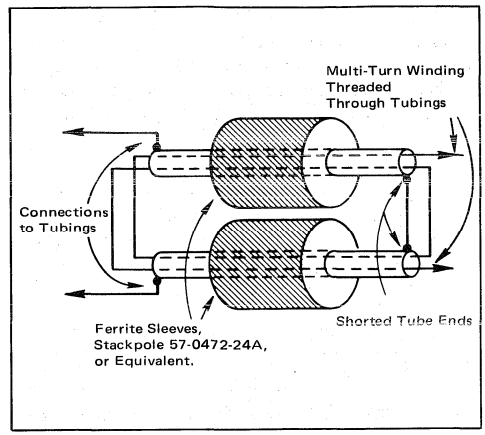


FIGURE 4 – Physical Construction of a 16:1 Transformer
(Actual Number of Turns Not Shown)

A similar piece of laminate is soldered to the opposite ends of the tubes, and the copper foil is divided into two sections, thus isolating the ends where the primary connections are made. The secondary winding is formed by threading wire with good RF insulating properties through the tubes for the required number of turns.

Although the measurements indicate negligible differences in performance for various wire sizes and types (stranded or solid), the largest possible diameter should be chosen for lower resistive losses. The initial permeability of the ferrite sleeves is determined by the minimum inductance required for the lowest frequency of operation according to the previous formula. Typical μ_r's can vary from 800 to 3000 depending upon the cross sectional area and lowest operating frequency. Instead of the ferrite sleeves, a number of toroids which may be more readily available, can be stacked.

The coupling coefficient between the primary and secondary is almost a logarithmic function of the tube diameter and length. This factor becomes more important with very high impedance ratios such as 36:1 and up, where higher coupling coefficients are required. The losses in the ferrite are determined by the frequency, permeability and flux density. The approximate power handling capability can be calculated as in Reference 4 and 6, but the ferrite loss factor should be taken into consideration. The μ_r in all magnetic materials is inversely proportional to the frequency, although very few manufacturers give this data.

Two other variations of this transformer are shown in Figure 5. The smaller version is suitable for input matching, and can handle power levels to 20 W. It employs a stackpole dual balun ferrite core 57-1845-24B. The low impedance winding is made of 1/8" copper braid. The portions of braid going through the ferrite are rounded, and openings are made in the ends with a pointed tool. The high impedance winding is threaded through the rounded portions of the braid, which was uncovered in each end of the ferrite core. (See Figures 4 and 5.)

6

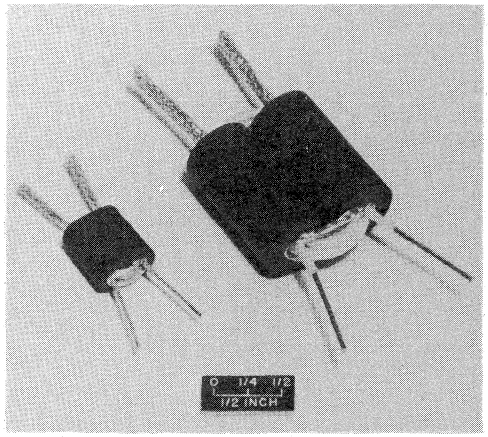


FIGURE 5 – Variations of Transformers in Figure 1A

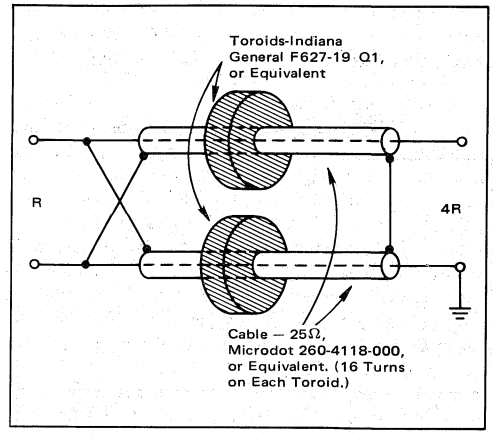


FIGURE 6 – Transformer Construction (Figure 1B)

The construction technique of the larger version transformer is similar, except two separate ferrite sleeves are employed. They can be cemented together for easier handling. This transformer is intended for output applications, with a power handling capability of 200-250 W employing Stackpole 57-0472-27A ferrites. For more detail, see Reference 7.

The transformer shown in Figure 1B is superior in bandwidth and power handling capability. Table 4 shows data taken on a 4:1 transformer of this type. The transmission lines (a and b) are made of 25-Ohm miniature co-axial cable, Microdot 260-4118-000 or equivalent. Two 50 Ohm cables can also be connected in parallel.

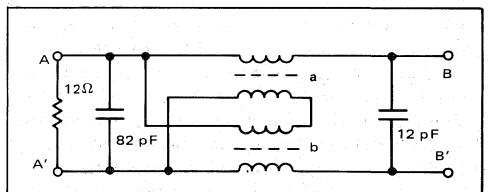
The balun, normally required to provide the balanced to unbalanced function is not necessary when the two transmission lines are wound on separate magnetic cores, and the physical length of the lines is sufficient to provide the necessary isolation between AA′ and BB′. The minimum line length required at 2.0 MHz employing Indiana General F627-19-Q1 or equivalent ferrite toroids is 4.2 inches, and the maximum permissible length at 30 MHz would be approximately 20 inches, according to formulas 9 and 10 presented in Reference 2. The 4.2 inches would amount to four turns on the toroid, and measures 1.0 μH. This complies with the results obtained with the formula given earlier for minimum inductance calculations.

Increasing the minimum required line length by a factor of 4 will provide the isolation, and the total length is still within the calculated limits. The power loss in this PTFE insulated co-axial cable is 0.03 dB/ft at 30 MHz in contrast to 0.12 dB/ft for a twisted wire line. The total line loss in the transformer will be about 0.1 dB

The number of turns on the toroids has been increased beyond the point where the flux density of the magnetic core is the power limiting factor. The combined line and core losses limit the power handling capability to approximately 300 W, which can be slightly increased by employing lower loss magnetic material.

Note the connection arrangement (Figure 6), where the braid of the cable forms the high current path of the primary.

TABLE 4 – Impedance at Terminals BB′
Transformer Terminated as Shown



f (MHz)	R_p (Ohms)	X_p (Ohms)
1.0	48.3	+j 460
2.0	48.1	+j 680
4.0	48.0	+j 920
8.0	48.0	+j 1300
16.0	48.1	+j 900
32.0	48.1	+j 690

HIGH-FREQUENCY POWER COMBINING TECHNIQUES EMPLOYING HYBRID COUPLERS

The zero degree hybrids described here are intended for adding the powers of a multiple of solid-state amplifiers, or to combine the outputs of groups of amplifiers, usually referred to as modules. With this technique, powers to the kW level at the high-frequency bands can be realized.

When reversed, the hybrids can be used for splitting signals into two or more equal phase and amplitude ports. In addition, they provide the necessary isolation between the sources. The purpose of the isolation is to keep the system operative, even at a reduced power level during a possible failure in one amplifier or module. The isolation is especially important in output combining of linear

amplifiers, where a constant load impedance must be maintained. Sometimes the inputs can be simply paralleled, and a partial system failure would not have catastrophic effects, but will merely result in increased input VSWR.

For very high frequencies and narrow bandwidths, the hybrid couplers may consist of only lengths of transmission line, such as co-axial cable. The physical lengths of the lines should be negligible compared to the highest operating frequency to minimize the resistive losses, and to avoid possible resonances. To increase the bandwidth and improve the isolation characteristics of the line, it is necessary to increase the impedance for non-transmission line currents (parallel currents) without effecting its physical length. This can be done by loading the line with magnetic material. Ideally, this material should have a linear BH curve, high permeability and low losses over a wide frequency range. For high-frequency applications, some ferrites offer satisfactory characteristics, making bandwidths of four or more octaves possible.

Depending upon the balance and phase differences between the sources, the currents should be mostly cancelled in the balun lines. In a balanced condition, very little power is dissipated in the ferrite cores, and most occurring losses will be resistive. Thus, a straight piece of transmission line loaded with a high permeability ferrite sleeve, will give better results than a multiturn toroid arrangement with its inherent higher distributed winding capacitance.

It is customary to design the individual amplifiers for 50 Ohm input and output impedances for testing purposes and standardization. 50-and 25-Ohm co-axial cable can then be employed for the transmission lines. Twisted wire lines should not be used at power levels higher than 100 Watts average, due to their higher dielectric losses.

Variations of the basic hybrid are shown in Figure 7A and B where both are suitable for power dividing or combining.

The balancing resistors are necessary to maintain a low VSWR in case one of the 50-Ohm points reaches a high impedance as a result of a transistor failure. As an input power splitter, neither 50-Ohm port will ever be subjected to a short due to the base compensation networks, should a base-emitter junction short occur. An open junction will result in half of the input power being dissipated by the balancing resistor, the other half still being delivered to the amplifier in operation. The operation is reversed when the hybrid is used as an output combiner. A transistor failure will practically always cause an increase in the amplifier output impedance. Compared to the 50-Ohm load impedance it can be regarded as an open circuit. When only one amplifier is operative, half of its output power will be dissipated by R, the other half being delivered to the load. The remaining active source will still see the correct load impedance, which is a basic requirement in combining linear amplifiers. The resistors (R) should be of noninductive type, and rated for 25% of the total power, unless some type of automatic shutoff system is incorporated. The degree of isolation obtainable depends upon the frequency, and the overall design of the hybrid. Typical

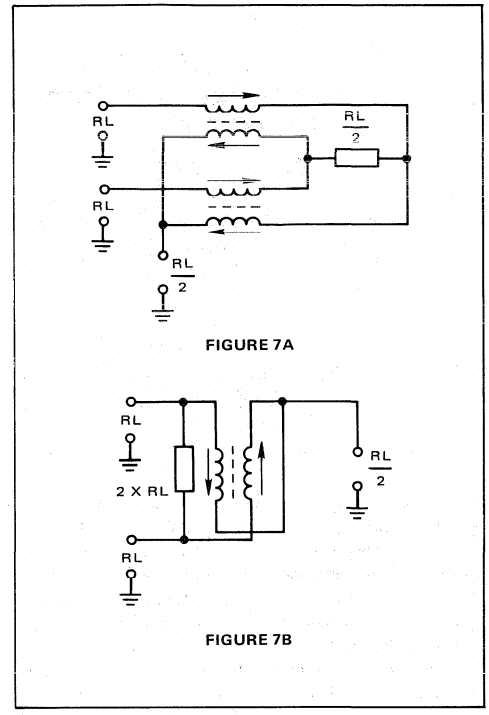


FIGURE 7 — Variations of Basic Hybrid

figures for 2 to 30 MHz operation are 30-40 dB. Figures 8A and B show 4 port "totem pole" structures derived from Figures 7A and 7B. Both can be used with even number of sources only, e.g. 4, 8, 16, etc. For type 8B, it is more practical to employ toroidal multi-turn lines, rather than the straight line alternatives, discussed earlier. The power output with various numbers of inoperative sources can be calculated as follows, if the phase differences are negligible: (Reference 2)

$$P_{out} = \left(\frac{P}{N}\right) N_1$$

where: P = Total power of operative sources
N = Total number of sources
N_1 = Number of operative sources

Assuming the most common situation where one out of four amplifiers will fail, 75% of the total power of the remaining active sources will be delivered to the load.

Another type of multiport hybrid derived from Figure 7A is shown in Figure 9. It has the advantage of being capable of interfacing with an odd number of sources or loads.

In fact, this hybrid can be designed for any number of ports. The optimum values of the balancing resistors will vary according to this and also with the number of ports assumed to be disabled at one time. Two other power combining arrangements are shown in Figures 10 and 11.

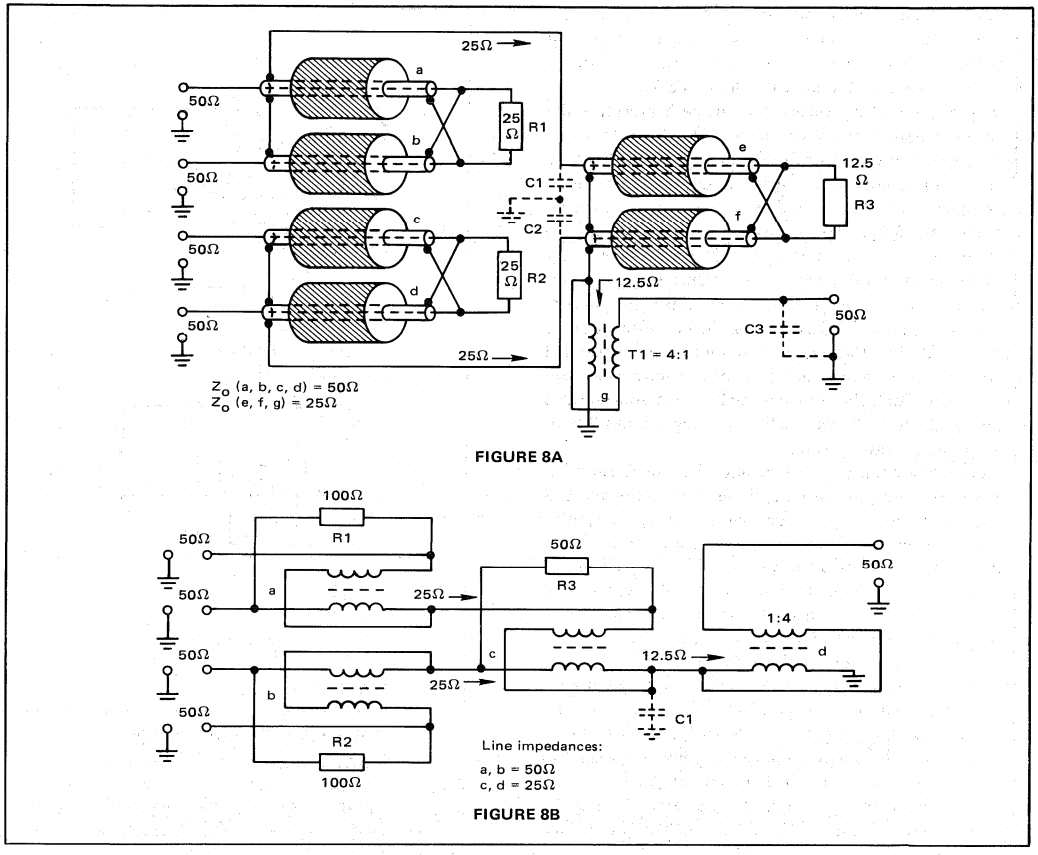


FIGURE 8 – Four Port "Totem Pole" Structure

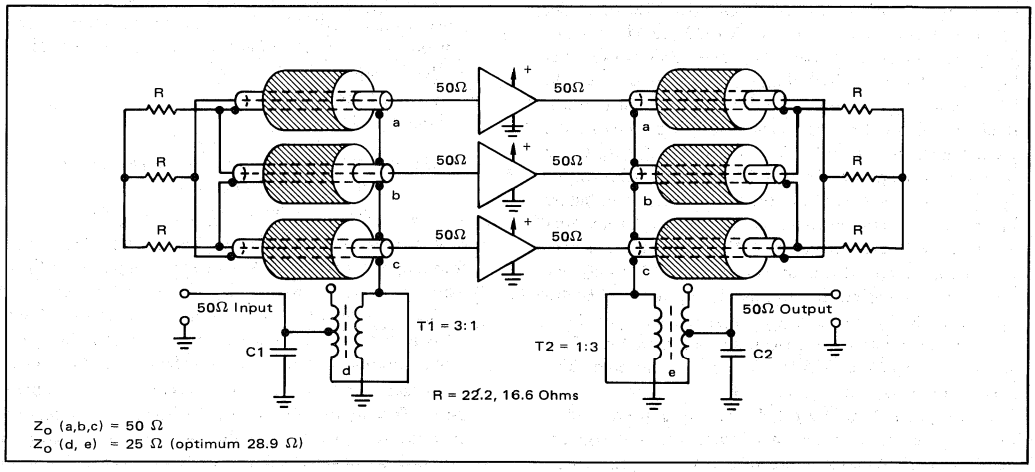
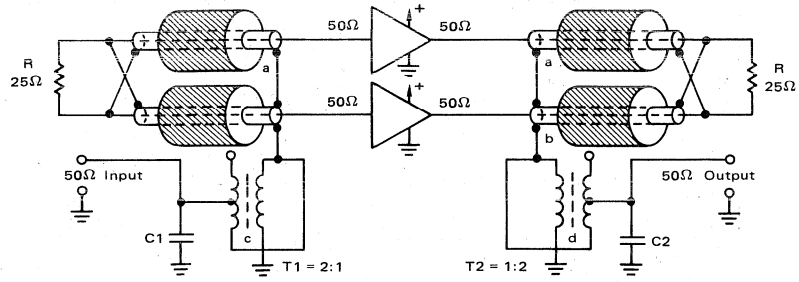


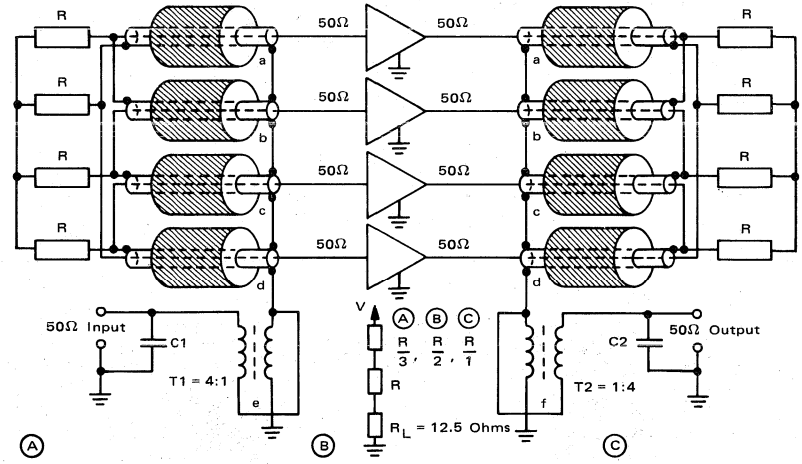
FIGURE 9 – Three-Port Hybrid Arrangement

6



Z_o (a,b) = 50 Ω
Z_o (c,d) = 25 Ω (optimum 35.4 Ω)

FIGURE 10 — Two-Port Hybrid System



Ⓐ
1 PORT INOPERATIVE.
Optimum R = 28.3 Ohms
$P_{out} = (P1+P2+P3)-(P_R + P\frac{R}{3})$

Ⓑ
2 PORTS INOPERATIVE.
Optimum R = 25 Ohms
$P_{out} = (P1+P2)-(P_R+P\frac{R}{2})$

Ⓒ
3 PORTS INOPERATIVE.
Optimum R = 18.75 Ohms
$P_{out} = P1-(P_R+P\frac{R}{1})$

P1, P2, P3 = Power at any operative port, P_R = Power dissipated in R, excluding R_L.
V = RMS voltage at any 50 Ohm point.
(The phase differences are assumed negligible.)

Z_o (a,b,c,d) = 50 Ω
Z_o (e,f) = 25 Ω (optimum)

FIGURE 11 — Four-Port Hybrid System

6

The isolation characteristics of the four-port output combiner were measured, the data being shown in Table 5. The ferrite sleeves are Stackpole 57-0572-27A, and the transmission lines are made of RG-142/U co-axial cable. The input power dividers described here, employ Stackpole 57-1511-24B ferrites, and the co-axial cable is Microdot 250-4012-0000.

TABLE 5 – Isolation Characteristics of Four Port Output Combiner

f (MHz)	Isolation, Port-to-Port (dB)
2.0	27.0-29.4
4.0	34.8-38.2
7.5	39.0-41.2
15	32.1-33.5
20	31.2-33.0
30	31.0-33.4

The input and output matching transformers (T1 – T2) will be somewhat difficult to implement for such impedance ratios as 2:1 and 3:1. One solution is a multi-turn toroid wound with co-axial cable, such as Microdot 260-4118-000. A tap can be made to the braid at any point, but since this is 25-Ohm cable, the Z_O is optimum for a 4:1 impedance ratio only. Lower impedance ratios will normally require increased values for the leakage inductance compensation capacitances (C1 – C2). For power levels above 500-600 W, larger diameter co-axial cable is desirable, and it may be necessary to parallel two higher impedance cables. The required cross sectional area of the toroid can be calculated according to the B_{max} formulas presented in References 4 and 6.

The 2 to 30 MHz linear amplifier (shown in Figure 13) consists of two 300 W modules (8). This combined amplifier can deliver 600 W peak envelope power. The CW power output is limited to approximately 400 W by the heatsink and the output transformer design.

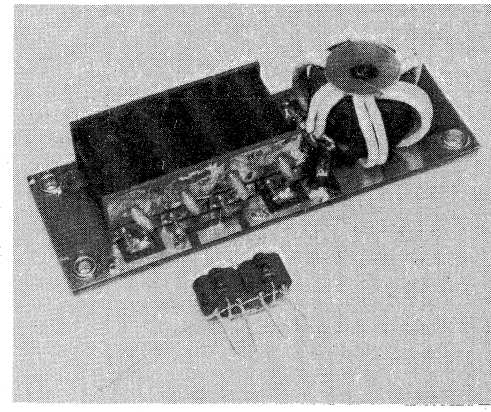


FIGURE 12 – Two-Four Port Hybrids

The one at the lower left is intended for power divider applications with levels to 20 – 30 W. The larger one was designed for amplifier output power combining, and can handle levels to 1 – 1.5 kW. (The balancing resistors are not shown with this unit.)

The power combiner (Figure 13A) and the 2:1 step-up transformer (Figure 13B) can be seen in the upper right corner. The input splitter is located behind the bracket (Figure 13C). The electrical configuration of the hybrids is shown in Figures 7A and 10. Note the loops equalizing the lengths of the co-axial cables in the input and output to assure a minimum phase difference between the two modules.

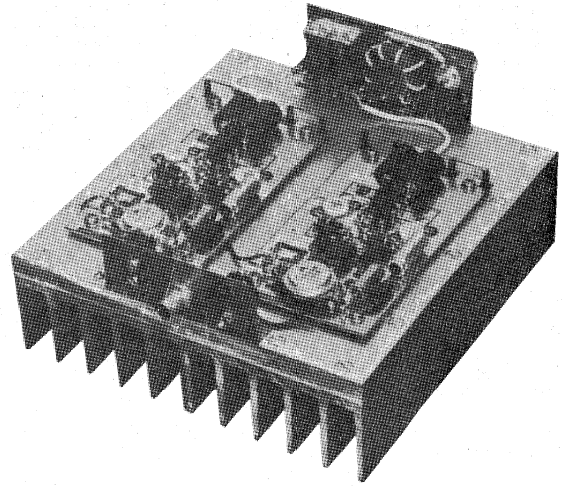


FIGURE 13 – 2 to 30 MHz Linear Amplifier Layout

REFERENCES

1. Ruthroff: Some Broad Band Transformers, *IRE, Volume 47,* August 1957.
2. Pizalis-Couse: Broadband Transformer Design for RF Transistor Amplifiers, *ECOM-2989,* U.S. Army Electronics Command, Fort Monmouth, New Jersey, July 1968.
3. Lewis: *Notes on Low Impedance H.F. Broad Band Transformer Techniques,* Collins Radio Company, November 1964.
4. Hilbers: Design of H. F. Wideband Power Transformers, *Philips Application Information #530.*
5. *Philips Telecommunication Review, Volume 30, No. 4,* pp. 137-146, November 1972.
6. Granberg, H.: *Broadband Linear Power Amplifiers Using Push-Pull Transistors,* AN-593, Motorola Semiconductor Products Inc.
7. Granberg, H.: *Get 300 Watts PEP Linear Across 2 to 30 MHz From This Push-Pull Amplifier,* EB-27, Motorola Semiconductor Products Inc.
8. Lefferson: Twisted Wire Transmission Line, *IEEE Transactions on Parts, Hybrids and Packaging, Vol. PHP-7, No. 4,* December 1971.
9. Krauss-Allen: Designing Toroidal Transformers to Optimize Wideband Performance, *Electronics,* August 1973.

A TWO-STAGE 1 kW SOLID-STATE LINEAR AMPLIFIER

Prepared by
Helge O. Granberg
RF Circuits Engineering

INTRODUCTION

This application note discusses the design of 50 W and 300 W linear amplifiers for the 1.6 to 30 MHz frequency band. Both amplifiers employ push-pull design for low, even harmonic distortion. This harmonic distortion and the 50 Vdc supply voltage make the output impedance matching easier for 50-Ohm interface, and permits the use of efficient 1:1 and 4:1 broadband transformers.

Modern design includes integrated circuit bias regulators and the use of ceramic chip capacitors throughout the RF section, making the units easily mass producible.

Also, four 300 W modules are combined to provide a 1 to 1.2 kW PEP or CW output capability. The driver amplifier increases the total power gain of the system to approximately 34 dB.

Although the transistors employed (MRF427 and MRF428) are 100% tested against 30:1 load mismatches, in case of a slight unbalance, the total dissipation ratings may be well exceeded in a multi-device design. With high drive power available, and the power supply current limit set at much higher levels, it is always possible to have a failure in one of the push-pull modules under certain load mismatch conditions. It is recommended that some type of VSWR based protective circuitry be adapted in the equipment design, and separate dc regulators with appropriate current limits provided for each module.

The MRF428 is a single chip transistor with the die size of 0.140 x 0.248", and rated for a power output of 150 W PEP or CW. The single chip design eliminates the problem of selecting two matched die for balanced power distribution and dissipation. The high total power dissipation rating (320 W) has been achieved by decreasing the thermal resistance between the die and the mount by reducing the thickness of the BeO insulator to 0.04" from the standard 0.062", resulting in $R_{\theta JC}$ as low as 0.5°C/W.

The MRF427 is also a single chip device. Its die size is 0.118 x 0.066", and is rated at 25 W PEP or CW. This being a high voltage unit, the package is larger than normally seen with a transistor of this power level to prevent arcing between the package terminals.

The MRF427 and MRF428 are both emitter-ballasted, which insures an even current sharing between each cell, and thus improving the device ruggedness against load mismatches.

The recommended collector idling currents are 40 mA and 150 mA respectively. Both devices can be operated in Class A, although not specified in the data sheet, providing the power dissipation ratings are not exceeded.

GENERAL DESIGN CONSIDERATIONS

Similar circuit board layouts are employed for the four 300 W building block modules and the preamplifier. A compact design is achieved by using ceramic chip capacitors, of which most can be located on the lower side of the board. The lead lengths are also minimized resulting in smaller parasitic inductances and smaller variations from unit-to-unit.

Loops are provided in the collector current paths to allow monitoring of the individual collector currents with a clip-on current meter, such as the HP-428B. This is the easiest way to check the device balance in a push-pull circuit, and the balance between each module in a system such as this.

The power gain of each module should be within not more than 0.25 dB from each other, with a provision made for an input Pi attenuator to accommodate device pairs with larger gain spreads. The attenuators are not used in this device however, due to selection of eight closely matched devices.

In regards to the performance specifications, the following design goals were set:

Devices: 8 x MRF428 + 2 x MRF427A

Supply Voltage: 40 – 50 V

η, Worst Case: 45% on CW and 35% under two-tone conditions

IMD, d_3: -30 dB Maximum (1 kW PEP, 50 V and 800 W PEP, 40 V)

Power Gain, Total: 30 dB Minimum

Gain Variation: 2.0 – 30 MHz: ±1.5 dB Maximum

Input VSWR: 2.0:1 Maximum

Continuous CW Operation, 1 kW: 50% Duty Cycle, 30-minute periods, with heatsink temperature <75°C.

Load Mismatch Susceptibility: 10:1, any phase angle

Determining the figures above is based on previous performance data obtained in test circuits and broadband amplifiers. Some margin was left for losses and phase errors occurring in the power splitter and combiner.

THE BIAS VOLTAGE SOURCE

Figure 1 shows the bias voltage source employed with each of the 300 W modules and the preamplifier. Its basic components are the integrated circuit voltage regulator MC1723C, the current boost transistor Q3 and the temperature sensing diode D1.

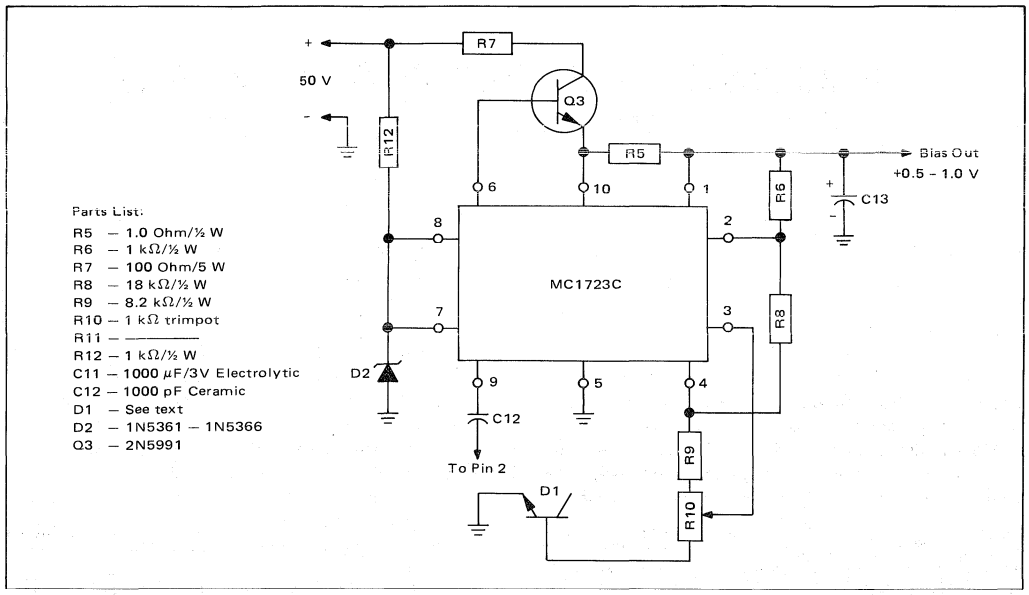


FIGURE 1 – Bias Voltage Source

Although the MC1723C is specified for a minimum V_O of 2 Volts, it can be used at lower levels with relaxed specifications, which are sufficient for this application. Advantages of this type bias source are:

1. Line voltage regulation, which is important if the amplifier is to be operated from various supply voltages.
2. Adjustable current limit.
3. Very low stand-by current drain.

Figure 1 is modified from the circuit shown on the MC1723 data sheet by adding the temperature sensing diode D1 and the voltage adjust element R10. D2 and R12 reduce the supply voltage to a level below 40 V, which is the maximum input voltage of the regulator.

D1 is the base-emitter junction of a 2N5190, in a Case 77 plastic package. The outline dimensions allow its use for one of the circuit board stand-offs, attaching it automatically to the heatsink for temperature tracking.

The temperature compensation has a slight negative coefficient. When the collector idling current is adjusted to 300 mA at 25°C, it will be reduced to 240 – 260 mA at a 60°C heatsink temperature. (-1.15 to -1.7 mA/C°.)

The current limiting resistor R5 sets the limiting to approximately 0.65 A, which is sufficient for devices with a minimum h_{FE} of 17, ($I_B = \frac{I_C}{h_{FE}}$) when the maximum average I_C is 10.9 A. (2 MHz, 50 V, 250 CW.) Typically, the MRF428 h_{FE}'s are in the 30's.

The measured output voltage variations of the bias source (0 – 600 mA) are ±5 to 7 mV, which amounts to a source impedance of approximately 20 milliohms.

THE 300 W AMPLIFIER MODULE

Input Matching

Due to the large emitter periphery of the MRF428, the series base impedance is as low as 0.88, -J.80 Ohm at 30 MHz. In a push-pull circuit a 16:1 input transformer would provide the best impedance match from a 50-Ohm source. This would however, result in a high VSWR at 2 MHz, and would make it difficult to implement the gain correction network design. For this reason a 9:1 transformer, which is more ideal at the lower frequencies, was chosen. This represents a 5.55 Ohm base-to-base soure impedance.

In a Class C push-pull circuit, where the conduction angle is less than 180°, the base-to-base impedance would be about four times the base-to-emitter impedance of one device. In Class A where the collector idling current is approximately half the peak collector current, the conduction angle is 360°, and the base-to-base impedance is twice the input impedance of one transistor. When the forward base bias is applied, the conduction angle increases and the base-to-base impedance decreases rapidly, approaching that of Class A in Class AB.

A center tap, common in push-pull circuits, is not necessary in the input transformer secondary, if the transistors are balanced. (C_{ib}, h_{FE}, V_{BEf}.) The base current return path is through the forward biased base-emitter

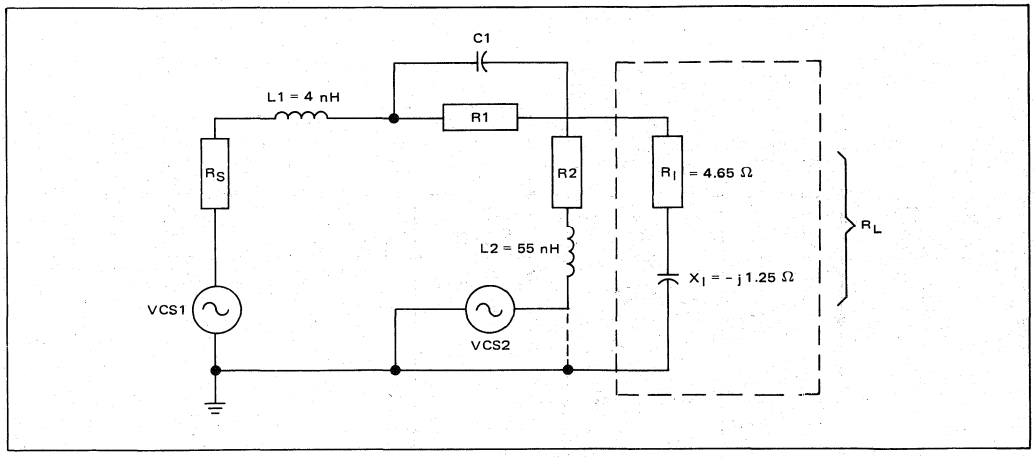


FIGURE 2 – Equivalent Base Input Circuit

junction of the off transistor. This junction acts as a clamping diode, and the power gain is somewhat dependent upon the amount of the bias current. The equivalent input circuit (Figure 2) represents one half of the push-pull circuit, and for calculations R_S equals the total source impedance (R_S') divided by two.

Since a junction transistor is a current amplifier, it should ideally be driven from a current source. In RF applications this would result in excessive loss of power gain. However, input networks can be designed with frequency slopes having some of the current source characteristics at low frequencies, where excess gain is available.

The complex base input characteristics of a transistor would place requirements for a very sophisticated input compensation network for optimum overall performance. The design goal here was to maintain an input VSWR of 2:1 or less and a maximum gain variation of ±1.5 dB from 2 to 30 MHz. Initial calculations indicated that these requirements can be met with a simple RC network in conjunction with negative collector-to-base feedback. Figure 2 shows this network for one device. L1 and L2 represent lead lengths, and their values are fixed. The feedback is provided through R2 and L2. Because the calculations were done without the feedback, this branch is grounded to simulate the operating conditions.

The average power gain variation of the MRF428 from 2 to 30 MHz is 13 dB. Due to phase errors, a large amount of negative feedback in an RF amplifier decreases the linearity, or may result in instabilities. Experience has shown that approximately 5 – 6 dB of feedback can be tolerated without noticeable effects in linearity or stability, depending upon circuit layout. If the amount of feedback is 5 dB, 8 dB will have to be absorbed by the input network at 2 MHz.

Omitting the reactive components, L1, L2, C1, and the phase angle of X_I which have a negligible effect at 2 MHz, a simple L-pad was calculated with R_S = 2.77 Ω, and $R_L = \sqrt{4.65^2 + 1.25^2} = 4.81\ \Omega$.

From the device data sheet we find the G_{PE} at 2 MHz is about 28 dB, indicating 0.24 W at R_L will produce an output power of 150 W, and the required power at R_S = 0.24 W + 8 dB = 1.51 W.

Figuring out currents and voltages in various branches, results in: R1 = 1.67 Ω and R2 = 1.44 Ω.

The calculated values of R1 and R2 along with other known values and the device input data at four frequencies were used to simulate the network in a computer program. An estimated arbitrary value of 4000 pF for C1 was chosen, and VCS2 represents the negative feedback voltage (Figure 2.) The optimization was done in two separate programs for R1, R2, C1 and VCS2 and in several steps. The goals were: a) VCS and R2 for a transducer loss of 13 dB at 2 MHz and minimum loss at 30 MHz. b) R1 and C1 for input VSWR of <1.1:1 and <2:1 respectively. The optimized values were obtained as:

C1 = 5850 pF R2 = 1.3 Ω
R1 = 2.1 Ω VCS2 = 1.5 V

The minimum obtainable transducer loss at 30 MHz was 2.3 dB, which is partly caused by the highest reflected power at this frequency, and can be reduced by "over-compensation" of the input transformer. This indicates that at the higher frequencies, the source impedance (R_S) is effectively decreased, which leaves the input VSWR highest at 15 MHz.

In the practical circuit the value of C1 (and C2) was rounded to the nearest standard, or 5600 pF. For each half cycle of operation R2 and R4 are in series and the value of each should be $\frac{1.3\ \Omega}{2}$ for VCS2 = 1.5 V. Since the voltage across ac and bd = V_{CE}, a turns ratio of 32:1 would be required. It appears that if the feedback voltage

6

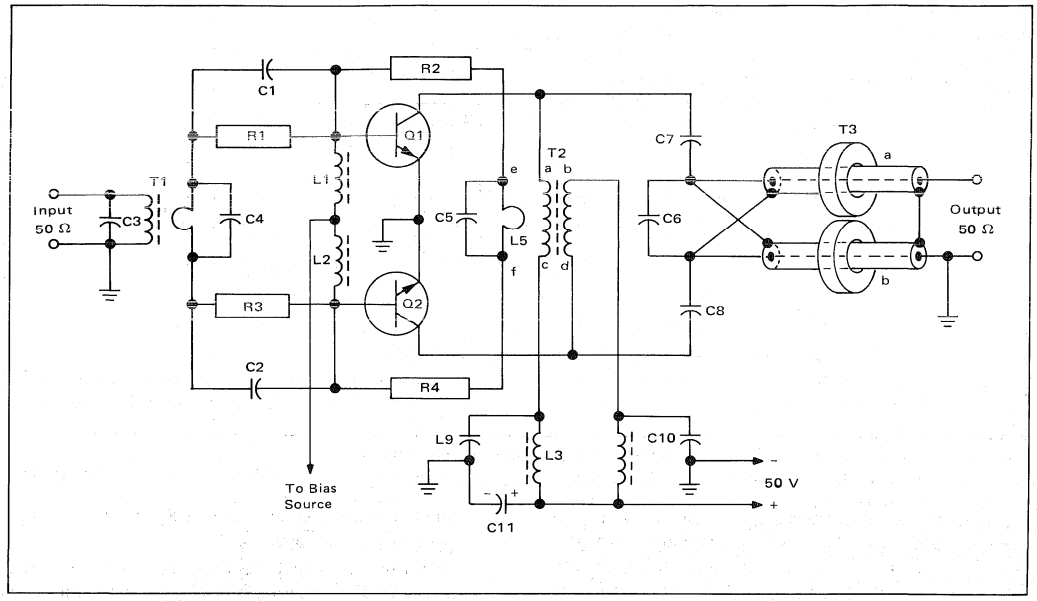


FIGURE 3 –

on the bases remains unchanged, the ratio of the voltage across L5 (VCS2) and R2R4 can be varied with only a small effect to the overall input VSWR. To minimize the resistive losses in the bifilar winding of T2 (Figure 3), the highest practical turns ratio should not be much higher than required for the minimum inductance, which is

$$\frac{4R}{2\pi f} = \frac{50}{12.5} = 4.0\ \mu H.$$

R = Collector-to-Collector Impedance = 12.5 Ω

f = 2 MHz

ac or bd will then be 1.0 μH, which amounts to 5 turns. (See details on T2.) 25% over this represents a 7:1 ratio setting VCS2 to 6.9 V.

In addition to providing a source for the negative feedback, T2 supplies the dc voltage to the collectors as well as functions as a center tap for the output transformer T3.

The currents for each half cycle are in opposite phase in ac and bd, and depending on the coupling factor between the windings, the even harmonic components will see a much lower impedance than the fundamental. The optimum line impedance for ac, bd would equal one half the collector-to-collector impedance, but experiments have shown that increasing this number by a factor of 2-3 affects the 2nd and 4th harmonic amplitudes by only 1 to 2 dB.

Since the minimum gain loss obtainable at 30 MHz with network as in Figure 2, and the modified VCS2 source was about 3.8 dB at 30 MHz, C5 was added with the following in mind: C5 and L5 form a parallel resonant circuit with a Q of approximately 1.5. Its purpose is to increase the shunting impedance across the bases, and to disturb the 180° phase difference between the input signal and the feedback voltage at the higher frequencies. This reduces the gain loss of 3.8 dB, of which 1.4 dB is caused by the feedback at 30 MHz. The amount depends upon the resonant frequency of C5 L5, which should be above the highest operating frequency, to avoid possible instabilities.

When L5 is 45 nH, and the resonance is calculated for 35 MHz, the value of C5 becomes 460 pF, which can be rounded to the closest standard, or 470 pF. The phase shift at 30 MHz is:

$$\text{Tan}^{-1}\left[\frac{2\pi f L}{R\left(1-\frac{f^2}{f_o{}^2}\right)}\right] = \text{Tan}^{-1}\left[\frac{6.28 \times 30 \times 0.045}{6.8\left(1-\frac{900}{1225}\right)}\right]$$

$$= \text{Tan}^{-1}\left(\frac{8.48}{1.80}\right) = 78.0^{o}$$

The impedance is: $\frac{R}{\cos\theta} = \frac{6.8}{\cos 78^{o}} = 32.7\ \Omega$

At 2 MHz the numbers are respectively 4.76° and 6.83 Ω.

The 1.4 dB feedback means that the feedback voltage is 16% of the input voltage at the bases. By the aid of

vectors, we can calculate that the 78° phase shift and the increased impedance reduces this to 4%, which amounts to 0.35 dB. These numbers were verified in another computer program with VCS2 = 6.9 V, and including C5. New values for R1 and R2 were obtained as 1.95 Ω and 6.8 Ω respectively, and other data as shown in Table 1.

The VSWR was calculated as

$\frac{Z1 - Z2}{Z1 + Z2}$ where:

Z1 = Impedance at transformer secondary.

TABLE1:

Frequency MHz	Input VSWR	Input Impedance Real	Input Impedance Reactive	Attenuation dB
2.0	1.07	2.79	-0.201	13.00
4.0	1.16	2.66	-0.393	12.07
7.5	1.33	2.35	-0.615	10.42
15	1.68	1.77	-0.611	7.40
20	1.82	1.57	-0.431	5.90
30	1.74	1.62	-0.21	2.70

Although omitted from the preliminary calculations, the 2 x 5 nH inductances, comprising of lead length, were included in this program.

The input transformer is a 9:1 type, and uses a television antenna balun type ferrite core, made of high permeability material. The low impedance winding consists of one turn of 1/8" copper braid. The sections going through the openings in the ferrite core are rounded to resemble two pieces of tubing electrically. The primary consists of AWG #22 TFE insulated wire, threaded through the rounded sections of braid, placing the primary and secondary leads in opposite ends of the core. (4) (5). The saturation flux density is about 60 gauss which is well below the limits for this core. For calculation procedures, see discussion about the output transformer.

This type physical arrangement provides a tight coupling, reducing the amount of leakage flux at high frequencies. The wire gauge, insulation thickness, and number of strands have a minimal effect in the performance except at very high impedance ratios, such as 25:1 and up. The transformer configuration is shown in Figure 4. By using a vector impedance meter, the values for C3 and C4 were measured to give a reasonable input match at 30 MHz, (Z_{in} = 1.62 - j 0.21 x 2 = 3.24 - j 0.42) with the smallest possible phase angle.

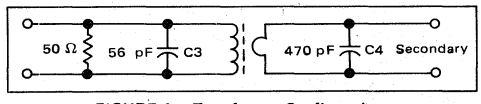


FIGURE 4 – Transformer Configuration

When the high impedance side was terminated into 50 Ω, the following readings were obtained at the secondary:

Z2 = Input impedance of compensation network x 2 (R_S in Figures 2 and 3) as in computer data presented ahead.

The effect of the lower VSWR to the power loss in the input network can be calculated as follows:

$$10 \text{ Log} \left[\frac{\left(1 - \left(\frac{S1 - 1}{S1 + 1}\right)^2\right)}{\left(1 - \left(\frac{S2 - 1}{S2 + 1}\right)^2\right)} \right]$$

where:
S1 = VSWR 1 (Lower)
S2 = VSWR 2 (Higher)

$$\text{which at 30 MHz} = 10 \text{ Log} \frac{\left(1 - \left(\frac{1.11 - 1}{1.11 + 1}\right)^2\right)}{\left(1 - \left(\frac{1.74 - 1}{1.74 + 1}\right)^2\right)}$$

$$= 10 \text{ Log} \left(\frac{0.997}{0.927}\right) = 0.32 \text{ dB}, 2.7 - 0.32 = 2.38 \text{ dB}$$

These figures for other frequencies are presented with the data below. Later, some practical experiments were done with moving the resonance of C5 L5 lower, to find out if instabilities would occur in a practical circuit. When the resonance was equal to the test frequency, slight breakup was noticed in the peaks of a two-tone pattern. It was then decided to adjust the resonance to 31 MHz, where C5 = 560 pF, and the phase angle at 30 MHz increases to 87°. The transducer loss is further reduced by about 0.2 dB.

Several types of output transformer configurations were considered. The 12.5 Ω collector-to-collector im-

TABLE 2:

Frequency MHz	R_S Ohms	X_S Ohms	VSWR	Attenuation dB
2.0	5.59	+0.095	1.05	12.99
4.0	5.55	+0.057	1.15	12.06
7.5	5.50	+0.046	1.32	10.40
15	4.90	+0.25	1.48	7.28
20	4.32	+0.55	1.38	5.63
30	3.43	+0.73	1.11	2.38

(Above readings with transformer and compensation network.)

6

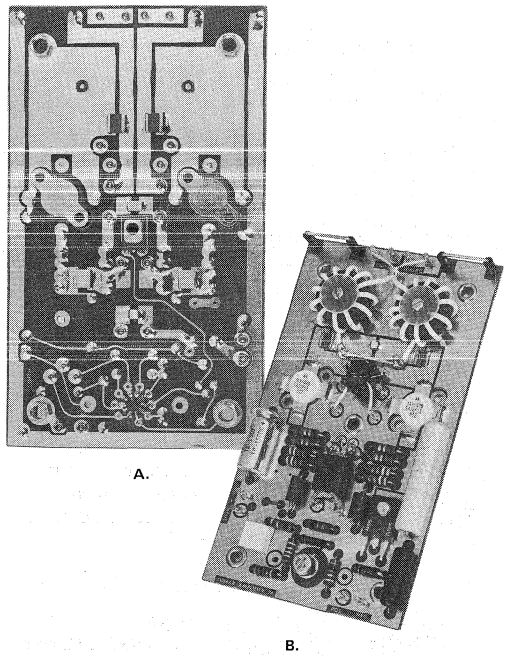


FIGURE 5 – Bottom and Top of the 300 W Module Circuit Board

pedance estimated earlier, would require a 4:1 transformer for a 50 Ω output. The type used here as the input transformer exhibits good broad band characteristics with a convenient physical design. However, according to the low frequency minimum inductance formula presented earlier in connection with T2, the initial permeability required would be nearly 3000, with the largest standard core size available. High permeability ferrites are almost exclusively of Nickel-Manganese composition, and are lossy at radio frequencies. Although their Curie points are higher than those of lower permeability Nickel-Zinc ferrites, the core losses would degrade the amplifier performance. With the core losses being a function of the power level, these rules can sometimes be disregarded in low power applications.

A coaxial cable version was adapted for this design, since the transmission line type transformers are theoretically ideal for RF applications, especially in the 1:4 impedance ratio. A balanced to unbalanced function would normally require three separate transmission lines including a balun (5) (6). It appears that the third line can be omitted, if lines a and b (Figure 3) are wound on separate magnetic cores, and the physical length of the lines is sufficient to provide the necessary isolation between the collectors and the load. In accordance to formulas in (7), the minimum line length required at 2 MHz, employing Stackpole 57-9074 or equivalent ferrite toroids is 4.2", and the maximum permissible line length at 30 MHz would be approximately 20". The 4.2" amounts to four turns on the toroid, and measures 1.0 μH, which in series with the second line is sufficient for 2 MHz. Increasing the minimum required line length by a factor of 4 is still within the calculated limits, and in practical measurements the isolation has been found to be over 30 dB across the band. The main advantage with this arrangement is a simplified electrical and physical lay-out.

The maximum flux density of the toroids is approximately 200 gauss (3), and the number of turns has been increased beyond the point where the flux density of the magnetic core is the power limiting factor.

The 1:4 output transformer is not the optimum in this case, but it is the closest practical at these power levels. The optimum power output at 50 V supply voltage and 50 Ω load is:

$V_{RMS} = 4 \times (V_{CC} - V_{CE(sat)} \times 0.707) = 135.75$ V, when $V_{CE(sat)} = 2$ V

$$I = \frac{135.75}{50} = 2.715 \text{ A}, P_{out} = 2.715 \times 135.75 = 368.5 \text{ W}$$

The optimum V_{CC} at $P_{out} = 300$ W would be:

$$V_{CC} = V_{CE(sat)} + (\sqrt{R_{in} \times 2 P_{out}}) = 2 + (\sqrt{6.25 \times 300}) = 45.3 \text{ V}$$

The above indicates that the amplifier sees a lower load line, and the collector efficiency will be lowered by 1-2%. The linearity at high power levels is not affected, if the device h_{FE} is maintained at the increased collector currents. The linearity at low power levels may be slightly decreased due to the larger mismatch of the output circuit.

The required characteristic line impedance (a and b, Figure 3) for a 1:4 impedance transformer is: $\sqrt{R_{in} R_L} = \sqrt{12.5 \times 50} = 25$ Ω, enables the use of standard miniature 25 Ω coaxial cable (i.e., Microdot 260-4118-000) for the transmission lines. The losses in this particular cable at 30 MHz are 0.03 dB/ft. With a total line length of 2 x 16.8" (2 x 4 x 4.2"), the loss becomes 0.084 dB, or

$$300 - \left(\frac{300}{10 \text{ antilog } 0.084 \text{ dB}}\right) = 5.74 \text{ W}.$$

For the ferrite material employed, Stackpole grade #11 (or equivalent Indiana General Q1) the manufacturers data is insufficient for accurate core loss calculations (6). The B_H curves indicate that 100-150 gauss is well in the linear region.

The toroids measure 0.87" x 0.54" x 0.25", and the 16.8" line length figured above, totals to 16 turns if tightly wound, or 12-14 turns if loosely wound. The flux density can then be calculated as:

$$B_{max} = \frac{V_{max} \times 102}{2 \pi f n A}$$

where: f = Frequency in MHz
n = Total number of turns.
A = Cross sectional area of the toroid in cm^2.
V = Peak voltage across the 50 Ω load,

$$\sqrt{\left(\frac{300}{50}\right)\left(\frac{50}{0.707}\right)} = 173 \text{ V}$$

$$B_{max} \text{ (for each toroid)} = \frac{86.5 \times 10^2}{6.28 \times 2 \times 28 \times .25} = 98.3 \text{ gauss}$$

Practical measurements showed the core losses to be negligible compared to the line losses at 2 MHz and 30 MHz. However, the losses increase as the square of B_{max} at low frequencies.

With the amount of HF compensation dependent upon circuit layout and the exact transformer construction, no calculations were made on this aspect for the input (or output) transformers. C3, C4, and C6 were selected by employing adjustable capacitors on a prototype whose values were then measured.

A photo of the circuit board is shown in Figure 5, A-bottom and B-top. The performance data of the 300 W module can be seen in Figure 6.

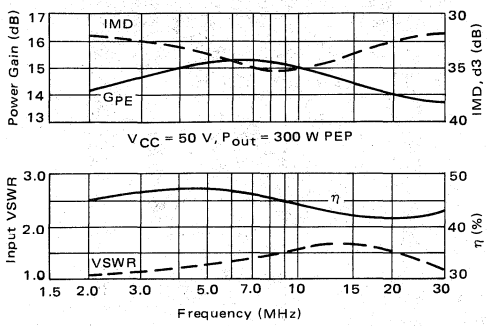


FIGURE 6 – IMD, Power Gain, Input VSWR and Efficiency versus Frequency of a 300 W Module

THE DRIVER AMPLIFIER

The driver uses a pair of MRF427 devices, and the same circuit board layout as the power amplifier, with the exception of the type of the output transformer.

The input transformer is equal to what is used with the power amplifier, but has a 4:1 impedance ratio. The required minimum inductance in the one turn secondary (Figures 3 and 4) being considerably higher in this case,

$$\frac{4R}{2\pi f} = \frac{4 \times 12.5}{12.5} = 4\ \mu H$$

the A_L product of the core is barely sufficient. The measured inductances between a number of cores range 3.8 - 4.1 μH.

This formula also applies to the output transformer, which is a 1:1 balun. The required minimum inductance at 2 MHz is 16 μH, amounting to 11 turns on a Ferroxcube 2616P-A100-4C4 pot core, which was preferred over a toroid because of ease of mounting and other physical features. Although twisted wire line would be good at this power level, the transformer was wound with RG-196 coaxial cable, which is also used later for module-driver interconnections.

The required worst case driver output is 4 x 12 W = 48 W. The optimum P_{out} with the 1:1 output transformer is

$$\frac{V_{RMS}}{50} \times V_{RMS} = \frac{67.7}{50} \times 67.7 = 92\ W.$$

The MRF 427 is specified for a 25 W power output. Having a good h_{FE} versus I_C linearity, the 1 to 2 load mismatch has an effect of 2-3 dB in the IMD at the 10% power level, and the reduced efficiency in the driver is insignificant regarding the total supply current in the system.

The component values for the base input network and the feedback were established with the aid of a computer, and information on the device data sheet, as described earlier with the 300 W module. The HF compensation was done in a similar manner as well. Neither amplifier employs LF compensation. C7 and C8 are dc blocking capacitors, and their value is not critical.

In T2 (Figure 7), b and c represent the RF center tap, but are separated in both designs – partly because

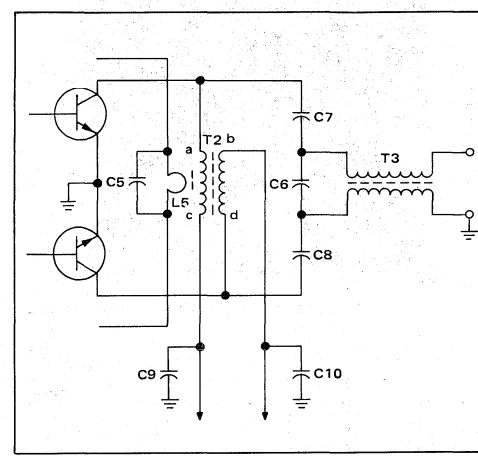


FIGURE 7

of circuit lay-out convenience and partly for stabilization purposes.

The test data of the driver is presented later along with the final test results.

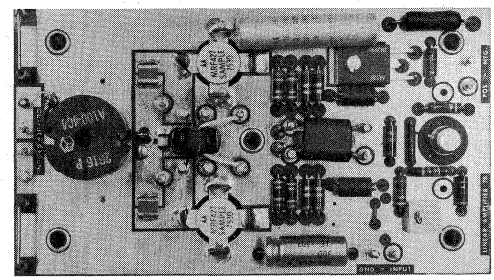


FIGURE 8 – Driver Amplifier Board Layout

COMBINING FOUR 300 W POWER MODULES

The Input Power Divider

The purpose of the power divider is to divide the input power into four equal sources, providing an amount of isolation between each. The outputs are designed for 50 Ω impedance, which sets the common input at 12.5 Ω. This requires an additional 4:1 step down transformer to provide a 50 Ω load for the driver amplifier. Another requirement is a 0° phase shift between the input and the 50 Ω outputs, which can be accomplished with 1:1 balun transformers. (a, b, c and d in Figure 10.) For im-

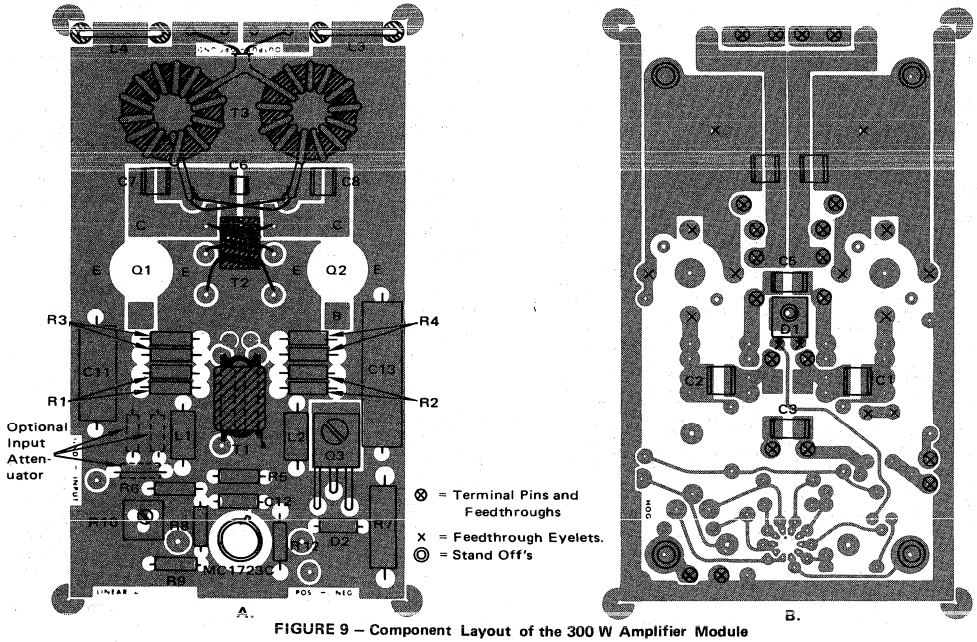


FIGURE 9 – Component Layout of the 300 W Amplifier Module

PARTS LIST
(Power Module and Driver Amplifier)

	Power Module	Driver Amplifier
C1, C2	5600 pF	3300 pF
C3	56 pF	39 pF
C4	470 pF	Not Used
C5	560 pF	470 pF
C6	75 pF	51 pF
C7, C8	0.1 μF	0.1 μF
C9, C10	0.33 μF	0.33 μF
C11	10 μF/150 V	10 μF/150 V
R1, R2	2 x 3.9 Ω/½ W in parallel	2 x 7.5 Ω/½ W in parallel
R3, R4	2 x 6.8 Ω/½ W in parallel	2 x 18 Ω/½ W in parallel
L1, L2	Ferroxcube VK200 19/4B ferrite choke	Ferroxcube VK 200 19/4B ferrite choke
L3, L4	6 ferrite beads each, Ferroxcube 56 590 65/3B	6 ferrite beads each, Ferroxcube 56 590 65/3B
	All capacitors, except C11, are ceramic chips. Values over 100 pF are Union Carbide type 1225 or 1813 or Varadyne size 18 or 14. Others ATC Type B.	
T1	9:1 type, see text.	4:1 type, see text.
	(Ferrite cores for both: Stackpole 57-1845-24B or Fair-Rite Products 287300201 or equivalent.)	
T2	7 turns of bifilar or loosely twisted wires. (AWG #20.) Ferrite cores for both: Stackpole 57-9322, Indiana General F627-8Q1 or equivalent.	
T3	14 turns of Microdot 260-4118-00 25 Ω miniature coaxial cable wound on each toroid. (Stackpole 57-9074, Indiana General F624-19Q1 or equivalent.)	11 turns of RG-196, 50 Ω miniature coaxial cable wound on a bobbin of a Ferroxcube 2616P-A100-4C4 pot core.

proved low frequency isolation characteristics the line impedance must be increased for the parallel currents. This can be done, without affecting the physical length of the line, by loading the line with magnetic material. In this type transformer, the currents cancel, making it possible to employ high permeability ferrite and a relatively short physical length for the transmission lines. In an absolutely balanced condition, no power will be dissipated in the magnetic cores, and the line losses are reduced. The minimum required inductance for each line can be calculated as shown for the driver amplifier output transformer, which gives a number of 16 μH minimum at 2 MHz. A low inductance value degrades the isolation characteristics between the 50 Ω output ports, to maintain a low VSWR in case of a change in the input impedance of one or more of the power modules. However, because of the base compensation networks, the power splitter will never be subjected to a completely open or shorted load.

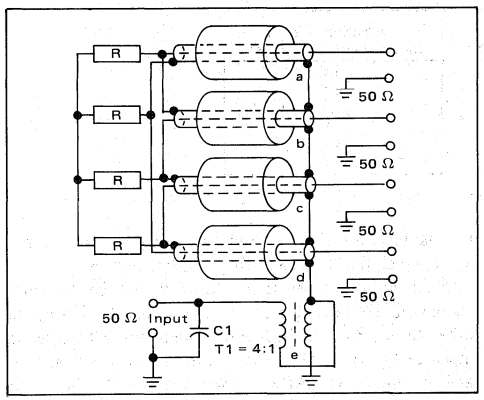


FIGURE 10 – Four Port Power Divider

The purpose of the balancing resistors (R) is to dissipate any excess power, if the VSWR increases. Their optimum values, which are equal, are determined by the number of 50 Ω sources assumed unbalanced at one time, and the resistor values are calculated accordingly.

Examining the currents with one load open, it can be seen that the excess power is dissipated in one resistor in series with three parallel resistors. Their total value is 50 - 12.5 = 37.5 Ω. Similarly, if two loads are open, the current flows through one resistor in series with two parallel resistors, totaling 37.5 Ω again. This situation is illustrated in Figure 11.

Except for a two port power divider [5], the resistor values can be calculated for odd or even number systems as:

$$R = \left(\frac{R_L - R_{in}}{n + 1}\right) n \text{ where:}$$

R_L = Impedance of the output ports, 50 Ω.
R_{in} = Impedance of the input port, 12.5 Ω.
n = Number of output ports properly terminated.

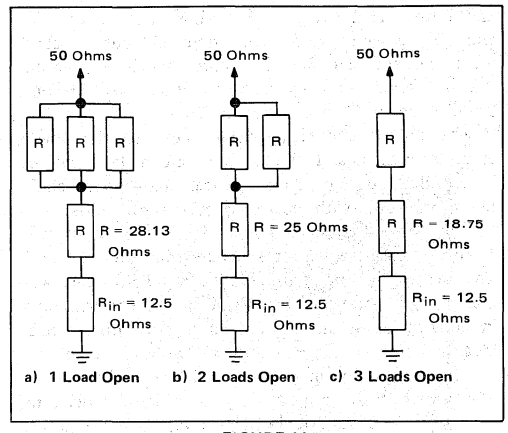


FIGURE 11

Although these resistor values are not critical in the input divider, the formula also applies to the output power combiner, where mismatches have a larger effect in the total power output and linearity.

The practical power divider employs large ferrite beads (Fair-Rite Products 2673000801 or Stackpole 57-1511-24B or equivalent) over a 1.2 inch piece of RG-196 coaxial cable. The arrangement is shown in Figure 10. Both above ferrite materials have a μr of about 2500, and the inductance for one turn is in excess of 10 μH.

The step-down transformer (T1, Figure 10) is wound on a Stackpole 57-9322-11 toroid with 25 Ω miniature coaxial cable. (Microdot 260-4118-000 or equivalent.) Seven turns will give a minimum inductance of 4/16 μH, required at 2 MHz.

For the preamplifier interface, C1 could be omitted in order to achieve the lowest input VSWR.

The structure is mounted between two phenolic terminal strips as can be seen in the foreground of Figure 14, providing a sufficient number of tie points for the coaxial cable connections.

THE OUTPUT COMBINER

The operation of the output combiner is reversed from that of the input power divider. In this application we have four -50 Ω inputs and one 12.5 Ω output, which is transformed to 50 Ω by a 1:4 impedance ratio transformer.

An arrangement similar to the input power divider is employed in the combiner. The baluns consist of straight pieces of coaxial cable loaded by a sleeve of magnetic material (ferrite). The line length is determined by the physical dimensions of the ferrite sleeves. The μr versus cross sectional area should be calculated or measured to give sufficient loading inductance.

Straight line baluns as these have the advantage over multiturn toroidal types in introducing a smaller possibility for phase errors, due to the smaller length of the line. The largest possible phase errors occur in the input

and output connecting cables, whose lengths are 18" and 10" respectively. All four input and output cables must be of equal length within approximately ¼", and the excess in some, caused by the asymmetrical system layout, can be coiled or formed into loops.

The output connecting cables between the power amplifier outputs and the combiner are made of low loss RG-142B/U coaxial cable, that can adequately handle the 300 W power with the average current of 2.45 A.

The balun transmission lines are also made of RG-142B/U coaxial cable, with an outer diameter of 0.20". The line length is not critical as it is well below the maximum length permitted for 30 MHz (7). The minimum inductance, as in the input divider, is 16 μH per line. Measurements were made between two port combiners, one having the line inductance of 17 μH (7 Ferroxcube 768 series 3E2A toroids) and the other 4.2 μH (one Stackpole 57-0572-27A ferrite sleeve). The results are shown in Table 3.

The power output with various numbers of disabled sources, referring to Figures 11 and 12 can be calculated as:

$$Pn - P_R + \frac{P_R}{n}$$

where: n = Number of Operative Sources.
Pn = Total Power of Operative Sources.
P_R = Power Dissipated in Balancing Resistors.

For one disabled source:

$$P_R = 250\left(\frac{28.13}{50}\right) = 140.65,$$

$$P_{out} = (250 \times 3) - \left(140.65 + \frac{140.65}{3}\right) =$$

750 - 187.5 = 562.5 W

This is assuming that the phase errors between the active sources are negligible. Otherwise the formula in (7) can be adapted, but if the errors between the active sources are unequal, the situation will get rather complex.

f MHz	Isolation dB (Line Inductance 17 μH)	Isolation dB Line Inductance 4.2 μH)
2.0	40.2	29.1
4.0	40.0	38.3
7.5	39.6	39.1
15	37.5	37.8
20	35.8	36.2
30	33.4	33.5

TABLE 3:

The main difference is at 2 MHz – and it was decided that the 29 dB of isolation is sufficient, as the high frequency isolation in either case is not much better. The 3E2A and other similar materials are rather lossy at RF, and with their low Curie points, would present a danger of overheating in case of a source unbalance.

Figure 12 shows the electrical design of the four-port power combiner.

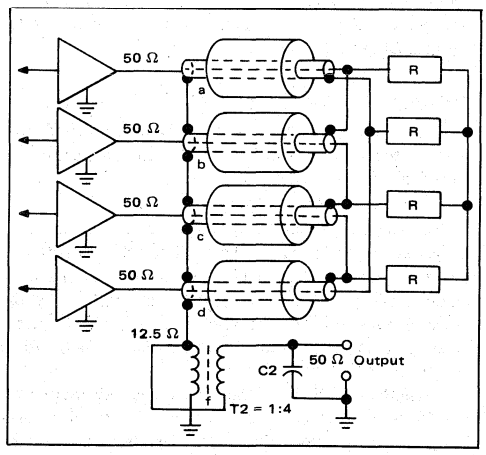


FIGURE 12 – Four Port Output Combiner

From above we see that 140.65 W will be dissipated by one of the balancing resistors and only 15.6 W by the other three. For this high power dissipation the resistors must be the type which can be mounted to a heat sink, and noninductive. After experiments with the "non-inductive" wirewound resistors which exhibited excess inductance at 30 MHz and were bulky with 50 and 100 W ratings, thin film terminations were specially fabricated in-house for this application.* These terminations are deposited on a BeO wafer, which is attached to a copper flange. They are rated for 50 W continuous power, but can be operated at 100 or even 150 W for nonextended periods if the flange temperature is kept moderately low. The balancing resistors can be seen on the upper side of the combiner, which is shown in the foreground of Figure 15.

The purpose of the step-up transformer T2, (Figure 12) is to transform the 12.5 Ω impedance from the combiner up to 50 Ω. It is a standard 1:4 unbalanced-to-unbalanced transmission line type transformer, (6, 7, 8) in which the line is made of two RG-188 coaxial cables connected in parallel in the manner as shown in Figure 13.

Normally the loss in RG-188 at 30 MHz is 0.08 dB/foot. In this connection arrangement, the currents in both directions are carried by the braid in parallel with the

*Similar attenuators and terminations are available from Solitron, EMC Technology, Inc., and other manufacturers of microwave components.

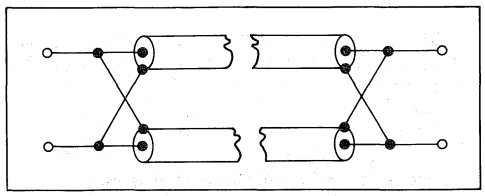


FIGURE 13

inner conductor and the power loss is reduced to approximately 0.025 dB/foot. The impedance becomes 25 Ω, and depending on how close the cables are to each other physically, it can be as low as 22 Ω. The minimum line inductance can be calculated as shown before, and is 16 μH for the 50 Ω side. This inductance is achieved by winding several turns of the dual cable line on a magnetic core. In contrast to the balun transformers in the combiner, the line currents do not cancel and the magnetic core must handle the full power, and must be made of lower loss material. The form of a toroid was figured to require the shortest line length for a specific inductance, and out of the standard sizes, two stacked units resulted in a shorter line length than a single larger one with similar cross sectional area.

Six turns on two Indiana General F626-12-Q1 toroids give 4.8 and 23 μH for the secondary; the line length being 16 inches.

In continuous operation the core temperature was measured as 95-90°C. This resulted in a decision to change the core material to Q2, which exhibits about 70% lower losses at 30 MHz. The permeability is also lower (35), and with the same number of turns gives only 13 μH.

The line length could not be increased according to (7), and the measurements indicated no difference in operation at 2 MHz, so the Q2 toroids with the low inductance were considered permanent.

The maximum flux density of the toroids is calculated as shown before:

$$B_{max} = \frac{V_{max} \times 10^2}{2\pi f \eta A} \text{ gauss, where:}$$

V = Peak voltage across the secondary, (50 point) 316.2 V
f = Frequency in MHz (2.0)
η = Number of turns at the 50 Ω point. (12)
A = Core cross sectional area (1.21 cm^2)

$$B_{max} = \frac{316.2 \times 10^2}{6.28 \times 2 \times 12 \times 1.21} = 260 \text{ gauss}$$

From the BH curves we can see that the linear portion extends to 800-1000 gauss, and the saturation occurs at over 3000 gauss. Comparable materials are Stackpole grade 14 and Fair-rite products 63.

The core losses are minimal compared to the line losses, which for the 16" length amount to 0.035 dB or 0.81%.

As in the input transformer, the HF compensation (C2) was not required. The lay-out of the combiner and T2 is

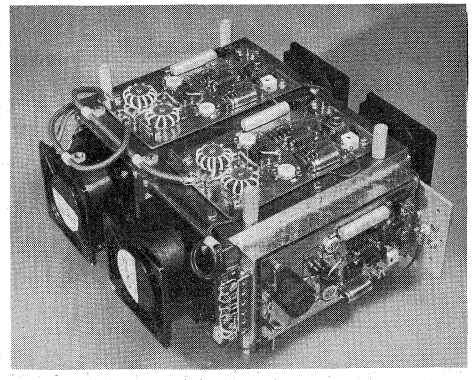


FIGURE 14 – 1 kW Linear Amplifier showing the input power divider in the foreground, to the right is the preamplifier. Two of the four 300 W modules can be seen on the upper side of the structure. The other two modules are shown in Figure 15.

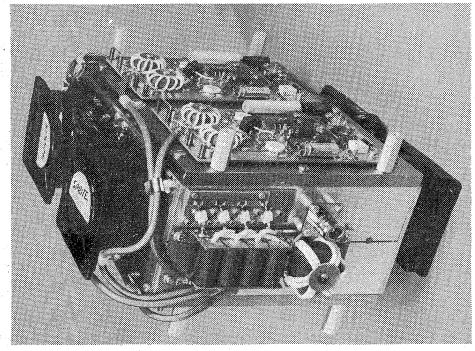


FIGURE 15 – 1 kW Linear Amplifier showing the output combiner in the foreground, to the right is the 1:4 stepup transformer. The four balancing resistors, mounted to the heat sink, can be seen directly above the combining network.

such that minimum lead lengths are obtained, and the structure is mounted on a PC board having feedthrough eyelets to a continuous ground plane on its lower side.

MEASUREMENTS

Six 300 W modules were built using matched pair production MRF428's. The maximum gain distribution was 0.9 dB, and in the four units selected for the amplifier, the gain varied from 13.7 to 14.1 dB at 30 MHz, so it was not necessary to utilize the option of the input attenuators.

Figure 16 shows the test set-up arrangement employed for testing the modules and the combined amplifier.

The heatsink design was not optimized as it was felt to be outside the scope of this report; concentration was made in the electrical design. However, it was calculated to be sufficient for short period testing under two-tone or CW conditions at full power. The heatsink consists of

6

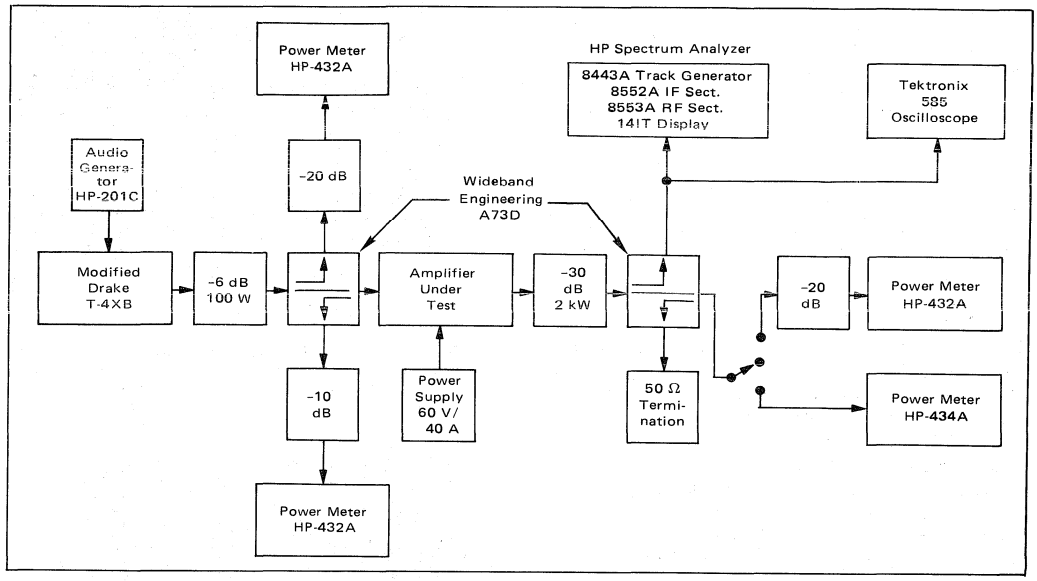


FIGURE 16 — For two tone operation, a signal from an external audio oscillator is added to a signal from the T-4XB built-in oscillator, which has been adjusted to 800 Hz.

During single tone testing, the external oscillator (1200 Hz) is switched off. A calorimeter wattmeter in the output can be used to calibrate the HP-432A's at frequencies below ≈10 MHz, where their response roll-off begins.

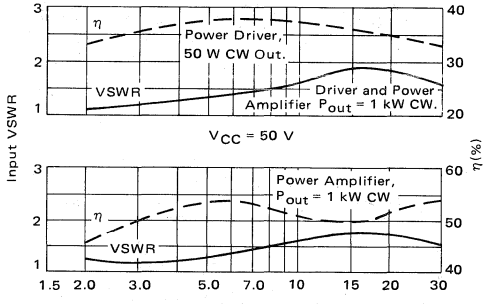


FIGURE 17 — VSWR and Efficiency versus Frequency

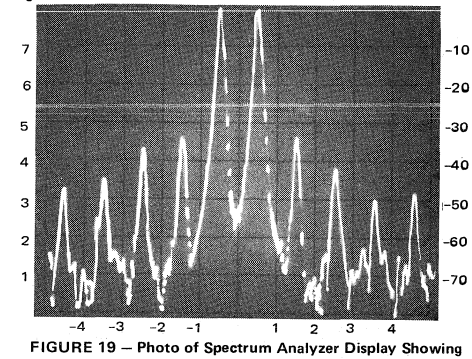


FIGURE 19 — Photo of Spectrum Analyzer Display Showing the IMD Products to the 9th Order. Power Output = 1 kW at 30 MHz (50 V).

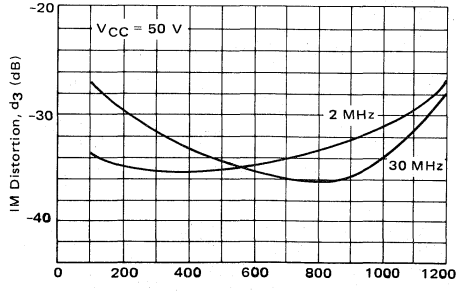


FIGURE 18 — IMD versus Power Output

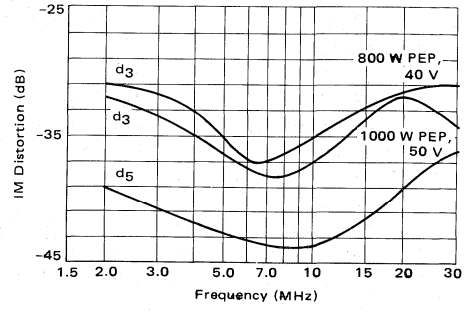


FIGURE 20 — IMD versus Frequency

four 9" lengths of Thermalloy 6151 extrusion, each having a free air thermal resistance of 0.7°C/W. They are bolted in pairs to two 9" x 8½" x 3/8" copper plates, to which the four power modules are mounted. Assuming a coefficient of 0.85 between two parallel extrusions, a total thermal resistance of 0.4°C/W is realized. Two of these dual extrusions are mounted back-to-back to provide

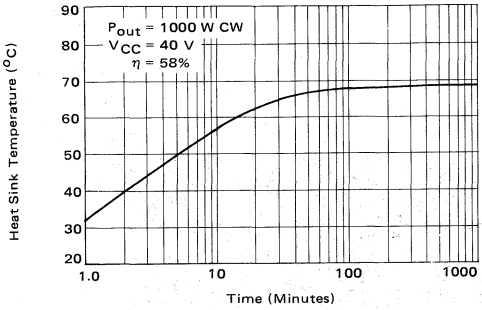


FIGURE 21 – Heat Sink Temperature versus Time

a channel for the air flow from four Rotron SP2A2 4" fans. Two are mounted in each end of the heatsink, and the four fans operating in the same direction provide an air flow of approximately 150 CFM.

The third order harmonic is 14 dB below the fundamental at certain frequencies, as can be seen in Figure 22. This number is typical in a four octave amplifier, and it is obvious that some type of output filter is required when it is used for communications purposes.

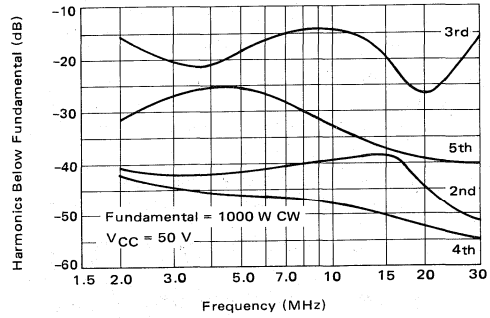


FIGURE 22 – Output Harmonic Contents versus Frequency

The 10:1 load mismatch was simulated with 34 feet of RG-58 coaxial cable, which has an attenuation of approximately 0.9 dB at 30 MHz, representing 1.8 dB return loss. The coaxial was terminated into an LC network consisting of a 2 x 15 – 125 pF variable capacitor and two inductors as shown in Figure 23.

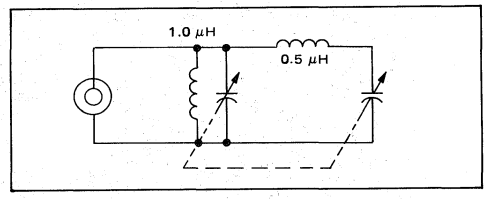
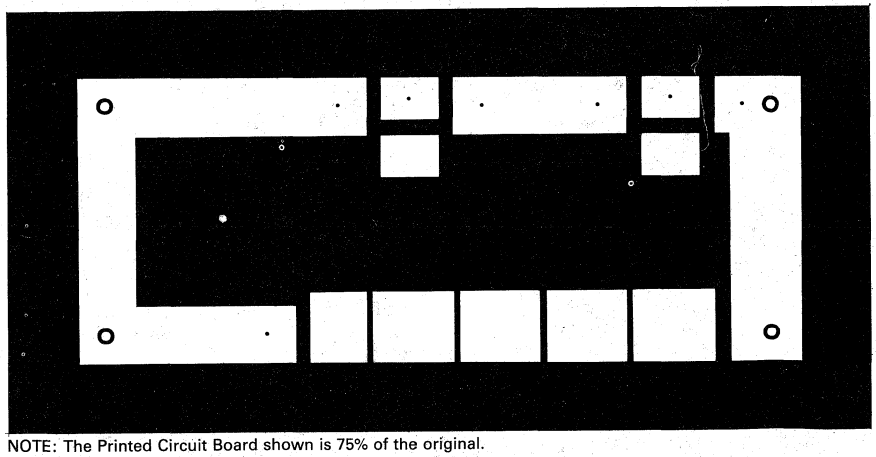


FIGURE 23 – Load Mismatch Test Circuit



NOTE: The Printed Circuit Board shown is 75% of the original.

FIGURE 24 – Circuit Board Layout of the Power Combiner Assembly

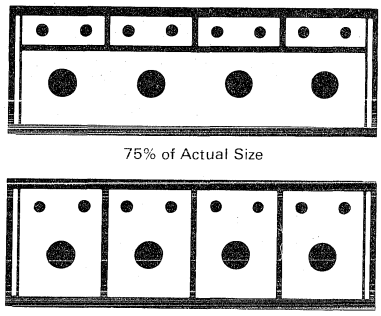
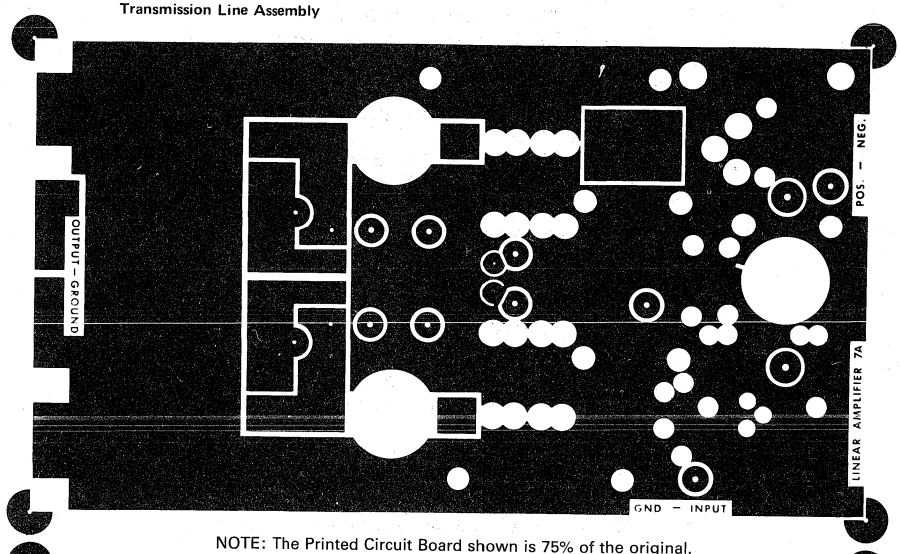


FIGURE 25 – Board Layout of the Power Combiner Transmission Line Assembly

The high current mode appears at a phase angle of -90° and 20 Ω, where the monitored individual collector currents increased to 6.8 A. At 50 V this amounts to 340 W, which almost entirely represents device dissipation.

At 20:1 load mismatch an equal power dissipation is reached at a power output of approximately 650 W CW.

Since the collector voltages remain below the device breakdown at the high impedance mode (+90°C, 150 Ω), it may be concluded, that the load mismatch susceptibility is limited by overdissipation of the transistors.



NOTE: The Printed Circuit Board shown is 75% of the original.

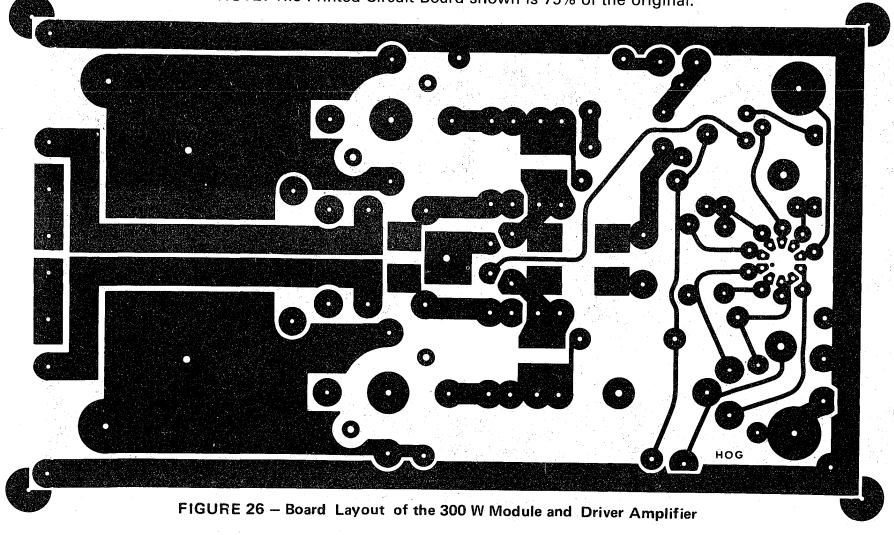


FIGURE 26 – Board Layout of the 300 W Module and Driver Amplifier

REFERENCES

1. Ruthroff: Some Broad Band Transformers, *IRE, Volume 47,* August 1975.
2. Lewis: *Notes on Low Impedance H.F. Broad Band Transformer Techniques,* Collins Radio Company, November 1964.
3. Granberg, H.: *Broadband Linear Power Amplifiers Using Push-Pull Transistors,* AN-593, Motorola Semiconductor Products Inc.
4. Granberg, H.: *Get 300 Watts PEP Linear Across 2 to 30 MHz From This Push-Pull Amplifier,* EB-27, Motorola Semiconductor Products Inc.
5. Granberg, H.: *Broadband Transformers and Power Combining Techniques for RF,* AN-749, Motorola Semiconductor Products Inc.
6. Hilbers: Design of H.F. Wideband Power Transformer Techniques, *Phillips Application Information #530.*
7. Pizalis-Couse: Broadband Transformer Design for RF Transistor Amplifiers, *ECOM-2989,* U.S. Army Electronics Command, Fort Monmouth, New Jersey, July 1968.
8. *Philips Telecommunication Review,* Volume 30, No. 4, pp. 137-146, November 1972.
9. Hejhall, R.: *Solid-State Linear Power Amplifier Design,* AN-546, Motorola Semiconductor Products Inc.
10. Lefferson: Twisted Wire Transmission Line, *IEEE Transactions on Parts, Hybrids and Packaging,* Volume PHP-7, No. 4, December 1971.
11. Krauss-Allen: Designing Toroidal Transformers to Optimize Wideband Performance, *ELECTRONICS,* August 1973.

LINEAR AMPLIFIERS FOR MOBILE OPERATION

Prepared by
Helge O. Granberg
RF Circuits Engineering

INTRODUCTION

The three versions of the amplifier described here are intended mainly for amateur radio applications, but are suitable for other applications such as marine radio with slight modifications.

100 W is obtained with two MRF455's. MRF460 or MRF453 is also adaptable to this design, resulting in approximately 1.0 to 2.5 dB higher overall power gain than the values shown. The MRF454 devices which can be directly substituted with MRF458's for slightly lower IMD, deliver the 140 W, and two MRF421 devices are used in the 180 W version.

The use of chip capacitors results in good repeatability, making the overall design suitable for mass production.

There are several precautions and design hints to be taken into consideration regarding transistor amplifiers:

1. Eliminate circuit oscillation. Oscillations may cause overdissipation of the device or exceed the breakdown voltages.
2. Limit the power supply current to prevent excessive dissipation.
3. Adopt protective circuitry, such as fast acting ALC.
4. Ensure proper attachment of the device to a heatsink using Silicone grease (such as Corning 340 or GC Electronics 8101) to fill all thermal gaps.

THE TRANSISTORS

The MRF421 with a specified power output of 100 W PEP or CW is the largest of the three RF devices. The maximum dissipation limit is 290 Watts, which means that the continuous collector current could go as high as 21.3 A at 13.6 V operated into any load. The data sheet specifies 20 A; this is actually limited by the current carrying capability of the internal bonding wires. The values given are valid at a 25°C mount temperature.

The minimum recommended collector idling current in Class AB is 150 mA. This can be exceeded at the expense of collector efficiency, or the device can be operated in Class A at an idling current of approximately one fourth the maximum specified collector current. This rule of thumb applies to most RF power transistors, although not specified for Class A operation.

The MRF454 is specified for a power output of 80 W CW. Although the data sheet does not give broadband performance or IMD figures, typical distortion products are ≈ -31 to -33 dB below one of the two test tones (7) with a 13.6 V supply. This device has the highest figure of merit (ratio of emitter periphery and base area), which correlates with the highest power gain.

The maximum dissipation is 250 Watts, and the maximum continuous collector current is 20 A. The minimum recommended collector idling current is 100 mA, and like the MRF421, can be operated in Class A.

The data sheet specification for the MRF455 is 65 W CW, but it can be operated in SSB mode, and typically makes -32 to -34 dB IMD in reference to one of the two test tones at 50 W PEP, 13.6 volts. It contains the same die as MRF453 and MRF460, but is tested for different parameters and employs a smaller package. The MRF455/MRF453/MRF460 has a higher figure of merit than the two devices discussed earlier. Due to this and the higher associated impedance levels, the power gain exceeds that of the MRF454 and MRF421 in a practical circuit. The minimum recommended collector idling current is 40 mA for Class AB, but can be increased up to 3.0 A for Class A operation.

It should be noted that the data sheet figures for power gain and linearity are lowered when the device is used in multi-octave broadband circuit. Normally the device input and output impedances vary by at least a factor of three from 1.6 to 30 MHz. Therefore, when impedance correction networks are employed, some of the power gain and linearity must be sacrificed.

The input correction network can be designed with RC or RLC combinations to give better than 1 dB gain flatness across the band with low input VSWR. In a low-voltage system, little can be done about the output without reducing the maximum available voltage swing.

At power levels up to 180 Watts and 13.6 V, the peak currents approach 30 A, and every 100 mV lost in the emitter grounding or collector dc feed also have a significant effect in the peak power capability. Thus, these factors must be emphasized in RF power circuit design.

THE BASIC CIRCUIT

Figure 1 shows the basic circuit of the linear amplifier. For different power levels and devices, the impedance ratios of T1 and T3 will be different and the values of R1, R2, R3, R4, R5, C1, C2, C3, C4 and C6 will have to be changed.

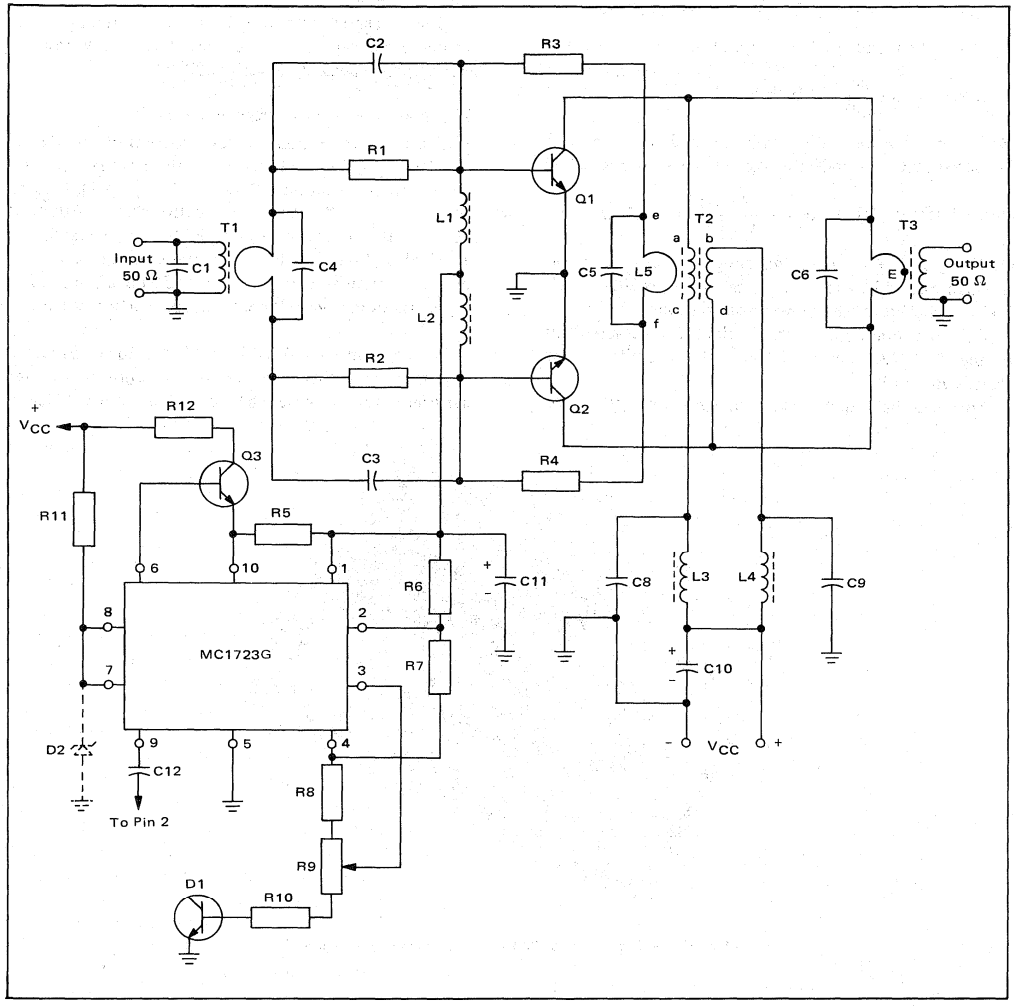


FIGURE 1 – Basic Circuit of Linear Amplifier

The Bias Voltage Source

The bias voltage source uses active components (MC1723G and Q3) rather than the clamping diode system as seen in some designs. The advantages are line voltage regulation capability, low stand-by current, (≈1.0 mA) and wide range of voltage adjustability. With the component values shown, the bias voltage is adjustable from 0.5 to 0.9 Volts, which is sufficient from Class B to Class A operating conditions.

In Class B the bias voltage is equal to the transistor V_{BE}, and there is no collector idling current present (except small collector-emitter leakage, I_{CES}), and the conduction angle is 180°.

In Class A the bias is adjusted for a collector idling current of approximately one-half of the peak current in actual operating conditions, and the conduction angle is 360°.

In Class AB, (common for SSB amplifiers) the bias is set for a low collector quiescent current, and the conduction angle is usually somewhat higher than 180°.

The required base bias current can be approximated as:

$$\frac{I_C}{h_{FE}},$$

where:

I_C = Collector current, assuming an efficiency of 50%

and P_{out} of 180 W is: $\frac{2P_{out}}{V_{CC}} = \frac{360}{13.6} = 26.47$ A.

h_{FE} = Transistor dc beta (typical 30, from data sheet)

Bias current = $\frac{26.47}{30} = 0.88$ A

R12 shares the dissipation with Q3, and its value must be such that the collector voltage never drops below approximately 2.0 V (e.g. $\frac{(13.6-2)}{0.88} = 13.2\ \Omega$). The MRF421 devices used for this design had h_{FE} values on the high side (45), and R12 was calculated as 20Ω, which is also sufficient for the lower power versions.

R5 determines the current limiting characteristics of the MC1723, and 0.5 Ω will set the limiting point to 1.35 A, ± 10%.

For SSB operation, excluding two-tone testing, the duty cycle is low, and the energy charged in C11 can supply higher peak bias currents than required for 180 W PEP.

It is possible to operate the basic regulator circuit, MC1723, at lower output voltages than specified, with modified component values, at a cost of reduced line and output voltage regulation tolerances which are still more than adequate for this application. Temperature sensing diode D1 is added for bias tracking with the RF power transistors. The base-emitter junction of a 2N5190 or similar device can be used for this purpose. The temperature tracking within 15% to 60°C is achieved, even though the die processing is quite different from that of the RF transistors. The physical dimensions of Case 77 (2N5190) permits its use for the center stand-off of the circuit board.

The measured output voltage variations of the bias source from zero to 1.0 A were ± 8-12 mV resulting in a source impedance of ≈ 30 mΩ.

The Input Frequency Correction Network

The input correction network consists of R1, R2, C2 and C3. With the combination of the negative feedback derived from L5 through R3 and R4 (Figure 1), it forms an attenuator with frequency selective characteristics. At 30 MHz the input power loss is 1-2 dB, increasing to 10-12 dB at 1.6 MHz. This compensates the gain variations of the RF transistors over the 1.6 to 30 MHz band, resulting in an overall gain flatness of approximately ±1.0 to ±1.5 dB.

Normally an input VSWR of 2.0:1 or lower (Figure 8) is possible with this type of input network (considered sufficient for most applications). More sophisticated LRC networks will yield slightly better VSWR figures, but are more complex and sometimes require individual adjustments.

Additional information on designing and optimizing these networks can be found in reference(2).

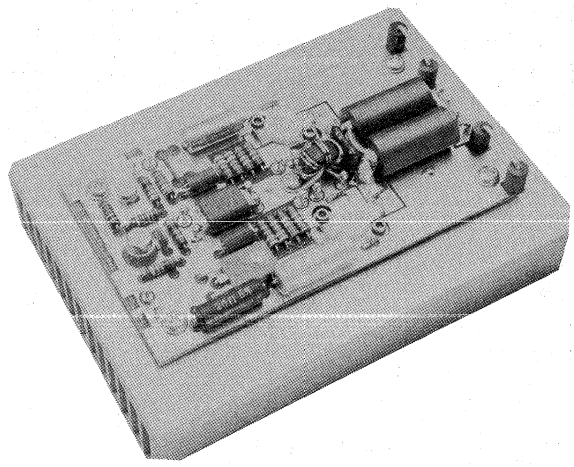
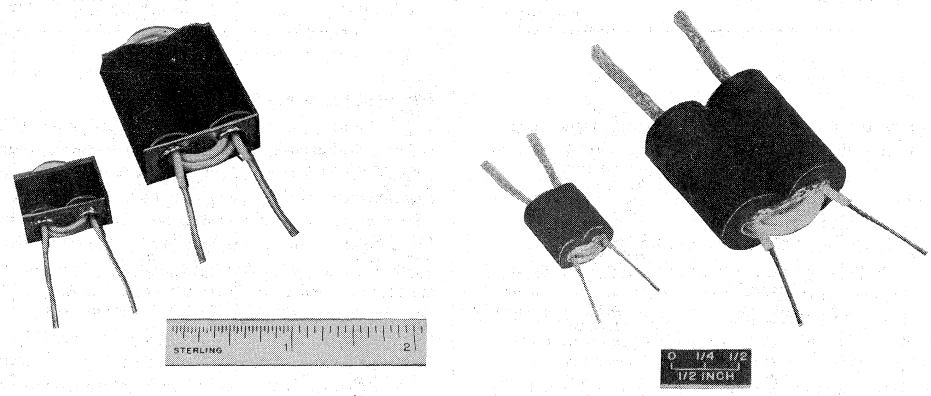


FIGURE 2 – Photograph of 180 W Version of the Linear Amplifier

The Broadband Transformers

The input transformer T1 and the output transformer T3 are of the same basic type, with the low impedance winding consisting of two pieces of metal tubing, electrically shorted in one end and the opposite ends being the connections of this winding (Figure 3A). The multiturn high impedance winding is threaded through the tubing so that the low and high impedance winding connections are in opposite ends of the transformer.



A. B.

FIGURE 3 — Two Variations of the Input and Output Transformers (T1 and T3)

The physical configuration can be implemented in various manners. A simplified design can be seen in Figure 3B. Here the metal tubing is substituted with copper braid, obtained from any co-axial cable of the proper diameter (4). The coupling coefficient between the primary and secondary windings is determined by the length-to-diameter ratio of the metal tubing or braid, and the gauge and insulation thickness of the wire used for the high impedance winding. For high impedance ratios (36:1 and higher), miniature co-axial cable where only the braid is used, leaving the inner conductor disconnected gives the best results. The high coefficient of coupling is important only at the high-frequency end of the band, e.g. 20 to 30 MHz. Additional information on these transformers can be found in reference (5).

Both transformers are loaded with ferrite material to provide sufficient low-frequency response. The minimum required inductance in the one turn winding can be calculated as:

$$L = \frac{R}{2\Pi f}$$

where L = Inductance in μH
R = Base-to-Base or Collector-to-Collector Impedance
f = Lowest Frequency in MHz

For example, in the 180 Watt version the input transformer is of 16:1 impedance ratio, making the secondary impedance 3.13 Ω with a 50 Ω interface.

Then: $L = \frac{3.13}{6.28 \times 1.6} = 0.31\ \mu H$

For the output transformer having a 25:1 impedance ratio to a 50 Ω interface, $L = \frac{2}{6.28 \times 1.6} = 0.20\ \mu H$.

It should be noted that in the lower power versions, where the input and output impedances are higher and the transformers have lower impedance ratios, the required minimum inductances are also higher.

T2, the collector choke supplying the dc to each collector, also provides an artificial center tap for T3. This combination functions as a real center tapped transformer with even harmonic cancellation. T2 provides a convenient low impedance source for the negative feedback voltage, which is derived from a separate one turn winding.

T3 alone does not have a true ac center tap, as there is virtually no magnetic coupling between its two halves. If the collector dc feed is done through point E (Figure 1) without T2, the IMD or power gain is not affected, but the even harmonic suppression may be reduced by as much as 10 dB at the lower frequencies.

The characteristic impedance of ac and bd (T2) should equal one half the collector-to-collector impedance but is not critical, and for physical convenience a bifilar winding is recommended.

The center tap of T2 is actually bc (Figure 1), but for stabilization purposes, b and c are separated by RF chokes by-passed individually by C8 and C9.

TABLE 1 — Parts List

	100 W AMPLIFIER	140 W AMPLIFIER	180 W AMPLIFIER
C1	51 pF	51 pF	82 pF
C2, C3	5600 pF	5600 pF	6800 pF
C4	—	390 pF	1000 pF
C5	680 pF	680 pF	680 pF
C6	1620 pF (2 x 470 pF chips + 680 pF dipped mica in parallel)	1760 pF (2 x 470 pF chips + 820 pF dipped mica in parallel)	1940 pF (2 x 470 pF chips + 1000 pF dipped mica in parallel)
C8,C9	0.68 μF	0.68 μF	0.68 μF
C10	100 μF/20 V electrolytic	100 μF/20 V electrolytic	100 μF/20 V electrolytic
C11	500 μF/3 V electrolytic	500 μF/3 V electrolytic	500 μF/3 V electrolytic
C12	1000 pF disc ceramic	1000 pF disc ceramic	1000 pF disc ceramic
R1, R2	2 x 3.9 Ω/½ W in parallel	2 x 3.6 Ω/½ W in parallel	2 x 3.3 Ω/½ W in parallel
R3, R4	2 x 4.7 Ω/½ W in parallel	2 x 5.6 Ω/½ W in parallel	2 x 3.9 Ω/½ W in parallel
R5	1.0 Ω/½ W	0.5 Ω/½ W	0.5 Ω/½ W
R6	1.0 kΩ/½ W	1.0 kΩ/½ W	1.0 kΩ/½ W
R7	18 kΩ/½ W	18 kΩ/½ W	18 kΩ/½ W
R8	8.2 kΩ/½ W	8.2 kΩ/½ W	8.2 kΩ/½ W
R9	1.0 kΩ trimpot	1.0 kΩ trimpot	1.0 kΩ trimpot
R10	150 Ω/½ W	150 Ω/½ W	150 Ω/½ W
R11	1.0 kΩ/½ W	1.0 kΩ/½ W	1.0 kΩ/½ W
R12	20 Ω/5 W	20 Ω/5 W	20 Ω/5 W
L1, L2	Ferroxcube VK200 19/4B ferrite choke		
L3, L4	Two Fair-Rite Products ferrite beads 2673021801 or equivalent on AWG #16 wire each.		
L5	1 separate turn through toroid of T2.		
T1	9:1 (3:1 turns ratio)	9:1 (3:1 turns ratio)	16:1 (4:1 turns ratio)
	Ferrite core: Stackpole 57-1845-24B, Fair-Rite Products 2873000201 or two Fair-Rite Products 0.375" OD x 0.200" ID x 0.400", Material 77 beads for type A (Figure 3) transformer. See text.		
T2	6 turns of AWG #18 enameled, bifilar wire		
	Ferrite core: Stackpole 57-9322, Indiana General F627-8 Q1 or equivalent.		
T3	16:1 (4:1 turns ratio)	16:1 (4:1 turns ratio)	25:1 (5:1 turns ratio)
	Ferrite core: 2 Stackpole 57-3238 ferrite sleeves (7D material) or number of toroids with similar magnetic characteristics and 0.175" sq. total cross sectional area. See text.		
	All capacitors except C12, part of C5 and the electrolytics are ceramic chips.		
	Values over 82 pF are Union Carbide type 1225 or Varadyne size 14.		
	Others are type 1813 or size 18 respectively.		
Q1, Q2	MRF453, MRF460, MRF455	MRF454, MRF458,	MRF421
Q3		2N5989 or equivalent	
D1		2N5190 or equivalent	
D2		Not Used	
	c. Dotted line in performance data.	b. Dashed line in performance data.	a. Solid line in performance data.

GENERAL DESIGN CONSIDERATIONS

As the primary and secondary windings of T3 are electrically isolated, the collector dc blocking capacitors (which may also function as low-frequency compensation elements) have been omitted. This decreases the loss in RF voltage between the collectors and the transformer primary, where every 100 mV amounts to approximately 2 W in output power at 180 W level. The RF currents at the collectors operating into a 2Ω load are extremely high, e.g.: $I_{RF} = \sqrt{\frac{180}{2.0}} = 9.5$ A, or peak $\frac{9.5}{0.707} = 13.45$ A.

Similarly, the resistive losses in the collector dc voltage path should be minimized. From the layout diagram of the lower side of the circuit board (Figure 4), V_{CC} is brought through two 1/4" wide runs, one on each side of the board. With the standard 1.0 oz. laminate, the copper thickness is 1.4 thousands of an inch, and their combined cross sectional area would be equivalent to AWG #20 wire. This is not adequate to carry the dc collector current which under worst case conditions can be over 25 A. Therefore, the high power version of this design requires 2 oz. or heavier copper laminate, or these runs should be reinforced with parallel wires of sufficient gauge.

The thermal design (determining the size and type of a heat sink required) can be accomplished with information in the device data sheet and formulas presented in references 5 and 6. As an example, with the 180 W unit using MRF421's, the Junction-to-Ambient Temperature

($R_{\theta JA}$) is calculated first as $R_{\theta JA} = \frac{T_J - T_A}{P}$ where:

T_J = Maximum Allowed Junction Temperature (150°C).
T_A = Ambient Temperature (40°C).

P = Dissipated Power $(\frac{180}{\eta}) \times (100 - \eta)$

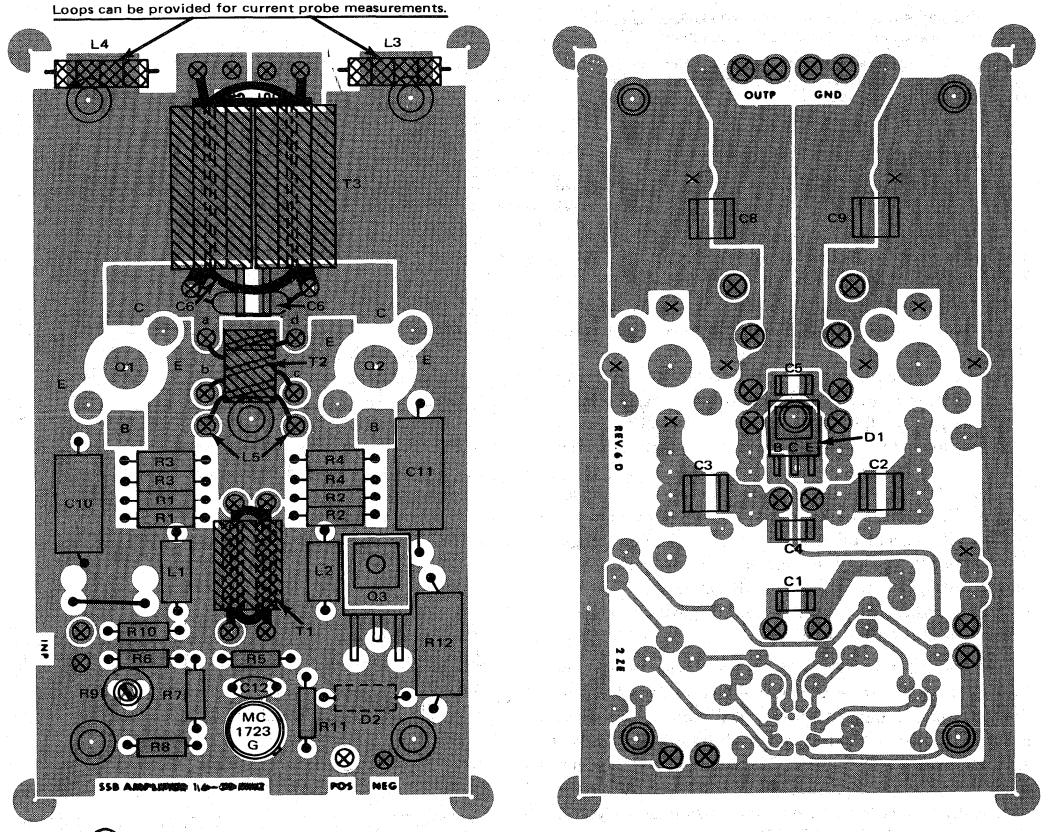
η = Collector Efficiency (%).

If the worst case efficiency at 180 W CW is 55%, then

P = 148 W, and $R_{\theta JA} = \frac{150 - 40}{(\frac{148}{2})} = 1.49^{\circ}$ C/W (for one device). The Heat Sink-to-Ambient Thermal Resistance, $R_{\theta SA} = R_{\theta JA} - (R_{\theta JC} + R_{\theta CS})$ where: $R_{\theta JC}$ = Device Junction-to-Case Thermal Resistance, 0.60°C/W* (from data sheet).
$R_{\theta CS}$ = Thermal Resistance, Case-to-Heat Sink, 0.1°C/W (from table in reference 5).

Then: $R_{\theta SA} = \frac{1.49 - (0.60 + 0.1)}{2} = 0.395^{\circ}$ C/W

This number can be used to select a suitable heat sink for the amplifier. The information is given by most manufacturers for their standard heat sinks, or specific lengths of extrusion. As an example, a 9.1" length of thermalloy 6153 or a 7.6" length of Aavid Engineering 60140 extrusion would be required for 100% duty cycle, unless the air velocity is increased by a fan or other means.



○ = Board Stand Off's
⊗ = Terminal Pins and Feedthroughs
X = Feedthrough Eyelets

* The $R_{\theta JC}$ figure of 0.875°C/W given for the MRF421 is in error, and will be corrected in the future prints of the data sheet.

FIGURE 4 – Component Layout of the Basic Amplifier

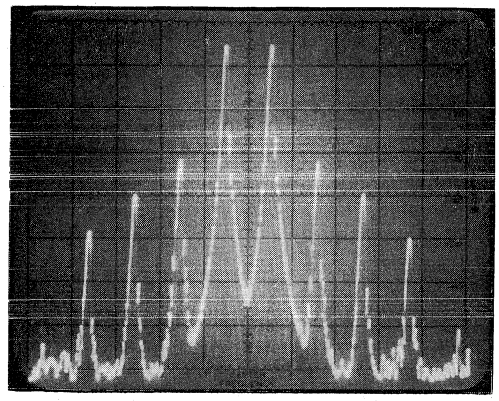


FIGURE 5 – An Example of the IMD Spectral Display (c. Power Output = 180 W PEP, 30.00 MHz)

The Two Tones Have Been Adjusted 6 dB Below the Top Line, and the Distortion Products Relative to Peak Power can be Directly Read on the Scale.

PERFORMANCE AND MEASUREMENTS

The performance of each amplifier was measured with equipment similar to what is described in reference (2). The solid lines in Figures 6, 7, 8 and 9 represent the 100 W unit, the dashed lines represent the 140 W unit, and the dotted lines refer to the 180 W version. The data presented is typical, and spreads in the transistor h_{FE}'s will result in slight variations in RF power gain (Figure 7).

The performance data is also affected by the purity of the driving source. There should be at least 5–6 dB IMD margin to the expected power amplifier specification, and a harmonic suppression of 50 dB minimum below the fundamental is recommended (7).

The IMD measurements were done in accordance to the E.I.A. proposed standard, commonly employed in Ham Radio and other commercial equipment design. The distortion products are referenced to the peak power, and adjusting the tone peaks 6 dB below the 0 dB line on the spectrum analyzer screen (Figure 5) provides a direct reading on the scale.

The collector efficency under two tone test conditions is normally 15 – 20% lower than at CW. The load line has been optimized for the peak power (as well as possible in a broadband system with transformer impedance ratios of 4:1, 9:1, 16:1, 25:1, etc. available), which at SSB represents a smaller duty cycle, and the power output varies between zero and maximum. Typical figures are 40 – 45% and 55 – 65% respectively.

The stability and load mismatch susceptibility were tested at 15 and 30 MHz employing an LC network (2) to simulate high and low reactive loads at different phase angles. The maximum degree of load mismatch was controlled by placing high power 50-Ohm attenuators between the amplfiier output and variable LC network.

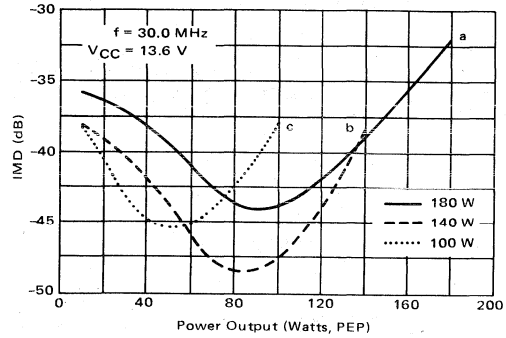


FIGURE 6 – Intermodulation Distortion versus Power Output

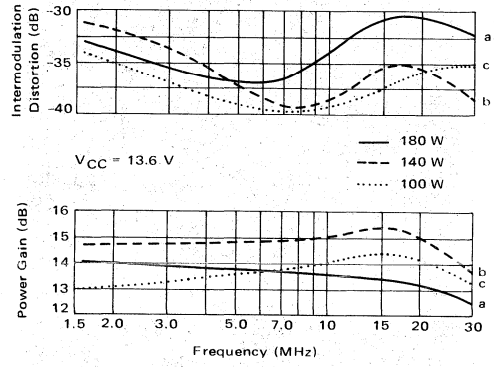


FIGURE 7 – IMD and Power Gain versus Frequency

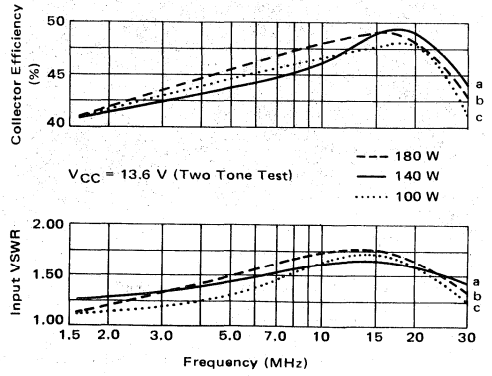


FIGURE 8 – Input VSWR and Collector Efficiency versus Frequency

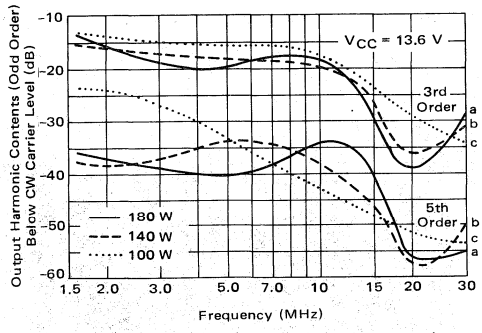


FIGURE 9 – Output Harmonic Contents (Odd Order) versus Frequency

A 2 dB attenuator limits the output VSWR to 4.5:1, 3 dB to 3.0:1, 6 dB to 1.8:1 etc., assuming that the simulator is capable of infinite VSWR at some phase angle. The attenuators for -1.0 dB or less were constructed of a length of RG-58A co-axial cable, which at 30 MHz has an attenuation of 3.0 dB/100 ft. and at 15 MHz 2.0 dB/100 ft. Combinations of the cable and the resistive attenuators can be used to give various degrees of total attenuation.

The tests indicated the 100 W and 140 W amplifiers to be stable to 5:1 output VSWR at all phase angles, and the 180 W unit is stable to 9:1. All units passed a load mismatch test at full rated CW power at an output load mismatch of 30:1, which they were subjected to, until the heat sink temperature reached 60°C. For this, the load mismatch simulator was motor driven with a 2 second cycle period.

Output Filtering

Depending on the application, harmonic suppression of -40 dB to -60 dB may be required. This is best accomplished with low-pass filters, which (to cover the entire range) should have cutoff frequencies e.g. 35 MHz, 25 MHz, 15 MHz, 10 MHz, 5.5 MHz and 2.5 MHz.

The theoretical aspect of low-pass filter design is well covered in the literature (8).

A simple Chebyshev type constant K, 2 pole filter (Figure 10) is sufficient for 40 – 45 dB output harmonic suppression.

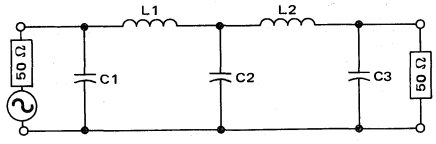


FIGURE 10

The filter is actually a dual pi-network, with each pole introducing a -90° phase shift at the cutoff frequency, where L1, L2, C1 and C3 should have a reactance of 50 Ohms, and C2 should be 25 Ohms. If C2 is shorted, the resonances of L1C1 and L2C3 can be checked with a grid-dip meter or similar instrument for their resonant frequencies.

The calculated attenuation for this filter is 6.0 dB per element/octave, or -45 dB for the 3rd harmonic. In practice, only -35 to -40 dB was measured, but this was due to the low Q values of the inductors (approximately 50). Air core inductors give excellent results, but toroids of magnetic materials such as Micrometals grade 6 are also suitable at frequencies below 10 MHz. Dipped mica capacitors can be used throughout.

If the filters are correctly designed and the component tolerances are 5% or better, the power loss will be less than 1.0 dB.

NOTE: The use of these amplifiers is illegal for Class D Citizens band service.

SUMMARY

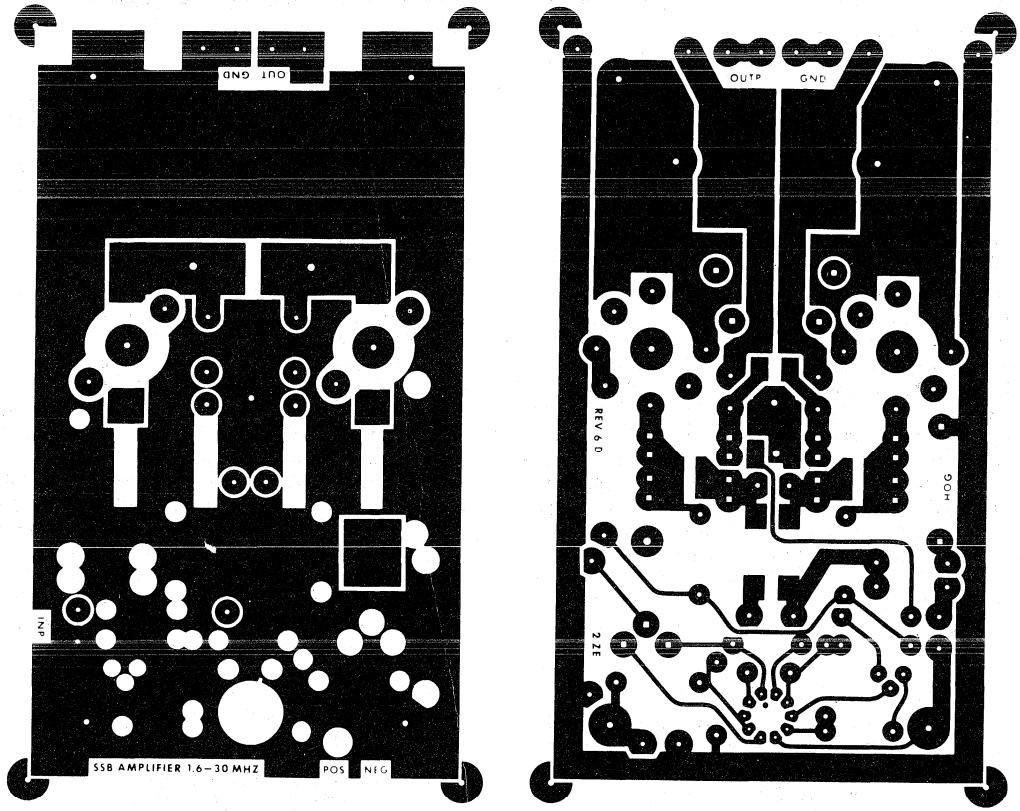
The basic circuit layout (Figure 1) has been successfully adopted by several equipment manufacturers. Minor modifications may be necessary depending on the availability of specific components. For instance, the ceramic chip capacitors may vary in physical size between various brands, and recent experiments show that values $> 0.001\ \mu F$ can be substituted with unencapsulated polycarbonate stacked-foil capacitors. These capacitors are available from Siemens Corporation (type B32540) and other sources. Also T1 and T2 can be constructed from stacks of ferrite toroids with similar material characteristics. Toroids are normally stock items, and are available from most ferrite suppliers.

The above is primarily intended to give an example of the device performance in non-laboratory conditions, thus eliminating the adjustments from unit to unit.

REFERENCES:

1. Hejhall R.: *Understanding Transistor Response Parameters,* AN-139A Motorola Semiconductor Products Inc..
2. Granberg, H.: *A Two Stage 1 kW Solid-State Linear Amplifier,* AN-758 Motorola Semiconductor Products, Inc..
3. Granberg, H.: *Get 300 W PEP Linear Across 2 to 30 MHz From This Push-Pull Amplifier,* EB-27A Motorola Semiconductor Products Inc..
4. Granberg, H.: *Broadband Transformers and Power Combining Techniques for RF,* AN-749 Motorola Semiconductor Products Inc..
5. White, John: Thermal Design of Transistor Circuits, *QST*, April 1972, pp. 30-34.
6. *Mounting Stripline-Opposed-Emitter (SOE) Transistors,* AN-555 Motorola Semiconductor Products Inc..
7. Granberg, H.: *Measuring the Intermodulation Distortion of Linear Amplifiers,* EB-38 Motorola Semiconductor Products Inc..
8. *Reference Data for Radio Engineers,* ITT, Howard & Sams Co., Inc.

The PCB layout below is a supplement to Figure 4 and may be used for generating printed circuit artwork.



NOTE: The Printed Circuit Board shown is 75% of the original.

FIGURE 11 — Printed Circuit Board Layout

LOW-DISTORTION 1.6 TO 30 MHz SSB DRIVER DESIGNS

Prepared by
Helge O. Granberg
RF Circuits Engineering

GENERAL CONSIDERATION

Two of the most important factors to be considered in broadband linear amplifier design are the distortion and the output harmonic rejection.

The major cause for intermodulation distortion is amplitude nonlinearity in the active element. The nonlinearity generates harmonics, and the fundamental odd-order products are defined as $2f_1-f_2$, $2f_2-f_1$, $3f_2-2f_2$, $3f_2-2f_1$, etc., when a two-tone test signal is used. These harmonics may not always appear in the amplifier output due to filtering and cancellation effects, but are generated within the active device. The amplitude and harmonic distortion cannot really be distinguished, except in a case of a cascaded system, where even-order products in each stage can produce odd-order products through mixing processes that fall in the fundamental region.[2] This, combined with phase distortion—which in practical circuits is more apparent at higher frequencies—can make the distortion analysis extremely difficult;[5,2] whereas, if only amplitude distortion was present, the effect of IMD in each stage could easily be calculated.

In order to expect a low harmonic output of the power amplifier, it is also important for the driving source to be harmonic-free. This is difficult in a four-octave bandwidth system, even at 10-20 watt power levels. Class A biasing helps the situation, and Class A push-pull yields even better results due to the automatic rejection of even harmonics.

Depending on the application, a full Class A system is not always feasible because of its low efficiency. The theoretical maximum is 50%, but practical figures are not higher than 25% to 35%. It is sometimes advantageous to select a bias point somewhere between Class AB and A which would give sufficiently good results, since filtering is required in the power amplifier output in most instances anyway.

In order to withstand the high level of steady dc bias current, Class A requires a much larger transistor die than Class B or AB for a specific power output. There are sophisticated methods such as generating the bias voltage from rectified RF input power, making the dc bias proportional to the drive level.[1] This also yields to a better efficiency.

20 W, 25 dB AMPLIFIER WITH LOW-COST PLASTIC DEVICES

The amplifier described here provides a total power gain of about 25 dB, and the construction technique allows the use of inexpensive components throughout. The plastic RF power transistors, MRF475 and MRF476, featured in this amplifier, were initially developed for the CB market. The high manufacturing volume of these TO-220 packaged parts makes them ideal for applications up to 50 MHz, where low cost is an important factor.

The MRF476 is specified as a 3-watt device and the MRF475 has an output power of 12 watts. Both are extremely tolerant to overdrive and load mismatches, even under CW conditions. Typical IMD numbers are better than -35 dB, and power gains are 18 dB and 12 dB, respectively, at 30 MHz.

The collectors of the transistors are electrically connected to the TO-220 package mounting tab which must be isolated from the ground with proper mounting hardware (TO-220 AB) or by floating heat dissipators. The latter method, employing Thermalloy 6107 and 6106 heat dissipators, was adapted for this design. Without an airflow, the 6106 and 6107 provide sufficient heat sinking for about 30% duty cycle in the CW mode. Collector idle currents of 20 mA are recommended for both devices, but they were increased to 100 mA for the MRF475 and to 40 mA for the MRF476 to reduce the higher order IMD products and to achieve better harmonic suppression.

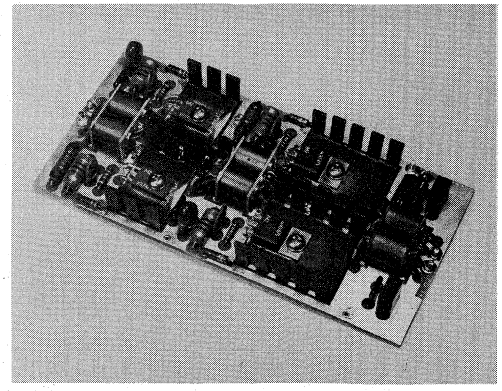


FIGURE 1

Biasing and Feedback

The biasing is achieved with the well-known clamping diode arrangement (Figure 2). Each stage has it own diode, resistor, and bypass network, and the diodes are mounted between the heat dissipators, being in physical contact with them for temperature-tracking purposes. A better thermal contact is achieved through the use of silicone grease in these junctions.

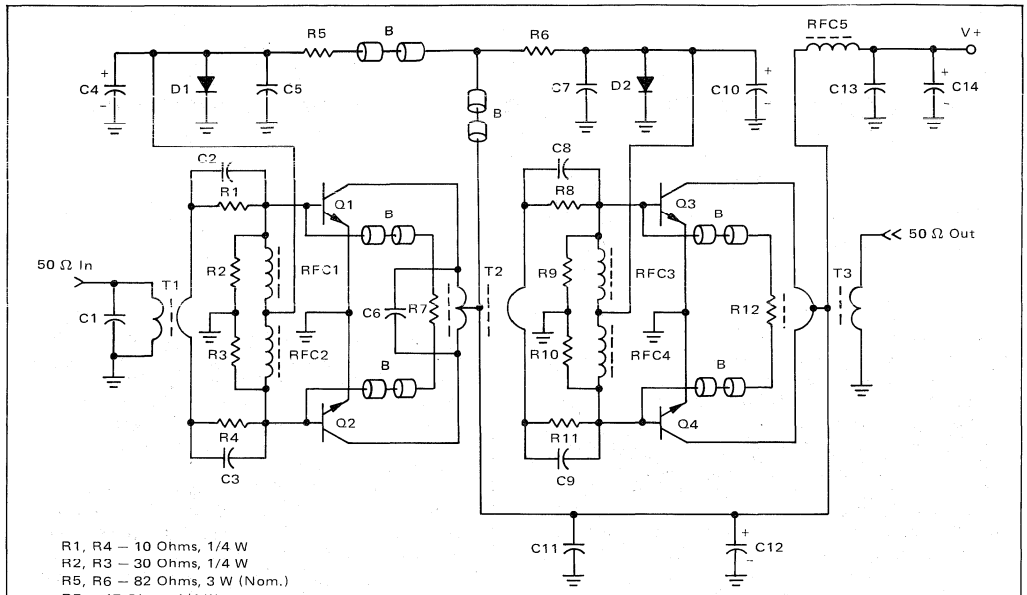


FIGURE 2

The bias currents of each stage are individually adjustable with R5 and R6. Capacitors C4 and C10 function as audio-frequency bypasses to further reduce the source impedance at the frequencies of modulation.

This biasing arrangement is only practical in low and medium power amplifiers, since the minimum current required through the diode must exceed I_C/h_{fe}.

Gain leveling across the band is achieved with simple RC networks in series with the bases, in conjunction with negative feedback. The amplitude of the out-of-phase voltages at the bases is inversely proportional to the frequency as a result of the series inductance in the feedback loop and the increasing input impedance of the transistors at low frequencies. Conversely, the negative feedback lowers the effective input impedance presented to the source (not the input impedance of the device itself) and with proper voltage slope would equalize it. With this technique, it is possible to maintain an input VSWR of 1.5:1 or less from 1.6 to 30 MHz.

Impedance Matching and Transformers

Matching of the input and output impedances to 50 ohms, as well as the interstage matching, is accomplished with broadband transformers (Figures 3 and 4).

Normally only impedance ratios such as 1:1, 4:1, 9:1, etc., are possible with this technique, where the low-impedance winding consists of metal tubes, through which an appropriate number of turns of wire is threaded to form the high-impedance winding. To improve the broadband characteristics, the winding inductance is increased with magnetic material. An advantage of this design is its suitability for large-quantity manufacturing, but it is difficult to find low-loss ferrites with sufficiently high permeabilities for applications where the physical size must be kept small and impedance levels are relatively high. Problems were encountered especially with the output transformer design, where an inductance of 4 µH minimum is required in the one-turn winding across the collectors, when the load impedance is

$$\frac{2(V_{CE} - V_{CEsat})^2}{P_{out}} = \frac{2(13.6 - 2.5)^2}{20} = 12.3 \text{ ohms.}^{4,8}$$

Ferrites having sufficiently low-loss factors at 30 MHz range only up to 800–1000 in permeability and the inductance is limited to 2.5–3.0 µH in the physical size required. This would also limit the operation to approximately 4 MHz, below which excessive harmonics are

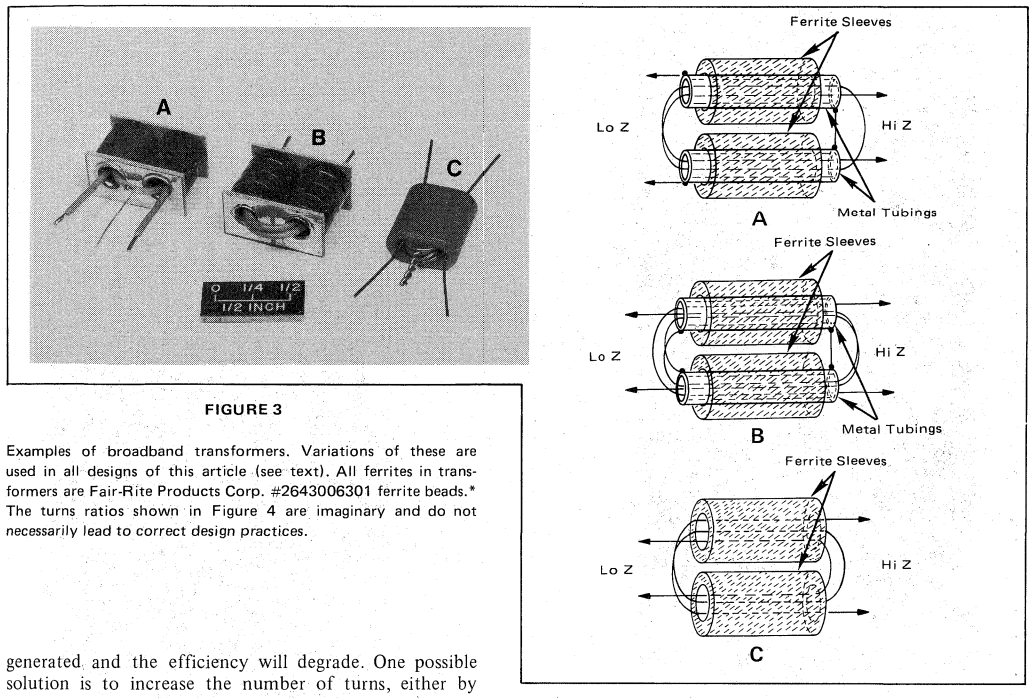


FIGURE 3

Examples of broadband transformers. Variations of these are used in all designs of this article (see text). All ferrites in transformers are Fair-Rite Products Corp. #2643006301 ferrite beads.* The turns ratios shown in Figure 4 are imaginary and do not necessarily lead to correct design practices.

FIGURE 4

generated and the efficiency will degrade. One possible solution is to increase the number of turns, either by using the metal tubes for only part of the windings as in Figure 4B, or simply by winding the two sets of windings randomly through ferrite sleeves or a series of beads (Figures 3C and 4C). In the latter, the metal tubes can be disregarded or can be used only for mounting purposes. T3 was eventually replaced with a transformer of this type, although not shown in Figure 1.

Below approximately 100 MHz, the input impedances of devices of the size of MRF475 and smaller are usually capacitive in reactance, and the X_S is much smaller than the R_S, (Low Q). For practical purposes, we can then use the formula $\sqrt{(R_S^2 + X_S^2)}$ to find the actual input impedance of the device. The data-sheet numbers for 30 MHz are 4.5, -j2.4 ohms, and we get $\sqrt{(4.5^2 + 2.4^2)} =$ 5.1 ohms. The base-to-base impedance in a push-pull circuit would be four times the base-to-emitter impedance of one transistor. However, in Class AB, where the base-emitter junction is forward biased and the conduction angle is increased, the impedance becomes closer to twice that of one device. The rounded number of 11 ohms must then be matched to the driver output. The drive power required with the 10 dB specified minimum gain is

$$P_{out}/Log^{-1}(G_{PE}/10) = 2.0\ W$$

and the driver output impedance using the previous formula is $2(11.1^2)/2 = 123$ ohms. The 11 ohms in series with the gain-leveling networks (C8, R8 and C9, R11) is 17 ohms. The closest practical transformer for this interface would be one with 9:1 impedance ratio. This would present a higher-than-calculated load impedance to the driver collectors, and for the best linearity the output load should be lower than required for the optimum gain and efficiency. Considering that the device input impedance increases at lower frequencies, a better overall match is possible with a 4:1, especially since the negative feedback is limited to only 4 dB at 2 MHz due to its effect on the efficiency and linearity.

The maximum amount of feedback a circuit can tolerate depends much on the physical layout, the parasitic inductances, and impedance levels, since they determine the phase errors in the loop. Thus, in general, the high-level stages should operate with lower feedback than the low-level stages.

The maximum amount of feedback the low-level driver can tolerate without noticeable deterioration in IMD is about 12 dB. This makes the total 16 dB, but from the data sheets we find that the combined gain variation for both devices from 2 to 30 MHz is around 29 dB. The difference, or 13 dB, should be handled by the gain-leveling networks.

The input impedance of the MRF476 is 7.55, -j0.65 ohms at 30 MHz resulting in the base-to-base impedance of $2 \times \sqrt{(7.55^2 + 0.65^2)} = 15.2$ ohms. This, in series with networks R1, C1 and R4, C3 (2 x 4.4 ohms), gives 24 ohms, and would require a 2:1 impedance ratio transformer for a 50-ohm interface. However, due to the influence of strong negative feedback in this stage, a better overall matching is possible with 4:1 ratio. The input networks were designed in a manner similar to that described in Reference 8.

*Wallkill, N.Y. 12589

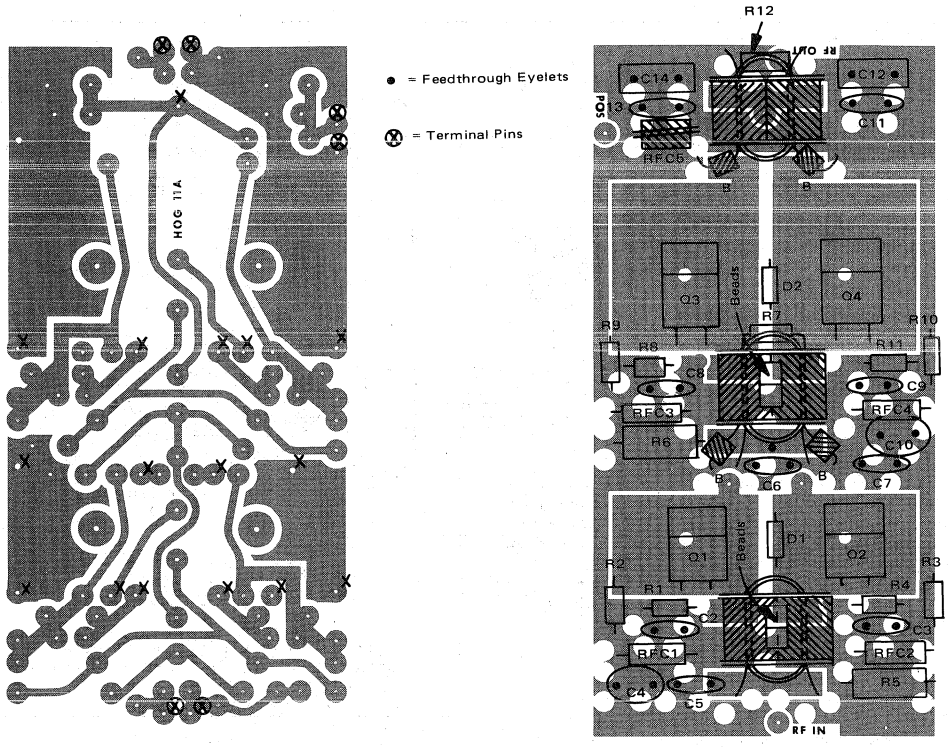


FIGURE 5
Component Layout Diagram of Low-Cost 20 W Amplifier

The leads of R7 and R12 form the one-turn feedback windings in T2 and T3. Ferrite beads in dc line can be seen located under T1 and T2.

Measurements and Performance Data

At a power output of 20 W CW, all output harmonics were measured about 30 dB or more below the fundamental, except for the third harmonic which was only attenuated 17 dB to 18 dB at frequencies below 5 MHz. Typical numbers for the higher order distortion products (d_9 and d_{11}) are in the order o. -60 dB above 7 MHz and -50 dB to -55 dB at the lower frequencies. These both can be substantially reduced by increasing the idle currents, but larger heat sinks would be necessary to accommodate the increased dissipation.

The efficiency shown in Figure 6 represents the overall figure for both stages. Currents through the bias networks, which are 82/(13.6 - 0.7) = 0.16 A each, are excluded. Modified values for R5 and R6 may have to be selected, depending on the forward voltage characteristics of D1 and D2.

Although this amplifier was designed to serve as a 1.6 to 30 MHz broadband driver, it is suitable for the citizens band use as well. With some modifications and design shortcuts, the optimization can be concentrated to one frequency.

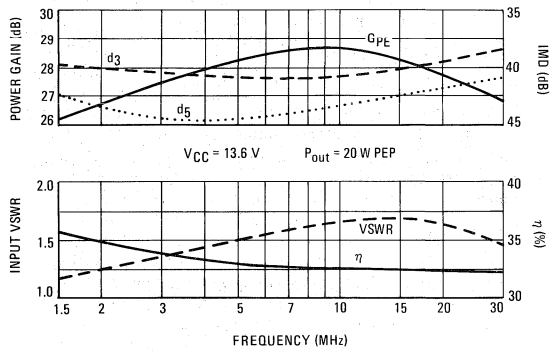


FIGURE 6

Intermodulation distortion and power gain versus frequency (upper curves).

Input VSWR and combined collector efficiency of both stages (lower curves).

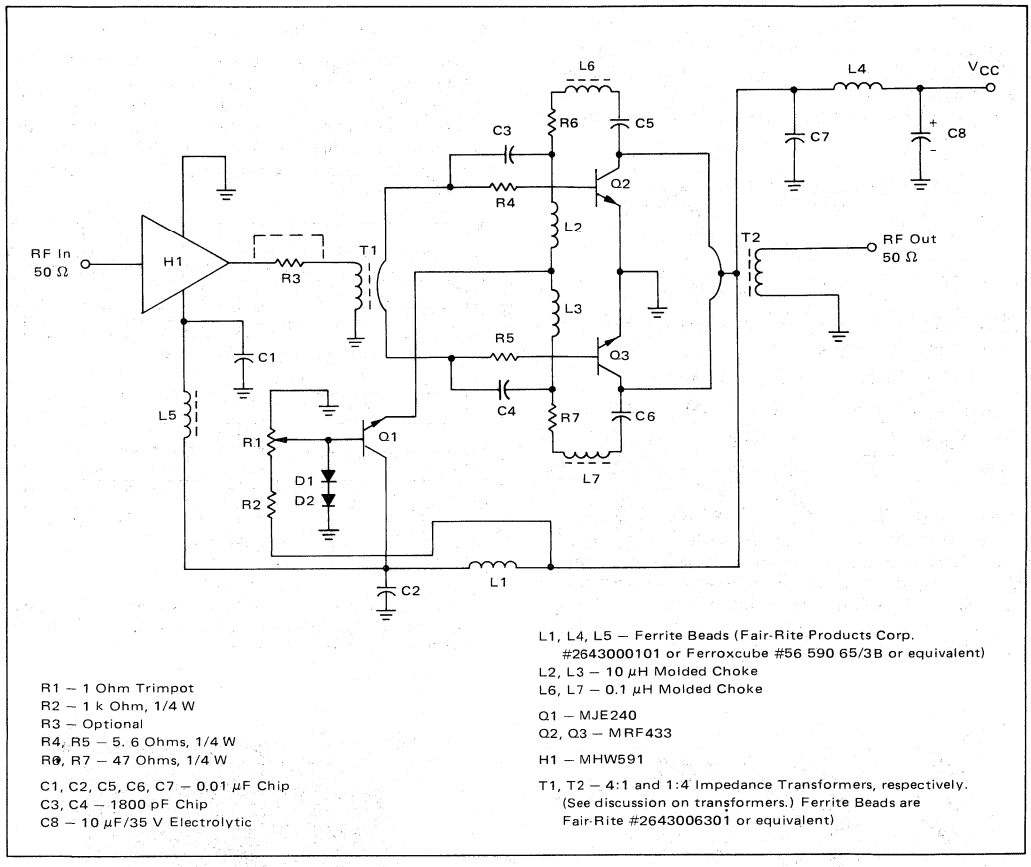


FIGURE 8

The output matching is done with a transformer similar to that described in the first part of this paper (Figures 4B, 4C). This transformer employs a multi-turn primary, which can be provided with a center tap for the collector dc feed. In addition to a higher primary inductance, more effective coupling between the two transformer halves is obtained, which is important regarding the even-order harmonic suppression.

28-Volt Version

A 28-V version of this unit has also been designed with the MHW592 and a pair of MRF401s. The only major change required is the output transformer, which should have a 1:1 impedance ratio in this case. The transformer consists of six turns of RG-196 coaxial cable wound on an Indiana General F-627-8-Q1 toroid. Each end of the braid is connected to the collectors, and the inner conductor forms the secondary. A connection is made in the center of the braid (three turns from each end) to form the center tap and dc feed.

The MRF433 and MRF401 have almost similar input characteristics, and no changes are necessary in the input circuit, except for the series feedback resistors, which should be 68–82 ohms and 1 W.

In designing the gain-leveling networks, another approach can be taken, which does not involve the computer program described in Reference 8. Although the input VSWR is not optimized, it has proved to give satisfactory results.

The amount of negative feedback is difficult to determine, as it depends on the device type and size and the physical circuit layout. The operating voltage has a minimal effect on the transistor input characteristics, which are more determined by the electrical size of the die. High-power transistors have lower input impedances and higher capacitances, and phase errors are more likely to occur due to circuit inductances.

Since the input capacitance is an indication of electrical size of the device, we can take the paralleled value (X_p) at 2 MHz, which is $X_S + (R_S^2/X_S)$ and for MRF433 $3.5 + (9.1^2/3.5) = 27$ ohms. The X_p of the largest devices available today is around 10 ohms at 30 MHz, and experience has shown that the maximum feedback should be limited to about 5 dB in such case. Using these figures

as constants, and assuming the G_{PE} is at least 10 dB, we can estimate the amount of feedback as: $5/(10^2/27) + 5 = 6.35$ dB, although only 4 dB was necessary in this design due to the low ΔG_{PE} of the devices.

The series base resistors (R4 and R5) can be calculated for 4 dB loss as follows:

$$\frac{[(V_{in} \times \Lambda 4dB) - V_{in}]}{I_{in}} = \frac{[(0.79 \times 1.58) - 0.79]}{0.04}$$

$$= 11.45 \text{ ohms, or}$$

$$11.45/2 = 5.72 \text{ ohms each.}$$

$Z_{in}(2\text{ MHz}) = \sqrt{(9.1^2 + 3.5^2)} = 9.75$ ohms, in Class AB push-pull 19.5 ohms.

$P_{in} = 20\text{ W} - 28\text{ dB} = 20/630 = 0.032\text{ W}$

V_{RMS} (base to base) $= \sqrt{(0.032 \times 19.5)} = 0.79\text{ V}$

$I_{in} = V_{in}/R_{in} = 0.79/19.5 = 0.04\text{ A}$

$\Delta V4\text{ dB} = \sqrt{[\text{Log}^{-1}(4/10)]} = 1.58\text{ V}$

The parallel capacitors (C3 and C4) should be selected to resonate with R (5.7 ohms) somewhere in the mid-band. At 15 MHz, out of the standard values, 1800 pF appears to be the closest, having a negligible reactance at 2 MHz, and 2.8 ohms at 30 MHz, where most of the capacitive reactance is cancelled by the transformer winding inductance.

Measurements and Performance Data

The output harmonic contents of this amplifier are substantially lower than normally seen in a Class AB system operating at this power level and having a 4.5-octave bandwidth. All harmonics except the third are attenuated more than 30 dB across the band. Between 20 and 30 MHz, -40 to -55 dB is typical. The third harmonic

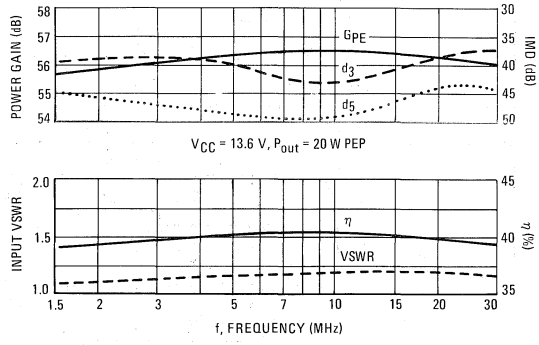


FIGURE 10

Intermodulation Distortion and Power Gain versus Frequency (Upper Curves). Input VSWR and Collector Efficiency (excluding MHW591) (Lower Curves).

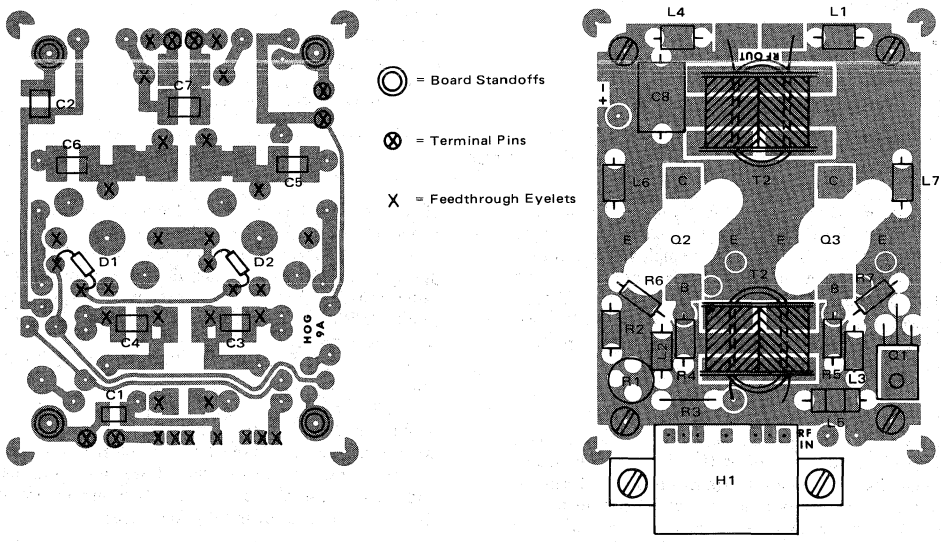


FIGURE 9
Component Layout Diagram of
20 W, 55 dB High-Performance Driver

The leads of D1 and D2 are bent to allow the diodes to contact the transistor mounting flanges.

Note that the mounting pad of Q1 must be connected to the lower side of the board through an eyelet or a plated through-hole.

has its highest amplitude (-20 to -22 dB), as can be expected, below 20 MHz. The measurements were done at an output level of 20 W CW and with 200 mA collector idle current per device. Increasing it to 400 mA improves these numbers by 3–4 dB, and also reduces the amplitudes of d_5, d_7, d_9, and d_{11} by an average of 10 dB, but at the cost of 2-3 dB higher d_3.

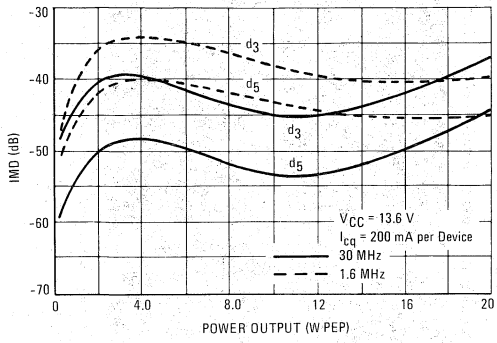


FIGURE 11 – IMD versus Power Output

CONCLUSION

The stability of both designs (excluding the 28 V unit) was tested into reactive loads using a setup described in Reference 8. Both were found to be stable into 5:1 load mismatch up to 7 MHz, 10:1 up to 30 MHz, except the latter design did not exhibit breakups even at 30:1 in the 20-30 MHz range. If the test is performed under two-tone conditions, where the power output varies from zero to maximum at the rate of the frequency difference, it is easy to see at once if instabilities occur at any power level.

The two-tone source employed in all tests consists of a pair of crystal oscillators, separated by 1 kHz, at each test frequency. The IMD (d_3) is typically -60 dB and the harmonics -70 dB when one oscillator is disconnected for CW measurements.

HP435 power meters were used with Anzac CH-130-4 and CD-920-4 directional couplers and appropriate attenuators. Other instruments included HP141T analyzer system and Tektronix 7704A oscilloscope-spectrum analyzer combination.

REFERENCES

1. "Linearized Class B Transistor Amplifiers," IEEE Journal of Solid State Circuits, Vol. SC-11, No. 2, April, 1976.

2. Pappenfus, Bruene and Schoenike, "Single Sideband Principles and Circuits," McGraw-Hill.

3. Reference Data for Radio Engineers, ITT, Howard & Sams Co., Inc.

4. H. Grandberg, "Broadband Transformers and Power Combining Techniques for RF," AN-749, Motorola Semiconductor Products Inc.

5. H. Grandberg, "Measuring the Intermodulation Distortion of Linear Amplifiers," EB-38, Motorola Semiconductor Products Inc.

6. K. Simons, Technical Handbook for CATV Systems, Third Edition, Jerrold Electronics Corp.

7. Data Sheets, Motorola MRF475, MRF476, MRF433, and MHW591

8. H. Grandberg, "Two-Stage 1 KW Solid-State Linear Amplifier," AN-758, Motorola Semiconductor Products Inc.

9. Phillips, "Transistor Engineering," McGraw-Hill.

The PCB layouts below are a supplement to Figures 5 and 9 and may be used for generating printed circuit artwork.

NOTE: The Printed Circuit Board shown is 75% of the original.

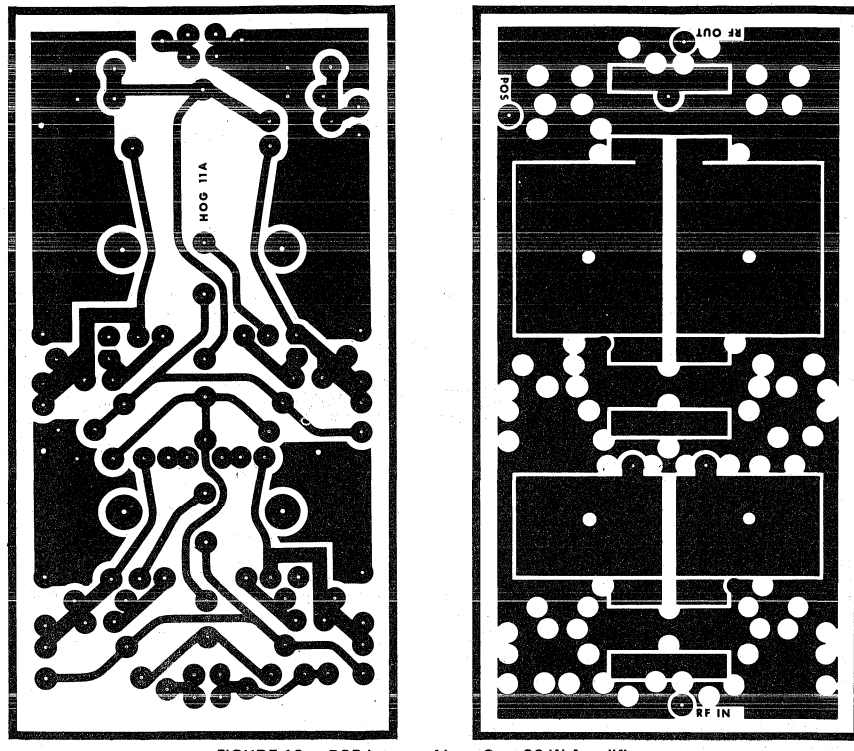


FIGURE 12 — PCB Layout of Low-Cost 20 W Amplifier

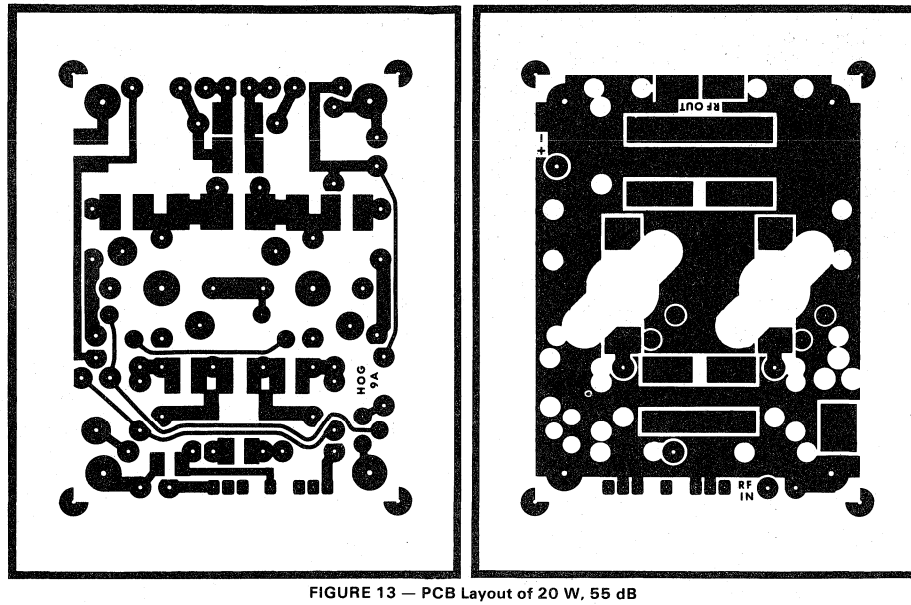


FIGURE 13 — PCB Layout of 20 W, 55 dB
High-Performance Driver

THERMAL RATING OF RF POWER TRANSISTORS

Prepared by:
Robert J. Johnsen

Reliability is of primary concern to many users of transistors. The degree of reliability achieved is controlled by the device user because he determines the stress levels applied by his circuit and environmental conditions. This application note will permit the device user to estimate transistor reliability from the circuit designer's point of view, namely power dissipation and case temperature.

Introduction

The temperature-dependent thermal properties of silicon and beryllium oxide have been measured and documented by many laboratories during the last twenty years. Only in rare cases has this information been disseminated by semiconductor device manufacturers to the users. The purpose of this note is to clarify and correct some long-standing industry-wide assumptions which have been commonly maintained about thermal resistance and high temperature derating.

Most manufacturer's data sheets include a single thermal resistance number ($R_{\theta JC}$) and use this number to calculate a linear derating constant out to some specified maximum junction temperature. The number cited on the data sheet was probably measured in the 25°C to 50°C range, and assumed constant over the whole range of temperatures up to the maximum specified junction temperature. How often have you calculated a junction temperature from a data sheet, as $T_J = T_A + (\theta_{JC})P_D$? Unfortunately, the thermal resistance of silicon increases by 80% from 25°C to 200°C. The thermal resistance of BeO changes by 30%, if the case temperature goes from 25°C to 100°C. Knowledge of the basic physical properties of the materials and the methods used to calculate and measure thermal resistance will assist the device user in transistor selection and equipment design.

NOTE: °K = °C + 273.

Temperature-Dependent Thermal Properties Of Silicon and Beryllia

The temperature-dependent thermal conductivities of silicon and beryllium oxide are seen in Figures 1 through 3 and Table 1. The temperature ranges are somewhat wider than are necessary for typical transistor operation, but are shown to emphasize the wide variation in thermal conductivities. Fulkerson et al[3] tabulate the values for thermal conductivity and resistivity of silicon from 100°K to 1350°K (see Table 1), and they find that the thermal resistivity of silicon as a function of temperature can be estimated by a linear approximation over the temperature range shown.

(400 – 660°K)

$$1/k = -0.1171 + 2.954 \times 10^{-3}\ T\ (^{\circ}K) \quad (1)$$

(600 – 1050°K)

$$1/k = -0.9609 + 4.229 \times 10^{-3}\ T\ (^{\circ}K) \quad (2)$$

A similar least-square fit to Fulkerson's data over the range 200 to 700°K, within 1%, is given by:

(200 – 700°K)

$$1/k = -0.2286 + 3.1683 \times 10^{-3}\ T\ (^{\circ}K) \quad (3)$$

Similarly for beryllia, one can fit the data of Elston et al[2] over the range of 200 to 800°K, with equation (4).

(200 – 800°K)

$$1/k = 1.943 \times 10^{-5}\ T\ (^{\circ}K)^{1.7} \quad (4)$$

where k is the thermal conductivity in units of watts/cm°K.

TABLE 1 — Smoothed Data for Thermal Conductivity and Resistivity of Silicon (Ref. 3)

T (°K)	Smoothed ORNL Values	
	k (W cm^{-1} deg^{-1})	W = 1/k (cm deg W^{-1})
100	7.52	0.133
150	3.88	0.258
200	2.44	0.410
250	1.78	0.563
300	1.40	0.716
350	1.15	0.870
400	0.939	1.065
450	0.825	1.212
500	0.736	1.359
550	0.663	1.508
600	0.604	1.656
650	0.555	1.803
700	0.500	1.999
750	0.452	2.210
800	0.413	2.420
850	0.380	2.634
900	0.351	2.845
950	0.327	3.055
1000	0.306	3.268
1050	0.287	3.479
1100	0.273	3.65
1150	0.261	3.82
1200	0.251	3.97
1250	0.245	4.08
1300	0.241	4.14
1350	0.239	4.18

FIGURE 1 — Temperature Dependent Thermal Conductivity of Silicon (Ref. 1)

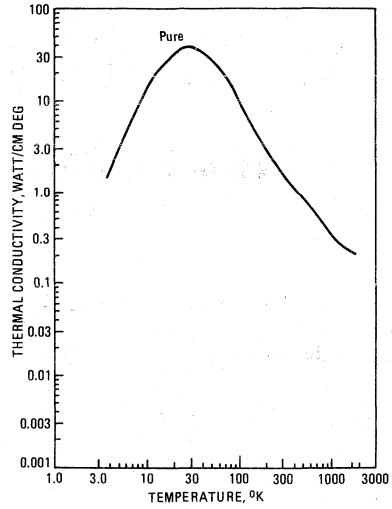


FIGURE 2 — Thermal Conductivity of BeO (Ref. 2)

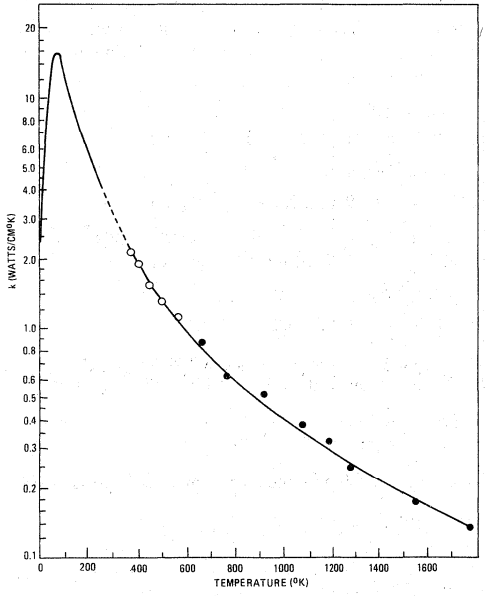
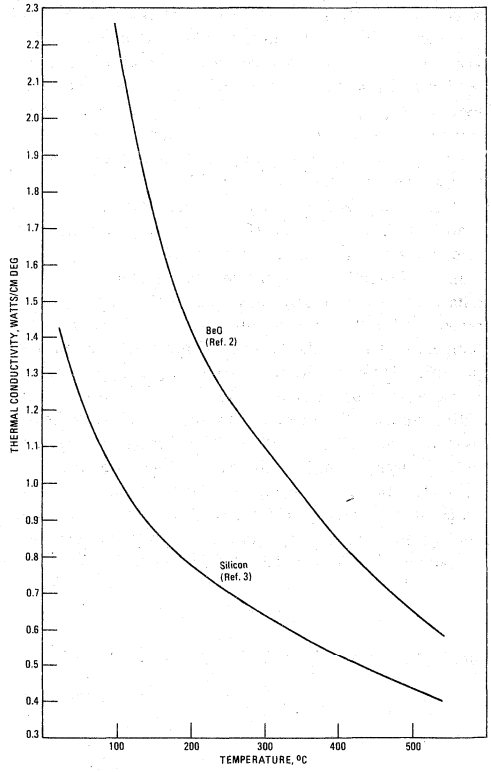


FIGURE 3 — Thermal Conductivity



6

Geometric Factors and Thermal Resistance Calculation

The thermal resistance of most silicon RF transistors is controlled by the bulk properties of silicon and beryllium oxide, geometry of the heat generating (base) areas, and the temperature of the heat sink (case). The interfaces generally are well behaved and contribute little to the overall total thermal resistance if the device, die and package elements are assembled and handled properly.

Die temperature calculations are performed in two steps. The first uses the method of Linsted and Surtey[4] to calculate the temperature distribution of a die by using a double Fourier series solution to Laplace's equation. Figure 4 shows the device geometry and some of the boundary conditions. Equation (5) will calculate the temperature rise at any (x,y,z) point in the die, where A,B,C,D,F are die and heat-generating area boundaries. Q is the heat input in watts, and k is the thermal conductivity of the material in watts/cm^{o}K (Linsted's equation).

$$
\begin{aligned}
T = & -\frac{Q}{K}\left(\frac{CD}{AB}\right)(z-F) \\
& + \sum_{m=1}^{\infty}\left(-\frac{Q}{K}\right)\left(\frac{2BC}{m^2\pi^2A}\right)e^{m\pi z/B}\left(\frac{1-\exp\left[2m\pi(F-z)/B\right]}{1+\exp\left(2m\pi F/B\right)}\right)\left[\sin\left(\frac{m\pi D}{B}\right)\cos\left(\frac{m\pi y}{B}\right)\right] \\
& + \sum_{n=1}^{\infty}\left(-\frac{Q}{K}\right)\left(\frac{2AD}{n^2\pi^2B}\right)e^{n\pi z/A}\left(\frac{1-\exp\left[2n\pi(F-z)/A\right]}{1+\exp\left(2n\pi F/A\right)}\right)\left[\sin\left(\frac{n\pi C}{A}\right)\cos\left(\frac{n\pi x}{A}\right)\right] \\
& + \sum_{m=1}^{\infty}\sum_{n=1}^{\infty}\left(-\frac{Q}{K}\right)\left(\frac{4}{\pi^2mn\gamma}\right)\left(\frac{1-\exp\left[2\gamma(F-z)\right]}{1+\exp\left(2\gamma F\right)}\right) \\
& \cdot e^{\gamma z}\sin\left(\frac{n\pi C}{A}\right)\sin\left(\frac{m\pi D}{B}\right)\cos\left(\frac{n\pi x}{A}\right)\cos\left(\frac{m\pi y}{B}\right)
\end{aligned}
\tag{5}
$$

where

$$\gamma^2 = \pi^2\left[\left(\frac{n}{A}\right)^2+\left(\frac{m}{B}\right)^2\right].$$

The Fourier series solutions are amenable to computer calculation and converge adequately within ten to twenty terms. Figure 5 shows the treatment of multiple base cell transistors. Lines of symmetry between adjacent base cells are considered to be adiabatic die boundaries as assumed by Lindsted. The power dissipated is assumed to be equally shared among the several base cells. The result of this calculation is the temperature rise of the silicon chip, assuming a constant thermal resistance for bulk silicon. The same model is used to calculate the temperature rise for the beryllia piece, using the silicon die area as the power dissipating area for the beryllia, again assuming the thermal resistance of the beryllia as a constant. The thermal resistances of the silicon die and the beryllia substrate are in series, so adding the above numbers gives a value for the thermal resistance of the device at a particular temperature and a power level low enough to avoid the effects of the temperature variations of the respective thermal resistances.

The second step in the thermal resistance calculation takes into account the temperature-dependent thermal resistivity. The calculated thermal resistance of the beryllia piece (from the previous section) is mathematically divided into fifty layers, each with 1/50 of the total BeO thermal resistance. The first layer at the bottom is assumed to have its temperature at the heat-sink ambient with its thermal resistance value corrected to the proper temperature using the equations for the temperature-dependent resistivity. The power flux through the first layer then leads to its temperature rise, and this new temperature determines the thermal resistivity value for the second layer. Its temperature rise is calculated, and so on, until the result for the top surface of the fiftieth layer gives the temperature rise above the ambient for the beryllia piece.

The same method is used for the silicon die, using the beryllia top surface temperature as the starting point, and correcting the thermal resistance of each of fifty layers based upon the temperature of the layer directly beneath it, until the top surface of the silicon die result gives the calculated die temperature for that particular case of ambient temperature and power dissipation. The results of these calculations indicate that the thermal resistance of a given device is not a constant number, but is a function of the dissipated power and the ambient (case) temperature. Another result is that the junction temperature of a device dissipating power will rise more than 1°C for a 1°C rise in ambient temperature, because of the increase in thermal resistance. Figures 6 through 9 show the calculated thermal resistance and die temperature for several different devices as a function of ambient temperature and power dissipation.

FIGURE 4 – Model for Heat Flow

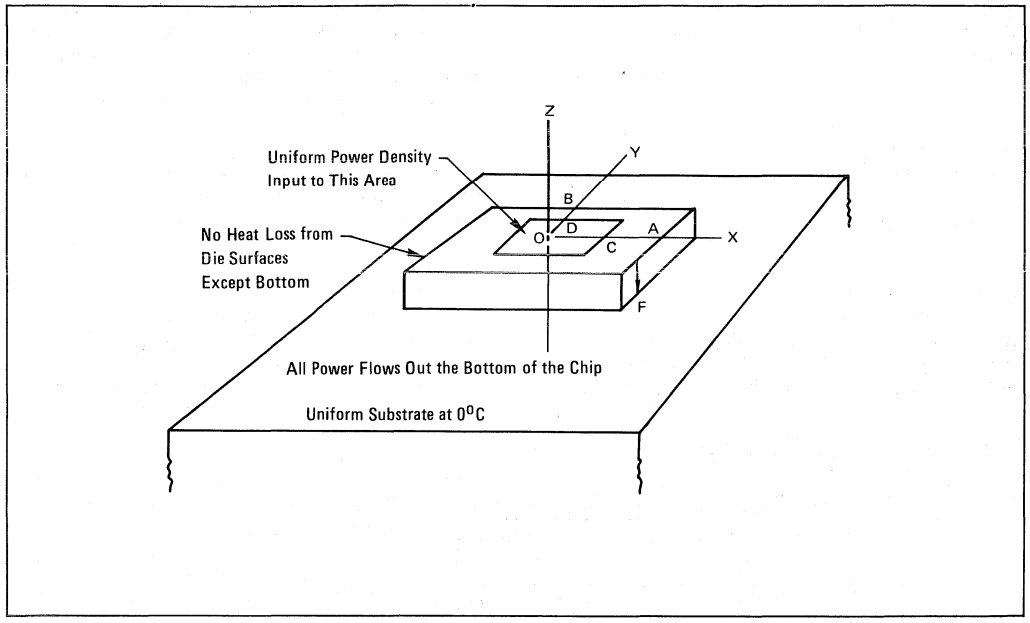
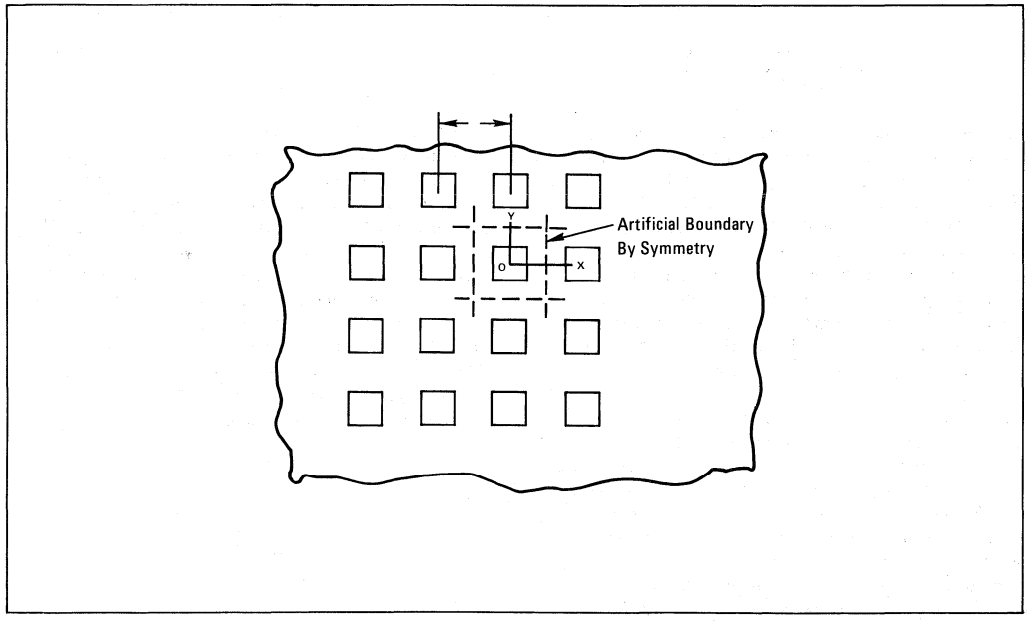


FIGURE 5 – Array of Base Areas in a Silicon Die



6

FIGURE 6 – Junction Temperature and Thermal Resistance as a Function of Power Dissipated, Flange (Heat Sink) Temperature

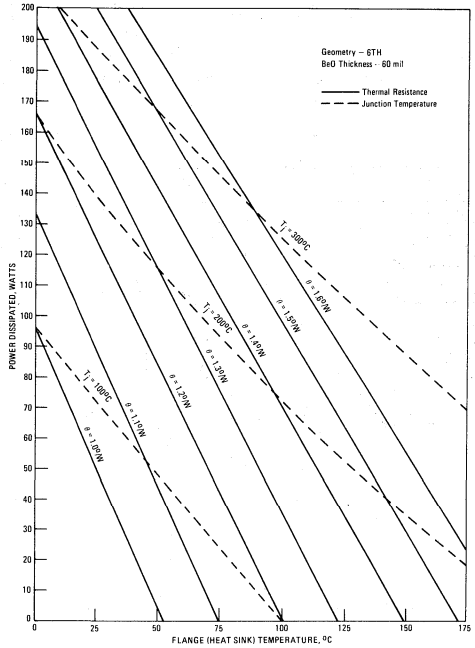


FIGURE 7 – Junction Temperature and Thermal Resistance as a Function of Power Dissipated, Flange (Heat Sink) Temperature

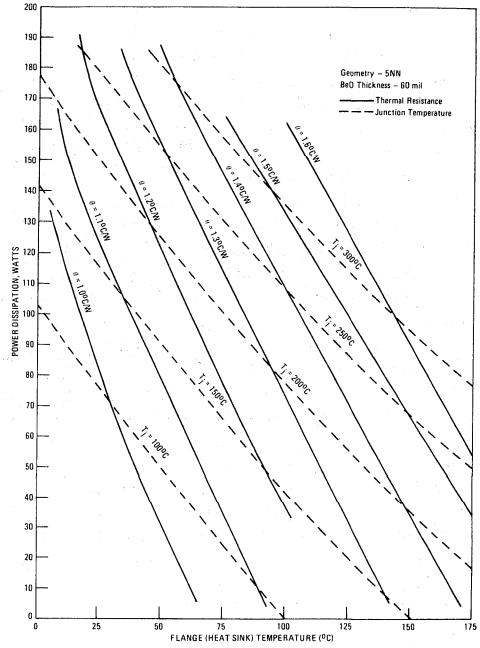


FIGURE 8 – Junction Temperature and Thermal Resistance as a Function of Power Dissipated, Flange (Heat Sink) Temperature

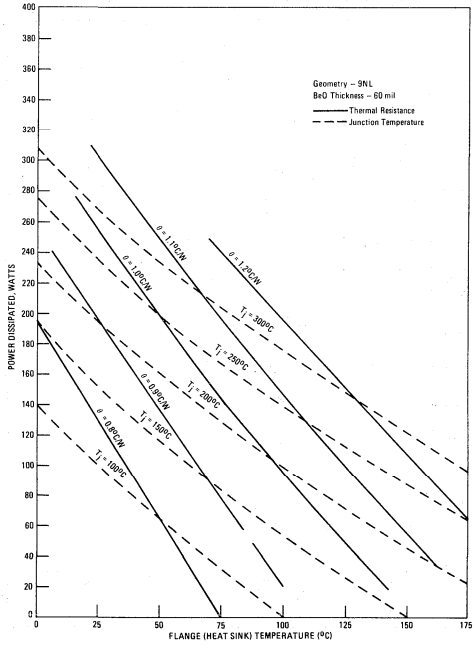
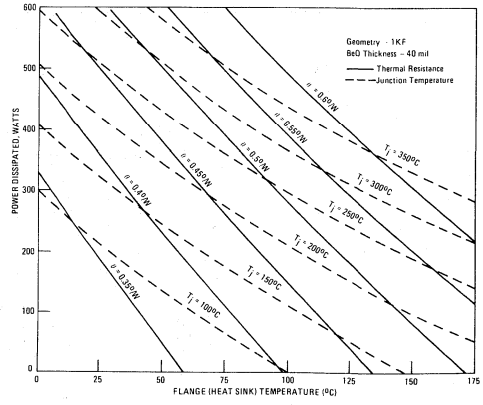


FIGURE 9 – Junction Temperature and Thermal Resistance as a Function of Power Dissipated, Flange (Heat Sink) Temperature



6

Experimental Verification Of Calculated Die Temperature

Actual temperature measurements are made with an infrared microscope, Barnes Eng. Co. Model RM2A. This instrument uses an indium antimonide diode photodetector at liquid nitrogen temperatures to measure the infrared radiance emitted from a 1.5 mil spot on the surface being examined. The IR radiance versus temperature curve is calibrated by measuring the radiance at various known temperatures monitored by a calibrated thermocouple while the device is heated by external means. An experimental calibration is necessary because the radiance output of the device at a given temperature is a function of the average emissivity in the area seen by the microscope, and this average emissivity is a function of the geometry and processing history of the device in question. The effective emissivity depends upon the relative amounts of metal and silicon and the infrared transparency of the varying thicknesses of SiO_2 glass in the field of view. The calibration data of radiance versus temperature can be least-squares curve fit to an equation of the form $T = (A)(R)^b$, where A and b are the fitted constants, and R the measured radiance.

The device is then powered up in its circuit, and the radiance data collected point-by-point around the surface of the silicon die. A computer program inputs the array of radiance data, calculates the actual temperature from the calibration equation, and prints a map of the temperature profile, as well as some statistical information about the temperature distribution.

Figures 10 through 12 are plots showing the correlation of measured to calculated temperature for several geometries, under various conditions of flange temperature (30°C to 150°C), supply voltage, drive power, and

FIGURE 10 – Actual vs Calculated Die Temperatures

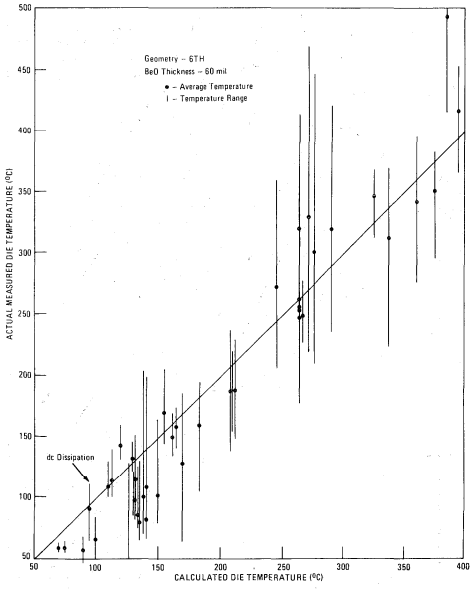


FIGURE 11 – Actual vs Calculated Die Temperatures

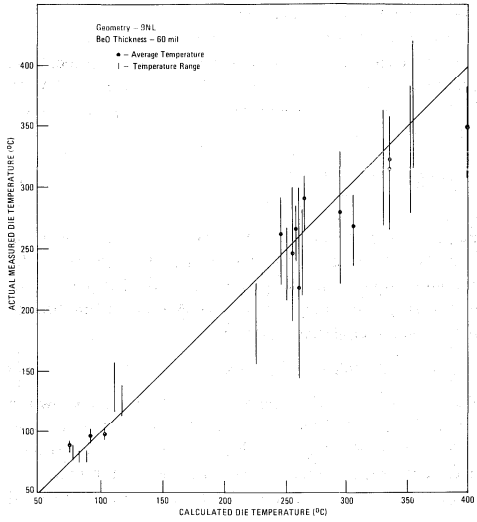
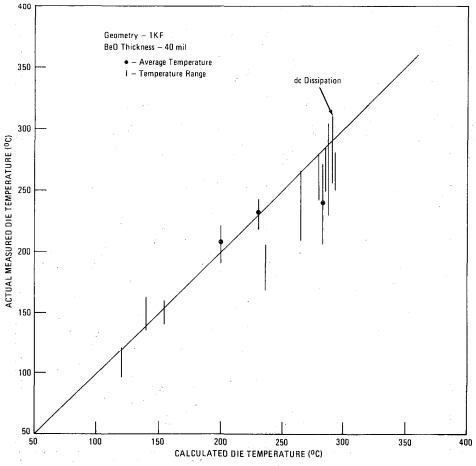


FIGURE 12 – Actual vs Calculated Die Temperatures



output load magnitude and phase angles from 50 Ω to over 30:1 VSWR. The calculated temepratures seem to be somewhat higher than measured at the higher power levels. The calculated temperatures are based on the calculated power dissipation, disregarding RF losses in the actual loads and circuits.

Metal Migration and Mean Time to Failure

The calculated/observed temperature agreements are seen to be close enough so that the calculated temperature can be used as the basis for reliability calculations of Mean Time Before Failure (MTBF) for metal migration based upon Black's[5] work.

$$\text{MTBF} = \frac{(\text{cross section})^3}{I^2 \cdot f(T^o)} \qquad (6)$$

Equation (6) is the equation used for calculating metal migration lifetime, where the cross section refers to the conducting stripe dimensions in cm^2, and I is the current in the stripe in amps. $f(T^o)$ is an Arrhenius function of the stripe material, having the form:

$$f(T^o) = B \exp(-\phi/KT) \qquad (7)$$

The material dependent parameters B and ϕ are shown in Table 2. K is Boltzman's constant, and T is in degrees Kelvin. A series of graphs (Figures 13 through 16) have been constructed, one for each device, that present the results of the calculations of device temperature and MTBF as a function of power and ambient temperature.

The temperature lines are valid for any combination of supply voltage, efficiency and drive power, by reading the power axis as power dissipated. The MTBF lines, because of the current dependence, have been constructed based upon the assumptions of 12.5-volt supply and 50% efficiency, so that the power axis should be interpreted as output power. It is possible to use the MTBF set of lines at other conditions. Enter the graphs by reading the power output parameter as power dissipated, and find the MTBF, then scale the MTBF by the ratio square of the $\eta = 50\%$ current to the actual current.

$$\text{MTBF} = \text{MTBF (from graph)} \times \left(\frac{I\,@\,\eta = 50\%}{I \text{ actual}}\right)^2 \qquad (8)$$

TABLE 2 – Material Dependent Parameters

Material	B	ϕ
Large Crystal Glassed Al (Ref. 5)	8.5×10^{-10}	1.2
Al-2% Cu Alloy (Ref. 6)	7.9×10^{-17}	0.6

FIGURE 13 – Metal Migration – MTBF

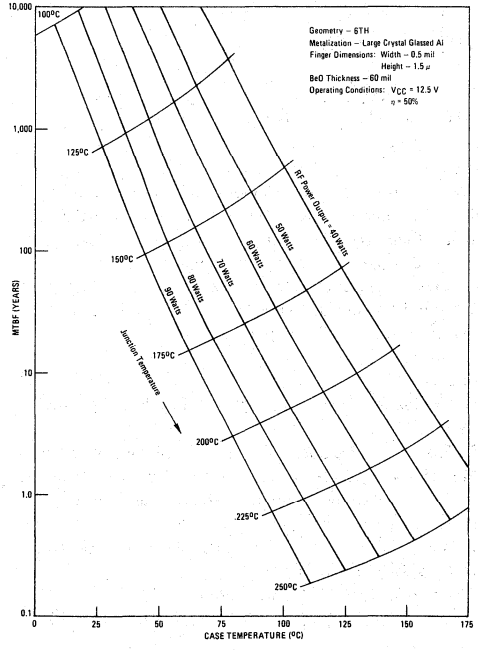


FIGURE 14 – Metal Migration – MTBF

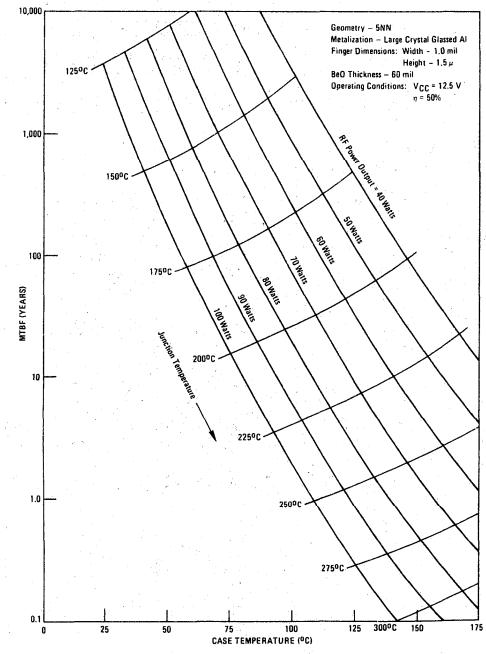


FIGURE 15 – Metal Migration – MTBF

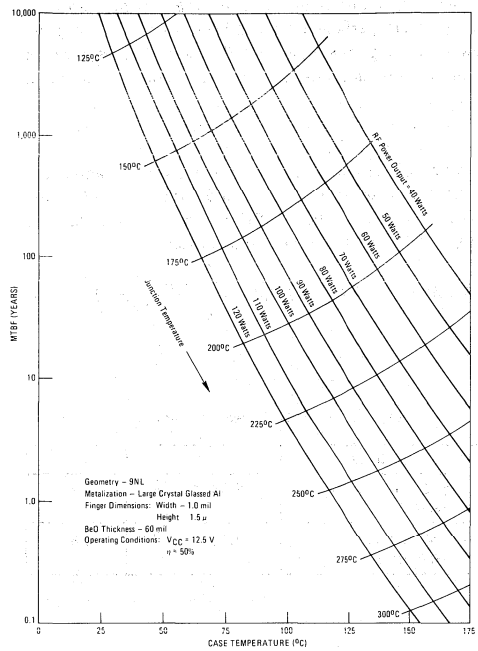


FIGURE 16 – Metal Migration – MTBF

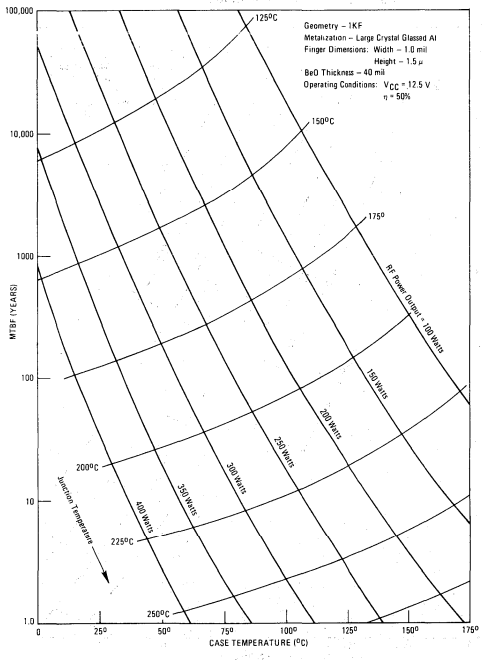


FIGURE 17 – Geometry Code to Standard Part Cross-Reference

Geometry Code	12.5	28		50	V_{CC} (V)
	Al	Al	Au	Al	Metal
1KF	MRF421	MRF422		MRF428A	
5NN	MRF243 MRF453/A MRF455/A MRF460		MRF316		
9NL	MRF245 MRF454/A	MRF463 MRF464/A	MRF317		
6TH	MRF648		MRF327 MRF328		

To Scale Metal Migration MTBF From 12.5 V to Other Operating Voltages

Keeping P_D and η constant, then the current for 28 V operation compared with that for 12.5 V operation is given by:

$$I_{12.5} \times 12.5 = I_{28} \times 28$$

$$\frac{I_{12.5}}{I_{28}} = \frac{28}{12.5}$$

From Black's[5] equation:

$$MTBF \propto \frac{1}{I^2}$$

For like geometries, the ratio of the MTBF at 28 V to the MTBF at 12.5 V is:

$$MTBF_{28} = MTBF_{12.5} \times \left(\frac{28}{12.5}\right)^2$$

$$MTBF_{28} = MTBF_{12.5} \times 5.02$$

Similarly, for 50 V operation:

$$MTBF_{50} = MTBF_{12.5} \times 16.$$

Conclusion

We have discussed the elements of thermal resistance and metal migration lifetime with particular attention paid to their variation with temperature as functions of power dissipation and ambient temperature.

Graphical presentations of the results are included which should be useful to the device user who is interested in better reliability in his application.

References

1. G. A. Slack, Journal of Applied Physics, 35, 3462, 1964.
2. J. Elston, J. DeGoer, and Z. Mihailovic, J. Nucl., Mater., 11, 333, 334, 1964.
3. Fulkerson, Moore, Williams, Graves, and McElroy, Phys. Rev., 167, 768–780.
4. Linsted and Surtey, IEEE Transactions on Electron Devices, ED-19, 42, 1972.
5. Black, Proc. IEEE, 57, 1587, 1969.
6. Hall, ECOM, DAAB07-70C 0164, October 1971.

6

A SIMPLIFIED APPROACH TO VHF POWER AMPLIFIER DESIGN

Prepared by
Helge O. Granberg
RF Circuits Engineering

This note discusses the design of 35-W and 75-W VHF linear amplifiers. The construction technique features printed inductors, the design theory of which is fully described. Complete constructional details, including a printed circuit layout, facilitate easy reproduction of the amplifiers.

Solid-state VHF amplifier design can be simplified by employing printed or etched lines for impedance matching. The lines, having a distant ground-plane reference and high Z_O, can be treated as lumped constant inductors, and make design and duplication easier than with wire-wound inductors.

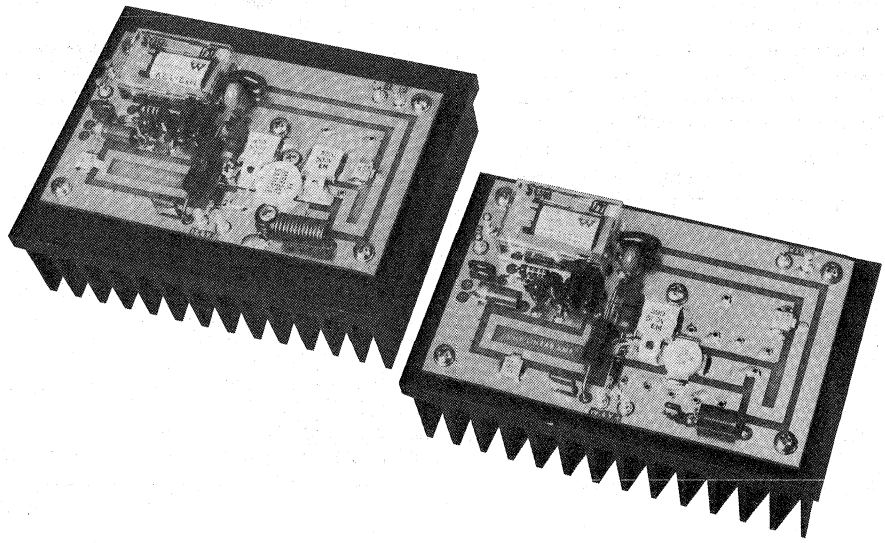
An example is an optimized 35-W amplifier which yields over 10 dB of power gain across the 2-meter amateur band. It employs an inexpensive, non-internally matched transistor, the MRF240, which has good linear characteristics for SSB operation.

A higher power version with the same board layout is concentrated around the MRF247, although this results in some compromise in the impedance matching.

A carrier operated T/R switch (COR) is incorporated, allowing applications such as a booster amplifier for hand-held and mobile radios.

Both designs are biased class AB for linear operation, but are suitable for FM operation as well. Figure 1 shows the two amplifiers.

FIGURE 1 – 35-watt and 75-watt Engineering Models



GENERAL

VHF solid state amplifier design is almost exclusively done with lumped constant LC matching networks. Broadband transformer matching is feasible when extremely wide bandwidths are required. Transmission lines for impedance transformation usually require quarter-wave electrical lengths and make designs bulky at VHF unless materials with high dielectric constant are used. Transmission lines can be realized with coaxial cable or printed lines (strip-lines) on a circuit board with a continuous ground plane, separated by a suitable dielectric material. The printed airlines discussed here are, in fact, high characteristic impedance transmission lines which, for the purposes of design calculation, are treated as inductors; therefore the quality of the board material is less critical. The printed airlines also have the advantage of repeatability and easy access for designing multi-element networks. The network calculations can be done in the same manner as if lumped-constant, round-wire inductors were used.

Input and output impedance matching in transistor amplifiers is required to transform the source impedance (usually 50 ohms) to the low complex input impedance of the device. The output load impedance, which is a function of the supply voltage and power level, must also be matched to a 50-ohm load except in multistage driver designs.

At VHF, the input and output impedances of a power transistor are both usually inductive in reactance (designated as +JX in data sheets), becoming capacitive (-JX) at lower frequencies. For transistors such as MRF240, 2N6084 and 2N5591, the crossover point is around 100 MHz. This is determined by the transistor die size, geometry and package type, and smaller devices can be capacitive up to UHF frequencies.

Since the bandwidth required here is only a fraction of an octave, (140-150 MHz) the impedance matching can be adequately done with two section networks. In Figure 2, X_1, which represents the +J input of the MRF240 transistor is not part of the external input matching network. C_1 and C_6 are dc blocking capacitors with measured parasitic inductances of close to 12 nH at the center frequency when the lead lengths are 0.1 inch. These inductances, as well as the relay inductance, are added to the values of L_1 and L_5.

If the relay were used in a 50-ohm system, it would result in 0.3 dB power loss due to impedance mismatch and losses. This can be minimized if the relay inductance is used as part of a resonant circuit, but the series inductance (37 nH per contact pair) obviously places an upper frequency limit.

The simplest approach to matching network design is with a purely resistive source and load. This can be accomplished by compensating the +J with an equal amount of capacitance (−J). C_3 and C_4 are used to accomplish the compensation in Figure 2. This is not always practical, however, especially when maximum bandwidths are required. In this case, only part of the inductive component may be cancelled, leaving the base and collector still inductively reactive. In either case, it may be considered that part of the impedance-matching occurs within the device package itself; this is more obvious with internally matched devices, which are discussed later.

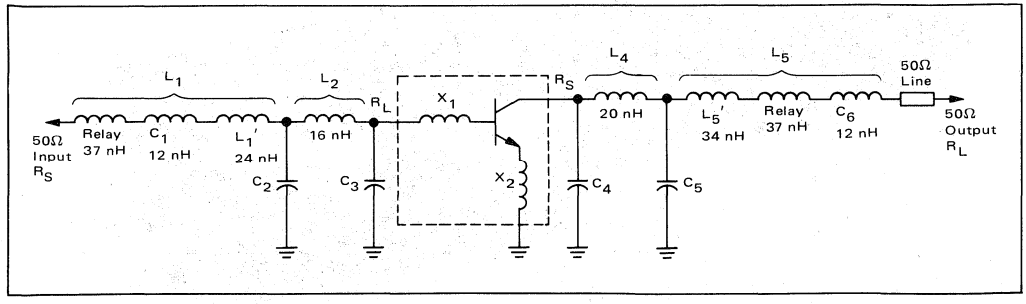
35-W LINEAR AMPLIFIER

The MRF240 was chosen for this application due to its ruggedness against load mismatch and inherently high power gain for a non-internally matched device. The transistor is rated for an output power of 40 W and a power gain of 8 dB at 175 MHz. A typical power gain at 145 MHz is 10 to 11 dB. At this frequency the input and output impedances of the MRF240 are 0.6 +J 0.8 ohms and 2.0 +J 0.1 ohms respectively (P_{out} = 35 W).

Before designing the matching networks, the values of C_3 and C_4 must be established to cancel the inductive reactance components at the base and the collector. For the input, the series numbers 0.6 +J 0.8 must be converted to parallel equivalent values, either by using a Smith chart or equations in references 3 and 4. The resulting equivalent values are: R_P = 1.67 ohms, X_P = 1.25 ohms or 880 pF.

All capacitors have a series inductive reactance component, normally called parasitic inductance. It could be only a fraction of a microhenry, but at VHF its effect is large enough to be taken into consideration. The para-

FIGURE 2 – Impedance Matching Network for 35 watt VHF Amplifier



sitic inductance results in an increased effective value of capacitance, and is frequency and impedance-level dependent.

The unencapsulated mica capacitors, widely used in VHF power applications, range from 1 to 2 nH in parasitic inductance for a single plate type, (up to 360 to 390 pF nominal values) depending on the mounting technique. Assuming a parasitic inductance of 1.5 nH, the equivalent low-frequency value can be calculated with Equation 1 as:

$$C_{Equiv} = \frac{C}{1 + [(2\pi f)^2\ LC]\ 10^{-9}} \quad (1)$$

where C = effective capacitance required in pF
L = parasitic inductance in nH
f = frequency in MHz

Substituting the values in equation (1):

$$C_{Equiv} = \frac{880}{1 + [(910)^2 \times 1.5 \times 880]\ 10^{-9}} = 420\ pF$$

Thus, for the required 880 pF, a capacitor of this type with equivalent low-frequency value of 420 pF, or the closest standard (390 pF), should be used.

Similarly, converting the output impedance (2.0 +J 0.1 ohms) to parallel form, R_P = 2.01 ohms and X_P = +J 26.8 ohms. The X_C represents a capacitance value of 47 pF for C_4 (from Equation 2), or a 43 pF nominal value.

$$C = \left(\frac{\frac{1}{X_C}}{2\pi f}\right) 10^6 \quad (2)$$

where X_C = capacitive reactance in ohms
C = capacitance in pF
f = frequency in MHz

This high reactance in parallel with the low collector impedance had no noticeable effect and was completely omitted in later functional tests of the unit. It would be easy to see from a Smith chart that the resistive components of 1.67 ohms and 2.01 ohms remain unchanged, and can be treated as a purely resistive load and source for the matching network calculations.

At high frequencies the base-emitter impedance of the transistor die itself is always lower than the collector output impedance. With power devices, both can be only a fraction of an ohm. The input impedance is increased by the base and emitter bonding wire and package lead frame inductances, which are effectively in series with the transistor base (Figure 2, X_1 and X_2). The collector has normally much less series inductance since it is attached directly to the package bonding pad.

From this it can be seen that part of the matching network is actually built into the transistor package, and it is obvious that the amplifier bandwidth cannot be accurately determined by calculating the Q values of the external matching networks. (See the discussion of a 75-W linear amplifier.)

As an approximation, the 3 dB bandwidth can be used to obtain a starting point. Assuming a 15 MHz bandwidth at ±1.5 dB is desired at 145 MHz center frequency, a loaded Q of approximately 9 is required. For simplicity this number is applied to both input and output network design.

In Figure 2, X_1 and X_2 represent the inductive impedance component of the transistor and are shown only to give an idea of the transistor internal structure. The values of L_1, L_2 and C_2 can be obtained from the Appendix, or calculated by using Equation 3:

$$XL_1 = R_S B$$

$$XL_2 = R_L Q$$

$$XC_2 = \frac{A}{Q + B} \quad (3)$$

$$A = R_L (1 + Q^2)$$

$$B = \sqrt{\frac{A}{R_S} - 1}$$

where R_S = source impedance
R_L = load impedance

For Q = 9:

$$XL_1 = R_S B = 50 \times 1.32 = 66\ ohms$$

$$XL_2 = R_L Q = 1.67 \times 9 = 15\ ohms$$

$$XC_2 = \frac{A}{Q + B} = \frac{137}{9 + 1.32} = 13.3\ ohms$$

$$A = 1.67\ (1 + 9^2) = 137$$

$$B = \sqrt{\frac{A}{50 - 1}} = 1.32$$

where R_S = 50 ohms, R_L = 1.67 ohms

Since $L = \left(\frac{XL}{2\pi f}\right) 10^3$ (4)

where XL = inductive reactance in ohms
L = inductance in nH
f = frequency in MHz

we have from Equations 3 and 4:

L_1 = 73 nH
L_2 = 16 nH
C_2 = 82 pF

Subtracting the relay inductance (37 nH) and the parasitic inductance of the blocking capacitor C_1 (12 nH) from the total value of L_1, $L_1' = 24$ nH. This means the total printed line inductance must be $L_1' + L_2 = 24 + 16 = 40$ nH.

Calculating the values of the output network in a similar manner, the values for L_4, L_5 and C_5 are obtained as 20 nH, 83 nH and 70 pF, respectively, and L_5' becomes 34 nH.

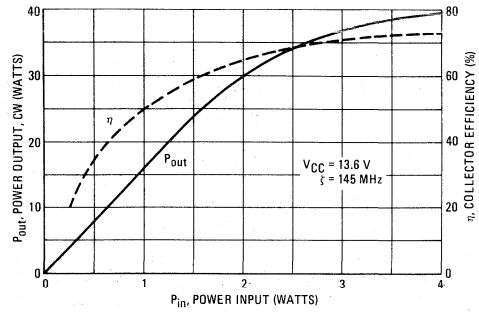
The capacitors employed for C_2 and C_5 are of the same unencapsulated mica type as C_3, but smaller in size, and their parasitic inductance is only about 1 nH. The equivalent values for C_2 and C_5 would then be 77 pF and 66 pF according to Equation 1. These are nonstandard values, and considering a 5% tolerance, a 68 pF marked value can be used for both.

Inductors L_1, L_2, L_4 and L_5 are comprised of etched lines on the circuit board. To determine their widths and lengths, the inductance of each line per unit length must be established. From the tables in the Reference section, it can be extrapolated that the inductance of #25 round wire is 24 nH per inch and #26 wire nearly 26 nH per inch. When a ground plane is 0.15 inch below, which in this case is the heat sink, and the side grounds are off an equal distance, the inductance is about one-half of this, which has been verified by measurement.

If the circuit board is made of 1-ounce, copper-clad material, (one ounce of copper per one square foot) the copper thickness is 1.4 mils. With a one mil solder plating, the total thickness is 2.4 mils, and a 100-mil-wide strip would be equivalent to a #26 round wire having a 240 square mil cross sectional area. Similarly, a 130-mil-wide strip would be equivalent to a #25 round wire with 312 square mil area. A wider line would have lower losses but would also be physically longer for a given inductance. As a compromise, a narrow line was used for the input in this design, and a wider line for the output, where the losses due to the high RF currents are more evident. Bends in the line have a minimal effect to the inductance compared to the presence of the ground plane.

From the above, the resulting inductances for the 100 mil and 130 mil lines are 13 nH per inch and 12 nH per inch, respectively. This means that for $L_1 + L_2$ a total length of 3.1 inches is required, and 4.4 inches for $L_4 + L_5'$. Then, for L_2 = 16 nH, C_2 should be located 1.3 inches from the transistor base along the input line. For L_4 = 20 nH, C_5 should be 1.6 inches from the collector along the output line. The Power Output and Efficiency vs. Power Input of the 35-W amplifier is shown in Figure 3.

FIGURE 3 – Power Input vs. Power Output and Collector Efficiency of 35-W Amplifier

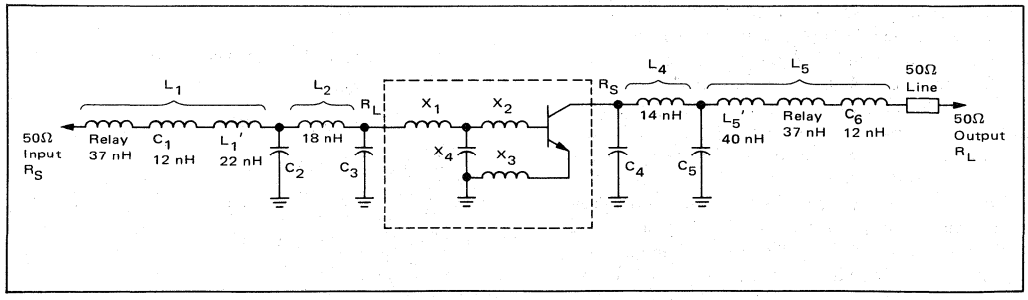


75-W LINEAR AMPLIFIER

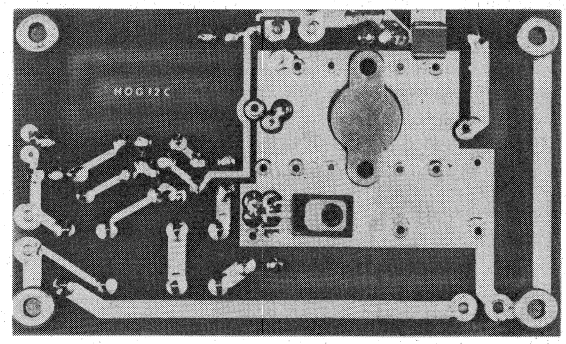
The MRF247 employed in this design is a version of the well-known MRF245, which has been reprocessed to improve the linear characteristics. It is a much larger device than the MRF240, resulting in lower input and output impedances. However, it employs internal base matching with a built-in MOS capacitor to bring the base impedance up to a level where external low loss matching networks can be realized.

In Figure 4 the dashed line encircles the specially designed T matching network, including the metal oxide capacitor X_4. X_1, X_2, and X_3 represent the bonding wires whose inductances can be varied by controlling the loop heights. This network will be part of the total matching network designed to match the transistor to function in a practical circuit.

FIGURE 4 – 75-Watt Amplifier Impedance Matching Network



Underside View of 75-W Amplifier



The internal matching still leaves the input impedance inductively reactive.

The MRF247 input impedance under forward biased conditions (100 mA) is 0.45 +J 0.85 ohms at 145 MHz, which translates to 2.06 +J 1.08 ohms in parallel form. A capacitive reactance of -J 1.08 ohms, converting to 1018 pF is required for C_3. The nominal value equivalent value, using Equation 1, is obtained as 450 pF.

Since the remaining resistive component of the base impedance (2.06 ohms) is only slightly higher than that of the MRF240, only minor changes in the input matching network are necessary. When $L_1 + L_2$ is fixed, and only their ratio can be varied, the resulting Q will be lower for the increased R_L. If only $L_1 + L_2$ is known, the Q can be calculated with Equation 5 as:

$$Q = \frac{[4X_T^2 + (R_S^2/R_L + X_T^2/R_L - R_S)\,4(R_S - R_L)]^{1/2} - 2X_T}{2(R_S - R_L)} \qquad (5)$$

where

$X_T = XL_1 + XL_2$ or $XL_4 + XL_5$

R_S = source impedance

R_L = load impedance

Reverse for output network calculations

Therefore,

$$Q = \frac{\sqrt{[26244 + (1214 + 3185 - 50)\,(192)]} - 162}{95.88}$$

$$Q = \frac{928 - 162}{95.88} = 7.99$$

$Q = 8$

where

$X_T = XL_1 + XL_2 = 81$ ohms

$RS = 50$ ohms

$RL = 2.06$ ohms

Then, with Equations 1, 2, 3 and 4, the values for L_1, L_2 and C_2 can be calculated as: $L_1 = 71$ nH, $L_2 = 18$ nH, $C_2 = 63$ pF (56 pF nearest standard). The position of C_2 will be approximately 1.6 inches from the transistor base. (See line inductance calculations in the discussion for the 35-watt amplifier.)

The measured output impedance of MRF247 is 0.65 +J 0.45 ohms, which is much lower and more reactive than the values shown for MRF240. The output matching must also be done with the existing total line inductance, $(L_4 + L_5)$ and it can be expected that a higher factor of compromise in the output matching is evident regarding the network bandwidth.

The above impedance numbers convert to 0.96 ohms resistive and -J 1.39 ohms reactive in parallel form. Since -J 1.39 ohms = 790 pF, a nominal value of 400 pF (C_4) is required at the collector. To find the Q:

$X_T = 94$ ohms $(XL_4 + XL_5)$

$R_S = 0.96$ ohms

$R_L = 50$ ohms

Then:

$Q = 13.7$ (Eq. 5), and:

$L_4 = 13$ ohms = 14 nH

$L_5 = 81$ ohms = 89 nH

$C_5 = 11.8$ ohms = 93 pF

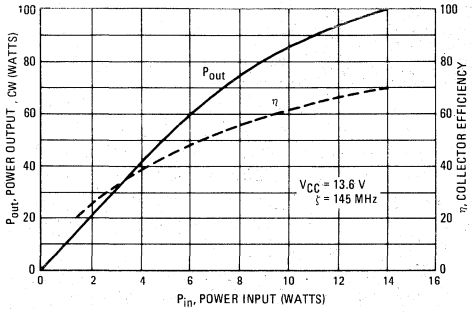
A practical value of 82-91 pF can be used for C_5, and it should be located 1.1 inches along the output line from the collector, to give the above inductance values for L_4 and L_5.

Although the output Q is higher than the value calculated earlier for the 40 W unit, the total bandwidth of this version is increased as shown in Figure 7. The input matching network is usually dominant in determining the total bandwidth since the impedance transformation required is greater than the output requires, although the output circuit also has secondary effect. The internal matching elements of the device further make the total

6

effective Q even lower than the calculated value, which in this case was 8. The higher output Q usually results in higher collector efficiency and better harmonic suppression, but at the same time the circulating RF currents will increase, resulting in higher overall circuit losses which is especially noticeable at increased power levels. These factors are difficult to determine without knowing all the internal transistor parameters.

FIGURE 5 – Power Input vs. Power Output and Collector Efficiency of 75-W Amplifier



CLASS AB BIASING AND OTHER CONSIDERATIONS

The biasing system, as seen in Figure 6, uses a forward biased transistor, Q_2, to provide a voltage source of 0.6 to 0.7 volts. When the collector is connected to the base, a second current path is formed, decreasing the base current according to the h_{FE}, and thus lowering the voltage drop across the base-emitter junction. In this manner the voltage drop can be adjusted by selecting the appropriate h_{FE} for Q_2. For the 2N5190 series h_{FE} is typically in the range of 80–100, although the minimum spec is 20–25.

Typical h_{FE}'s for the MRF240 and MRF247 are 50–60, and the worst case collector currents around 4A and 9A respectively. The minimum base currents required, $I_E(Q_2)$ are 80 mA and 180 mA (I_C/h_{FE}).

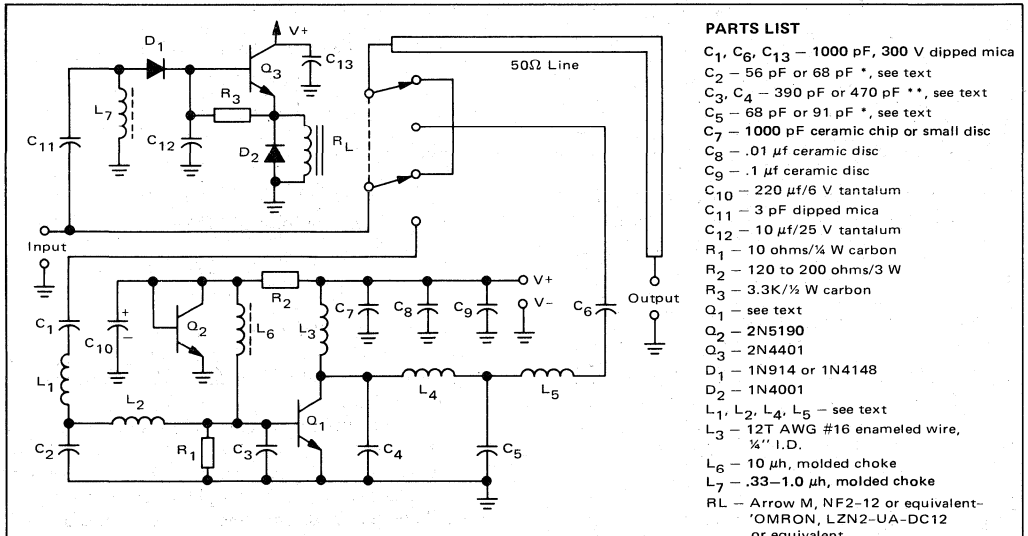
$$R_2 = \frac{V_{CC} - V_{BE}(Q_2)}{I_E(Q_2)} = 160 \text{ ohms and } 75 \text{ ohms.}$$

The bias, which should not exceed 50 mA for MRF240 and 150 mA for MRF247, can be further adjusted by varying the value of R_2, but the minimum $I_E(Q_2)$ should be maintained.

It should be noted that since Q_2 is attached to the heat sink for temperature tracking purposes, its collector must be electrically isolated from the ground. The anodized surface of the heat sink is normally sufficient, or a separate insulating washer can be employed.

The 0.3 dB relay insertion loss mentioned earlier amounts to a VSWR of 1.7:1. However, the reflected power is only 0.2% (VSWR = 1.1:1) in a straight-through mode (receive), indicating that most of the relay losses are due to contact resistance and the dielectric insula-

FIGURE 6



PARTS LIST

C_1, C_6, C_{13} – 1000 pF, 300 V dipped mica
C_2 – 56 pF or 68 pF *, see text
C_3, C_4 – 390 pF or 470 pF **, see text
C_5 – 68 pF or 91 pF *, see text
C_7 – 1000 pF ceramic chip or small disc
C_8 – .01 μf ceramic disc
C_9 – .1 μf ceramic disc
C_{10} – 220 μf/6 V tantalum
C_{11} – 3 pF dipped mica
C_{12} – 10 μf/25 V tantalum
R_1 – 10 ohms/¼ W carbon
R_2 – 120 to 200 ohms/3 W
R_3 – 3.3K/½ W carbon
Q_1 – see text
Q_2 – 2N5190
Q_3 – 2N4401
D_1 – 1N914 or 1N4148
D_2 – 1N4001
L_1, L_2, L_4, L_5 – see text
L_3 – 12T AWG #16 enameled wire, ¼" I.D.
L_6 – 10 μh, molded choke
L_7 – .33–1.0 μh, molded choke
RL – Arrow M, NF2-12 or equivalent-'OMRON, LZN2-UA-DC12 or equivalent

Elecromotive Corp. (ELMENCO) *Type MCM01/010
Lauter Avenue **Type EMJ10
Florence, S.C. 29501

Standex Electronics *Type 3HS0006
P.O. Box 67 **Type J-101
Casey, Ill. 62420

tion resistance, rather than impedance mismatch.

Both amplifier designs may be employed in FM applications without modification. The bias networks may be omitted and L_6 connected to ground, which modifies the operation to Class C. The increased input impedance of the device operating class C results in increased input VSWR, but it will still remain less than 1.5:1 for the 145–150 MHz band.

FIGURE 7 – IMD vs. Power Output

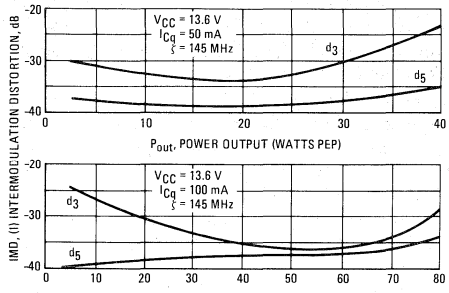
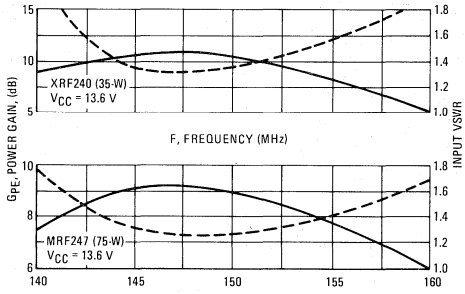


FIGURE 8 – Power Gain and VSWR vs. Frequency



The two amplifiers may be connected in cascade to provide a total power gain of around 20 dB; however, an attenuator of 4 to 6 dB is required between the two units to prevent overdrive of the MRF247. Since 10 to 20 watts will be dissipated in the attenuator, it cannot be built from discrete resistors. Most convenient, size and costwise, are the thin film attenuators such as those manufactured by Pyrofilm.

The COR circuit requires 400 to 500 mW for the relay to switch. At this drive level, without the attenuator, the second amplifier would already produce full power output.

The COR (Figure 5) incorporates one of the standard circuits popular with mobile add-on amplifiers. Part of the RF input signal is being rectified by D_1. The dc turns on Q_3 which activates the relay. L_7 and R_3 provide the bias for D_1 and Q_3, and D_2 suppresses inductive transients produced by the relay coil inductance. A time constant for SSB operation is provided by C_{12}, whose value can be changed according to individual requirements. For FM this capacitor can also be omitted along with the bias network.

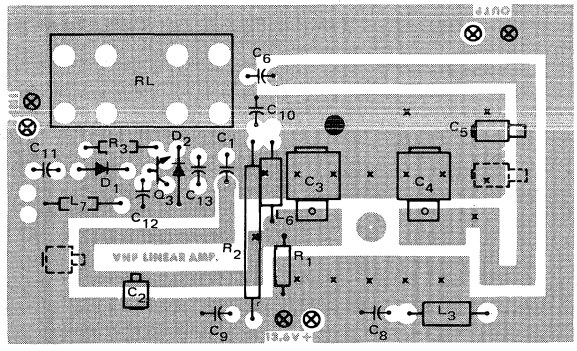
The repeatability of these amplifiers has been proven by constructing more than half a dozen units. Capacitors C_2 and C_5 were simply located within the marked areas on the circuit board (see Figure 9 and the photograph). On these capacitors, 20% tolerances can be allowed, but this may result in adjustments of each individual unit for optimum performance.

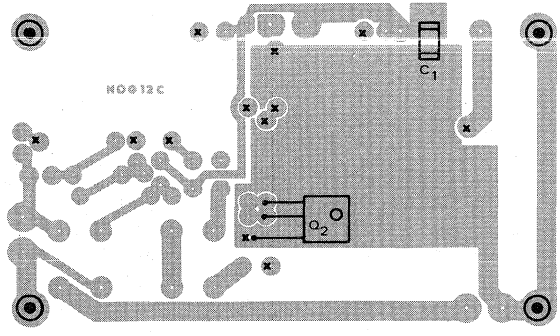
References

1. Frederick Emmons Terman, Sc. D. Radio Engineers Handbook, McGraw - Hill Co., Inc., 1943
2. Donald Kochen, Practical VHF and UHF Coil Winding Data, *Ham Radio,* April 1971
3. Davis, "Matching Network Design with Computer Solutions," AN-267, Motorola Semiconductor Products Inc. (See appendix).
4. Becciolini, "Impedance Matching Networks Applied to RF Power Transistors," AN-721, Motorola Semiconductor Products Inc.

6

FIGURE 9 – Component Layout Diagram of 35W and 75W Amplifiers





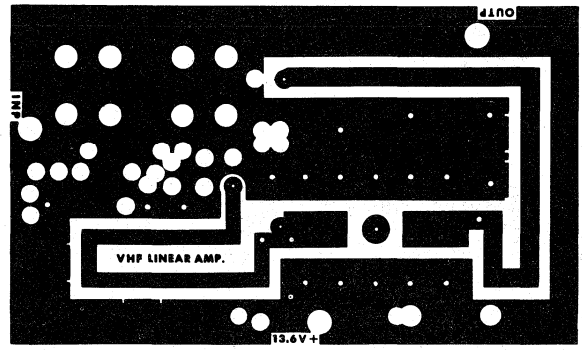
× DENOTES FEED THROUGH EYELETS OR PLATED THROUGH HOLES

⊗ DENOTES TERMINAL PINS

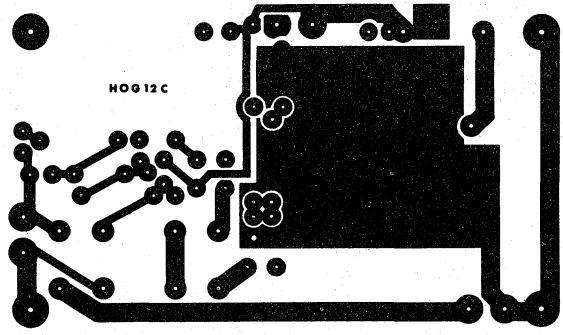
⊙ DENOTES BOARD STANDOFFS

6

FIGURE 10 – Printed Circuit Board Layout



NOTE: The Printed Circuit Board shown is 75% of the original.



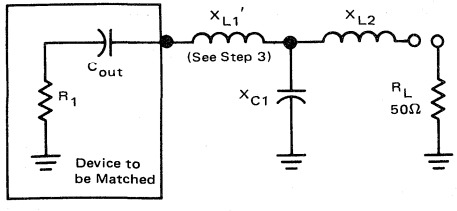
APPENDIX

This information was originally published in Motorola Application Note AN-267, "Matching Network Designs with Computer Solutions."

NETWORK D

The following is a computer solution for an RF "Tee" matching network.

Tuning is accomplished by using a variable capacitor for C_1. Variable matching may also be accomplished by increasing X_{L2} and adding an equal amount of X_C in series in the form of a variable capacitor.



TO DESIGN A NETWORK USING THE TABLES

1. Define Q, in column one, as X_{L1}/R_1.
2. For an R_1 to be matched and a desired Q, read the reactances of the network components from the charts.
3. X_{L1}' is equal to the quantity X_{L1} obtained from the tables plus $|X_{C_{out}}|$.
4. This completes the network.

6

Q	X_{L1}	X_{L2}	X_{C1}	R_1
8	8	27.39	7.6	1
8	16	63.25	14.03	2
8	24	85.15	20.1	3
8	32	102.47	25.87	4
8	40	117.26	31.42	5
8	48	130.38	36.77	6
8	56	142.3	41.95	7
8	64	153.3	46.99	8
8	72	163.55	51.9	9
8	80	173.21	56.7	10
8	88	182.35	61.39	11
8	96	191.05	65.98	12
8	104	199.37	70.49	13
8	112	207.36	74.91	14
8	120	215.06	79.26	15
8	128	222.49	83.54	16
8	136	229.67	87.74	17
8	144	236.64	91.89	18
8	152	243.41	95.97	19
8	160	250	100	20
8	168	256.42	103.97	21
8	176	262.68	107.9	22
8	184	268.79	111.77	23
8	192	274.77	115.59	24
8	200	280.62	119.38	25
8	208	286.36	123.11	26
8	216	291.98	126.81	27
8	224	297.49	130.47	28
8	232	302.9	134.09	29
8	240	308.22	137.67	30
8	256	318.59	144.73	32
8	272	328.63	151.65	34
8	288	338.38	158.46	36
8	304	347.85	165.14	38
8	320	357.07	171.71	40
8	336	366.06	178.18	42
8	352	374.83	184.56	44
8	368	383.41	190.83	46
8	384	391.79	197.02	48
8	400	400	203.13	50
8	440	419.82	218.04	55
8	480	438.75	232.49	60
8	520	456.89	246.53	65
8	560	474.34	260.2	70
8	600	491.17	273.52	75
8	640	507.44	286.52	80
8	680	523.21	299.23	85
8	720	538.52	311.66	90
8	760	553.4	323.84	95
8	800	567.89	335.78	100
8	1000	635.41	392.36	125
8	1200	696.42	444.63	150
8	1400	752.5	493.49	175
8	1600	804.67	539.57	200
8	1800	853.67	583.29	225
8	2000	900	625	250
8	2200	944.06	664.96	275
8	2400	986.15	703.38	300

Q	X_{L1}	X_{L2}	X_{C1}	R_1
9	9	40	8.37	1
9	18	75.5	15.6	2
9	27	98.99	22.4	3
9	36	117.9	28.88	4
9	45	134.16	35.09	5
9	54	148.66	41.09	6
9	63	161.86	46.91	7
9	72	174.07	52.56	8
9	81	185.47	58.07	9
9	90	196.21	63.45	10
9	99	206.4	68.71	11
9	108	216.1	73.86	12
9	117	225.39	78.92	13
9	126	234.31	83.88	14
9	135	242.9	88.76	15
9	144	251.2	93.55	16
9	153	259.23	98.28	17
9	162	267.02	102.93	18
9	171	274.59	107.51	19
9	180	281.96	112.03	20
9	189	289.14	116.49	21
9	198	296.14	120.89	22
9	207	302.99	125.23	23
9	216	309.68	129.53	24
9	225	316.23	133.77	25
9	234	322.65	137.97	26
9	243	328.94	142.12	27
9	252	335.11	146.22	28
9	261	341.17	150.28	29
9	270	347.13	154.3	30
9	288	358.75	162.23	32
9	306	370	170	34
9	324	380.92	177.63	36
9	342	391.54	185.14	38
9	360	401.87	192.52	40
9	378	411.95	199.78	42
9	396	421.78	206.93	44
9	414	431.39	213.98	46
9	432	440.79	220.93	48
9	450	450	227.78	50
9	495	472.23	244.52	55
9	540	493.46	260.74	60
9	585	513.81	276.51	65
9	630	533.39	291.85	70
9	675	552.27	306.8	75
9	720	570.53	321.4	80
9	765	588.22	335.67	85
9	810	605.39	349.63	90
9	855	622.09	363.31	95
9	900	638.36	376.71	100
9	1125	714.14	440.24	125
9	1350	782.62	498.94	150
9	1575	845.58	553.81	175
9	1800	904.16	605.54	200
9	2025	959.17	654.64	225
9	2250	1011.19	701.48	250
9	2475	1060.66	746.36	275
9	2700	1107.93	789.51	300

"A 15-WATT AM AIRCRAFT TRANSMITTER POWER AMPLIFIER USING LOW-COST PLASTIC TRANSISTORS"

Prepared by
Dave Hollander

INTRODUCTION

This application note describes a 15 watt carrier power, amplitude modulated broadband amplifier covering the 118-136 MHz AM aircraft band. Simplicity and low cost are emphasized in this design through the use of Motorola's common emitter TO-220 VHF power transistors. The power amplifier is designed to operate from 13.5 VDC. High level AM modulation is accomplished by a series modulator operating from a 27 volt supply.

CIRCUIT DESCRIPTION

The transmitter power amplifier has three stages using an MRF340 transistor as a pre-driver, a MRF342 as a driver, and a MRF344 as the final amplifier. All three devices are common emitter where the mounting tab is the emitter. The pre-driver stage is forward biased to enhance linearity and dynamic range. Amplitude modulation is applied fully to all three stages.

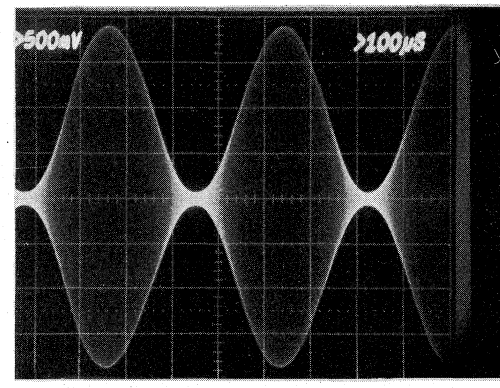
The P.A. is designed to operate with 50 ohm source and load impedances.

DESIGN CONSIDERATIONS

The design objectives are that the transmitter must be capable of operating over the range of 118 to 136 MHz with a minimum carrier output power of 15 watts. It must also be capable of being amplitude modulated greater than +85% over the frequency range, and the transmitter should be free from instability.

Other important considerations involve the interstage and the output networks. The output network is to operate efficiently at both the carrier power of 15 watts and the peak power of 60 watts while providing harmonic suppression. The interstage networks transform the output impedance of the device to the input impedance of the following device during modulation of all three stages.

FIGURE 1 – Modulated Output Waveform of Power Amplifier



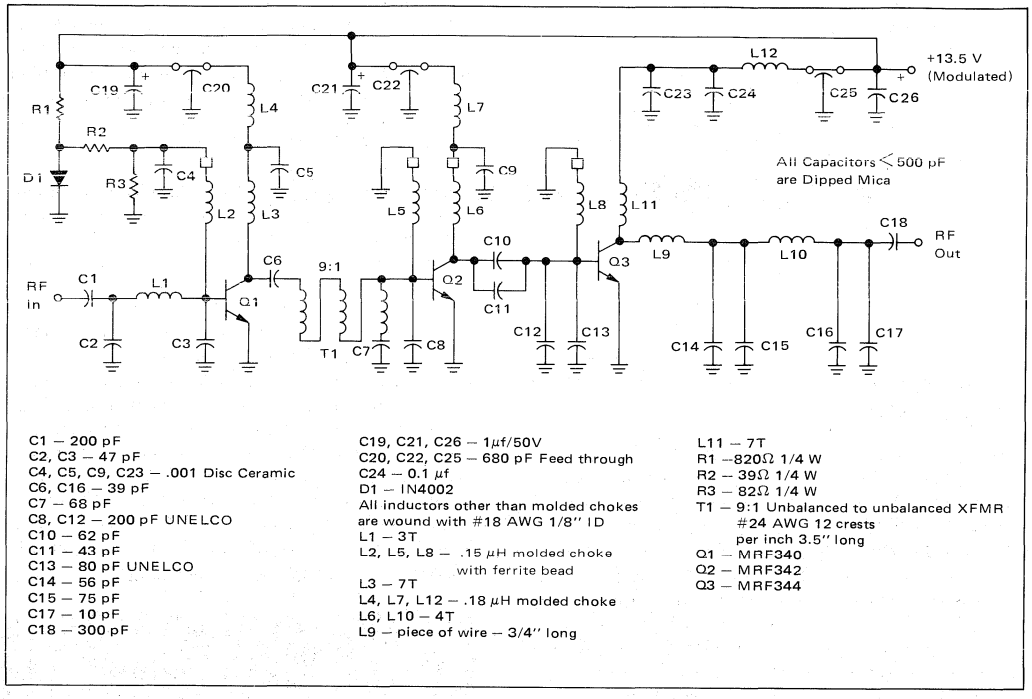
f = 136 MHz Pcarrier = 15 Watts (2 cms)
% Upward Modulation = 90%

In designing the networks, the Smith Chart is used to obtain initial values. These values were then optimized using a computer aided design program.

Figure 2 shows a schematic diagram of the transmitter P.A. RF circuitry.

The pre-driver stage uses a simple π-section input matching network. Forward bias for this stage is obtained through the network consisting of R_1, R_2, R_3, D_1, and is applied to Q_1 through L_2. The quiescent current is approximately 20ma for the MRF340.

FIGURE 2 – Schematic Diagram



C1 – 200 pF
C2, C3 – 47 pF
C4, C5, C9, C23 – .001 Disc Ceramic
C6, C16 – 39 pF
C7 – 68 pF
C8, C12 – 200 pF UNELCO
C10 – 62 pF
C11 – 43 pF
C13 – 80 pF UNELCO
C14 – 56 pF
C15 – 75 pF
C17 – 10 pF
C18 – 300 pF

C19, C21, C26 – 1μf/50V
C20, C22, C25 – 680 pF Feed through
C24 – 0.1 μf
D1 – IN4002
All inductors other than molded chokes are wound with #18 AWG 1/8" ID
L1 – 3T
L2, L5, L8 – .15 μH molded choke with ferrite bead
L3 – 7T
L4, L7, L12 – .18 μH molded choke
L6, L10 – 4T
L9 – piece of wire – 3/4" long

L11 – 7T
R1 – 820Ω 1/4 W
R2 – 39Ω 1/4 W
R3 – 82Ω 1/4 W
T1 – 9:1 Unbalanced to unbalanced XFMR #24 AWG 12 crests per inch 3.5" long
Q1 – MRF340
Q2 – MRF342
Q3 – MRF344

The interstage between Q_1 and Q_2 is designed as follows. The effective collector load impedance is estimated to be 100-j50 ohms. The input impedance, Z_{IN}, of the MRF 342 is 1.75+j2 ohms at 136 MHz (as taken from the data sheet). One way to match the output of the MRF340 to the input of the MRF342 with a minimum of components is through the use of a 9:1 transformer (1,2). Figure 3 shows a Smith Chart plot of the interstage network with the chart normalized to 50 ohms. Starting at point A, this impedance is rotated to point B by a shunt capacitor C_8. The impedance at this point is approximately 5 to 5.5 ohms. A 9:1 transformer transforms this impedance to approximately 50 ohms. Point C, the 50 ohm point, is rotated to D by series capacitor C_6. Point D is then rotated to point E, the complex conjugate of the output impedance of Q_1, by shunt inductor L_3.

A different approach is used for the Q_2 - Q_3 interstage network. The MRF342 output impedance Z_{OL}, and the MRF344 input impedance Z_{IN}, are taken from the data sheets. Figure 4 shows a Smith Chart plot of this network with the chart normalized to 50 ohms. Point A is the input impedance of the MRF344. This impedance is rotated to the real axis by shunt capacitors – C_{12} and C_{13}. Point B is then rotated to point C by series capacitors – C_{10} and C_{11}. This impedance is then transformed to the complex conjugate of the output impedance of the MRF342 by shunt inductor L_6.

The MRF344 output matching network consists of a shunt inductor at the collector of Q_3 followed by two L-sections. L-sections were used because they provide excellent harmonic suppression and good efficiency over the entire band. Figure 5 shows a Smith Chart of the output network, with the chart normalized to 50 ohms.

All impedance matching element values calculated using the Smith Chart and optimized with the computer program were used as starting points in building the networks. The final component values shown in Figure 2 were derived through on-the-bench tuning and adjustment and differ from the calculated values as the Figure 2 values cover 118-136 MHz. The calculated values are only for 136 MHz.

Since low cost is a key factor in the use of the TO-220 devices, inexpensive components are used wherever applicable. Molded chokes, dipped mica and dipped ceramic capacitors are used throughout the circuit. One of the problems encountered when using dipped micas at VHF is their series lead inductance. The higher capacitance values approach resonance at VHF. Selected values were

6

measured on an HP network analyzer at 125 MHz. The results are shown in Table 1.

TABLE 1

Cnominal (PF)	Cmeasured (PF)
5	5
10	10
25	26
30	33
39	45
50	64
75	106
100	161
200	750

Note: All lead lengths kept to an absolute minimum (<0.1 inch)

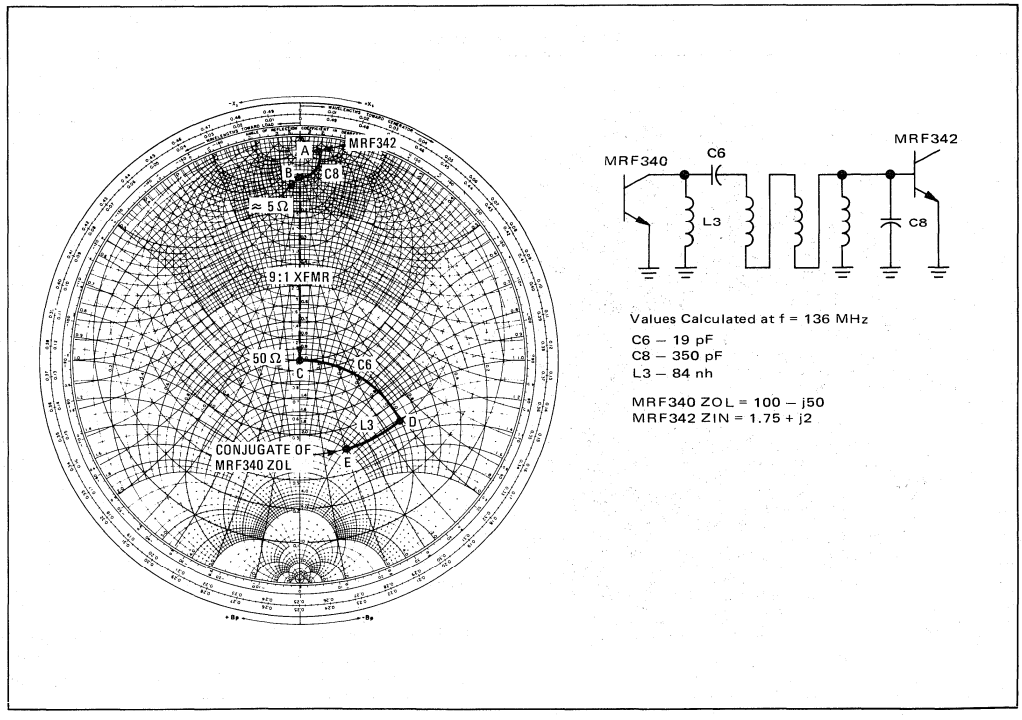
The data obtained shows that values below 75pf are usable. Lead length should be kept to a minimum when using both the dipped mica and the disc ceramic capacitors. UNELCO capacitors are used in place of the dipped micas at the base of Q_2 and Q_3, since the net required capacitance and base current is very high.

CONSTRUCTION TECHNIQUES

The amplifier is assembled on a 2" X 5" double sided printed circuit board. Board material is G-10 with a thickness of 0.062". A 1:1 photomaster of the top side of the board is shown in Figure 6. Eyelets are placed through the board at points marked by the letter "O". The eyelets are soldered to both sides of the PCB to connect the top ground to the bottom side ground return. Feed-thru capacitors are mounted on the DC feed bar which is made of G-10 PCB. A 1:1 photomaster of the feedbar is also shown in Figure 6. Eyelets are placed at points marked by an "O" and feed-thru capacitors are placed at points marked by an "X". The DC feedbar is soldered to the main board. The location of the critical components is shown in Figure 7. Construction details of the 9:1 impedance transformer are shown in Figure 8. (1,2)

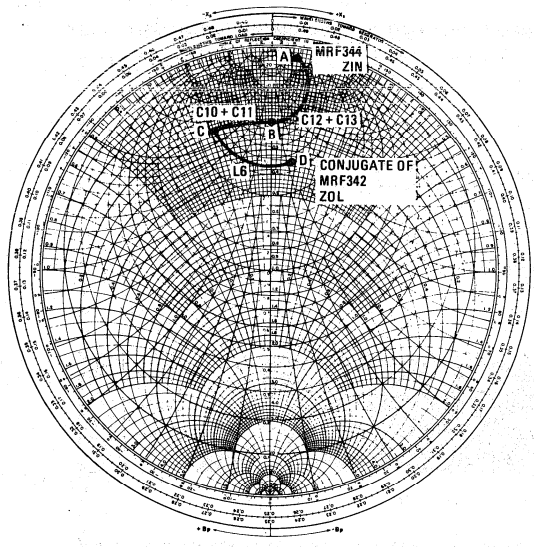
For reliable operation, the transistors must not only be heatsunk, but they must also be mounted properly for emitter RF ground return. Figure 9 shows mounting details for the TO-220 package. More detailed information on mounting is available in AN-778.(3) The entire assembly is mounted on a 6" extruded aluminum heatsink using 4-40 X ¼ machine screws. The heatsink surface should be flat and free of burrs, particularly around the transistor mounting holes.

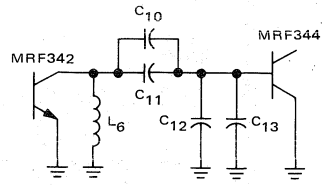
FIGURE 3 – MRF340 – MRF342 Interstage Network



6

FIGURE 4 – MRF342-MRF344 Interstage Network



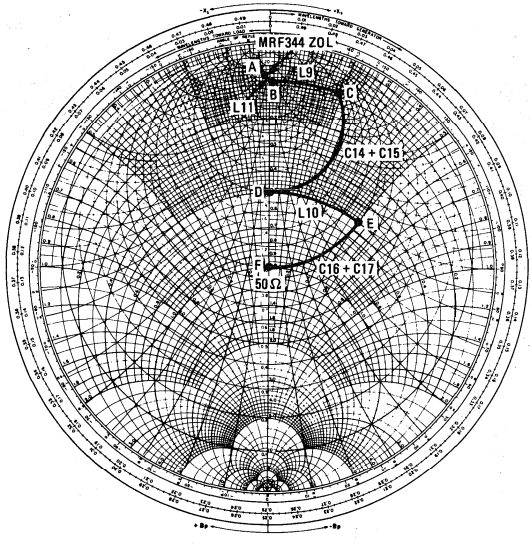


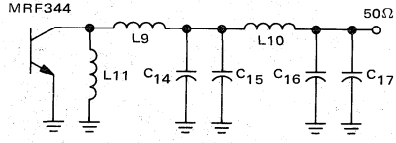
Values Calculated at f = 136 MHz

C10 + C11 – 130 pF
C12 + C13 – 365 pF
L6 – 15 nh

MRF342 ZOL = 17-j4.7
MRF344 ZIN = 1.25 + j2.86

FIGURE 5 – MRF344 Output Network





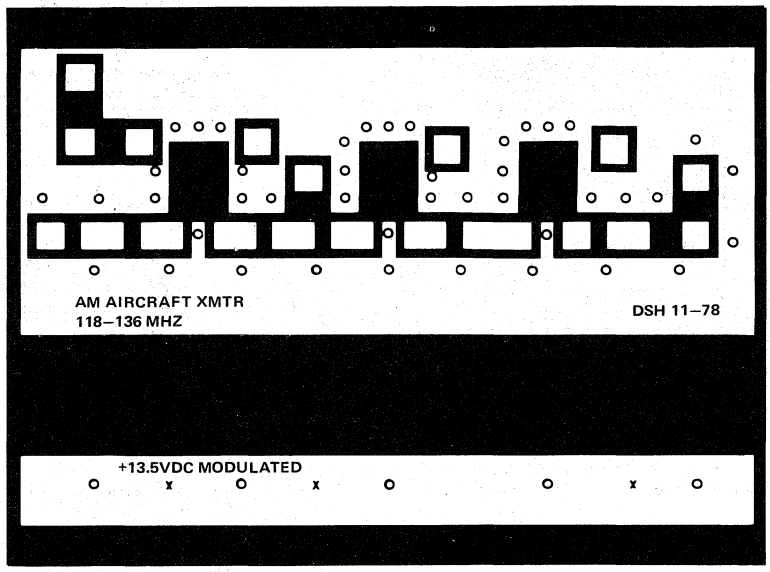
Calculated Values at f = 136 MHz

C14 + C15 = 100 pF
C16 + C17 = 23 pF
L9 = 11 nh
L10 = 28nh
L11 = 90 nh

MRF344 ZOL = 4.2-j0.32

6

FIGURE 6 – Photomaster



NOTE: The Printed Circuit Board shown is 75% of the original.

FIGURE 7 – Location of Critical Components

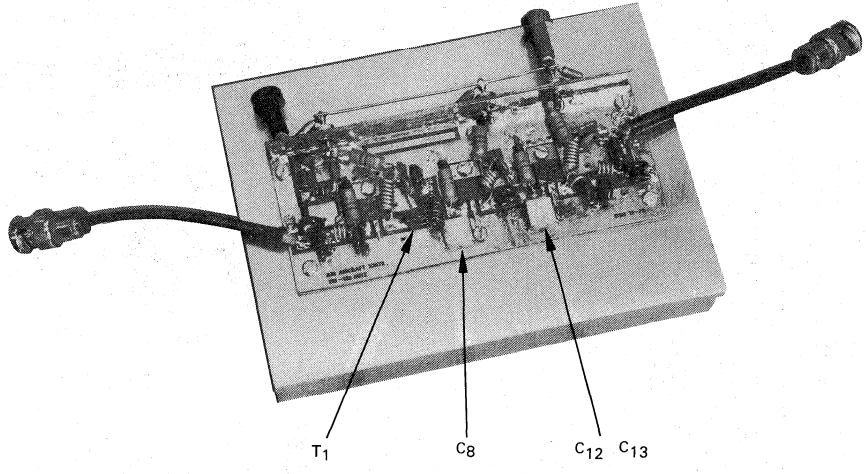


FIGURE 8 – Construction Details of the 9:1 Unbalanced to Unbalanced Transformer

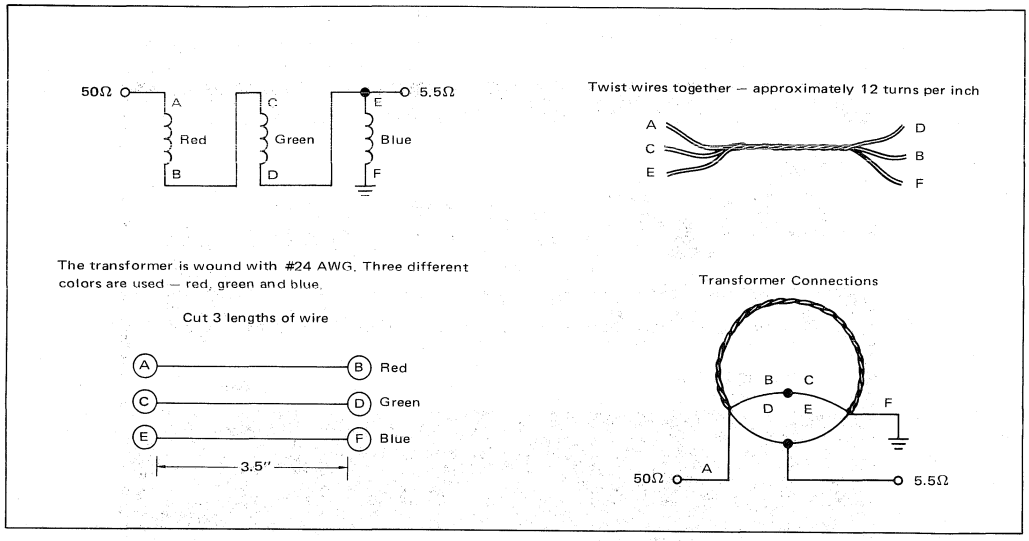


FIGURE 9 – Mounting Details for TO-220 Package

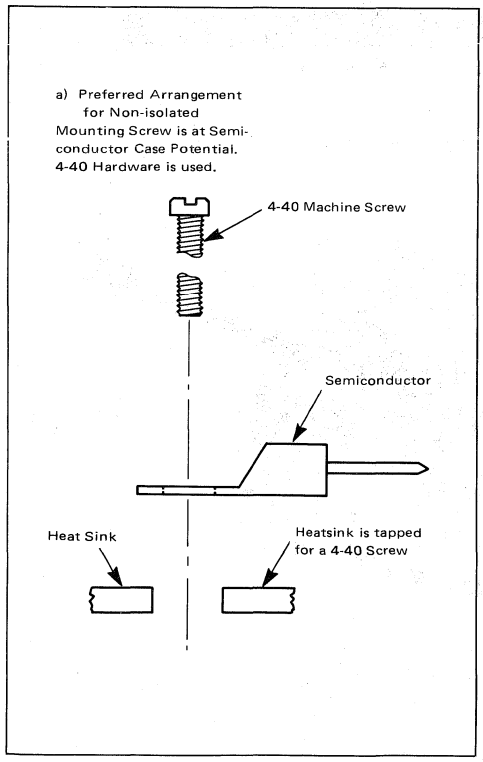
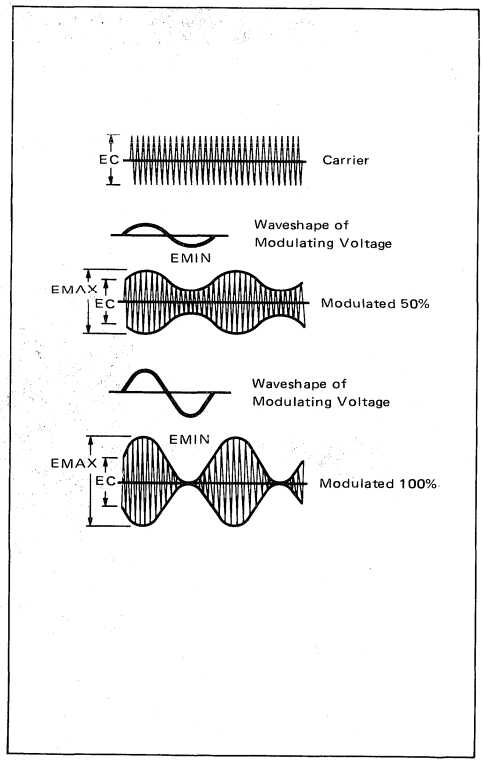


FIGURE 10 – Amplitude Modulation Waveforms



6

MODULATION

In an amplitude modulated waveform the amplitude of each cycle of the modulated wave varies in accordance with the modulating signal. Using voice modulation, the resultant waveform is not only complex, but difficult to analyze. Therefore, when testing and analyzing the transmitter P.A., a simple 1 KHz sine wave is used as the modulating signal. When analyzing an AM waveform, one of the things to consider is the modulation factor (M). M is usually expressed as percent modulation and is calculated as follows:

$$M = \frac{Emax - Emin}{Emax + Emin} \times 100\%$$

Figure 10 shows amplitude modulation waveforms.

The above formula is valid only when the modulation process is symmetrical and little distortion is present. If significant assymmetry is present then up modulation and down modulation must be analyzed separately.

$$M = \frac{Emax - Ec}{Ec} \times 100\% \quad \text{For positive peak modulation}$$

$$M = \frac{Ec - Emin}{Ec} \times 100\% \quad \text{For negative peak modulation}$$

When a carrier is modulated by a pure sine wave, two sidebands are generated at the carrier frequency plus and minus the modulating frequency. The power level of the sidebands is dependent upon the percentage of modulation. At 100% modulation, the total power contained in the sidebands is one-half the carrier power or one-fourth in each sideband. For modulation levels of less than 100%, the total power is:

$$PSB = \frac{1}{2} m^2 PC$$

where m = modulation factor
Pc = carrier power

Collector modulation is a commonly used method for modulating a solid state transmitter. Using this method, the modulating voltage is applied to a collector through a transformer. The secondary winding of the transformer must be capable of handling the DC current required by the transistor and have low DC resistance, so as not to cause a significant voltage drop. The voltage drop will reduce the voltage applied to the collector of the stage being modulated.

Another form of collector modulation uses a series modulator. This type of modulator is used to evaluate the transmitter in this application note.(4) A series modulator uses audio power transistors instead of a transformer secondary. A schematic diagram of the series modulator is shown in Figure 11. 27 volts is applied to the modulator and the quiescent DC voltage applied to the transmitter is set by the 10KΩ potentiometer.

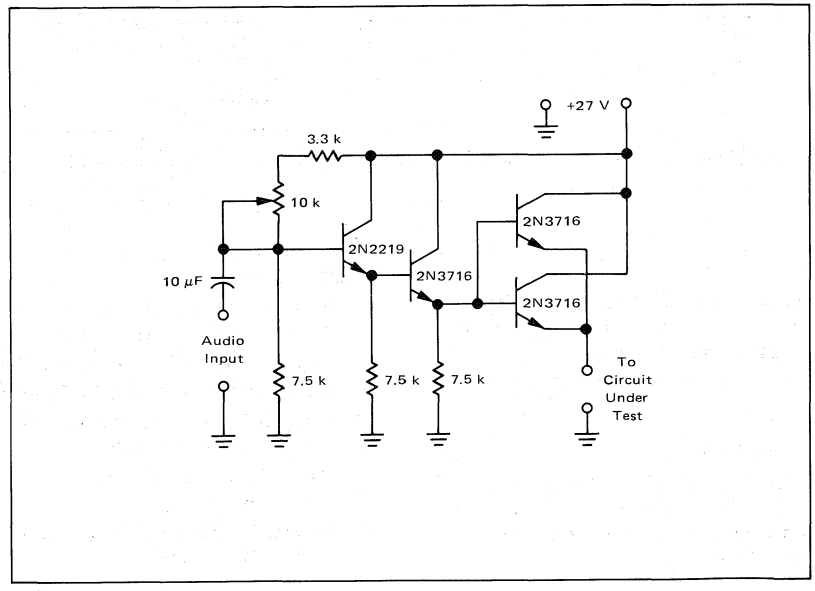
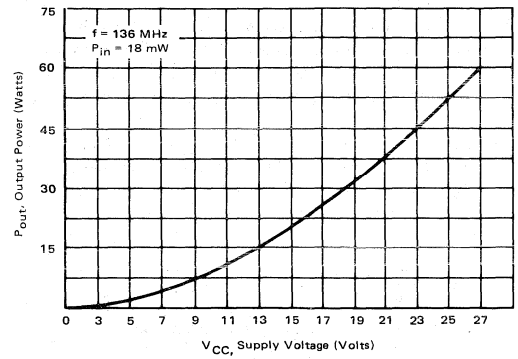


FIGURE 11 – Series Modulator

Table 2 – Performance of the 15 Watt Amplifier

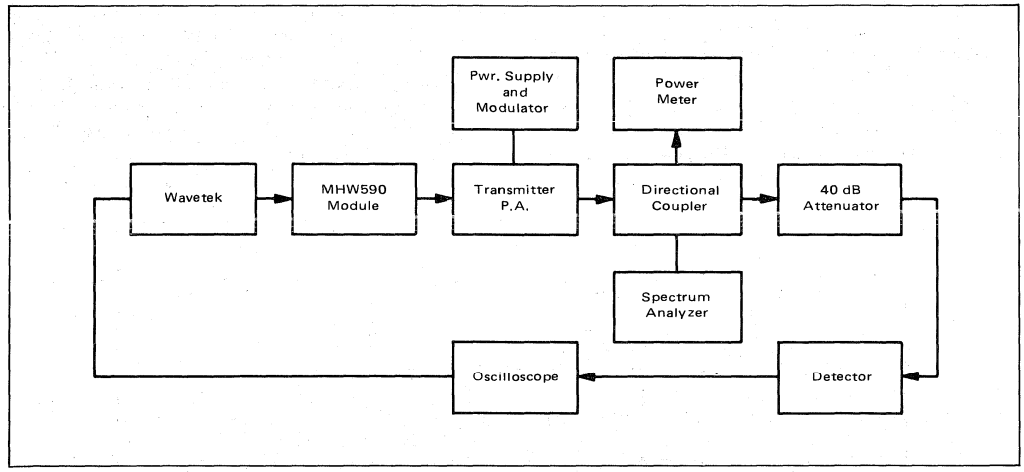
	118 MHz	127 MHz	136 MHz
P_{in} (mW)	14.0	15.0	18.0
Pcarrier (W)	15.0	15.0	15.0
Total Current (Adc)	2.2	2.0	2.5
Power Supply Voltage (Vdc)	13.5	13.5	13.5
Upward Modulation (%)	89.0	88.0	90.0
Harmonic Rejection (dB) (Relative to Peak Power)			
2f 3f	55.0 58.0	55.0 58.0	52.0 57.0
Load Mismatch	Capable of Operating into 3:1 Load VSWR.		

OUTPUT POWER VERSUS SUPPLY VOLTAGE



P_{out} is initially set at the carrier power of 15 watts at 13.5 Vdc, then the supply votlage is varied from 0 to 27 Vdc keeping P_{in} constant. This demonstrates the peak power output capability of the transmitter P.A.

FIGURE 12 – Block Diagram of Swept Set-Up for Tuning Up the Transmitter



TEST SET-UP

When adjusting a broadband RF power amplifier, it is advantageous to have a swept test station. Using a swept set-up, one can observe the following:

1) The effect of varying individual component values
2) Bandwidth
3) Instability
4) Input VSWR bandwidth.

A Wavetek 1002 Sweep Generator driving a Motorola MHW590 module is recommended as a drive source. Figure 12 shows a block diagram of the swept set-up used to test and evaluate the amplifier.

REFERENCES

1. Ruthroff, "Some Broadband Transformers," PROC. IRE Vol. 47, No. 8, August, 1959
2. Granberg, H. "Broadband Transformers and Power Combining Techniques for RF," Motorola AN-749
3. Roehr, Bill, "Mounting Techniques for Power Semiconductors," Motorola AN-778
4. "A 13-W Broadband AM Aircraft Transmitter," Motorola AN-507
5. Terman, Frederick E., "Electronic and Radio Engineering," McGraw-Hill

6

POWER MOSFETs versus BIPOLAR TRANSISTORS

Prepared by
Helge O. Granberg
Sr. Staff Engineer

What is better, if anything, with the power FETs if we can get a bipolar transistor with an equal power rating for less than half the price?

Several manufacturers have recently introduced power FETs for RF amplifier applications. Devices with 100 W output capabilities are available for VHF frequencies and smaller units are made for UHF operation. All are enhancement mode devices, which means that the gate must be biased with positive voltage (N channel) in respect to the source to "turn it on." Early designs were so called V-MOS FETs, where the channel is in a V-groove. The V-groove must be etched with a special process, and the silicon material must have a different crystal orientation from the material normally used for bipolar transistors. The difficulty of the etching process in production has led to the development of other types of channel structures such as HEX and T, which are still vertical channel structures, but V-groove is eliminated, and the gate is on a straight surface. Thus, for an equal gate periphery, more room

TABLE A

	Bipolar	TMOS FET
Z_{in} RS/ XS(30 MHz):	0.65 - J0.35 Ohms	2.20 - J2.80 Ohms
Z_{in} RS/ XS(150 MHz):	0.40 + J1.50 Ohms	0.65 - J0.35 Ohms
Z_{OL} (Load Impedance):	Almost equal in each case, depending on power level and supply voltage.	
Biasing:	Not required, except for linear operation, high current voltage source necessary.	Some gate bias always required. Low current source, such as resistor divider sufficient.
Ruggedness:	Fails usually under current conditions. Thermal runaway and secondary breakdown possible.	Failure modes: Gate punch through, exceeding of breakdown voltages, over dissipation.
Linearity:	Low order distortion depends on die size and geometry. High order IMD is a function of type and value of ballast resistors.	Low order distoriton worse than bipolar for a given die size and geometry. High order IMD better due to lack of ballast resistors.
Advantages:	Wafer processing easier. Low collector-emitter saturation voltage, which makes devices for low voltage operation possible.	Input impedance more constant under varying drive level. Lower high order IMD. Easier to broadband. Devices or die can be paralleled. High voltage devices easy to implement.
Disadvantages:	Low input impedance with high reactive component. Internal matching required to lower Q. Input impedance varies with drive level. Devices or die cannot easily be paralled.	Larger die required for comparable power level. Nonrecoverable gate breakdown. High drain — source saturation voltage, which makes low voltage, high power devices less feasible.

on the surface is required. Japanese manufacturers seem to favor geometries with horizontal channels. They are similar to small signal MOSFETs with a number of them paralleled on one chip. This technique represents even more wasteful use of the die surface than HEX or TMOS. Typically a power FET requires 50 to 100 percent more die area than a bipolar transistor for equal power output performance. For TMOS the number is about 50 percent. This is mainly due to the higher saturation voltage, but the geometry also gives some 30 percent less gate periphery than available base area in bipolar. Since the price of a solid state device is a function of a die size, we get fewer watts per dollar. This is completely opposite from what the industry has been trying to do in the past years with bipolar transistors. So, one may ask: What is better, if anything, with the power FETs if we can get a bipolar transistor with an equal power rating for less than half the price? This is where we come to the purpose of this article, which is to discuss the characteristics of the FET and bipolar device. Both have the same basic geometry, but with some mask changes, one was processed as a MOSFET and the other as a bipolar.

CIRCUIT CONFIGURATIONS

Since the gate of a MOSFET device is essentially a capacitor, which consists of MOS capacitance distributed between the channel and the surface metalization, the input Q is normally extremely high. For this reason, the gate must be de-Q'ed with a shunt resistance or applying negative feedback or a combination of the two. Unless this is done properly, the affect of feedback capacitance (C_{rss}) will result in conditions, where stable operation is impossible to achieve.

Figure 1 shows a Smith Chart plot of a 150 W MOS FET and a bipolar device using the same basic geometry for comparison purposes. The gate of the FET has been shunted by a resistance of 20 ohms. Without the shunt resistance the input impedance would be a pure capactive reactance, if package inductances are disregarded.

The input Q is an inverse function of the broadbandability of a device. With the techniques mentioned above, the Q can be controlled to a large degree, but some power gain will be sacrificed, unless only some type of selective negative feedback is employed for that purpose. Amplifiers in the 100 W power level, covering five octaves can be designed, and the limiting factor only seems to be the proper design of the broadband matching transformers.

Due to the lack of base diode junctions inherent to bipolar devices, where the diode forward conductance depends on the drive level, the MOSFET gate impedance varies only slightly with the input voltage amplitude. The gate MOS capacitance should be more or less independent of voltage, depending on the die processing. This is considered one of the advantages with FETs, especially regarding amplitude modulated applications, where a constant load for the driver stage is important. Negative feedback should be limited, since it tends to deteriorate this characteristic. Another advantage is the AGC capability by varying the gate voltage. In common source configuration, depending on the initial power gain, etc., an AGC range of 20 dB is achievable.

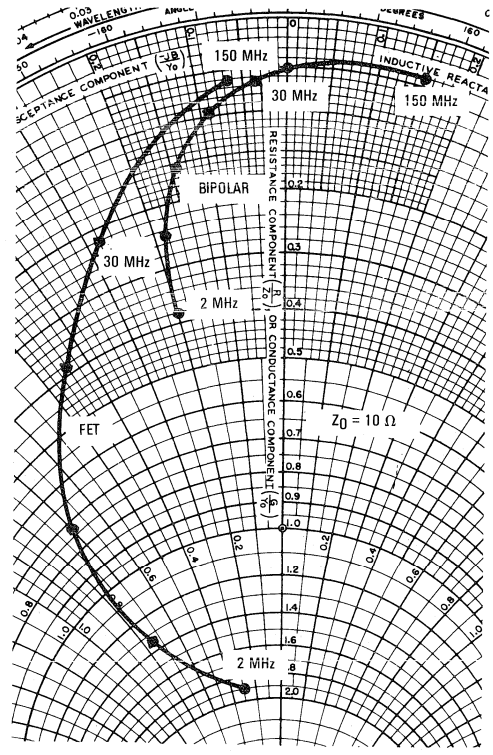


FIGURE 1 — 150 Watt MOSFET and Bipolar Comparison

Common gate configuration has some advantages, although it is not useful in applications requiring linearity. The load impedance is reflected back to the gate and in effect is in parallel with the source to ground impedance. The total input impedance is more constant with frequency than in common source mode, but varies greatly with output power level and supply voltage. As in a comparable configuration with bipolar transistors, the overall power gain is low, but the unity gain frequency (f_α) extends higher, which makes the common gate circuit attractive at UHF designs. It also

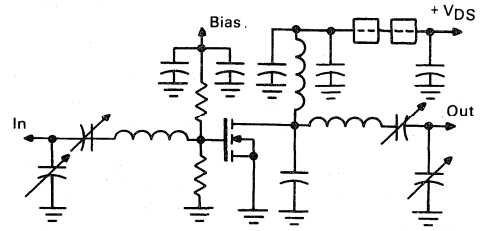


FIGURE 2 — A Typical Common Source MOSFET Power Amplifier Circuit

has more tendency for parasitic oscillations, since the input and output are in the same phase. The de-Q'ing of the input can be done in the same manner as in a common source circuit, but negative feedback is not as easy to implement. This circuit also exhibits greater power gain versus bias voltage variation characteristics. In applications, where 40 dB to 50 dB AGC range is required, the common gate configuration should be considered.

A common drain configuration represents the emitter follower in bipolar circuits. In both cases the input impedance is high and the load impedance is effectively in series with the input. The input capacitance, (drain-to-gate, or collector-to-base) is lower than in common source or common gate circuits, and several times lower for the FET than bipolar for equal die size. This is due to lack of the diode junction. A MOSFET source follower can not be regarded as having current gain as the emitter follower. The amplification rather takes place through impedance transformation. Due to the fair amount of input de-Q'ing required, the available power gain is lower than in common source circuit for example. Having less than unity voltage gain, the circuit exhibits exceptional stability, and negative feedback is not necessary, nor can it be easily implemented. Push pull broadband circuits for a frequency range of 2 to 50 MHz have been designed for 200-300 watt power levels. Their inherent characteristics are good linearity and gain flatness without any leveling networks. High power SSB amplifiers are probably the most suitable application for common drain operation. The AGC range is comparable to that in common source, but higher voltage swing is required. It must be noted that the MOS devices used must have high gate rupture voltage, since during the negative half cycle of the input signal, the gate voltage approaches the level of V_{DS}.

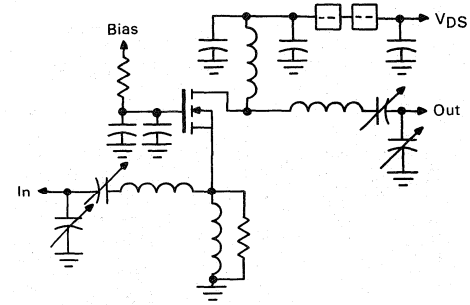


FIGURE 3 — A Typical Common Gate MOSFET Power Amplifier Circuit

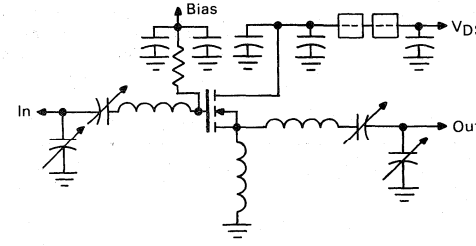


FIGURE 4 — A Typical Common Drain, Narrow Band MOSFET Power Amplifier Circuit

LINEARITY ASPECTS

Some literature claims that MOS power FETs are inherently more linear than the bipolar transistors. This is only true up to the point where envelope distortion, caused by saturation, instabilities or other reasons, is not present. It is also a function of the bias current (I_{DQ}). The FETs usually require higher idling currents than the bipolars to get full advantage of their linearity. Bipolars are usually biased only to get the base-emitter diode into forward conduction, whereafter increasing the bias helps little. Class A is an exception, but the device must then be operated at 20-25 percent of the rated Class AB level.

Probably the main advantage with the MOS power FETs is their greatly superior high order IM distortion performance. This is mainly due to the fact that ballasting resistors are not required with FETs. In bipolar RF power transistors, nonlinear feedback is distributed to each emitter site through the MOS capacitance from the collector. In devices using diffused silicon resistors, this effect is even worse, and caused by additional nonlinear diode capacitance between the collector and the emitters. The high order IMD (9th and up) is actually in direct relation to the ballasting resistor values, which must be optimized for an even power distribution along the die. Too low values would result in a fragile device, and the opposite would, in addition to the IMD problem, result in high collector-emitter saturation voltage and low power gain.

The feedback capacitance, drain-to-gate or collector-to-base for example, also has a secondary effect in IMD. In both cases it is a function of the die geometry, and is usually lower with devices with higher figure of merit, such as the ones made for UHF and microwave applications. A MOS power FET exhibits some five times lower feedback capacitance than a bipolar transistor with a similar geometry. In a bipolar transistor this capacitance partly consists of the collector-base junction, which is highly nonlinear with voltage. This, together with the varying input impedance, generates internal feedback, which is nonlinear and produce high order IMD to some degree. A more noticeable effect is that the low order IMD goes up with reduced drive levels as shown in Figure 6.

This can be related to different turn on characteristics between the two device types. When a bipolar device is biased to Class AB, the bias does not usually, completely overcome the V_{BE} knee. Thus, at lower signal levels, the remaining nonlinear portion covers a larger area of the total voltage swing. Increasing the bias from the normally recommended Class AB values will help and full Class A should eliminate the problem completely.

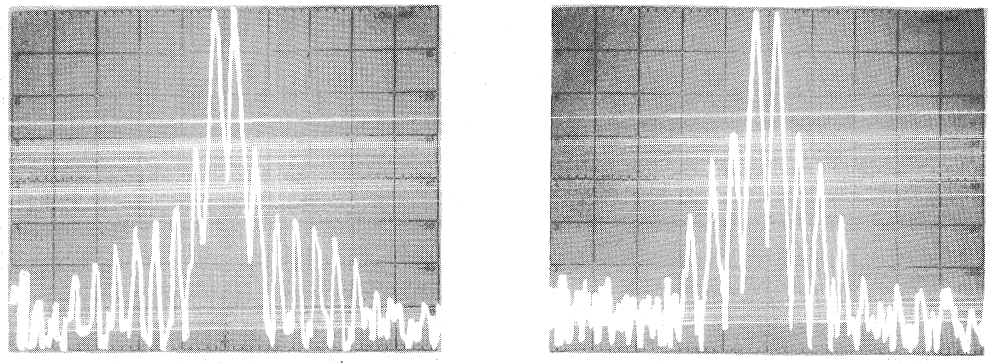


FIGURE 5 — Two Tone Spectrographs of 300 W PEP, 50 V Amplifier Outputs
a. using bipolar transistors and b. with TMOS power FETs. 500 mA of bias current per device was used in each case. Doubling the bias current has a minimal effect in a. but b. the 7th order products would be lowered by 10–12 dB.

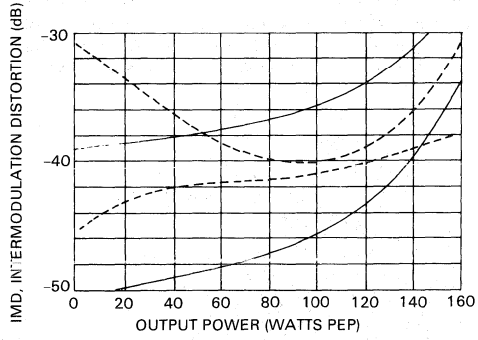


FIGURE 6 — IM Distortion as a Function of Power Output. Solid Curves MOSFET, Dashed Curves Bipolar Transistor

CLASS D/E APPLICATIONS

Switching mode RF power amplifiers have only become feasible since the introduction of the power FET. Being a majority carrier device, the FET does not exhibit the storage time phenomena, that limits the switching speed of a bipolar. For a given device, the switching speed is mainly determined by the speed the gate capacitance can be charged and discharged. If the capacitance is in the order of several hundred pF, a smaller FET is required to provide the fast charge-discharge switch. For low power stages, bipolars can be used, since the storage time is mainly an inverse function of the f_T and device size. The advantages of a Class D amplifier are high efficiency, linearity and ruggedness, since power is ideally dissipated only during the switching transitions.

These amplifiers are readily applicable for FM modulation, after harmonic filtering. The analog gain is obtained by pulse-width modulation of the input switching signal, and demodulation of the output with suitable filters. Linearity is required only from the modulator, which is easy to achieve at small signal levels. The high speed voltage controlled one shot MC10198 should be ideal for a linear pulse-width modulator. By properly adjusting its operating point, low level AM or suppressed carrier double sideband signals can be generated.

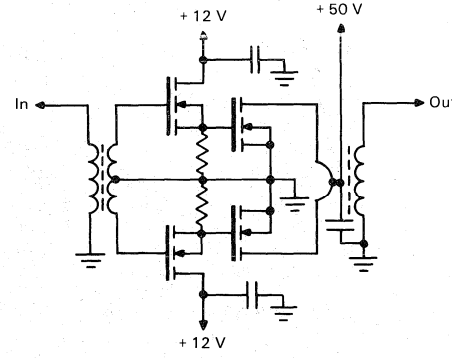


FIGURE 7 — A Typical Power MOSFET Class D RF Amplifier, Arranged in Push-Pull Configuration

GENERAL

All MOSFETs can in theory have a positive temperature coefficient on the gate threshold voltage. This means that the gate threshold voltage increases with temperature, trying to "turn the device off." In addition the g_m will decrease, which also helps in preventing the thermal runaway, which is commonly a problem with bipolars. The coefficient of the gate threshold

voltage is also a function of the drain current. Normally the coefficient is negative at low current levels, and turns positive at higher currents. The turnaround point, which can be controlled by doping the other fabrication steps, must be at a current level not to exceed the maximum dissipation rating, taking the derating factor into account. Thus, the power MOS devices can be easily biased to Class A, without fear of a thermal runaway.

Two types of high frequency noise are generated by bipolar transistors. Shot noise is caused by the forward biased junctions, and thermal noise by moving carriers upon flow of electrons. Both have different noise spectrums, and only the latter is present in a FET. In a transmitter, where the devices are biased for linear operation, the shot noise becomes a problem, especially if a receiver is in close proximity, as in transceiver designs. Also, if several stations are operated near each other, the noise can be transmitted through the antenna, disturbing the reception at nearby stations. In most instances, the bias of the power devices must be switched on and off during the transmit and receive functions, which will prevent a full break-in operation. Measurements of 150 W devices, intended for SSB applications, were performed at 30 MHz, at the proper idling current levels. The difference in the total noise figure between a bipolar and a FET is about three to one, or 7 dB and 2.2 dB respectively. The amount of noise that can be tolerated varies with each situation, and whether the difference above is significant in practice depends on other factors involving the design of the equipment.

CONCLUSION

From the above we must conclude that it is doubtful the power FET ever will replace the bipolar transistor in all areas of communications equipment. It will have its applications in low and medium power VHF and UHF amplifiers, eliminating the need for internal matching, and up to medium power low band and VHF SSB, where the high order IMD is beginning to be more and more in emphasis due to the crowded frequency spectrums. The author's personal opinion is that the power FET is the most feasible device for the amplitude compandored sideband (ACSB) applications, proposed for future use in land mobile communications. The system principle requires extreme linearity in the amplifying stages, which in the past has only been achieved with Class A operation. The power FET also opens new applications for high efficiency switching mode power amplifiers, which have not been possible in the past for reasons described earlier. The possible upper frequency limit would be dictated by the physical lay-out of the system.

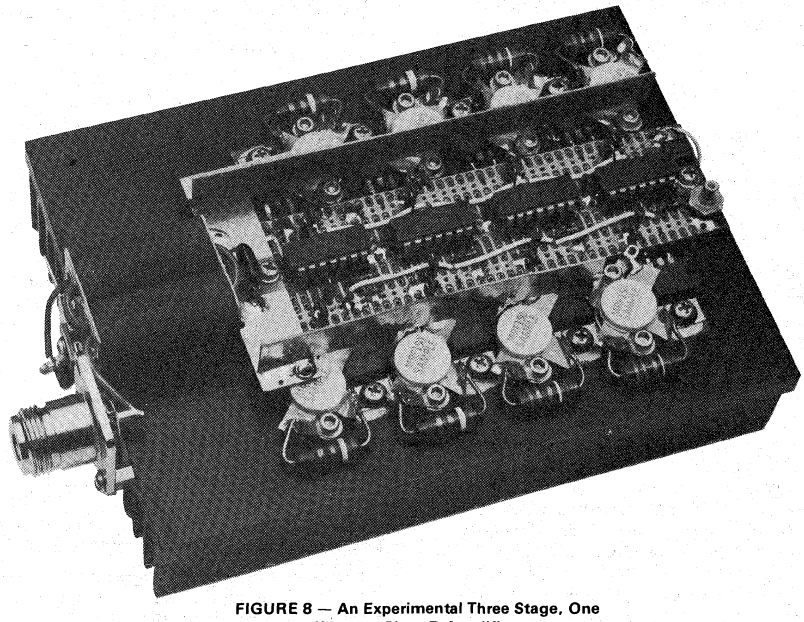


FIGURE 8 — An Experimental Three Stage, One Kilowatt Class D Amplifier.

The unit operates up to 10 MHz yielding an efficiency of 85 percent. The power gain is 30 dB.

VHF MOS POWER APPLICATIONS

Prepared by
Roy Hejhall
Sr. Staff Engineer

INTRODUCTION

The assumption is made that the reader is familiar with the types, construction, and electrical characteristics of FETS. References 1 and 2 contain information on this subject.

Silicon RF power FETs are generally N-Channel MOS enhancement mode devices. Most are vertical structures, meaning that current flow is primarily vertical through the chip with the bottom forming the drain contact. Vertical construction has the advantage of providing greater current density which translates to more watts per unit area of silicon.

The assembly of RF power FET wafers into finished devices is similar to the assembly of bipolar RF power transistors (BPTs). Identical packaging is utilized for both types of devices.

ADVANTAGES OF RF POWER FETS

The advantages of FETs have been described elsewhere,[3,4] and will not be repeated in detail. Some observations on this subject are given below.

The inherently higher power gain is illustrated by a comparison of the MRF171 FET and MRF315 BPT. Both are VHF devices rated at 45 watts power output. Typical power gains at similar operating conditions (f = 150 MHz, P_{out} = 45 W, dc supply voltage = 28 V) are 15.0 dB for the FET and 11 dB for the BPT.

Any gain comparison should also include ruggedness data. Ruggedness is defined as the ability of a device to survive operation into mismatched loads. Obviously, UHF and microwave BPTs are available with gains exceeding that of the MRF171 FET at 150 MHz, but the higher frequency BPTs will not survive much abuse at VHF. The superior ruggedness of the FET is even more impressive when it is recognized that no source site ballasting is used.

Another gain comparison at VHF is provided by the MRF174 FET and MRF317 BPT. The MRF317 is rated at 100 watts output, and contains an internal input matching network which increases the device gain by typically 5.0 dB. The MRF174 is rated at 125 watts output and has no internal input matching, yet the typical gain of the MRF174 at 125 watts output is 12 dB while the typical gain of the MRF317 is 10 dB at 100 watts output (both devices operating at 150 MHz with a 28 Vdc supply).

Impedance differences are found mainly at the device input. FET input impedance at dc approaches infinity, dropping at VHF to a level approximately equal to, but slightly higher than the input impedances of comparable BPTs.

This point can be illustrated by considering again the aforementioned 45 watt VHF devices. When operating at 150 MHz with a 28 Vdc supply and 45 watts output, the large-signal input impedances are 1.89 − j4.81 ohms for the MRF171 FET and 1.2 + j1.0 ohms for the MRF315 BPT.

These devices illustrate another difference. The large-signal input impedance of FETs at VHF is capacitive. By contrast, most VHF BPTs with power outputs greater than 20 watts have an inductive input impedance at 150 MHz. The input impedance of the MRF315 passes through resonance at about 100 MHz.

The low-noise figure of the FETs facilitates the design of low-noise power amplifiers and high dynamic range receiver front ends. Noise figures of less than 3.0 dB at f = 150 MHz, V_{DS} = 28 V, I_D = 2.0 A have been measured with the 125 watt MRF174. The MRF134 5.0 W VHF FET has a typical noise figure of 2.0 dB at 150 MHz, 28 V, 100 mA, and values as low as 1.5 dB have been measured. Transmitter noise floor determines the antenna front to back ratio required for duplex systems.

A most interesting FET characteristic is the inherent gain control mechanism. The power output of a FET amplifier can be varied from full rated output over a range of greater than 20 dB (with RF input power held constant) by varying the dc gate voltage. Further, the device gate does not draw dc current, so the dc source utilized for gain control does not have to deliver any power to the FET. This capability, which does not exist in the RF power BPT, facilitates the design of systems requiring gain control, either manual or automatic.

AMPLIFIER DESIGN

The design of TMOS FET RF power amplifiers has much in common with the design of BPT amplifiers. The amplifier must include dc circuitry to apply bias voltages and RF matching networks to perform the necessary impedance transformation over the frequency band of interest. Amplifier design consists of the synthesis of circuitry to perform the above tasks.

A positive dc supply voltage is required on the drain. To date most RF power FETs have been designed for the standard BPT operating collector voltages, i.e. 12.5 V, 28 V, and 50 V. Some higher voltage FETs are also available. The FETs described are designed for 28 V operation.

There is no FET parallel to the popular zero base bias BPT amplifier. The typical FET RF power amplifier requires forward gate bias for optimum power output and gain. That is the bad news; the good news is that the FET gate is a dc open circuit and the bias network may often be just a simple resistive divider.

A convenient gate bias source is the drain supply. When utilizing this technique care must be taken in filtering the bias circuitry. An inadequately filtered bias circuit connected to the drain supply can form an output-to-input feedback path for oscillations.

BPT amplifiers. These networks usually take the form of broadband transformers at HF, lumped reactive elements at VHF, and microstrip lines with RF chip capacitors at UHF.[5,6]

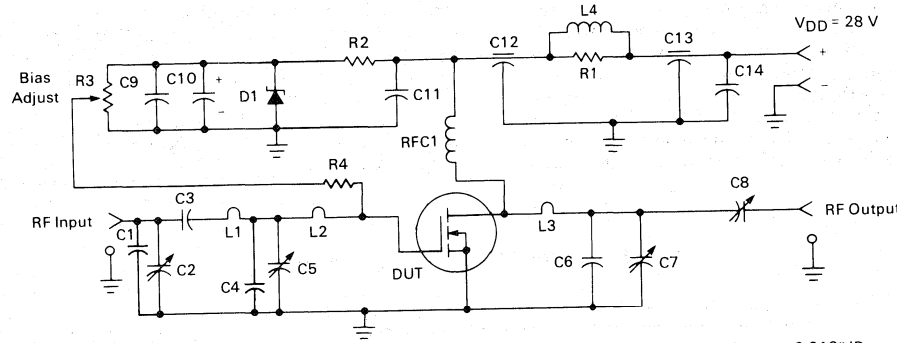
Solid-state power amplifier drain or collector load impedances are set primarily by supply voltage and power level. Therefore, FET and BPT amplifiers with like performance parameters can utilize similar output networks.

The inductive input impedance of high power VHF BPTs usually dictates that the input network design include shunt capacitors placed as close to the transistor package as is physically possible. FETs, with their capacitive input impedances at VHF, do not require these critical capacitive circuit elements.

Figure 1 shows a 125 watt 150 MHz amplifier which utilizes the MRF174 TMOS FET. Note the following items which have been discussed previously:

1. No shunt capacitors at the gate.
2. Resistive bias network operating from the drain supply voltage.
3. Impedance matching networks similar to those of a comparable BPT amplifier (except for item 1 above).

FIGURE 1 — 125 Watt, 150 MHz TMOS FET Amplifier



C1 — 35 pF Unleco
C2, C5 — Arco 462, 5-80 pF
C3 — 100 pF Unleco
C4 — 25 pF Unleco
C6 — 40 pF Unleco
C7 — Arco 461, 2.7-30 pF
C8 — Arco 463, 9-180 pF
C9, C11, C14 — 0.1 μF Erie Redcap
C10 — 50 μF, 50 V
C12, C13 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener

L1 — #16 AWG, 1-1/4 Turns, 0.213″ ID
L2 — #16 AWG, Hairpin 0.25″ × 0.062″
L3 — #14 AWG, Hairpin 0.47″ × 0.2″
L4 — 10 Turns #16 AWG Enameled Wire on R1
RFC1 — 18 Turns #16 AWG Enameled Wire, 0.3″ ID
R1 — 10 Ω, 2.0 W
R2 — 1.8 kΩ, 1/2 W
R3 — 10 kΩ, 10 Turn Bourns
R4 — 10 kΩ, 1/4 W

FET amplifier I_{DQ} (quiescent drain current) is not critical and values in the 10-150 mA range are suggested. I_{DQ} may be varied from less than 100 mA to values approaching Class A operation without large changes in gain and efficiency at full rated power. Linear applications are an exception to this where I_{DQ} should be selected to optimize linearity.

The design of RF impedance matching networks for FET amplifiers is similar to the corresponding task for

This amplifier operates from a 28 volt dc supply. It has a typical gain of 12 dB, and can survive operation into a 30:1 VSWR load at any phase angle with no damage.

The amplifier has an AGC range in excess of 20 dB. This means that with input power held constant at the level that provides 125 watts output, the output power may be reduced to less than 1.0 watt continuously by driving the dc gate voltage negative from its I_{DQ} value. Figure 2 illustrates this performance feature. Note that

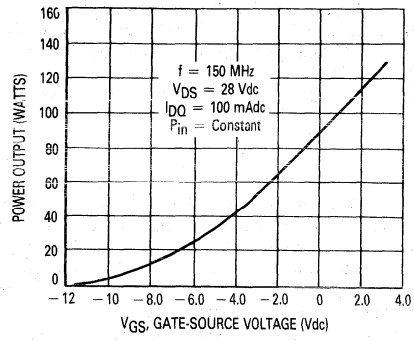


FIGURE 2 — Gain Control Performance of 125 Watt Amplifier

a negative voltage capability would have to be added to the bias system to take full advantage of this AGC performance.

Another useful feature of RF power FETs is that they have less variation of input and output impedances with power level than does a BPT. This characteristic permits the use of small-signal 2 port scattering parameters to develop useful design information for gain, stability, and impedances.[7] S-parameters are often found on RF power FET data sheets. While s-parameters will not provide an exact design solution for high power operation, they do produce a useful first approximation.

Power FETs with outputs below the 40 watt range often have such high gain at HF and VHF that stability problems may be encountered. This problem can be addressed by the classic methods used to stabilize RF small-signal amplifiers — loading of input or output terminals, feedback, or both. Here is an area where s-parameters are useful in calculating the effects of circuit techniques for achieving stability. References 7 and 8 discuss amplifier stability.

Figure 3 shows a 5.0 watt 150 MHz amplifier utilizing the MRF134 TMOS power FET. The MRF134 is a very high gain FET which is potentially unstable at both VHF and UHF. Note that a 68 ohm input loading resistor has been utilized to enhance stability. This amplifier has a gain of 14 dB and a drain efficiency of 55%. Figure 4 shows a 5.0 watt 400 MHz amplifier with a nominal gain of 10.5 dB.

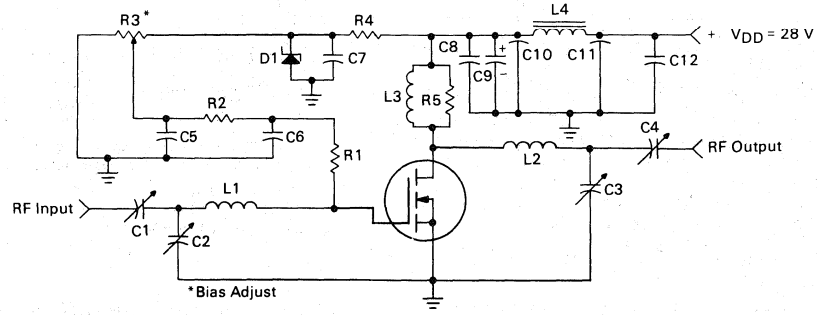
CAUTIONARY NOTES

Some precautions regarding FET RF power amplifiers should be mentioned.

One involves temperature coefficient. Literature abounds with statements that FETs are totally immune to thermal runaway because of their negative temperature coefficient. Actually, many RF power FETs have a positive temperature coefficient over a portion of their operating range. Increasing drain current usually shifts the coefficient from positive to negative. See Figure 5.

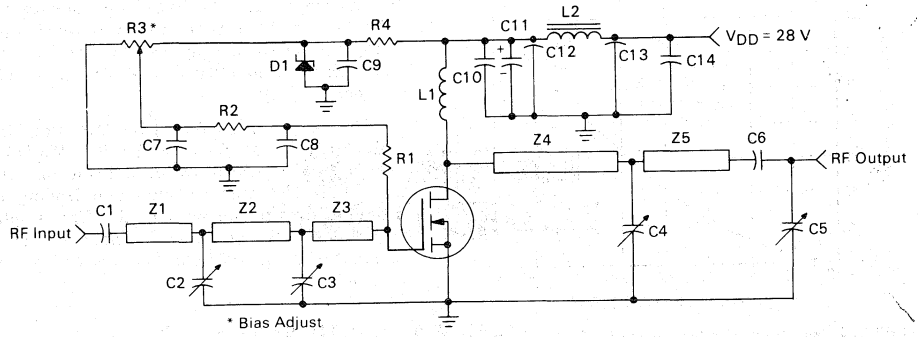
DC bias experiments have been conducted with several RF TMOS FETs. While they all had positive temperature coefficients over a portion of their operating ranges, none exhibited a tendency toward thermal runaway at drain currents ranging from less than 100 mA to full Class A bias. Thermal runaway does not appear to be a problem, but the positive temperature coefficients suggest that the designer should not completely ignore the thermal aspects of dc bias design.

FIGURE 3 — 5.0 Watt, 150 MHz TMOS FET Amplifier



C1, C4 — Arco 406, 15-115 pF
C2 — Arco 403, 3-35 pF
C3 — Arco 402, 1.5-20 pF
C5, C6, C7, C8, C12 — 0.1 μF Erie Redcap
C9 — 10 μF, 50 V
C10, C11 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener
L1 — 3 Turns, 0.310″ ID, #18 AWG Enamel, 0.2″ Long
L2 — 3-1/2 Turns, 0.310″ ID, #18 AWG Enamel, 0.25″ Long
L3 — 20 Turns, #20 AWG Enamel Wound on R5
L4 — Ferroxcube VK-200 — 19/4B
R1 — 68 Ω, 1.0 W Thin Film
R2 — 10 kΩ, 1/4 W
R3 — 10 Turns, 10 kΩ Beckman Instruments 8108
R4 — 1.8 kΩ, 1/2 W
R5 — 1.0 MΩ, 2.0 W Carbon
Board — G10, 62 mils

FIGURE 4 — 5.0 Watt, 400 MHz TMOS FET Amplifier



C1, C6 — 270 pF, ATC 100 mils
C2, C3, C4, C5 — 0-20 pF Johanson
C7, C9, C10, C14 — 0.1 μF Erie Redcap, 50 V
C8 — 0.001 μF
C11 — 10 μF, 50 V
C12, C13 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener
L1 — 6 Turns, 1/4" ID, #20 AWG Enamel
L2 — Ferroxcube VK-200 — 19/4B
R1 — 68 Ω, 1.0 W Thin Film
R2 — 10 kΩ, 1/4 W
R3 — 10 Turns, 10 kΩ Beckman Instruments 8108
R4 — 1.8 kΩ, 1/2 W
Z1 — 1.4" × 0.166" Microstrip
Z2 — 1.1" × 0.166" Microstrip
Z3 — 0.95" × 0.166" Microstrip
Z4 — 2.2" × 0.166" Microstrip
Z5 — 0.85" × 0.166" Microstrip
Board — Glass Teflon, 62 mils

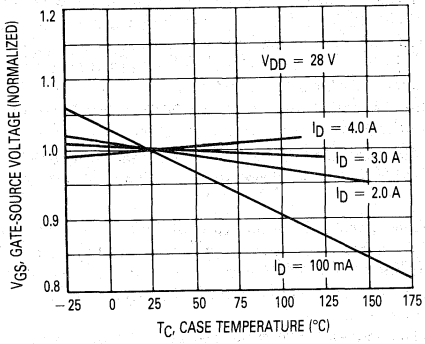


FIGURE 5 — Gate-Source Voltage versus Case Temperature For Constant Values of Drain Current MRF174

A second potential problem is the danger of permanent damage to FET gates from static electricity. Fortunately, the larger capacitances of power devices reduce this danger. No special precautions have been taken to protect the FETs described from static damage, and there were no failures known to be caused by static induced voltages. However, it is worthwhile to exercise the usual precautions taken in handling all MOS devices.

SUMMARY

The construction, characteristics, and advantages of RF power FETs have been described with emphasis on the VHF frequency range. Particular attention was given to the excellent gain control characteristics of these devices.

REFERENCES

1. *Field Effect Transistors in Theory and Practice,* Motorola Semiconductor Sector Application Note AN-211A.
2. *The Radio Amateur's Handbook,* 59th Edition, Chapter 4, ARRL, Inc., Newington, CT.
3. H. Granberg, *Power MOSFETs versus Bipolar Transistors,* R.F. Design Magazine, Nov./Dec., 1981. Also available as Motorola Semiconductor Sector Application Note AN-860.
4. D. DeMaw, *Practical Class-A and Class-C Power-FET Applications at HF,* paper presented at Midcon Electronic Show & Convention, December, 1982.
5. H. Granberg, *Broadband Transformers and Power Combining Techniques for RF,* Motorola Semiconductor Sector Application Note AN-749.
6. B. Becciolini, *Impedance Matching Networks Applied to RF Power Transistors,* Motorola Semiconductor Sector Application Note AN-721.
7. *S-Parameters ... Circuit Analysis and Design,* Hewlett-Packard, Palo Alto, CA, Application Note 95.
8. R. Hejhall, *RF Small-Signal Design using Two-Port Parameters,* Motorola Semiconductor Sector Application Note AN-215A.

800 MHz TEST FIXTURE DESIGN

by
DAN MOLINE
Product Manager
Landmobile Power Products

Although this article presents techniques for the general case of UHF-800 MHz circuit design, the emphasis is placed specifically on test fixture design for 800 MHz. Text fixtures tend to be the last consideration for most RF power amplifier development programs, yet they are the most valuable tool available for measuring and maintaining device consistency. Minimum power gain, collector efficiency and broadband performance requirements, though they are always detailed in some form of written specification, are meaningless unless they are demonstrated and controlled by a test fixture. A good test fixture will assure correlation between the customer and vendor and function as a trouble shooting tool in the event of radio problems. When alternate sources are pursued for a stage, test fixtures can shorten qualification cycles. But the prevention of gradual shifts in RF performance over the lifetime of a product is the major purpose of a test fixture.

Motorola has recognized the importance for good test fixtures and has established general guidelines for their implementation.

Each hi-tech product is tied to a well defined test fixture, which has the following general specifications:

- Broadband performance, demonstrating typical characteristics throughout the band. (Ex.: UHF; 450–512 MHz, 800; 800–870 MHz)
- A 3" x 5" mechanical format, which is rugged for high volume test applications.
- Simple RF match construction to represent realistic radio performance.
- Devices must meet all minimum test requirements at the specified test frequency. UHF: 470 MHz, 800: 870 MHz.

The repeatability, mechanical ruggedness and broadband performance are all very important factors needing consideration in the design of test fixtures. The remainder of this article goes into detail, using the MRF846 as an example.

The schematic representation of the fixture outlined in this article is shown below (Figure 1).

C_I and C_O represent the shunt capacitors at the input and output (respectively) which cancel most of the inductive reactance associated with the transistor's input and output impedance. Mini clamped-mica capacitors are used for these components and are physically located beneath the common lead wear blocks. Inductance "L" is introduced by the input (and output) wear blocks. Because of this parasitic inductance, L, trimmer capacitors (C'_I or C'_O) are required to transform the now reactive impedance back to real before launching off into the $\lambda/4$ transmission lines.

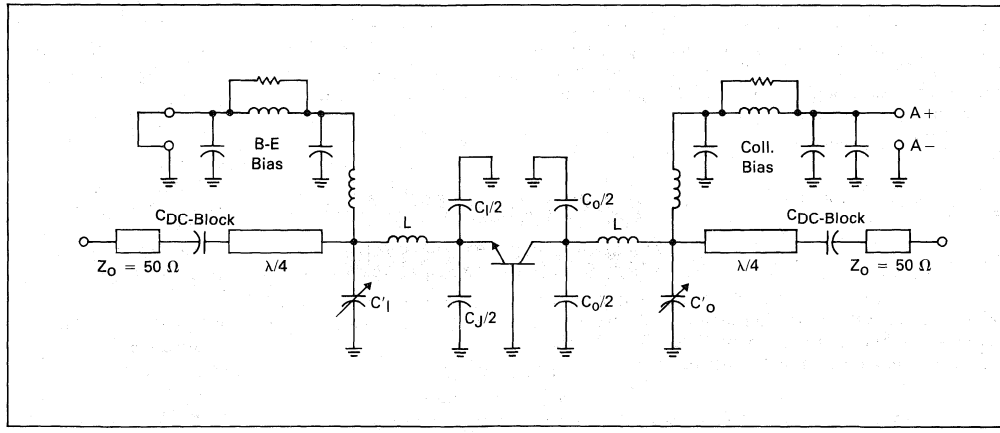


FIGURE 1 — SCHEMATIC REPRESENTATION OF TEST FIXTURE

The transistor's input and output impedance can be represented as a combined series resistor and inductor as shown in Figure 2.

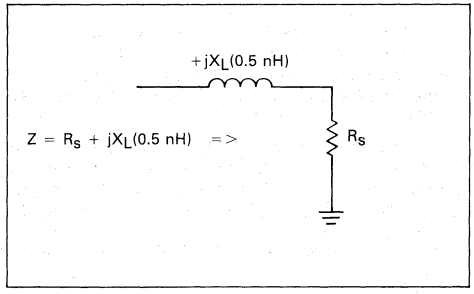


FIGURE 2 — EQUIVALENT CIRCUIT FOR Z_{in} OR Z_{out}

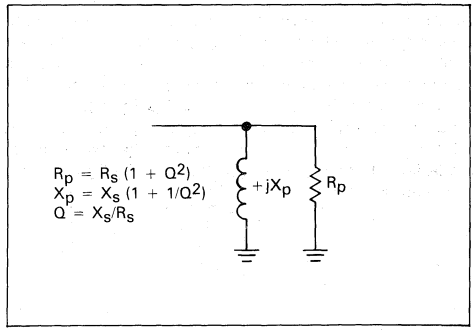


FIGURE 3 — PARALLEL EQUIVALENT CIRCUIT

This series combination can be transformed into a parallel equivalent by using the equations shown in Figure 3. The capacitors C_I and C_O are selected by calculating the value necessary to form a parallel resonance with X_p. Since all capacitors have a finite, series lead inductance, the capacitor is actually considered as a simple series resonant circuit. The resulting effect is the capacitance is always higher than the marked value and goes through resonance at some frequency. Mini clamped-mica capacitors are recommended for test fixture design due to the very low parasitic inductance associated with them which increases the usable range of capacitances. (They are also extremely high "Q"). A typical measured series inductance for clamped-mica capacitors is about 0.5 nH. The equivalent capacitance is calculated by subtracting the series lead inductance from the capacitive reactance, or $X_C(\text{equiv}) = X_C - X_{L(0.5\ nH)}$.

Since two capacitors are used in parallel, the total capacitance is derived as shown in Figure 4.

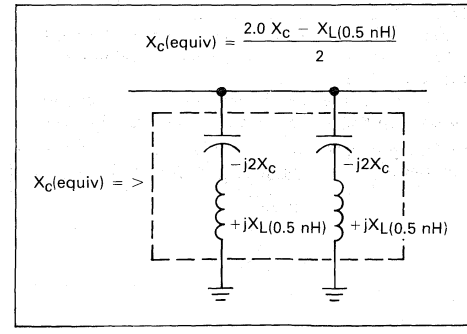


FIGURE 4 — EQUIVALENT REACTANCE FOR CAPACITORS IN PARALLEL

A value of 2.0 X_c is used in the above example since each capacitor will contribute only ½ to the total capacitance. By setting X_c(equiv.) equal to the parallel equivalent reactance calculated in Figure 3, the exact capacitor values may be determined.

$$X_p = \frac{2.0\ X_c - X_{L(0.5\ nH)}}{2}$$

$$X_c = \frac{2.0\ X_p + X_{L(0.5\ nH)}}{2} \qquad (X_c = 1/2\ fC)$$

$$C = \frac{1}{\pi f\,(2.0\ X_p + X_{L(0.5\ nH)})}$$

Introducing an actual example at this time should help in explaining the remaining steps involved in a test fixture design. The MRF846 is a 40 W, 12.5 V, 800 MHz device whose input and output impedances are:

TABLE 1 — Z_{in}, Z_{out} FOR MRF846

Frequency	Z_{in}	Z_{out}
800 MHz	1.1 + j4.8	1.20 + j2.4
836 MHz	1.0 + j4.9	1.15 + j2.5
870 MHz	1.0 + j5.0	1.10 + j2.7
900 MHz	0.9 + j5.1	1.10 + j2.8

Since X_p will vary as a function of frequency, C_I and C_O need only be calculated for one point within the frequency band. Typically, the input response of an RF power transistor is optimized about the center of the band. Hence, the input R_p and X_p are generally calculated at this frequency [$(f_h + f)/2$].

The output response is different. If C_O were selected for a resonance to occur with X_p at band-center, an unacceptable performance roll-off would be seen at the upper end of the frequency band. Overall performance is best when C_O is calculated at a frequency within 20% of the upper end of the band. Since device gain increases as frequency decreases, the performance at lower frequencies is generally no problem.

Using the MRF846 as an example, input and output capacitor values may be determined as follows:

INPUT:
Frequency = 836 MHz

$Z_{in} = 1 + j4.9$
$= 4.9 \quad Q = 4.9/1$

$X_p = 4.9\left(1 + \frac{1}{(4.9)^2}\right)$
$= 5.1\ \Omega$

$X_{L(0.5\ nH)} = 2.0\pi (836x10^6)(0.5x10-9)$
$= 2.63\ \Omega$

$C = 1/[\pi(836x10^6)(2x5.1+2.63)] = 29.7$ pF

2–15 pF Capacitors would be the best choice.

OUTPUT:
Frequency = 870 MHz

$Z_o = 1.1 + j2.7$; $Q = 2.7/1.1$
$= 2.45$

$X_p = 2.7\left(1 + \frac{1}{(2.45)^2}\right)$
$= 3.15\ \Omega$

$X(0.5\ nH) = 2.0\pi (870x10^6)(0.5x10-9)$
$= 2.7\ \Omega$

$C = 1/[\pi(870x10^6)(2x3.15+2.7)] = 40.7$ pF

2–20 pF Capacitors would be the best choice.

(20 pF Capacitors were not available, so an 18 pF & a 24 pF capacitor were chosen instead. The total C = 42 pF.)

Though the MRF846 test fixture used at Motorola does use these capacitor values, the above calculations may act only as a good starting point. Empirical measurements and more precise impedance measurements for a given application may result in minor deviations from these values.

Assuming no additional circuit parasitics had to be accounted for, the quarter wave transmission line sections could now be determined. The input (and output) fixture wear blocks do, however, contribute additional series lead inductance to the impedances. These inductances are counteracted by the trim capacitors C′I and C′O. The wear block inductance could be calculated and then used to determine the proper capacitance values. However, since there are other, less obvious frequency and grounding effects which may influence the impedance transformation, it is a more practical (and generally a more accurate) procedure to measure the impedance which will be transformed by the transmission line to 50 Ω.

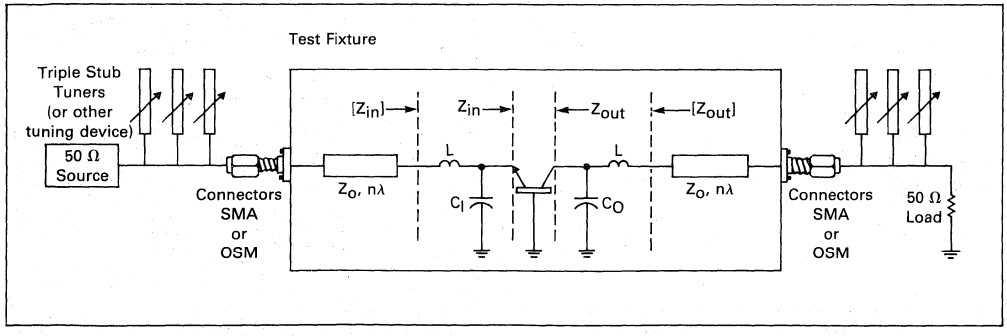


FIGURE 5 — BASIC CIRCUIT TO MEASURE Z_{in}, Z_{out}

The capacitors C_I and C_O should be mounted into the test fixture and a known characteristic impedance transmission line soldered into place as shown below in Figure 5.

Triple stub tuners are used on the input and output to tune for maximum output power and minimum reflected power at various frequencies throughout the band. Band edges and band center are generally adequate for a good circuit design. Due to higher impedance levels produced by adding C_I and C_O, (Z_{in}) and (Z_{out}) are measured instead of the real transistor impedances, Z_{in} and Z_{out}. Also, by measuring impedances in the actual applications fixture, the design can be optimized for the particular fixture. Perhaps a maximum gain tuning point is not what is desired. Obtaining impedances for an efficiency/gain compromise may be more desirable. If this is the case, an impedance table for the appropriate conditions may be obtained. It is then for these impedances that C_I, C_O and Z_o will be calculated.

The procedure for obtaining the impedances is simple and requires a vector voltmeter (VVM) or a network analyzer. Both are used at Motorola, but a vector voltmeter is less expensive and if used with a high directivity directional coupler, (>40 dB), is very accurate. The set-up is constructed as shown in Figure 5. With frequency set, stub tuners are adjusted for the desired performance. Again, using the MRF846 as an example, numbers shown in Table 2 were measured for P_{in} = 12.0 W, V_{CC} = 12.5 V.

The output stub tuners were adjusted for maximum gain at each frequency and the input stub tuners were adjusted for zero watts reflected power. After each measurement, the impedance presented to the fixture by the triple stub tuner and load (or source) combination is measured by the vector voltmeter. The impedance is then translated by the transmission line used in the test fixture to obtain (Z_{in}) and (Z_{out}). In the above example a 26 Ω, 0.309λ (@836 MHz) transmission line was arbitrarily chosen to be in the MRF846 measurements. By using the equation: $Z \angle\theta = R_o [(1 + \Gamma\angle\theta) / (1 - \Gamma\angle\theta)]$ or various computer or calculator programs, the transformation is easily calculated. The most important part of the whole procedure is obtaining an accurate measurement from the stub tuners. Prior to making any measurements, the vector voltmeter must be referenced to a short (180° on a Smith Chart). As a means of accounting for the errors introduced by the connectors at the fixture's input and output, that same connector is used for a referencing short as shown in Figure 6.

The measurement reference plane is now the edge of the connector used on the test fixture, which is also the beginning of the transmission line. Assuming the same reference plane is maintained during the measurements, an accurate impedance value will be produced. A good technique for maintaining the appropriate reference plane is accomplished by creating a new connector to measure the triple stub tuners. Two connectors are attached as shown in Figure 7.

TABLE 2 — PERFORMANCE OF MRF846 versus FREQUENCY

806 MHz	838 MHz	870 MHz
P_{out} = 50.0 W Eff. = 53.3% Prefl. = 0 W	P_{out} = 48.3 W Eff. = 55.2% Prefl. = 0 W	P_{out} = 44 W Eff. = 58% Prefl. = 0 W

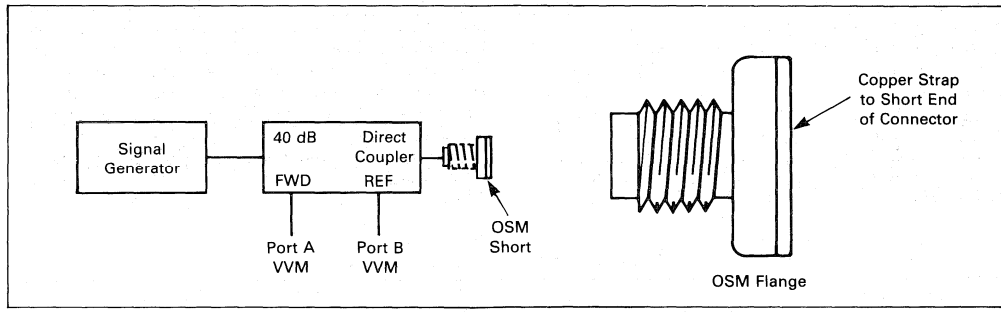


FIGURE 6 — ESTABLISHING REFERENCE PLANE

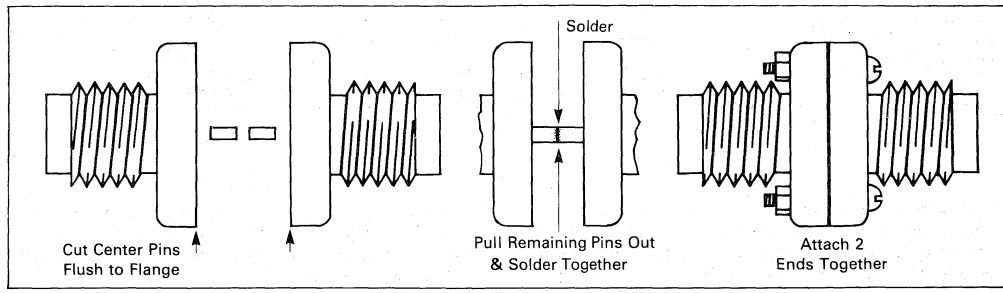


FIGURE 7 — MAINTAINING REFERENCE PLANE

The triple stub tuner, load combination may now be measured with an adequate degree of accuracy using the test setup shown in Figure 8.

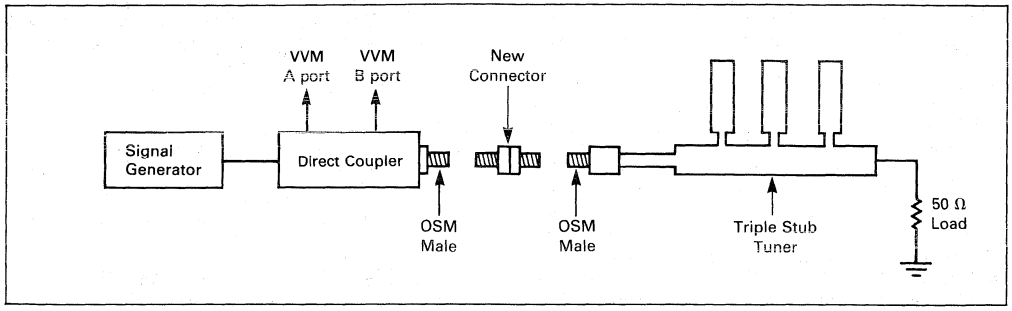


FIGURE 8 — TEST SETUP TO MEASURE STUB TUNER W/LOAD

Repeat the process for the input stub tuner combination. Two numbers are obtained for each frequency which (Z_{in}) and (Z_{out}) can be calculated from, as shown in the MRF846 example below:

TABLE 3 — MEASURED Z VALUES FOR TEST FIXTURE

Frequency		Measured $\Gamma\angle\theta$	$\Gamma\angle\theta$ converted to Impedance in Ohms	Impedance Transformed Over 26 Ω Line in Ohms
806 MHz	INPUT	$0.35\angle 155°$	24.97 + j8.42	20.72 − j5.64 = [Z_{in}*]
	OUTPUT	$0.37\angle 144°$	24.86 + j12.53	17.72 − j6.66 = [Z_{out}*]
838 MHz	INPUT	$0.26\angle 166°$	29.78 + j3.98	21.35 + j0 = [Z_{in}*]
	OUTPUT	$0.22\angle 154°$	33.30 + j6.58	18.68 + j.74 = [Z_{out}*]
870 MHz	INPUT	$0.14\angle -169°$	38.25 − j1.99	20.21 + j6.92 = [Z_{in}*]
	OUTPUT	$0.07\angle -158°$	44.10 − j2.24	17.90 + j8.3 = [Z_{out}*]

Note: [Z_{out}*] is conjugate of [Z_{out}]
[Z_{in}*] is conjugate of [Z_{in}]

The new impedances can be obtained by using a Smith Chart or using the equation $Z\angle\theta = R_0\,[(1 + \Gamma\angle\theta)/(1 - \Gamma\angle\theta)]$. These impedances (shown in the last column of Table 3) are the impedances which the test fixture will be optimized around. Once again, it is convenient to convert these numbers into parallel equivalents. By doing so, the values of C'_I and C'_O become more obvious. Table 4 shows this process.

TABLE 4 — CONVERSION OF Z VALUES TO C VALUES

Series Impedance [Z_{in}] & [Z_{out}]	R_p	X_p	Capacitance Required
20.72 + j5.64	22.26	j81.8	2.42 pF C'_I
17.72 + j6.66	20.2	j53.8	3.67 pF C'_O
21.35 + j0	21.35	—	0.0 pF C'_I
18.68 + j.74	18.7	j472	0.40 pF C'_O
20.21 − j6.92	21.6	−j68.3	−2.68 pF C'_I
17.90 − j8.3	21.75	−j46.9	−3.90 pF C'_O

From Table 4, notice the calculated values of C_I and C_O come close to giving the desired frequency response. C'_I is zero at the band center, indicating the capacitors selected for the input are optimum. The values for C'_O produce a slight skew in performance toward the high end of the band. Capacitor values for the output could be reduced slightly, but they will remain the same until final fixture performance is determined.

Since C'_I and C'_O are very small capacitor values, little or no capacitance is actually needed for C'_I or C'_O. However, to allow minor tuning adjustments, a small trimmer capacitor is included at the wear block/transmission line interface.

The final calculation which needs to be performed is that of finding the optimum characteristic impedance for the transmission line. The recommended approach for doing this is to use a computer optimization program which will iterate any number of variables for a desired frequency response. The variables available to be optimized at this point are Z_0, C'_I and C'_O and even $n\lambda$ (transmission line length). Z_0, C'_I and C'_O are the very minimum variables.

In the example of the MRF846, where input R_p varies from 22.3 Ω to 21.6 Ω over the frequency band, a close approximation can be had by using a mean value of 21.9 Ω. This results in a Z_0 of 50 x 21.9 = 33 Ω. The output R_p starts at 20.2 Ω, dips to 18.7 Ω and goes back up to 21.75 Ω. Using the same method as before, Z_0 is calculated as 50 x 20.2 = 31.7 Ω where 20.2 Ω is the mean value of 18.7 and 21.75. Using a computer optimization program, a 32 Ω, quarter wave transmission line is optimum for the input and a 30 Ω quarter wave line is optimum for the output. These are the values used in the MRF846 test fixture.

After constructing the MRF846 test fixture and tuning the small trimmer capacitors for best overall gain and input reflected response, the average data shown in Figure 9 was obtained.

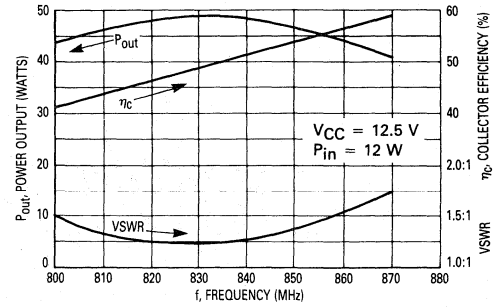


FIGURE 9 — TEST FIXTURE PERFORMANCE OF MRF846

The goal was to demonstrate 12/40 W across the band with less than 2.0:1 input VSWR and greater than 45% collector efficiency. Further optimization could be done by performing impedance measurements on additional transistors or characterizing the test fixture more accurately. However, the above performance is very satisfactory to the required performance. The best compromise for a second pass fixture would be to trade-off gain at 806 and 838 MHz for efficiency, and redesign input and output matching networks for the new impedance tables. This, of course, is only one of the many procedures which may be followed in developing an 800 MHz test fixture.

MOUNTING TECHNIQUES FOR POWERMACRO TRANSISTOR

Prepared by:
Harry Swanson
RF Product Development/Applications Engineer
Motorola Semiconductor Sector

For reliable operation, the PowerMacro plastic molded transistor must be properly mounted. Methods of mounting and heatsinking are discussed. Tradeoffs of implementation and thermal performance are considered.

INTRODUCTION

The Stripline Opposed Emitter (SOE) package when used to mount an RF power transistor for output power levels less than 2.0 watts is excellent electrically but relatively expensive for the function performed. This application note describes an equally effective electrical package called the PowerMacro package.

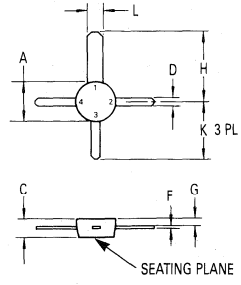
The primary advantages of the PowerMacro package are (1) its low cost and (2) that it is a drop-in replacement for the 0.204″ SOE pill or stud package using the same transistor die. Note that this package will also substitute for most low power applications of an SOE device with comparable RF and thermal performance.

The PowerMacro package has excellent thermal properties; however, it is essential to utilize proper mounting techniques. Therefore, this application note emphasizes thermal considerations and methods of heat sinking the package.

DESCRIPTION OF THE POWERMACRO PACKAGE

Figure 1 is the case outline drawing of the Power Macro package. It is similar to the Macro-X package except for the wider collector lead. Figure 2 is a cut away view showing the component parts of a PowerMacro package. The package consists of an epoxy molded copper leadframe which has a 100 mil wide collector lead. A transistor die is silicon-gold eutectic die bonded to the collector lead and is wirebonded in a manner similar to the SOE package. Completion of the assembly process is accomplished by molding the copper leadframe and tin plating the four leads.

STYLE 2:
PIN 1. COLLECTOR
2. EMITTER
3. BASE
4. EMITTER



DIM	Millimeters		Inches	
	Min	Max	Min	Max
A	4.44	5.21	0.175	0.205
C	1.90	2.54	0.075	0.100
D	0.84	0.99	0.033	0.039
F	0.20	0.30	0.008	0.012
G	0.63	1.01	0.025	0.040
H	8.84	9.72	0.348	0.383
K	7.24	8.13	0.285	0.320
L	2.46	2.64	0.097	0.104

FIGURE 1 — Case Outline Drawing of the PowerMacro Package

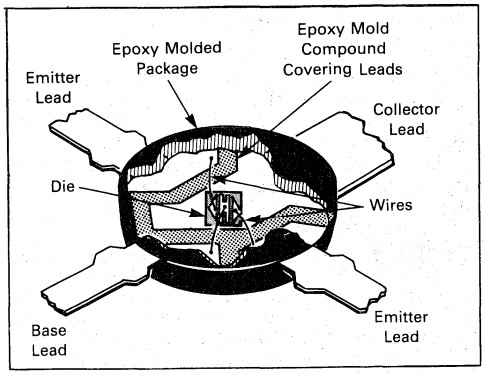


FIGURE 2 — Cut Away View of the PowerMacro Package

THERMAL RATING OF THE POWER MACRO TRANSISTOR

The RF PowerMacro transistor is guaranteed to have a certain thermal performance defined by the total device dissipation, P_D, at a certain case temperature, T_C, which is measured on the collector lead immediately adjacent to the package body. The parameters are defined for T_J max of 150°C. In order to use the thermal data presented on the RF data sheet, the concepts and ground rules for heat flow must be defined. Table 1 compares the thermal parameters to their more familiar electrical analogs. The task of the designer is to get the heat out the collector lead (case) of the PowerMacro transistor. This presents a classical heat transfer problem ideally calling for an "infinite heat sink" which can absorb any amount of heat with no temperature rise, ΔT, whatsoever. In a realistic sense, such a heat sink does not exist; however, a practical solution can be obtained. A practical heat sink is characterized by a certain temperature rise, ΔT, for a given ambient condition with a known amount of heat input or power dissipation, P_D.

When the collector lead and ambient temperature of PowerMacro transistor and power dissipation are known, then the thermal resistance from case-to-ambient can be calculated. First, the power being dissipated in the device, P_D, is obtained by:

$$P_D = P_{DC} + P_{in} - P_{out} - P_{ref}$$

Where: P_D = Power dissipated in transistor in watts;
P_{DC} = DC power into transistor in watts;
P_{in} = RF power into transistor in watts;
P_{out} = RF power out of the transistor in watts;
P_{ref} = RF input power reflected in watts;
P_D is used in the equation below to obtain θ_{CA}.

$$\theta_{CA} = \frac{T_C - T_A}{P_D}$$

Where: θ_{CA} = Thermal resistance device case to ambient
T_C = Device case temperature
T_A = Ambient temperature
The junction temperature under a given operating condition is defined by:

$$T_J = (\theta_{JC} + \theta_{CA})\, P_D + T_A$$

Where: T_J = Junction temperature
θ_{JC} = Published thermal resistance junction-to-case.

Since θ_{JC} is fixed by the transistor type used, the user can only control the junction temperature by θ_{CA}.

A low θ_{CA} requires an effective heat sink and interface between the case and heat sink. In general, an effective heat sink requires that materials with high thermal conductivity and high specific heat be used. A table of thermal properties for various materials is found in the Appendix. A well designed interface and heat sink requires that all thermal paths be as short as possible and of maximum cross sectional area.

TABLE 1. Thermal Parameter and Their Electrical Analogs

Thermal			Electrical Analog	
Symbol	Parameter	Units*	Symbol	Parameter
ΔT	Temperature Difference	°C	V	Voltage
H	Heat Flow	Watts	I	Current
θ	Thermal Resistance	°C/ Watts	R	Resistance
γ	Heat Capacity	$\frac{\text{Watt-Sec}}{°C}$	C	Capacity
K	Thermal Conductivity	$\frac{\text{Cal}}{\text{Sec-cm}}$ °C	σ	Conductivity
Q	Quantity of Heat	Cal	q	Charge
t	Time	Sec	t	Time
$\theta\gamma$	Thermal Time Constant	Sec	RC	Time Constant

*Note the one major difference in thermal and electrical units — Q is in units of energy, whereas q is simply charge. Hence, H is in units of power and may be equated to an electrical power dissipation.

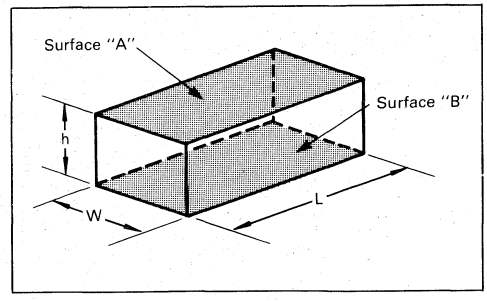


FIGURE 3 — Bar of Conducting Material

The thermal resistivity from Surface A to Surface B in the conductive bar shown in Figure 3 is:

$$\theta = \frac{h}{KWL} = \frac{h}{KA}$$

Where: h = Length of thermal path
A = Cross-sectional area of thermal path
K = Thermal conductivity

In order to define the thermal resistance factors still further for our purpose, θ_{CA} is defined as:

$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

Where: θ_{CS} = Interface thermal resistance — case to heat sink
θ_{SA} = Heat sink thermal resistance — heat sink to ambient

Thus the thermal resistance, junction-to-ambient is the sum of individual components and T_J is then defined as:

$$T_J = P_D (\theta_{JC} + \theta_{CS} + \theta_{SA}) + T_A$$

This gives the basic thermal resistance model for the PowerMacro as indicated by Figure 4.

The thermal resistance of the transistor (the junction-to-case thermal resistance), θ_{JC}, is not constant; it is a function of biasing and temperature as given on the data sheet. The thermal resistance of the heat sink is also variable; it decreases as ambient temperature increases.

The interface thermal resistance, θ_{CS}, is affected by the mounting technique and interface material used.

Since this thermal resistance may be significant compared to the others, it will receive primary emphasis in the following section on mounting techniques.

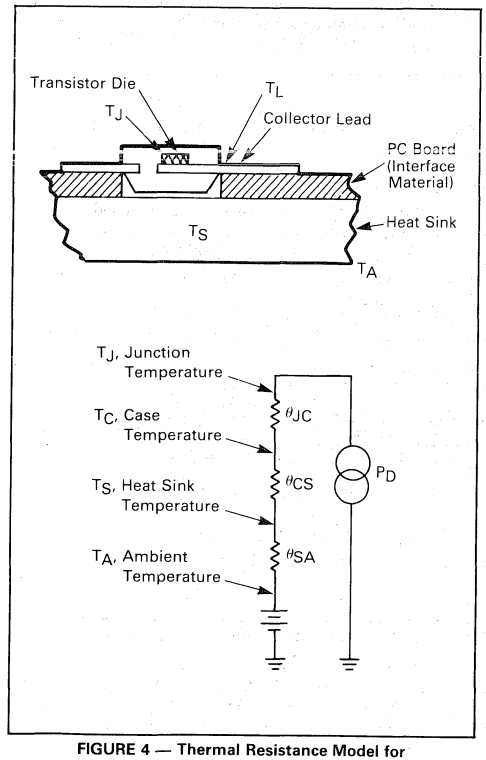


FIGURE 4 — Thermal Resistance Model for the PowerMacro Transistor

MOUNTING TECHNIQUES FOR POWERMACRO

The available heat sink will vary depending on the application. In the case of the handheld radio, the heat sink is relatively small and lightweight. In the case of a predriver in a mobile radio the heat sink is relatively large but it is shared with other devices of higher power dissipation. In general, the size and weight of the heat sink should be as small as possible.

The intent of this section is to discuss in detail the different techniques and tradeoffs involved in reducing the thermal interface resistance in the PowerMacro.

The wide lead collector of the PowerMacro offers an excellent thermal path from the transistor chip. This wide lead should be utilized effectively to provide the best thermal interface. Since this lead is the output of the device, it is necessary to consider RF matching and DC biasing. Thus, the lead is usually mounted to some PC board material such as G-10, glass teflon, alumina, or beryllium oxide (BeO). Table A1 in the Appendix lists the typical thermal data from IR scans of the MRF553 PowerMacro transistor (1.5 Watts P_{out} — 7.5/12.5 V VHF device). The analysis compares two PC board materials:

1. G-10
2. Alumina

for various operating conditions of P_{out}, P_D, T_J (die junction temperature), T_C (collector lead temperature), and T_S (heat sink temperature) and $T_A \approx 25°C$.

Figure A1 shows the circuit used to provide the thermal data of the MRF553 device mounted to a 62 mil thick G-10 PC board. The device is soldered to the PC board which is mounted to a 3" x 5" x 3/4" aluminum heat sink.

Figure A2 shows the circuit used to provide the thermal data of the MRF553 device mounted with alumina interface. The device is soldered into a specially constructed socket (see Figure A3) which is mounted to a 3" x 5" x 3/4" aluminum heat sink. The socket is copper and uses 28 mils thick alumina substrates (195 mils x 250 mils) with 62 mils thick copper tabs (125 mils x 250 mils) on the input and output. These components are soldered together using high temperature solder.

A comparison of the data in Table A1 shows the relative performance of the two mounting techniques. IR Scan II of the alumina/copper mounting technique clearly shows its superior thermal performance. Comparing the data at $P_D \approx 1.9$ watts for IR Scan I (G-10 PC board mounting) and IR Scan II (alumina/copper mounting) demonstrate the better thermal interface using alumina/copper. θ_{JS} for the alumina/copper mounting is 30.7°C/W while θ_{JS} for the G-10 PC board is 39°C/W.

As expected, the θ_{JL} is approximately the same for the two mounting techniques. The difference in θ_{JS} is dependent on the mounting technique used. The resulting θ_{CS} is calculated from the IR scan data by:

$$\theta_{CS} = \theta_{JS} - \theta_{JL}$$

6

Thus for IR Scan I (G-10 mounting):

θ_{CS} = (39–23.2) °C/W = 15.8°C/W

Whereas, for Scan II (alumina/copper mounting):

θ_{CS} = (30.7–24.4) °C/W = 6.3°C/W

Therefore, the IR scan results show a marked improvement in thermal performance when using the alumina/copper.

The heat spreading effects of the epoxy mold compound are also analyzed by IR scan of a molded device and an unmolded device. The molded device was chemically etched to expose the surface of the transistor die while maintaining the maximum epoxy compound around the transistor leads. The unmolded device was soldered into the RF circuit in leadframe form and then the lead interconnects were trimmed to make the part functional.

A comparison of RF Scan I and RF Scan III shows that the epoxy mold compound aids in spreading the heat from the collector lead to the other three leads. For example, at $P_D \approx 1.9$ watts, the junction temperature, T_J, of the molded device is only 106.2°C versus 154.3°C for the unmolded device. Thus, the heat transfer ability of the epoxy mold compound is significant.

Additional heat transfer can be realized by applying a small amount of heat sink compound to the heat sink side of the PowerMacro package and by mounting the device so that the package body contacts the heat sink. The thermal conductivity of the heat sink compound (K = 0.0018) is close to that of the epoxy mold compound (K = 0.0026) and it is 3 times better than G-10 (K = 0.0056). Table A2 in the Appendix lists and defines the thermal conductivity K, the specific heat S and mass density P of various materials.

SUMMARY

This application note utilizes the IR scan results in Table A1 to quantify the tradeoffs in performance of the two mounting techniques. A more rigorous analysis should be made by the designer when considering a particular application of a PowerMacro device. In a particular application, there usually are certain constraints, such as:

(1) Ambient and operating conditions
(2) Available heat sink size
(3) Available circuit layout space
(4) PC board material choice
(5) Assembly manufacturing techniques that are available and cost effective

These constraints may limit the designer's available options in providing the best interface and heat sink for the PowerMacro transistor.

The PowerMacro package is an excellent RF low power package. With proper mounting and applications of device specifications, the transistor will function reliably. The data sheet specifications for θ_{JL}, T_L, and P_D are based on mounting the device to G-10 PC board or equivalent at T_A = 25°C.

APPENDIX

Table A1 lists the IR scan results of the MRF553 PowerMacro transistor comparing two PC board materials. The mounting and RF circuit techniques are shown in Figures A1, A2 and A3.

TABLE A1. IR Scan Results for MRF553 PowerMacro

Mounting Technique	P_{out} (W) f = 175 MHz	P_{in} (mW) / P_R (mW)	V_{CC} (Vdc) / I_C (A)	P_D (W)	Die Temp. T_J (°C) Hot Spot	Die Temp. T_J (°C) Aver.	Collector Lead Temp. T_L (°C)	θ_{JL} Aver. (°C/W)	θ_{JL} Hot Spot (°C/W)	Ckt. Heatsink Temp. T_S (°C)	θ_{JS} Aver. (°C/W)	θ_{JS} Hot Spot (°C/W)	T_A (°C) Ambient Temp.
IR Scan I:	1.0	55 / 3.8	12.5 / 0.20	1.55	96.62	99.5	55.3	25.3	26.65	32	40.3	41.7	25
G-10 PC Board with Epoxy (Case Material)	1.5	88 / 8.4	12.5 / 0.25	1.70	101.40	99.1	59.7	23.2	24.5	32	39.5	40.8	25
	2.0	140 / 14	12.5 / 0.30	1.88	108.9	106.2	62.7	23.2	24.6	33	38.95	40.4	25
	2.5	222 / 21.5	12.5 / 0.35	2.08	120	116.9	67.35	23.8	25.3	35	39.4	40.9	25
	3.0	380 / 40	12.5 / 0.41	2.46	138.35	134.8	74.2	224.6	26.1	37	39.75	41.2	25
IR Scan II:	1.5	75 / 3.7	12.5 / 0.200	1.07	68	66.7	33.8	24.5	25.7	28	36.2	37.4	25
Alumina/ Copper Board with Epoxy (Case Material)	2.0	135 / 13	12.5 / 0.252	1.27	73.8	71.9	35.3	24.3	25.8	29	33.8	35.3	25
	2.5	350 / 60	12.5 / 0.33	1.92	90	88	41.1	24.4	25.5	29	30.7	31.8	25
	3.0	710 / 165	12.5 / 0.430	3.0	120.5	117.7	48.8	23.4	24.3	29	29.7	30.7	25
	3.2	1000 / 300	12.5 / 0.473	3.4	136.8	131.3	49	24.2	25.8	29	30.1	31.7	25
IR Scan III:	1.0	52 / 7.6	12.5 / 0.20	1.54	138.99	137.1	91.9	29.2	30.5	28	70.8	72.1	25
G-10 PC Board with No Epoxy (Case Material)	1.5	84 / 11	12.5 / 0.25	1.69	146.28	143.5	95.6	28.2	29.8	28	68	69.7	25
	2.0	140 / 16	12.5 / 0.30	1.87	156.64	154.3	101.35	28.35	29.6	28	67.4	68.6	25

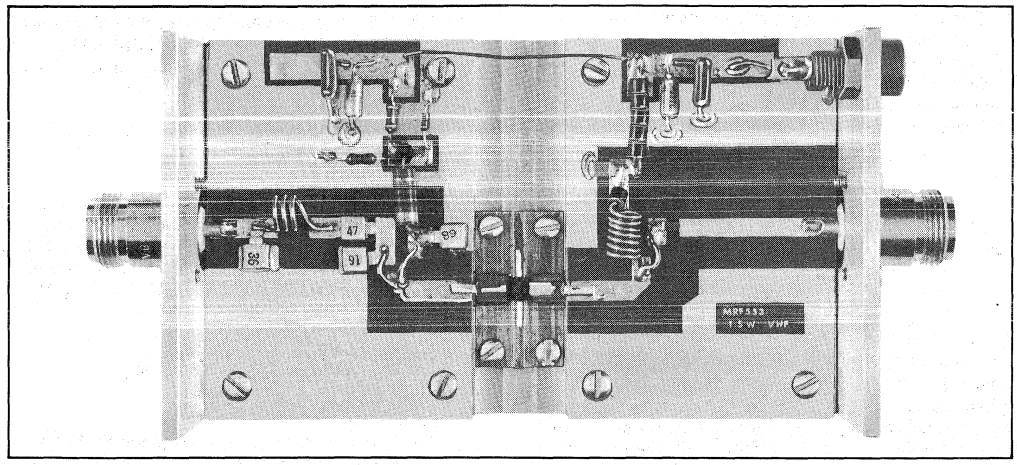


FIGURE A1 — Circuit Using G-10 PC Board

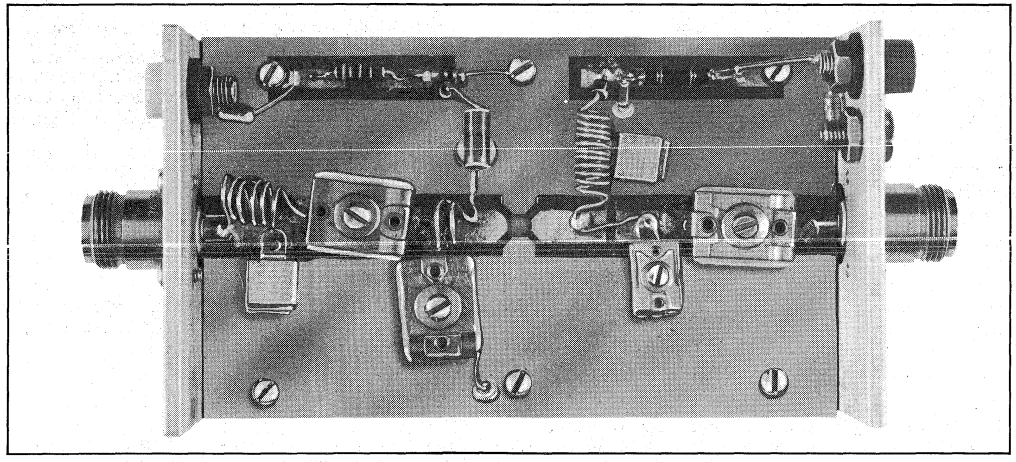


FIGURE A2 — Circuit Using Alumina/ Copper Socket

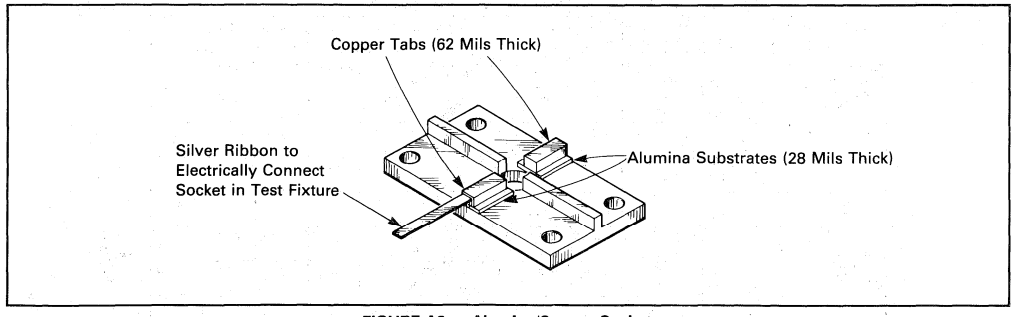


FIGURE A3 — Alumina/Copper Socket

6

The IR scans were made using a Barnes radiometric scope (Model No. RM2). The transistor's active area was IR measured at 6 points to adequately map the junction temperature. Also, the collector lead was IR measured immediately adjacent to the body of the package to obtain the case temperature, T_L of the device (see Figure A4).

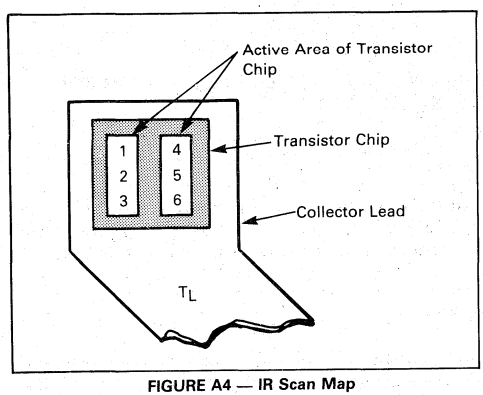


FIGURE A4 — IR Scan Map

Each operating condition chosen was allowed to reach steady state before the IR scan measurements were made.

In order to aid in heat sinking and mounting designs a table of thermal properties of common materials is presented. Three important thermal properties of common heat sink materials are given in Table A2. These properties should be considered in order to properly evaluate the choice of materials used in heat sinking/mounting of a PowerMacro for a given application.

Thermal Conductivity is a measure of the ability of a material of known cross sectional area to transfer heat a given distance in a given time with a given temperature difference. Generally metals are good thermal conductors.

Specific Heat is a measure of the amount of heat a given mass of material can accept for a given rise in temperature. The scale is normalized to the heat capacity of water (H_2O = 1.0).

Mass Density is simply the mass per unit volume of a material. This parameter is important in heat sink design in as much as large heat sinks of dense materials are undesirable.

The devices were decapsulated using a machine called a "Jet Etch." This machine is manufactured by:

B & G Enterprises
62B Hanger Way
Watsonville, California 95076-2486

The jet etch machine uses hot sulfuric acid to decapsulate the molded device. The device can be decapsulated so that there is no mechanical damage, no corrosive damage, and no loosening of external leads. Thus, the device is fully RF functional.

TABLE A2. Typical Thermal Properties of Materials

Material	Thermal Conductivity K (Cal/Sec-cm-°C)*	Specific Heat S (Cal/gm-°C)	Mass Density, P (gm/cm-°C)
Copper	0.94	0.093	8.9
Beryllia Ceramic	0.55	0.31	2.8
Aluminum	0.49	0.22	2.7
Brass	0.26	0.094	8.6
Silicon	0.20	0.18	2.4
Steel	0.12	0.12	7.8
Solder	0.09	0.04	8.7
Kovar	0.046	0.11	8.2
Alumina Ceramic	0.04	0.21	3.7
Plastic Epoxy	0.0026	0.2	2.0
Glass	0.0026	0.2	2.0
Mica	0.0018	0.2	3.2
Teflon	0.00056	0.25	2.2
Heatsink Compound	0.0018	—	—

*Conversion Factor: 1 watt/m = 2.39 x 10^{-3} Cal/Sec. cm. The thermochemical calorie = 4.184 joules. The absolute joule per second or watt is thus related in terms of calorie per second.

A Cost Effective VHF Amplifier For Land Mobile Radios

By Ken Dufour
Motorola Power Products Division

INTRODUCTION

This application note describes a two stage, 30 watt VHF amplifier featuring high-gain, broad bandwidth and outstanding ruggedness to load mismatch, achieved by use of the new MRF1946A power transistor. It uses a die geometry intended for RF power devices operating in the UHF region. The emitter periphery (EP) to base area (BA) ratio of this die is 4.9, up from the normal EP/BA range of 1.5 to 3.5 for VHF devices. Power sharing and current sharing in the chip are controlled with diffused emitter resistors. The end result is a VHF transistor with very high power gain (10 + dB), sufficient so that processing steps can be taken to provide tolerance to load mismatch while still maintaining excellent performance. By mounting this die in the 0.380 flange or stud package and providing characterization data that spans 136 to 220 MHz, Motorola has provided a very versatile component for the RF designer.

CIRCUIT DESCRIPTION

Smith chart techniques were used to develop the two stage amplifier shown pictorially in Figure 1 and schematically in Figure 2. The end result is an amplifier that can produce 20 dB overall gain in the specified band (150 to 175 MHz), with a midband efficiency of 50 percent. The Motorola MRF237 was selected for the driver stage. This

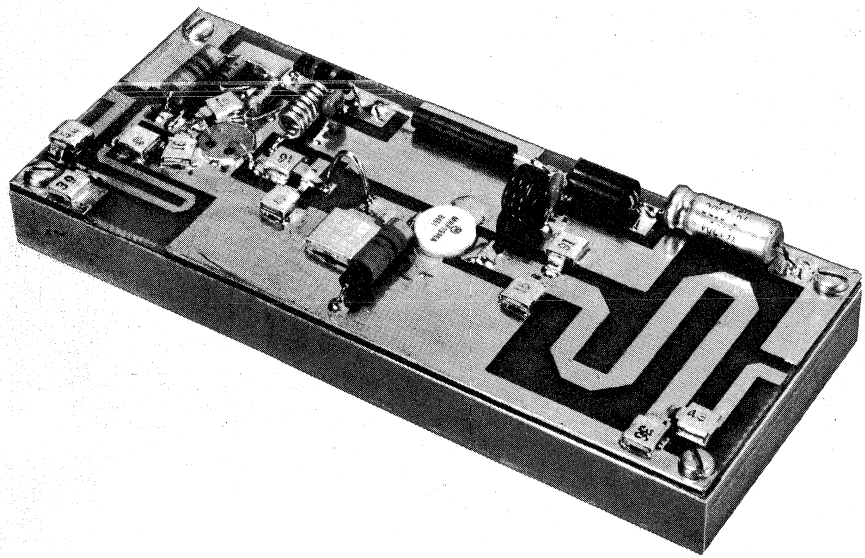
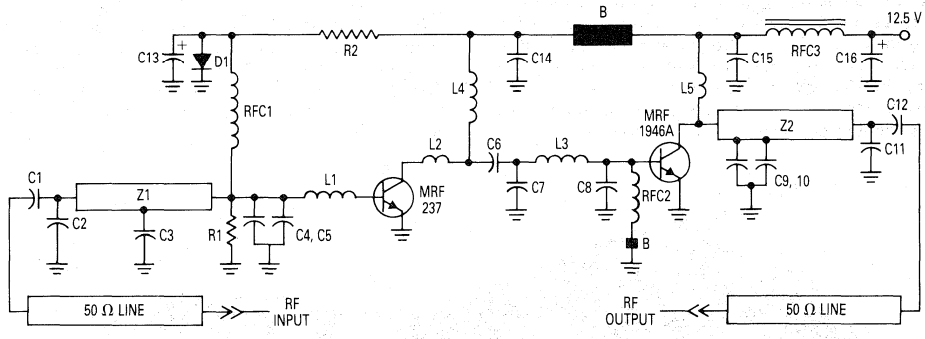


Figure 1. Engineering Model of MRF1946A Wideband Amplifier

common emitter (TO-39) RF power transistor produces high-gain, is easy to mount and is cost effective. In this design, the MRF237 is inserted into a hole in the circuit board and soldered to the ground plane for heat sinking, as shown in Figures 1 and 3. This method of attachment also provides a very effective emitter ground connection. By introducing a small amount of forward bias (5–15 mA) to the MRF237, it will track low drive levels and help maintain stability in the input stage. The amplifier is constructed on 1/16", double sided G-10 board with 2 ounce copper cladding. A photomaster of the printed circuit board is shown in Figure 4. The top and bottom ground planes of the board are connected by wrapping the board edges with thin copper foil (0.002") and then soldering it in place. Figures 1 and 3 illustrate how and where the board edges are wrapped in the prototype amplifier. No eyelets or plated-through-holes are required to achieve the level of performance noted here. Printed lines are used to match the devices' input and output impedance to 50 ohms, and an inductor and two capacitors form the interstage match. This allows some flexibility in shaping the overall frequency response and helps conserve board area. The MRF1946A stage is operated in Class C and is mounted to the heatsink using conventional methods, i.e.; an 8–32 stud inserted into an appropriately prepared heatsink. An alternate packaging arrangement, the 0.380 flange, allows one to attach the transistor to the topside of the heatsink with two screws. A Motorola Application Note on mounting techniques for various semiconductors is available and provides detailed information on installing either of these package styles (see reference 1). Additional information on thermal considerations can be found in reference 2. Performance of the amplifier is illustrated in Figures 5, 6 and 7. Figure 5 is a plot of P_{out} versus P_{in} at 160 MHz, 12.5 volts; Figure 6 shows output power, input VSWR and collector efficiency as functions of frequency; while Figure 7 demonstrates harmonic content for 30 watts output power.



C1 = 56 pF Dura Mica
C2 = 39 pF Mini-Unelco
C3, C7 = 68 pF Mini-Unelco
C4, C5, C6, C9, C10 = 91 pF Mini-Unelco
C8 = 250 pF Unelco J101
C11 = 36 pF Mini-Unelco
C12 = 43 pF Mini-Unelco
C13 = 1 μF, 25 V Tantalum
C14, C15 = 0.1 μF Mono-Block
C16 = 10 μF 25 V Electrolytic

D1 = Diode, 1N4933 or Equivalent
L1 = Base Lead Cut to 0.4", Formed Into Loop
L2 = Collector Lead Cut To 0.35", Formed Into Loop
L3 = 0.7" #18 AWG Into Loop
L4 = 7 Turns #18 AWG, 1/8" ID
L5 = 3 Turns #16 Enam, 3/16" ID
R1 = 10 Ω, 1/4 W Carbon

R2 = 1500 Ω, 1/2 W (Select For Most Appropriate ICQ)
RFC1 = 10 μH Molded Choke
RFC2 = 0.15 μH Molded Choke
RFC3 = VK200–4B Choke
Z1, Z2 = Printed Line
Z3 = 50 Ohm Printed Line
B = Ferroxcube Ferrite Bead 56-590-65-3B

Figure 2. Schematic Diagram of MRF1946A Wideband Amplifier

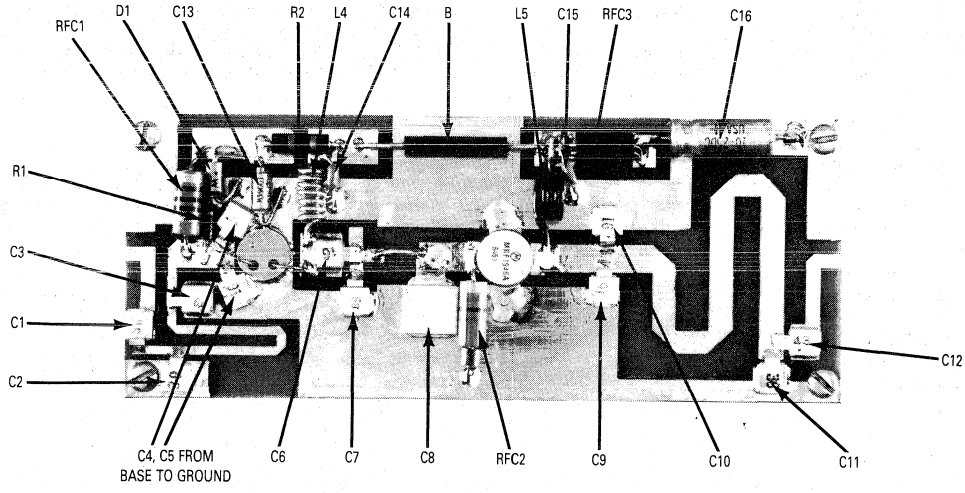
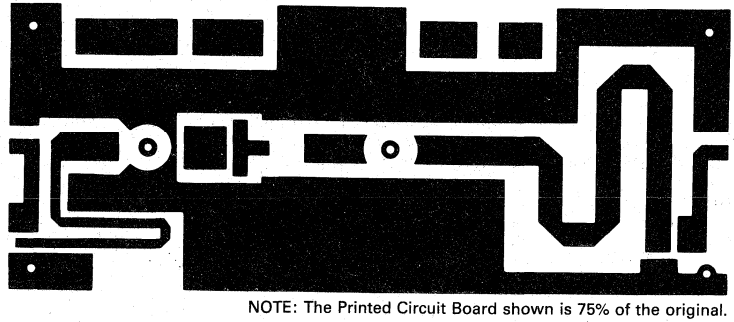


Figure 3. Parts Placement



NOTE: The Printed Circuit Board shown is 75% of the original.

Figure 4. PCB Photomaster

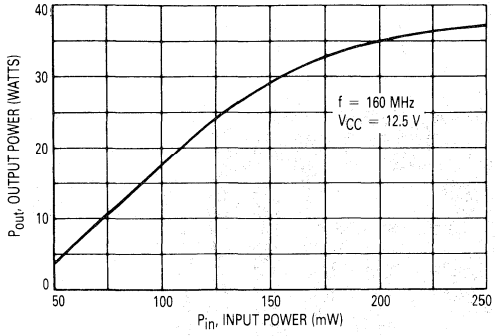


Figure 5. Output Power versus Input Power

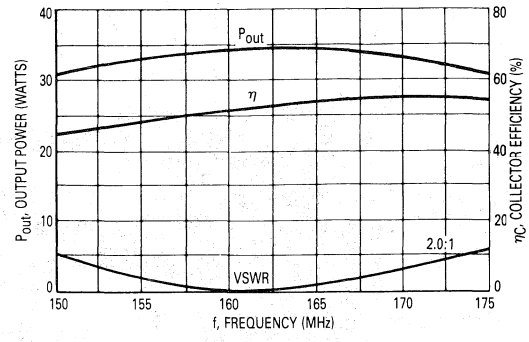


Figure 6. Output Power, Efficiency, and Input VSWR versus Frequency

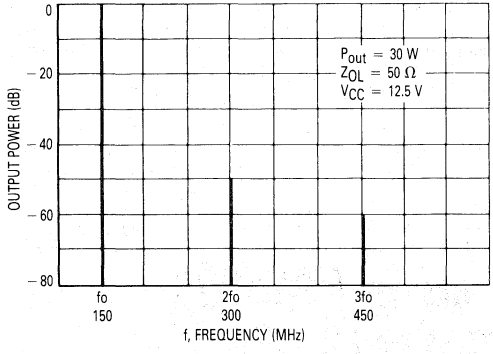


Figure 7. Output Spectrum

CONCLUSIONS

The two-stage amplifier described produces greater than 20 dB gain with 30 watts of output power over the frequency range of 150 to 175 MHz. Ruggedness and stability are achieved by use of the new MRF1946/A power transistor. The amplifier illustrates that relatively unsophisticated construction techniques properly implemented with the appropriate high gain devices can provide a cost effective 30 watt VHF amplifier for land mobile applications.

REFERENCES

1. Roehr, Bill: Mounting Techniques for Power Semiconductors, AN778. Motorola Semiconductor Products, Inc.
2. Johnsen, Robert J.: Thermal Rating of RF Power Transistors, AN790. Motorola Semiconductor Products, Inc.

Applying Power MOSFETs in Class D/E RF Power Amplifier Design

Reprinted by permission from RF DESIGN, June, 1985 issue. ©1985 Cardiff Publishing Co., a subsidiary of Argus Press Holdings, Inc.

By H.O. Granberg
Motorola Semiconductor Products, Inc.

Class D and E are variations of switching mode amplifiers which are designated in the literature at least up to Class S. Switching means that the amplifying devices are either conducting or "open" during each half cycle and the switching from one state to the other is done as fast as possible. In some systems the switching is done at other than the carrier frequencies for modulation or other purposes. Class D and E usually refer to carrier switched amplifiers and are best suited for high frequency applications where the rise and fall times of the switching waveform are of main importance. They are directly adaptable to CW or FM, but other types of modulation are also possible by pulse width or amplitude modulation (1, 2, 3, 4, 5). The theoretical aspects have been well covered by F.H. Raab and N. Sokal in numerous publications over the years, and practical low power designs have also been shown. The author feels that since the evolution of the RF power FET, high power switching amplifiers can be designed at least up to 30 MHz and possibly 50 MHz.

6

Currently, Class D or E transmitters are marketed at up to 10kW power levels for the broadcast band (.55 MHz-1.6 MHz) and at 1 kW for shortwave (up to 15 MHz). All use power FETs as the switches and advertise high efficiency and reliability. When the efficiency is higher, the reliability is better since the transistor (FET) die operates at a lower temperature. Efficiencies of at least 70 percent to 80 percent in Class D and 80 percent to 90 percent in Class E are possible with the present RF power FETs at moderate power levels. Efficiency in Class D is limited mainly by the saturation resistance of the devices and the output capacitance. The objective in Class E is to use the device output capacitance as part of a tuned circuit, thus eliminating its effect as a load capacitance. In an ideal form it also ensures that the switching voltage and current waveforms are not overlapping (6, 7).

An obvious advantage of high efficiency is the smaller amount of heat generated compared to power output. This results in a smaller heat sink and more compact design, leading to smaller output devices and reduced cost. An important application of high efficiency amplifiers is in battery powered transmitters, where battery lifetimes 25 percent to 30 percent longer than Class C should be possible. Another advantage is simplified circuit design, since interstage matching networks are not required, as they are with Class A, B and C, where the amplifying devices act as current sources rather than switches. From the low level limiter to the P.A. the power gain can be as high as 40 dB to 50 dB and the system bandwidth is limited only by the response of the output transformer or matching network. Assuming a constant pulse width from the limiter on, extremely wide-band amplifiers can be designed with no variation in power gain. Figure 1 shows an estimated power level vs. frequency curve of Class D/E feasibility with today's technology.

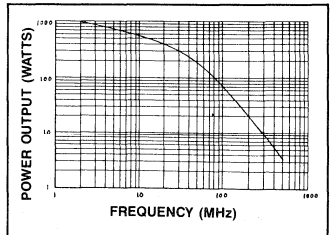


FIGURE 1. Estimated maximum power levels with a push-pull or single ended Class D/E amplifier based on present technology.

Preparing the Carrier Input Signal

Since the emphasis here is on relatively high power levels (up to 300W-400W per push-pull pair), the signal processing circuitry is only designed to operate up to 50 MHz. At higher frequencies it may be desirable to employ single ended designs in order to avoid any possible phase errors, which become exponentially more difficult to control with increasing frequency. The phase errors can be minimized in a push-pull circuit by providing the P.A. input drive through a transformer with bandwidth characteristics that will not affect the input rise and fall times considerably. Due to the difficulty in designing such transformers, which would require a bandwidth of one to several hundred MHz for a 2 MHz to 50 MHz carrier, it was decided to create the required 180 degree out-of-phase signals with ECL integrated circuits (Fig. 2).

The RF drive is first limited in a pair of cross coupled hot carrier diodes and then in three sections of ECL line receivers (MC 10H116). The limiter has approximately 50 dB dynamic range for amplitude modulated signals such as SSB. A peak detector circuit, shown at the upper left, was included, although the scope of this article is not to describe a modulated system.

The detector was designed to operate at audio frequencies, 300 Hz to 3 kHz, with an RF carrier down to 2 MHz. The detector output with two-tone RF input is shown in Figure 3.

The output audio envelope can be fed to an audio amplifier which can drive an emitter-follower or switchmode regulator that supplies the V_{DD} to the Class D P.A. The principle is to provide the amplitude information through this audio chain and the phase information through the RF chain. They are then combined in the output stage to provide a restored AM or SSB signal. This technique is called Envelope

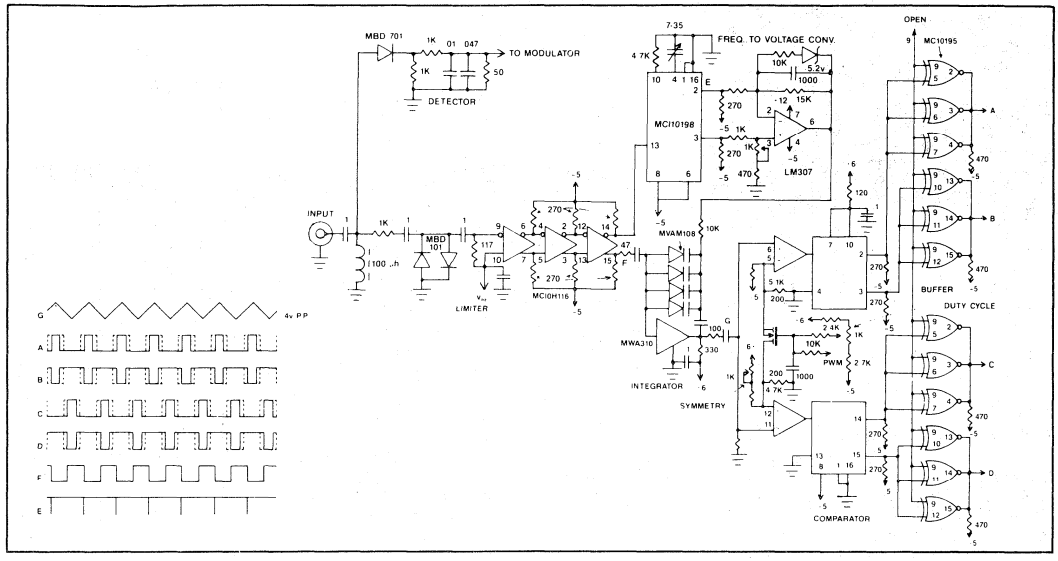


FIGURE 2. Schematic of the signal processor used in all the Class D experiments described. If the input is in sine wave, the amplitude can vary from .5 to 100 peak to peak. The output duty cycle is independent of the frequency.

Elimination and Restoration (EER) (2, 3, 4, 5). Pulsewidth modulation techniques can also be used to amplify AM and SSB signals with a Class D amplifier (1); however, the technique involves generating an inverse sine reference signal at the carrier frequency, and the distortion would be directly reflected to the output. The finite switching speeds also limit the dynamic range in this system. Both problems make the pulse width modulation technique practical only up to a few MHz. In contrast, distortion in an EER system is generated only by phase errors between the audio and RF chains (4, 5).

Although the circuit in Figure 2 is not intended for pulse width modulation, a provision was made to adjust the pulse width manually to allow the power output to be varied and to ensure that the P.A. drive signals would not be overlapping. The objective was to provide a constant duty cycle with frequencies anywhere between 2 MHz and 50 MHz. This was difficult to achieve, and the final result was that the frequency was split into two segments: 2-25 MHz and 25-50 MHz. Adjustments in the MC10198 (one shot) timing as well as the LM307 and the comparator biases were necessary to cover each band. The problem was mainly with the limited capacitance range of the MVAM108 tuning diodes in the integrator. Their capacitance should track the frequency in order to provide a constant amplitude triangular wave output from the integrator. It must be pointed out that the physical circuit layout of the integrator is critical for low distortion output. All lead lengths should be minimized and elsewhere proper ECL wiring techniques should be followed.

The circuit of Figure 2 was intended to be used with a number of Class D P.A.s studied. It is remotely located from the driver and the P.A. assembly, and the signals between the two are connected by twisted wire lines. The pull down resistors in the MC10195 outputs are provided only for testing purposes, while the terminations are located at the driver and P.A. assembly.

The Driver

Because of direct coupling between the stages, each side of the push-pull circuit requires its own driver and pre-driver. This has the advantage that the high peak current requirement from the driver is divided between two circuits, which will be discussed later in detail. For this reason also the push-pull configuration was chosen. A single ended design would require an output FET twice as large, having proportionally higher gate input capacitance.

The ECL level limited signal must be converted first to a voltage swing of at least 2 to 3 volts above ground to feed the driver, which may have a FET or bipolar input. The circuit shown in Figure 4E can be used for this, or 4F, if the ECL is operated between ground and +5 volts. Alternatively, integrated circuits, such as the MC10G125 ECL to TTL converter or MC10177 MOS clock driver, can be used for this function, as shown in Figure 5. These ICs can be operated with single phase inputs as well as two phase. The voltage swing must be increased to 8 to 10 volts above ground to ensure that the P.A. FETs will be fully "turned on."

Figure 4 gives examples of drivers that are fairly simple and can drive heavy capacitance loads. Figure 4A is the most complex, but it performs well providing the devices are correctly selected and the gate threshold voltages of Q3 and Q5 are equal. Without a load no current should flow through Q2 and Q3. The last statement applies to 4B also, if Q2 and Q3 are switched correctly. This basic circuit is used in the output stages of many TTL gates and buffers, and in integrated form the transistor base-emitter forward and saturation voltages can be controlled closely. In a discrete form the value of Q1 emitter resistor must be adjusted according to the parameters above. In addition, Q3, which is in common emitter configuration, must be of a fine geometry, high frequency design to minimize the base-emitter junction stored charge effect. Such devices in the NPN polarity are currently available in many package configurations.

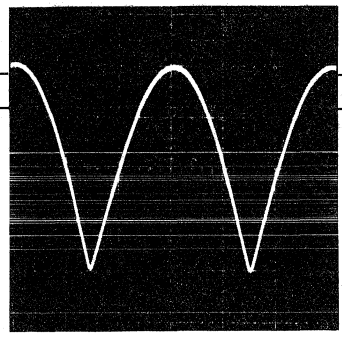


FIGURE 3. The peak detector output waveform (Fig. 2) with a two tone SSB drive signal. This can be used to control the P.A. supply voltage for amplitude modulation.

Circuits in 4C and 4D are the simplest and least critical, although both have some drawbacks. 4D uses a passive pull down, where the resistor value can be calculated for the desired turn off time when the voltage and FET input capacitances are known. A typical value for a 50W FET operating at 50 MHz would be around 3 to 4 ohms. The resistor current will be added to the input capacitance (C_{iss}) charge current, requiring a doubled current capability from the emitter follower (Q_2), although the average power dissipated is equal to that of circuits with active pull down. The complementary emitter follower in 4C is probably the most efficient driver, considering its simplicity. It is tolerant against variations in device parameters and has the lowest output impedance if the transistors are properly selected. The only disadvantage is the scarcity of high frequency PNP transistors with sufficient current capabilities. In all Figure 4 circuits the pre-driver (Q_1) can be a bipolar transistor or a FET depending on the exact requirements and the input signal amplitude.

Power MOSFET HF Switching Characteristics

At low frequencies the MOSFET gate should present a purely capacitive load to the driver. In switching applications, however, the rise and fall times represent a much higher frequency component than the fundamental. For example, if at 30 MHz carrier 4 nanosecond switching times can be tolerated, at 80 percent amplitude the 4 ns represents roughly a 100 MHz sine wave. Examining the MRF150 Smith Chart (data sheet) and converting the information into parallel form we find that the input capacitance remains a constant 800 pF up to 150 MHz. This is an average value under biased and linear operating conditions, but it indicates that the wire bond and package inductances have a minimal effect at that frequency. For switching applications, where the FET goes into saturation, the input capacitance is more difficult to define.

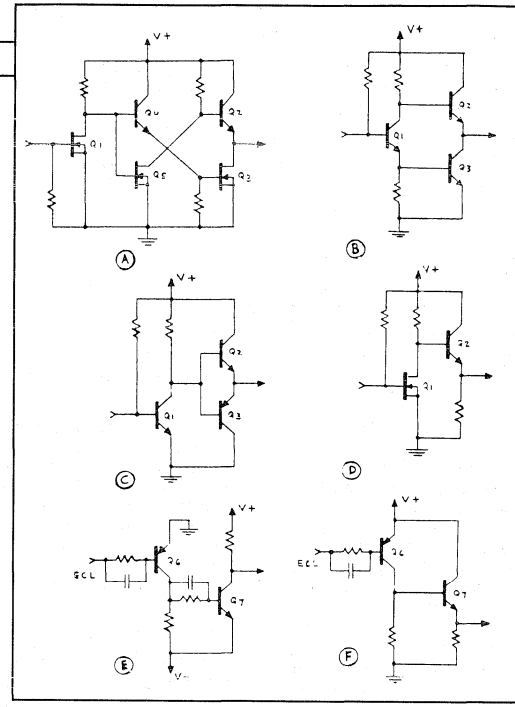


FIGURE 4. Various Class D driver configurations. E and F are intended for ECL to positive level conversion, while A, B, C and D are designed to operate from higher voltage inputs to drive capacitive loads, such as the FET fates.

As shown in Figure 5, the C_{iss} varies with gate and drain voltages. At left (zero gate voltage) we can see the value under the conditions where the parameter is normally specified. At increased gate voltage the capacitance goes down to its lowest value, just before reaching the threshold voltage. When the FET begins to draw drain current, there is a point where the device gain is at its highest value. At that time the drain voltage is also lowered, resulting in reduction of the depletion area and causing an overlap between the gate and the bulk material. This in turn increases the value of drain to gate capacitance (C_{rss}), which will be multiplied further by the gain and reflected back to the gate. As a result, a sharp peak in the C_{iss} will occur. When the FET is fully saturated, the C_{iss} settles to its value under zero drain voltage and positive gate conditions. A similar effect is present with all power MOSFETs to some extent depending on their exact parameters. The data was taken at 1 MHz but is not expected to change considerably at higher frequencies.

Figure 6 shows two input drive waveforms superimposed at 25 MHz repetition rate: the driver waveform without a load (A) and when loaded by the FET gate (B).

The notches in B are the result of the C_{iss} peak in both turn on and turn off. In low frequency switching applications this may not be directly noticeable due to the much slower transition times involved. For HF, the peak value of the C_{iss} must definitely be taken into consideration when designing the driver. Assuming the driver pulse amplitude is 8 volts, the driver has a relatively easy task in turning the FET on. The C_{iss} is low up to the threshold point, approximately 3.5 volts, increasing to 4.5 volts. After this, the voltage only has to increase another 3.5 volts, loaded by the high capacitance. Since this period falls within the "on" cycle of the FET, a slower rise time is of lesser importance. In turning the FET off the driver must supply the highest current at the beginning of the cycle. Its dissipation is also at the peak at this point and high until the first 3.5 volts of discharge is completed, the load capacitance lowered and the voltage across the driver gradually reduced. This is the most critical part of the cycle since it can result in a

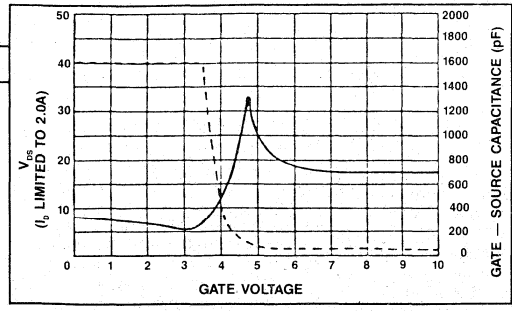


FIGURE 5. Typical TMOS (MRF-150) gate-source capacitance versus gate and drain voltages. All power MOSFETs behave more or less similarly, depending on their die structures, geometries and electrical parameters.

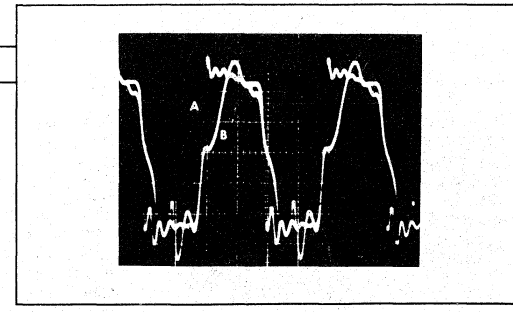


FIGURE 6. Driver output waveform at 25 MHz. A without a load. B loaded by the P.A. FET gate. Results of the uneven gate capacitance distribution versus gate and drain voltage can be noticed in B. 10 nS and 2v/div.

delay in the turn off of the FET, causing both sides of a push-pull circuit to draw current simultaneously for a part of the cycle. The delay can be prevented or minimized by adjusting the driver voltage amplitude only to a level necessary to switch the output FETs to a full saturation and completely off. Any excess voltage swing increases the delay and also the dissipation in the driver.

Considering the complex nature of the FET C_{iss}, a most realistic figure for the required driver output impedance can be obtained if it is calculated for the peak capacitance value and the gate voltage swing between saturation and threshold:

$$\frac{-t}{C \times L_n(1 - \frac{V_2}{V_1})}$$

where:

–t = required switching time (4ns).
C = FET input capacitance at the peak (1300 pF).
V_1 = gate voltage at saturation (8V).
V_2 = gate voltage between saturation and threshold (4.5V).

then:

$$\frac{-4 \times 10^{-9}}{1.3 \times 10^{-9}(-.82)} = \frac{-4}{1.3 \times (-.82)}$$

= 3.74 ohms

This translates to 1.2 amperes up to where the driver transistors (NPN and PNP) must have a linear h_{FE}. As stated earlier, the 4 ns transition times represent about a 100 MHz sine wave, which means that an HF beta of 10 would require an f_t of 1000 MHz for the driver transistors according to the 6 dB/octave slope (8). The DC beta (h_{FE}) is not critical but must be greater than 10.

For the complementary emitter follower, the PNP half may be difficult to find with the above specifications. In fact, some special units were built for experimental purposes using a multiple die similar to the 2N5583. The NPN counterpart was an MRF630. This combination worked well except that heat sinking of the TO-39 packages was difficult because of the close proximity of the pair, which is necessary to minimize all inductances.

Output Impedance Matching

In low voltage Class A, B and C designs the output impedance matching becomes difficult due to the low impedance levels involved at 100 W and higher output levels, if broadband operation is required at HF. The matching is usually done with broadband transformers, of which the transmission line types offer the best broadband performance. For many applications, however, they are considered impractical and bulky in higher than 9:1 or 16:1 impedance ratios (9). There are other transformer types that are more convenient in physical aspects but lack the bandwidth characteristics. This poses a real problem, especially for Class D where bandwidths from 1 MHz to 100 MHz or higher may be required. A transformer type which is fairly good for impedance ratios to 25:1 and higher is one where the low impedance winding is formed by metal tubes inside ferrite sleeves and the high impedance widing is threaded through the tubes (7, 9). Such a transformer was used in the design of Figure 7, where the power output specification was 100 W, requiring the closest integer of 16:1 impedance ratio.

Two points in its behavior must be noted.

1. The high leakage inductance of this type transformer requires an unusually large capacitance for compensation limiting the bandwidths. These capacitances, of which the device output capacitance will be a part, are normally located across the primary or secondary windings, or both (Figure 7, C_1 and C_2). The required compensation can be calculated from the measured leakage inductance, and the maximum frequency will be limited by the device output and stray capacitances. At the resonant frequency the transformer VSWR will be 1.2:1, increasing to approximately 6:1 an octave higher (10). The leakage inductance can be measured across the secondary with the primary shorted. The connection inductances must be added to this and the maximum tolerable value is:

$$L_1 = \frac{R_L}{2\pi f}$$

where:

L_1 = Leakage inductance (μH)
R_L =Load impedance (50 ohms)
f = Maximum frequency (Mhz)

In Class D, the limited bandwidth will slow down the output rise and fall times. Since the transformer acts as a low Q resonant circuit, this can be used to place the amplifier in Class E mode of operation by moving the resonance down to the carrier frequency, although the Q cannot be properly controlled and the system may not be optimized.

2. The coupling between the two halves of the low impedance primary winding is only provided through the secondary and is very poor at higher frequencies due to the leakage inductances. If the amplifier is designed for voltage switching configuration, the transformer center tap is bypassed to ground. Due to the decreasing coupling the effect of the center tap is lost and at higher frequencies the amplifier will turn into current switching mode. With these two configurations the drain voltage and current waveforms are reversed (7), resulting in unpredictable waveshapes at the between frequencies. This will not affect the amplifier's efficiency, which theoretically should be equal for voltage and current switching modes, but makes its operation more difficult to analyze. If the transformer is properly designed, e.g., the tube diameter to

length ratio is high for increased couplings and the inductances between the transformer and FET drains are low, satisfactory operation up to 50 MHz is possible, depending on the impedance ratio in question.

Efficiency Considerations

The efficiency of an amplifier is defined as the ratio of DC input power to RF output power and is usually expressed in percentage. There are three main device parameters that affect the efficiency of a Class D amplifier:

1. Saturation voltage, in some data sheets given as saturation resistance, is directly proportional to the current and more linear with FETs than with bipolar transistors due to the latter's nonlinear diode characteristics. In contrast to the bipolar the FET has a highly positive temperature coefficient slope (saturation voltage increases with temperature), approximately 1 percent/°C. The DC value starts higher with FETs than with comparable devices. At RF the saturation voltage is further increased by the package and wire bond inductances and is more noticeable with low voltage devices due to the low impedances and high current levels involved. The RF saturation voltage can be more accurately measured than calculated. Typical values for MRF140 and MRF150, for example, are 1.7 volts and 3.0 volts, respectively, at 10 amperes and 30 MHz. From these numbers the efficiency can be calculated simply as:

$$\frac{V_{DD}-V_{sat}}{V_{DD}}$$

2. The switching speed of a transistor or a FET is mainly related to its high frequency characteristics, as discussed earlier in the driver paragraph. The internal capacitances have a large effect, but they in turn are a function of f_t, except for small differences between various FET structures such as interdigitated and overlay or TMOS and VMOS. For comparable geometries the FET has about three times higher f_t than the BPT. This means that some of the low frequency switching FETs can be used as RF switches up to 20 MHz to 30 MHz if a low output impedance driver is provided. In case of a sine-wave driving signal (7) the switching speed relies totally on the device high frequency gain and the input signal amplitude, whereas with a square-wave drive, it is affected by the input rise and fall times as well. Assuming a linear ramp with no distortion, the effect of transition times on efficiency can be calculated as:

$$\frac{360 \times \sin\Theta s}{2\pi \times \Theta s}$$

where: Θs is the phase angle portion of a full cycle that the transition time covers.

3. The device output capacitance, or any external capacitance shunting the output, reduces the efficiency of an amplifier. This capacitance must be charged to nearly twice the supply voltage during each cycle, and the power used is dissipated in the amplifying device. In narrowband designs and Class E switching it can be tuned out but not completely since its value varies with the output voltage swing. With power transistors and power FETs, the C_{ob} or C_{oss} is usually dominant and stray capacitances can be disregarded for practical purposes. Their values in data sheets are specified at DC and at the recommended supply voltage for RF, or mostly at 25 volts for LF switching. For example, the C_{oss} for the MRF150 is given as 250 pF at 50 volts but is higher at lower voltage and increases sharply at voltages below 5; thus, for accurate calculations a higher C_{oss} value should be used for an average, but it can only be obtained from a C_{oss} vs voltage curve. According to the formula in Reference 7, (p.446) the power loss for a push-pull amplifier is:

$P_s = C_s(2\ V_{eff})^2(2f) = 8\ C_s\ V_{eff}^2 f$ where:
P_s = Power loss
C_s = Device output capacitance
$V_{eff} = V_{DD} - V_{sat}$
f = Frequency

From this we can see that power loss depends mostly on supply voltage and on capacitance and frequency to a lesser degree. The output rise and fall times for these calculations are irrelevant since they only affect the peak power dissipated in charging the load capacitance, the average power remaining constant.

For a pair of MRF150s operating at 50 volts and a power output of 300 watts the power loss would be 8 (250 x 10^{-12}) $(47)^2$ (30 x 10^6), considering the worst case at 30 MHz. (2 x 10^{-3}) (2200) (30) = 132 watts and the efficiency is:

$$\frac{300}{132 + 300}$$

= 69 percent.

If the same die (MRF140), with its 450 pF output capacitance, were used in a similar 28 volt system, the efficiency would be (3.6 x 10^{-3}) (692) (30) = 75 percent. This is in contrast to the belief that a higher supply voltage automatically results in higher efficiency except when the circuit losses become high at very low output impedances. Considering this, it would seem that Class D efficiency is not much better than Class B or Class C, at least at higher supply voltages. If we calculate the total efficiency, taking all the above factors into account, it is only about 60 percent, However, efficiencies up to 80 percent have been demonstrated in practice in similar systems, using the MRF150s or comparable devices.

It is obvious that load capacitance is the one factor that limits amplifier efficiency most seriously, unless it can be compensated for. Assuming a perfect output transformer in a Class D push-pull amplifier,

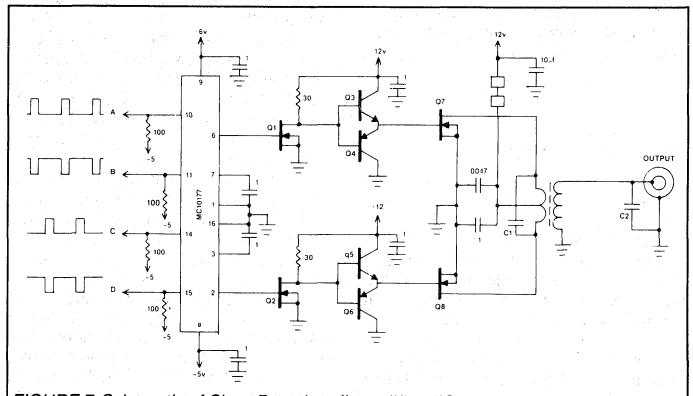


FIGURE 7. Schematic of Class D push-pull amplifier. ECL integrated circuits are used to provide the 180 out of phase input signal (see Fig. 12). This makes the pulse width easy to control compared to transformer coupling.

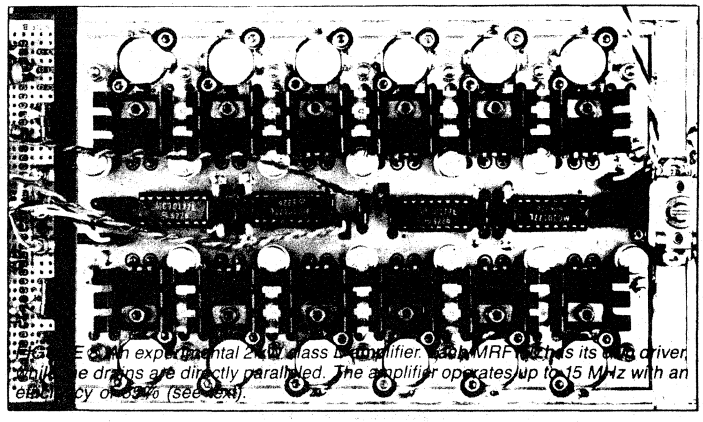


Figure 8. 2 kW experimental 2 kW Class E amplifier. Each MRF150 has its own driver, while the drains are directly paralleled. The amplifier operates up to 15 MHz with an efficiency of 83% (see text).

the compensation could be done by inserting a required amount of series inductance between the drains and the transformer primary. This would form a resonant circuit with the device C_{oss}, limiting the bandwidth to some extent, and the advantage of the perfect transformer would be lost. This inductance can be used and sometimes is used unintentionally to tune out the device output capacitance, but since the effective C_{oss} varies within the RF cycle, total compensation can hardly be achieved. Thus, in practical amplifier circuits of this type, there is a tradeoff between efficiency and bandwidth, which also applies to Classes B and C.

Conclusion

Commercial Class D and E transmitters up to 1 kW and 10 to 15 MHz are on the market. The author demonstrated a 1 kW, 10 MHz amplifier in 1981 (11), which was later evaluated by the National Bureau of Standards. Other designs since then include an 800 W amplifier at 13.54 MHz with four MRF150 FETs, a 100W unit for 25 to 50 MHz operating at 12 volts and a 2 kW, 50 volt system (Fig. 8) which did not function as expected at frequencies above 15 MHz. The main problem was increasing inductance in the power FET drain connections to the output transformer. The component physical size undoubtedly places a limit for high power designs of this type, unless multidimensional constructions can be made feasible.

The importance of the physical layout must be emphasized, since it is the key to a properly operating system no matter how good the electrical design is. We must remember that we are dealing with frequency components of 100 MHz and higher in a 30 to 50 MHz carrier system, where even a nanosecond difference in delays between each side of a push-pull circuit drive signal will noticeably affect efficiency.

Since high power Class D and E designs up to 15 MHz with efficiencies far exceeding those at Class B have been shown, the author feels that the frequency range can be extended to at least 30 MHz with proper physical design, leading to high efficiency linear and other applications.

About the Author

Helge Granberg is Principal Staff Engineer at Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, AZ 85036.

References

1. F.H. Raab, "Radio Frequency Pulsewidth Modulation," IEEE Trans. Commun., Aug. 1973.
2. L.R. Kahn, "Single-Sideband Transmission by Envelope Elimination and Restoration," IRE Proceedings, July 1953.
3. L.R. Kahn, "Comparison of Linear Single-Sideband Transmitters with Envelope Elimination and Restoration Single-Sideband Transmitters," IRE Proceedings, Dec. 1956.
4. A.D. Sokal and N.O. Sokal, "High-Efficiency Linear Power Amplification of Modulated Carrier Signals by Envelope Elimination and Restoration," Report: April 6, 1981 Design Automation, Inc., 869 Massachusetts Ave., Lexington, Mass. 02173.
5. F.H. Raab, "Intermodulation Products in EER Systems," Report: April 1, 1982, Green Mountain Radio Research Co., 50 Vermont Ave. Ft. Ethan Allen, Winooski, VT 05404.
6. N.O. Sokal and A.D. Sokal, "Class E Switching — Mode RF Power Amplifiers," *RF Design* magazine, summer 1980.
7. Krauss, Bostian, Raab, "Solid State Radio Engineering," Wiley & Sons, Inc. 1980.
8. A.B. Phillips, "Transistor Engineering," McGraw-Hill, 1962.
9. H. Granberg, "Broadband Transformers and Power Combining Techniques for RF," Motorola Semiconductor Sector Application Note AN-749, and all references cited in this publication.
10. G.S. Pondian, "Broadband RF Transformers and Components Constructed with Twisted Multiwire Transmission-Lines," Thesis, Indian Institute of Technology, Delhi, Dec. 1983.
11. H. Granberg, "Power MOSFETs versus Bipolar Transistors," *RF Design* magazine, Nov./Dec. 1981.

RF power MOSFETs

While switching type MOSFETs gather all the acclaim, RF types are quietly starting to find their niche

Helge Granberg
Principal Staff Engineer
Motorola Semiconductor Products
Phoenix AZ

Since their introduction in the mid-70s, power MOSFETs have found major use in switching power supplies and in motor control circuits. More recently, however, they are being considered more and more for use as RF power amplifiers because they offer certain advantages over bipolar transistors. These advantages include higher input impedance (in all circuit configurations), gain control by varying the DC gate voltage bias, and immunity to thermal runaway. They do have some disadvantages, though — probably the biggest is their higher cost. Other disadvantages of MOSFETs include a higher saturation voltage than bipolars and their susceptibility to gate punch-through.

RF and switching MOSFETs differ

Power MOSFETs made for RF applications differ in a number of ways from those made for switching applications. For example, RF power MOSFETs usually have much finer die geometries than switching MOSFETs. Also, their die metallization pattern is divided into a number of segments, with each segment having separate gate and source bonding wires. This reduces wire bonding inductances and lowers the MOS capacitances within the die, greatly increasing their operating frequency capabilities.

RF power MOSFETs are generally n-channel, enhancement-mode devices, which means that the drain is positive with respect to the source and the gate must be biased to a positive voltage with respect to the source for drain-source current to flow. Some other RF devices, such as GaAs FETs, are depletion-mode devices and must be turned off by a negative bias like electron tubes.

While most designers are very familiar with bipolar transistor parameters, this isn't so for power MOSFET types. The table, *"Comparison of bipolar and power MOSFET DC parameters,"* explains the various MOSFET parameters and their importance to the designer, and relates them to bipolar parameters.

One important DC parameter not listed in the table is thermal stability. A MOSFET is almost always biased to some level of idle current, while the bipolar must be biased for linear operation. The forward voltage variations in a base-emitter junction are 1 to 2 mV/°C, and always have a negative temperature coefficient. Gate threshold voltage must be measured against a constant drain current and also has a negative coefficient at low current levels. However, the material bulk resistance of an FET has a positive coefficient, which becomes dominant at higher current levels. Thus, an FET's g_{FS} goes down as temperature goes up.

Stabilizing RF transistors

Looking at bipolar collector and MOSFET drain currents versus temperature at constant base and gate voltages (Fig. 2), it can be seen that the bipolar transistor has a negative coefficient up to high current levels but the FET "turns around" before the device dissipation rating is exceeded. Since these parameters are h_{FE}, g_{FS}, and current dependent, it is not easy to provide temperature stabilization for biased devices. For the bipolars, a forward-biased diode with suitable

© 1983 Hearst Business Communications, Inc.,
UTP Division, Garden City, NY 11530
All rights reserved. Reproduced by permission.

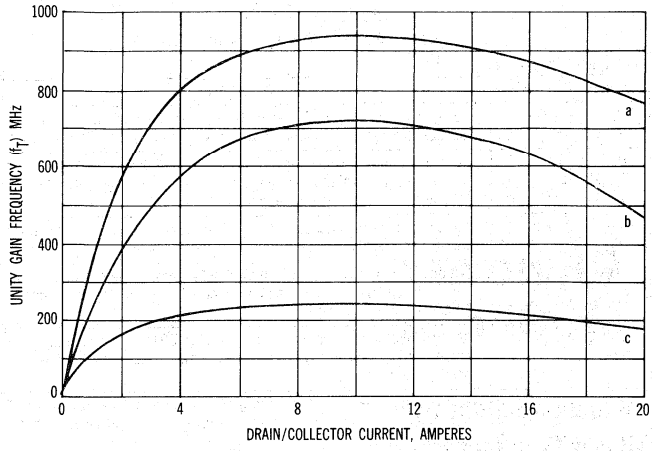


Fig. 1. Unity gain frequency versus I_C or I_D. Curve (a) represents a 150-W RF power MOSFET. Curve (c) is a bipolar having the same basic die geometry. Curve (b) is a standard switching power MOSFET with approximately equal gate periphery for comparison purposes.

characteristics kept at or near the transistor case temperature is usually considered a sufficient bias voltage source. In MOSFETs the required voltage can vary by several volts and the rate of change can be several times that of a bipolar at low drain currents. Thus, the FETs require more sophisticated methods for their temperature compensation. Resistor-thermistor combinations, together with regulators or op amps, are typical of these methods.

Despite the power MOSFET's parameter and cost-related drawbacks, its advantages still make it the choice over bipolars in certain applications. At VHF and UHF, the high gate-input impedance and the high power gain of the MOSFET make it possible to design broadband amplifiers with simpler input matching networks. Since the gate-source impedance remains capacitive to much higher frequencies, it makes internal matching networks unnecessary at least up to VHF even for devices of 100 to 150 W power ratings. On the other hand, VHF bipolar transistors with power ratings of 50 W and higher commonly employ internal matching networks, which means that the first section of the total network is built inside the device to transform the die impedance up to practical levels.

In general, at frequencies below VHF, the input and output matching for power FETs and bipolars are very similar. Only the network element values differ in most cases. At high frequency (2 to 90 MHz), where the configuration is mostly push-pull, ferrite broadband transformers or lumped-constant balanced LC transformers can be used depending on the exact requirements.

Amplifier circuit configurations such as common base (bipolar) and common drain (MOSFET) are also possible and practical. The common base circuit may be useful where more constant input impedance-versus-frequency or wider gain control range with gate voltage is required.

The MOSFETs common drain circuit configuration represents an emitter follower in bipolar circuits. Its specific merits are exceptional stability and linearity. However, these are attained at the cost of low power gain and at the danger of exceeding the V_g.

A MOSFET source follower cannot be considered as having current gain like an emitter follower. Rather, the amplification is achieved through impedance transformation. Note that the FET gate, which consists mostly of MOS capacitance, normally presents a high Q input to any matching network. This will impair the broadband performance and stability of the amplifier unless the Q is lowered by artificial means. A

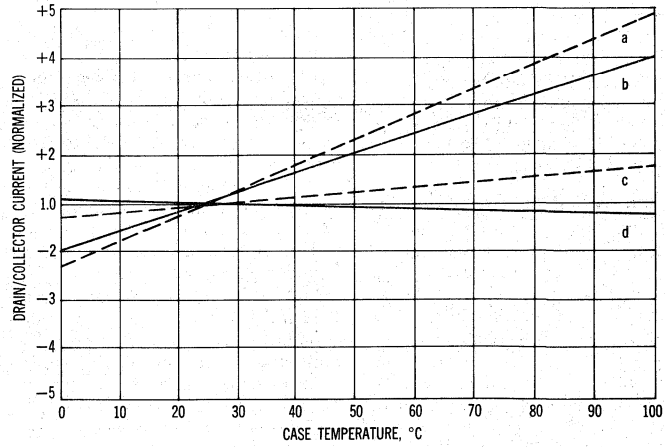


Fig. 2. Collector and drain idle current versus temperature at constant base or gate voltages. (a) and (c) represent a bipolar device at collector currents of 100 mA and 10 A respectively. (b) and (d) is a power MOSFET at drain currents of 100 mA and 10 A respectively.

gate shunt resistor, which can be part of the biasing circuit, serves this purpose.

A more sophisticated method of achieving broadband performance and stability is to employ negative feedback, which can be easily implemented only in the common source configuration. The feedback can be brought to the gate through an RLC network which, in combination with the shunt resistor, allows easier tailoring of the gain slope. In each case some power gain will be sacrificed, but this can be minimized at the high frequency end of the band (where the power gain is the lowest to begin with) by proper choice of component values in the feedback network.

The FET gate should never be connected to only inductive reactances in an attempt to use the inductance to control the gate Q. The C_{ISS} is highly drain-source voltage dependent and under certain conditions the total Q may be high enough to allow transients to exceed the V_g, thereby causing instant device failure.

Compare linearity and noise

It's commonly believed that power MOSFETs have more linear transfer characteristics than bipolars. This is only true if the FET is operated at a reduced power level and high bias (near or in class A). Based on two-tone linearity tests, the low order distortion products (3rd, 5th and 7th) fall faster with MOSFETs than with bipolars at reduced amplifier power outputs. However, FCC specifications are relaxed on low order distortion — −31 dB below the transmitter peak power — a figure easy to achieve with both types of transistors. It's when it comes to high-order distortion — 9th order and up — that MOSFETs are superior to bipolars (see Fig. 3).

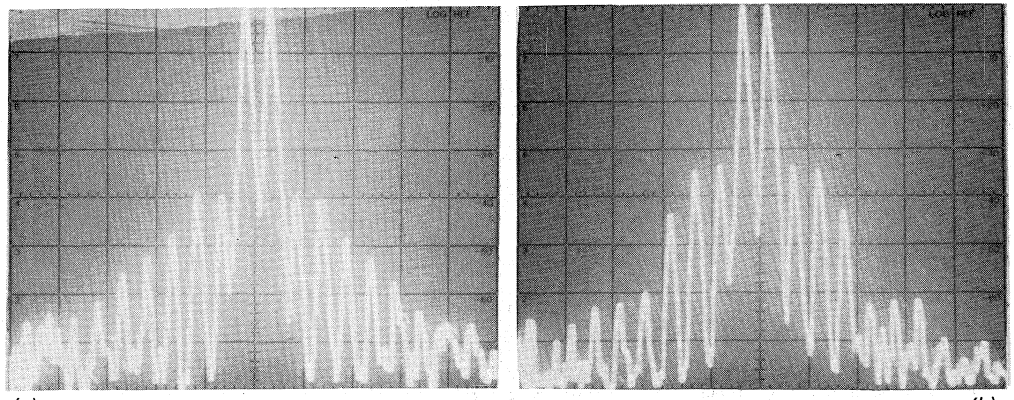
High-order distortion causes disturbances to adjacent communication channels, whereas low-order distortion only relates to the quality of the modulation. High-order distortion results from phase nonlinearities between the input and output, from amplitude nonlinearities at low drive levels, and from

Comparison of bipolar and power MOSFET DC parameters

"Equivalent" Parameters

Bipolar	MOSFET	Description
BV_{CEO}	BV_{DSO}	Not specified or measurable with MOSFETs. In case of low gate-source leakage, the gate can charge to voltages exceeding the punch-through.
BV_{CES}	BV_{DSS}	Normal method of measuring the MOSFET breakdown voltage. It refers to the maximum drain to source voltage the FET is allowed with the gate DC biased or in the same potential as the source.
BV_{CBO}	BV_{DGO}	Not specified or measurable with MOSFETs. Gate-source rupture voltage would be exceeded in case of any drain-source leakage present.
BV_{EBO}	Vg	Not specified or measurable with MOSFETs unless done carefully at low current levels. Gate rupture can be compared to exceeding a capacitor's maximum voltage rating.
V_B (forward)	Vg(th)	Not specfied or necessary in most cases for BPTs. For a MOSFET, this parameter determines the turn-on gate voltage and must be known for biasing the device.
I_{CES}	I_{DSS}	Drain-source leakage current with gate shorted to source. BPT and FET parameters equal and normally only refer to wasted DC power and reliability.
I_{EBO}	I_{gs}	Normally not given in BPT data sheets, but important for MOSFETs for biasing purposes. Both affect their associated device's long term reliability.
$V_{CE(SAT)}$	$V_{DS(SAT)}$ or $R_{DS(ON)}$	Not usually given in BPT data sheets but important in certain applications. With power MOSFETs this parameter is of main importance. The numbers are assumably higher than with BPTs, and are material and die geometry dependent.
h_{FE}	g_{FS}	These are parameters for low frequency current and voltage gain, respectively. In a MOSFET the g_{FS} is more an indication of device electrical size and to a certain extent depends on processing.
f_T	(f_T)	Unity current or voltage gain frequency. Not given in many of the BPT or MOSFET data sheets. The figure can be two to five times higher for the MOSFET for an equivalent basic geometry and electrical size (see Fig. 1). The figure of merit of a MOSFET is usually considered as the ratio of the gate-source capacitance to the G_{FS}, but other parameters such as the R_{DS} (on) have some effect on the figure of merit.
G_{PE}	G_{PS}	Power gain in common emitter or common source configuration. This parameter is equal for both types of devices, except normally regarded as current gain for the BPT and voltage gain for the FET. At lower frequencies, where the FET gain is extremely high, the number may be merely an indication of how much stable and useable gain is available.
C_{IB}	C_{ISS}	Base to emitter or gate to source capacitance. Rarely given for BPTs. In RF power FETs the C_{ISS} has a larger effect on the gate-source impedance. In fact, if stray inductances from the die metal pattern, wire bonds, and package were absent, the gate impedance would be a pure capacitive reactance. The C_{ISS} consists mostly of die MOS capacitance, whereas the C_{IB} of BPT is a combination of MOS and diode junction capacitance. Since the diode(s) are forward biased during one half cycle and reverse biased during the other, it is obvious that the base impedance is largely drive level dependent.
C_{OB}	C_{OSS}	Collector to emitter or drain to source capacitance. Both are usually specified and are approximately equal in value for a given device rating and voltage Both are combinations of MOS and diode capacitances. Each effect the device efficiency since this capacitance must be charged and discharged at the rate of the operating frequency.
C_{RB}	C_{RSS}	Collector to base or drain to gate capacitance. Rarely specified for BPTs. Normally referred to as the feedback capacitance and very important for MOSFETs considering their lower gate-source capacitance and superior high frequency performance. At low frequencies C_{RSS} provides a 180° out of phase feedback to the gate, but can turn to positive feedback at high frequencies depending on stray inductances and the C_{ISS}. The results will be noticed as parasitic oscillations, unless C_{RSS} is low or the resonances fall outside the device's frequency capabilities.

6



(a) (b)

Fig. 3. Typical intermodulation distortion for a bipolar RF transistor (a) and for an RF power MOSFET (b). For the bipolar transistor, distortion products are visible up to the 15th order; for the MOSFET, 9th order and higher products are down in the noise.

nonlinear feedback. Most of the nonlinear phase and amplitude feedback in the bipolars is delivered through the emitters, which are coupled to the collectors through diodes and MOS capacitance. The emitter ballast resistors, although very low in value, allow enough feedback to the emitters to cause distortion. These ballast resistors in FETs are unnecessary, and the source is directly grounded. Thus, high-order distortion in a MOSFET is only possible through the C_{RSS}, which is very, very low.

Much like the high-order distortion in SSB communications, the broadband noise generated in any transmitter causes adjacent channel interference. The noise can be generated by the signal source, mixers, or any stage in the amplifier chain. The noise generated in the low level stages is amplified in all succeeding stages, and is of most concern. In linear amplifiers, where all stages are biased, the bias current alone can generate sufficient noise to block a nearby receiver. Both MOSFETs and bipolars generate thermal noise, which comes from the moving electrons. In addition, the forward-biased diode(s) in bipolars generate white noise, which is not present in MOSFETs. The two types of noise is usually measured together, and since a bipolar typically has about three times higher noise figure than a comparable FET, it appears that a majority of the noise generated comes from the base-emitter junction.

When higher current levels or higher amplifier power outputs are required than one semiconductor device can provide, paralleling devices is often the first thing that comes to mind. Bipolars are often paralleled at DC and low frequencies, where their balance can be assured with external ballast resistors. At RF, however, this technique can not be used due to excessive losses in power gain. Instead the devices must be closely matched. At VHF and UHF, where the base impedance is very low and mostly inductive in reactance, added inductance in the form of the interconnections would make the design of matching networks difficult. So, in practical designs, the low impedance of each device is transformed to a higher level, before the point where the parallel connection is made.

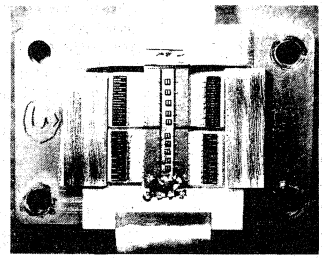


Fig. 4. In this experimental RF MOSFET four die are connected in parallel. Chip-type silicon gate resistors are located at the center.

The above problem is present with MOSFETs also, but they are more tolerant of gain mismatches because of the large amount of drain ballasting inherent in their structure. The MOSFET's higher, and capacitive, input impedance allows direct paralleling of higher power devices up to 150 to 200 MHz. However, a new problem arises when the MOSFETs are paralleled. When MOSFETs are paralleled directly, a multivibrator type oscillator is formed, in which the feedback is derived through the C_{RSS} and the time constant is the cross-coupled C_{ISS} plus wire bond and interconnect inductances in series. This may also occur when individual die are paralleled in the same package unless the C_{ISS} is low and the resonances fall outside the device limits. A commonly used cure for these parasitic oscillations is to de-Q all gates with series resistors (see Fig. 4) but this lowers the frequency response, making this technique impractical for truly high frequency applications. □

6

HOW TO APPLY THE MHW709/MHW710 UHF POWER MODULES

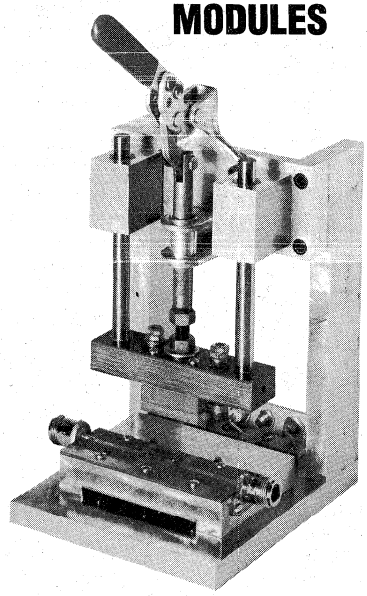


FIGURE 1 — UHF POWER MODULE TEST INFORMATION (MHW709 AND MHW710)

TEST CIRCUIT

Motorola's UHF Power Modules use thin film construction to minimize parasitics, and for manufacturing consistency. They're flange mount for easy, one-sided assembly. They reduce your system inventory, eliminate the need for special production equipment. But even though the MHW709/MHW710 are "complete" UHF power drivers and reduce RF design and production to a new level of ease, there are a few operation and testing considerations to follow for best results.

The modules are conservatively rated. Actual output power capability is 50 to 70% above rated power. However, the equipment designer should not design a product using the module above the rated output power. In some cases, if smaller margins are acceptable and certain other conditions are met, some of the reserve power output can be used. In this case, please contact your Motorola representative for specific recommendations.

When operated within published specifications, the maximum device current density seen in a limit module will be 1.5×10^5 A/cm^2. Maximum die temperature with a 100° C base plate temperature will be 165° C.

Nominal ratings are for a 12.5 Vdc supply (V_s at pin 5) and control (V_{sc} at pin 3) voltage. Specifications such as power gain, efficiency, and input VSWR are measured with the nominal 12.5 Vdc supply and an output power of 13 W (MHW710) and 7.5 W (MHW709).

Gain Control

The preferred method of operation is to apply 12.5 Vdc to both pin 3 and pin 5 through the recommended decoupling network. (In general, the module output power should be limited to 14 W, MHW710; 8.5 W, MHW709.) The output of the module is then set by adjusting the input drive level. Operation in this manner will result in the best performance with temperature variation.

Pin 5 supplies collector voltage to the input stage in the module. This pin is internally bypassed by a .018 μF chip capacitor effective for frequencies from 5 MHz through the operating frequency. Due to size limitations in the module, additional external low frequency decoupling effective below 5 MHz is required (as is required with discrete UHF transistors). If pin 5 is used to reduce the module output, two characteristics may cause an application problem.

One is that with the drive power appreciably above that required (+2 dB or so) for 13 watts output, the voltage on the first stage may be as low as four or five volts. This low voltage tends to increase the slump in output power with increasing temperature as opposed to the condition of pin 5 = pin 3 = 12.5 V and drive adjusted for desired power output. Second, if voltage to pin 5 is derived from a series dropping resistor and the value of the resistor is

above 10 to 20 ohms, the output power will tend to rise with decreasing drive which could cause problems in an application using an automatic gain or output leveling circuit. If pin 5 is fed from a regulated voltage source, as opposed to a series dropping resistor, this problem does not arise, however, the temperature slump characteristic is still present.

Typically, the MHW710 slump at 80° C from rated output at 25° C with V3 = V5 = 12.5 Vdc is 9 to 12%. With pin 5 voltage set for rated output power and rated drive applied, the typical slump will be 10 to 16% at 80° C. Slump in the MHW709 under the same conditions is typically 5% less than the above figures.

Decoupling

As mentioned, size limitations in the module make it necessary to provide external coupling for frequencies below 5 or 10 MHz. This can take the form of a network as shown on the data sheet. All decoupling capacitors internal to the module are .018 μF chips. Output and interstage blocking capacitors are 39 pF NPO chips. This chip type has a nominal reactance to 9 ohms in the UHF band and was selected to decrease the module gain at frequencies below the pass band. Also, the base return chokes in all stages were selected to degrade gain slightly at UHF with greater effect at lower frequencies. The use of small coupling and blocking capacitors along with low impedance base returns reduces the loop gain at low frequencies to minimize low frequency problems from the increased device gains below the operating frequency.

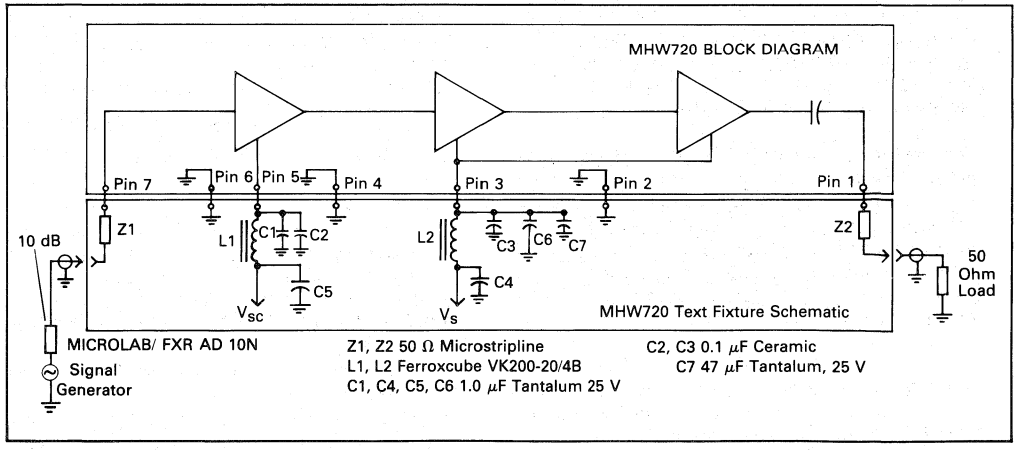
The decoupling network shown on the data sheet is used during final test of the module and has been found effective for our test setup. Differences in test circuit layout, ground current paths or other low frequency feedback circuits could require a modified decoupling network. Some applications may benefit from the use of a series R-C damping circuit connected to ground from pins 5 or 3. This can consist of a 5 to 10 ohm carbon resistor in series with a 1 to 10 μF, 25 volt electrolytic or tantalum capacitor.

Source and Load Impedances

The modules are designed for proper operation with source and load impedances of 50 ohms resistive. With proper decoupling, they will be stable with 2:1 VSWR source and load impedances, any phase angle and any combination of phase angles at nominal drive and power output. In addition, the rf drive and supply voltage can be varied over wide ranges. Typically, during this test, no spurious outputs are seen except with drive powers above 300 mW taken simultaneously with supply voltages below 4 or 5 volts. This condition of simultaneous high drive and low voltage will most likely never be seen in actual applications.

Most problems with module instabilities are a function of poor source impedance or poor decoupling. If a tendency is seen for the module to "snap on" or have hysteresis in the output power versus input power curve, the problem is most likely due to a source VSWR above 2:1 relative to 50 ohms. To check this, put a 3 dB or 6 dB

FIGURE 2 — UHF POWER MODULE TEST SETUP



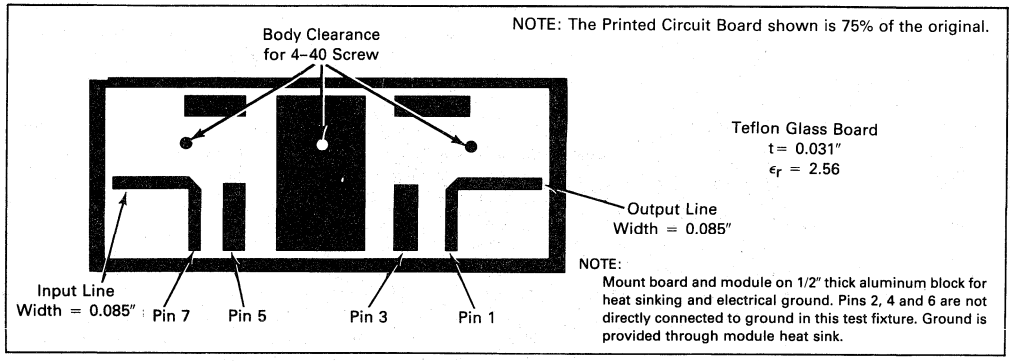
NOTE: No Internal D.C. blocking on input pin.

matched pad between the source and the module. The hysteresis or "snap" should disappear if the problem is source impedance. If "jumps" are noticed during varying input power conditions, the problem is most likely low frequency breakup due to insufficient low frequency decoupling—this can be seen on a spectrum analyzer sampling the output power. If a spectrum analyzer is not available, an ac-coupled 10 MHz oscilloscope on the dc feed pins at the module will usually detect low frequency breakup.

a spectrum analyzer. It has been found that at least 90 percent of semiconductor failures during load mismatch tests are due to spurious breakup during the test. When the spurious problems are solved, the burnout problems are also solved.

The MHW modules are 100% tested for burnout and spurious breakup two times during the production process. One test is performed after the module is completed and on the heatsink, another is performed after the module is capped and marked. The 13 watt modules are tested at 17 to 20 watts output into a load with a return loss of less than 0.7 dB at all phase angles (greater than 25:1 VSWR) and the 7.5 watt modules are tested at 10 to 12 watts into the same load.

FIGURE 3 — UHF POWER MODULE TEST FIXTURE PRINTED CIRCUIT BOARD



When using the module as a drop-in for other modules, it has been found that circuit "tweaks" made to compensate for antenna switching and output filter VSWR to provide optimum performance with a particular type module may degrade the performance of the MHW series modules. The output circuit in this module is a low-pass Chebyshev impedance transforming network. It is carefully designed to provide a 50 ohm source impedance with a VSWR of less than 1.3:1 at 13 watts power output and 12.5 V supply. The power available to the load (forward power as measured by a directional coupler) with this module will not degrade more than 20% from the power set into a 50 ohm load when a load with a VSWR of 2:1 is placed on the output and varied through all phase angles. This characteristic holds true throughout the rated frequency range of the module.

Load Mismatch

When performing a load mismatch capability test with any semiconductor device, especially in a new environment where all sources of regeneration are not yet identified, one should monitor the output of the device with a directional sampling scheme and display this output on

In summary, it is recommended that the MHW709/710 series modules be operated under the following conditions:

1. Source and load VSWR $\leq$2:1 with respect to 50 ohms.
2. Proper low frequency decoupling.
3. Supply voltage of 12.5 volts applied to both pin 5 and pin 3 with driver power adjusted for desired output power.
4. Sufficient heatsinking so that module flange does not exceed 100° C (preferably 80° C).
5. Flange at rf ground potential. The "ground" pins 2, 4, and 6 are not sufficient to establish a good rf ground at UHF by themselves.

When these rules are followed, the MHW709/710 series modules will provide the performance you expect.

CONTROLLED — Q RF TECHNOLOGY — WHAT IT MEANS, HOW ITS DONE

The difficult transfer of high frequency energy from a signal source to the control element of an RF power transistor is efficiently achieved by a new design philosophy. Both monolithic and hybrid IC techniques are used to include a matching network in the transistor package and overcome this tough design problem.

The insertion of a matching network into an RF power transistor package has cured many evils encountered in high frequency circuit design. Devices using such an internal impedance matching network have been dubbed Controlled Q because that is exactly what the added package circuitry does — it gives the power transistor a consistent and highly controlled electrical quality (Q) factor. In a nutshell controlled Q increases guaranteed gains from previously available 4 dB to 5 or 6 dB in the 470 MHz region at 12.5 V. The controlled Q means that these devices are easier to match into circuit networks, and offer better consistency of high frequency parameters than other, non-controlled Q RF power devices.

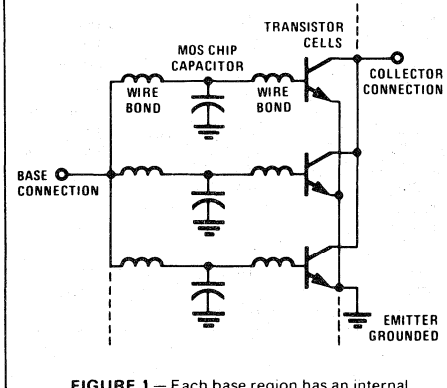


FIGURE 1 — Each base region has an internal matching network included in the CQ package.

The Old and the New

There are no panaceas for the complexities of broadband RF circuit design. With or without controlled Q, circuit networks must be designed to impedance-match the different stages. Gain and power output has to be optimized for the particular application, while maintaining a specified overall circuit bandwidth.

With older RF power devices, such as the 2N6136, a complete interstage matching network had to be provided using discrete passive components external to the transistor package. Not only did the circuit take up a lot of space, but its overall series component reactance limited design capability — especially in bandwidth. In addition, parasitic elements caused by the extra components, and package geometries interfered with establishing a solid signal ground.

With newer controlled Q devices, "inside-the-package" construction of some of the network matching elements brings the network closer to the active transistor die. Not only does this eliminate the number of required external components, but it also means that a small amount of capacitance can minimize the imaginary part of the input impedance for maximum bandwidth. Internal construction techniques help establish a better signal ground by removing most parasitic reactance.

A Closer Look

Controlled Q transistors use both monolithic and hybrid techniques in their construction. The active transistor die is fabricated using monolithic integrated circuit methods. A small MOS chip capacitor is wire bonded to the active transistor die thus incorporating hybrid technology. The

resulting total transistor package can be thought of as an active transmission line element for high frequency (to 500 MHz) amplifier design. Figure 1 shows a portion of the device circuit.

To meet the high power handling requirements the controlled Q transistors are specially constructed with each of its multiple emitters having its own ballast resistor. These nichrome (NiCr) resistors, shown in the close-up of Figure 2, have different resistance values to compensate for thermal differences of various portions of the transistor chip. This prevents overloading of some emitters due to temperature difference. This Isothermal* resistor design technique assures balanced current distribution throughout the transistor for more consistent operation at various power levels.

Emitter inductance and its undesirable gain reducing negative feedback are minimized in controlled Q devices, by establishing a solid ground for the transistor emitters. This is accomplished by using the lead frame to extend the ground plane completely around the device. Emitter wires are then attached to this ground plane. Such an emitter bonding technique has been shown to contribute more than 50% of the gain increase of a controlled Q device in the 470 MHz region. Its total gain of 5.22 dB is significantly higher than a non-CQ device of the same 25 W version that gives around 4.0 dB gain.

Controlled Q transistors also have bonding wires extending from each transistor base region to the MOS capacitor chip and then out to the package base lead. These bonding wires and the MOS capacitor interconnect one half of an input impedance matching network as in Figure 3.

*Trademark of Motorola Inc.

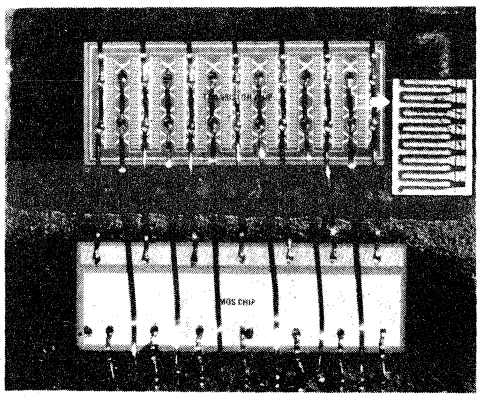


FIGURE 2— A close-up view of the emitter ballasting resistors.

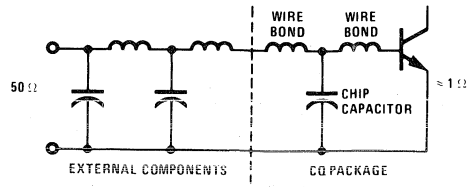


FIGURE 3 – Part of the transmission network inductance and capacitance is provided in CQ transistor packages.

Controlled Q production methods not only increase device yield, but also allow all final factory testing to be done in fixed-tuned test equipment. This means ease of final test for the semiconductor manufacturer, but more importantly, insures the consistency of controlled Q transistors from device to device. To the RF equipment manufacturer, this means that once a piece of communications gear has been designed, controlled Q devices can be dropped into amplifier modules with a minimum of circuit adjustment and tuning.

What's Available

Motorola's MRF series of high frequency power devices are available in stripline opposed emitter packages which offer excellent thermal characteristics along with controlled Q operation. Available in both 12.5 V and 28 V devices, these transistors listed in Table I are capable of operating at frequencies to 900 MHz with power outputs to 50 watts.

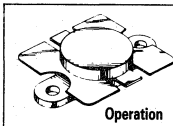
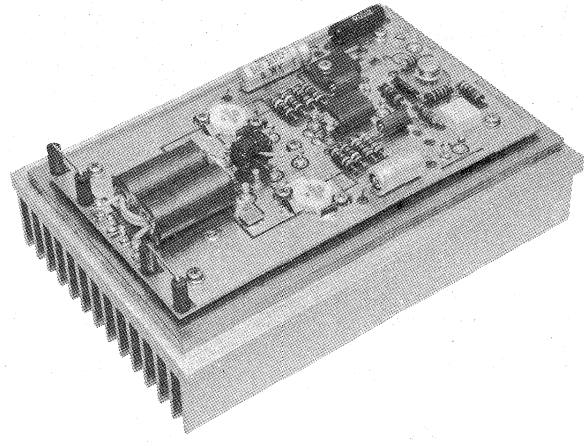


TABLE I – Controlled Q RF Power Transistors

Device	Operation Voltage	Output Power	Frequency	Comment
MRF243 MRF245	12.5 V	60 W 80 W	to 175 MHz	For VHF Large Signal Application
MRF316 MRF317	28 V	80 W 100 W	to 200 MHz	For VHF MIL Aircraft and Mobile Operation
MRF641 MRF644 MRF646 MRF648	12.5 V	15 W 25 W 40 W 60 W	to 512 MHz	For UHF FM Mobile Applications
MRF325 MRF326 2N6439 MRF327 MRF338 MRF329	28 V	30 W 40 W 60 W 80 W 80 W 100 W	to 500 MHz	For 225-400 MHz Aircraft and Mobile Operation
MRF840 MRF842 MRF844 MRF846		7 W 20 W 30 W 40 W	to 900 MHz	For 900 MHz Land Mobile

GET 300 WATTS PEP LINEAR ACROSS 2 TO 30 MHz FROM THIS PUSH-PULL AMPLIFIER

Prepared by
Helge Granberg
Circuits Engineer, SSB

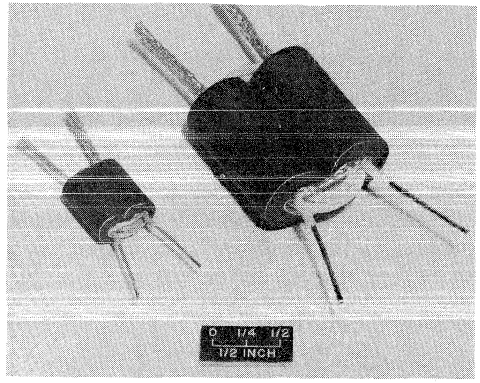


(The heat sink shown with amplifier is sufficient only for short test periods under forced air cooling.)

This bulletin supplies sufficient information to build a push-pull linear amplifier for 300 watts of PEP or CW output power across the 2- to 30-MHz band. One of Motorola's new high-power transistors developed for single-sideband, MRF422, is used in this application.

Like all transistors in its family of devices, MRF422 combines single-chip construction that is advancing the state-of-the-art, and improved packaging to accommodate the low collector efficiencies encountered in class B operation. Rated maximum output power is 150 watts CW or PEP with intermodulation distortion spec'd at −30 dB maximum, −33 dB typical. Although not recommended, a saturated power level of 240- to 250-W is achievable. Maximum allowable dissipation is 300 W at 25°C.

Because of its excellent load and line voltage regulating capabilities, an integrated circuit bias regulator is used in the amplifier. The MPC1000, originally described in this bulletin, consisted of a MC1723 chip and a built-in pass transistor. The manufacture of this device has been discontinued however, and the board lay-out was modified to incorporate the above two in separate packages. The load regulation typically measures less than 2% at current levels up to 0.5 A, which assumes an h_{FE} of 40 for the RF power devices. The board surface provides a sufficient heat sink for the 2N5990 pass transistor, but a separate heat dissipator, such as Thermalloy 6107 can be added if necessary. With the component values shown, the bias is adjustable from 0.4 to 0.8 volts.



Transformer Construction

Gain flatness over the band is achieved using base input networks R_1C_2 and R_2C_3 and negative feedback through R_3 and R_4. The networks represent a series reactance of 0.69 ohms at 30 MHz rising to 1.48 ohms at 2 MHz. A single-turn winding in the collector choke provides a low-impedance negative feedback source, thus R_3 and R_4 determine the amount. The reactance of C_4 reduces feedback at high frequencies with the result that feedback increases an average of 4 dB per octave at decreasing frequency.

For continuous operation at full power CW, it is recommended that heat sink compound, such as Dow Corning #340, be applied between the board surface and R_3 and R_4, and if possible have air circulating over the top of the circuit board as well.

The effective base-to-base impedance, increased by the RC networks is about 5 ohms at midband. As a result of this and the 9:1 impedance ratio in the input transformer T1, the input VSWR is limited to 1.9:1 or less across the band. Transformer T2, in addition to providing a source for the feedback and carrying the dc collector current, acts as the rf center tap of the output transformer. To construct T2, wind 5 turns of 2 twisted pairs of AWG No. 22 enameled wire on a Stackpole 57-9322 toroid (Indiana General F627-8Q1).

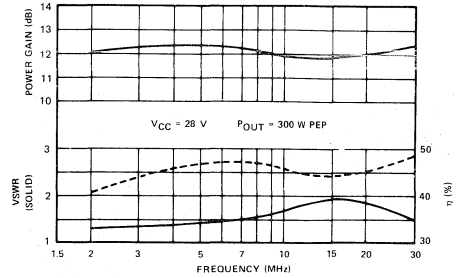
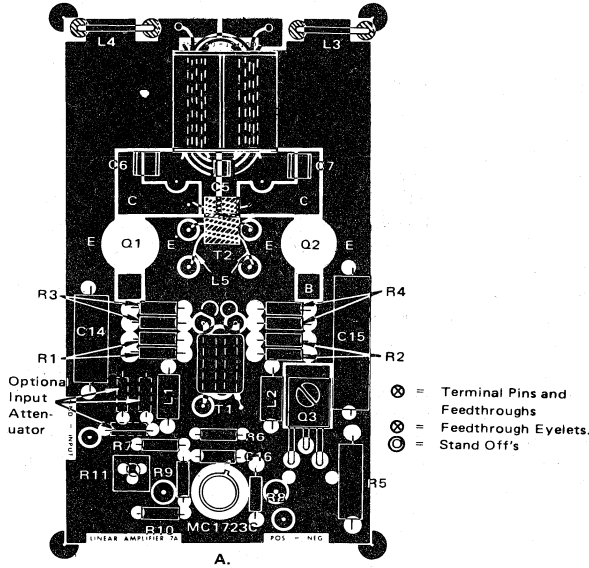
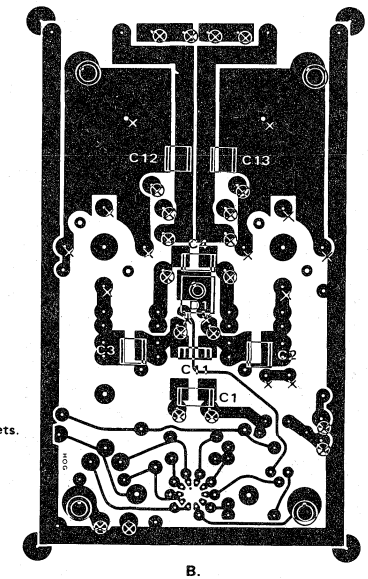


Figure 1 — Collector Efficiency, Power Gain and VSWR vs Frequency

A Stackpole dual balun ferrite core 57-1845-24B is used for T1. The secondary is made of ⅛″ copper braid, through which three turns of the primary winding (No. 22 Teflon® insulated hook-up wire) are threaded. The construction of T3 is similar to that of T1. It employs two Stackpole 57-3238* ferrite sleeves which are cemented together for easier construction. The primary is made of ¼″ copper braid, through which three turns of No. 16 Teflon® insulated wire are threaded for the secondary.

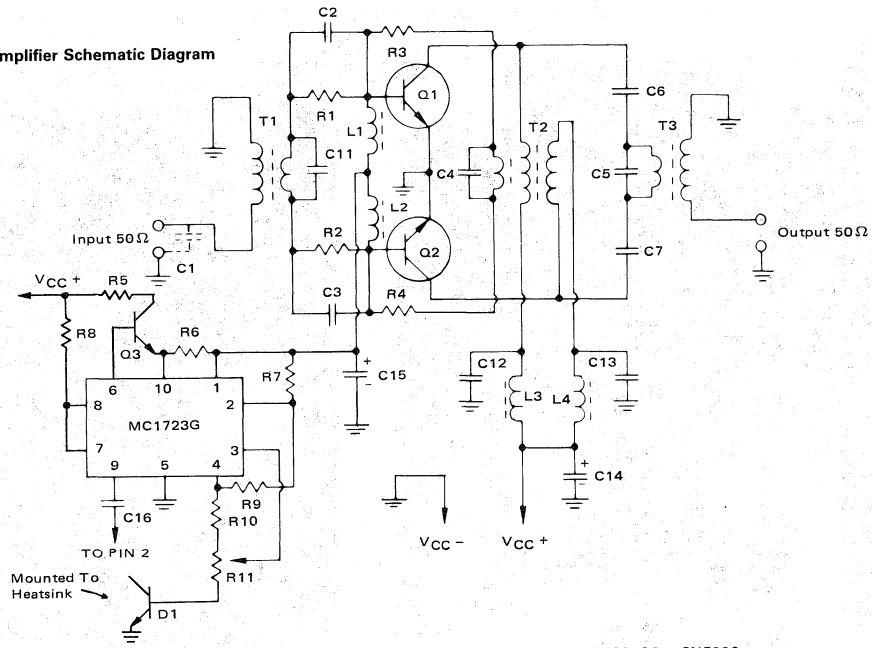


A.



B.

300-Watt Linear Amplifier Schematic Diagram



C1 – 100 pF
C2, C3 – 5600 pF
C4, C5 – 680 pF
C6, C7 – 0.10 μF
C11 – 470 pF
C12, C13 – 0.33 μF
C14 – 10 μF – 50 V electrolytic
C15 – 500 μF – 3 V electrolytic
C16 – 1000 pF

R1, R2 – 2 X 3.3Ω, 1/2 W in parallel
R3, R4 – 2 X 3.9Ω, 1/2 W in parallel
R5 – 47Ω, 5 W
R6 – 1.0Ω, 1/2 W
R7, R8 – 1.0 k, 1/2 W
R9 – 18 k, 1/2 W
R10 – 8.2 k, 1/2 W
R11 – 1.0 k Trimpot
D1 – 2N5190
L1, L2 – Ferroxcube VK200 20/4B
L3, L4 – 6 ferrite beads each, Ferroxcube 56590 65/3B

Q1, Q2 – MRF422, Q3 – 2N5990
T1, T2, T3 – See text

All capacitors except electrolytics and C16 are chips –

Union Carbide type 1813 and 1225, or Varadyne size 18 or 14, or equivalent

For production quantities, the braid in T_3 may be made of brass or copper tubes with their ends soldered to pieces of PC board laminate. See cover picture and Motorola AN-749 for details.

The bandwidth characteristics of these transformers do not equal those of the transmission line type, but they're much easier to duplicate.

The measured performance of the amplifier is shown in figures 1, 2, and 3 and harmonic rejection data in table I.

Table I. Output harmonic contents, measured at 300-W CW (all test data taken using a tuned output, narrow band signal source).

	2nd	3rd	4th	5th
f (Mhz)	(dB below the carrier)			
30.0	−38	−25	−34	−48
20.0	−33	−13	−43	−45
15.0	−50	−10	−51	−47
7.50	−40	−30	−55	−47
4.0	−37	−22	−55	−37
2.0	−36	−18	−45	−37

*A similar product is available from Fair-Rite Products Corp., Wallkill, N.Y., 12589

®Registered trademark of DuPont

PCB, chips capacitors, transformers T_1, T_2, T_3, and ferrite beads are available from: COMMUNICATIONS CONCEPTS, 2648 N. Aragon Ave., Kettering, Ohio 45420. Telephone: (513) 294-8425.

NOTE: The Printed Circuit Board shown is 75% of the original.

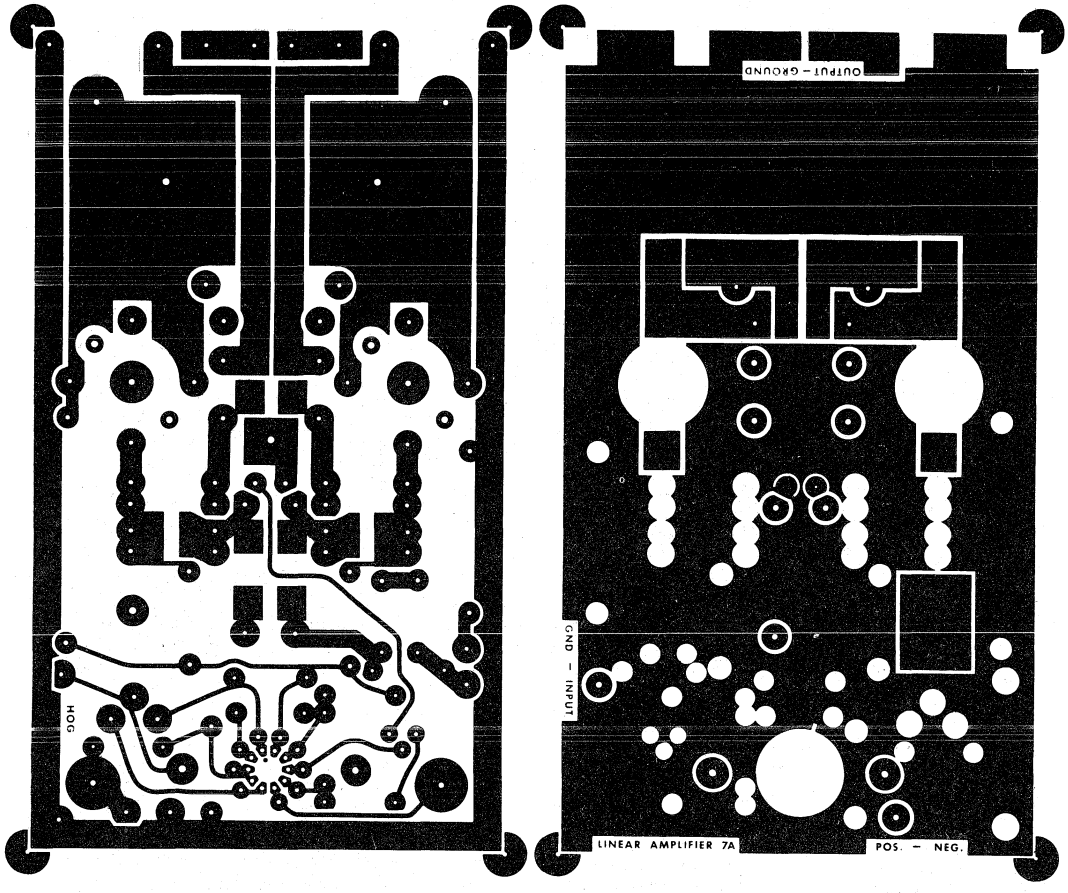


Figure 2 — IMD vs Frequency

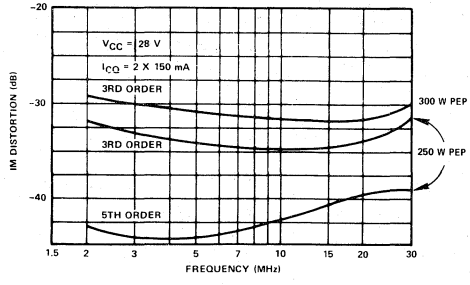
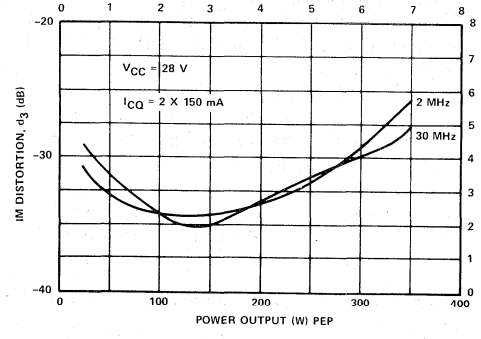
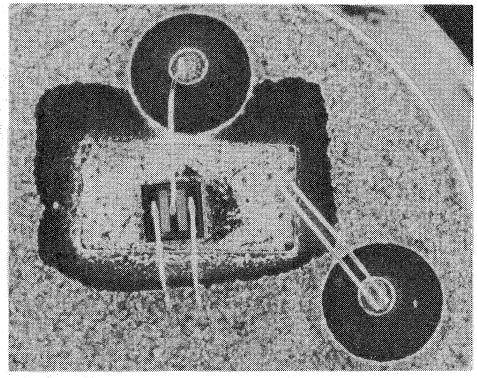


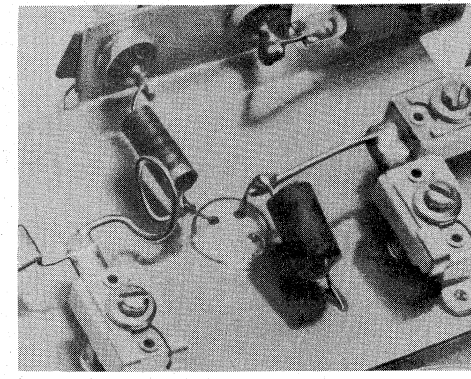
Figure 3 — IMD vs Power Output



THE COMMON EMITTER TO-39 AND ITS ADVANTAGES

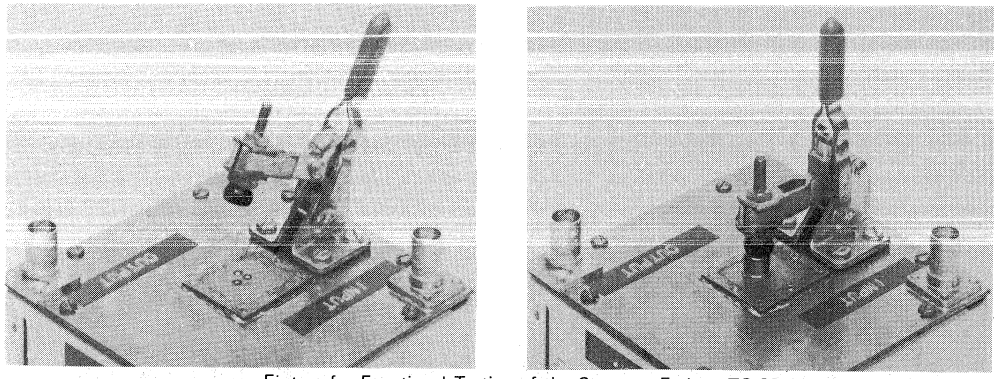
Prepared By Rich Potyka





The common emitter TO-39 package is one of Motorola's latest innovations in low-cost rf packages. It differs from conventional TO-39's or TO-5's in that the emitter, not the collector, is connected to the metal case. To achieve this, a Be0 insulating block metallized on top and bottom is brazed to the can bottom and the transistor chip brazed to the Be0 insulator. Wires are then bonded from the chip and insulator block to the terminals and the can bottom as shown in the photo. With NPN transistors, this configuration permits direct connection of the can to rf and negative dc ground for many class B and C circuits.

Two important advantages can be derived from the common emitter TO-39: By connecting the case to the rf circuit ground, emitter inductance is reduced and gain increased by 3 to 5 dB over that of comparable, conventionally wired transistors. And the case may be directly pressed, clipped, or soldered to the heat sink with no effect on rf performance. This feature may eliminate the need for the heat radiating "coolers" because soldering the transistor bottom to the circuit, typically a PC board, improves dissipation by removing heat through the thick metal base rather than the thin can.

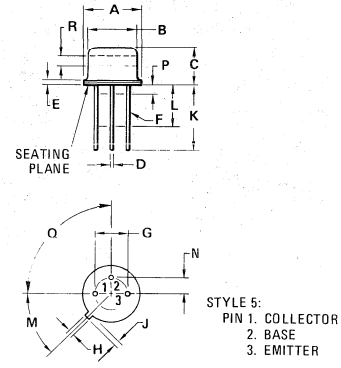


Fixture for Functional Testing of the Common Emitter TO-39

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO-39



For example, the MRF227 was mounted in this manner and a θ_{jc} of 15°C/W was measured using a Barnes RM-2A Infrared Microscope. Compared to an MRF607 in a conventional package operating under identical conditions, this is greater than a 2:1 reduction in thermal resistance. And as side benefits, the lower θ_{jc} also reduces power slump and improves reliability.

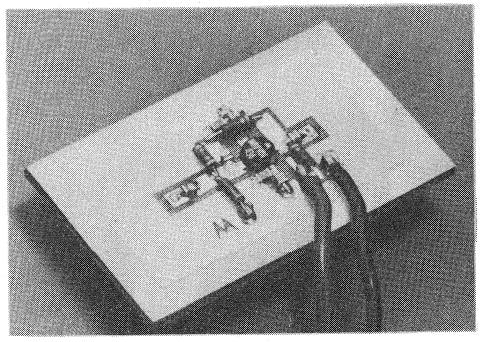
In many mobile radios CE-TO39 devices can replace stud or flange mounted stripline parts used for 1- to 4-watt drivers. This conversion should normally offer a significant savings in the cost of parts as well as the costs of mounting hardware and labor.

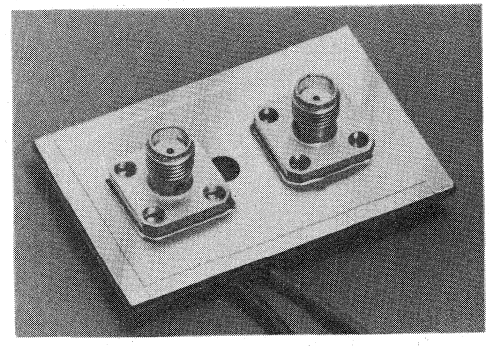
The designer of compact handheld radio equipment will find the CE-TO39 offers a real advantage from the elimination of interstage RFI or coupling because the can is at rf ground. Stability is usually improved and the higher available gain may reduce the number of transmitter stages. Simplified and improved cooling may also be obtained by connecting the can directly to the radio housing or chassis.

To sum it up: The emitter-to-can wired TO-39 known as the CE-TO39 offers the designer significant improvements in both gain and thermal performance. Because of its price, compared to SOE and TO-60 packages, the designer can use the CE-TO39 to reduce costs. And he can make his design easier to assemble with no loss in rf performance.

AMPLIFIER GAINS 10 dB OVER NINE OCTAVES

Prepared by:
Mike Hadley
Industrial Applications Engineer





The introduction of Motorola encapsulated transistors fabricated with ion-implanted arsenic emitters has made a reality of economical small-signal amplifiers with bandwidths exceeding 1 GHz. The recently developed MRF901, an example of this technology, has an f_T exceeding 4.5 GHz, and a maximum noise figure at 1 GHz of 2.5 dB. The device package (case 302) employs the Motorola dual emitter bonding concept to minimize parasitic inductance and enhance high-frequency performance.

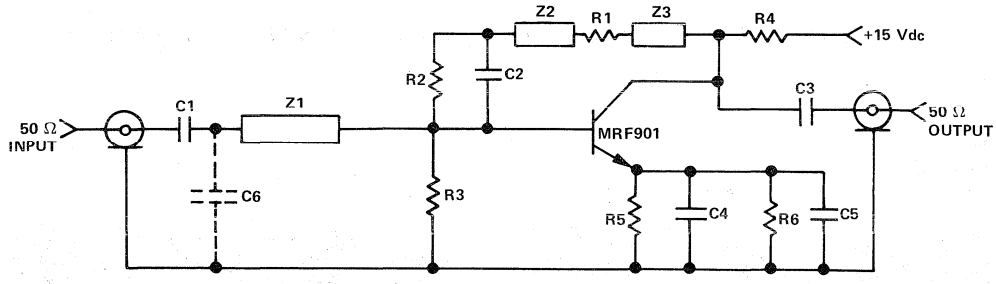
Using the MRF901, an amplifier has been developed which exhibits a nominal gain of 10 dB over nine octaves of bandwidth. The circuit design is a class A amplifier employing both ac and dc feedback. Bias is stabilized at 15 mA of collector current using dc feedback from the collector. The ac feedback from collector to base, and in each of the partially bypassed emitter circuits, compensates for the increase in device gain with decreasing frequency, yielding a flat response over a maximum bandwidth. Transistor S parameters, as provided by the MRF901 data sheet, and computer-aided circuit optimization techniques were used to choose component values for gain flatness, input VSWR and output VSWR. The described performance was achieved using common high-frequency amplifier construction techniques and a standard printed circuit board substrate. Even better results could be expected from the use of today's hybrid circuit technology.

Evaluation of the amplifier shows a nominal 10 dB power gain from 3 MHz to 1.4 GHz. With only a minimum matching network used at the amplifier input, the input VSWR remains less than 2.5:1 to approximately 1 GHz while the output VSWR stays under 2:1 to approximately 1.4 GHz (figure 2). If input impedance matching were of prime consideration, connecting a 2.1 pF capacitor from the junction of C1 and Z1 to ground (C6 in figure 1) would hold input VSWR below 2.2:1 over the complete frequency range (figure 3). Note that a slight degradation in gain flatness and output VSWR occurs with the addition of C6. A more elaborate network design would probably optimize impedance matching while maintaining gain flatness.

The amplifier was built on a glass Teflon® printed circuit board 1.8″ x 1.2″. A 2:1 reproduction of the circuit pattern is provided in figure 4. The type OSM215 50-ohm input and output connectors were mounted opposite the component side to facilitate laboratory measurements. Board size could be reduced to approximately half by reducing the ground plane around the circuit perimeter. A combination of chip capacitors, chip resistors and standard carbon resistors were used to obtain maximum performance at minimum cost.

Extra care was taken to keep all component lead lengths to an absolute minimum and to provide a good ground plane. In the interest of maintaining a good ground, copper foil was soldered at the board edges to connect the top and bottom circuit grounds, and an eyelet was inserted near each emitter lead.

Figure 1. Schematic Diagram



C1–C3 – 2200 pF chip capacitor
C4, C5 – 6.5 pF chip capacitor
C6 – Optional 2.1 pF chip capacitor
Z1 – 0.3" x 0.125" microstrip line
Z2 – 0.15" x 0.125" microstrip line
Z3 – 0.3" x 0.125" microstrip line
R1 – 200 Ω, 1/8" W, ±5% carbon resistor
R2 – 4.3 kΩ carbon resistor
R3 – 680 Ω carbon resistor
R4 – 560 Ω carbon resistor
R5, R6 – 15 Ω ±5% chip resistor
Substrate – 1 oz. copper, double-sided glass Teflon® board 0.0625" thick, $\epsilon_r \approx 2.5$
® Registered trademark of DuPont

Figure 2.
Gain and VSWR vs Frequency

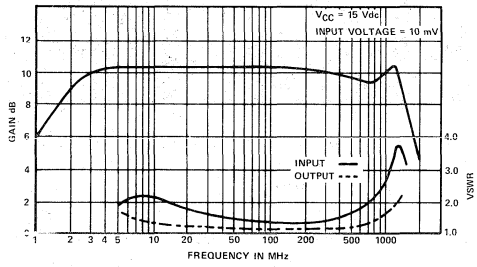


Figure 3.
Gain and VSWR vs Frequency with Matching Capacitor C6

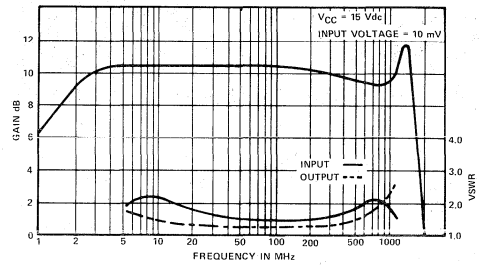


Figure 4. Amplifier PCB Artwork

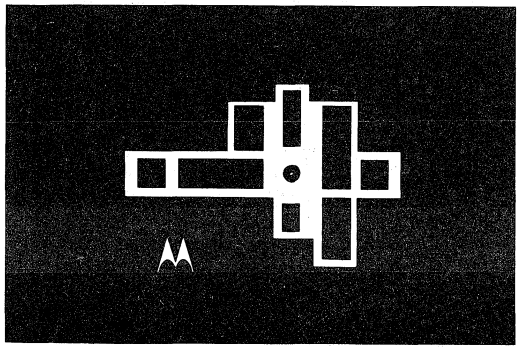
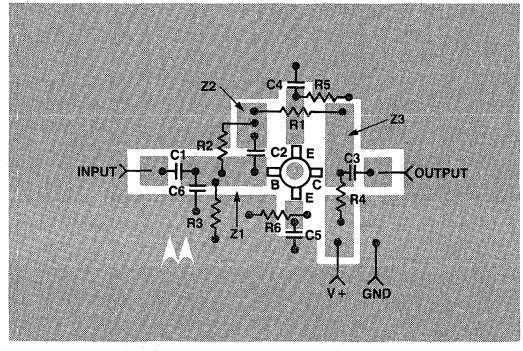


Figure 5. Parts Layout



6

MEASURING THE INTERMODULATION DISTORTION OF LINEAR AMPLIFIERS

Prepared by
Helge Granberg
Circuits Engineer, SSB

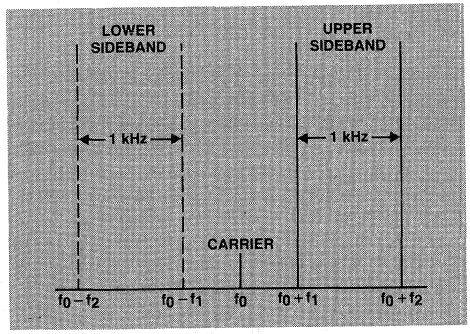
The measured distortion of a linear amplifier, normally called Intermodulation Distortion (IMD), is expressed as the power in decibels below the amplifier's peak power or below that of one of the tones employed to produce the complex test signal.

A signal of three or more tones is used in certain video IMD tests, but two tones are common for HF SSB. The two-tone test signal provides a standard, controlled test method, whereas the human voice contains an unknown number of frequencies of various amplitudes and couldn't be used for accurate power and linearity measurements. Separation of the two tones, for voice operation equipment, may be from 300 Hz to 3 kHz, 1 kHz being a standard adopted by the industry.

Generation of the Test Signal

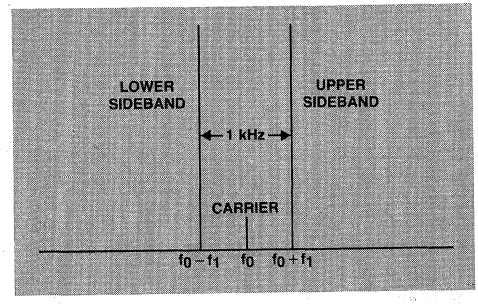
The two-tone IMD test signal can be generated by a number of means of which the following three are the most common:

System A—A two-tone audio signal is formed by algebraically adding two sine wave voltages of equal amplitude which are not harmonically related, e.g., 800 Hz and 1.8 kHz. This two-tone audio signal is fed into a balanced modulator together with an RF carrier, one sideband filtered out, and the resultant further mixed to the desired frequency and then amplified. The system is useful in testing complete SSB transmitters. A commercial transmitter can also be used as a signal source for testing linear amplifiers.



SYSTEM A

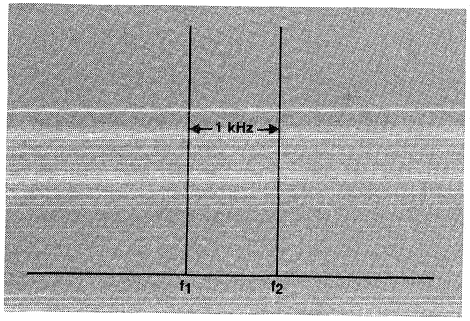
System B—In this method, a signal of approximately 500 Hz is fed into a balanced modulator together with an RF carrier and amplified to the required power level.



SYSTEM B

The resultant is a double-sideband signal that resembles a single-sideband signal generated under two-tone sine wave conditions. Viewed on a scope screen, the envelope produced by this method appears the same as a SSB two-tone pattern. However, unlike the System A test signal, there is a controlled and fixed phase relationship between the two output tones. This system is widely employed to generate the test signal for linearity measurements.

System C—Two equal amplitude RF signals, separated in frequency by 1 kHz, are algebraically added in a hybrid coupler. The isolation between input ports must be high enough to avoid interaction between the two RF signal generators. Short-term stability (jitter) should be



SYSTEM C

less than one part per million at 30 MHz. The carrier is nonexistent as compared to A and B, and the two-tone signal is generated as the RF voltages cancel or add at the rate of their difference frequency according to their instantaneous phase angles. Because no active components are involved, very low IM distortion is achievable. This system is useful in applications where low distortion and low power levels are required.

Except for the position of the carrier in respect to the two tones, displays of the signals produced by systems A, B and C appear identical on a spectrum analyzer screen. Sometimes, however, the suppressed carrier may remain below the noise level of the instrument. Any spectrum analyzer used for SSB linearity measurements must have an IF bandwidth of less than 50 Hz to allow the two closely spaced tones to be displayed with good resolution. Figure 1 shows a low distortion, two-tone envelope displayed on a scope screen. On a spectrum analyzer screen the same signal displays as two discrete frequencies separated by the difference of the audio frequency or frequencies. See figure 2. The display represents the rate at which peak power occurs when the two frequencies are in phase and the voltages add. Thus, one peak contains one-fourth (–6 dB) of the peak envelope power (PEP). An average reading power meter would read the combined power of the tones, or half the PEP, assuming the envelope distortion is negligible. The third order distortion products (d_3), fifth order (d_5), etc., can be seen on each side of the tones. The actual power (PEP) of each distortion product can be obtained by deducting the number of decibels indicated by the analyzer from the average power. This value may be useful in determining the linearity requirements of the signal source. While the maximum permissible distortion levels of the driver stages in a multi-stage amplifier may be difficult to specify, a 5- to 6-dB margin is usually considered sufficient.

Types of Distortion

The nonlinear transfer characteristics of active devices are the main cause of amplitude distortion, which is both device and circuit dependent. On the other hand, harmonic and phase distortion, also present in linear amplifiers, are predominantly circuit dependent. Even order harmonics, particularly noticeable in broadband designs, cause the harmonic distortion. Push-pull design will climinate most of the even-order-caused harmonic distortion and the driver stages, where efficiency is of less concern, can be biased to class A.

Phase distortion can be caused by any amplitude or frequency sensitive components, such as ceramic capacitors or high-Q inductors, and is usually present in multi-stage amplifiers. This distortion may have a positive or negative sign, resulting in occasions where the level of some of the final IMD products (d_3 or d_5, or both) may be lower than that of the driving signal, due to cancelling effects of opposite phases. Actual levels depend on the relative magnitude of each distortion product present.

From the above it is apparent that the distortion figures presented by the spectrum analyzer represent a combination of amplitude, harmonic and phase distortion.

Measurement Standards

As indicated earlier, there are two standard methods of measuring the IM distortion:

Method 1–In military standard (1131 A-2204B), the distortion products are referenced to one of the two tones of the test signal. The maximum permissible IMD is not specified but, numbers like –35 dB are not uncommon in some equipment specifications. However, when this measuring system is employed in industrial applications, the IMD requirement (d_3) is usually relaxed to –30 dB. Figure 3 shows the frequency spectrum of IM distortion products and their relative amplitudes for a typical class AB linear amplifier. Biasing the amplifier more toward class B will cause the lower order distortion products to go down and the amplitudes of the higher order products to increase. There is a bias point where the d_3 and d_5 products become equal resulting in 2–5 dB improvement in the lower order IMD readings.

Method 2–In the proposed EIA standard, the amplitude of the distortion products is referenced to the peak envelope power, which is 6 dB higher in power than that represented by one of the two tones. The amplifier or device indicating a maximum distortion level of –30 dB in Method 1 represents –36 dB with the EIA proposed standard. Conversely, a –30 dB reading with EIA's PEP reference would be –24 dB when measured with the more conservative military method. In practical measurements, the two tones can be adjusted 6 dB down from the zero dB line, and direct IMD readings can be obtained on the calibrated scale of the analyzer. Alternatively, the tone peaks can be set to the zero dB level and 6 dB deducted from the actual reading.

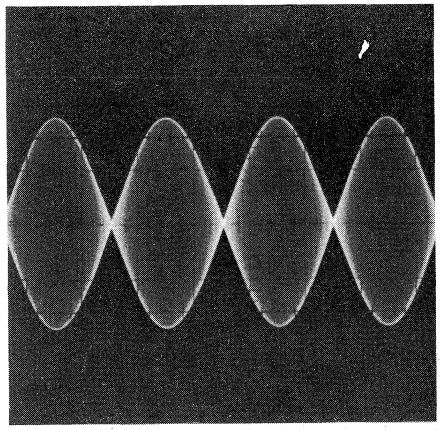


FIGURE 1. Two-tone test pattern generated by A, B or C.

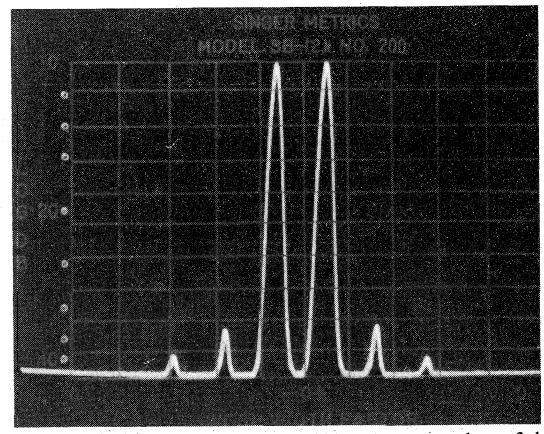


FIGURE 2. Test signal of figure 1 displayed by a spectrum analyzer. 3rd and 5th order distortion products are visible.

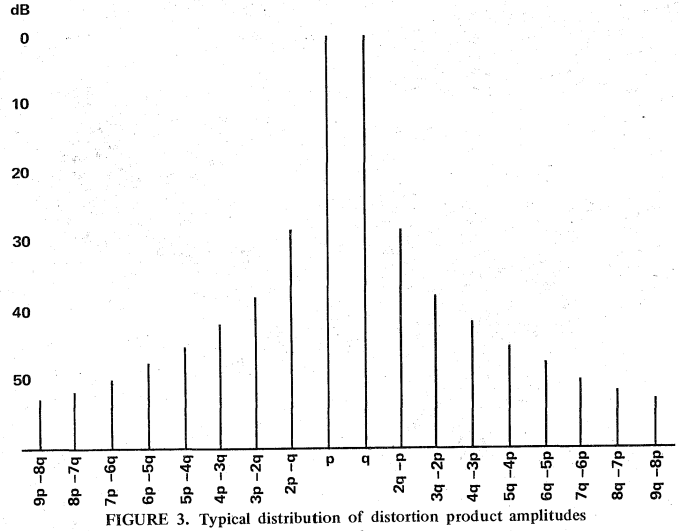


FIGURE 3. Typical distribution of distortion product amplitudes compared to the two fundamental frequency components.

The military standard, with the relaxed –30 dB IMD specification, is employed by most manufacturers of high power commercial transmitters and marine radio base stations. *The EIA measuring method is used by the majority of ham radio equipment and CB radio manufacturers. It is also used to measure IMD in various mobile radio applications operating from a 12.5-V nominal dc supply.

Because of the importance to your design, data sheets of the newer generation Motorola devices specify linearity tests appropriate to the expected application of the particular device and test conditions are always indicated.

*FCC specifications are now in effect covering maximum permissible distortion up to the 11th order products.

REFERENCES:

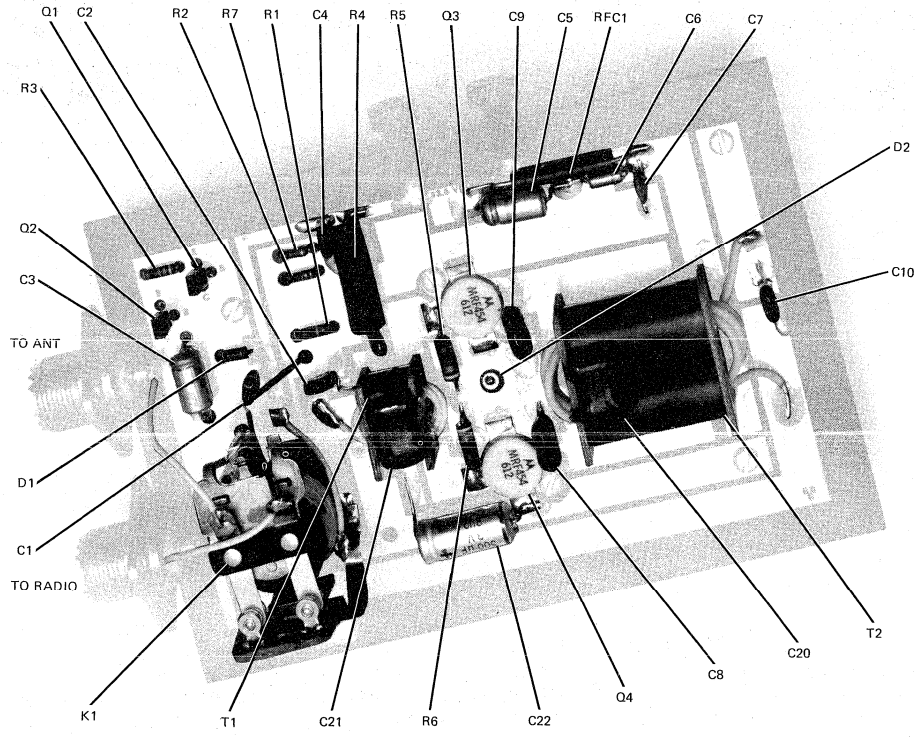
Pappenfus, Brueue & Schoenike, "Single-Sideband Principles and Circuits," McGraw-Hill.

William I. Orr, "Radio Handbook," 18th Edition, Editors and Engineers, Ltd.

Stoner, Goral, "Marine Single-Sideband," Editors and Engineers, Ltd.

Hooton, "Single-Sideband, Theory and Practice," Editors and Engineers, Ltd.

140W (PEP) AMATEUR RADIO LINEAR AMPLIFIER 2-30 MHz



The popularity of 2-30 MHz, SSB, Solid State, linear amplifiers is increasing in the amateur market. This EB describes an inexpensive, easy to construct amplifier and some pertinent performance information. The amplifier uses two MRF454 devices. These transistors are specified at 80 Watts power output with 5 Watts of input drive, 30 MHz, and 12.5 Vdc. The MRF454 is used because it is a readily available device and has the high saturation power and ruggedness desired for this application. This device is not characterized for SSB. However, IMD specs for the amplifier are shown in Figures 2 and 3.

THE AMPLIFIER

The performance of the amplifier can be seen in Figures 1, 2, 3, 5, 6, 7 and 8. The quiescent current is 500 mA on each device. This amount of bias was needed to prevent "cross over" at the higher output powers during SSB operation. The amplifier operates across the 2-30 MHz band with relatively flat gain response and reaches gain saturation at approximately 210 Watts of output power. Figure 5 depicts the amplitude modulated waveform with respect to a 100-Watt carrier. Figure 6 depicts the increased amplitude modulation at 50-Watt carrier. In both cases the peak output power is equal to approximately 210 Watts due to the saturation of the MRF454. The 50-Watt carrier is thus recommended in any amplitude modulated applications.

The bias diode D2 has been mounted in the heatsink for temperature tracking. The cathode is pressed into the heatsink and the anode extends through the circuit board. (See Figure 9.) Both input and output transformers are 4:1 turns ratio (16:1 impedance ratio) to achieve low input SWR across the specified band and a high saturation capability. T1* is made from FairRite Products, ferrite beads, material #77, .375" O.D. × .187/.200" I.D. × .44L". T2* is made from Stackpole Co. ferrite sleeves #57-3238-7D.

When using this design, it is important to interconnect the ground plane on the bottom of the board to the top; especially at the emitters of the MRF454s. Eyelets were used in this design, which are easier to apply, but #18 AWG wire can be used. On the photomask, (see Figure 10) ":" signifies where the ground plane has been interconnected. The letter "O" designates where the 4–40 screws are installed to fasten the board to the heatsink. 6–32 nuts are used as spacers on the 4–40 screws between the board and the heatsink to keep the board from touching the heatsink.

THE DESIGN

This amplifier was designed for simplicity. The design goal was to allow repeatability of assembly and reduce the number of components used. The amplifier will accept Single Side Band or Amplitude Modulation without external switching. A carrier operated relay circuit is on the same layout to make this an easy amplifier to add on to any suitable radio with an RF output of 1.0–5.0 Watts. All components used are readily available at most distributors and are relatively inexpensive.

*Ref: Application Notes
AN749 BroadBand Transformers and Power Combining Techniques for RF – H. Granberg
AN762 Linear Amplifiers for Mobile Operation – H. Granberg

NOTE: Parts and Kits for this amplifier are available from:

Communications Concepts
2648 N. Aragon Avenue
Kettering, OH 45420
(513) 296-1411

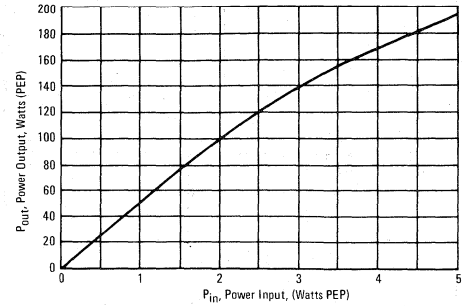


FIGURE 1–P_{out} vs. P_{in}, 30 MHz, 13.6 Vdc

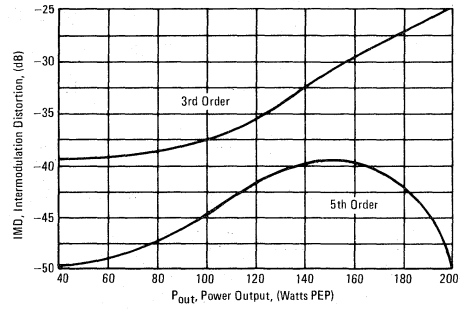


FIGURE 2–Intermodulation Distortion Versus P_{out}, 30 MHz, 13.6 Vdc

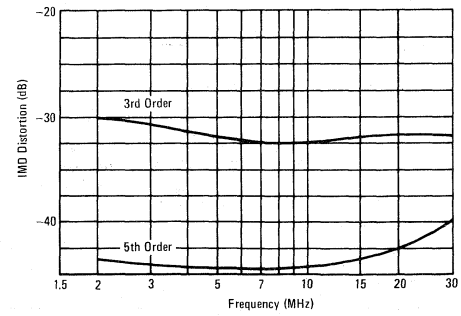
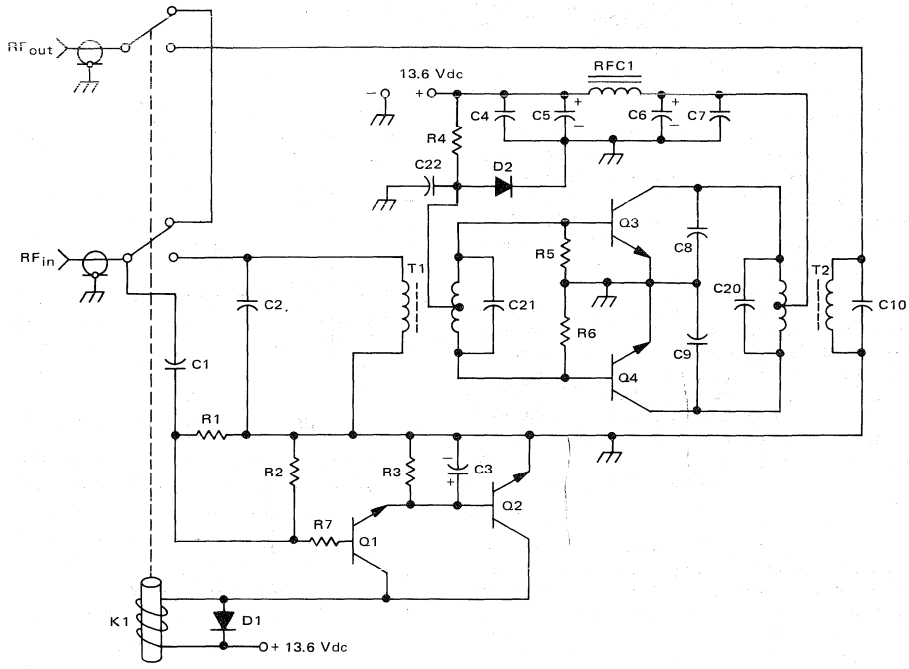
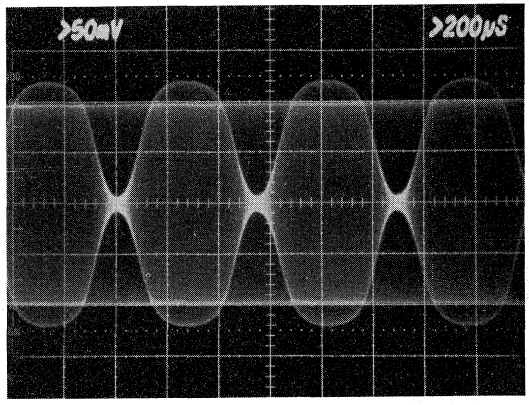


FIGURE 3–IMD vs. Frequency, P_{out} = 140 Watt PEP, 13.6 Vdc



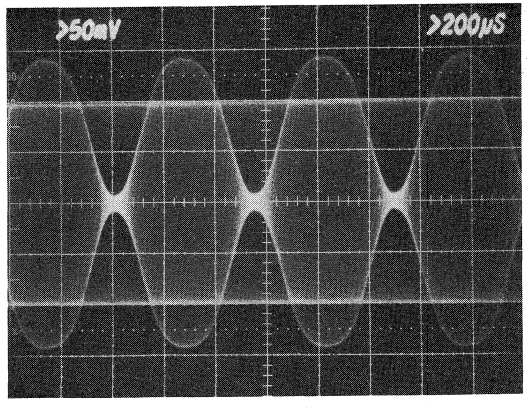
C1 = 33 pF Dipped Mica
C2 = 18 pF Dipped Mica
C3 = 10 μF 35 Vdc for AM operation, 100 μF 35 Vdc for SSB operation.
C4 = .1 μF Erie
C5 = 10 μF 35 Vdc Electrolytic
C6 = 1 μF Tantalum
C7 = .001 μF Erie Disc
C8, 9 = 330 pF Dipped Mica
R1 = 100 kΩ 1/4 W Resistor
R2, 3 = 10 kΩ 1/4 W Resistor
R4 = 33 Ω 5 W Wire Wound Resistor
R5, 6 = 10 Ω 1/2 W Resistor
R7 = 100 Ω 1/4 W Resistor
RFC1 = 9 Ferroxcube Beads on #18 AWG Wire
D1 = 1N4001
D2 = 1N4997
Q1, Q2 = 2N4401
Q3, 4 = MRF454
T1, T2 = 16:1 Transformers
C20 = 910 pF Dipped Mica
C21 = 1100 pF Dipped Mica
C10 = 24 pF Dipped Mica
C22 = 500 μF 3 Vdc Electrolytic
K1 = Potter & Brumfield KT11A 12 Vdc Relay or Equivalent

FIGURE 4—Schematic Diagram



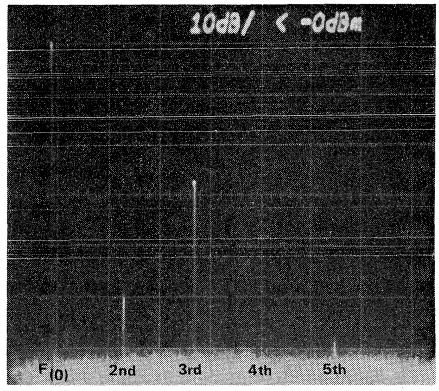
Amplitude Modulated Waveform with Superimposed Carrier. Carrier Conditions: f = 30 MHz; P_{in} = 2.2 Watts; P_{out} = 100 Watts (carrier); V_{CC} = 13.6 Vdc

FIGURE 5



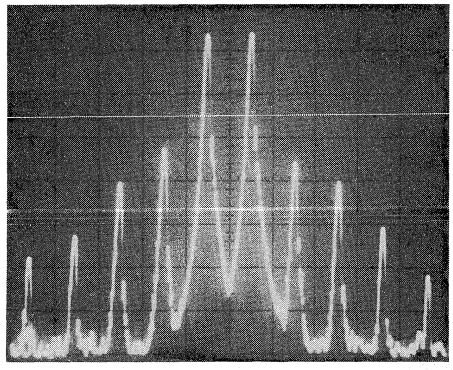
Amplitude Modulated Waveform with Superimposed Carrier. Carrier Conditions: f = 30 MHz; P_{in} = 1.3 Watt; P_{out} = 50 Watts; V_{CC} = 13.6 Vdc

FIGURE 6



Frequency Spectrum, 30 MHz ($F_{(0)}$, 2nd, 3rd, and 5th harmonics are visible). Vertical resolution: 10 dB/div. Horizontal 20MHz/div.

FIGURE 7



INTERMODULATION DISTORTION, 30, 30.001 MHz (3rd, 5th, 7th, 9th) order distortion products are visible. Vertical resolution: 10 dB/div. Horizontal: 1KHz/div.

FIGURE 8

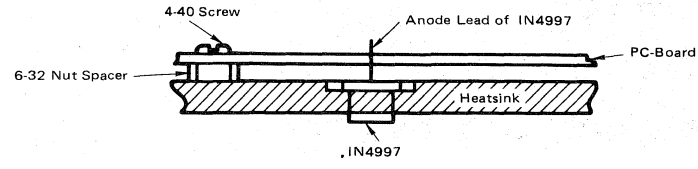
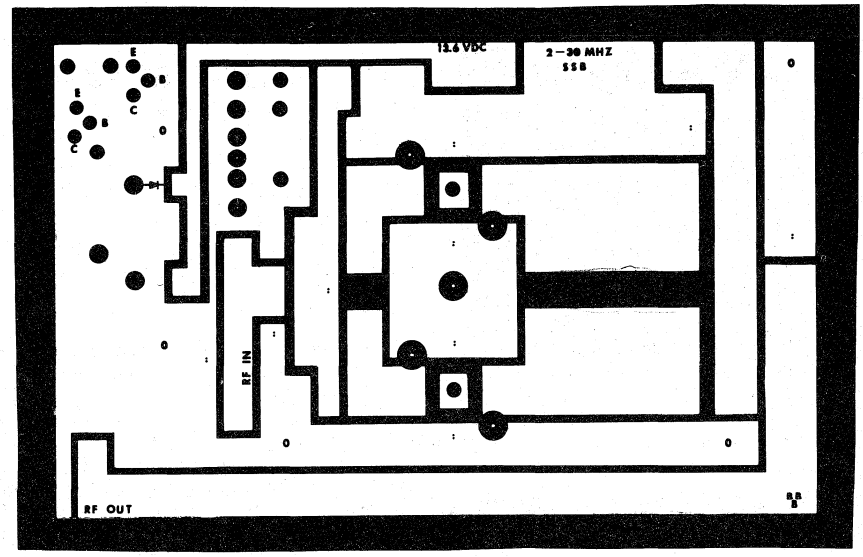


FIGURE 9 – Mounting Detail of IN4997 and 6-32 Nut (Spacer)

6



NOTE: The Printed Circuit Board shown is 75% of the original.

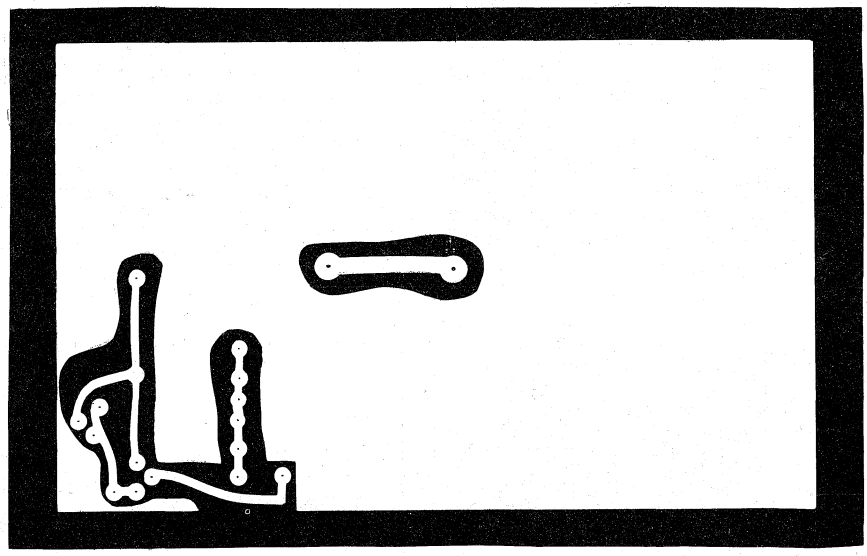


FIGURE 10– Photomaster (Positive)

Note: The use of this amplifier is illegal for Class D Citizen Band service.

A 10 WATT 225–400 MHz AMPLIFIER — MRF331

Prepared by
Dave Hollander
RF Power Engineering

This bulletin describes a broadband amplifier covering the 225–400 MHz military communications band producing 10 watt RF output power and operating from a 28 volt supply. The amplifier can be used as a driver for higher power devices such as 2N6439 and MRF327. Typical performance curves are shown in Figures 5, 6, and 7.

Circuit Description

The circuit is designed to be driven by a 50 ohm source and operate into a nominal 50 ohm load. The input matching network[1] consists of a π-section composed of C3, C4, Z2, C5 and C6. C2 is a dc blocking capacitor, and T1 is a 4:1 impedance ratio coaxial transformer. Z1 is a 50 ohm transmission line. A compensation network consisting of R1, C1, and L1 is used to improve the input VSWR and flatten the gain response of the amplifier. L2 and a small ferrite bead make up the base bias choke.

The output network is made up of a microstrip L-section consisting of Z3 and C7, and a high pass section consisting of C8 and L3. C8 also serves as a dc blocking capacitor.

Collector decoupling is accomplished through the use of L4, L5, C9, C10, C11, C12, and C13.

Construction

The circuit is constructed on a 3.375 X 2.5 inch (8.57 X 6.35 cm) double sided PC board. Board material is 3M Glass Teflon,* with a thickness of 0.031 inch (0.0787 cm). Glass Teflon was selected for its low loss and dielectric consistency. Figure 2 is a 1:1 scale photomaster print of the top side of the board. Eyelets are placed at the points marked by plus signs. The eyelets are soldered to both sides of the PCB to control ground current return paths. The edges of the transistor mounting hole beneath the emitter leads are also wrapped, using copper foil soldered in place to insure a solid emitter ground.[2,3] Due to a ground imbalance caused by the transformer, a component placement layout of the RF circuitry is shown in Figure 1. It is important that this layout is followed in order to duplicate performance. Construction details of the 4:1 transformer are shown in Figure 4.

*Registered Trademark of Dupont

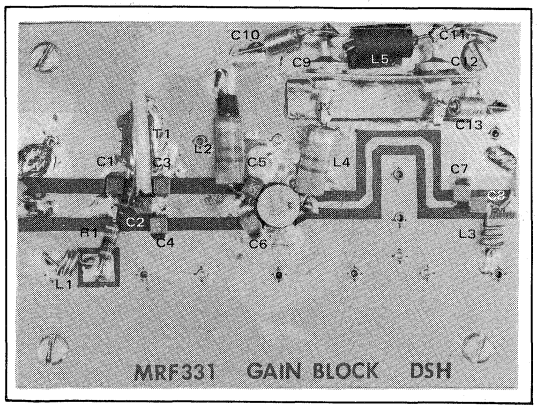
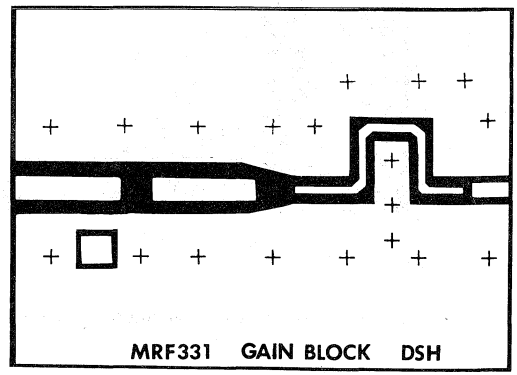
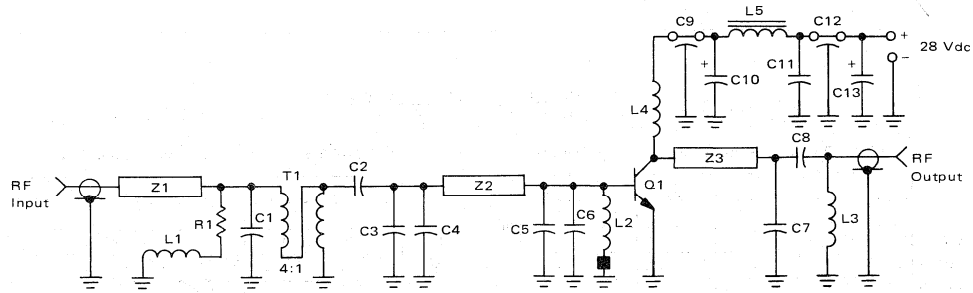


FIGURE 1 — Component Layout of the Amplifier



NOTE: The Printed Circuit Board shown is 75% of the original.

FIGURE 2 — Printed Circuit Board Layout



C1 – 8.2 pF Chip*
C2 – 270 pF Chip*
C3 – 36 pF Chip*
C4, C7 – 15 pF Chip*
C5, C6 – 50 pF Chip*
C8 – 82 pF Chip*
C9, C12 – 680 pF Feedthru
C10, C13 – 1.0 μF 50 V Tantalum
C11 – 0.1 μF Erie Redcap

L1, L3 – 3 Turns #22 AWG 1/8" (3.175 mm) ID
L2 – 0.15 μH Molded Choke
L4 – 0.15 μH Molded Choke with Ferroxcube Bead (Ferroxcube 56 590 65/4B on Ground End of Choke)
L5 – Ferroxcube VK200-19/4B

*100 mil A.C.I. Chip Capacitors

R1 – 36 Ω 1/4 Watt

T1 – 25 Ω Subminiature Coax (Type UT34-25) – 1.75 inches (44.45 mm) long

Z1 – Microstrip Line
720 mils L X 162 mils W
18.29 mm L X 4.115 mm W

Z2 – Microstrip Line
680 mils L X 162 mils W
17.27 mm L X 4.115 mm W

Z3 – Microstrip Line
2200 mils L X 50 mils W
55.88 mm L X 1.27 mm W

Board – 0.0625" (1.588 mm) Glass Teflon, $\epsilon_r = 2.56$

Q1 – MRF331

FIGURE 3 – Schematic Diagram and Component List

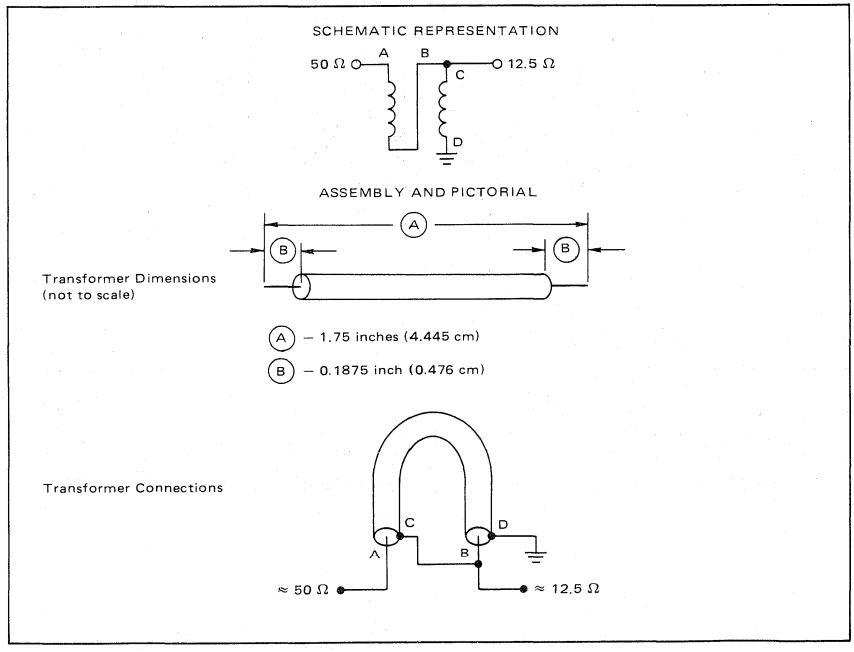


FIGURE 4 – Construction Details of 4:1 Impedance Ratio Transformer

6

AMPLIFIER PERFORMANCE

FIGURE 5 – Power Gain and Efficiency versus Frequency

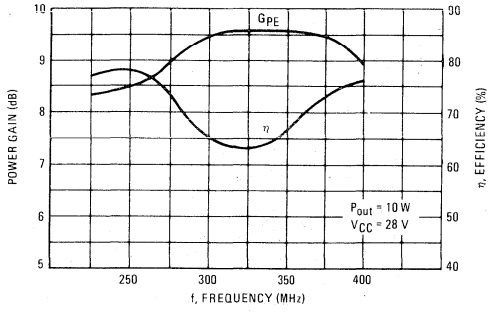


FIGURE 6 – Output Power versus Input Power

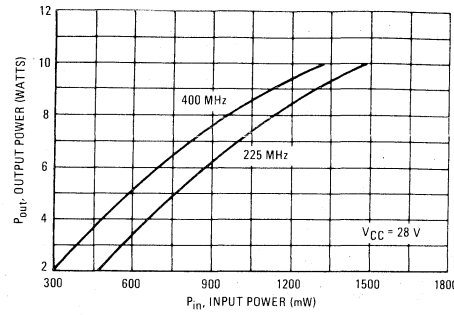
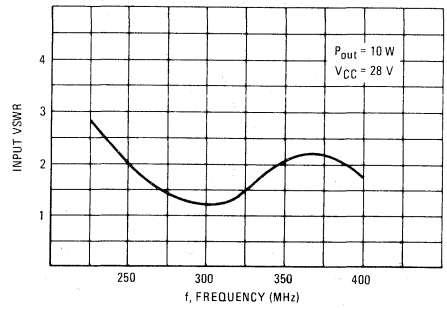


FIGURE 7 – Input VSWR versus Frequency



6

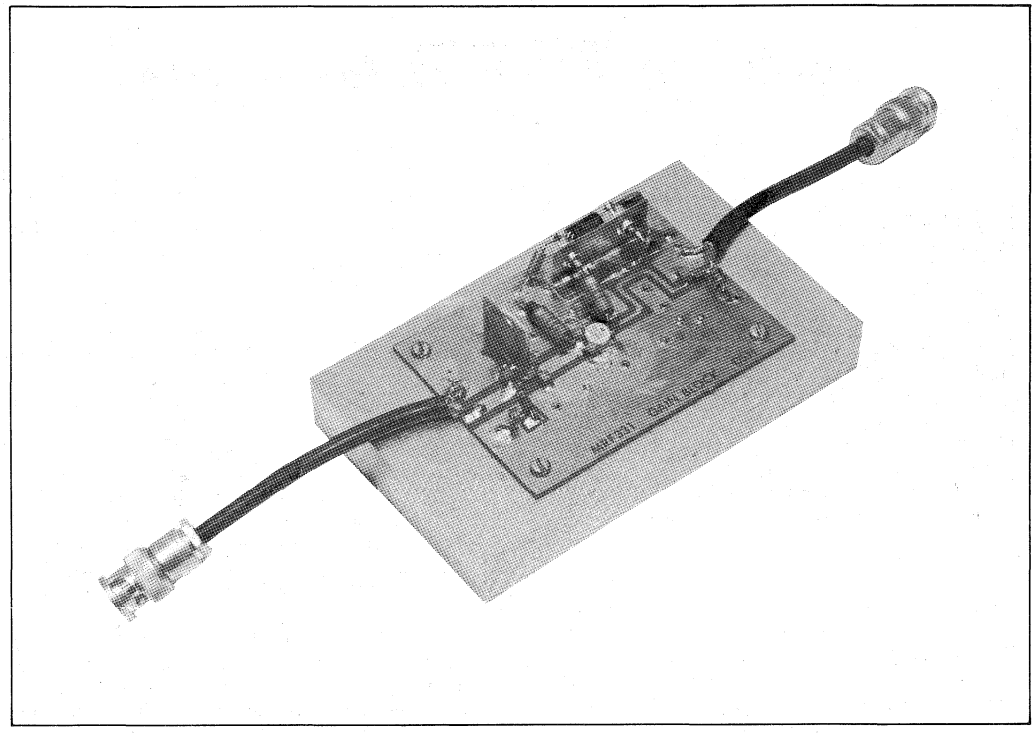


FIGURE 8 — Amplifier Assembly

References

1. Roy Hejhall, "Systemizing RF Power Amplifier Design," Motorola Application Note AN-282A, Motorola Semiconductor Products Inc., Phoenix, Arizona.
2. "Mounting Stripline – Opposed Emitter (SOE) Transistors," Motorola Application Note AN-555, Motorola Semiconductor Products Inc., Phoenix, Arizona.
3. Glenn Young, "Microstrip Design Techniques for UHF Amplifiers," Motorola Application Note AN-548A, Motorola Semiconductor Products Inc., Phoenix, Arizona.

A 60-WATT 225–400 MHz AMPLIFIER — 2N6439

Prepared by
Dave Hollander

This bulletin describes a 60 watt, 28 volt broadband amplifier covering the 225–400 MHz military communications band. The amplifier may be used singly as a 60 watt output stage in a 225–400 MHz transmitter, or by using two of these amplifiers combined with quadrature couplers, a 100 watt output amplifier stage may be constructed. Typical performance curves of gain, efficiency, and input SWR are shown in Figures 5, 6, and 7.

Circuit Description

This circuit is designed to be driven from a 50 ohm source and work into a nominal 50 ohm load. The input network consists of two microstrip L-sections composed of Z1, Z2 and C2 through C6. C1 serves as a dc blocking capacitor. A 4:1 impedance ratio coaxial transformer T1 completes the input matching network. L1 and ferrite bead serve as a base decoupling choke.

The output circuit consists of shunt inductor L2 at the collector, followed by two microstrip L-sections composed of Z3, Z4 and C8 through C11. C12 serves as a dc blocking capacitor, and is followed by another 4:1 impedance ratio coaxial transformer.

Collector decoupling is accomplished through the use of L3, L4, C14 through C16 and R1.

Construction

The circuit is constructed on a 3.375 × 2.5 inch (8.57 × 6.35 cm) double sided PC board. Board material is 3M Glass Teflon*, with a thickness of 0.031 inch (0.0787 cm). Glass Teflon was selected for its low loss and dielectric consistency. Figure 2 is a photomaster print of the top side of the board. Eyelets are placed at the points marked by a plus sign to carry the top ground to the bottom side ground return. The edges of the transistor mounting hole beneath the emitter leads are also wrapped, using copper foil soldered in place to insure a solid emitter ground.[1,2] Construction details of the 4:1 transformers are shown in Figure 4.

*Registered Trademark of DuPont

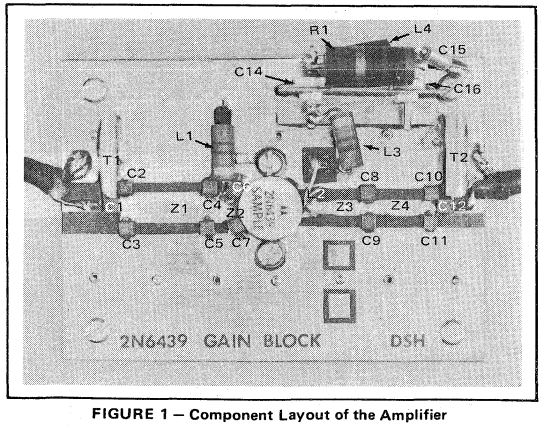
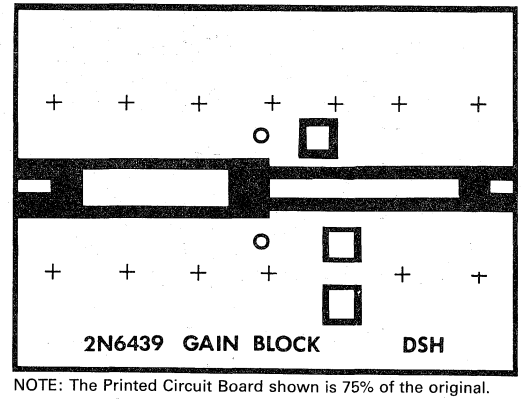
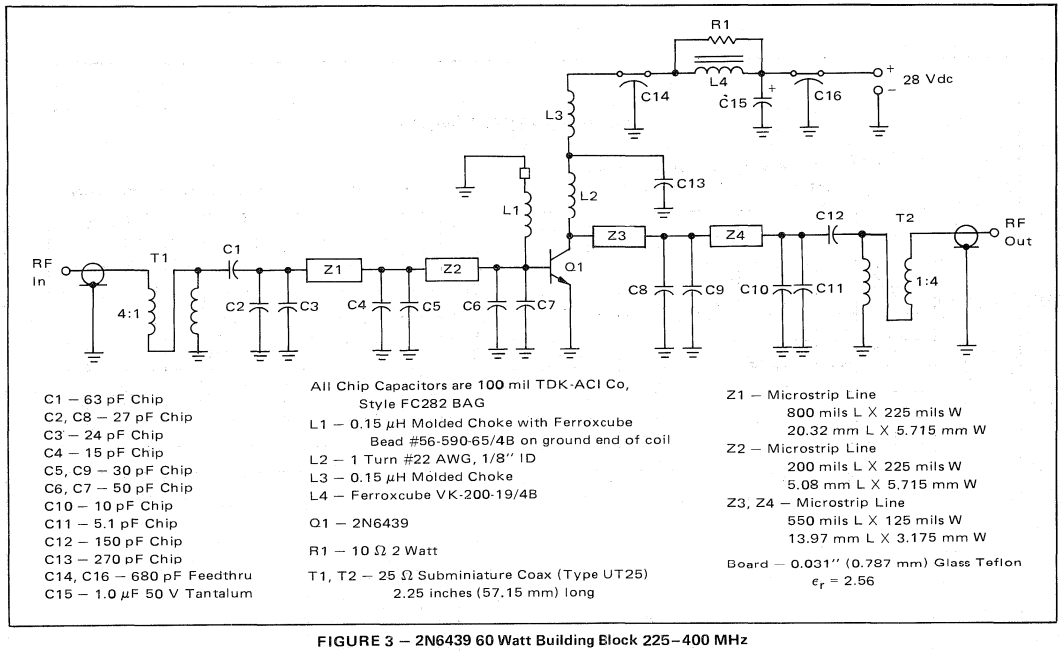


FIGURE 1 — Component Layout of the Amplifier



NOTE: The Printed Circuit Board shown is 75% of the original.

FIGURE 2 — Photomaster of Circuit Board



C1 – 63 pF Chip
C2, C8 – 27 pF Chip
C3 – 24 pF Chip
C4 – 15 pF Chip
C5, C9 – 30 pF Chip
C6, C7 – 50 pF Chip
C10 – 10 pF Chip
C11 – 5.1 pF Chip
C12 – 150 pF Chip
C13 – 270 pF Chip
C14, C16 – 680 pF Feedthru
C15 – 1.0 μF 50 V Tantalum

All Chip Capacitors are 100 mil TDK-ACI Co, Style FC282 BAG
L1 – 0.15 μH Molded Choke with Ferroxcube Bead #56-590-65/4B on ground end of coil
L2 – 1 Turn #22 AWG, 1/8" ID
L3 – 0.15 μH Molded Choke
L4 – Ferroxcube VK-200-19/4B

Q1 – 2N6439

R1 – 10 Ω 2 Watt

T1, T2 – 25 Ω Subminiature Coax (Type UT25) 2.25 inches (57.15 mm) long

Z1 – Microstrip Line
800 mils L X 225 mils W
20.32 mm L X 5.715 mm W
Z2 – Microstrip Line
200 mils L X 225 mils W
5.08 mm L X 5.715 mm W
Z3, Z4 – Microstrip Line
550 mils L X 125 mils W
13.97 mm L X 3.175 mm W

Board – 0.031" (0.787 mm) Glass Teflon
ϵ_r = 2.56

FIGURE 3 – 2N6439 60 Watt Building Block 225–400 MHz

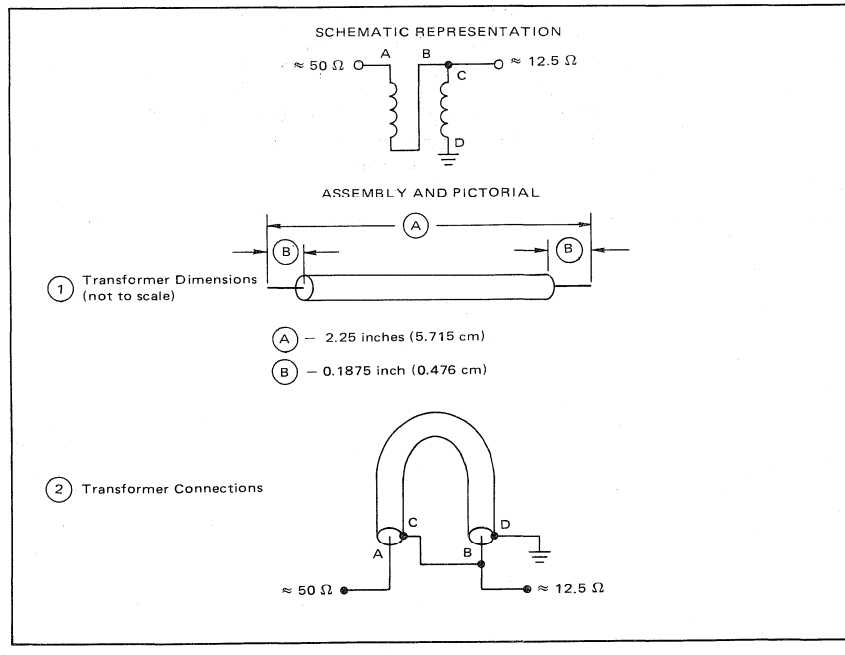


FIGURE 4 – Construction Details of the 4:1 Unbalanced to Unbalanced Transformers

AMPLIFIER PERFORMANCE

FIGURE 5 – Power Gain versus Frequency
Efficiency versus Frequency

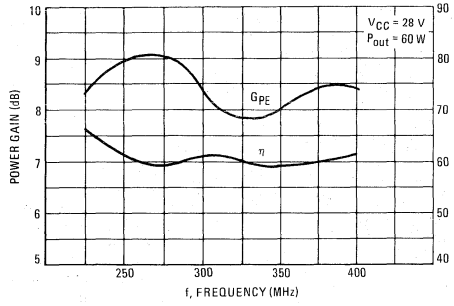


FIGURE 6 – Output Power versus Input Power

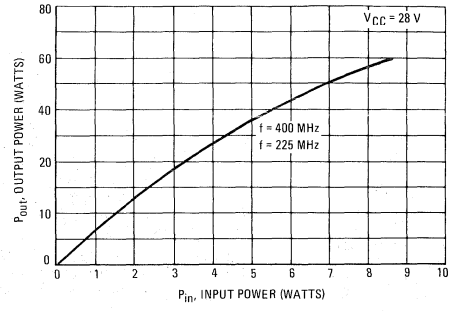
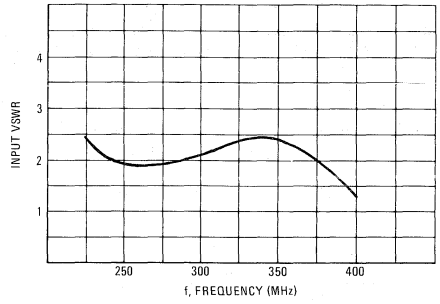


FIGURE 7 – Input VSWR versus Frequency



6

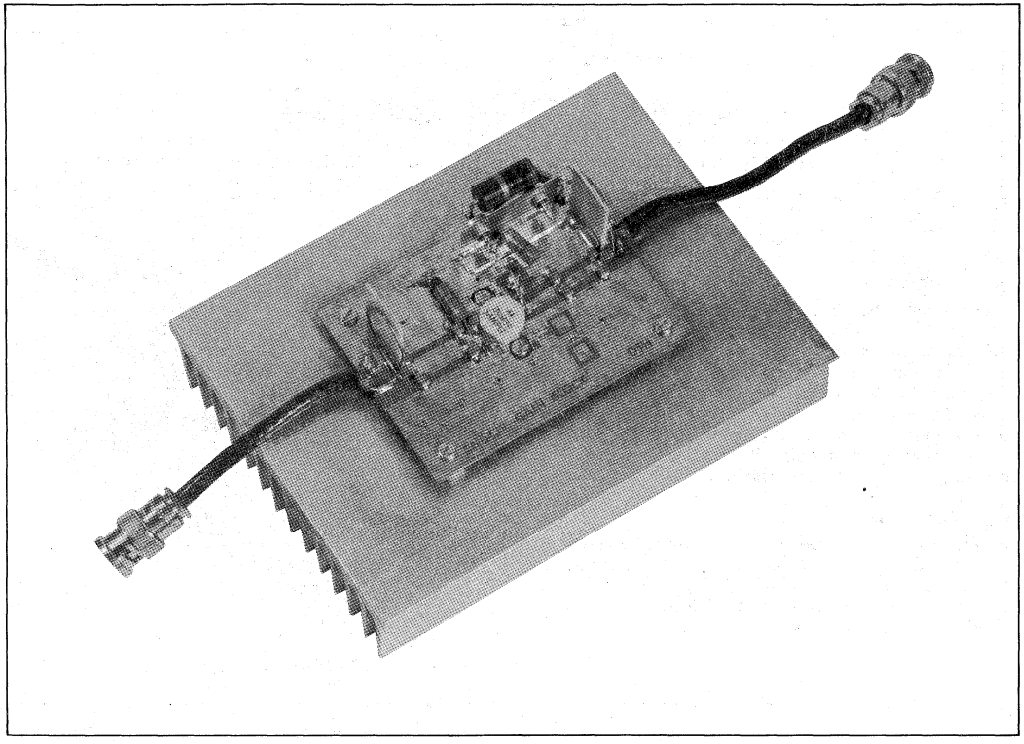


FIGURE 8 – Amplifier Assembly

Bibliography

1. "Mounting Stripline – Opposed Emitter (SOE) Transistors," Motorola Application Note AN-555, Motorola Semiconductor Products Inc., Phoenix, Arizona.

2. Glenn Young, "Microstrip Design Techniques for UHF Amplifiers," Motorola Application Note AN-548A, Motorola Semiconductor Products Inc., Phoenix, Arizona.

3. Roy Hejhall, "Systemizing RF Power Amplifier Design," Motorola Application Note AN-282A, Motorola Semiconductor Products Inc., Phoenix, Arizona.

NOTE: A 10 Watt 225–400 MHz Amplifier–MRF331 is described in Engineering Bulletin EB-74.

A 1-WATT, 2.3 GHz AMPLIFIER

Prepared by
Mike Miceli

Introduction

Simplicity and repeatability are featured in this 1-watt S-band amplifier design. The design uses an MRF2001 transistor as a common base, Class C amplifier. The amplifier delivers 1-watt output with 8 dB minimum gain at 24 V, and is tunable from 2.25 to 2.35 GHz. Applications include microwave communications equipment and other systems requiring medium power, narrow band amplification. A photograph of the amplifier is shown in Figure 1.

Circuit Description

The amplifier circuitry consists almost entirely of distributed microstrip elements. A total of six additional components, including the MRF2001, are required to build a working amplifier. Refer to Figure 2 for the schematic diagram of the amplifier.

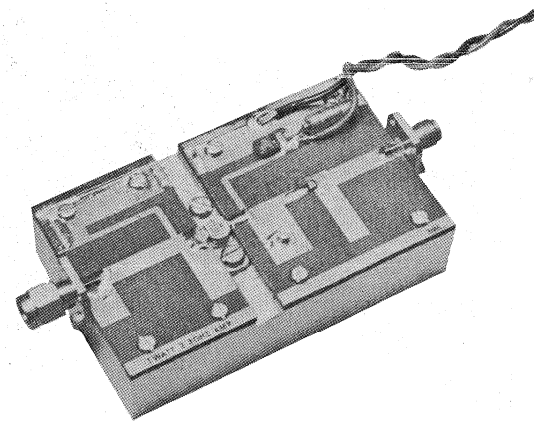
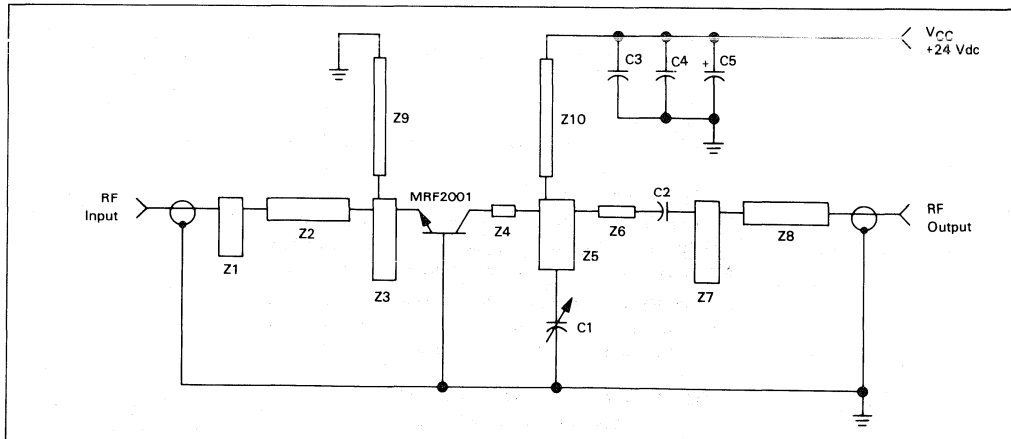


FIGURE 1 — 1-W, 2.3 GHz Amplifier

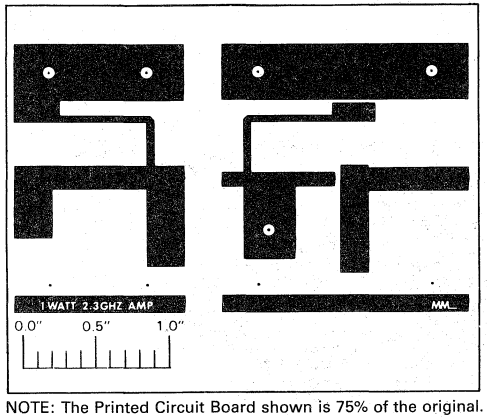


C1 — 0.4-2.5 pF Johanson 7285*
C2, C3 — 68 pF, 50 mil ATC**
C4 — 0.1 μF, 50 V
C5 — 4.7 μF, 50 V Tantalum
Z1-Z10 — Microstrip; see Photomaster, Figure 3

Board Material — 0.0625" 3M Glass Teflon,***
$\epsilon_r = 2.5 \pm 0.05$
*Johanson Manufacturing Corp., 400 Rockaway Valley Road, Boonton, NJ 07005
**American Technical Ceramics, One Norden Lane, Huntington Station, NY 11746
***Registered Trademark of Du Pont

FIGURE 2 — Schematic Diagram

The input and output impedances of the transistor are matched to 50 ohms by double section low pass networks. The networks are designed to provide about 3% 1 dB power bandwidth while maintaining a collector efficiency of approximately 30%. There is one tuning adjustment in the amplifier — C1 in the output network. Ceramic chip capacitors, C2 and C3, are used for DC blocking and power supply decoupling. Additional low frequency decoupling is provided by capacitors C4 and C5. Refer to Figure 3 for a 1:1 photomaster of the circuit boards.



NOTE: The Printed Circuit Board shown is 75% of the original.

FIGURE 3 — Circuit Photomaster

Amplifier Assembly

The circuit boards are mounted on a 3.125″ × 1.875″ × 0.750″ aluminum block. A 0.062″ deep and 0.260″ wide slot is milled in the heat sink as shown in Figure 4.

The transistor mounts in the slot with two 4-40 screws. An alternate approach that would eliminate the need for milling is the laminated structure shown in Figure 5.

Using the laminated assembly, the transistor is mounted on the surface of the block and 0.062″ aluminum shim stock is sandwiched between the block and the circuit boards. Connector mounting plates are required if SMA type connectors are used for the RF input and output. The SMA connectors can be fastened directly to the block if the milled approach is used. Either method results in the same performance for this 1-watt design. The laminated structure, however, may not be suitable for higher power designs. With higher power levels the transistor impedances are lower. The RF ground impedance through the laminated metal may be sufficiently high to impair gain and stability. This point emphasizes the fact that the successful design of RF amplifiers is dependent not only on attention to electrical considerations, but to the physical construction as well. While construction related parasitics cannot be totally ignored at medium frequencies, they can pose serious problems at microwave frequencies. It is recommended that the following construction techniques be followed when building this amplifier. Refer to Figure 6 for the component placement diagram.

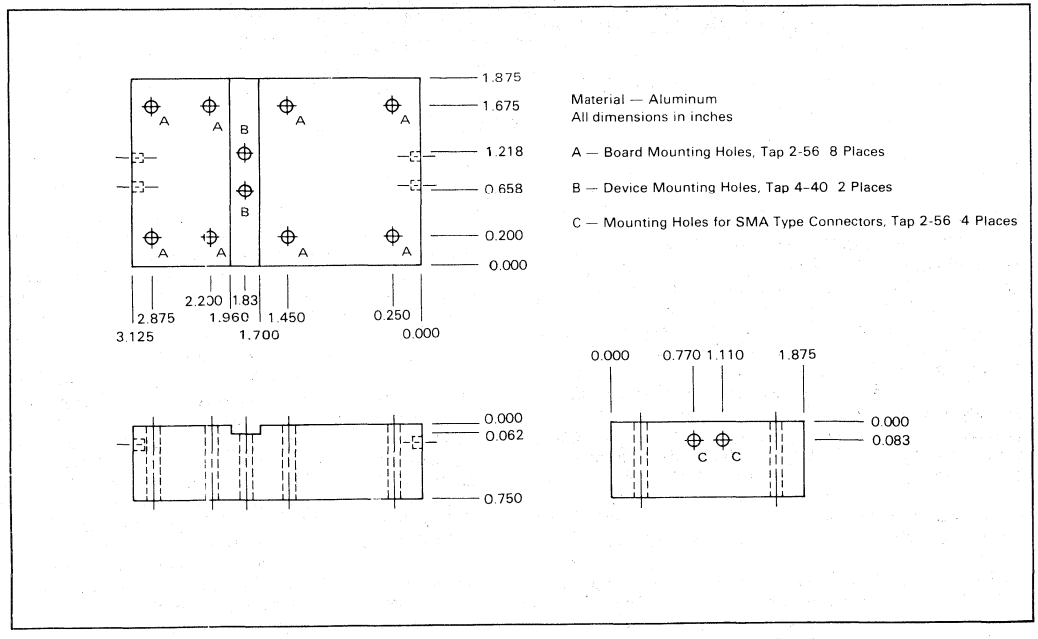


FIGURE 4 — Amplifier Heat Sink

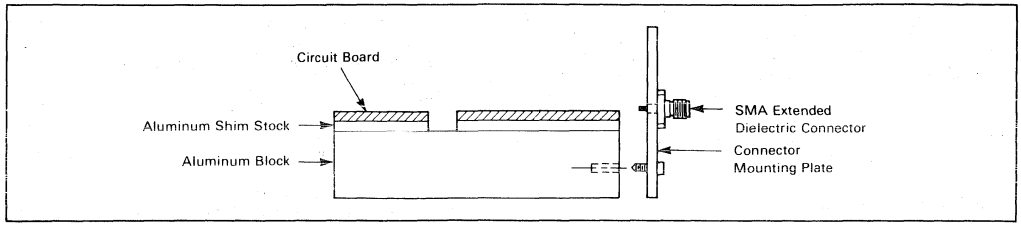
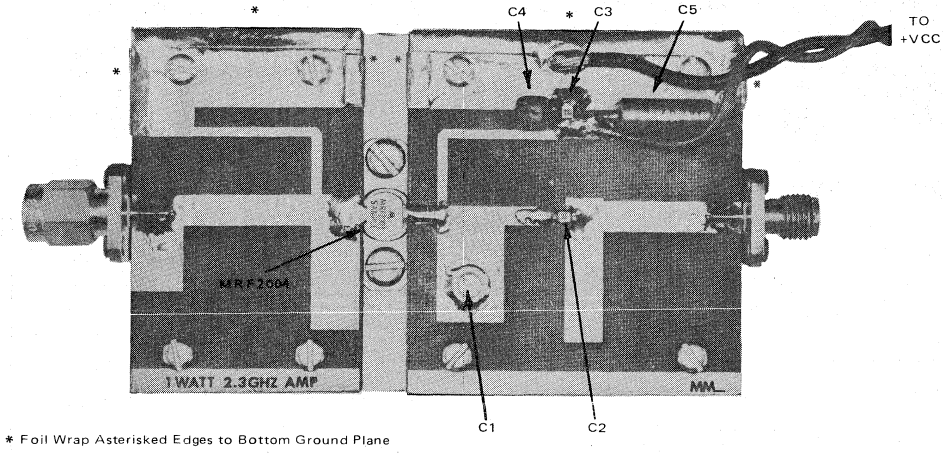


FIGURE 5 — Laminated Assembly



* Foil Wrap Asterisked Edges to Bottom Ground Plane

FIGURE 6 — Assembly Diagram

Construction Notes

1. The transistor is fastened to the heat sink with two 4-40 screws. The mounting surface should be flat and clean. Thermal compound should not be used on the underside of this device; the flange provides the transistor base connection and must make good electrical contact with the heat sink. The wide lead is the emitter and the narrow lead is the collector.

2. The edges of the boards marked with an asterisk (see Figure 6) must be foil wrapped to the bottom ground plane to provide a low impedance RF ground connection for C3, C4, C5 and the emitter choke, Z9. This is accomplished by soldering a 1/4″-wide strip of 1- to 5-mil thick copper foil to the top ground plane and then wrapping it around the edge of the board. The other edge of the foil is soldered to the bottom ground plane.

3. Use a #31 drill bit to drill the board mounting holes. With the transistor already mounted to the heat sink, slide the boards into position so they butt up against the transistor. This will insure that the excess lead inductance of the transistor is kept to a minimum. The boards can now be fastened to the heat sink and the remaining components mounted.

4. Use a minimum of heat when soldering C2 and C3. Excess heat could cause the end metal of the chip capacitor to separate from the ceramic.

5. C1 is a miniature variable capacitor whose high self-resonant frequency makes it ideal for use at microwave frequencies. The package design makes it very convenient to use wherever a shunt capacitive element is desired and is used here to vary the capacitance of microstrip stub, Z5. The capacitor is mounted by drilling a 0.120″ diameter hole (#31 drill bit) at the point indicated in Figure 6. Using the circuit board as a template, mark the point on the heat sink directly below the mounting hole. Since the capacitor is slightly longer than the thickness of the board, a clearance hole is needed at this point. The bottom of the capacitor is soldered to the ground plane on the bottom of the board. The flange of the capacitor is soldered to Z5. Avoid getting solder into the area above the flange as this will prevent the movement of the tuning piston.

FIGURE 7 — Performance Curves

Performance Data

Amplifier tune-up is accomplished by adjusting C1 for maximum output power with minimum collector current. The amplifier will tune from 2.25 to 2.35 GHz while maintaining an input VSWR of less than 2:1. Typical performance curves appear in Figure 7. Figures 7a and 7b show performance with the amplifier re-tuned for each frequency. Figure 7c shows performance without re-tuning. Note from Figure 7c that the instantaneous 1 dB bandwidth is approximately 70 MHz with the amplifier tuned to a center frequency of 2.3 GHz.

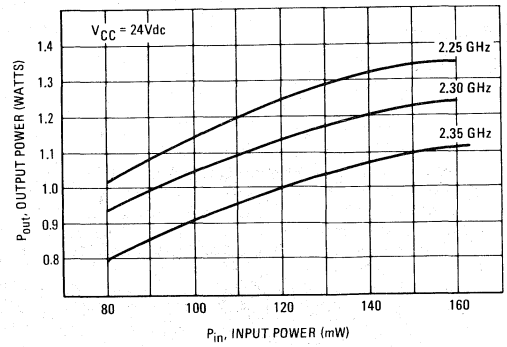


FIGURE 7a — Output Power versus Input Power

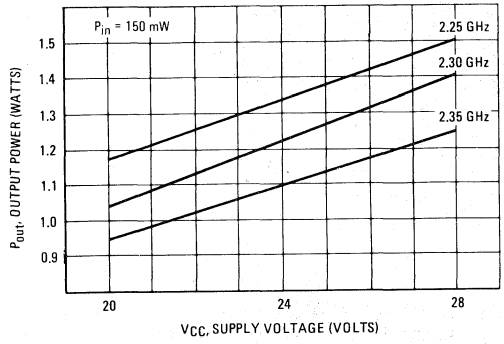


FIGURE 7b — Output Power versus Supply Voltage

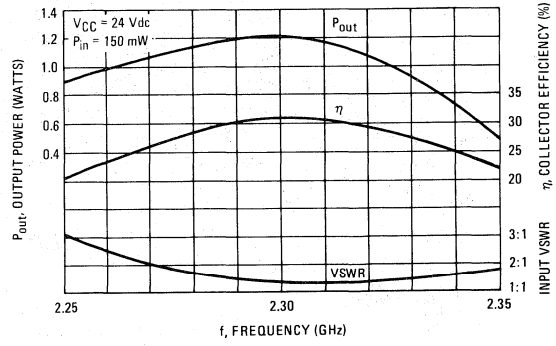


FIGURE 7c — Output Power, Efficiency and VSWR versus Frequency

NOTE: The MRF2001 is one of a family of 2 GHz power transistors with RF output powers as indicated below:

MRF2001 1 W	MRF2005 5 W
MRF2003 3 W	MRF2010 10 W

LOW-COST VHF AMPLIFIER HAS BROADBAND PERFORMANCE

Prepared by
Ken Dufour

Introduction

This bulletin presents two VHF amplifier designs intended for FM or CW service in the 136–174 MHz band. Both amplifiers feature the Motorola MRF260 and MRF262 plastic encased VHF transitors which are rated at 5.0 W and 15 W power output respectively. This new series is derived from a line of highly successful device types of similar capability, but packaged in a standard configuration, (i.e., stripline packages). The MRF260 and MRF262 are in a standard TO-220 silicone epoxy case with the emitter wired to the metal tab and center lead of the device. This common emitter configuration results in good RF performance, improved thermal conductivity, and ease of mounting in an RF amplifier, by connecting the transistor mounting flange to RF and DC ground.

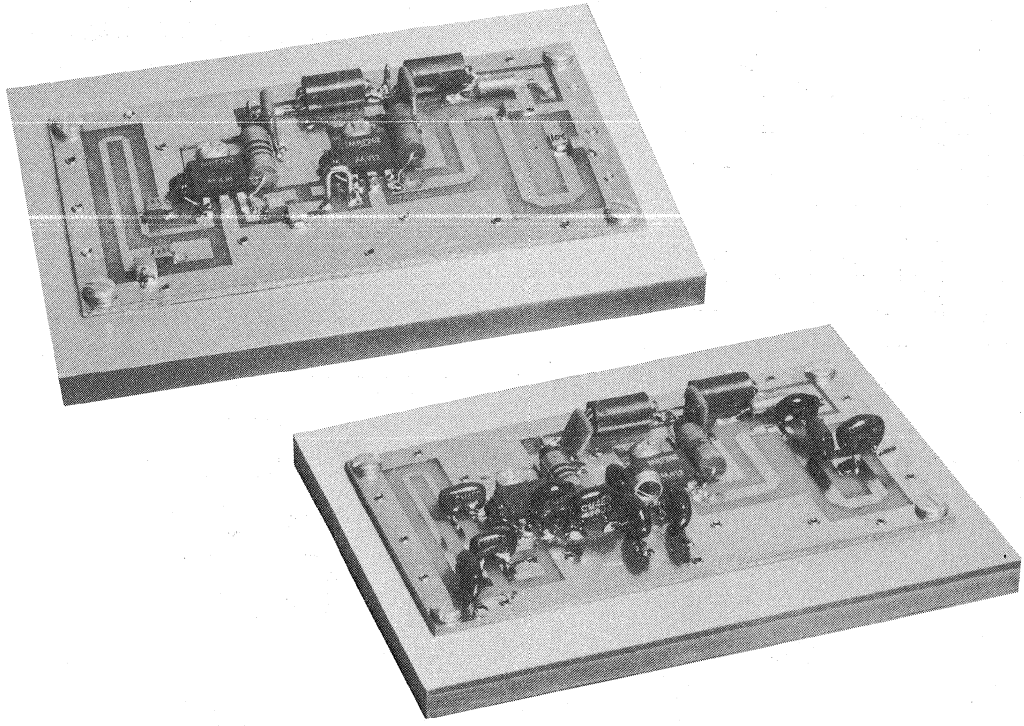


FIGURE 1 — Engineering Models. A Common Board Layout is Used for Both Versions

References

1. Hatchett, John: 25 Watt and 10 Watt VHF Marine Band Transmitters, AN-595, Motorola Semiconductor Products, Inc.
2. Granberg, H: A Simplified Approach to VHF Power Amplifier Design, AN-791, Motorola Semiconductor Products, Inc.
3. Hollander, D: A 15 Watt AM Aircraft Transmitter Power Amplifier Using Low Cost Plastic Transistors, AN-793, Motorola Semiconductor Products, Inc.

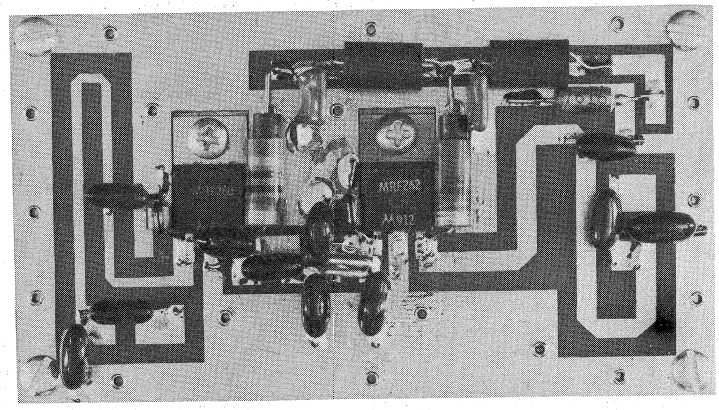


FIGURE 2 — 136-160 MHz Amplifier

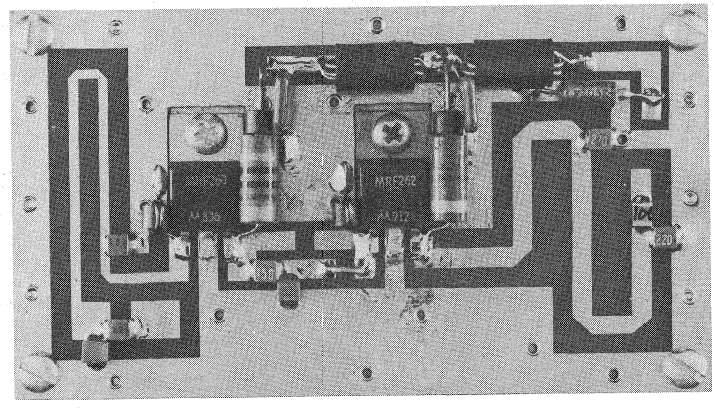


FIGURE 3 — 160-174 MHz Amplifier

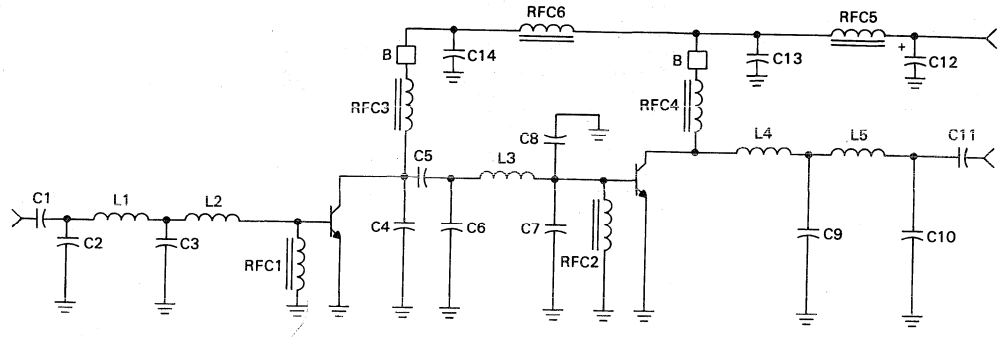
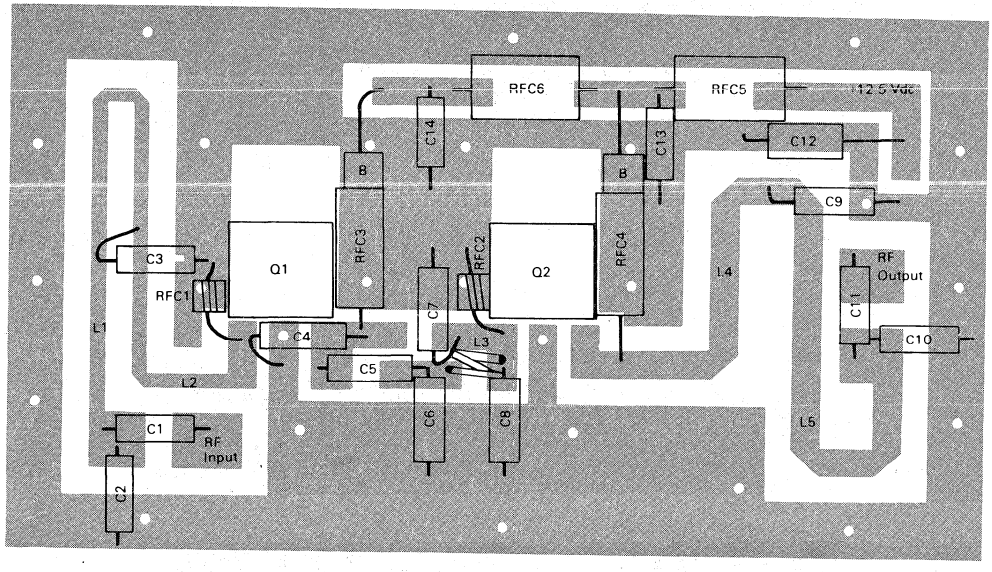


FIGURE 4 — Schematic Diagram of Dipped Silvered Mica Capacitor Version (136-160 MHz)



C2 — 33 pF
C3 — 47 pF
C4 — 18 pF
C5, C8 — 43 pF
C6 — 12 pF
C7, C9 — 50 pF

C11 — 100 pF
C12 — 1.0 μF Tantalum
C13, C14 — 0.05 μF Erie Redcap
L1-L5 — Printed Inductor
L3 — 1.25" #18 AWG, 1-1/2 Turns, 9/64 ID
Q1 — MRF260

RFC1, RFC2 — 2 Turns #26 Enameled on Ferrite Bead Ferroxcube 56-590-65/3B
RFC3 — 10 μH Molded Choke
RFC4 — 0.15 μH Molded Choke
RFC5, RFC6 — VK200-4B
B — Bead, Ferroxcube 56-590-65/3B

FIGURE 5 — Component Placement, 136-160 MHz Amplifier

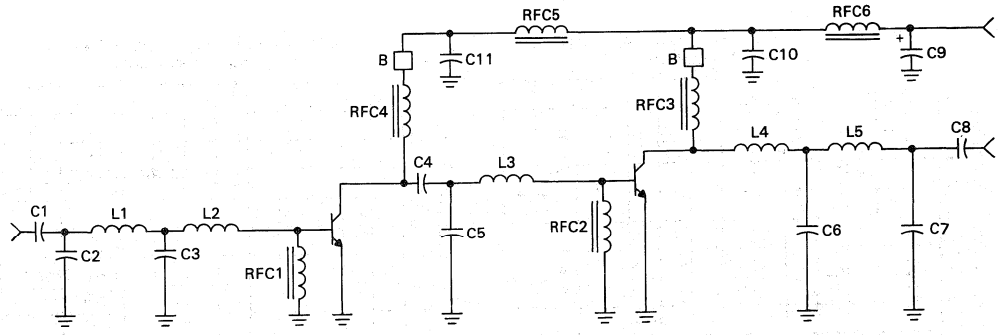
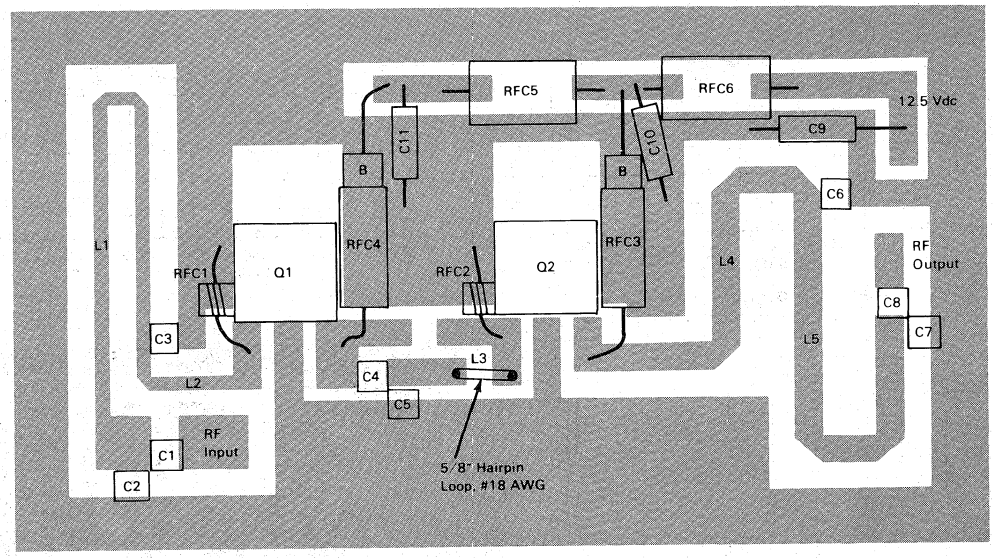


FIGURE 6 — Schematic Diagram of Chip Capacitor Version (160-174 MHz)



C1 — 220 pF, TDK 100 mil Chip Capacitor
C2 — 43 pF, TDK 100 mil Chip Capacitor
C3 — 150 pF, TDK 100 mil Chip Capacitor
C4 — 15 pF, TDK 100 mil Chip Capacitor
C5 — 63 pF, TDK 100 mil Chip Capacitor
C6 — 27 pF, TDK 100 mil Chip Capacitor
C7 — 22 pF, TDK 100 mil Chip Capacitor
C8 — 100 pF, TDK 100 mil Chip Capacitor
C9 — 1.0 μF Tantalum
C10 — 0.1 μF Erie Redcap, 100 V General Purpose
C11 — 0.05 μF Erie Redcap, 100 V General Purpose

L1-L5 — Printed Inductor
L3 — 5/8" #18 AWG Wire formed into hairpin loop
Q1 — MRF260
Q2 — MRF262
RFC1, RFC2 — 2 Turns #26 Enameled Wire through Ferrite Bead Ferroxcube 56-590-65/3B
RFC3 — 0.15 μH Molded Choke
RFC4 — 10 μH Molded Choke
RFC5, RFC6 — VK200-4B
B — Bead, Ferroxcube 56-590-65/3B

FIGURE 7 — Component Placement, 160-174 MHz Amplifier

FIGURE 8 — Power Output versus Frequency, 136-160 MHz Amplifier

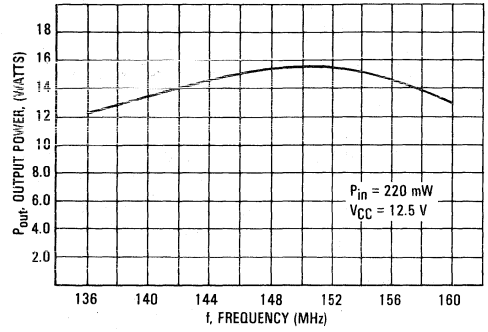


FIGURE 9 — Power Output versus Frequency, 160-174 MHz Amplifier

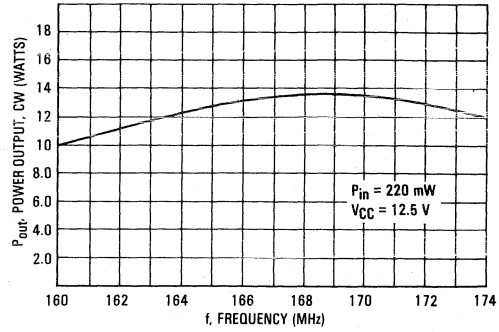


FIGURE 10 — Power Gain and Input VSWR versus Frequency, 136-160 MHz Amplifier

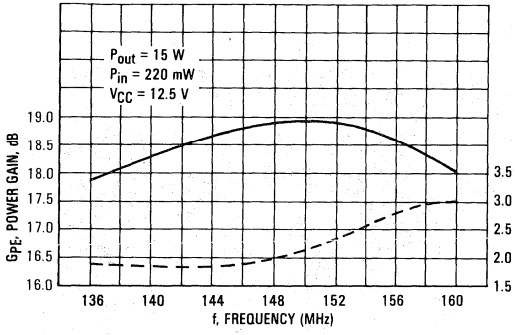


FIGURE 11 — Power Gain and Input VSWR, versus Frequency, 160-174 MHz Amplifier

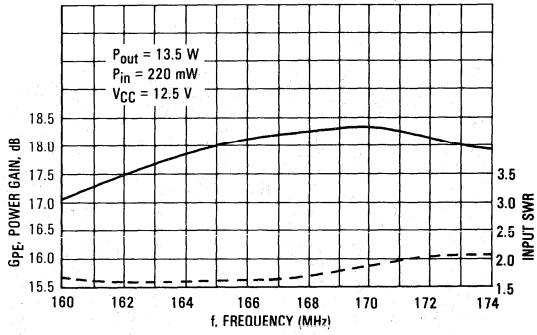


FIGURE 12 — Output Spectrum 136-160 MHz Model

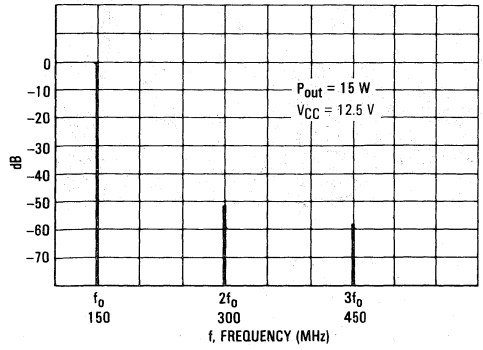
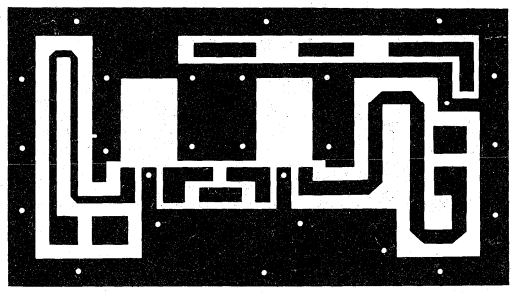


FIGURE 13 — PCB Photomaster



Note: Grounding eyelet locations are indicated by dots.

The Printed Circuit Board shown is 75% of the original.

Design Considerations

The lower frequencies (136–160 MHz) are serviced by a design utilizing low-cost dipped silver mica capacitors. For a broadband response in the higher frequencies; (160–174 MHz), low inductance, ceramic chip capacitors are used.

Ease of assembly, repeatability and fast economical construction received the utmost consideration in the design of this amplifier. TO-220 devices result in a low profile circuit which minimizes the volume occupied by the amplifier. Additionally, the MRF262 transistor used in the output stage is a rugged device, able to tolerate high load SWR conditions. Maximum use of printed inductors assures good repeatability.

Both amplifiers utilize stagger tuned networks to enhance bandwidth. Additionally, each design retains excellent gain and stability characteristics when narrow banded. All of these merits are attributed to optimum device gain and the reasonably high inter-stage impedance levels incurred at these power levels.

Circuit Description

The amplifier has two stages and uses 5.0 W and 15 W rated transistors to accomplish the desired gain and power output. Two stage transmission line Chebyshev networks accomplish coupling and impedance transformation at the input and output. Nominal impedance levels are 50 ohms, while the interstage network transforms device impedances directly. Values for the reactive elements of these networks were almost entirely generated by computer aided design. Although the interstage network is straight forward in design, it required some modification and refinement of computer generated values to achieve the final results and accomodate available component values.

Construction

The amplifier is assembled on double-sided G-10 fiberglass board with 1 oz. copper cladding. The format is 2.0″ × 3.5″ and a photomask is provided (Figure 13). Some method of electrically connecting the upper and lower ground plane is required. Eyelets or plated through holes are recommended, but alternative measures such as short pieces of wire soldered to both planes can be used successfully. Failure to provide an adequate or consistent ground plane may result in poor RF performance, instability, and unpredictable tuning. The reverse side of the board retains all copper and forms the ground plane. Component placement and the recommended position of grounding eyelets is shown in Figures 13, 5, and 7. All component leads are positioned and soldered above the board. There are no through connections other than grounding points. This facilitates component positioning, replacement, and accessability. The transistors are fitted into a 0.4″ by 0.65″ opening in the board and are installed directly against the heat sink. A coating of heat sink compound such as Dow Corning 340 between each device and the heat sink improves thermal contact and helps prevent power slump.

At frequencies beyond 100 MHz, dipped silver mica capacitors generally become inductive, and do so with a high degree of unpredictability. This phenomenon is also dependent upon component value and becomes more pronounced with an increase in frequency. (Ref: 1, 2, 3). To maintain predictable performance beyond 160 MHz, a second layout featuring ceramic chip capacitors is offered (Figure 3, 6, 7). The design of these capacitors allows them to remain capacitive beyond the VHF frequencies. Maintaining the bandwidth of 160–174 MHz with this circuit board, the networks become lossy and power output suffers slightly. Variable capacitors may make this condition more tolerable and can be installed in the input and interstage networks. In some cases the ease of adjustment and added flexibility would justify the added cost of the variable capacitors.

Performance

Normally, this amplifier will not require tuning provided that components are as described and are positioned as shown on Figure 5 and 7. If an accurate method of measuring power is available, a quick check of amplifier performance can be accomplished by comparing its parameters with the performance data of Figures 8 through 11. Drive must be maintained at 220 mW (±20 mW) and V_{CC} held to 12.5 Vdc to accurately reproduce the overall response noted here. Allow some degree of tolerance (10%) in output power to account for differences inherent in component values and transistor performance. To assure broadband performance and tailored frequency response, the amplifier should be checked using a swept frequency generator capable of 200–300 mW output. Tuning for maximum power out and minimum reflected power at band centers will not necessarily provide a broadband response. Figures 8 through 11 graphically depict typical levels of performance achieved with this amplifier. Either version is stable into higher than 3:1 VSWR load mismatch at all phase angles. The output device is tolerant of short term operation into an open or short circuit load at full drive.

Harmonic content of a 150 MHz signal at the output of the dipped silver mica version is illustrated in Figure 12. The 2nd harmonic is approximately -50 dB with respect to the fundamental. This level of performance cannot be maintained across the entire band, therefore, some additional filtering of the output signal will be required to meet more stringent requirements.

With the amplifier mounted on aluminum stock, 2.0″ × 8.5″ and 0.090″ thick, a 25% duty cycle (1 min on, 4 min off) produced a temperature of 50°C (122°F) after two hours of operation. A 50% duty cycle (1 min on, 1 min off) raised this temperature to 60°C (140°F) and full key down operation caused a stabilized temperature of 80°C (176°F). All temperatures were measured on the heat sink at the final device with output power maintained at 15 watts. One can safely assume that a panel on the outside edge (i.e., backside) of a transceiver could be successfully used as a heat sink for this amplifier.

60 WATT VHF AMPLIFIER USES SPLITTING/COMBINING TECHNIQUES

Prepared by
Ken Dufour
RF Product Group

Using proven combining techniques to obtain higher output power or added reliability at VHF can be accomplished with excellent results. Simple matching networks and power transistors featuring moderate gain capability can produce a level of performance comparable to that of a single-stage amplifier using a larger, more expensive device. Though not the ultimate answer in VHF amplifier design, the splitter/combiner method does have distinct advantages over designs that brute force the transistors into a parallel configuration. Current hogging and reduced impedance level problems associated with that technique are minimized. The exotic materials or expensive board layout required to produce a true push-pull design operating at VHF again makes combining techniques more appealing.

This 60 W amplifier operates from 150 to 175 MHz and features two, low-cost Motorola MRF264 transistors. These devices are designed for operation at VHF and individually produce 30 watts of rated output power and 6.0 dB of gain with a 12.5 volt supply. The amplifier design makes use of a modified Wilkinson combiner technique to produce 60 watts output with a drive level of 15 watts.

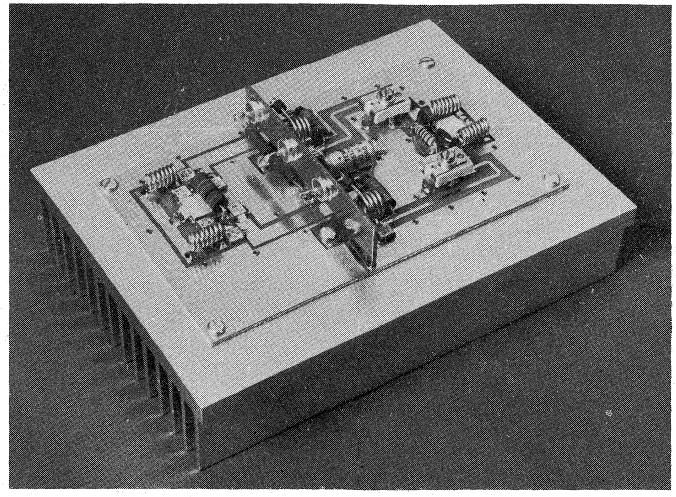


FIGURE 1 — Engineering Model

Design Considerations

Experimental work with 90° (quadrature) couplers proved unsuitable for this application. Generally, they are sensitive to mismatch and tend to create instability and loss of power when used in an amplifier. In-phase (Wilkinson) couplers provide an adequate solution to this problem. (Ref: 1) They are relatively insensitive to phase changes and offer good bandwidth characteristics.

Printed transmission lines for the frequency of interest can become somewhat cumbersome on standard circuit board material. Therefore, lumped reactances (L1, 2, 9, 10 and C1, 2, 3, 14, 15, 16, Figure 5) are used to simulate 70.7 ohm 1/4 wave transmission lines, the main element in the couplers. This approach not only conserves board space, but provides a means to compensate for small variations in associated component values.

Microstrip techniques are incorporated in the amplifier networks to balance RF performance and promote reproducibility. Because of the lower circulating currents and reduced component heating in the collector circuitry of low-powered stages, smaller capacitors can be used in the networks at that point than would be required for a single-ended 60 watt design. Separating the major heat producing devices to two areas on the heatsink produces a more even heat transfer to the ambient air. The combined amplifier presented here has good harmonic suppression (Figure 8). A low-pass filtering effect is noticeable with the Wilkinson combiners.

Construction and Alignment

A 1:1 photomask of the circuit is provided in Figure 9 and double-sided G-10 fiberglass board with two-ounce copper cladding is recommended for construction. The ground points are indicated on the PCB photomask.

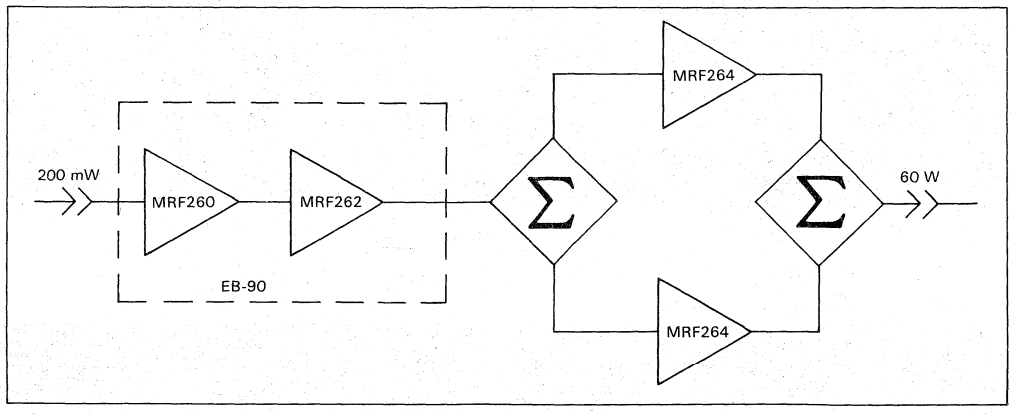
The inductors required for the splitter/combiner are constructed by winding the appropriate number of turns (closewound) on a temporary 1/8 inch form and then separating the individual turns by 0.020 inch. An Xacto number 11 knife blade was used for this purpose and provides the correct turns spacing. The 100-ohm isolation resistors, R1 and R2, must be noninductive and carbon composition resistors proved to be entirely adequate. In a properly tuned and balanced amplifier these resistors should remain fairly cool to the touch during normal operation. Each amplifier and coupler input and output port is designed to be terminated into 50-ohms to facilitate testing into a 50-ohm system.

A PCB bridge (Figures 3 and 9) is used to carry all of the dc feed circuitry. It acts as a continuation of the ground plane and enhances circuit stability. Solid copper (0.027 inch) and double-sided circuit board were used as a construction medium and no difference in performance was noted with either material.

Initial alignment is accomplished by driving the amplifier with a 5 watt CW source at approximately 160 MHz. The applied voltage is set at 12.5 volts and the variable capacitors, C4 and C5, are adjusted in an alternating manner to provide maximum output power. Full drive (15 watts) is then applied and the capacitor adjustments are repeated. At this point, the circuitry should be delivering 60 watts or more to the 50-ohm load with the 15 watts input. After the final adjustments are made, the isolation resistor temperature in either coupler should be relatively cool to the touch and the input VSWR should be at a minimum. Best results will be obtained if the transistors are beta matched (±10%) prior to installing them in the circuit.

Additional Comments

This amplifier has been extensively tested for ruggedness and reproducibility. The 15 watt input level makes it compatible with the EB-90 two-stage VHF amplifier as a driver. Together they form a chain requiring 200 mW of input power for a 60 watt or more output.



References

1. Lawrence R. Laveller; "Two Phased Transistors Shortchange Class C Amps," *Microwaves*, Pg. 48-54, February, 1978.

2. Ernest J. Wilkinson; "An N-Way Hybrid Power Divider," *PGM TT Transactions*, pg. 116-118, January, 1960.

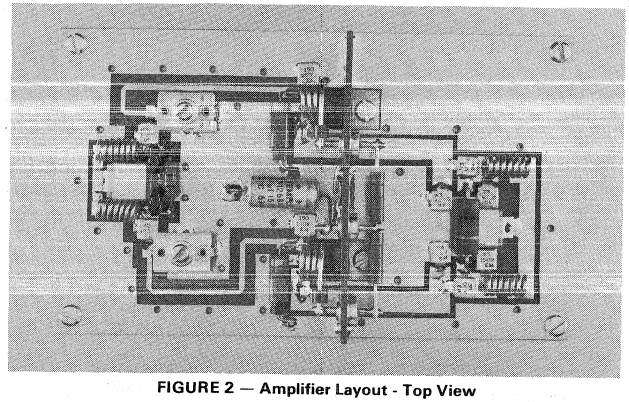


FIGURE 2 — Amplifier Layout - Top View

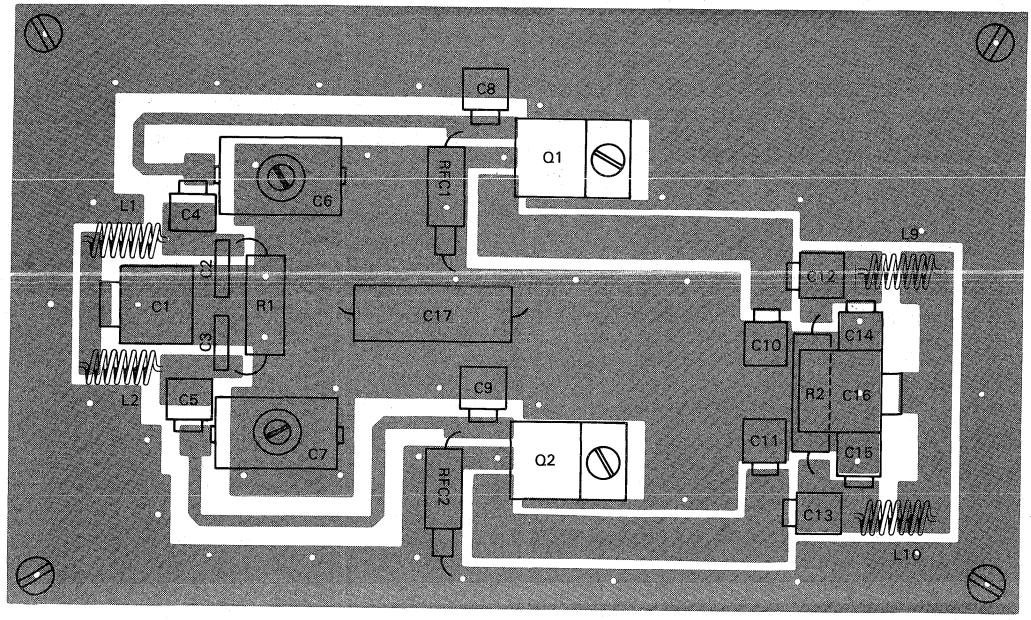
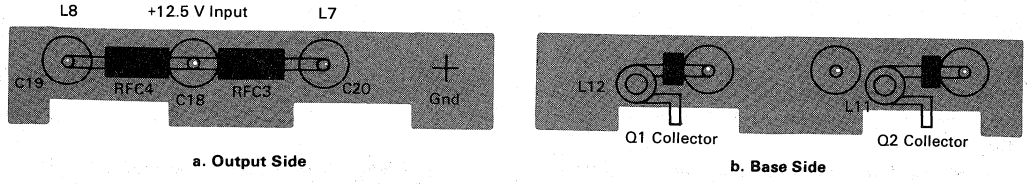


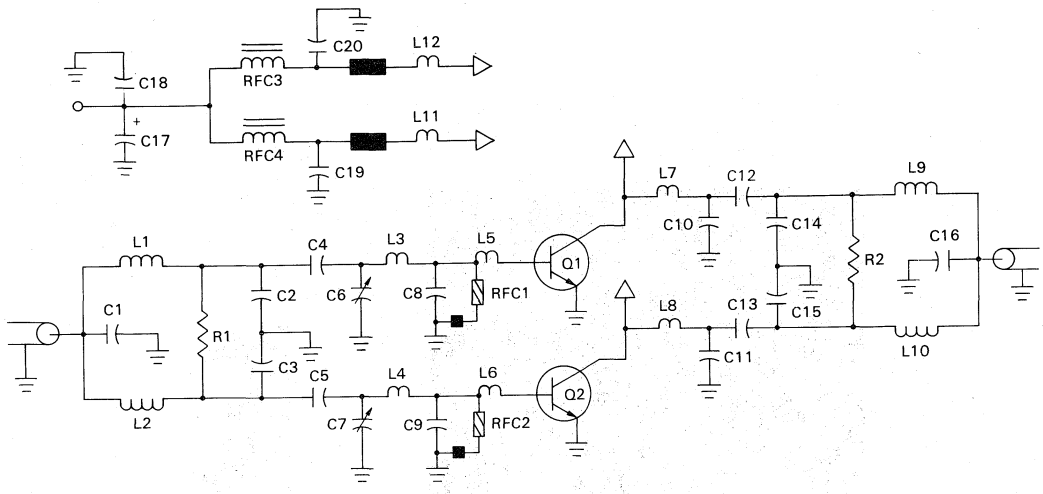
FIGURE 3 — Component Placement



a. Output Side

b. Base Side

FIGURE 4 — PCB Bridge Details



C1, C16 — 25 pF Unelco (J101)
C2, C3 — 15 pF CM04 Mica
C4, C5 — 68 pF Standex
C6, C7 — Arco 404 Variable
C8, C9 — 150 pF Standex
C10, C11 — 56 pF Standex
C12, C13 — 39 pF Standex
C14, C15 — 15 pF Standex
C17 — 100 μF @ 16 V Electrolytic
C18, C19, C20 — 680 pF Allen Bradley Feedthru

L1, L2 — 7 Turns #18, 0.125" ID
L3, L4, L5, L6 — Printed Inductors
L7, L8 — Printed Inductors
L9, L10 — 7 Turns #18 AWG, 0.125 ID
L11, L12 — 4 Turns #18 AWG, 0.250 ID w/Bead
Q1, Q2 — MRF264
RFC1, RFC2 — 0.15 μH Molded Choke w/Bead, Ferroxcube 56-590 65/3B
RFC3, RFC4 — 4 Ferrite Beads each on #18 AWG
R1 — 100 Ω 1/2 W Carbon
R2 — 100 Ω 2.0 W Carbon

FIGURE 5 — Schematic - 60 W Amplifier

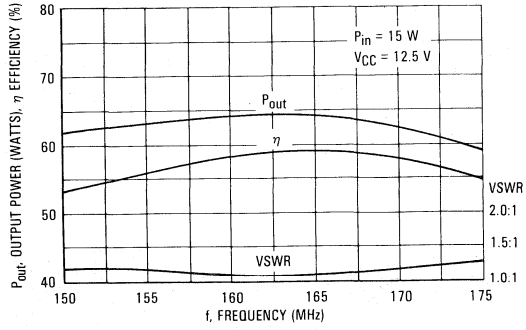


FIGURE 6 — Output Power, Efficiency, and Input VSWR versus Frequency

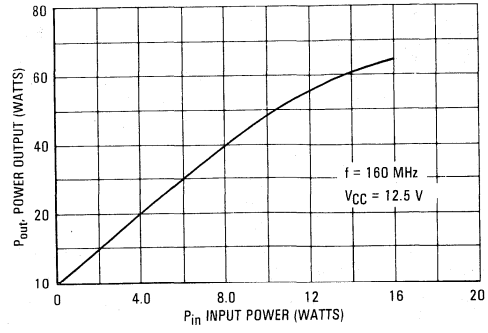
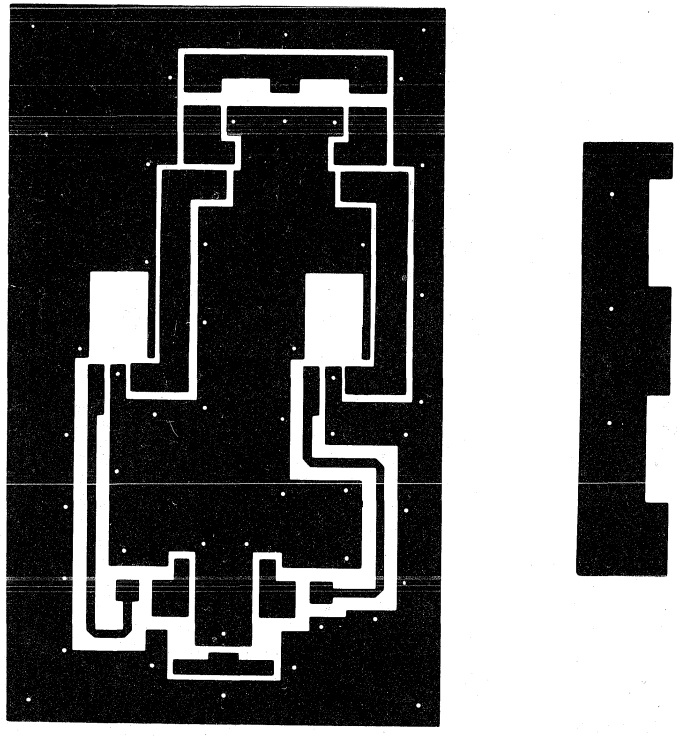


FIGURE 7 — Output Power versus Input Power



NOTE: The Printed Circuit Board shown is 75% of the original.

FIGURE 8 — PCB Photomaster

GET 600 WATTS RF FROM FOUR POWER FETs

Prepared by
Helge Granberg
Circuits Engineer, SSB

This unique push-pull/parallel circuit produces a power output of four devices without the added loss and cost of power splitters and combiners. Motorola MRF150 RF power FET makes it possible to parallel two or more devices at relatively high power levels. This technique is considered impractical for bipolar transistors due to their low input impedance. In a common-source amplifier configuration, a power FET has approximately five to ten times higher input impedance than a comparable bipolar transistor in a common emitter circuit. The output impedance in both cases is determined by the dc supply voltage and power level. The limit to the number of FETs that can be paralleled is dictated by physical, rather than electrical restrictions, where the mutual inductance between the drains is the most critical aspect, limiting the upper frequency range of operation. The magnitude of these losses is relative to the impedance levels involved, and becomes more serious at lower supply voltages and higher power levels. Since the minimum mounting distance of the transistors is limited by the package size, the only real improvement would be a multiple die package. For higher frequency circuits, these mutual inductances could be used as a part of the matching network, but it would seriously limit the bandwidth of the amplifier. This technique is popular with many VHF bipolar designs.

In paralleling power FETs another important aspect must be considered: If the unity gain frequency (f_α) of the device is sufficiently high, an oscillator will be created, where the paralleling inductances together with the gate and drain capacitances will form resonant circuits. The feedback is obtained through the drain to gate capacitance (C_{rss}), which will result in 360° phase shift usually somewhere higher than the amplifier bandwidth. Thus, the oscillations may not be directly noticed in the amplifier output, but may have high amplitudes at the drains. This can be cured by isolating the paralleling inductance, which consists of the dc blocking capacitors (C7-C10; Figure 2) and their wiring inductance from the gates. Low value non-inductive resistors which do not appreciably affect the system gain can be used for this purpose.

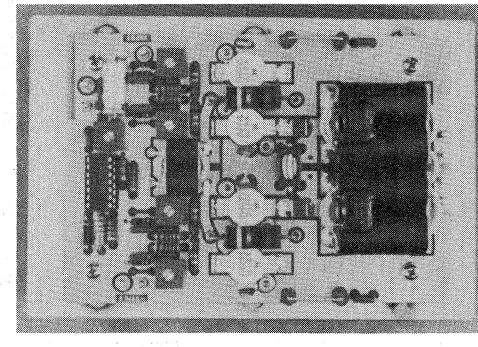
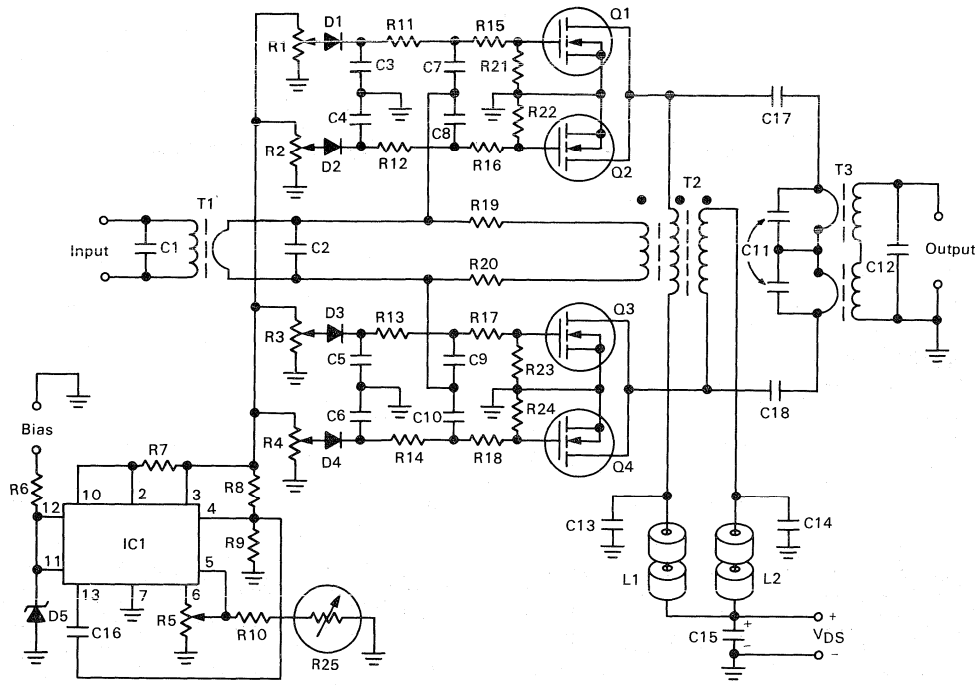


FIGURE 1 — Photograph of the 600 Watt 2.0-30 MHz MOSFET Linear Amplifier

CIRCUIT DESCRIPTION

Figure 2 shows a detailed schematic of the 600 W RF FET amplifier. It can be operated from supply voltages of 40 to 50 depending on linearity requirements. The bias for each device is independently adjustable, therefore no matching is required for the gate threshold voltages. Since the power gain of a MOSFET is largely dependent on the drain bias current, only g_m matching is required, and it can be only ± 10%.

FIGURE 2 — Detailed Schematic

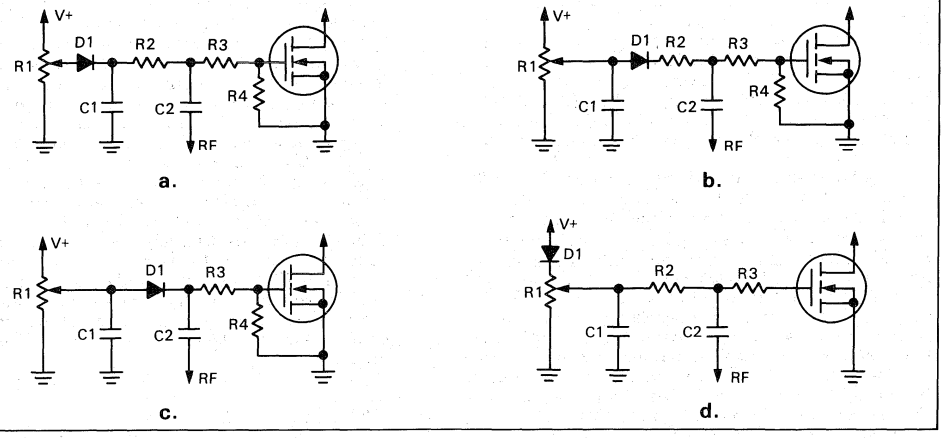


R1–R5 — 10 k Trimpot
R6 — 1.0 k/1.0 W
R7 — 10 Ohms
R8 — 2.0 k
R9, R21–R24 — 10 k
R10 — 8.2 k
R11–R14 — 100 Ohms
R15–R18 — 1.0 Ohms
R19–R20 — 10 Ohms/2.0 W Carbon
R25 — Thermistor, 10 k (25°C), 2.5 k (75°C)
C1 — Not used
C2 — 820 pF Ceramic chip
C3–C6, C13, C14 — 0.1 μF Ceramic
C7–C10 — 0.1 μF Ceramic chip
C11 — 1200 pF each, 680 pF mica in parallel with an Arco 469 variable or three or more smaller value mica capacitors in parallel
C12 — Not used
C15 — 10 μF, 100 V Electrolytic
C16 — 1000 pF Ceramic
C17, C18 — Two 0.1 μF, 100 V Ceramic each, (ATC 200/823 or equivalent)
D1–D4 — IN4148
D5 — 28 V Zener, IN5362 or equivalent
L1, L2 — Two Fair-Rite 2673021801 ferrite beads each or equivalent, 4.0 μH
T1–T3 — See text
Q1–Q4 — MRF150
IC1 — MC1723CP
All resistors 1/2 W carbon or metal film unless otherwise designated.

6

The circuit board was designed to allow several different gate biasing configurations (Figure 3). In circuit "a", which is used in the amplifier described here, D1 serves a purpose of preventing positive voltage from getting fed back to the bias source in case of a drain-gate short in a FET. This protects the other three devices from gate overvoltage. C1-R2 combination establishes an RF shunt from the gate to ground, which is necessary for stabilization. R4 could also be used for this purpose, but it would have to be a relatively low value, resulting in unnecessary high current drain from the bias supply. Normally R4 is only a dc return to ground, which is required with D1 preventing an open circuit in one direction. R3 is a low value resistor to prevent parasitic oscillations in a parallel FET circuit, as discussed earlier. Variations "b" and "c" are basically the same, except for R2, which can be used to control the amount of RF rectified by D1. In addition to blocking the dc in one direction, D1 can be used for proportional biasing, in which the bias voltage increases with RF drive. This allows the initial idle current to be set to a lower than normal value, increasing the system efficiency.

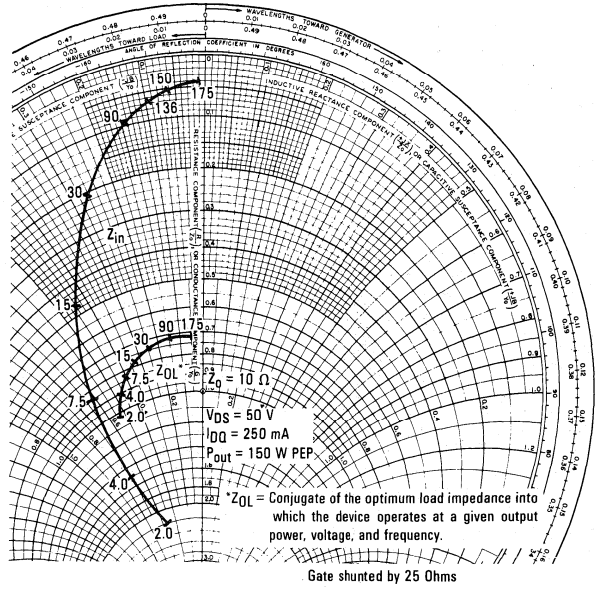
FIGURE 3 — Various Bias Configurations



The gate de-Qing in these circuits is done with R4. Circuit "d" is another variation, where D1 is moved in series with R1 eliminating R4. The value of R1 must be high to prevent destruction from a drain-gate short. The common bias is derived from IC1 (MC1723CP) which provides both line and load regulation. The line voltage regulation is defeated when the voltage to Pin 12 falls below 24 V, and the bias input can be used for Automatic Level Control (ALC) shut-down or linear ALC function. The regulator output voltage is adjustable from 0.5 to 9.0 volts with R5, which can be permanently set to 7.0–8.0 V. This voltage is also controlled by the combination of R10 and R25. R25 is a thermistor, and is tied to the heat sink for bias temperature compensation.

In Figure 2, the input from T1 is fed to the gates through C7-C10 and R15-R18. The input matching is initially done at the high end of the band (30 MHz). In contrast to a bipolar push-pull circuit, where the base-to-base impedance varies with class of operation, the gate-to-gate impedance of a common source FET circuit is always twice that from gate to ground. In this case, where two FETs are in parallel on each side, the gate-to-gate impedance equals the gate-to-ground impedance of one device. From the Smith chart information (Figure 4) this can be established as 3.45 ohms.

FIGURE 4 — Series Equivalent Impedance



The effect of R11–R14 and R21–R24 is minimal and can be disregarded. Considering the standard integers for T1 impedance ratio, 9:1 with its 5.55 ohms secondary appears to be the closest. This would set the values of R15–R18 at 2.0 ohms each, which would result in 3.5 dB gain loss, and about 1.0 W would be dissipated in each resistor. For this reason it was decided to reduce their values to 1.0 ohm, and trim the values of C1 and C2 for lowest input VSWR. As a trade-off, the VSWR will peak slightly at 15–20 MHz, but still remain below 2:1.

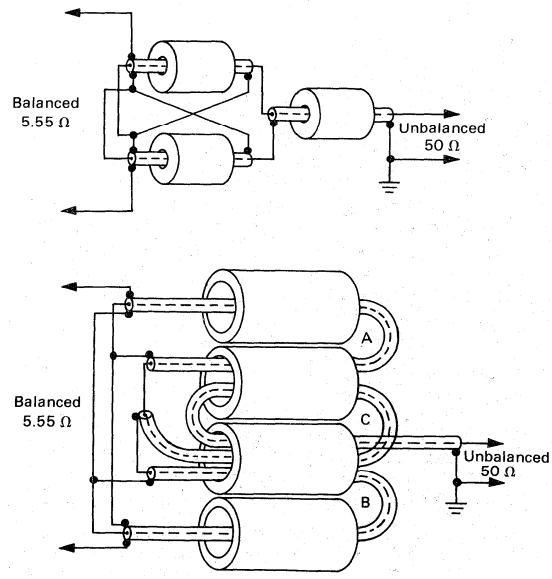
Negative feedback is derived from a winding in T2 through R19 and R20. Its purpose is to equalize the load impedance for T1 and reduce the amplifier gain at low frequencies. Since the gate to source capacitance of a MOSFET is fairly constant with frequency, the amount of feedback voltage is inversely proportional to its reactance. This function should be more or less linear, unless the inductive reactance of T1 is too low, or if resonances occur somewhere in the circuit. No computer analysis (as in Reference 2) was performed on the negative feedback system. Instead a simple approach described in Reference 1 was taken, where the gain difference between 2.0 and 30 MHz determines the feedback voltage required to equalize the voltages of the secondary of T1 at these frequencies. With an input impedance of 45 ohms at 2.0 MHz, and the feedback source delivering 15 $V_{(RMS)}$, (P_{out} = 600 W) the values of R19 and R20 will be around 10 ohms each.

A ferrite toroid or a two hole balun type core can be used for T2. Relatively low μi material with high curie temperature is recommended, since the minimum inductance requirement for the dc feed winding is less than 2.0 μH. Depending on the material, T2 can reach temperatures of 200–250°C, which the wire insulation must also be able to withstand. Several different output transformer configurations (T3) were tried, including a transmission line type in Figure 5. Although difficult to make, it has the advantage that low μi, low loss ferrite can be used with multiple turn windings. At this power level, heat in the output transformer was a major problem. High permeability materials, required in the metal tube and ferrite sleeve transformers could not be used because of their higher losses and low curie temperature. On the other hand, low μi cores with larger cross sectional areas were not readily available. To reach the minimum inductance required for 2.0 MHz, two of these transformers, with low permeability ferrite cores were connected in series. Both have 9:1 impedance ratios. Alternatively the secondaries can be connected in parallel with twice the number of turns (6) in each. C11 must withstand high RF currents, and must be soldered directly across the transformer primary connections. Regular mica or ceramic capacitors cannot be used, unless several smaller values are paralleled.

PERFORMANCE

Due to the mechanical proximity of the four MOS FET devices, the RF ground of the circuit board is poor, and results in 1.0–1.5 dB gain loss at 30 MHz, which can be seen in Figure 6. The ground plane can be improved by connecting all source leads together with a metal strap over the transistor caps. Another method is to place solder lugs under each transistor mounting screw, and solder each one to the nearest source lead. In this case, the heat sink will serve as the RF ground. Although the 3rd order IM distortion is not exceptionally good, (Figures 6, 7) the worst case 5th order

FIGURE 5 — Number of Turns Shown is not Actual



products are better than -30 dB at all frequencies, and as can be expected with FETs, the 9th and higher order products are in the -50 to -60 dB level. It can also be noticed from Figure 6, that the IMD does not increase at reduced power levels, as common with bipolar amplifiers. The even order output harmonic content depends greatly on the device balance as in any push-pull circuit. The worst case is at the low frequencies, where numbers like -30 to -40 dB for the 2nd harmonic is typical. The highest 3rd harmonic amplitude of -12 dB is at 6.0-8.0 MHz carrier frequency. Information on suitable harmonic filters is available in Reference 3. The stability of the amplifier has been tested into a 3:1 load mismatch at all phase angles. It was found to be completely stable, even at reduced supply voltages.

In a MOSFET (common source) the ratio of feedback capacitance to the input impedance is several times higher than that of a bipolar transistor (common emitter). As a result, a properly designed FET circuit should be inherently more stable, especially under varying load conditions.

It must be noted, that special attention must be given to the heat sink design for this unit. With the 200-300 watts of heat generated by the transistors in a small physical area, it must be conducted into a heat sink efficiently. This can be only done with high conductance material, such as copper. If aluminum heat sink is used, a copper heat spreader is recommended between the transistor flanges and the heat sink surface.

FIGURE 6

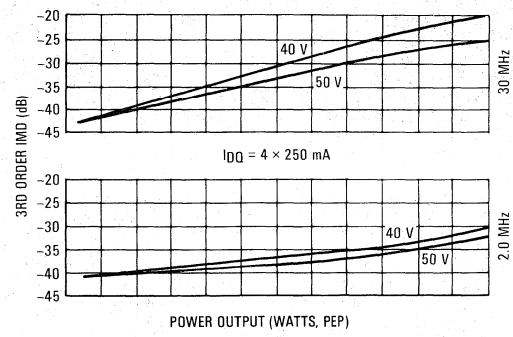
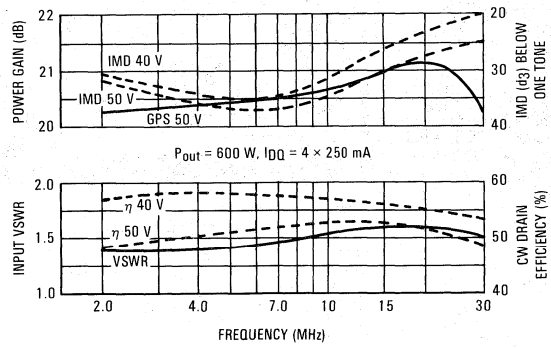
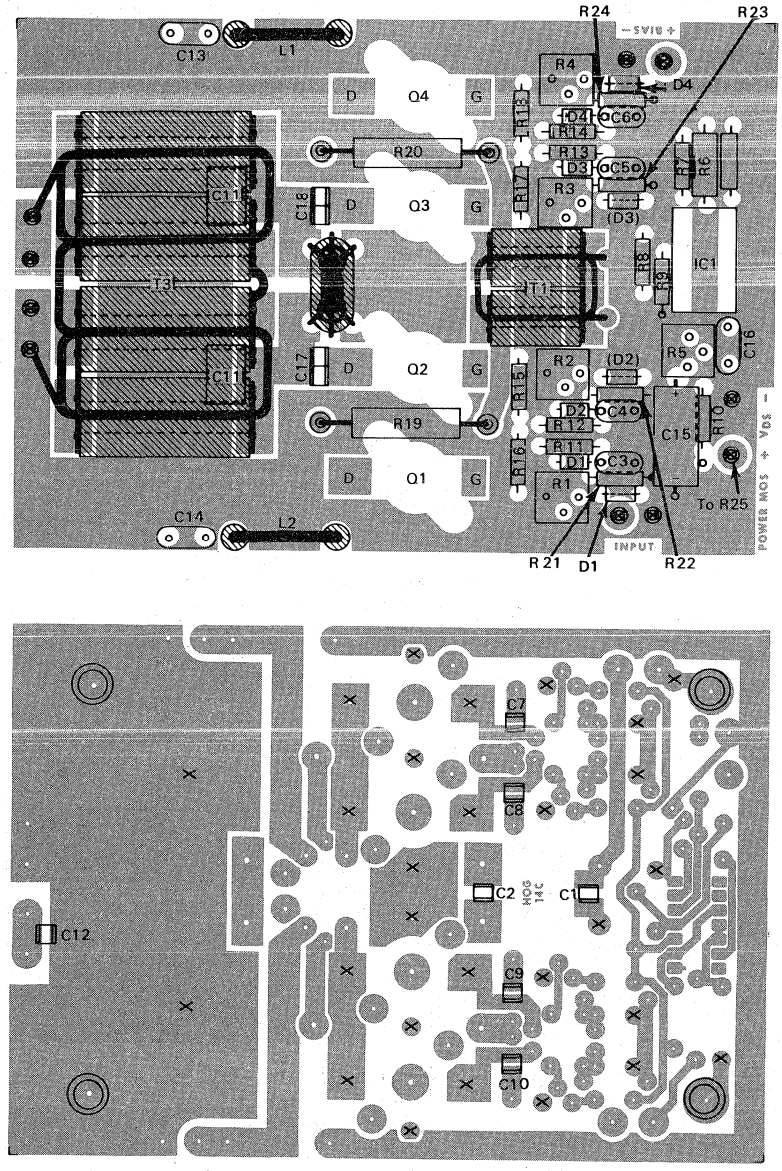


FIGURE 7



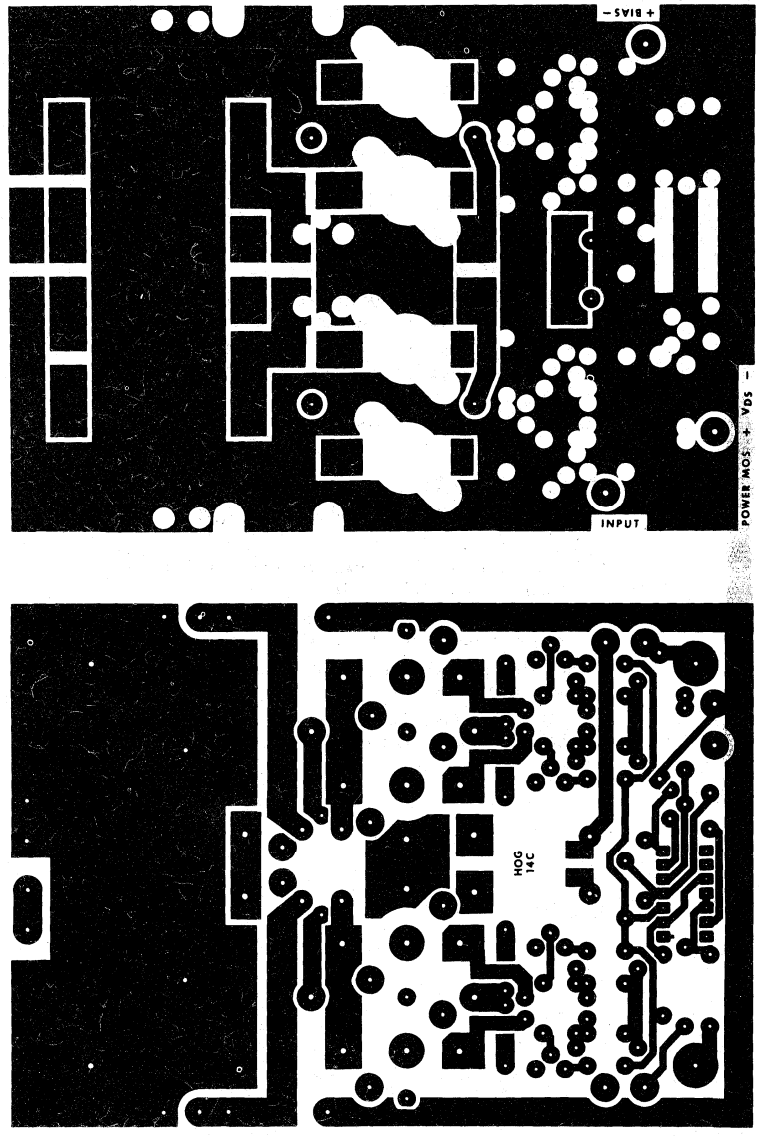


X denotes feed-through eyelets

⊗ denotes terminal pins

◎ denotes board spacers

FIGURE 8 — Component Locations



NOTE: The Printed Circuit Board shown is 75% of the original.

FIGURE 9 — Circuit Board Photo Master

REFERENCES

1. "A Two-Stage 1.0 kW Solid-State Linear Amplifier," AN-758, Motorola Semiconductor Products, Inc.
2. "Low-Distortion 1.6 to 30 MHz SSB Driver Designs," AN-779, Motorola Semiconductor Products, Inc.
3. H. Granberg, "MOS FET Power in the kW Level," QST, Dec., 1982, Jan., 1983

BIBLIOGRAPHY

1. O'Hern, *Simple Low-Pass Filter Design,* QST, Oct. 1958
2. Wetherhold, *Low-Pass Filters for Amateur Radio Transmitters,* QST, Dec., 1979
3. Granberg, *Power MOS FETs versus Bipolar Transistors,* RF Design, Nov. - Dec., 1981.
4. Hejhall, *VHF MOS Power Applications,* MIDCOM Paper, Dec., 1982
5. DeMaw, *Practical Class-A and Class-C Power — FET Applications at HF,* MIDCOM Paper, Dec., 1982

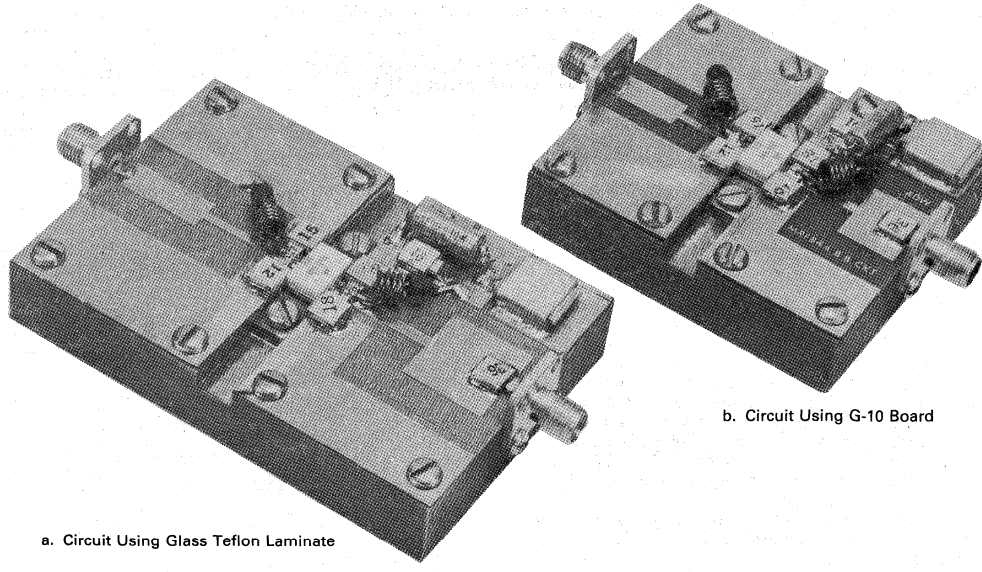
A 30 WATT, 800 MHz AMPLIFIER DESIGN

Prepared by
Alan Wood
Semiconductor Product Sector

INTRODUCTION

Simplicity and compactness mark the design of this 30 Watt amplifier designed for the 800 MHz mobile communications band. The amplifier uses the internally matched MRF844 transistor in a common base Class C configuration providing a minimum of 5.0 dB gain over a fixed tuned bandwidth of 800 to 870 MHz at 12.5 volts.

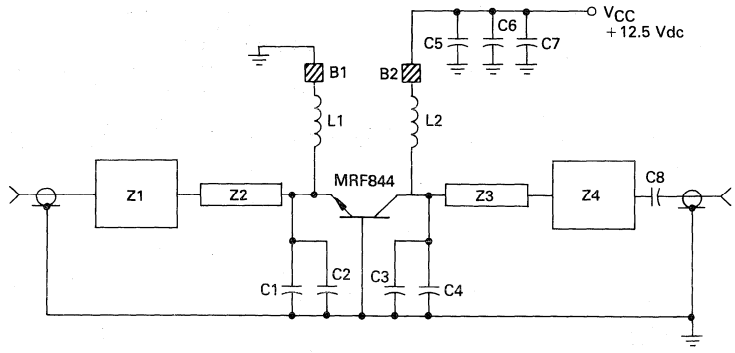
Lower manufacturing costs are of prime concern to land mobile equipment suppliers and single-board, fixed tuned transmitter amplifier designs are becoming increasingly common. Two versions are therefore presented, one using glass teflon laminate and the second using less expensive G-10 board. (Figure 1).



a. Circuit Using Glass Teflon Laminate

b. Circuit Using G-10 Board

Figure 1 — Two Versions of MRF844 Broadband Circuit



B1, B2 — Ferroxcube Bead 56-590-65/3B
C1 — 15 pF Mini-Underwood Mica
C2 — 12 pF Mini-Underwood Mica
C3, C4 — 18 pF Mini-Underwood Mica
C5 — 91 pF Mini-Underwood Mica
C6 — 1000 pF Unelco Mica
C7 — 1.0 μF Electrolytic
C8 — 36 pF Mini-Underwood Mica

L1, L2 — 4 Turns, #20 AWG Enameled Wire 0.15″ ID
Z1 – Z4 — Microstrip; See Photomasters
Board Material — See Text

Figure 2 — Circuit Schematic of 30 Watt 806-870 MHz Amplifier

CIRCUIT DESCRIPTION

The circuit is designed to be driven from a 50 ohm source and be terminated in a nominal 50 ohm load. Both input and output matching networks are similar in design and consist of two element short-step Chebyshev transmission line transformations fabricated as microstrip lines (Reference 1). Mini-Underwood mica capacitors are used at the input and output of the transistor, transforming the complex inductive impedance to an essentially non-reactive real impedance over most of the band. A minimum of additional components provide the dc biasing and RF decoupling. Refer to Figure 2 for a schematic diagram of the amplifier.

Design of microstrip circuits using a G-10 board material is complicated by several factors. This is discussed in detail in Reference 2. The main points to be considered are, the lack of control over the dilectric constant in the manufacturing process; a greater tolerance in the dilectric thickness than in the case of higher quality substrates intended for microstrip applications, and changes in relative dilectric constant with frequency. Despite these apparent disadvantages, G-10 board can be used successfully if the ultimate in bandwidth is not sought.

Frequency dependence of the relative dilectric constant was determined by characterizing a nominal 25 ohm microstrip line over a wide range of frequencies using an automatic network analyser. Compensation for the coaxial to microstrip transitions was established using a computer optimized model (Reference 3). Figure 3 is a graph of the relative dilectric constant versus frequency determined for the laminate used by this method. It should be noted that differences in epoxy composition could affect both the low frequency dilectric constant and its frequency dependence.

CONSTRUCTION PROCEDURES

Both amplifiers were mounted on 0.5″ thick copper blocks, 2.25″ by 2″ in the case of the G-10 board design and 3″ by 2″ for the glass teflon board. The blocks were slotted to a depth of 0.130″ to enable mounting the transistor leads level with the top of the circuit board. Thermal compound was used between the transistor flange and the mounting block to ensure low thermal resistance. With the block held in contact with a larger heatsink this configuration proved adequate for test purposes. In a production design, the transistor would normally be thermally connected to the case of the transmitter. However, care should be taken to operate the device under all conditions within the Power Dissipation limits shown on the data sheet.

As with any circuit designed to work at UHF frequencies, good grounding is essential for best performance and stability. Copper foil was wrapped around the board adjacent to the transistor mounting to connect the underside ground plane to the transistor common leads.

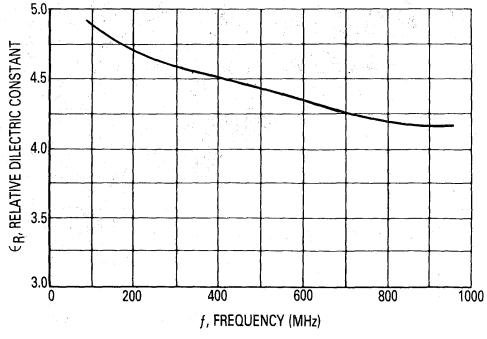


Figure 3 — Relative Dilectric Constant (G-10) versus Frequency

Additional copper foil was wrapped around the board to connect the 1000 pF Unelco capacitor pad to the lower ground plane.

Positioning of the emitter and collector shunt capacitors is critical to the resulting amplifier performance. The capacitors should be mounted as close to the transistor case as possible. Minor tuning of the circuit can be achieved by lateral movement of these components. Larger tuning adjustments can be incorporated by replacing part of the fixed shunt capacitance by a variable trimmer.

Both circuits use 28 mil dilectric 2 ounce copper clad laminate. Refer to Figure 6 for a 1:1 Photomaster of the circuit boards.

PERFORMANCE DATA

Similar performance was measured for the same part soldered in either circuit. Typical performance curves for this broadband design are shown in Figures 4a, 4b, and 4c for the glass teflon design and Figures 5a, 5b, and 5c for the G-10 based circuit. Circuit losses in the G-10 board were less than expected and were certainly minimized by the short fractional wavelength transmission lines employed.

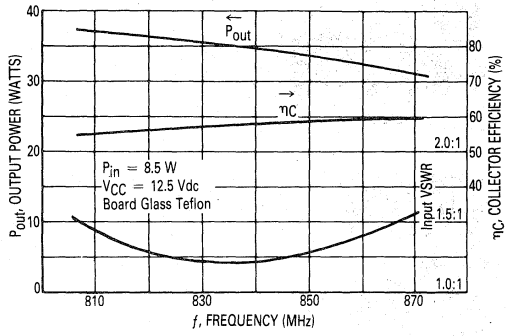


Figure 4a — Typical Performance in Broadband Circuit

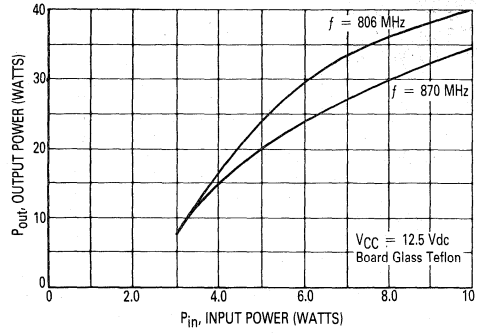


Figure 4b — Output Power versus Input Power

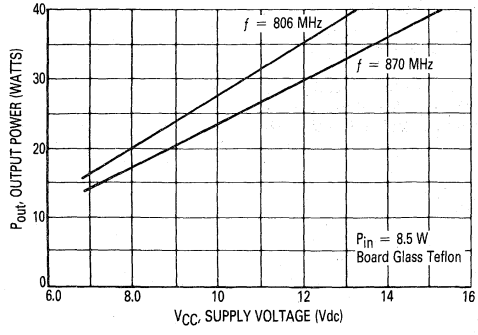


Figure 4c — Output Power versus Supply Voltage

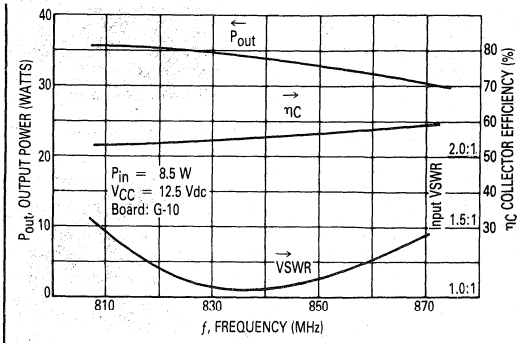


Figure 5a — Typical Performance in Broadband Circuit

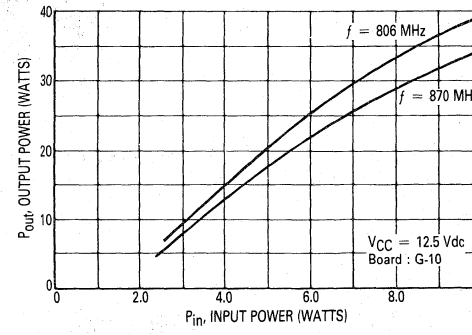


Figure 5b — Output Power versus Input Power

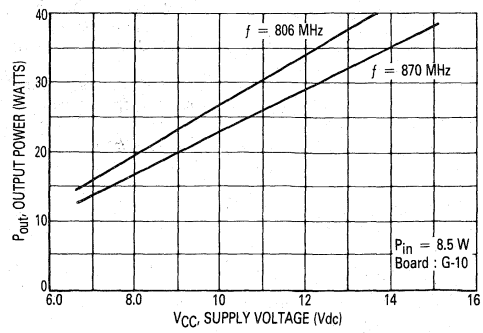
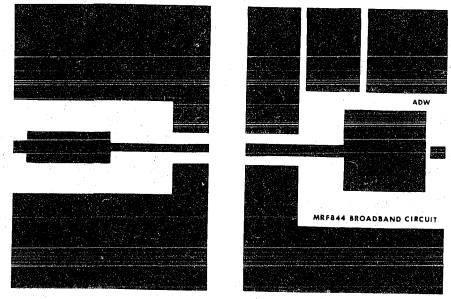
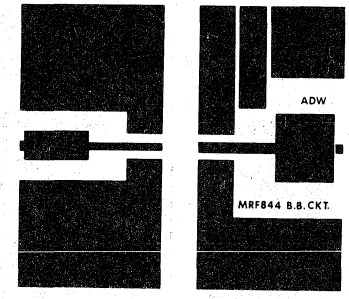


Figure 5c — Output Power versus Supply Voltage

NOTE: The Printed Circuit Board shown is 75% of the original.



a. Photomaster Using Glass Teflon Laminate



b. Photomaster Using G-10 Board

Figure 6 — Two Photomaster Versions of MRF844 Broadband Circuit

REFERENCES

1. G. L. Mattheai. *Short-Step Impedance Transformers. IEEE Transactions on Microwave Theory and Techniques.* Vol. MTT-14 No 8 August 1966.
2. Glenn Young. *UHF Microstrip Amplifiers Utilizing G-10 Epoxy Glass Laminate.* Motorola Application Note AN-578.
3. M. L. Majewski. *Modeling and Characterization of Microstrip to Co-axial Transistions. IEEE Transactions on Microwave Theory and Techniques.* Vol. MTT-29 No 8 August 1981.

MOUNTING CONSIDERATIONS FOR MOTOROLA RF POWER MODULES

Prepared by:
Henry Pfizenmayer *and* Sam Coffman
RF Power Modules

INTRODUCTION

The packaging used for standard Motorola RF Power modules consists of a copper flange on which the substrates are soldered and a non-conductive cover which is either of a "snap-on" or epoxy attached design. The ceramic substrates are either 96% alumina ($A1_2O_3$), 99.5% alumina or 99% Beryllium oxide (BeO). These substrates are attached to the copper flange using either lead-tin or indium based soft solders. Typical liquidus temperatures of these solders are in the 149°C to 163°C range.

The purpose of this paper is to present the mechanical factors which should be considered in mounting these modules in equipment.

MAJOR MOUNTING FACTORS

There are three major considerations in mounting an RF power module. First, the flange is used for the RF electrical ground reference. Typical inductance of the connection pins used on these modules is about 18 nanohenries per inch or 1.8 nanohenries per 100 mils. Since at 800 MHz a nanohenry has about 5.0 ohms reactance, it is easy to see that it would be almost impossible to achieve a low reactance ground through the use of pins alone. Second, the copper flange provides the thermal path for the removal of the heat produced in the active devices present in the module. Thus, proper thermal handling must be considered in mounting the module. Finally, we must consider the mechanical stresses placed on the module by the mounting techniques used. Here we consider stresses placed on the leads and bending or twisting of the mounting flange which would cause ceramic fractures.

MODULE FLANGE FLATNESS

During the processing of the module, consideration has to be given to the various stresses produced. Through analysis of these stresses and the materials used we can arrive at the maximum allowable flange bending which can be tolerated from a mechanical standpoint. In determining the allowable flange flatness conditions, both analytical and empirical analyses were performed. Agreement between both of these analyses was very good. The theoretical analysis was performed by Motorola Government Electronics Group, Mechanical Engineering Laboratory. GEG was selected to do this work because they have done extensive work in the area of laminate stresses and have available several proven computer programs which apply directly to this problem. The assigned task was to provide an estimate of the maximum amount of initial bow (curvature) in the mounting flange which would not subsequently cause the ceramic substrate to fracture in the final assembled state. For the results of this analysis, see Table 1.

MOUNTING CONSIDERATIONS

The theoretical analysis shows that some of the responsibility for proper mounting rests on the user. Proper consideration should be given to the following items:

1. Flatness of the mounting area must be such that the final mounting of the module will not bend the flange beyond the limits given in Table 1.
2. Attention must be given to surface finish and cleanliness of the mounting surface. For instance, if one mounts the module with thermal compound and uses a dirty work area which allows 3 to 5 mil particles to be present in the compound, a failure mode can be produced.
3. Another consideration is the movement of material around tapped or punched holes. A tapped or punched hole which leaves a burr on the mounting surface can lead to failure modes.
4. In addition, rigidity of the mounting surface and its material should be considered. For instance, the copper flange on an aluminum heatsink will result in a bimetallic system which can create a bending problem. Consideration of the direction of ribs in a heatsink should be made to maximize stiffness in the direction of bending or adequate thickness of the heatsink must be provided to control bending.

It is not desirable to mechanically constrain the ends of the module so that no "slip" is possible between the module flange and its mounting surface. If the ends are constrained and the temperature differential between the module and the heatsink is significant, there can be enough bending of the module flange to break the ceramic. An example calculation is shown below to demonstrate this problem.

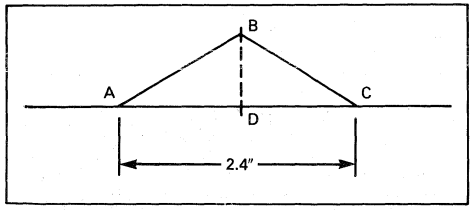
Assume that the ends of the flange are constrained at the centerline of the mounting holes. (2.4 inches for MHW612A/MHW710/MHW720 series modules). Assume

that the module is mounted on a machined aluminum heatsink.

Thermal expansion coefficients in μinch/inch/°C
Aluminum 25 x 10^{-6}
Copper 17 x 10^{-6}
L = 2.4 inches

For a reasonable approximation assume the thermally induced bending creates an isosceles triangle as shown in Figure 1.

FIGURE 1



Assume that the module flange changes temperature from 25°C to 50°C and the heatsink changes temperature from 25°C to 30°C in the same time (obviously the heat input to the system comes from the copper flange — more on this later).

Heatsink △ L (aluminum) = 2.4" x 5°C x 25 x 10^{-6}
= 0.0003"
Flange △ L (copper) = 2.4 x 25°C x 17 x 10^{-6}
= 0.00102"

So length ABC = 2.40102, AB = 1.20051"
length AC = 2.4003", AD = 1.20015
And $AB^2 = AD^2 + BD^2$
$BD = \sqrt{AB^2 - AD^2}$

So BD = 0.029397 inches which far exceeds the allowable flange bend.

This analysis also points out the advantage of keeping the heatsink and the flange at lowest possible temperature differential through the use of thermally conducting compounds between the surfaces.

For instance, in the example given above with an aluminum/copper system, the copper flange will remain in tension at any temperature *above* the temperature at which the system was constrained as long as the temperature ratio between the heatsink and flange is kept less than the ratio of the thermal expansion coefficients or 25/17. Incidentally, this assumes that the heat input source to the system originates in the copper flange. This situation points out the folly in some types of temperature cycling testing. For instance, if the aluminum/copper system is constrained at 25°C and is uniformly heated to say 125°C, the copper remains in tension — if the system is cooled below 25°C, the copper will go into compression. This is exactly the opposite situation obtained when the heat input to the system comes from the copper flange.

The above is a rather elementary analysis of the thermal effects on the module/heatsink system. Many other factors are involved such as relative strengths of the materials involved, bending of the mounting screws and so forth.

What should be derived from this discussion is that the design of the mounting for the module/heatsink system is not a simple one and should not be done in a casual manner.

Our recommendation is that a mock version of the system be constructed early in the equipment design and thermal cycling performed both with external heat input to the system and with heat input to the system from the module. This is a very effective "analog computer" and direct measurements of the flange/heatsink deflections can be made. In this manner the actual expected flange excursions can be compared to the recommended maximum flange bending to determine whether the design is adequate. Incidentally, the recommended maximum deflection values given in Table 1 have a safety factor of approximately 2. That is, the deflection required to crack the ceramic is approximately twice the value given. Table 1 includes data showing the empirical deflections required to fracture a ceramic board in the module.

5. We strongly recommend the use of a good thermal compound between the mounting surface. Sufficient material must be used to fill all gaps which may be present. We have not been able to create any mechanical problem with excess compound as long as there is a path for the excess material to escape as the module is tightened down with the mounting screws. At this point it should be pointed out that unless both the module flange and the heatsink were lapped to absolute gauge block flatness, there will always be a significant air gap between areas of the flange and the heatsink. Since it is obviously not practical to achieve a lapped surface of this quality, this portion of the mounting problem resolves to one of mechanical rather than thermal considerations. As an aside, some of the Motorola modules also have machined surfaces which may be oxidized to some degree. Infrared thermography of the active die was performed to see if there was any thermal degradation due to this oxide layer and no degradation could be found. This has also been found true on lapped discrete transistor flange mount parts.

Several manufacturers of thermally conductive heatsink compound exist. We have used products from Wakefield and Dow Corning with success.

MOUNTING HARDWARE

Obviously an ideal mounting hardware scheme would be one in which the clamping pressure remained constant with age. One way of achieving this is through the use of conical washers — one trade name is Belleville washers. Another possibility is "wavy" washers. Proper selection of mounting hardware and torque is also necessary. We recommend the following mounting hardware sizes and torques:

4–40	3 in/lb
6–32	5 in/lb
8–32	5 in/lb

TIGHTENING SEQUENCE

A very important factor to be considered in mounting the module is the proper torquing sequence. The personnel involved in mounting the modules should be given careful instruction and their procedures monitored at regular intervals. Since the flanges are punched from a

roll of material, there can sometimes be a small "roll-up" at the end of the mounting flange. If one considers what can happen if the mounting hardware were tightened completely at one end first, it is easy to see that the other end could be "lifted" off the mounting surface well in excess of the allowable flange bending tolerance.

This should be avoided by first lightly alternately snubbing down the mounting hardware "finger-tight." Next, the hardware can be torqued to its final specification again in at least two sequential steps.

THE IMPORTANCE OF THIS TORQUING SEQUENCE CANNOT BE STRESSED TOO HIGHLY

LEADS

The leads used on the standard Motorola RF Power Modules are of either tinned copper, gold or silver plated KOVAR, or pure silver strap, typically 5 to 10 mils thick and 15 to 20 mils wide. The leads are intended for making electrical connections to the modules *only* and are not intended to support the module at any time in the assembly process. Consideration should be given to the stresses which may occur during mounting or testing. Poorly designed test fixtures can create lead stresses far above those encountered in the end-use equipment. It is recommended that the fixture be designed so the leads are always clamped after the flange is clamped and the tolerances be such that an upward force is never placed on the leads, even as the fixture wears. Motorola's specification for lead pull in shear and peel are 908 gm shear and 454 gm peel for BeO boards and 1500 gm shear and 750 gm peel for alumina boards. Modules from PC86, 90, and 91 product lines use BeO boards. Modules from the PC87, PC103 line use one alumina and one BeO board. PC41, PC64, and PC104 use alumina boards.

DEFLUXING

These modules are designed to be manually soldered into an assembly. The modules have a silicone die coat over the active die, MOS capacitors, and nichrome resistors. The die coat used will not withstand the normal flux removal fluids and severe reliability problems could be incurred if the flux removal fluids or solder fluxes penetrate the inside of the module. We recommend a flux activity of no more than R or RMA be used.

CONCLUSION

In mounting RF power modules, the following major areas should be considered:

1. Heatsink flatness.
2. Use thermal compound — eliminate dirt or grit in the compound or on mounting surfaces, use an adequate amount to fill gaps.
3. Tighten modules down in an alternate manner "finger-tight" before final torquing.
4. Be careful with defluxing operations.
5. Consider lead stresses, both in mounting and testing.

TABLE 1 — Maximum Deflection

DEVICES	THEORETICAL DEFLECTION TO BREAK LINE		***EMPIRICAL DEFLECTION TO BREAK MIN	AVG	MAXIMUM RECOMMENDED DEFLECTION COMBINED HEATSINK & FLANGE CONVEX	CONCAVE	OUTGOING QA SPEC. (MAX) CONVEX	CONCAVE
MHW709, 710	PC41	0.015	0.0190	0.0218	0.008	0.010	0.005	0.005
MHW720 *	PC64	0.015	0.0190	0.0206	0.008	0.010	0.005	0.005
MHW720 **	PC64	0.011	0.0075	0.0079	0.007	0.0085	0.003	0.005
MHW720A	PC104	—	0.0190	0.0206	0.008	0.010	0.005	0.005
MHW612, 613†	PC86	0.0025	0.0019	0.0028	0.0015	0.002	0.001	0.002
MHW612A, 613A†	PC87	0.011	0.0103	0.0108	0.007	0.0085	0.003	0.005
MHW808	PC90	—	0.0025	0.0034	0.0015	0.002	0.001	0.002
MHW808A	PC103	—	0.0065	0.0070	0.0035	0.004	0.0015	0.0025
MHW820	PC91	0.005	0.0073	0.0084	0.004	0.005	0.002	0.003

ALL UNITS IN INCHES

* PC64 was changed to alumina board — BeO carrier transistor construction similar to PC41 in February, 1983. All product with date code .883 and after has this construction.

** Old construction of PC64 with total BeO output board.

*** Measured deflection to break a substrate within 3 to 5 seconds of application of force.

† These devices will be obsolete on September 30, 1983. Contact Motorola for the current availability and recommended discrete transistor replacement lineup.

6

Engineering Bulletin

By Dan Moline
and
Dan Bennett
Motorola RF Circuits Engineering

LOW COST UHF DEVICE GIVES BROADBAND PERFORMANCE AT 3.0 WATTS OUTPUT

LOW COST UHF DEVICE GIVES BROADBAND PERFORMANCE AT 3.0 WATTS OUTPUT

INTRODUCTION

The major cost element in low-to-medium power (1.0–5.0 W) RF transistors is the package. Several years ago Motorola took a major step in limiting cost increases by introducing the common emitter TO-39 package. Through the use of appropriate circuit design and construction techniques, use of the CE TO-39 can be extended to broadband UHF amplifiers producing up to 3.0 W output power.

This bulletin describes a broadband circuit application of the low cost MRF630 — an all gold metallized, emitter ballasted, high figure of merit transistor capable of 3.0 W output power with 10 dB gain at 512 MHz. A photo of the amplifier is shown in Figure 1. Emphasis is placed on mounting techniques which minimize parasitic inductances and maximize heat transfer.

CONSTRUCTION

TO-39's used as RF amplifiers are most commonly found in transmitter exciter chains mounted on printed circuit boards. The parts are seated on small disc shaped insulators and are heatsunk using press-fit "top hat" style radiators (Figure 2). Heat is inefficiently conducted upwards through the metal can (Figure 3) and radiated by commercially available heatsinks, called "top hats". As a result, the θ_{JA} is excessive, causing elevated junction temperatures and thermal slump problems. Because the TO-39 is situated above the PC board resulting in long leads, input Q's are also excessive and combine to limit broadband performance and device gain. In low power applications (<1.0 W) and VHF frequencies or lower, the problems mentioned above may not be noticeable. Higher power devices

FIGURE 1

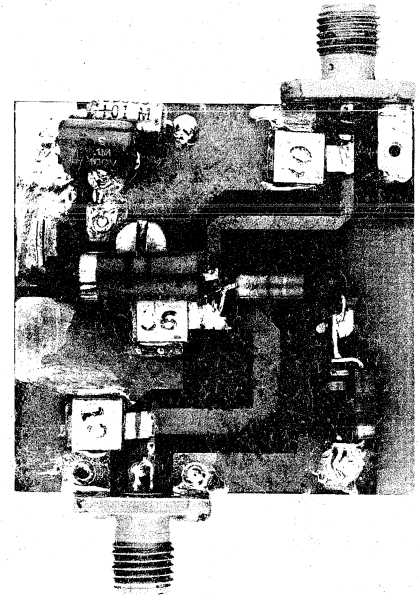


FIGURE 2

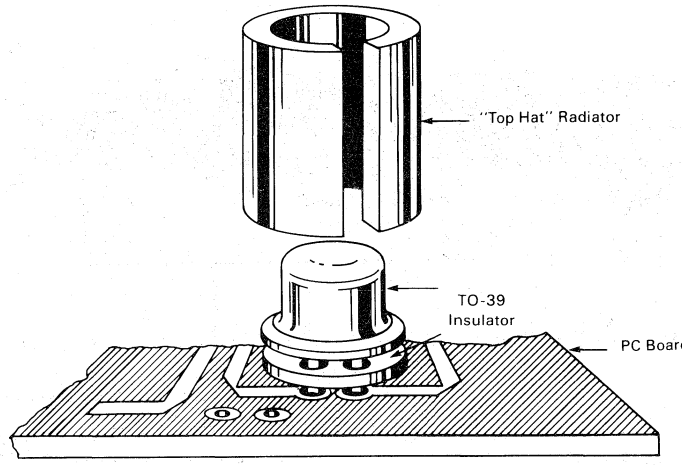
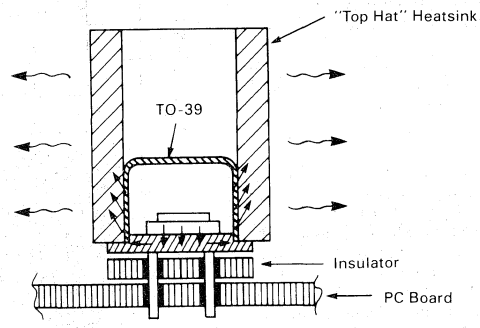


FIGURE 3



such as the MRF630, however, should be treated with the same considerations as any other RF power transistor (i.e., provisions for proper heatsinking and grounding).

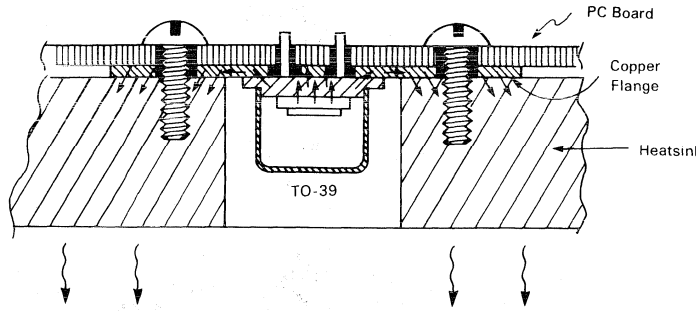
When using an SOE power transistor, heatsinking is simplified with the inclusion of a stud or flange. Since TO-39's have neither, some modifications are required. Figure 4 depicts a means of heatsinking by soldering a "flange" to the bottom side of the TO-39 package, thus providing a path for heat flow directly beneath the transistor die. The "flange" is secured to the amplifier heatsink by one or two screws. With this arrangement, maximum heat dissipation can be provided with a minimum amount of space consumption. This method also creates better electrical grounding as the package is now mechanically connected to chassis ground. The attachment of this "flange" provides improvements in both grounding and heatsinking. Both are fundamental requirements to obtain the expected performance from an RF power TO-39 such as the MRF630.

CIRCUIT DESCRIPTION

The circuit, which was optimized for the MRF630, uses a distributed element design. Tight tolerance control is achieved by substituting transmission lines for inductors and specifying capacitor placement carefully. With this approach, good broadband performance is possible.

Since transmission line characteristics are dependent on line widths, dielectric properties and circuit board thickness, glass teflon circuit board is generally selected, as it offers the best tolerance control over the latter two variables. The major drawbacks of glass teflon circuit board are its low dielectric constant and relatively high price. A less expensive alternative, which was used in the construction of the MRF630 amplifier, is G10 printed circuit board. Its lower price coupled with its higher dielectric constant results in a smaller circuit and lower overall cost. The dielectric constant of G10 is not a controlled parameter, yet G10 is consistent enough to be useful for many applications at UHF frequencies.

FIGURE 4



"Mini" clamped mica capacitors were chosen for the matching components in this amplifier design because of their low cost, availability and very high "Q". Mica is an extremely good dielectric and these capacitors, if carefully soldered (minimizing capacitor series lead inductance), boast a higher series reasonant frequency than some chip capacitors.

The use of G10 printed circuit board, "mini" clamped mica capacitors and the MRF630, enhance component repeatability, affordability, and availability.

PERFORMANCE

Broadband circuit performance is displayed in Figure 5 and a typical gain curve is shown in Figure 6. As can be seen, the MRF630 has excellent turn-on characteristics and saturated power capability. The normal gain roll-off above 490 MHz is expected but was minimized by optimizing both input and output impedance matching networks above that frequency. By adding additional matching sections, broadband performance down to 400 MHz could be achieved with respectable input VSWR's.

With the addition of the copper "flange" in the circuit assembly, average device θ_J-HS was limited to 12.3°C/W (dissipated power = 4.0 W, T_C = 60°C). The MRF630 was also mounted directly to the bottom of the printed circuit board, which was placed directly against the heatsink. The θ_J-HS degraded to only 15.6°C/W under the same conditions of power dissipation. If the PC board were "floating" using the same technique, higher θ_J-HS's would be observed. Assuming all circuit components were to be mounted in stripline fashion, allowing the PC board to be mounted directly to the heatsink, adequate heatsinking could be obtained without the addition of the "flange". The copper "flange" method of heatsinking is highly recommended for standard printed circuit boards which are isolated from the chassis heatsink.

An exploded view of the amplifier showing printed circuit board, flange and heatsink is shown in Figure 7. Figure 8 is a circuit schematic including parts list, while Figure 9 shows details of part location on the PC board. Finally, as an aid to duplication of the amplifier described herein, Figure 10 is a 1:1 photo master of the printed circuit board.

FIGURE 5 — Broadband Performance

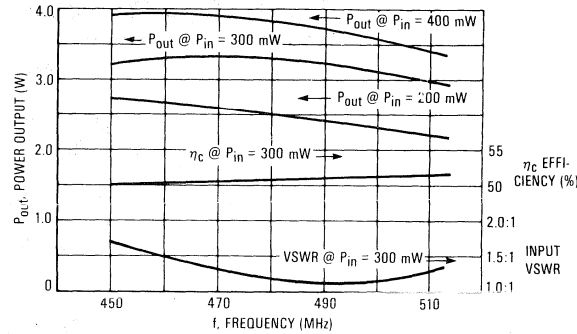
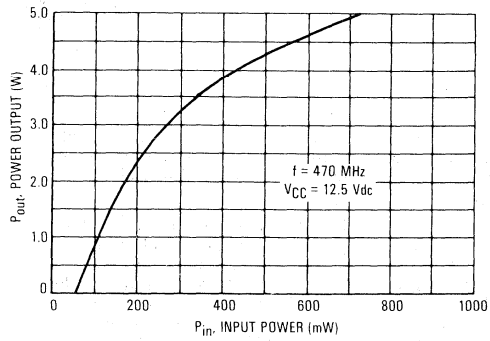


FIGURE 6 — Output Power versus Input Power



SUMMARY

Outlined in this article are methods of assuring the best possible performance from a low cost package; specifically, the MRF630 TO-39. If good construction practices are followed to ensure proper heatsinking and grounding, performance comparable to an SOE can be demonstrated, taking advantage of the cost benefits offered by a TO-39.

6

FIGURE 7 — Exploded View of Amplifier Assembly

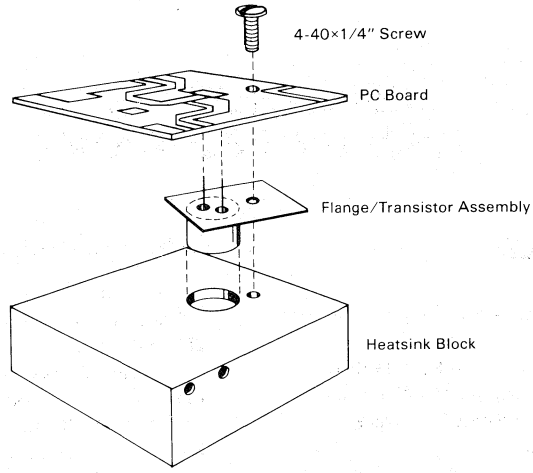
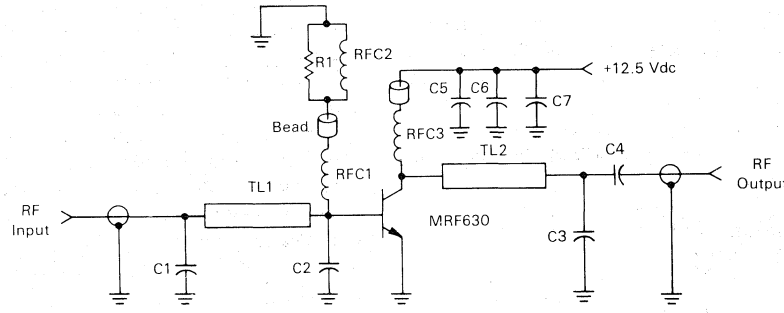


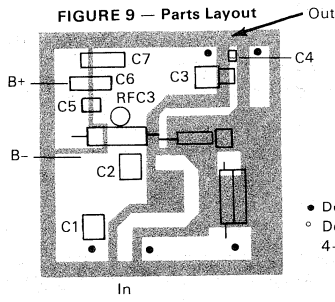
FIGURE 8 — Circuit Schematic and Parts List



C1, C3 — 10 pF Mini-Unelco
C2 — 36 pF Mini-Unelco
C4, C5 — 0.018 μF Chip Capacitor
C6 — 0.1 μF Dipped Capacitor
C7 — 1.0 μF Electrolytic
R1 — 12 Ω — 1/4 W Resistor

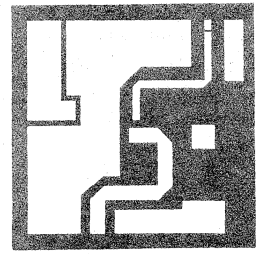
RFC1 — 0.15 μH Mini-Molded Choke
RFC2 — 1.0 μH Mini-Molded Choke
RFC3 — 0.15 μH Molded Choke
TL1 — Transmission Line 0.105 x 1.110" (W x L)
TL2 — Transmission Line 0.053 x 0.987" (W x L)
Board Material — 2 Oz. 0.0625" Epoxy Fiberglass (G-10)

FIGURE 9 — Parts Layout



• Denotes copper eyelets.
° Denotes 4-40 clearance for 4-40 screw mounting.

FIGURE 10 — 1:1 Photo Master



NOTE: The Printed Circuit Board shown is 75% of the original.

6

RELIABILITY AND QUALITY ASSURANCE

QUALITY LEVELS

RF Products are available from Motorola in three quality levels:

1. Industrial/commercial grade, identified by a prefix such as 2N, MRF, or MHW on the part number and tested to a published Corporate, JEDEC, or Proelectron specification.

2. Military grade, built and tested per MIL-S-19500 and identified by a 2N prefix and JAN, JTX, or JTXV suffix.

3. Customer-specified grade with screening, testing, and marking determined by the customer to meet his particular requirements. These may range from a custom-marked industrial/commercial grade product to a product which is subjected to the most stringent tests required for space or submarine applications.

POST-ASSEMBLY PROCESSING

After assembly, a production lot is first sent to Final Test, then is transferred to Quality Assurance.

Final Test Processing

In Final Test, 100% of a lot is processed. This processing may be as simple as electrical testing to a data sheet specification or as complex as a series of mechanical and environmental screening tests preceded and followed by electrical tests.

Quality Assurance Processing

Once in QA, high-rel lots may undergo additional 100% screening prior to testing. Using the popular 2N3866* family as an example, Table 1 compares the varying degrees of preconditioning and screening that are done on the 2N3866, 2N3866JAN, 2N3866JANTX and the 2N3866JTXV transistors. For testing, QA uses test sample groups A, B, and C as defined in MIL-STD 19500. Individual tests are defined in MIL-STD-202, 750, and 883. All lots, including industrial/commercial, receive Group A testing, usually to the same specification which is used by Final Test. In addition to the Group A tests, military and customer-specified high-rel specifications usually require Group B and C tests. Table 2 lists the standard LTPD, sample size and lot acceptance number used for Group A testing of standard products at Motorola. Military and high-rel specifications may call for a tighter Group A sample plan. Tables 3 and 4 list the Group B and C test requirements of the 2N3866JAN and 2N3866-JANTXV specifications.

Special Processing

Three additional tests that may be specified at extra cost by a high-rel customer are:

1. Scanning electron microscope inspection of a wafer.

2. X-ray examination of metal can transistors.

3. Particle Inclusion Noise Detection (PIND) test to detect loose particles trapped in a package.

*The 2N3866 is a 400 MHz, 1.0 Watt NPN silicon transistor mounted in a TO-39 metal can.

TABLE 1 – 100% PRECONDITIONING AND SCREENING (2N3866 Family)

Test	MIL-S-750 Method	Condition	2N3866/JAN	2N3866JTX/V
Final Test				
1. Electrical Tests (Same as Group A)		Go/No Go Remove Rejects	100%	100%
2. High Temperature Storage		200°C, 24 hours	Omit	100%
3. Temperature Cycling	1051	C, 10 cycles	Omit	100%
4. Constant Acceleration	2006	20,000 G Y_1	Omit	100%
5. Hermetic Seal	1071		Omit	100%
Fine Leak		G or H		
Gross Leak		A, B, C, D or F		
6. HT R B		150°C, 48 hr, 24 V	Omit	100%
7. Electrical Tests (Similar to Group A)			Omit	100%
QA				
8. Electrical Tests		Go/No Go	Omit	100%
9. Establish Identity			Omit	100%
10. Electrical Tests	I_{CBO} and h_{FE}		Omit	100%
11. Burn In	with	168 hr, 1.0 W	Omit	100%
12. Electrical Tests	Deltas	PDA = 10%	Omit	100%

TABLE 2 — STANDARD GROUP A SAMPLING PLANS (Discrete Products)

Characteristic (By Subgroup)	LTPD	Sample Size	Accept Number
Discrete Devices			
Visual and Mechanical	3.0	129	1
DC Parameters	3.0	129	1
AC and Temperature Parameters	7.0	55	1
Opens/Shorts	1.75	129	0
Discrete Wafers and Dice			
Visual and Mechanical			
Multipack and Decca Pack (100% Sorted)	10	38	1
Wafer Sales and Vial Package (no 100% Sort)	20	38	4
DC Parameters	10	38	1
AC and Temperature Parameters	15	25	1

6

TABLE 3 – GROUP B TESTS (2N3866 Family)

Inspection or Test	MIL-S-750 Method	Condition	LT P D (Accept No.)	
			2N3866JAN	2N3866JTX/V
Subgroup B-1 Physical Dimensions	2066		20(1)	20(1)
Subgroup B-2 Solderability Temperature Cycling Thermal Shock Hermeticity Fine Leak Gross Leak Moisture Resistance	 2026 1051 1056 1071 1021	 C B IIIa G, or H A, B, C, D or F	15(1)	15(1)
Subgroup B-3 Shock Variable Freq. Vib Constant Acceleration	 2016 2056 2006	 1500 G 20,000 G	15(1)	15(1)
Subgroup B-4 Lead Fatigue	 2036	 E	20(1)	20(1)
Subgroup B-5 Salt Atmosphere	 1041		20(1)	20(1)
Subgroup B-6 High Temperature Storage Life	 1031	 200°C	7(1) (340 hours)	5(1) (1000 hours)
Subgroup B-7 Steady State Operating Life	 1026	 $T_A = 25°C$ $V_{CB} = 25$ V $P_T = 1$ W	7(1) (340 hours)	5(1) (1000 hours)

TABLE 4 – GROUP C TESTS (2N3866 Family)

Inspection or Test	MIL-S-750 Method	Condition	LTPD (Accept No.)	
			2N3866JAN	2N3866JTX/V
Subgroup C-1 Barometric Pressure Thermal Resistance	 1001 3151		10(1)	10(1)
Subgroup C-2 Burnout by Pulsing	 3005		10(1)	10(1)
Subgroup C-3 High Temperature Storage Life	 1031	Extension of B-6 to 1000 hrs	10(1)	–
Subgroup C-4 Steady State Operating Life	 1026	Extension of B-7 to 1000 hrs	10(1)	–

Test Descriptions

The following tests are frequently used for screening, acceptance and evaluation of semiconductor devices.

A. Steady State Operating Life (SSOL)

The purpose of this test is to evaluate the bulk stability of the die and to generate defects resulting from manufacturing aberrations that are manifested as time and stress-dependent failures.

Conditions: T_A = 25°C, PD = max rated power

B. Intermittent Operating Life (IOL)

The purpose of this test is the same as Operating Life in addition to checking the integrity of both the wire and die bonds by means of thermal stressing.

Conditions: T_A = 25°C, PD = max rated power. $T_{(on)}$ = $T_{(off)}$ = 1 min.

C. High Temperature Storage Life

The purpose of this test is to generate time/temperature failure mechanisms and to evaluate long-term storage stability.

Conditions: T_A = 150°C no bias applied

D. High Temperature Reverse Bias (HTRB)

The purpose of this test is to align mobile ions by means of temperature and voltage stresses to form a high-current leakage path between two or more terminals.

Conditions: T_A = 150°C, V_{CB} = 80% max rated V_{CB},

E. High Temperature High Humidity Reverse Bias (H^3TRB)

The purpose of this test is to evaluate the moisture resistance of non-hermetic components. The addition of voltage bias accelerates the corrosive effect after moisture penetration has taken place. With time, this is a catastrophically destructive test.

Conditions: T_A = 85°C, RH = 85%, V_{CB} = 80% max rated V_{CB},

F. Moisture Resistance

The purpose of this test is to evaluate the moisture resistance of components under temperature/humidity conditions typical of tropical environments.

Conditions: Mil-Std-750, Method 1021.

G. Pressure Cooker

The purpose of this test is to evaluate the moisture resistance of non-hermetic components under pressure/temperature conditions.

Conditions: T = 121°C, P = 1 atmosphere (15 psig)

H. Temperature Cycle (Air to Air)

The purpose of this test is to evaluate the ability of the device to withstand both exposure to extreme temperatures and the transition between temperature extremes, and to expose excessive thermal mismatch between materials.

Conditions: Mil-Std-750, Method 1051, −55°C to 150°C, 15 minutes dwell time at each temperature

I. Thermal Shock (Liquid to Liquid)

This test is an accelerated version of temperature cycle.

Conditions: Mil-Std-750, Method 1056, 0°C to 100°C, 15 seconds dwell time at each temperature

J. Terminal Strength

The purpose of this test is to evaluate the ability of the device terminals to withstand the lead forming and tension associated with component installation into a circuit.

Conditions: Mil-Std-750, Method 2036, Condition E.

K. Solderability

The purpose of this test is to determine the solderability of the device terminals.

Conditions: Mil-Std-750, Method 2026.

L. Salt Atmosphere (Corrosion)

The purpose of this test is to accelerate the corrosion effects of an environment in which salt (NaC1) is present.

Conditions: Mil-Std-750, Method 1041

M. Mechanical Stress Tests

Vibration, shock and constant acceleration tests are infrequently used since they rarely generate failures in small-signal transistors. However, they are still specified for acceptance of military product.

HIGH RELIABILITY PROCESSING OF RF TRANSISTORS

I WAFER PROCESSING

After wafers are processed, they are subjected to Motorola visual inspection specifications then probe tested to determine compliance with Group A specifications upon completion. Probe tests include the following: (1) Class Probe — performed to determine device type and yield; (2) Unit Probe each unit is subjected to Group A electrical tests — rejects are inked. Following the class and unit probe tests, the wafer is scribed and broken.

II ASSEMBLY

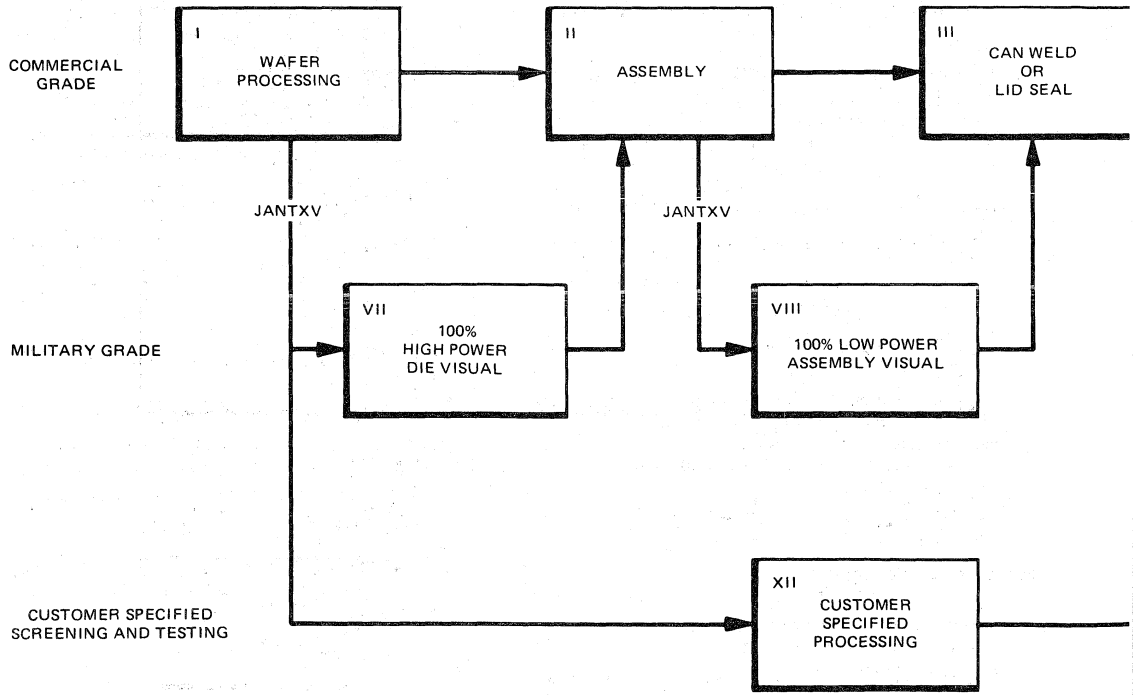
The die are attached to headers and then wire bonded. Wire pull tests are performed by Quality Control inspectors on a sample basis to ensure assembly process controls.

Units are stored in dry air until ready for capping.

III CAN WELD OR LID SEAL

Completed headers are loaded into a vacuum chamber for can weld or processed thru a furnace for metal top attachments on ceramic packages with solder preforms.

PROCESSING AND QUALITY CONTROL FLOW CHART



VII 100% HIGH POWER DIE VISUAL

The high power portion of the inspection is performed to assure good die construction and front metal conditions. Individual reject criteria includes the following: Metallization defects such as scratches, voids, corrosion, adherence, bridging and alignment. Poor die construction conditions such as oxide and diffusion faults are also rejected.

VIII 100% LOW POWER ASSEMBLY VISUAL

The low power visual inspection controls workmanship, i.e., die attachment, internal lead-wire attachment, and package defects. Die attachment inspection includes assuring good adherence, die placement and proper orientation. Internal lead wires must have proper arc and all attachment bonds must be properly placed and in good condition. Package defect inspection includes checking for foreign material, improper construction and cracked glass conditions.

IV FINAL ELECTRICAL TEST

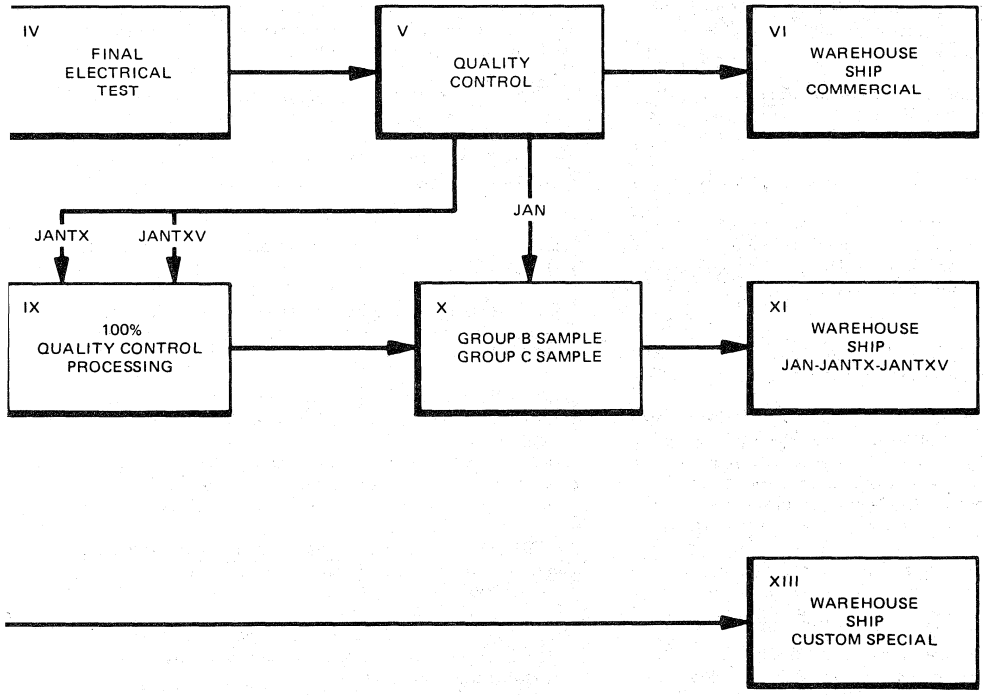
pleted units are selected for a Group A elec- test. Hand screening is performed where ssary. Electrical fallout units and over-runs ıubject to future screening.

V QUALITY CONTROL

Samples are taken for complete electrical analysis of the lot. Group A and B tests are performed on JAN devices. Group A and B tests and 100% processing are performed on JANTX devices. Some devices also require Group C inspection tests.

VI WAREHOUSE

Upon completion, the finished product is ready for shipping. Purchase order requirements are carefully checked again prior to shipping. Overruns are kept for future orders. Warranty tests (Group A) are performed every 24 months on military devices.



IX 100% QUALITY CONTROL

a. High temperature storage
b. High temperature reverse bias
c. Temperature cycling
d. Thermal shock
e. Hermetic seal
f. Acceleration
g. Read & Record parameters
h. Room temperature burn-in

X GROUP B AND GROUP C INSPECTION

Typical Group B Processing (Sample Basis)

a. Physical dimensions
b. Moisture resistance
c. Terminal strength
d. Hermetic seal
e. Solderability
f. Vibration fatigue
g. 1000 hr. storage life
h. 1000 hr. operating life

Typical Group C Processing (Sample Basis)

a. ac parameters
b. Barometric pressure
c. Burn out pulsing
d. Resistance to solvents

6

Glossary of Reliability and Quality Terms

Acceptable Quality Level (AQL) — A measure of quality for which a given lot will be accepted most of the time. This is usually established at a probability of acceptance equal to 95%. It is referred to as the producer's risk because the probability of rejecting a good lot is 5%.

Acceptance Number (Ac) — The largest number of defectives in an inspection sample under consideration that will permit acceptance of the lot.

Acceptance Tests — Tests to determine conformance to specification requirements as a basis for lot acceptance.

Average Outgoing Quality (AOQ) — The average quality of outgoing product after 100% screening of rejected lots. This is usually measured in parts per million (PPM).

Average Outgoing Quality Limit (AOQL) — The maximum average outgoing quality that is possible for a given sampling plan.

Defect — Any deviation of a device that does not conform to specified requirements. One device may contain more than one defect.

Defective — A device which contains one or more defects.

Double Sampling — Sampling inspection in which the inspection of the first sample leads to a decision to accept, to reject, or to take a second sample. The inspection of a second sample, when required, always leads to a decision to accept or to reject.

Failure — The inability of a device to perform a specified function within previously-established limits.

Failure Rate — The statistical probability of a failure occurring within a stated period of time. For electronic components it is usually assumed that failures follow an exponential distribution, in which case the failure rate over any stated period of time is constant. The failure rate of semiconductor devices is generally given in percent per thousand hours.

Infant Mortality — Premature failures occurring at a failure rate substantially greater than that observed during subsequent life prior to wear-out.

Lot — A group of devices from which samples are drawn and inspected to determine compliance with acceptance criteria (inspection lot).

Lot Tolerance Percent Defective (LTPD) — A measure of quality for which a given lot will be rejected most of the time. This is usually established at a probability of acceptance equal to 10%. It is referred to as the consumer's risk because the probability of accepting a bad lot is 10%.

Mean Time Between Failures (MTBF) — The total measured operating time of a group of equipments divided by the total number of failures of a repairable equipment. In the case of an exponential failure distribution, this ratio is the reciprocal of failure rate.

Operating Characteristic Curve (OC curve) — A graph of the probability of acceptance as a function of the lot quality or process average quality, whichever is applicable.

Percent Defective — The number of defective devices in a lot divided by the total number of devices in that lot, multiplied by 100.

Probability of Acceptance (Pa) — The fractional probability that a lot will be accepted, usually expressed as a decimal.

Process Average Quality — The expected quality of product from a given process, usually estimated from first sample results of previous inspection lots.

Quality — A measure of the degree to which a product conforms to specification and workmanship requirements.

Rejection Number (Re) — The smallest number of defectives in an inspection sample under consideration that will prevent acceptance of the lot.

Reliability — A measure of the performance of a product over a specified period of time.

Sample — One or more devices selected at random from an inspection lot to represent that lot for acceptance purposes.

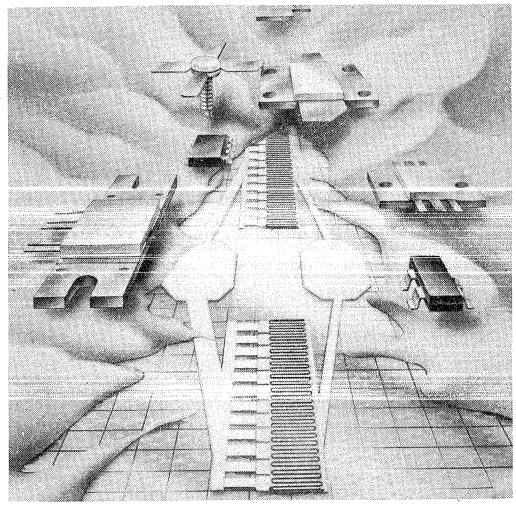
Sampling Plan — A specific plan which defines the sample size and the criteria for accepting or rejecting a lot.

Screening Tests — Tests employing nondestructive environmental, electrical, thermal and/or mechanical stresses, for the purpose of identifying anomalous devices.

Single Sampling — Sampling inspection in which a decision to accept or to reject is reached after the inspection of a single sample.

Wearout Failures — Those failures which occur as a result of deterioration processes and whose probability of occurrence increases with time.

100% Inspection — Inspection of every device, in which each device is accepted or rejected individually for the characteristic concerned, on the basis of its own inspection only.



1 Index and Cross-Reference

2 Selector Guide

3 Transistors

4 Amplifiers

5 Tuning, Hot Carrier and PIN Diodes

6 Technical Information

Transistor Design

Application Notes

Reliability and Quality Assurance

Literature Distribution Centers:

USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036

EUROPE: Motorola Ltd.; European Literature Center; 88 Tanners Drive-Blakelands Milton Keynes, MK145BP England

ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; P.O. Box 80300; Cheung Sha Wan Post Office; Kowloon Hong Kong